TPS22960 Low-Input Voltage, Dual-Load Switch With Controlled Turnon

1 Features

- Integrated Dual-Load Switch
- Input Voltage Range: 1.62 V to 5.5 V
- Low ON-State Resistance
  - r_{ON} = 342 mΩ at V_{IN} = 5.5 V
  - r_{ON} = 435 mΩ at V_{IN} = 3.3 V
  - r_{ON} = 523 mΩ at V_{IN} = 2.5 V
  - r_{ON} = 737 mΩ at V_{IN} = 1.8 V
- 500-mA Maximum Continuous Switch Current
- Low Quiescent Current and Shutdown Current
- Controlled Switch Output Rise Time: 75 µs or 660 µs
- Integrated Quick Output Discharge Transistor
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- 8-Pin SOT (DCN) Package: 3 mm × 3 mm
- 8-Pin UQFN (RSE) Package: 1.5 mm × 1.5 mm

2 Applications

- GPS Devices
- Cell Phones/PDAs
- MP3 Players
- Digital Cameras

3 Description

The TPS22960 is a small low-r_{ON} dual-channel load switch with controlled turnon. The devices contain two P-channel MOSFETs that can operate over an input voltage range of 1.62 V to 5.5 V. Each switch is independently controlled by on/off inputs (ON1 and ON2), which are capable of interfacing directly with low-voltage control signals. In TPS22960 a 85-Ω on-chip load resistor is added for quick discharge when the switch is turned off.

The rise time (slew-rate) of the device is internally controlled in order to avoid inrush current, and it can be slowed down if needed using the SR pin: at 3.3 V, TPS22960 features a 75-µs rise time with the SR pin tied to ground and 660-µs with the SR pin tied to high.

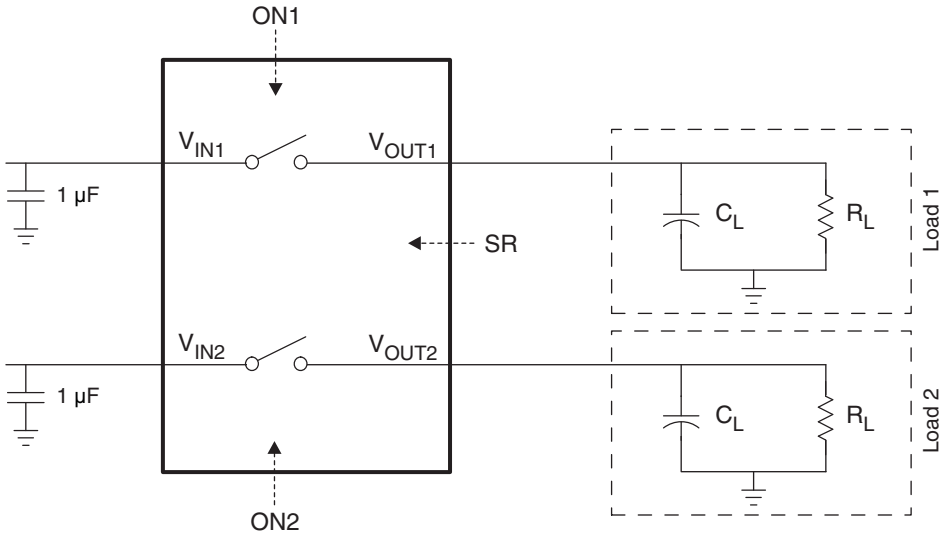
The TPS22960 is available in a space-saving 8-pin UQFN package and in an 8-pin SOT package. It is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22960	SOT (8)	2.90 mm × 1.63 mm
	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2015) to Revision D — **Page**

- Made changes to *Application Information* ... 1

Changes from Revision B (August 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated the *Thermal Information* table to remove 220°C/W and 116°C/W from the junction-to-ambient thermal resistance, and 123°C/W and 60°C/W from the junction-to-case (top) thermal resistance ... 4
- Changed values > 100°C/W in the *Thermal Information* table to contain only 3 significant figures ... 4

Changes from Revision A (August 2011) to Revision B — **Page**

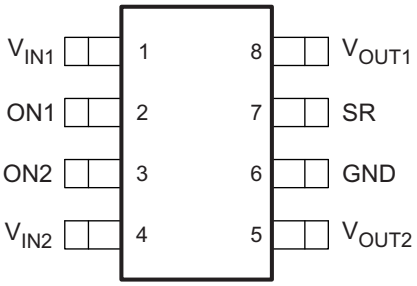
- Clarified text in the *Description* ... 1
- Added T_J to the *Absolute Maximum Ratings* table ... 3
- Updated Table 2 in *Device Functional Modes* ... 13

Changes from Original (April 2009) to Revision A — **Page**

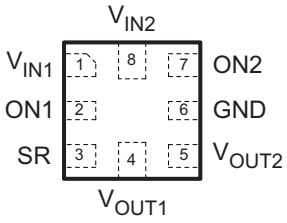
- Changed r_{ON} values for V_{INX} = 1.8 V (25°C) From: Typ 714, Max 855 To: Typ 737, Max 1100 ... 5
- Changed r_{ON} values for V_{INX} = 1.8 V (Full) From: Max 995 To: Max 1300 ... 5
- Changed r_{ON} values for V_{INX} = 1.62 V (25°C) From: Typ 830, Max 950 To: Typ 848, Max 1300 ... 5
- Changed r_{ON} values for V_{INX} = 1.62 V (Full) From: Max 1100 To: Max 1500 ... 5

5 Pin Configuration and Functions

DCN PACKAGE
8-PIN SOT
TOP VIEW



RSE PACKAGE
8-PIN UQFN
TOP VIEW



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT	UQFN		
V_{IN1}	1	1	I	Switch 1 input; bypass this input with a ceramic capacitor to GND
ON1	2	2	I	Switch 1 control input, active high. Do not leave floating.
ON2	3	7	I	Switch 2 control input, active high. Do not leave floating.
V_{IN2}	4	8	I	Switch 2 input; bypass this input with a ceramic capacitor to GND
V_{OUT2}	5	5	O	Switch 2 output
GND	6	6	—	Ground
SR	7	3	I	Slew rate control pin. SR = GND translates into a 75-µs rise time; SR = high translates into a 660-µs rise time
V_{OUT1}	8	4	O	Switch 1 output

6 Specifications

6.1 Absolute Maximum Ratings

(see (1))

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage		V_{IN} + 0.3	V
V_{ON}	Input voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		0.5	A
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		1.62	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V	1.5	5.5	V
		V_{INx} = 1.62 V to 3.0 V	1.4	5.5	
V_{IL}	Low-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V		0.5	V
		V_{INx} = 1.62 V to 3.0 V		0.4	
C_{IN}	Input capacitor		1 (1)		µF

(1) See *Application Information*

6.4 Thermal Information

THERMAL METRIC (1)		TPS22960		UNIT
		DCN (SOT)	RSE (UQFN)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	254	124	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	181	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	178	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Electrical Characteristics

V_{IN} = 1.62 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current (each switch)	I_{OUTx} = 0, V_{INx} = V_{ON}	V_{INx} = 5.5 V	Full		0.64	2	µA
			V_{INx} = 3.3 V	Full		0.35	1.2	
			V_{INx} = 2.5 V	Full		0.24	0.8	
			V_{INx} = 1.8 V	Full		0.15	0.5	
$I_{IN(OFF)}$	OFF-state supply current (each switch)	V_{ON} = GND, V_{OUTx} = Open	V_{INx} = 5.5 V	Full		0.47	3.6	µA
			V_{INx} = 3.3 V	Full		0.25	1.8	
			V_{INx} = 2.5 V	Full		0.18	1.3	
			V_{INx} = 1.8 V	Full		0.11	0.9	
r_{ON}	ON-state resistance (each switch)	I_{OUT} = –200 mA	V_{INx} = 5.5 V	25°C		342	400	mΩ
				Full			465	
			V_{INx} = 3.3 V	25°C		435	500	
				Full			595	
			V_{INx} = 2.5 V	25°C		523	620	
				Full			720	
			V_{INx} = 1.8 V	25°C		737	1100	
				Full			1300	
			V_{INx} = 1.62 V	25°C		848	1300	
				Full			1500	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		85	120	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 1.62 V to 5.5 V or GND		Full			0.25	µA

(1) Typical values are at T_A = 25°C.

6.6 Switching Characteristics

V_{IN} = 3.3 V, T_A = 25°C, RL_CHIP = 85 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		635		µs
			SR = GND		67		
t_{OFF}	Turn-OFF time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.2		
t_r	V_{OUT} rise time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		660		µs
			SR = GND		75		
t_f	V_{OUT} fall time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.5		

(1) Typical values are at the specified V_{IN} = 3.3 V and T_A = 25°C

6.7 Typical DC Characteristics

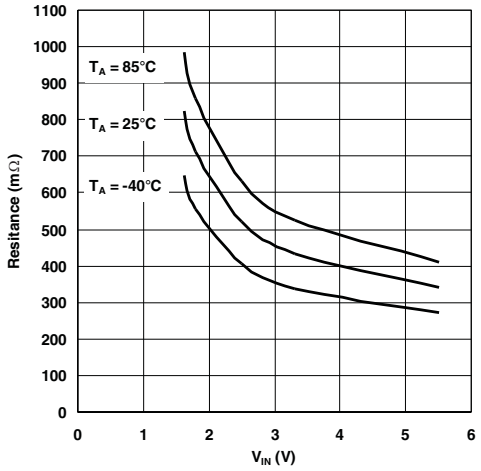


Figure 1. ON Resistance vs Input Voltage

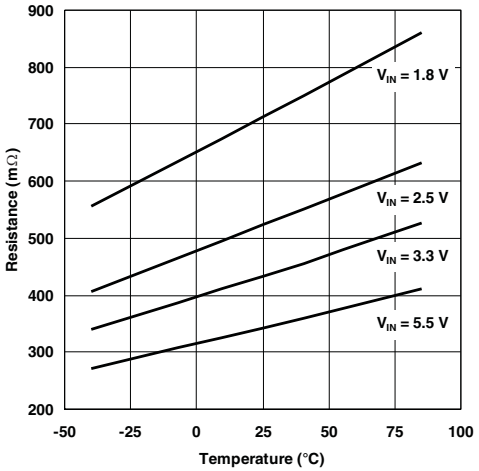


Figure 2. ON Resistance vs Temperature

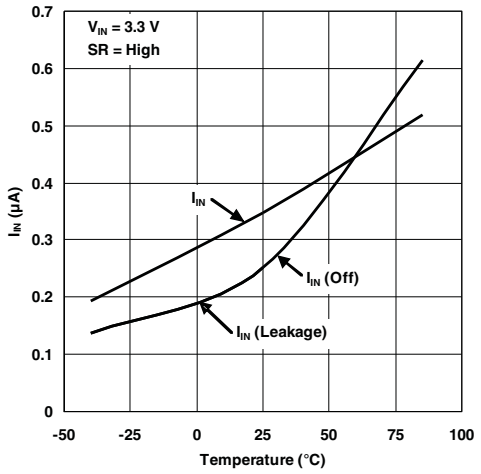


Figure 3. Quiescent Current vs Temperature

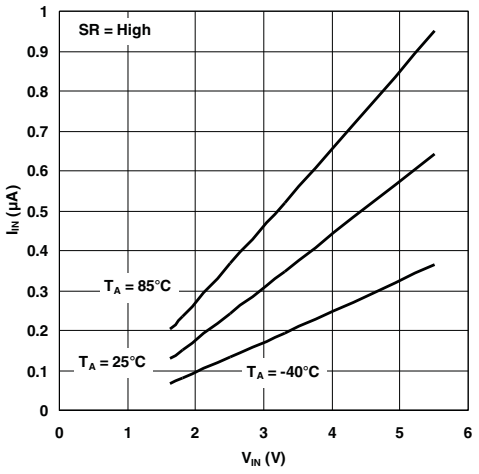


Figure 4. Quiescent Current vs Input Voltage

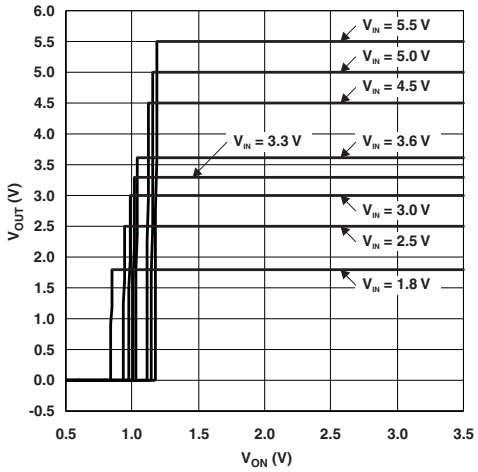


Figure 5. ON Threshold

6.8 Typical Switching Characteristics

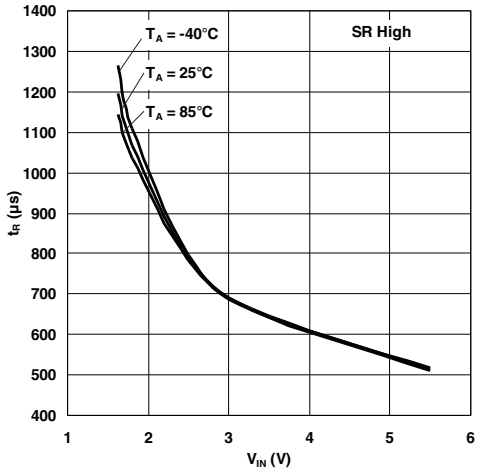


Figure 6. Rise Time vs Input Voltage

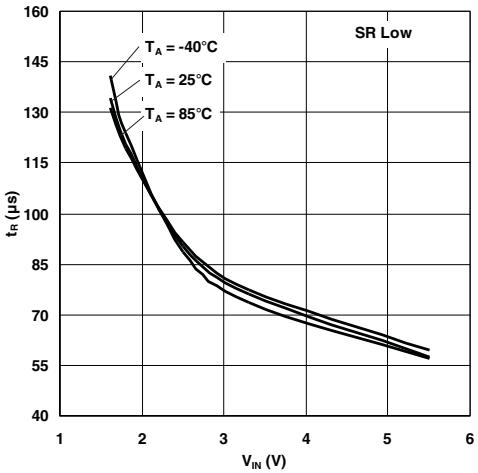


Figure 7. Rise Time vs Input Voltage

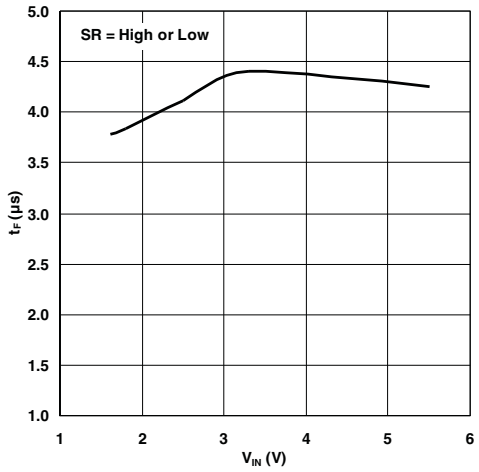


Figure 8. Fall Time vs Input Voltage

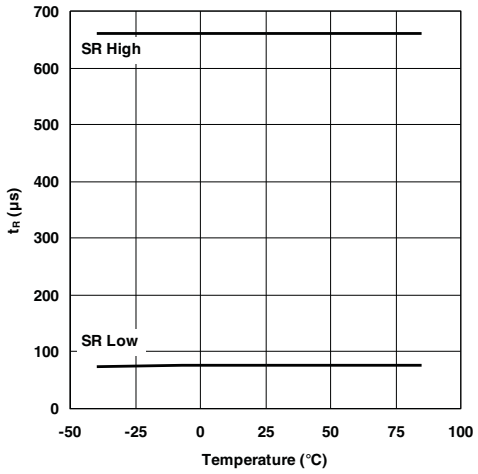


Figure 9. Rise Time vs Temperature

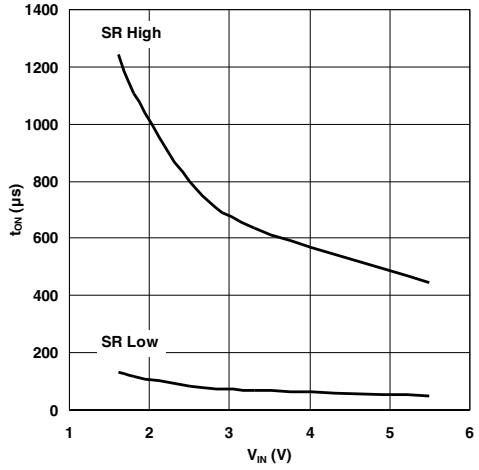


Figure 10. On Time vs Input Voltage

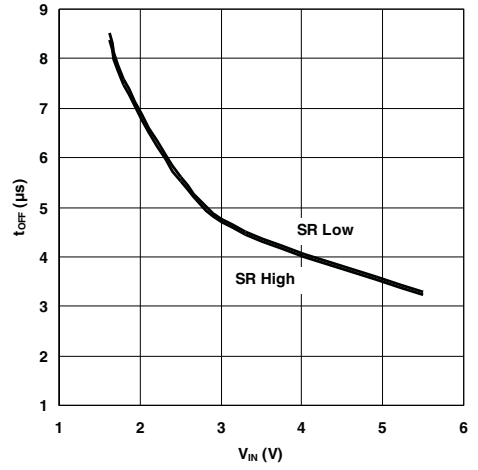


Figure 11. Off Time vs Input Voltage

Typical Switching Characteristics (continued)

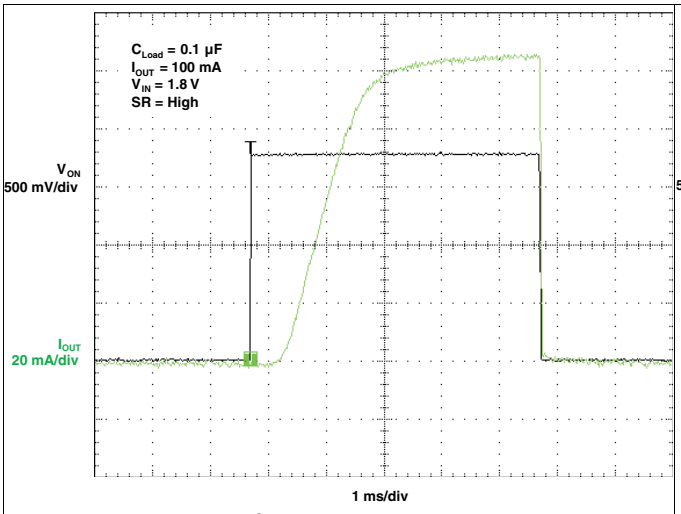


Figure 12. t_{ON} Response

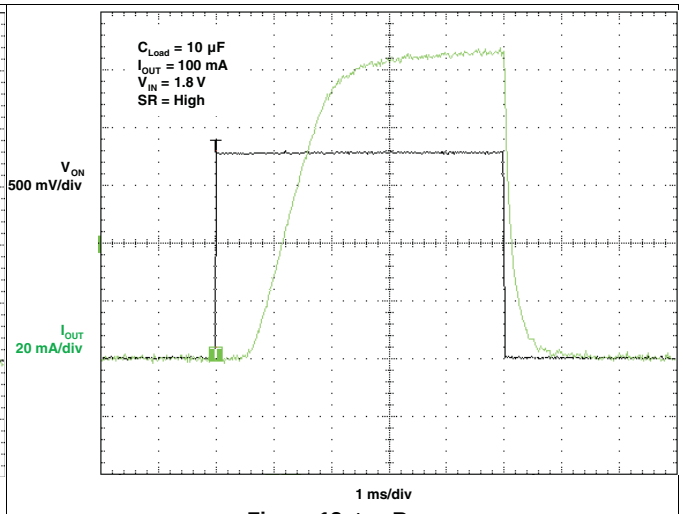


Figure 13. t_{ON} Response

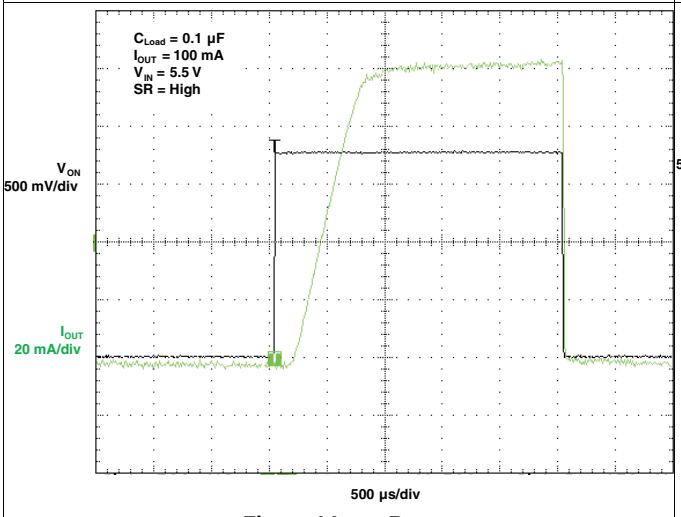


Figure 14. t_{ON} Response

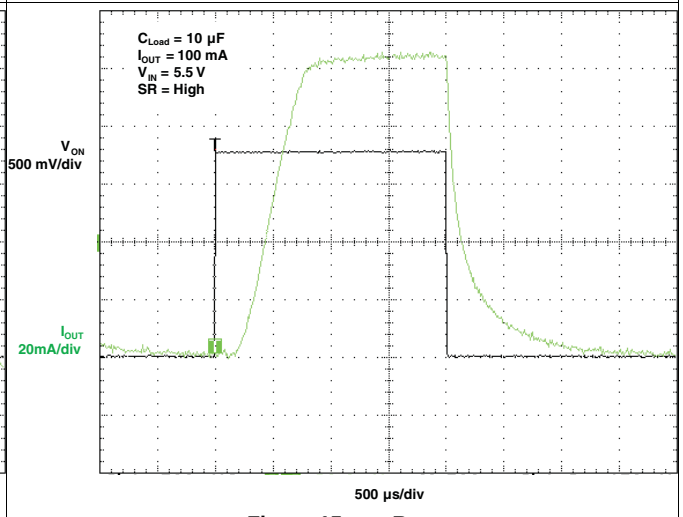


Figure 15. t_{ON} Response

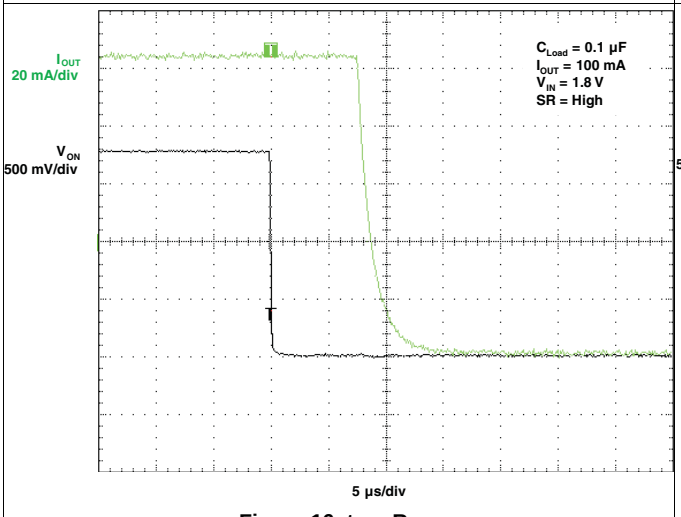


Figure 16. t_{OFF} Response

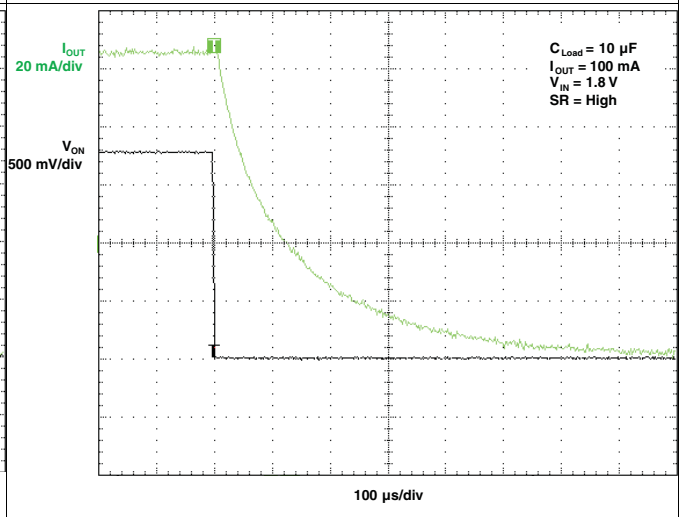


Figure 17. t_{OFF} Response

Typical Switching Characteristics (continued)

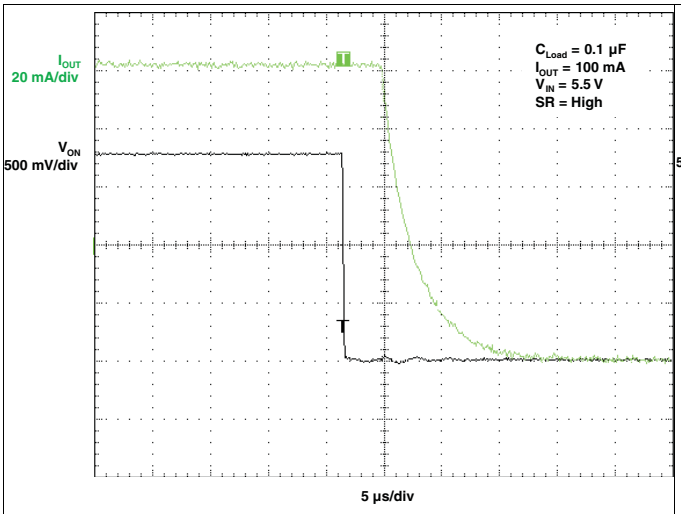


Figure 18. t_{OFF} Response

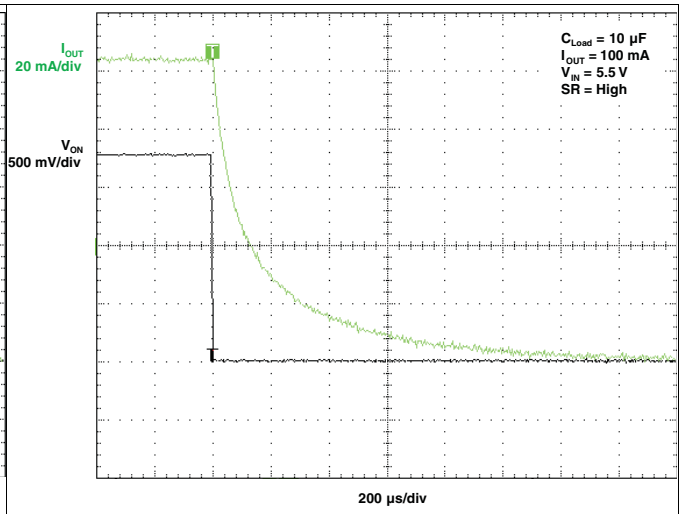


Figure 19. t_{OFF} Response

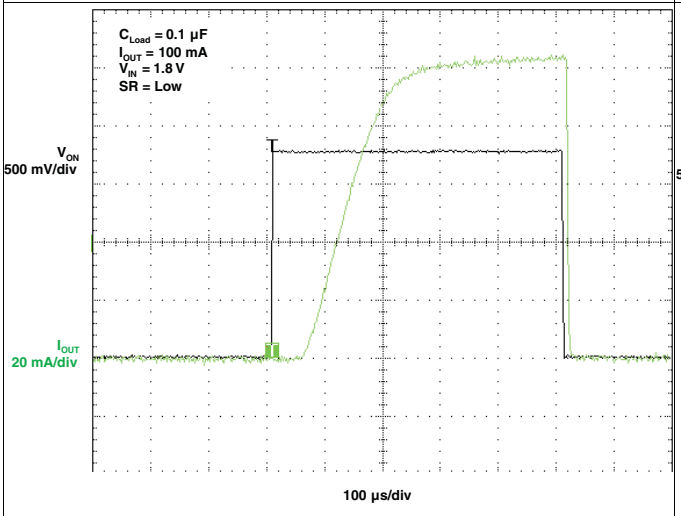


Figure 20. t_{ON} Response

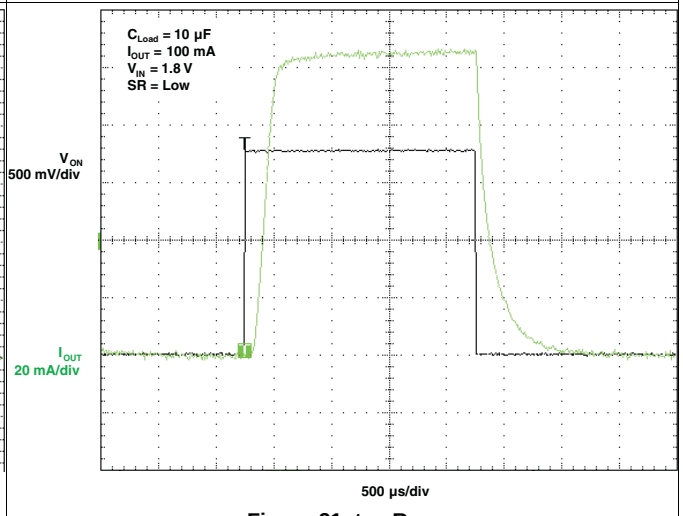


Figure 21. t_{ON} Response

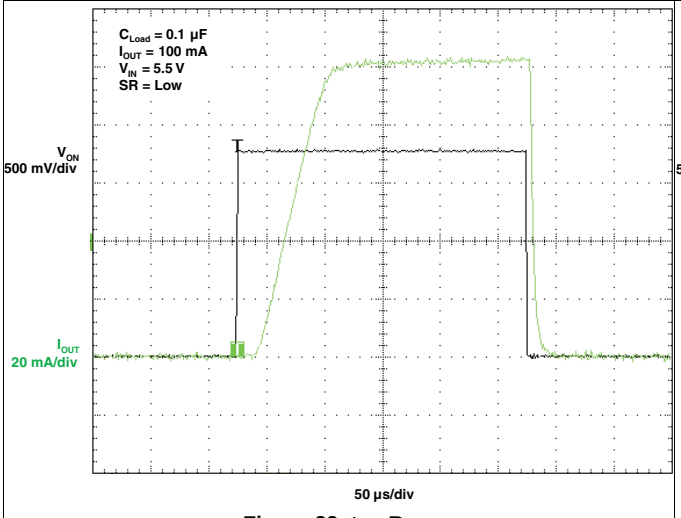


Figure 22. t_{ON} Response

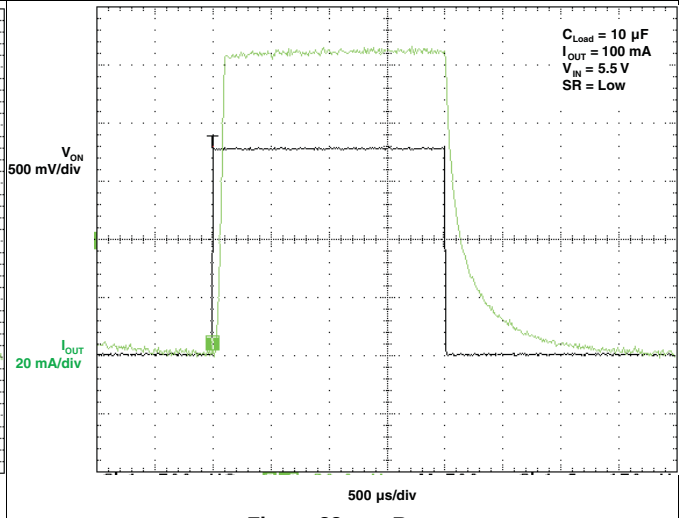


Figure 23. t_{ON} Response

Typical Switching Characteristics (continued)

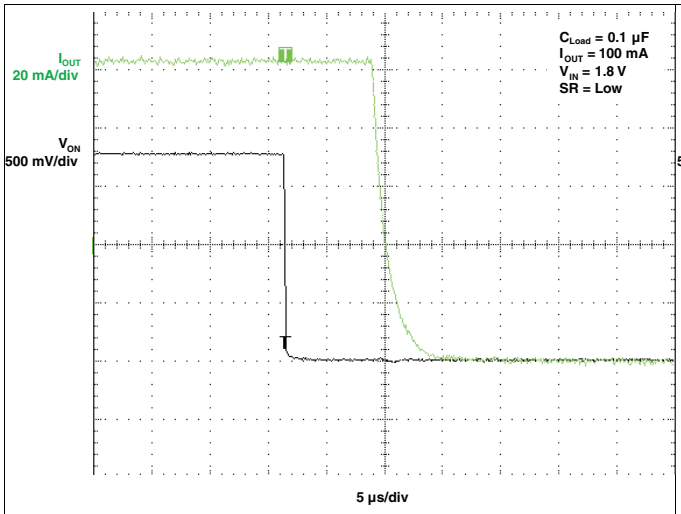


Figure 24. t_{OFF} Response

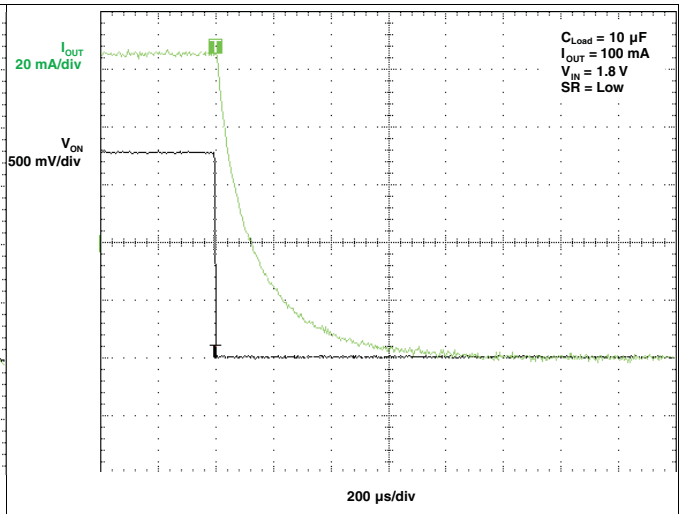


Figure 25. t_{OFF} Response

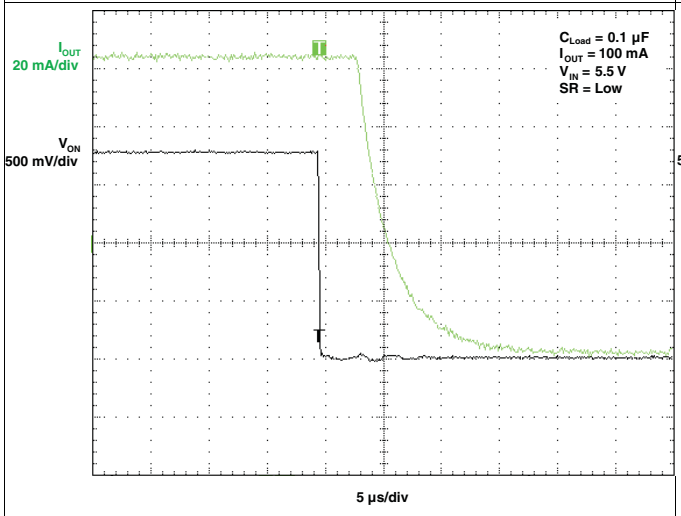


Figure 26. t_{OFF} Response

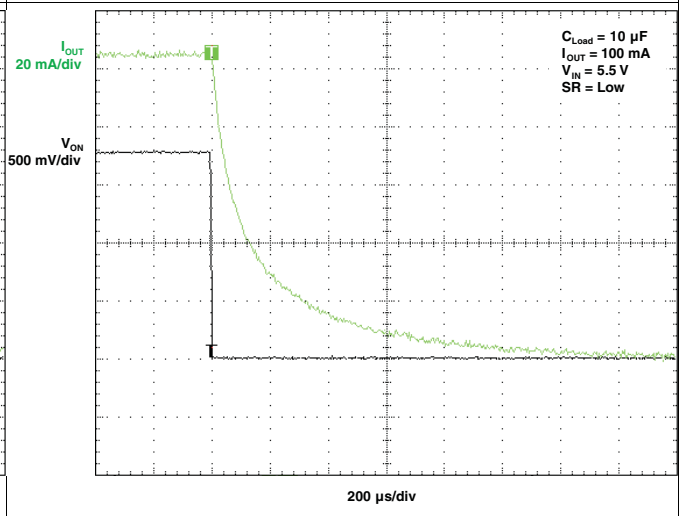
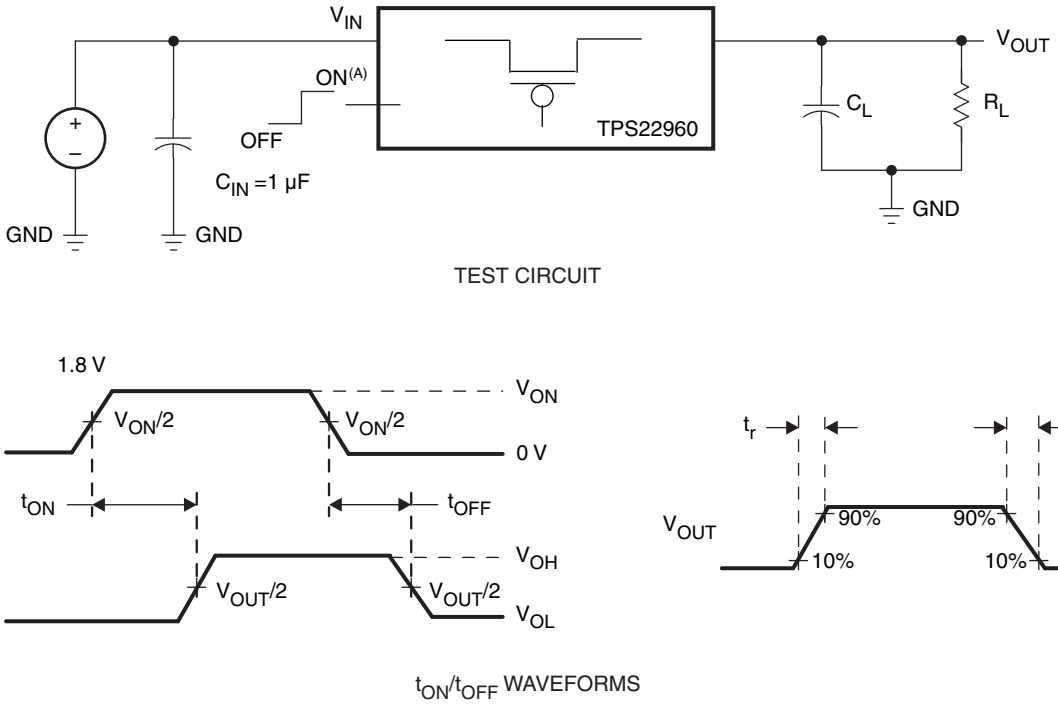


Figure 27. t_{OFF} Response

7 Parameter Measurement Information



A. t_{rise} and t_{fall} of the control signal is 100 ns.

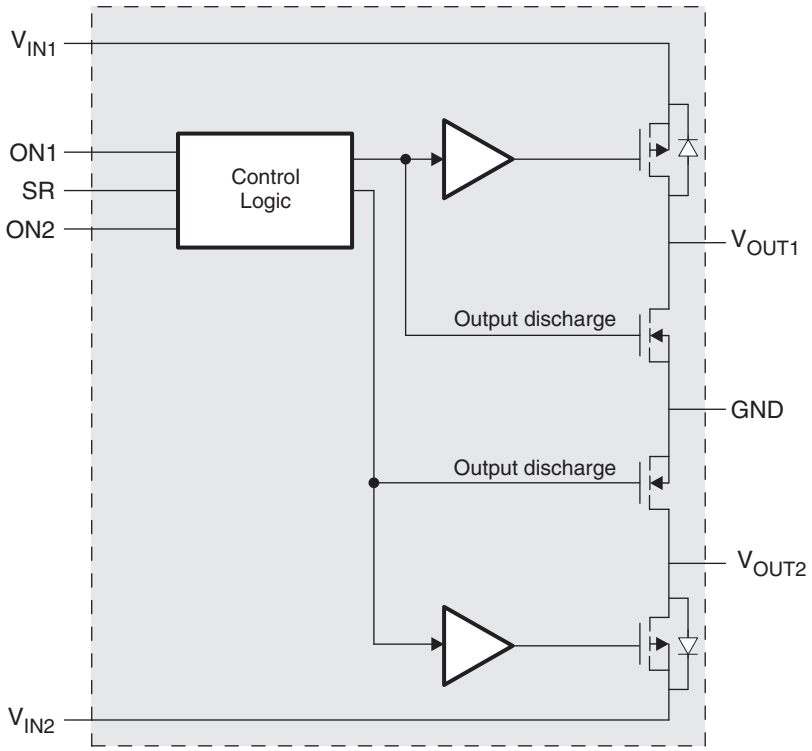
Figure 28. Test Circuit and t_{ON}/t_{OFF} Waveforms

8 Detailed Description

8.1 Overview

The TPS22960 is a dual-channel load switch. The two channels can be independently controlled using the ONx pins. Each channel has an 85-Ω quick discharge resistance from V_{OUTX} to GND when disabled. A single control pin (SR) is used to set the slew rate for both channels..

8.2 Functional Block Diagram



8.3 Feature Description

This section will discuss the features of the TPS22960 which have been summarized in Table 1.

Table 1. Feature Summary

DEVICE	r_{ON} AT 3.3 V (TYP)	SLEW RATE AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE(1)	MAX OUTPUT CURRENT	ENABLE
TPS22960	435 mΩ	75 µs with SR = low 660 µs with SR = high	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through an 85-Ω resistor, preventing the output from floating.

8.3.1 Output Slew Rate (SR) Control

The slew rate (rise time) of the device is internally controlled in order to avoid inrush current, and it can be slowed down if needed using the SR pin. At 3.3 V, TPS22960 features a 75-µs rise time with the SR pin tied to ground, and a 660-µs rise time with the SR pin tied high. Both channels will have the same slew rate set by the SR pin.

8.3.2 Quick Output Discharge (QOD)

Each channel of the TPS22960 includes an independent QOD feature. When the channel is disabled, a discharge resistor is connected between VOUTx and GND. This resistor has a typical value of 85 Ω and prevents the output from floating while the switch is disabled.

8.4 Device Functional Modes

Table 2. Configurable Logic Function Table

ONx	V_{INx} TO V_{OUTx}	V_{OUTx} TO GND
L	OFF	ON
H	ON	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state, as long as there is no fault. ON is active HI and has a low threshold, making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

9.1.2 Input Capacitor

To limit voltage drop or voltage transients, sufficient capacitance needs to be placed on the input side of the load switch (from V_{IN} to GND). In most cases, a 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. However, when switching heavy capacitive loads, higher values of C_{IN} may be needed to prevent the system supply voltage from dropping.

9.1.3 Output Capacitor

The integral body diode in the PMOS switch will allow reverse current flow if V_{OUT} exceeds V_{IN}. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} if the system supply is removed. In the case where the system supply could be removed and reverse current is a concern, a C_{IN} greater than C_L is recommended.

9.2 Typical Application

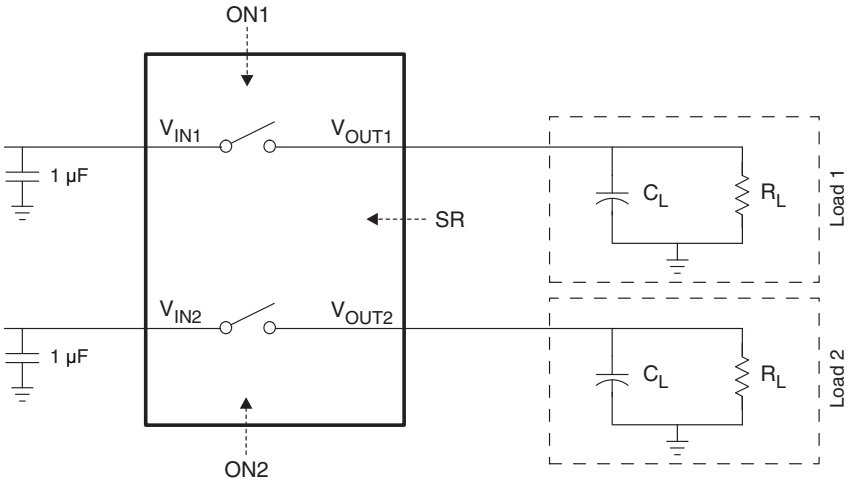


Figure 29. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use input parameters in Table 3.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
C_L	22 µF
Maximum acceptable inrush current	200 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (in this example, 3.3 V). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times dV / dt \quad (1)$$

Where:

C = output capacitance

dV = output voltage

dt = rise time

The TPS22960 offers selectable rise time control for V_{OUT}. This feature allows the user to control the inrush current during turnon. Equation 1 can be used to find the required rise time to limit the inrush current to the design requirements

$$200\ \text{mA} = 22\ \mu\text{F} \times (3.3\ \text{V} \times 80\%) / dt \quad (2)$$

$$dt = 290\ \mu\text{s} \quad (4)$$

To ensure an inrush current of less than 200 mA, SR must be set high for a rise time greater than 290 µs. The following application curves show the different inrush for each SR setting in this design example.

9.2.3 Application Curves

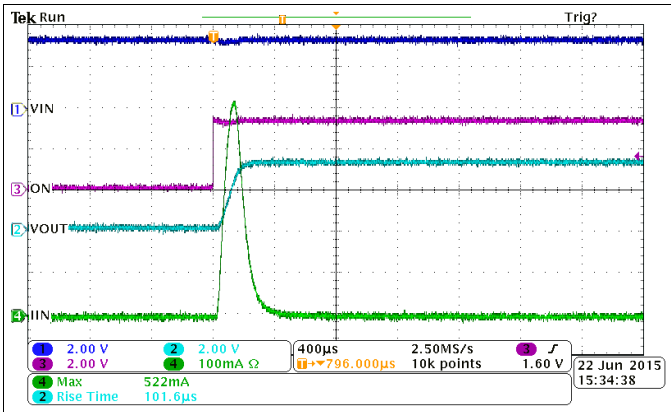


Figure 30. Inrush Current with SR = Low

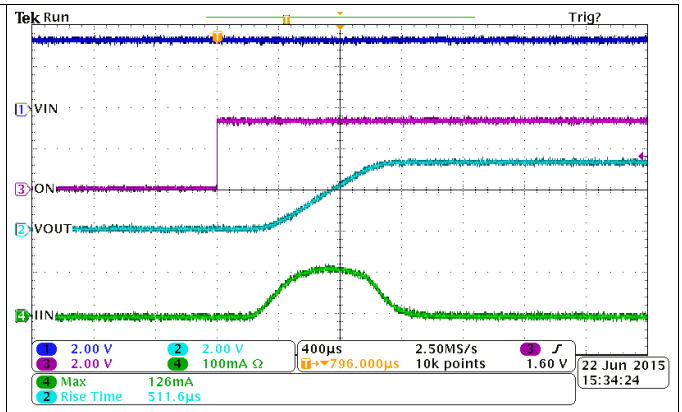


Figure 31. Inrush Current with SR = High

10 Power Supply Recommendations

The device is designed to operate from an input voltage range of 1.62 V to 5.5 V. The power supply should be well-regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input

The requirements for larger input capacitance can be mitigated by selecting the slower slew rate +SR=high. This will cause the load switch to turn on more slowly and limit the inrush current.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VI_N, V_{OUT}, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

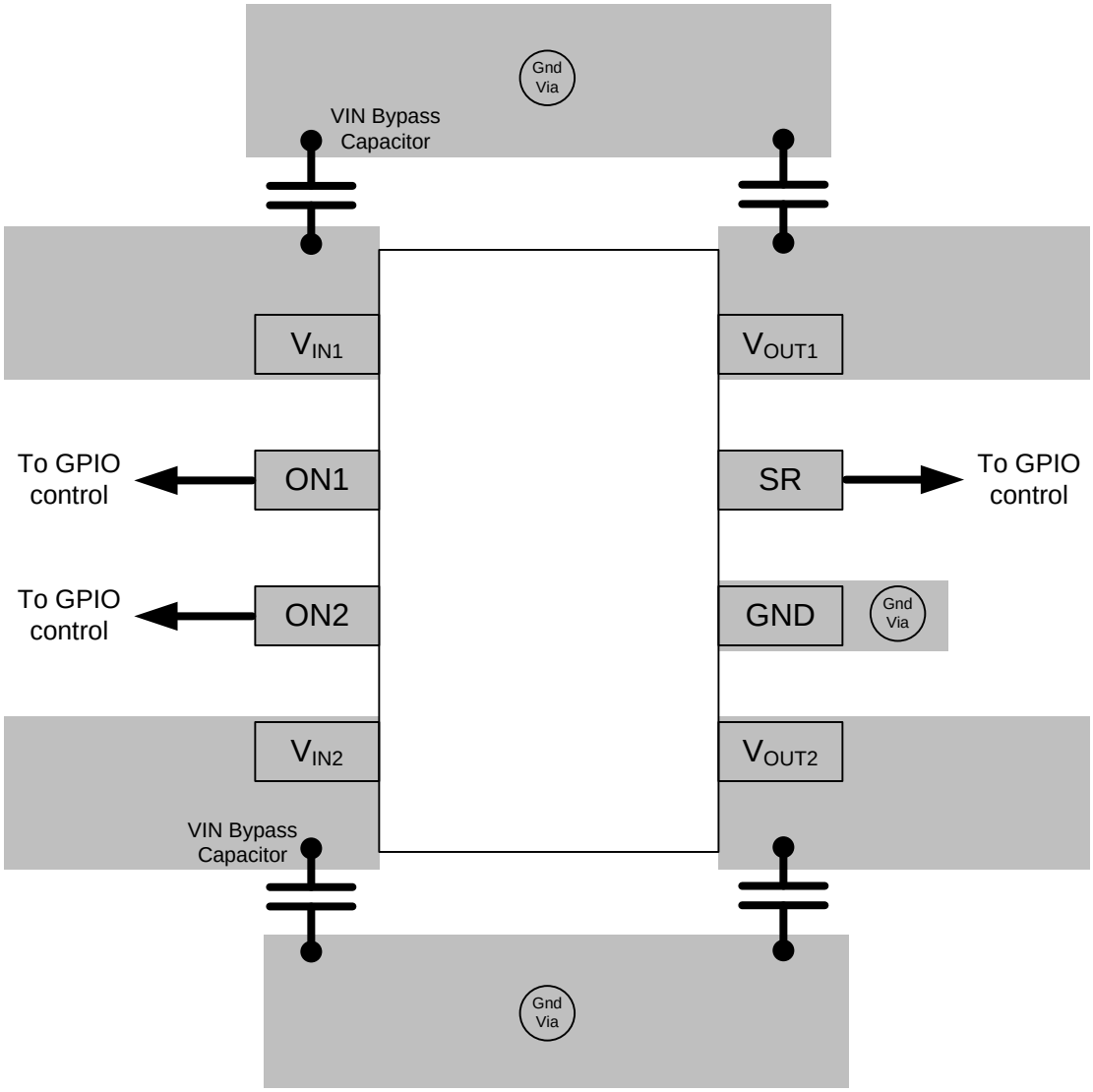


Figure 32. DCN Package Layout

Layout Example (continued)

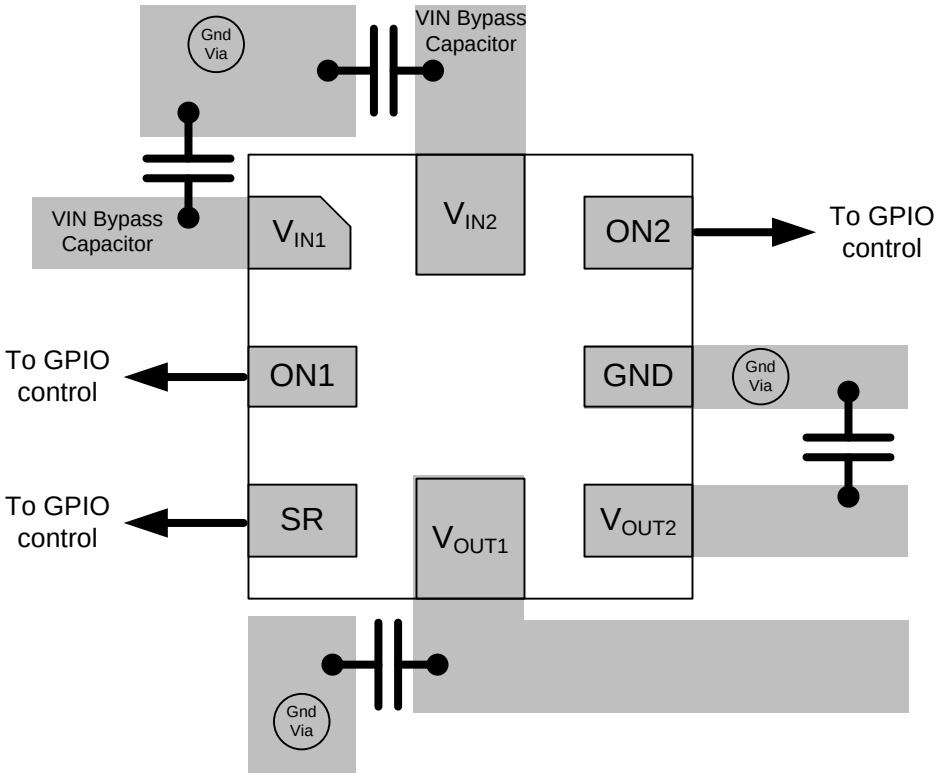


Figure 33. RSE Package Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

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All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22960DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO ~ NFRR)	Samples
TPS22960RSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	Samples
TPS22960RSET	ACTIVE	UQFN	RSE	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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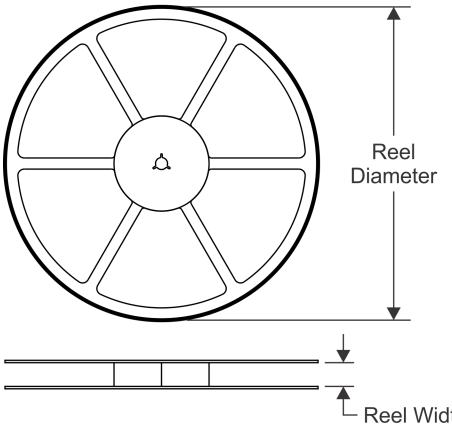
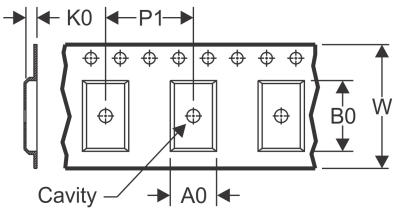
TAPE AND REEL INFORMATION

REEL DIMENSIONS

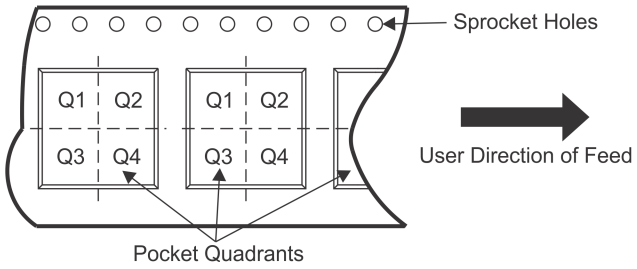


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

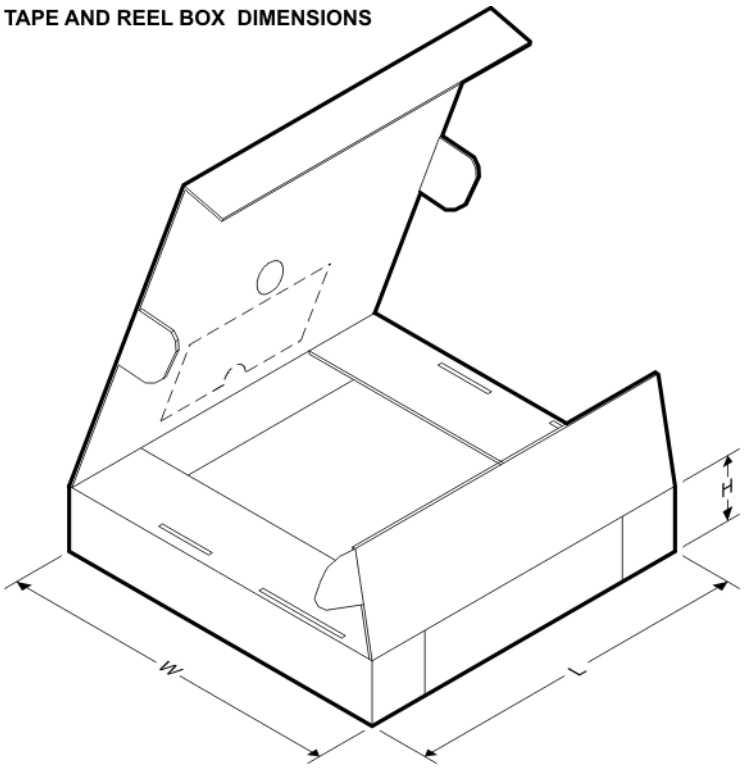
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22960DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS22960DCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22960RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22960RSET	UQFN	RSE	8	250	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

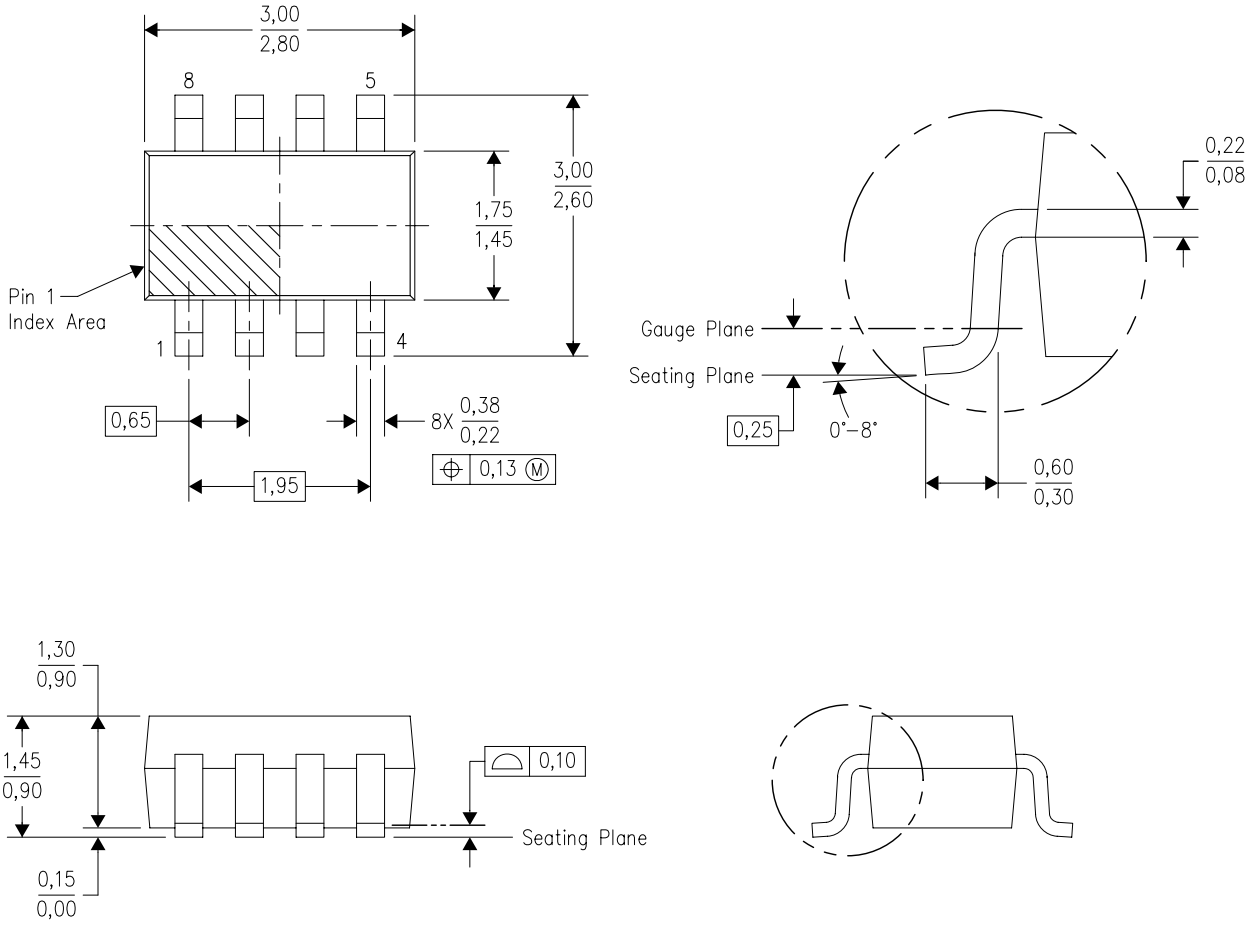
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

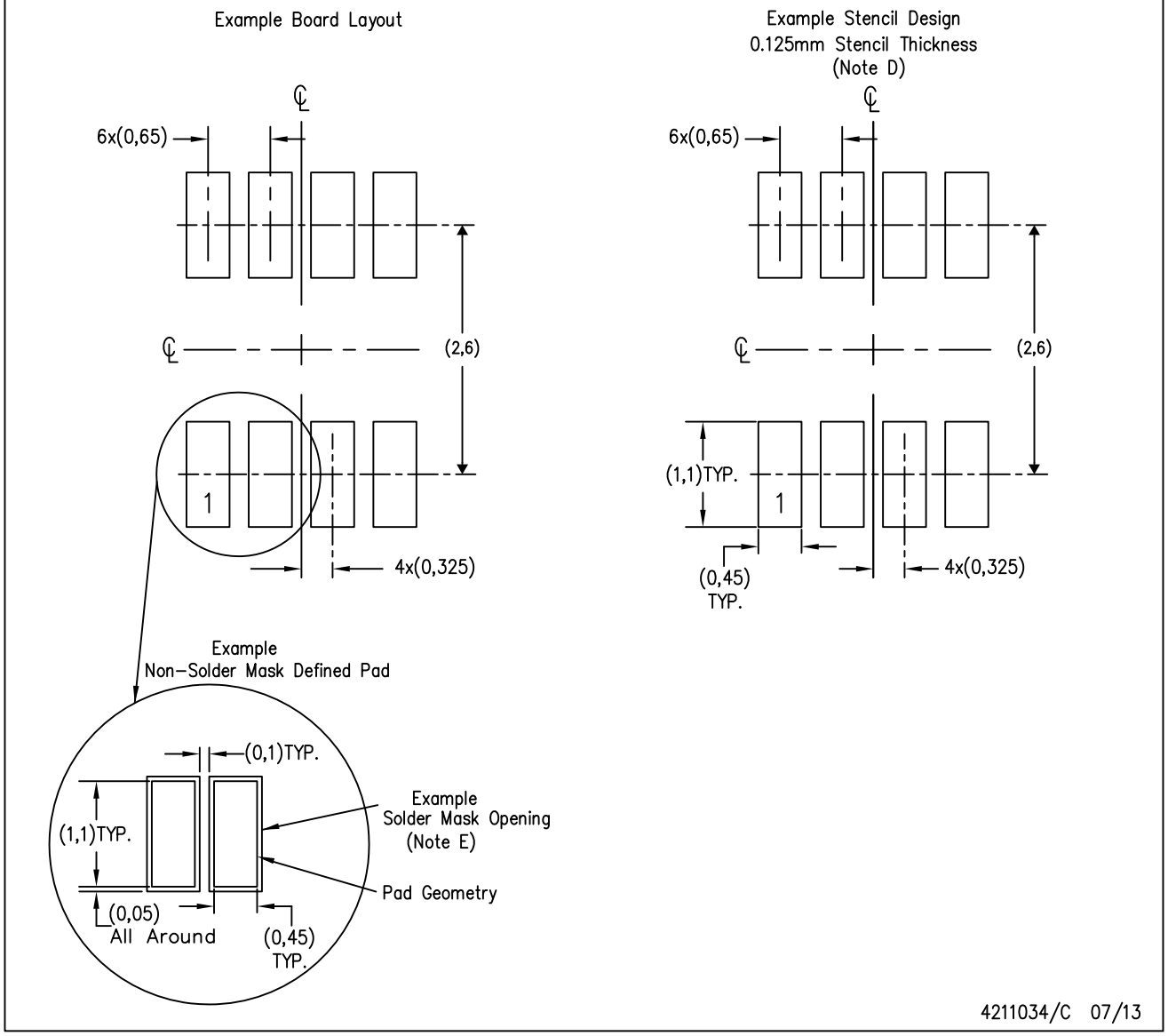
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22960DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPS22960DCNR	SOT-23	DCN	8	3000	203.0	203.0	35.0
TPS22960RSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22960RSET	UQFN	RSE	8	250	202.0	201.0	28.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



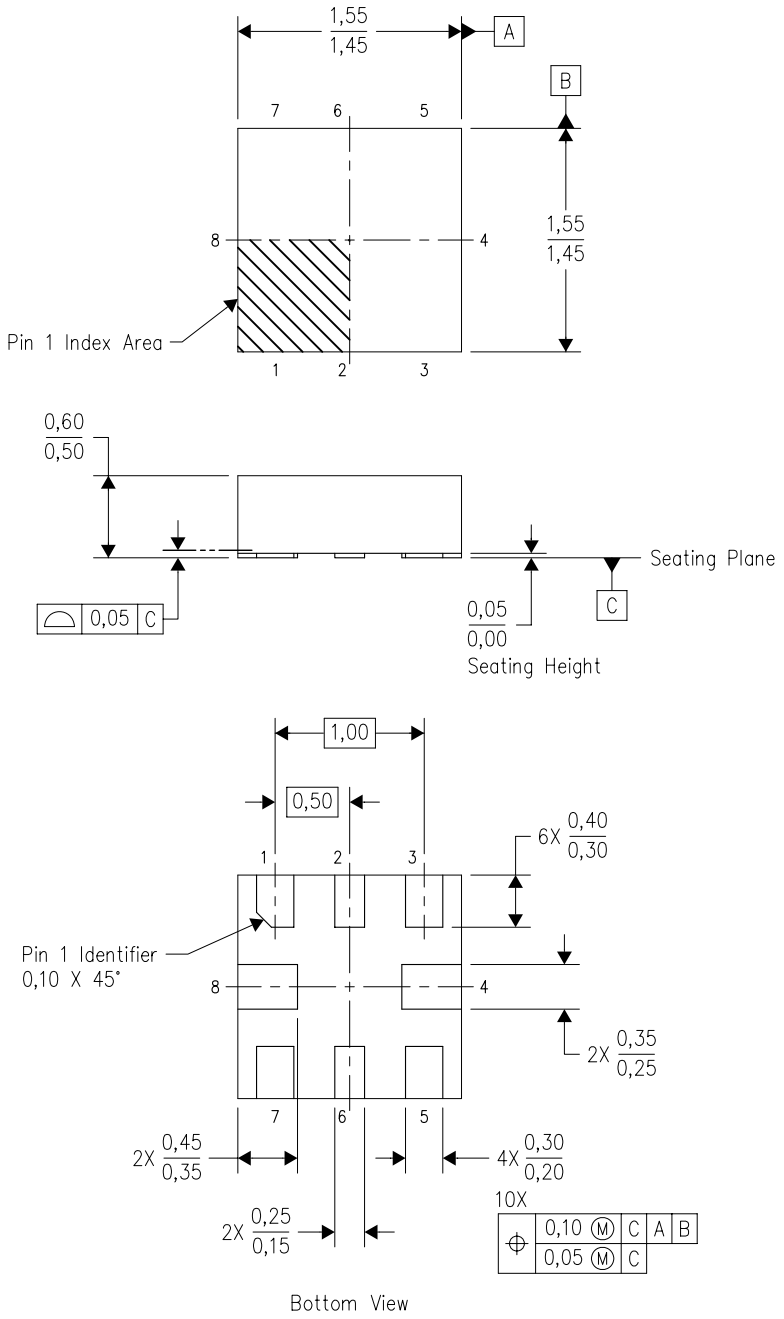
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

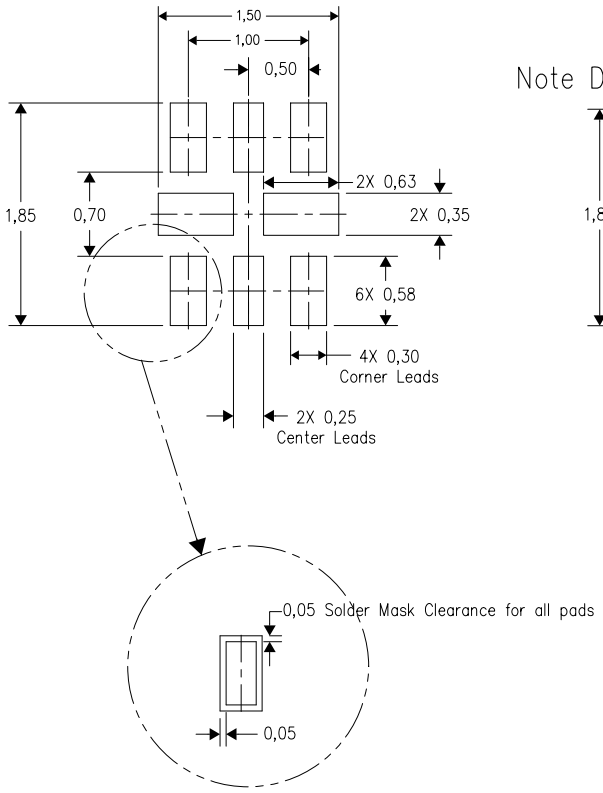


4207268–2/D 01/11

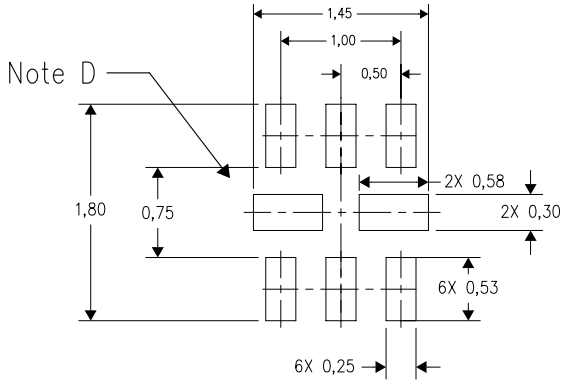
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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