TPS2124 2.8-V to 22-V Priority Power MUX with Seamless Switchover

1 Features

- Wide operating range: 2.8 V to 22 V
  - Absolute maximum input voltage of 24 V
- Low R_{ON} resistance:
  - TPS2124: 62 mΩ (typical)
- Adjustable over-voltage supervisor (OVx):
  - Accuracy < ±5%
- Adjustable priority supervisor (PR1):
  - Accuracy < ±5%
- Output current limit (ILM):
  - TPS2124: 1 A – 2.5 A
- Channel status indication (ST)
- Adjustable input settling time (SS)
- Adjustable output soft start time (SS)
- Low I_Q from enabled input: 200 µA (typical)
- Low I_Q from disabled input: 15 µA (Typical)
- Manual input source selection (OVx)
- Over-temperature protection (OTP)

2 Applications

- Backup and standby power
- Input source selection
- Multiple battery management
- EPOS and barcode scanners
- Building automation and surveillance
- Tracking and telematics

3 Description

The TPS2124 device is a Dual-Input, Single-Output (DISO) Power Multiplexer (MUX) that is well suited for a variety of systems having multiple power sources. The device will Automatically Detect, Select, and Seamlessly Transition between available inputs.

Priority can be automatically given to the highest input voltage or manually assigned to a lower voltage input to support both ORing and Source Selection operations. A priority voltage supervisor is used to select an input source.

An Ideal Diode operation is used to seamlessly transition between input sources. During switchover, the voltage drop is controlled to block reverse current before it happens and provide uninterrupted power to the load with minimal hold-up capacitance.

Current limiting is used during startup and switchover to protect against overcurrent events, and also protects the device during normal operation. The output current limit can be adjusted with a single external resistor.

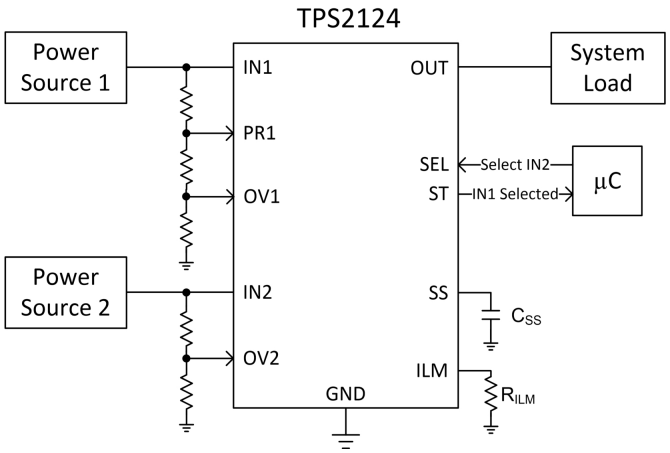
The TPS2124 device is available in a WCSP package characterized for operation for a temperature range of –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2124YFPR	WCSP (20)	1.5 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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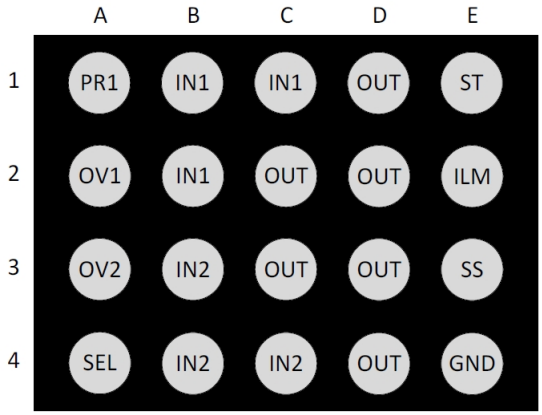
4 Revision History

DATE	REVISION	NOTES
June 2020	*	Initial release.

5 Pin Configuration and Functions

TPS2124 (YFP) Package
20-Pin WCSP
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	TPS2124 WCSP		
IN1	B1, B2, C1	I	Power Input for Source 1
IN2	B3, B4, C4	I	Power Input for Source 2
OUT	C2, C3, D1, D2, D3, D4	I	Power Output
ST	E1	O	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	O	Output Current Limiting for both channels.
SS	E3	O	Adjusts Input Setting Delay Time and Output Soft Start Time
GND	E4	—	Device Ground
PR1	A1	I	Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	I	Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	I	Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	I	Active low Enable for IN1. Allows GPIO to override priority operation and manually select IN2.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		Pins	MIN	MAX	UNIT
V_{IN1} , V_{IN2} , V_{OUT}	Maximum Power Pin Voltage	IN1, IN2, OUT	-0.3	24	V
V_{OV1} , V_{OV2}	Maximum Overvoltage Pin Voltage	OV1, OV2	-0.3	6	V
V_{PRI} , V_{SEL}	Maximum Control Pin Voltage	PRI, SEL	-0.3	6	V
V_{ST}	Maximum Control Pin Voltage	ST	-0.3	6	V
I_{OUT}	Maximum Output Current	OUT	Internally Limited		
$T_{J, MAX}$	Maximum Junction Temperature		Internally Limited		
T_{STG}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			Pins	VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	All	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		Pins	MIN	MAX	UNIT
V_{IN1} , V_{IN2}	Input Voltage Range (1)	IN1, IN2	2.8	22	V
V_{OUT}	Output Voltage Range	OUT	0	22	V
V_{OV1} , V_{OV2}	Overvoltage Pin Voltage	OV1, OV2	0	5.5	V
V_{PRI} , V_{SEL}	Control Pin Voltage	PRI, SEL	0	5.5	V
V_{ST}	Control Pin Voltage	ST	0	5.5	V
R_{ST}	Status Pin Pull Up Resistance	ST	6	20	kΩ
R_{ILM}	Current Limit Resistance	ILM	46	137	kΩ
C_{SS}	Soft-start Capacitor Voltage Rating	SS	4		V
I_{IN1} , I_{IN2}	Continuous Input Current	IN1, IN2		2	A
T_J	Junction temperature	-	-40	125	°C

(1) See Power Supply Recommendations Section for more Details

6.4 Thermal Information

THERMAL METRIC(1)		TPS2124 YFP (WCSP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information (continued)

THERMAL METRIC(1)		TPS2124 YFP (WCSP) 20 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
INPUT SOURCE (IN1, IN2)							
$I_{Q,\ INx}$	Quiescent Current (INx Powering OUT) (1)	OUT = Open	-40°C to 125°C		300	400	µA
$I_{SBY,\ INx}$	Standby Current (INx not powering OUT)(1)	$V_{OUT} = V_{INx}$	25°C	0	15	25	µA
			-40°C to 125°C			30	µA
$I_{LK,\ INx}$	Leakage Current (INx to OUT)	$\lvert V_{INx} - V_{OUT}\rvert > 0$	25°C	-200		200	µA
			-40°C to 125°C	-500		500	µA
$V_{UV,\ INx}$	Undervoltage Lockout	V_{INx} Rising	-40°C to 125°C	2.5	2.65	2.8	V
		V_{INx} Falling	-40°C to 125°C	2.4	2.55	2.7	V
OUTPUT SWITCHOVER (OUT)							
t_{SW}	Switchover Time	$V_{OUT} < V_{INx}$, CP2 < V_{REF}	-40°C to 125°C		100		µs
V_{COMP}	Input Voltage Comparator (V_{IN2} referenced to V_{IN1})	$V_{IN1} \geq V_{IN2}$	-40°C to 125°C	0	280	600	mV
		$V_{IN1} > V_{IN2}$, Falling Hysteresis	-40°C to 125°C	2.5	3.5	4.5	%
ON-RESISTANCE (INx to OUT)							
R_{ON}	ON-State Resistance	I_{OUT} = -200 mA, $V_{PRI} > V_{REF}$, $V_{INx} \geq 5.0$ V	25°C		62	75	mΩ
			-40°C to 85°C			90	mΩ
			-40°C to 105°C			100	mΩ
			-40°C to 125°C			120	mΩ
CURRENT LIMIT AND MONITOR (ILM)							
I_{LM}	Output Current Limit	R_{ILM} = 46.4kΩ	-40°C to 125°C	2	2.5	3	A
		R_{ILM} = 85kΩ	-40°C to 125°C	1	1.5	2	A
		R_{ILM} = 137kΩ	-40°C to 125°C	0.5	1	1.5	A
		R_{ILM} < 1kΩ	-40°C to 125°C	1.5	2.5	3.5	A
t_{LM}	Current Limit Response Time	Output Steady State	-40°C to 125°C		250		µs
CONTROL PINS (PRI, SEL, OV1, OV2)							
$V_{REF,\ x}$	Internal Voltage Reference	V_{PR1}, V_{OV1}, V_{OV2} Rising	-40°C to 125°C	1.01	1.06	1.1	V
		V_{PR1}, V_{OV1}, V_{OV2} Falling	-40°C to 125°C	0.99	1.04	1.09	V
$I_{LK,\ x}$	Pin Leakage Current	V_{PR1}, V_{OV1}, V_{OV2} = 0 V to 5.5 V	-40°C to 125°C	-0.1		0.1	µA
STATUS INDICATION PIN (ST)							
$I_{LK,\ ST}$	Pin Leakage	V_{ST} = 0 V to 5.5 V	-40°C to 125°C	-0.1		0.1	µA
t_{ST}	Status Delay	L to H	-40°C to 125°C		1		µs
I_{RCB}	Fast Reverse Current Detection Threshold	$V_{OUT} > V_{INx}$	-40°C to 125°C	0.2	1	2	A
FAST REVERSE CURRENT BLOCKING (RCB)							
V_{RCB}	RCB Release Voltage	$V_{OUT} > V_{INx}$	-40°C to 125°C	0	25	50	mV

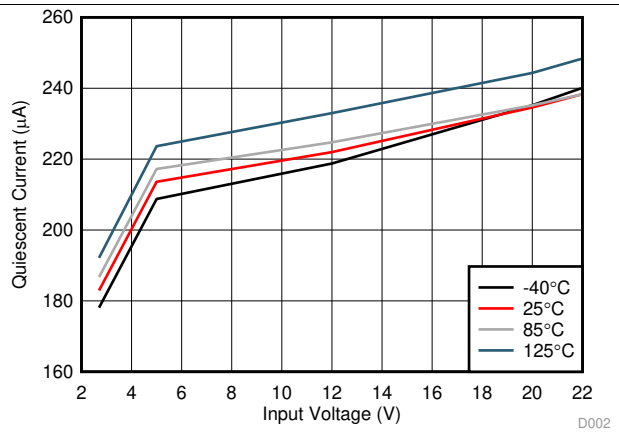
(1) When PR1 < V_{REF}, CP2 < V_{REF}, and $\lvert V_{IN1}-V_{IN2}\rvert$ < 1V, Quiescent current can be drawn from both IN1 and IN2 with combined current not to exceed $I_{Q,INx}$.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

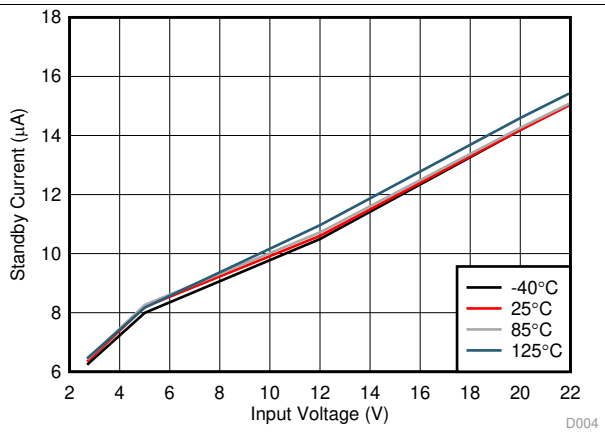
PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
t_{RCB}	Fast Reverse Current Blocking Response Time		-40°C to 125°C		10		µs
THERMAL SHUTDOWN (TSD)							
T_{SD}	Thermal Shutdown	Shutdown	Rising		160		°C
		Recovery	Falling		150		°C

6.6 Typical Characteristics



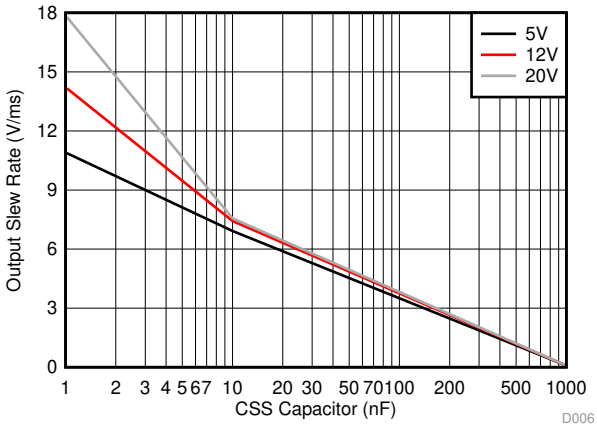
ILM = 1.5A

Figure 1. Quiescent Current vs Input Voltage



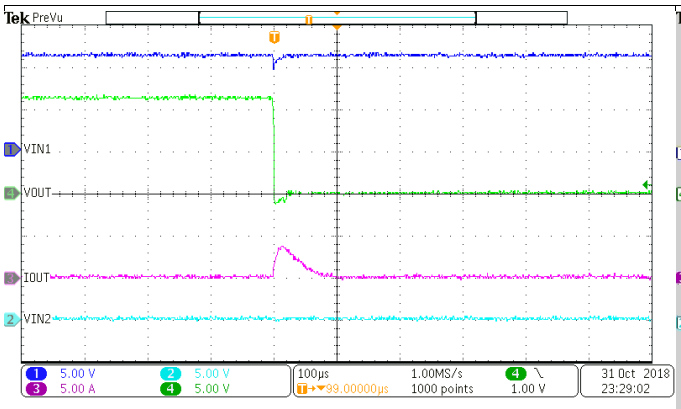
ILM = 1.5A

Figure 2. Standby Current vs Input Voltage



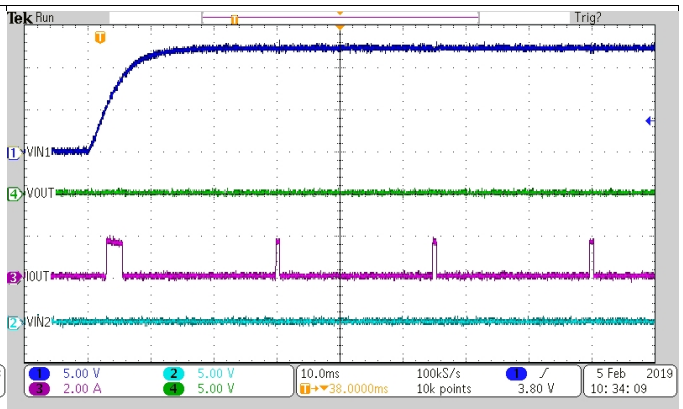
V_{IN1} > UVLO V_{IN2} = 0V

Figure 3. Output Slew Rate vs CSS Capacitor



V_{IN1} = 12 V V_{IN2} = 0 V

Figure 4. Hot Short on OUT while IN1 is Enabled



V_{IN1} = 12 V V_{IN2} = 0 V V_{OUT} = GND
R_{ILM} = 71.5kΩ

Figure 5. TPS2124 IN1 is Enabled with a Short on OUT

7 Parameter Measurement Information

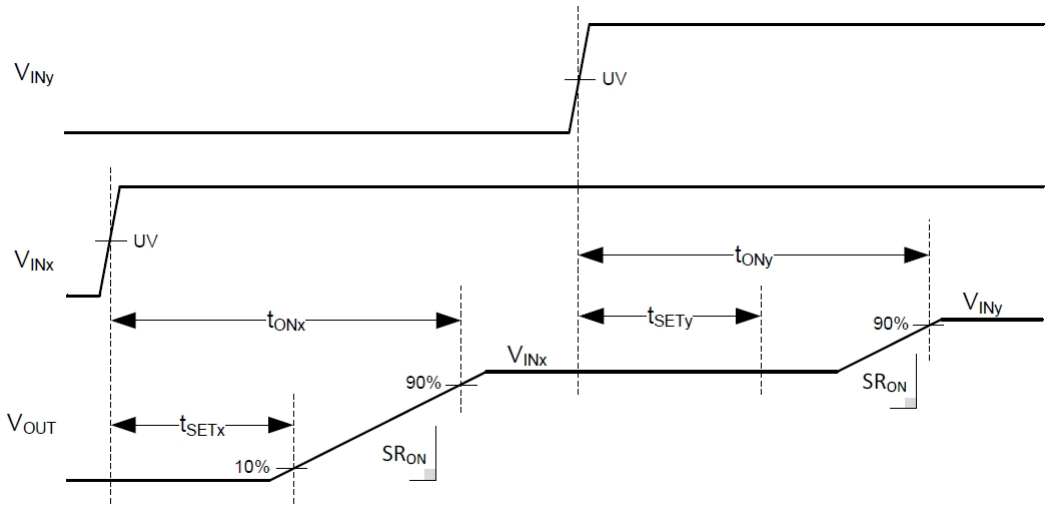


Figure 6. Timing Parameter Diagram

8 Detailed Description

8.1 Overview

The TPS2124 device is a Dual-Input, Single-Output (DISO) Power Multiplexer (MUX) that is well suited for a variety of systems having multiple power sources. The device will automatically detect, select, and seamlessly transition between available inputs. Priority can be automatically given to the highest input voltage or manually assigned to a lower voltage input to support both ORing and Source Selection operations. A priority voltage supervisor is used to select an input source.

An Ideal Diode operation is used to seamlessly transition between input sources. During switchover, the voltage drop is controlled to block reverse current before it happens and provide uninterrupted power to the load with minimal hold-up capacitance. Active current limiting is used during startup and switchover to protect against overcurrent, and also protects the device during normal operation. The output current limit can be adjusted with a single external resistor.

8.2 Functional Block Diagram

The below figure shows the block diagram for the TPS2124.

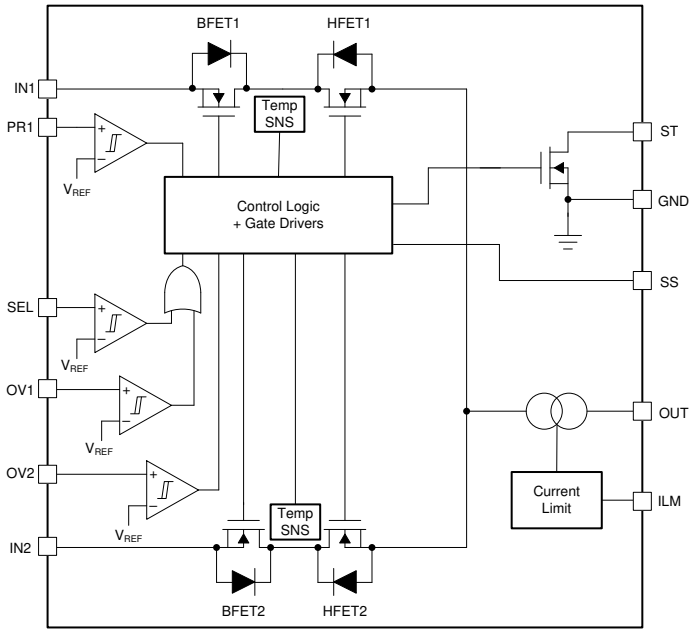


Figure 7. TPS2124 Functional Block Diagram

8.3 Feature Description

This section describes the different features of the TPS2124 power mux device.

8.3.1 Input Settling Time and Output Soft Start Control (SS)

The TPS2124 will automatically select the first source to become valid (INx >UV and INx <OV). The external capacitor (C_{SS}) will then be used as a timer to wait for the input to finish setting (t_{SETx}). When the settling timer has expired, C_{SS} will continue to charge and set the output slew rate (SR_{ON}) for a soft start. After the total turn on time (t_{ONx}), soft start will not be used again for INx until it ceases to be valid (INx <UV or INx >OV).

When the second source becomes valid (INy >UV and INy <OV), the external capacitor (C_{SS}) will be used again for a second settling time (t_{SETy}). After t_{SETy}, the TPS2124 will decide whether to continue sourcing the first source, or switchover to the second source. If the second source is selected at the end of t_{SETy}, then C_{SS} will be reused to set the output slew rate (SR_{ON}) for a second soft start. After the total turn on time (t_{ONy}), soft start will not be used again for INy until it ceases to be valid (INy <UV or INy >OV).

Feature Description (continued)

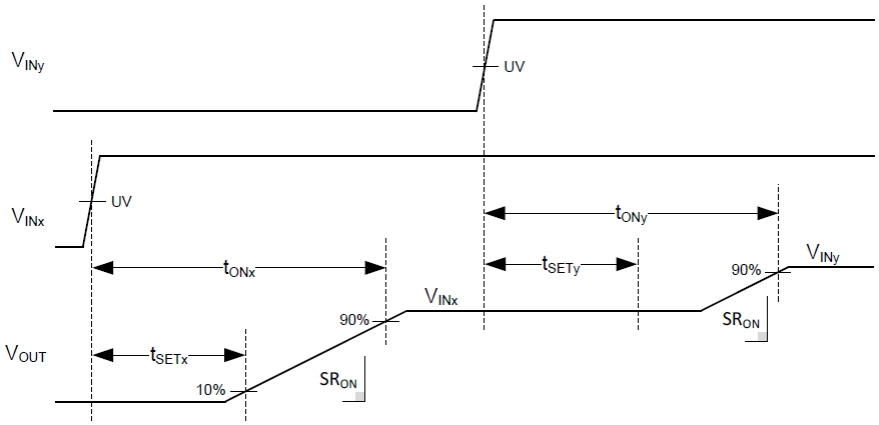


Figure 8. Settling and Soft Start Timing

If INy becomes valid before the end of t_{ONx}, t_{SETy} will be delayed and start after t_{ONx} has ended.

If INy is not selected during t_{SETy}, a second soft start will not take place, skipping t_{ONy}, and CSS will be retired until one of the inputs ceases to be valid.

8.3.1.1 Slew Rate vs. CSS Capacitor

Table 1 shows the estimated slew rate across CSS capacitance and VIN.

Table 1. Slew Rate vs. CSS Capacitor

CSS CAPACITOR	VIN = 5 V	VIN = 12 V	VIN = 20 V	UNITS
100 nF	780	800	880	V/s
1 uF	88	92	92	V/s
10 uF	8.8	9.6	10.4	V/s

8.3.2 Active Current Limiting (ILM)

The load current is monitored at all times. When the load current exceeds the current limit trip point I_{LM} programmed by R_{ILM} resistor, the device regulates the current within t_{ILM}. The following equations can be used to find the R_{ILM} value for a desired current limit, where R_{ILM} is in kΩ and between 46 kΩ to 137 kΩ.

TPS2124:

$$I_{LM} = \frac{69.1}{R_{ILM}^{0.861}} \quad (1)$$

During current regulation, the output voltage will drop resulting in increased device power dissipation. If the device junction temperature (T_J) reaches the thermal shutdown threshold (TSD) the internal FETs are turned off. After cooling down, the device will automatically restart.

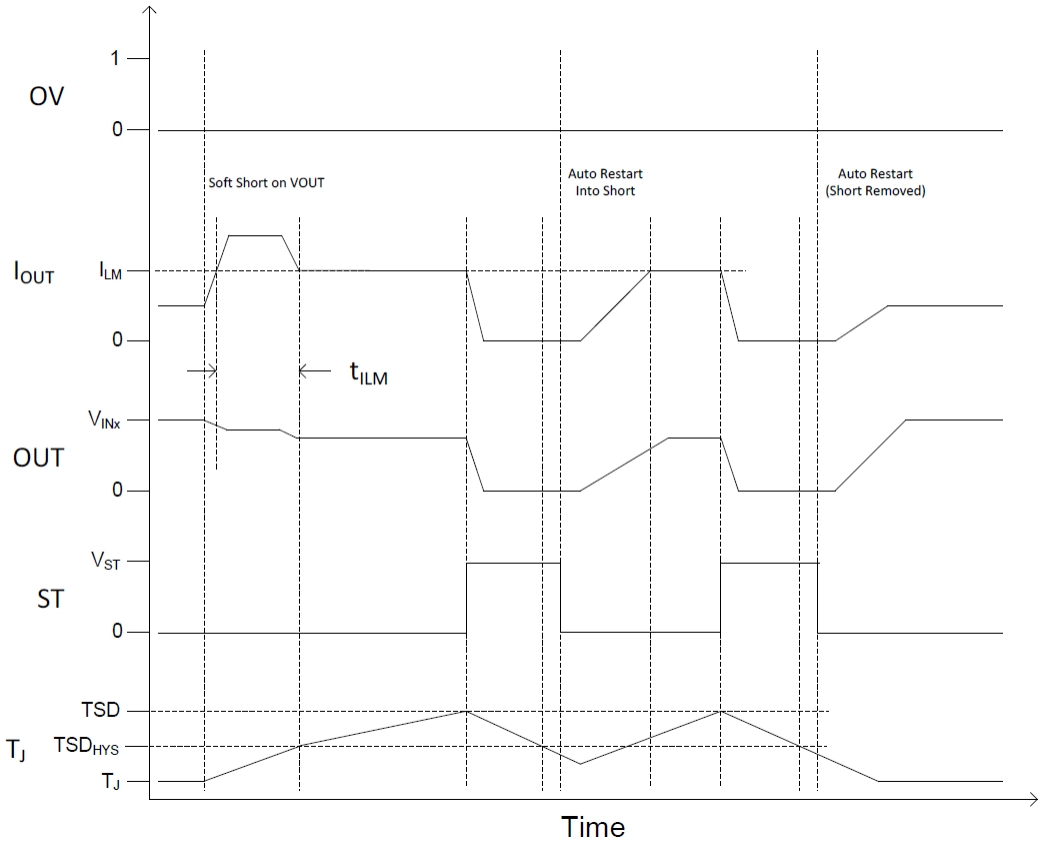


Figure 9. Current Limiting Behavior

8.3.3 Short-Circuit Protection

During a transient short circuit event, the current through the device increases very rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip overcurrent protection (OCP) comparator, with a threshold I_{OCP}. This comparator shuts down the pass device within 1 µs, when the current through internal FET I_{OUT} exceeds I_{OCP} (I_{OUT}> I_{OCP}). The trip threshold is set to about 2.4x of the programmed current limit I_{OCP} = 2.4 × I_{LM}. The OCP circuit holds the internal FET off for about 25 ms, after which the device turns back on. If the short is still present then the current-limit loop will regulate the output current to ILM and behave in a manner similar to a power up into a short.

8.3.4 Thermal Protection (T_{SD})

The TPS2124 device has built-in absolute thermal shutdown and relative thermal shutdown to ensure maximum reliability of the power mux. The absolute thermal shutdown is designed to disable the power FETs, if the junction temperature exceeds 160°C (typical). The device auto recovers about 25 ms after T_J < [T (TSD) – 10°C]. The relative thermal shutdown protects the device by turning off when the temperature of the power FETs increases sharply such that the FET temperature rises about 60°C above the rest of the die. The device auto recovers about 25 ms after the FETs cools down by 20°C. The relative thermal shutdown is critical for protecting the device against faults such as a power up into a short which causes the FET temperature to increase sharply.

8.3.5 Over-voltage Protection (OVx)

Output Over-voltage Protection is available for both IN1 and IN2 in case either applied voltage is greater than the maximum supported load voltage. The VREF comparator on the OVx pins allow for the Overvoltage Protection threshold to be adjusted independently for each input. When overvoltage is engaged, the corresponding channel will turn off immediately. Fast switchover to the other input is supported if it is a valid voltage.

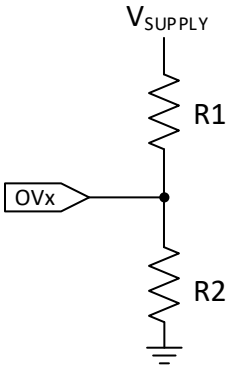


Figure 10. OVP Resistor Configuration

8.3.6 Fast Reverse Current Blocking (RCB)

Each channel has the always on reverse current blocking. If the output is forced above the selected input by V_{IRCB}, the channel will switch off to stop the reverse current I_{RCB} within t_{RCB}. As the output falls to within V_{RCB} of V_{IN}, the selected channel will quickly turn back on to avoid unnecessary voltage drops during fast switchover (t_{SW}).

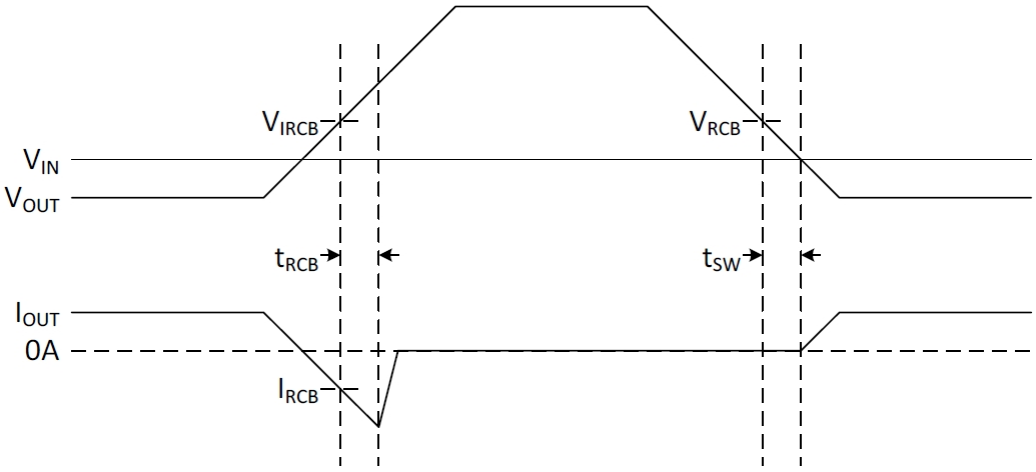


Figure 11. Reverse Current Blocking Behavior

8.3.7 Input Voltage Comparator (VCOMP)

If PR1 < VREF, the device will use an internal comparator between the two inputs to determine the priority source. V_{COMP} is configured to ensure IN2 will take priority if the input voltages are equal. If IN2 falls below the V_{COMP} Hysteresis, then IN1 will have priority.

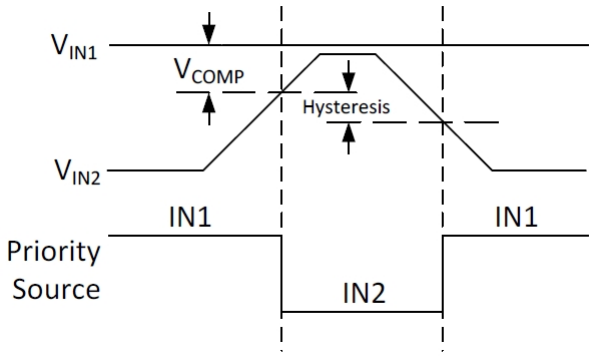


Figure 12. VCOMP Priority Source Selection

8.4 TPS2124 Device Functional Modes

Table 2 shows the TPS2124 functional behavior.

Table 2. TPS2124 Output Source Selection Table

DEVICE INPUTS				DEVICE OUTPUTS		MODE OF OPERATION
IN1 ≤ UV OR OV1 ≥ VREF OR SEL ≥VREF	IN2 ≤ UV OR OV2 ≥ VREF	PR1 ≥ VREF	VCOMP	OUT	ST	MODE
0	0	0	IN2 < IN1	IN1	H	VCOMP
0	0	0	IN2 ≥ IN1	IN2	L	VCOMP
0	0	1	X	IN1	H	VREF
0	1	X	X	IN1	H	Invalid Input
1	0	X	X	IN2	L	SEL / Invalid Input
1	1	X	X	Hi-Z	H	Invalid Inputs

A summary of the operation of the TPS2124 device can be found below:

- If only one input voltage is valid (above UV and below OV) then that input will power the output.
- If both inputs are not valid, then the output is Hi-Z.
- ST is pulled high when the output is Hi-Z or IN1. It is pulled low when IN2 is powering the output.
- If both inputs are valid and PR1 is pulled high (higher than VREF, 1.06-V typical), then IN1 is used.
- If both inputs are valid and PR1 is pulled low, then the highest voltage input is used.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2124 device is a highly configurable power mux that can be designed to meet various application requirements. When designing the TPS2124 for a power mux configuration, 3 key factors should be considered:

- VOUT voltage dip
- Manual and Automatic Switchover
- Switchover Time

The TPS2124 device can be configured in various modes to meet these considerations and provides a general table that describes each mode of operation. This application section will highlight 2 common modes of operation that address these factors.

9.2 Typical Application

Table 3 summarizes the applications highlighted in the following sections.

Table 3. TPS212x Application Summary Table

MODE	DEVICE	DESCRIPTION	SECTION
Manual Switchover	TPS2124	An external controller (such as an MCU) can be used to manually select between the two input sources.	Manual Switchover Schematic
Highest Voltage Operation (VCOMP)	TPS2124	The device automatically selects the highest voltage supply to power the output.	Highest Voltage Operation (VCOMP)

9.2.1 Manual Switchover Schematic

Figure 13 shows the application schematic for manual switchover on the TPS2124.

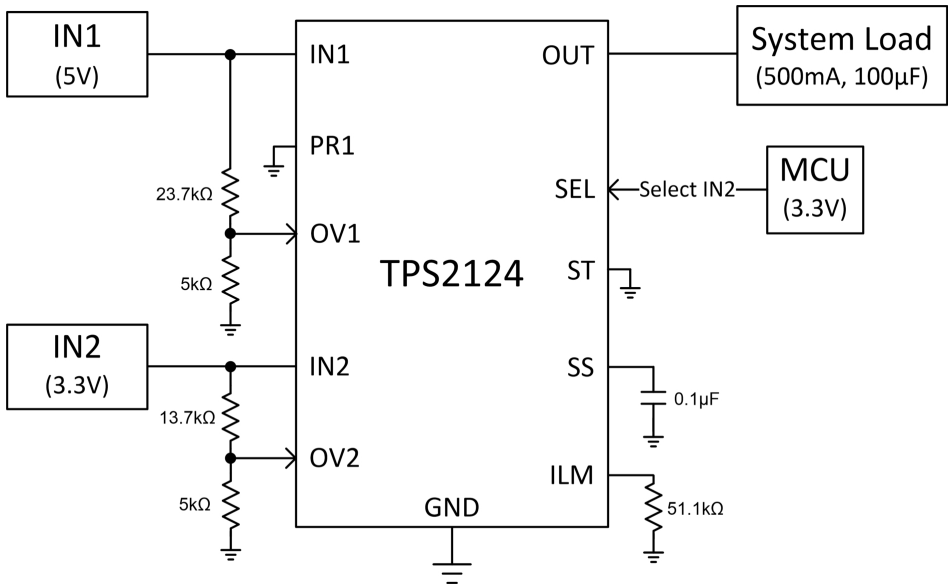


Figure 13. TPS2124 Manual Switchover

9.2.2 Design Requirements

In certain power architectures, an external MCU or controller monitors the downstream load. If the controller needs to select between multiple supplies, the controller can manually switch between inputs through a single GPIO. In this configuration, an external signal will switch between two input supplies, a 5-V supply (IN1) and a 3.3-V supply (IN2). Table 4 summarizes the design parameters for this example.

Table 4. Manual Switchover Design Requirements

DESIGN PARAMETER	Specification	Details
IN1 Voltage	V_{IN1}	5 V
IN2 Voltage	V_{IN1}	3.3 V
Load Current	I_{OUT}	500mA
Load Capacitance	C_L	100 µF
Maximum Inrush Current	I_{INRUSH}	100 mA
Current Limit		2 A
Switchover Time	t_{SW}	100 µs
Mode of Operation	Manual Switchover	VREF
External MCU Signal	V_{MCU}	3.3 V
Overvoltage Protection	V_{OV1} V_{OV2}	OV1 : 6.1 V OV2: 4 V

9.2.3 Detailed Design Description

The TPS2124 device can be configured to manually switch between IN1 and IN2 through an external GPIO. In this example, an external MCU signal is selecting between main power and auxiliary power to power a downstream load. By manually toggling the TPS2124, the device will switch between both sources, even if one supply is higher than the other supply. Ultimately, the main factor that will determine the switchover time between IN1 (5 V) and IN2 (3.3 V) is the output load.

Manual switchover can be enabled by configuring the TPS2124 for internal voltage reference control scheme (VREF). In the VREF scheme, if the voltage on PR1 is higher than the internal VREF voltage, 1.06 V (typical), the device will select IN1 as the output. If the voltage on PR1 drops below VREF, then the device will switch to IN2, as long as IN2 is presenting a valid input voltage. IN1 is commonly connected to PR1 with an external resistor divider. OV1 and OV2 can be configured to provide overvoltage protection. The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the status pin is high, IN1 is the output. If the pin is low, IN2 is the output. If this feature is not required, the ST pin can be connected to GND.

On the TPS2124, by connecting an external signal to the select pin (SEL), the device can override the PR1/VREF comparison. If the voltage on SEL is higher than VREF at approximately (1.06 V), then the device will select IN2, as shown on Table 2. If the voltage on SEL drops below VREF, then the device will switch to IN1 as long as PR1 >= VREF. Otherwise, the highest voltage input will be chosen between IN1 and IN2. In this example, since the IN1 is higher than IN2, at 5 V, it will be selected.

Figure 14 shows the application schematic for this design example on the TPS2124.

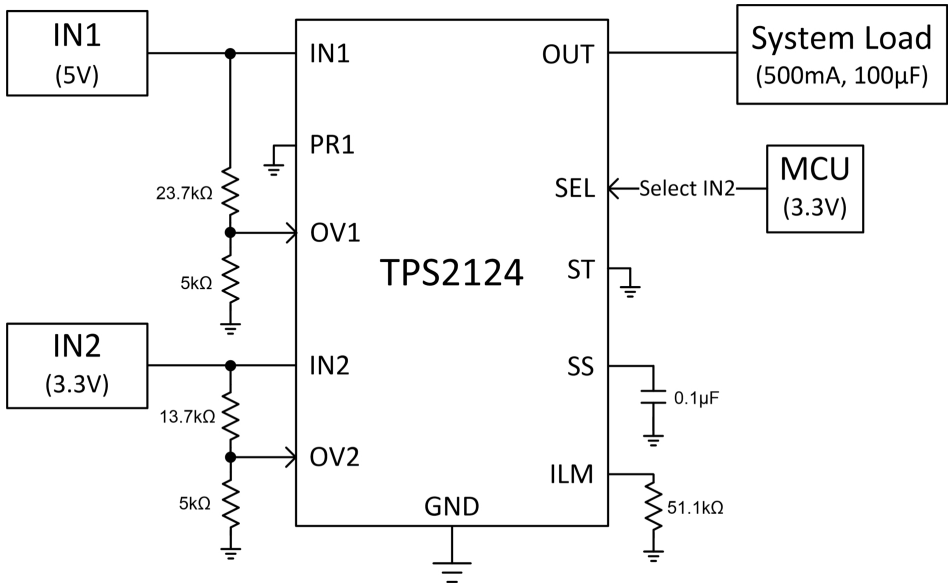


Figure 14. TPS2124 Manual Switchover

9.2.4 Design Procedure

9.2.4.1 Selecting OVx Resistors

Independent output overvoltage protection is available for both IN1 and IN2. The VREF comparator on the OV1 and OV2 pins allows for the overvoltage protection thresholds to be adjusted independently, allowing for different overvoltage thresholds on each channel. When overvoltage is engaged, the corresponding channel will turn off immediately if the pin reaches VREF, 1.06 V (typical). On this design, the overvoltage thresholds are triggered at roughly 1-V higher than the nominal input voltages. On IN1, the overvoltage resistor divider was programmed to be 6.08 V, where as the divider on IN2 was programmed to be 3.96 V. The OV resistor calculations are shown in Equation 2 and Equation 3.

$$1.06\ \text{V} = V_{IN1} \times \left(\frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + 23.7\ \text{k}\Omega} \right) = 6.08\ \text{V} \tag{2}$$

$$1.06\ \text{V} = V_{IN2} \times \left(\frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + 13.7\ \text{k}\Omega} \right) = 3.96\ \text{V} \tag{3}$$

9.2.4.2 Selecting Soft-Start Capacitor and Current Limit Resistors

Equation 1 can be used to determine the RLIM values for this application. In this example, the DC load current is 1 A. Setting the current limit to 2 A will limit potential inrush current events and protect downstream loads. See Equation 4 for the TPS2124 ILM Calculation:

$$I_{LM} = \frac{69.1}{59^{0.861}} = 2.06\,\text{A} \tag{4}$$

To calculate the slew rate needed to limit the inrush current to 100 mA, the Slew Rate Calculation can be used in Equation 5:

$$SR_{ON} = \frac{I_{INRUSH}}{C_L} \tag{5}$$

$$SR_{ON} = \frac{100\ \text{mA}}{100\ \mu\text{F}} = 1000\ \text{V/S} \tag{6}$$

Using this equation, the slew rate must be limited to 1000V/S or below to keep the inrush current below 100 mA. According to Table 1, at 5 V a CSS capacitance of 100 nF will provide a slew rate of 780V/S (typical), which is below the calculated threshold of 1000V/S. Therefore, a 100 nF capacitor will limit the inrush below 100 mA in a typical application.

9.2.5 Application Curves

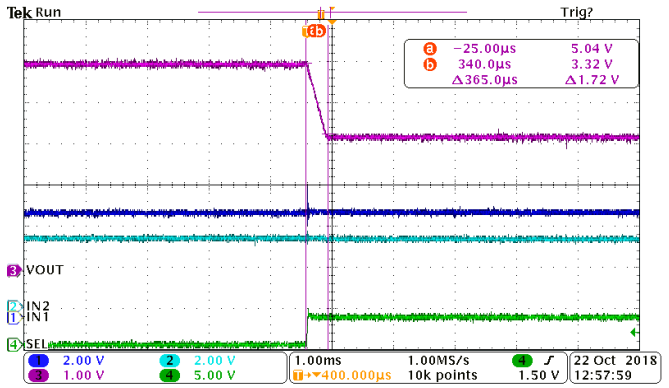


Figure 15. TPS2124 Switchover from IN1 to IN2

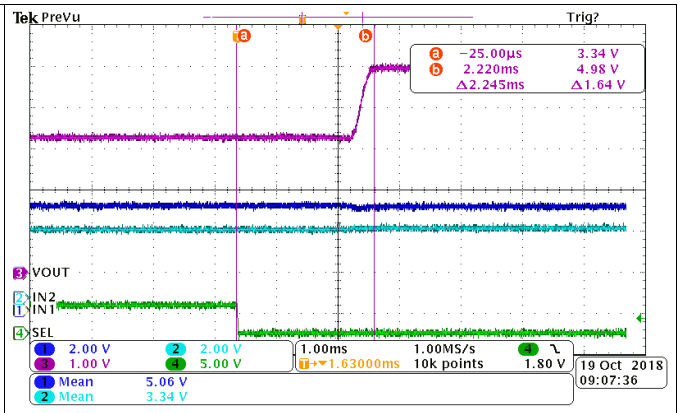


Figure 16. TPS2124 Switchover from IN2 to IN1

9.3 Highest Voltage Operation (VCOMP)

9.3.1 Application Schematic

Figure 17 shows the application schematic for highest voltage operation on the TPS2124.

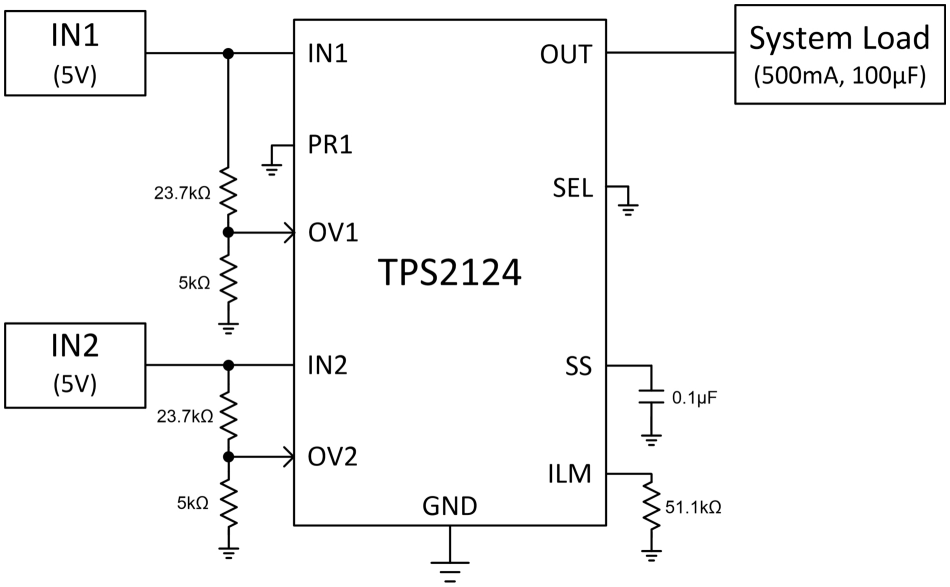


Figure 17. Highest Voltage Operation

Highest Voltage Operation (VCOMP) (continued)

9.3.2 Design Requirements

Table 5. Highest Voltage Design Requirements

DESIGN PARAMETER	Specification	Details
Input Voltage	V_{IN1}, V_{IN2}	5 V
Output Voltage	V_{OUT}	5 V
Load Current	I_{OUT}	0.5 A
Load Capacitance	C_L	100 µF
Switchover Time	t_{SW}	100 µs
Mode of Operation	Automatic Switchover	VCOMP

9.3.3 Detailed Design Description

In this mode of operation, the device will use an internal comparator between the two inputs to determine the priority source. If both PR1 and SEL are below VREF, priority is given to the highest input voltage. If both of the inputs voltages are equal, V_{COMP} and hysteresis ensures that IN2 takes priority. If IN2 falls below the V_{COMP} hysteresis, then IN1 will have priority. If IN2 gets reapplied, it will take priority when it falls within V_{COMP} of IN1.

In this example, the TPS2124 is configured with two 5-V inputs. When IN2 is applied to the system, it takes priority over IN1. Once it gets removed, priority returns to IN1.

9.3.4 Detailed Design Procedure

See Table 2 to summarize the priority between IN1 and IN2. Once IN2 reaches within VCOMP of IN1, the TPS2124 will switchover to IN2. Since IN1 is 5 V, once IN2 reaches 4.7 V (5 V – 300 mV), typically, the device will switch over to IN2. On the falling transition, once IN2 drops below VCOMP of IN1, the added hysteresis will prevent the device from switching back to IN1. Once IN2 drops below VCOMP and the hysteresis (3.5% typical) , the device will switch. Therefore, the device will switch back to IN1 once IN1 reaches (5 V – 300 mV – 175 mV), 4.525 V.

9.3.5 Application Curves

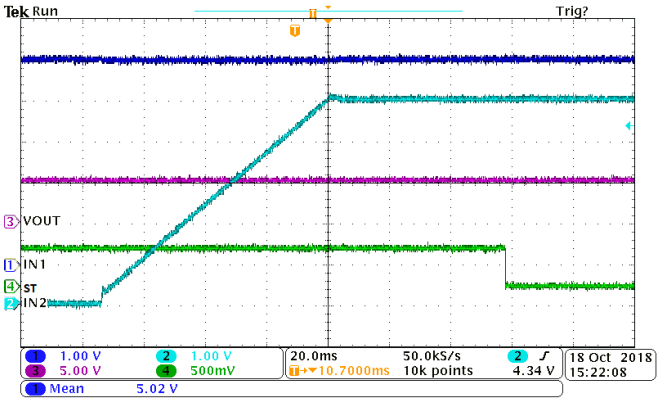


Figure 18. Switchover from IN1 to IN2

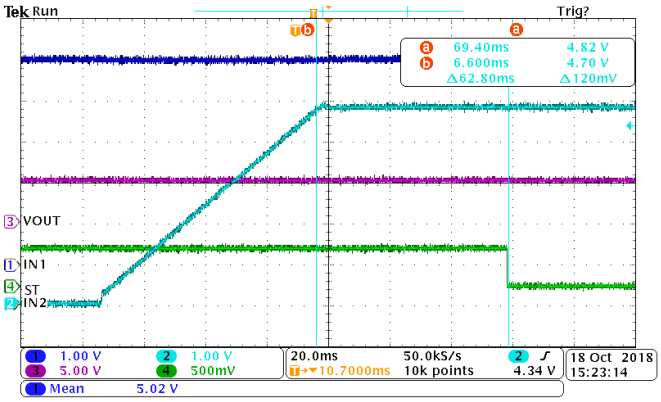


Figure 19. Timing from IN1 to IN2

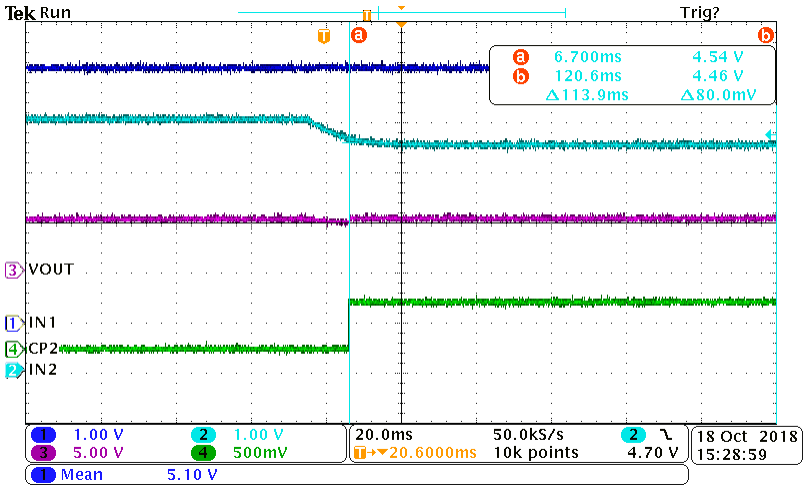


Figure 20. Switchover from IN2 to IN1

9.4 Reverse Polarity Protection with TPS2124

For applications that require reverse polarity protection, the TPS2124 can be configured to protect against mis-wiring input power supplies and block reverse current that could potentially damage the system. By connecting a diode on the GND pin of the TPS2124, this prevents reverse current from flowing back into the device when VIN is below system ground.

Since the TPS2124 has an absolute maximum rating of 24 V when referenced to device ground, the GND diode should be rated to standoff voltages up to the maximum reverse voltage. Furthermore, since the control pin voltages (PR1, OV1, OV2, etc.) are in reference to system GND, the voltage thresholds will need to be recalculated based on the voltage drop across the diode. To reduce the voltage drop, a resistor in parallel with the diode can also be used.

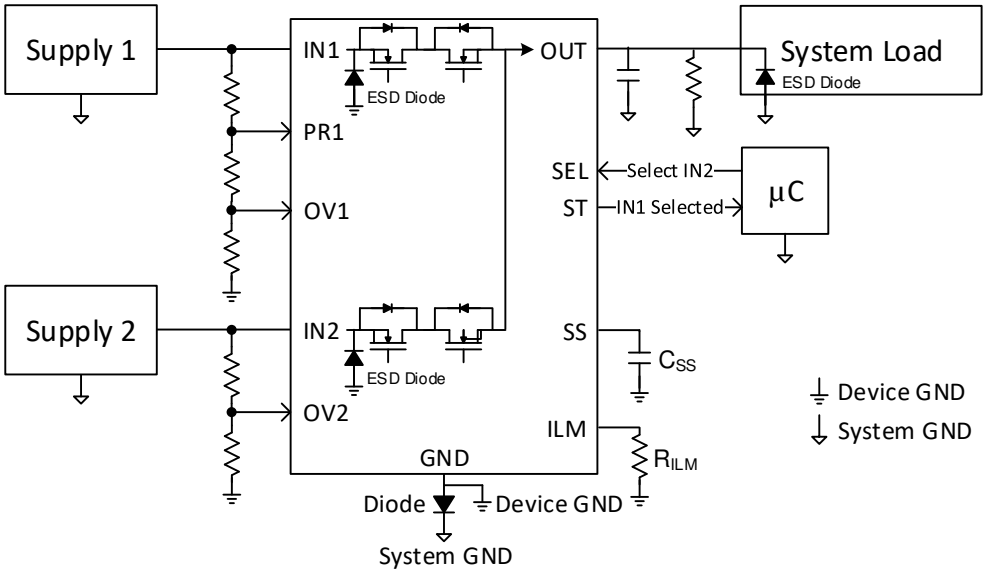


Figure 21. TPS2124 Reverse Polarity Configuration

10 Power Supply Recommendations

IN1, IN2, and OUT traces should all be wide enough to accomodate the amount of current passing through the device. Bypass capacitors on these pins should be placed as close to the device as possible. Low ESR ceramic capacitors with X5R or X7R dielectric are recommended.

To avoid output voltage drop, the capacitance on OUT can be increased. If the power supply cannot handle the inrush current transients due to the output capacitance, a higher input capacitance can be used. In the case where there are long cables or wires connected to the input of the device, there may be ringing on the supply. To help nullify the inductance of the cables and prevent ringing, a large capacitance can be used near the input of the device.

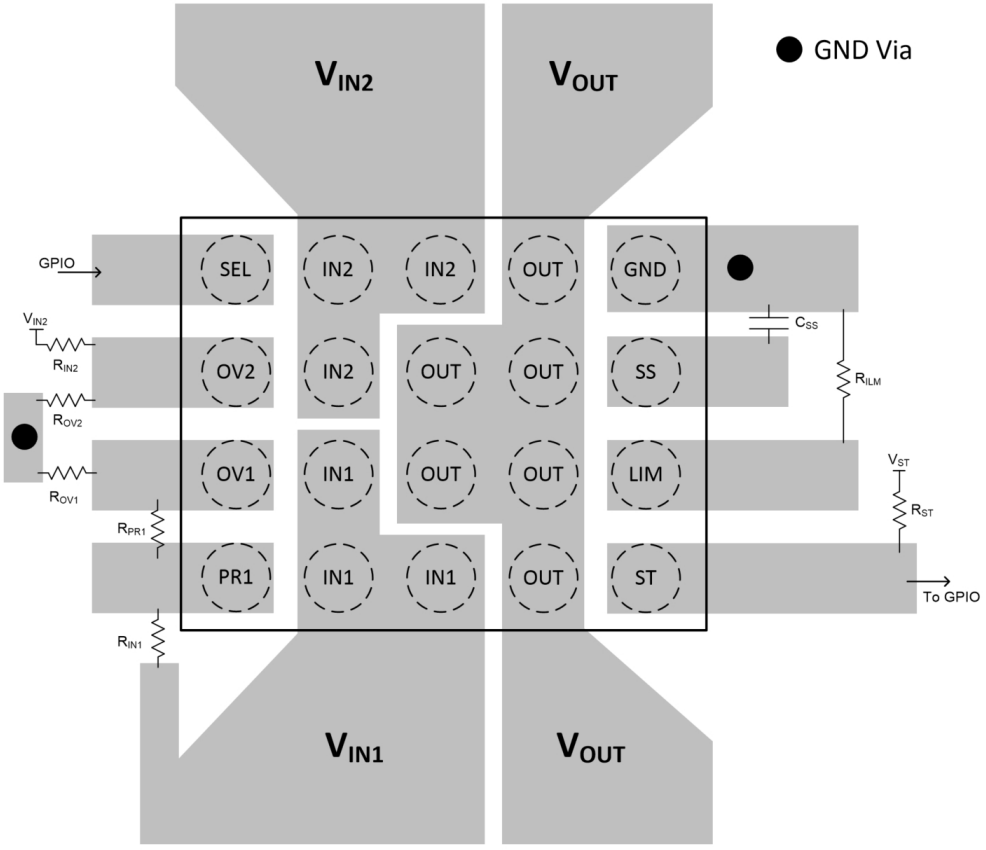
11 Layout

11.1 Layout Guidelines

Use short wide traces for input and output planes. For high current applications place vias near input and output pins to avoid current density and thermal resistance bottlenecks.

11.2 Layout Example

The example layout for the TPS2124 is shown below.



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2124YFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	24	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

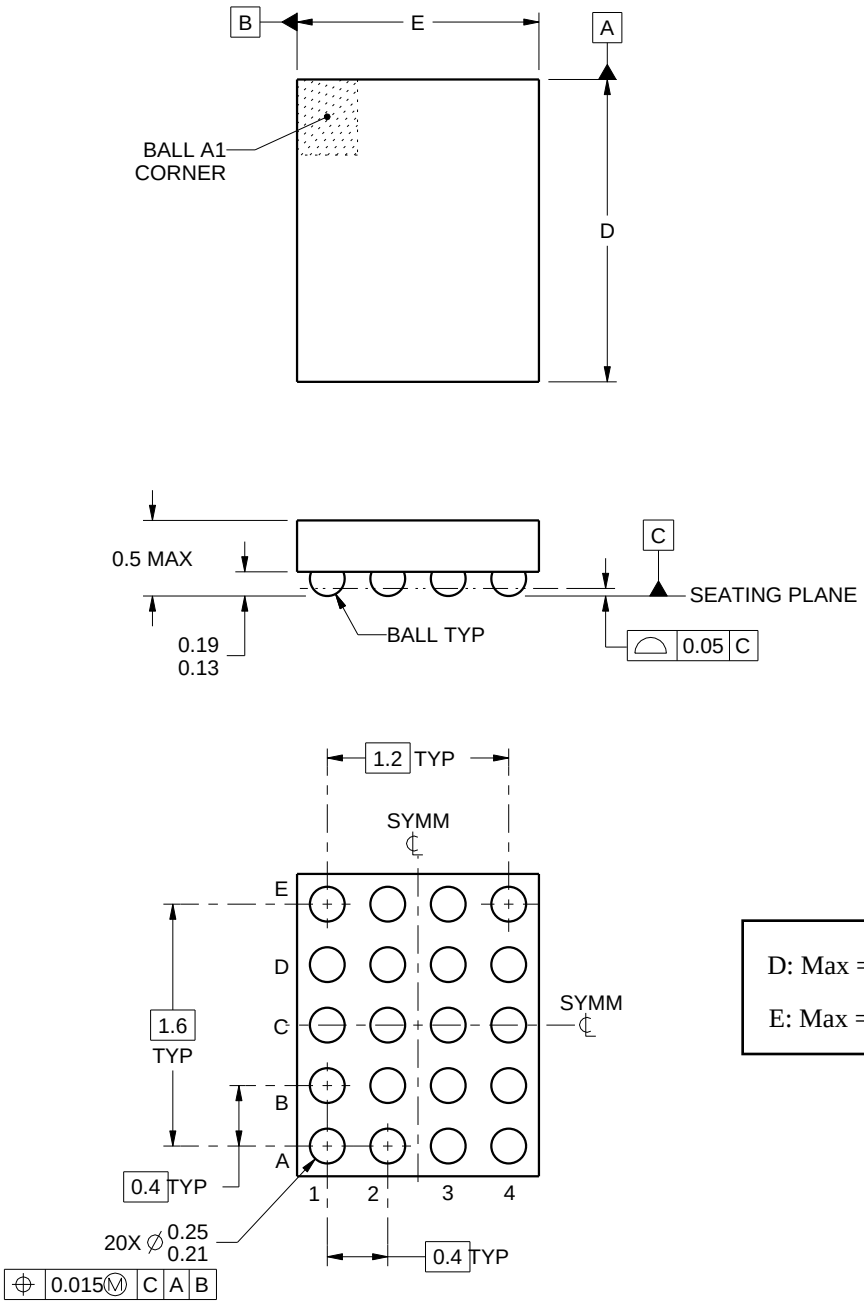
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



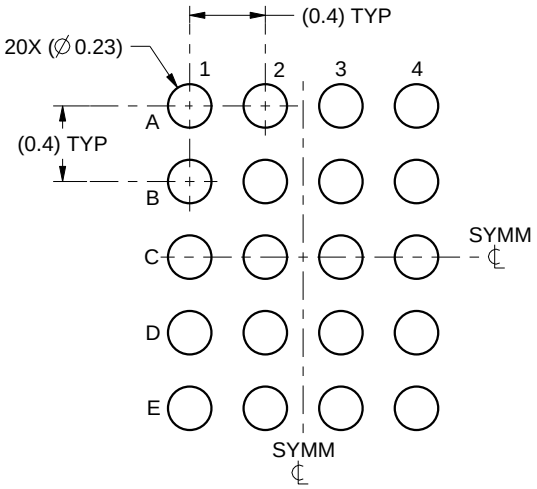
D: Max = 1.948 mm, Min =1.888 mm

E: Max = 1.548 mm, Min =1.488 mm

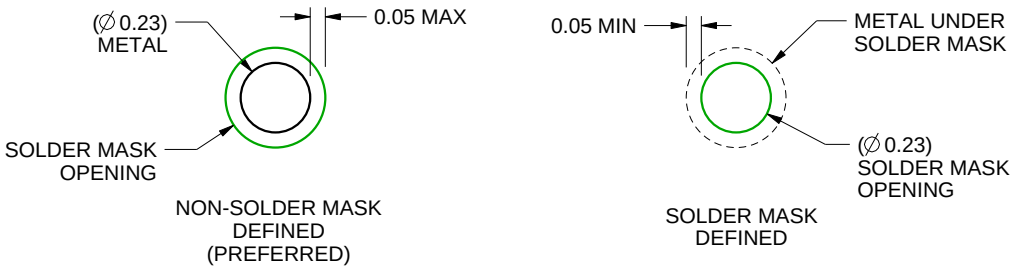
4222895/A 04/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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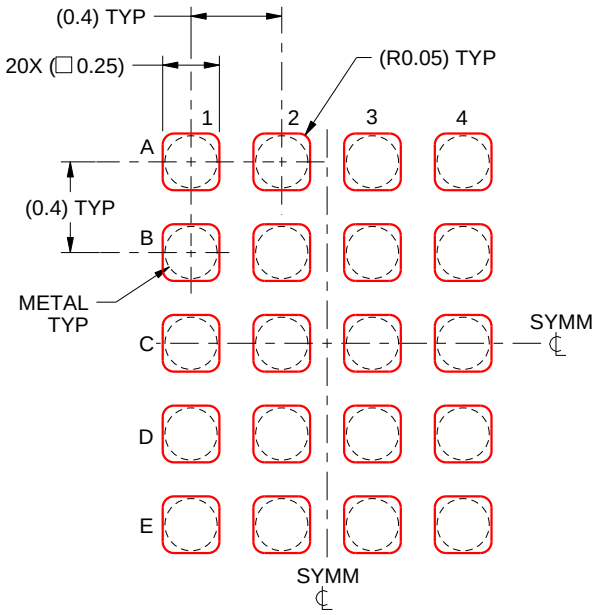
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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