Current-Limited, Power-Distribution Switches

Check for Samples: TPS20xxC

FEATURES

- **Single Power Switch Family**
- **Pin for Pin with Existing *TI Switch Portfolio***
- **Rated currents of 0.5 A, 1 A, 1.5 A, 2 A**
- **±20% Accurate, Fixed, Constant Current Limit**
- **Fast Over-Current Response – 2 µs**
- **Deglitched Fault Reporting**
- **Output Discharge When Disabled**
- **Reverse Current Blocking**
- **Built-in Softstart**
- **Ambient Temperature Range: –40°C to 85°C**

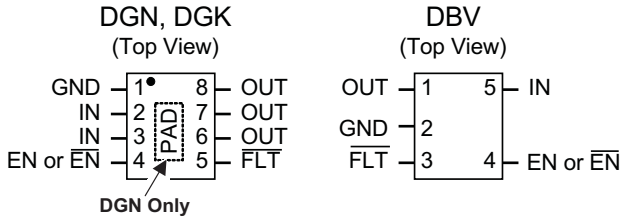
APPLICATIONS

- **USB Ports/Hubs, Laptops, Desktops**
- **High-Definition Digital TVs**
- **Set Top Boxes**
- **Short-Circuit Protection**

DESCRIPTION

The TPS20xxC power-distribution switch family is intended for applications such as USB where heavy capacitive loads and short-circuits are likely to be encountered. This family offers multiple devices with fixed current-limit thresholds for applications between 0.5 A and 2 A.

The TPS20xxC family limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current-limit threshold. This provides a predictable fault current under all conditions. The fast overload response time eases the burden on the main 5 V supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turn-on and turn-off.



TYPICAL APPLICATION

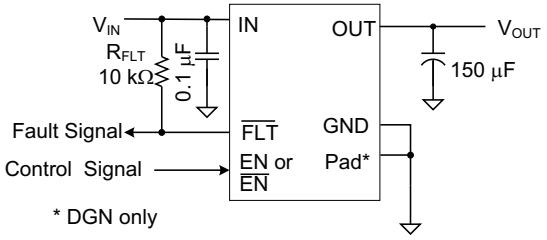


Figure 1. Typical Application

Table 1. DEVICES(1)

MAXIMUM OPERATING CURRENT	DEVICES	STATUS		
		MSOP-8 (PowerPad™)	SOT23-5	MSOP-8
0.5	TPS2051C	-	Active	-
1	TPS2065C	Active	Active	-
1.5	TPS2069C	Active	-	-
2	TPS2000C / 1C	Active	-	Active

(1) For more details, see the DEVICE INFORMATION table.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION(1)

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	BASE PART NUMBER	PACKAGED DEVICE AND MARKING(2)		
				MSOP-8 (DGN) PowerPAD™	SOT23-5 (DBV)	MSOP-8 (DGK)
0.5	Y	High	TPS2051C	–	VBYQ	–
1	Y	High	TPS2065C	VCAQ	VCAQ	–
1.5	Y	High	TPS2069C	VBUQ	–	–
2	Y	Low	TPS2000C	BCMS	–	PXFI
2	Y	High	TPS2001C	VBWQ	–	PXGI

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) "-" indicates the device is not available in this package.

ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE		UNIT
		MIN	MAX	
Voltage range on IN, OUT, EN or $\overline{EN}$, $\overline{FLT}$ (3)		–0.3	6	V
Voltage range from IN to OUT		–6	6	V
Maximum junction temperature, T_J		Internally Limited		
Electrostatic Discharge	HBM	2		kV
	CDM	500		V
	IEC 61000-4-2, Contact / Air (4)	8	15	kV

(1) Absolute maximum ratings apply over recommended junction temperature range.
(2) Voltages are with respect to GND unless otherwise noted.
(3) See the Input and Output Capacitance section.
(4) V_{OUT} was surged on a pcb with input and output bypassing per Figure 1 (except input capacitor was 22 µF) with no device failures.

THERMAL INFORMATION

THERMAL METRIC(1) (See DEVICE INFORMATION table.)		0.5 A or 1 A Rated	1.5 A or 2 A Rated	0.5 A or 1 A Rated	1.5 A or 2 A Rated	2 A Rated	UNITS
		DBV	DBV	DGN	DGN	DGK	
		5 PINS	5 PINS	8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	224.9	220.4	72.1	67.1	205.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	95.2	89.7	87.3	80.8	94.3	
θ_{JB}	Junction-to-board thermal resistance	51.4	46.9	42.2	37.2	126.9	
ψ_{JT}	Junction-to-top characterization parameter	6.6	5.2	7.3	5.6	24.7	
ψ_{JB}	Junction-to-board characterization parameter	50.3	46.2	42.0	36.9	125.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	39.2	32.1	N/A	
θ_{JA}Custom	See the Power DIssipation and Junction Temperature section	139.3	134.9	66.5	61.3	110.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		4.5		5.5	V
V_{EN}	Input voltage, EN or $\overline{EN}$		0		5.5	V
I_{OUT}	Continuous output current, OUT	TPS2051C			0.5	A
		TPS2065C			1	
		TPS2069C			1.5	
		TPS2000C/01C			2	
T_J	Operating junction temperature		–40		125	°C
$I_{\overline{FLT}}$	Sink current into $\overline{FLT}$		0		5	mA

ELECTRICAL CHARACTERISTICS: $T_J = T_A = 25°C$ (1)

Unless otherwise noted:, V_{IN} = 5 V, $V_{EN} = V_{IN}$ or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A. See the DEVICE INFORMATION table for the rated current of each part number. Parametrics over a wider operational range are shown in the second ELECTRICAL CHARACTERISTICS table.

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	Input – output resistance	0.5 A rated output, 25°C	DBV		97	110	mΩ
		0.5 A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
		1 A rated output, 25°C	DBV		96	110	mΩ
			DGN		86	100	
		1 A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
			DGN		86	120	
		1.5 A rated output, 25°C	DGN		69	84	mΩ
		1.5 A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DGN		69	98	mΩ
		2 A rated output, 25°C	DGN, DGK		72	84	mΩ
		2 A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DGN, DGK		72	98	mΩ
CURRENT LIMIT							
I_{OS} (2)	Current-limit, See Figure 7	0.5A rated output		0.67	0.85	1.01	A
		1 A rated output		1.3	1.55	1.8	
		1.5 A rated output		1.7	2.15	2.5	
		2 A rated output		2.35	2.9	3.4	
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled				0.01	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V				2	
I_{SE}	Supply current, switch enabled				60	70	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V				85	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}			0.1	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}				5	
OUTPUT DISCHARGE							
R_{PD}	Output pull-down resistance(3)	$V_{IN} = V_{OUT}$ = 5 V, disabled		400	470	600	Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See CURRENT LIMIT section for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted:4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A, typical values are at 5 V and 25°C. See the DEVICE INFORMATION table for the rated current of each part number.

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	Input – output resistance	0.5 A rated output	DBV		97	154	mΩ
		1 A rated output	DBV		96	154	mΩ
			DGN		86	140	
		1.5 A rated output	DGN		69	112	mΩ
		2 A rated output	DGN, DGK		72	112	mΩ
ENABLE INPUT (EN or $\overline{EN}$)							
	Threshold	Input rising		1	1.45	2	V
	Hysteresis			0.07	0.13	0.20	V
	Leakage current	(V_{EN} or $V_{\overline{EN}}$) = 0 V or 5.5 V		–1	0	1	µA
t_{ON}	Turnon time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑ or $\overline{EN}$ ↓. See Figure 2, Figure 4, and Figure 5					ms
		0.5A / 1A Rated		1	1.4	1.8	
		1.5A / 2A Rated		1.2	1.7	2.2	
t_{OFF}	Turnoff time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓ or $\overline{EN}$ ↑. See Figure 2, Figure 4, and Figure 5					ms
		0.5A and 1A Rated		1.3	1.65	2	
		1.5A / 2A Rated		1.7	2.1	2.5	
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 3					ms
		0.5A / 1A Rated		0.4	0.55	0.7	
		1.5A / 2A Rated		0.5	0.7	1.0	
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 3					ms
		0.5A / 1A Rated		0.25	0.35	0.45	
		1.5A / 2A Rated		0.3	0.43	0.55	
CURRENT LIMIT							
I_{OS}[2]	Current-limit, See Figure 8		0.5 A rated output	0.65	0.85	1.05	A
			1 A rated output	1.2	1.55	1.9	
			1.5 A rated output	1.6	2.15	2.7	
			2 A rated output	2.3	2.9	3.6	
t_{IOS}	Short-circuit response time[3]	V_{IN} = 5 V (see Figure 7), One-half full load → R_{SHORT} = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled				0.01	10	µA
I_{SE}	Supply current, switch enabled				65	90	µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, Measure I_{VOUT}			0.2	20	µA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Rising threshold	V_{IN}↑		3.5	3.75	4	V
	Hysteresis[3]	V_{IN}↓			0.14		V

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See CURRENT LIMIT section for explanation of this parameter.
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ELECTRICAL CHARACTERISTICS: –40°C ≤ T_J ≤ 125°C (continued)

Unless otherwise noted:4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A, typical values are at 5 V and 25°C. See the DEVICE INFORMATION table for the rated current of each part number.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
$\overline{FLT}$						
	Output low voltage, $\overline{FLT}$	$I_{\overline{FLT}}$ = 1 mA			0.2	V
	Off-state leakage	$V_{\overline{FLT}}$ = 5.5 V			1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ deglitch	$\overline{FLT}$ assertion/deassertion deglitch	6	9	12	ms
OUTPUT DISCHARGE						
R_{PD}	Output pull-down resistance	V_{IN} = 4 V, V_{OUT} = 5.0 V, disabled	350	560	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5.0 V, disabled	300	470	800	
THERMAL SHUTDOWN						
	Rising threshold (T_J)	In current limit	135			°C
		Not in current limit	155			
	Hysteresis (4)			20		

(4) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

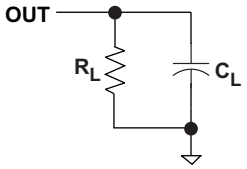


Figure 2. Output Rise / Fall Test Load

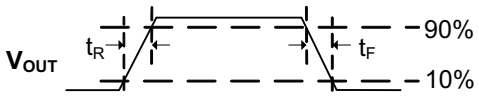


Figure 3. Power-On and Off Timing

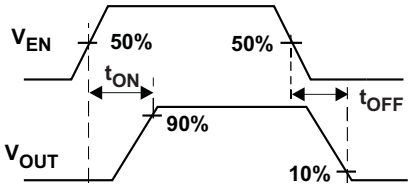


Figure 4. Enable Timing, Active High Enable

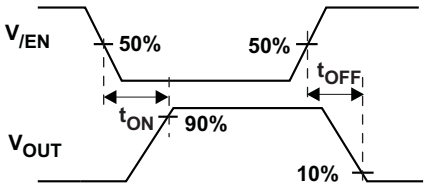


Figure 5. Enable Timing, Active Low Enable

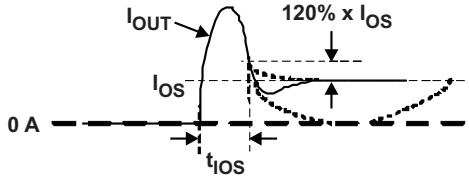


Figure 6. Output Short Circuit Parameters

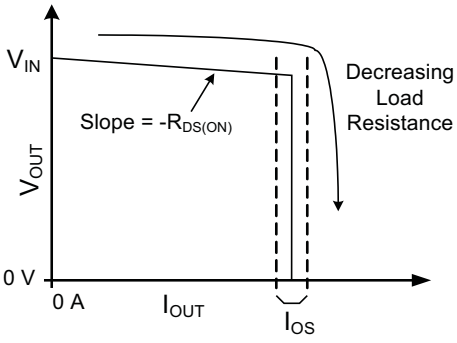
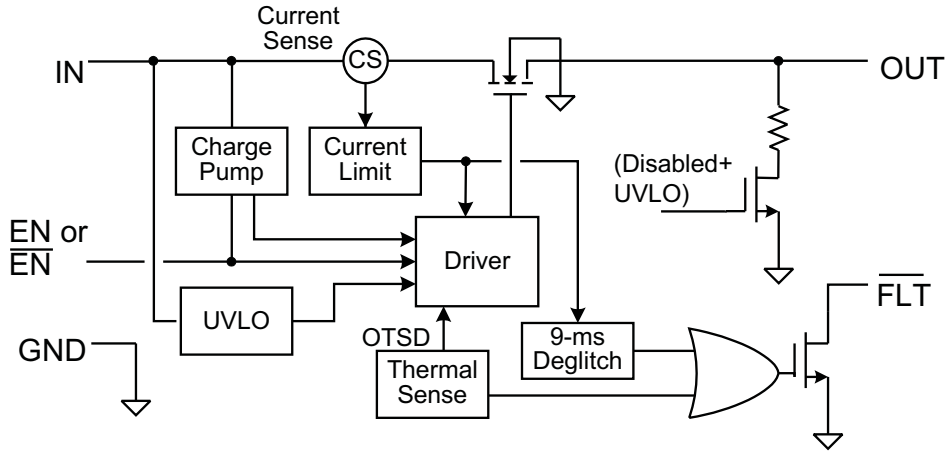


Figure 7. Output Characteristic Showing Current Limit

FUNCTIONAL BLOCK DIAGRAM

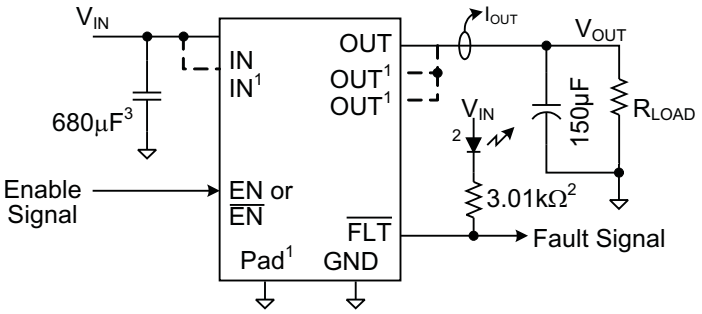


DEVICE INFORMATION

PIN FUNCTIONS

NAME	PINS	DESCRIPTION
8-PIN PACKAGE		
EN or $\overline{EN}$	4	Enable input, logic high turns on power switch
GND	1	Ground connection
IN	2, 3	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
$\overline{FLT}$	5	Active-low open-drain output, asserted during over-current, or over-temperature conditions
OUT	6, 7, 8	Power-switch output, connect to load
PowerPAD (DGN ONLY)	PAD	Internally connected to GND. Connect PAD to GND plane as a heatsink for the best thermal performance. PAD may be left floating if desired. See POWER DISSIPATION AND JUNCTION TEMPERATURE section for guidance.
5-PIN PACKAGE		
EN or $\overline{EN}$	4	Enable input, logic high turns on power switch
GND	2	Ground connection
IN	5	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
$\overline{FLT}$	3	Active-low open-drain output, asserted during over-current, or over-temperature conditions
OUT	1	Power-switch output, connect to load.

TYPICAL CHARACTERISTICS



(1) Not every package has all pins

(2) These parts are for test purposes

(3) Helps with output shorting tests when external supply is used.

Figure 8. Test Circuit for System Operation in Typical Characteristics Section

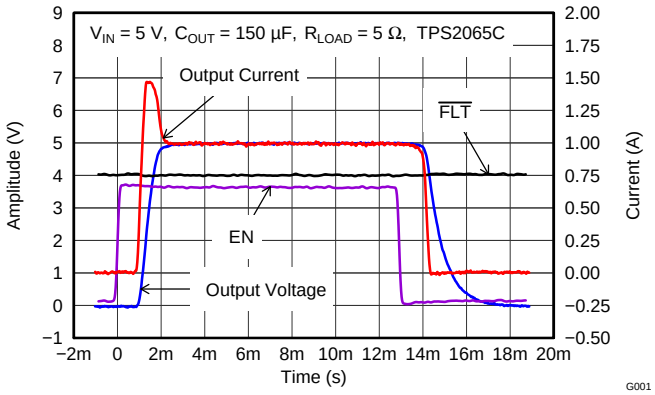


Figure 9. TPS2065C Output Rise / Fall 5Ω

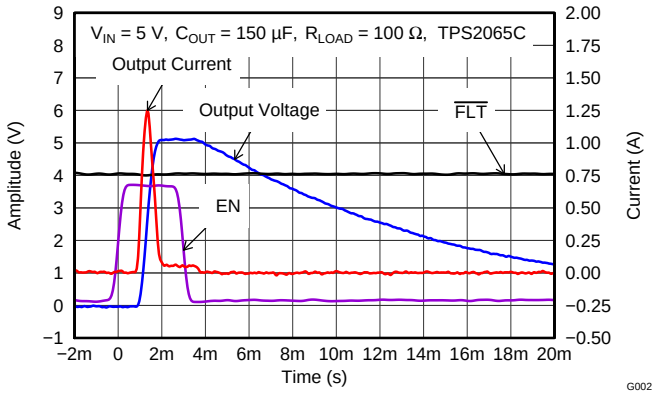


Figure 10. TPS2065C Output Rise / Fall 100Ω

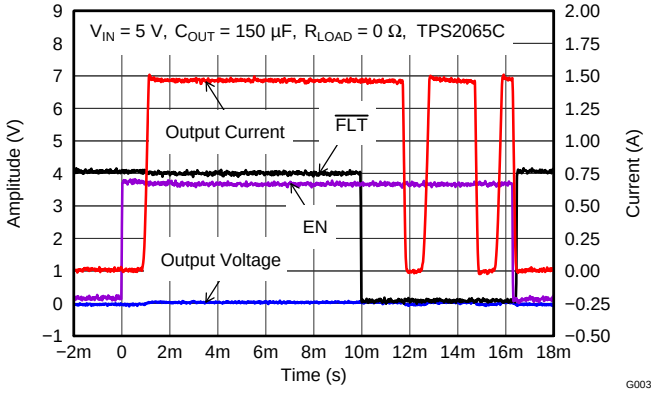


Figure 11. TPS2065C Enable into Output Short

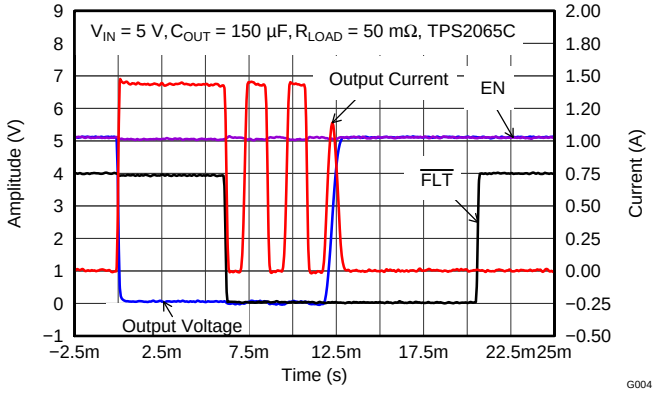


Figure 12. TPS2065C Pulsed Short Applied

TYPICAL CHARACTERISTICS (continued)

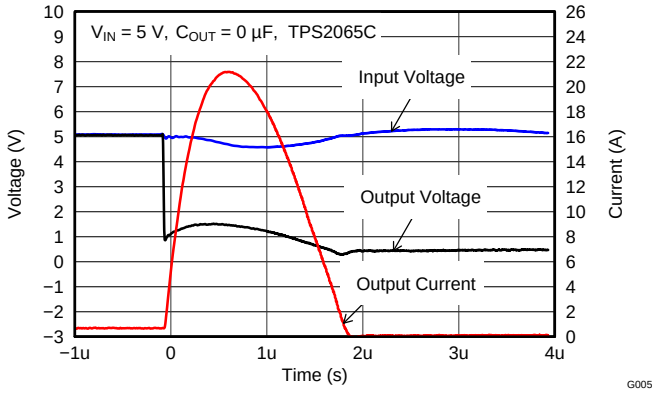


Figure 13. TPS2065C Short Applied

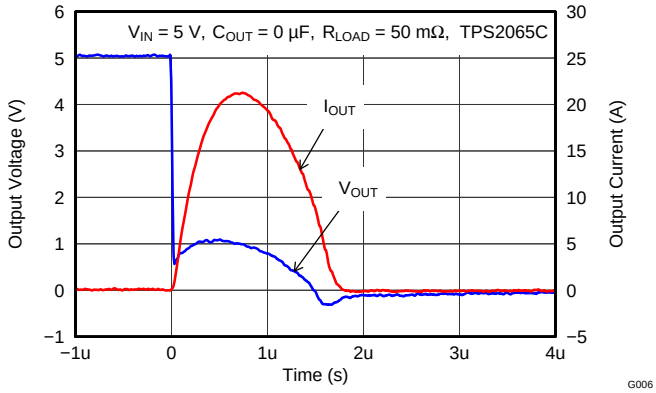


Figure 14. TPS2065C Pulsed 1.45-A Load

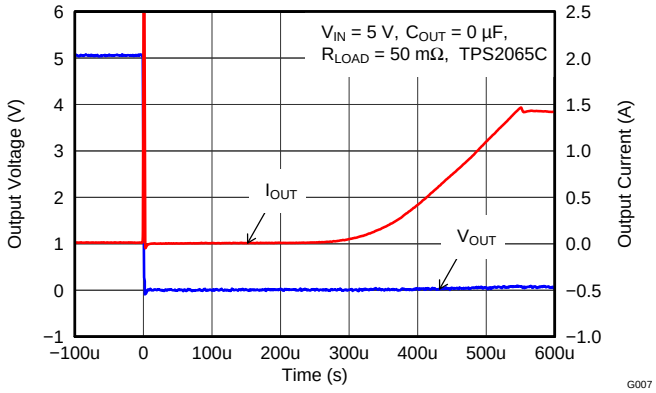


Figure 15. TPS2065C 50 mΩ Short Circuit

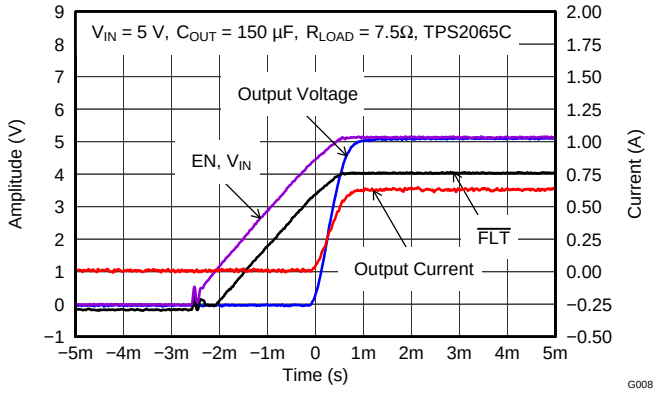


Figure 16. TPS2065C Power Up - Enabled

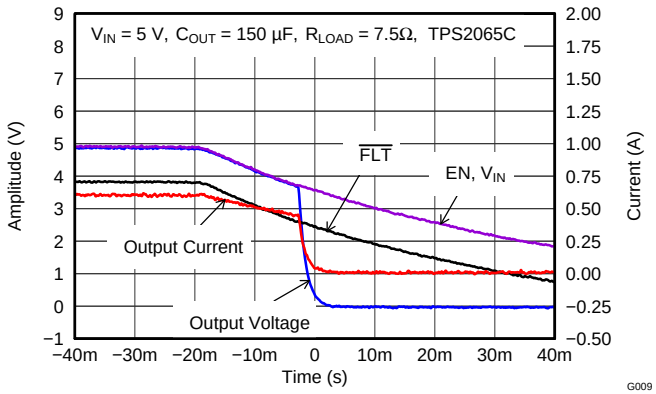


Figure 17. TPS2065C Power Down - Enabled

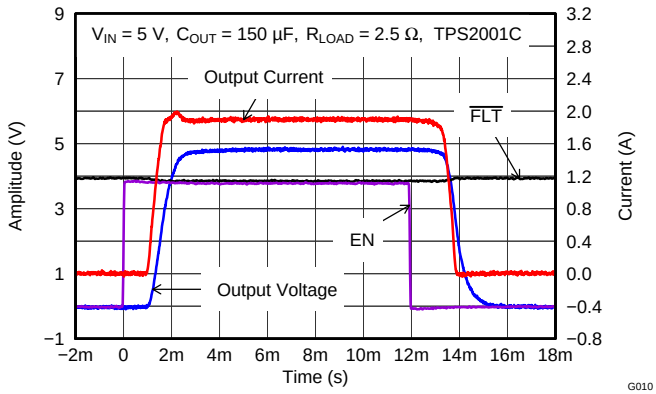


Figure 18. TPS2001C Turn ON into 2.5Ω

TYPICAL CHARACTERISTICS (continued)

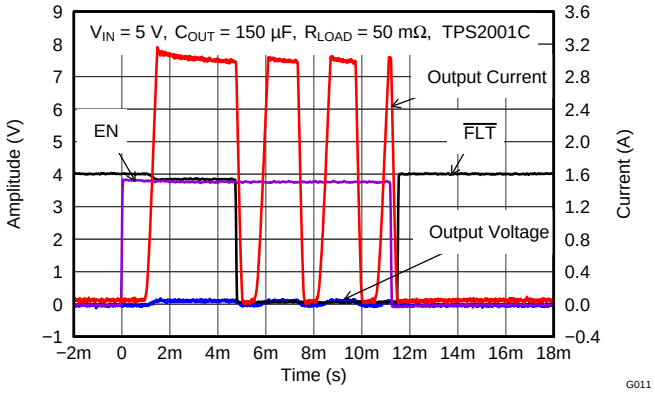


Figure 19. TPS2001C Enable into Short

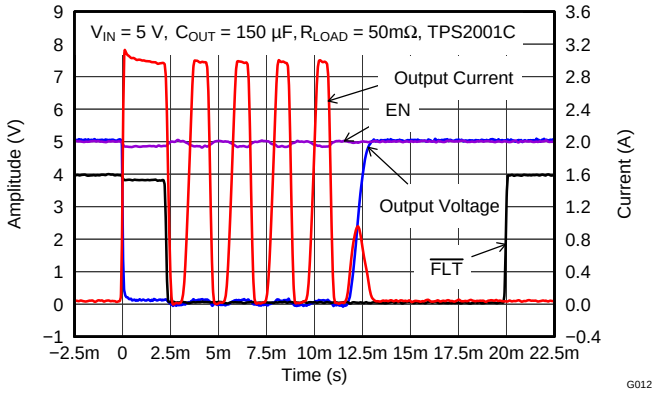


Figure 20. TPS2001C Pulsed Output Short

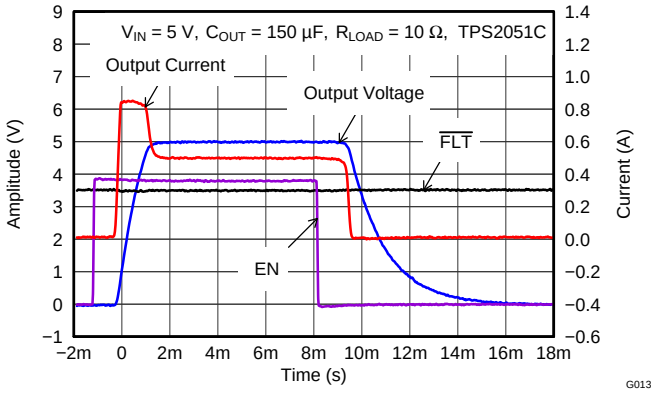


Figure 21. TPS2051C Turn ON into 10Ω

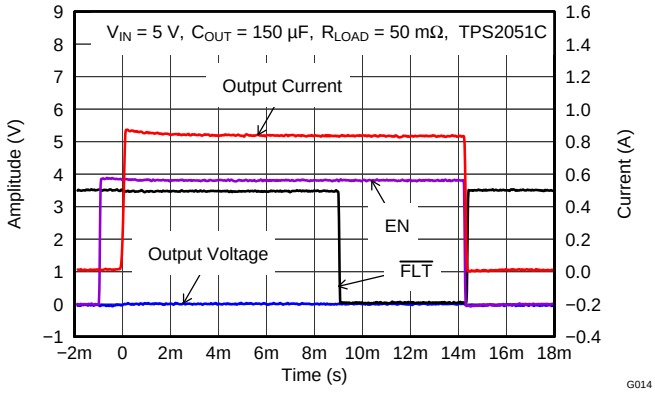


Figure 22. TPS2051C Enable into Short

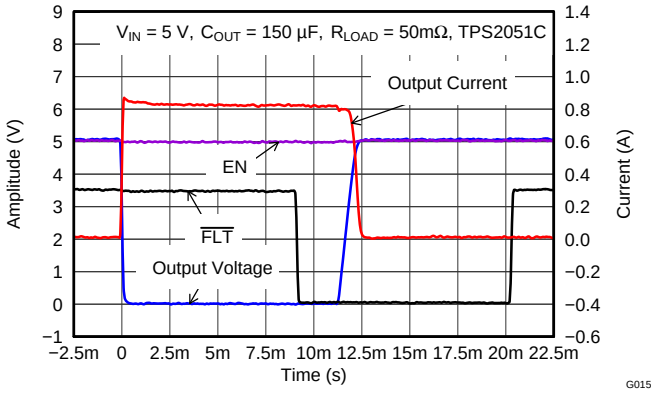


Figure 23. TPS2051C Pulsed Output Short

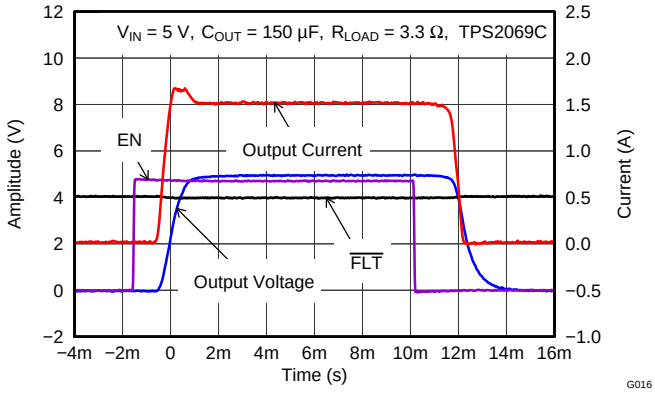


Figure 24. TPS2069CDGN Turn ON into 10Ω

TYPICAL CHARACTERISTICS (continued)

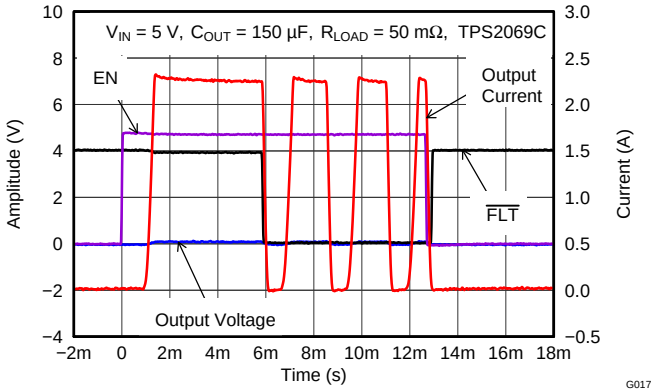


Figure 25. TPS2069CDGN Enable into Short

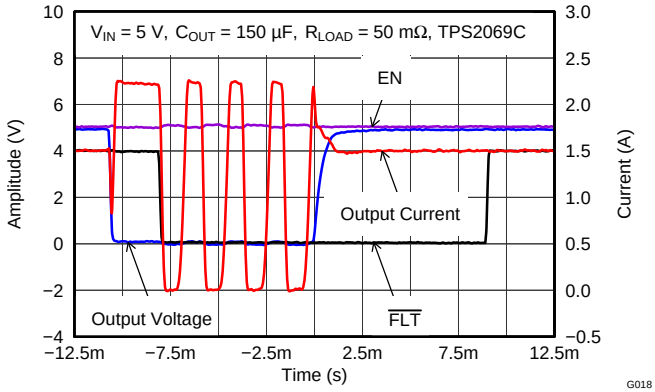


Figure 26. TPS2069CDGN Pulsed Output Short

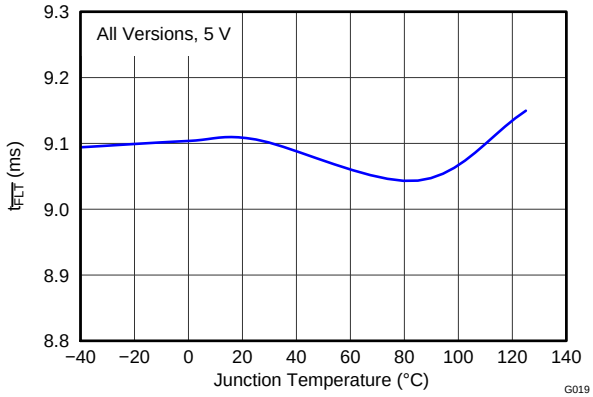


Figure 27. Deglitch Period ($t_{\overline{FLT}}$) vs Temperature

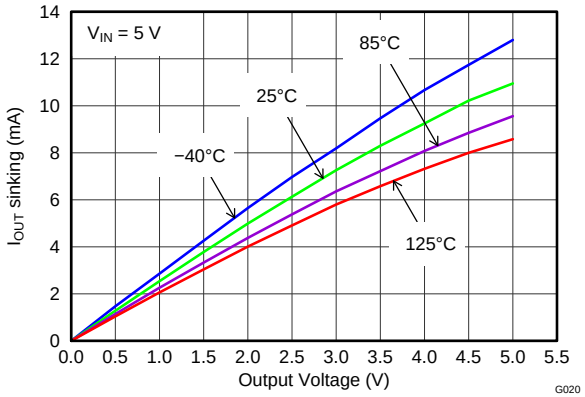


Figure 28. Output Discharge Current vs Output Voltage

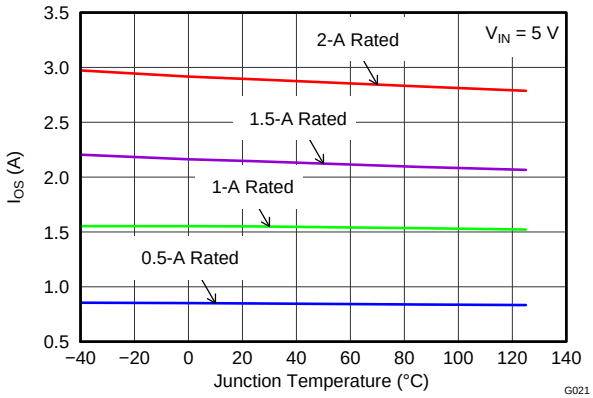


Figure 29. Short Circuit Current (I_{OS}) vs Temperature

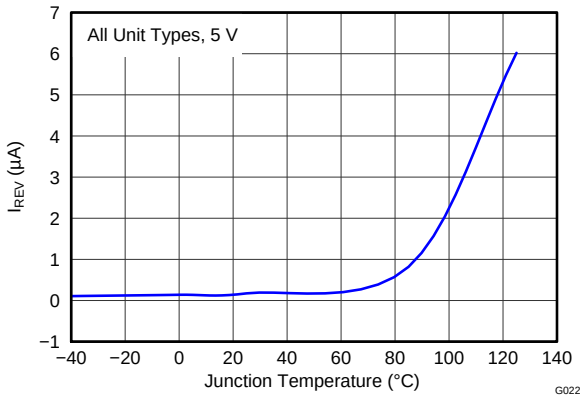


Figure 30. Reverse Leakage Current (I_{REV}) vs Temperature

TYPICAL CHARACTERISTICS (continued)

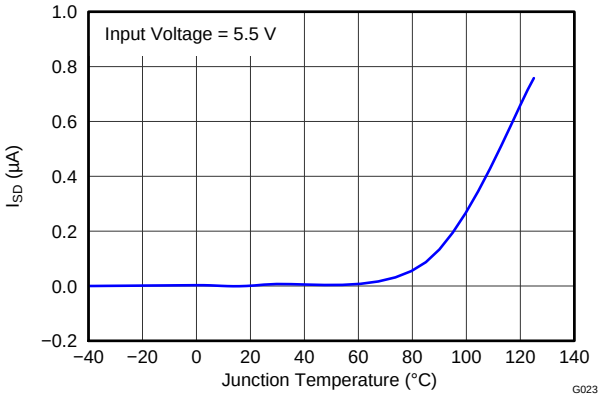


Figure 31. Disabled Supply Current (I_{SD}) vs Temperature

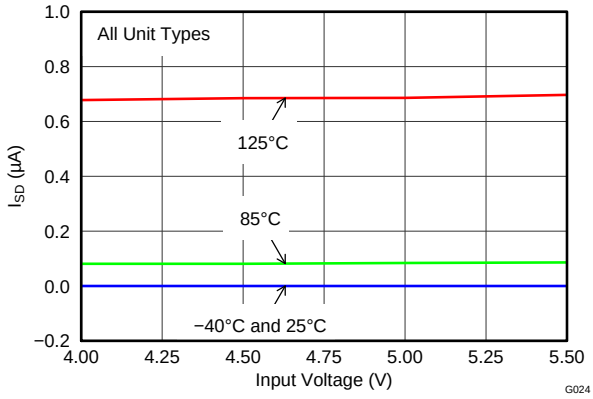


Figure 32. Disabled Supply Current (I_{SD}) vs Input Voltage

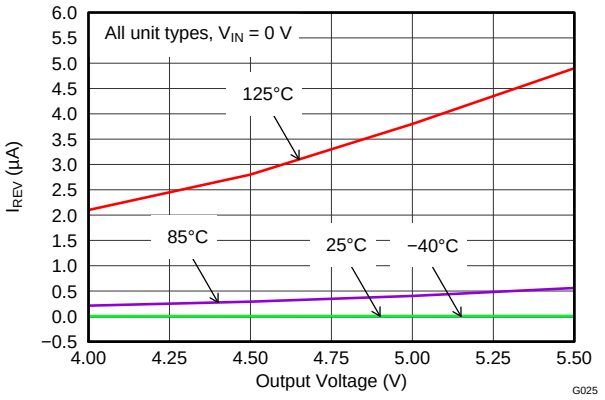


Figure 33. Reverse Leakage Current (I_{REV}) vs Output Voltage

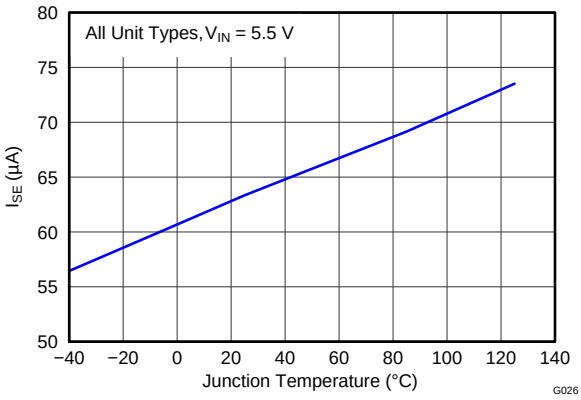


Figure 34. Enabled Supply Current (I_{SE}) vs Temperature

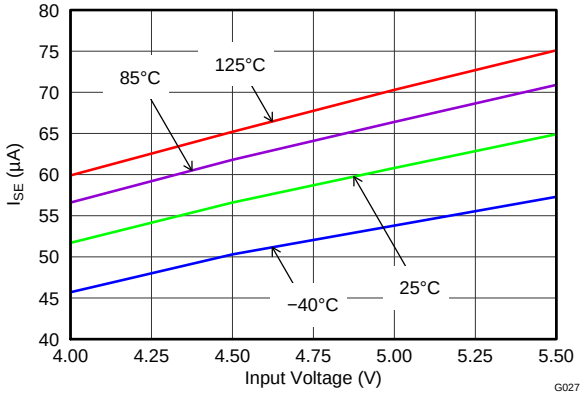


Figure 35. Enabled Supply Current (I_{SE}) vs Input Voltage

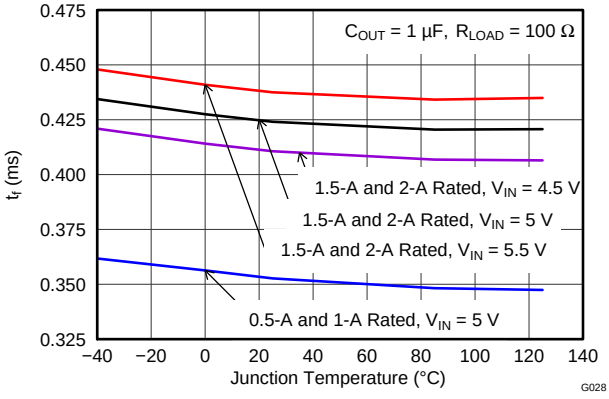


Figure 36. Output Fall Time (t_F) vs Temperature

TYPICAL CHARACTERISTICS (continued)

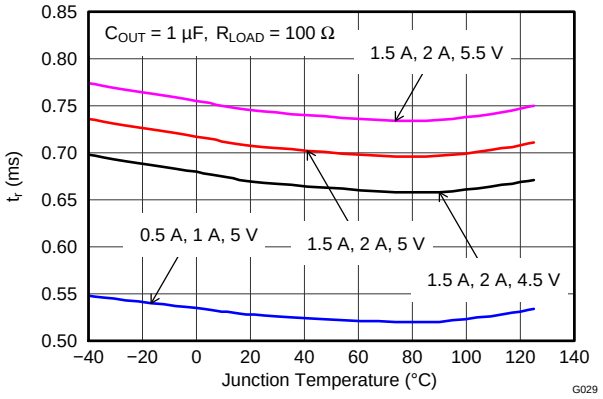


Figure 37. Output Rise Time (t_R) vs Temperature

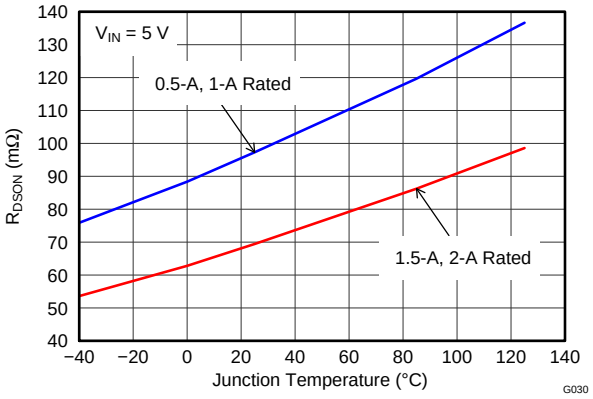


Figure 38. Input-Output Resistance ($R_{DS(ON)}$) vs Temperature

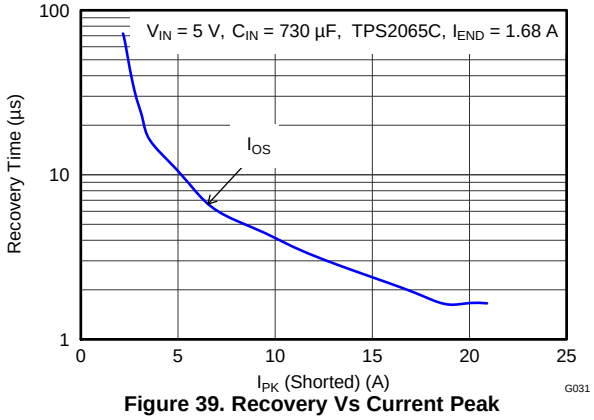


Figure 39. Recovery Vs Current Peak

DETAILED DESCRIPTION

The TPS20xxC are current-limited, power-distribution switches providing between 0.5 A and 2 A of continuous load current in 5 V circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. They are designed for applications where short circuits or heavy capacitive loads will be encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, over-temperature protection, and deglitched fault reporting.

UVLO

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges. $\overline{FLT}$ is high impedance when the TPS20xxC is in UVLO.

ENABLE

The logic enable input (EN, or $\overline{EN}$), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPS20xxC is disabled. Disabling the TPS20xxC will immediately clear an active $\overline{FLT}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPS20xxC and the external loading (especially capacitance). The fall time is controlled by the TPS20xxC, the loading (R and C), and the output discharge (R_{PD}). An output load consisting of only a resistor will experience a fall time set by the TPS20xxC. An output load with parallel R and C elements will experience a fall time determined by the (R × C) time constant if it is longer than the TPS20xxC's t_F.

The enable should not be left open, and may be tied to VIN or GND depending on the device.

INTERNAL CHARGE PUMP

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch will block current from OUT to IN when turned off by the UVLO or disabled.

CURRENT LIMIT

The TPS20xxC responds to overloads by limiting output current to the static I_{OS} levels shown in the Electrical Characteristics table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur.

The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$), or 2) input voltage is present and the TPS20xxC is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS20xxC ramps the output current to I_{OS}. The TPS20xxC will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 11 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 6 and Figure 7) when the specified overload (per Electrical Characteristics table) is applied. The response speed and shape will vary with the overload level, input circuit, and rate of application. The current-limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS20xxC will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated by Figure 12, Figure 13, and Figure 14.

The TPS20xxC thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) x I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPS20xxC. Many older designs have an output I vs V characteristic similar to the plot labeled "Current Limit with Peaking" in Figure 40. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS20xxC family of parts does not present noticeable peaking in the current limit, corresponding to the characteristic labeled "Flat Current Limit" in Figure 40. This is why the I_{OC} parameter is not present in the Electrical Characteristics tables.

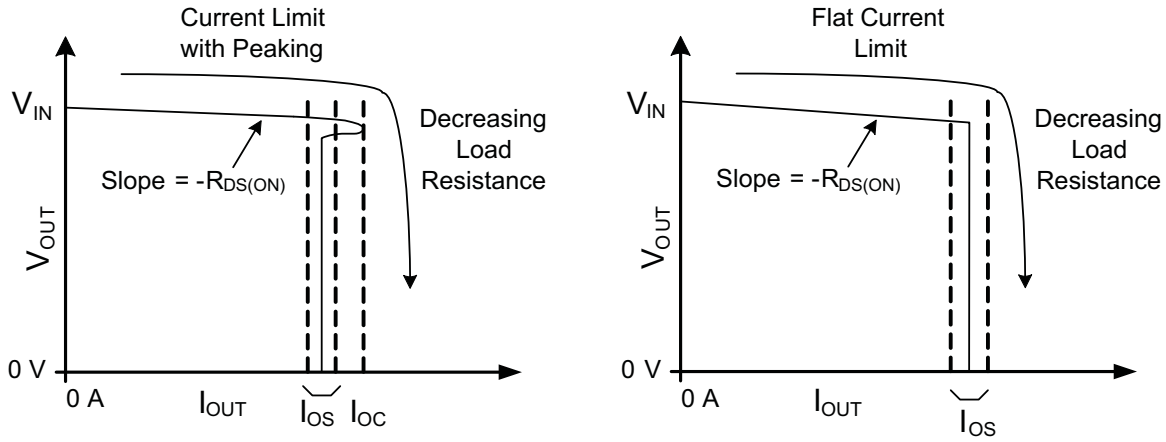


Figure 40. Current Limit Profiles

$\overline{\text{FLT}}$

The $\overline{\text{FLT}}$ open-drain output is asserted (active low) during an overload or over-temperature condition. A 9 ms deglitch on both the rising and falling edges avoids false reporting at startup and during transients. A current limit condition shorter than the deglitch period will clear the internal timer upon termination. The deglitch timer will not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of $\overline{\text{FLT}}$ around I_{OS} as the ripple will drive the TPS20xxC in and out of current limit.

If the TPS20xxC is in current limit and the over-temperature circuit goes active, $\overline{\text{FLT}}$ will go true immediately (see Figure 12) however exiting this condition is deglitched (see Figure 14). $\overline{\text{FLT}}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS20xxC will clear an active $\overline{\text{FLT}}$ as soon as the switch turns off (see Figure 11). $\overline{\text{FLT}}$ is high impedance when the TPS20xxC is disabled or in under-voltage lockout (UVLO).

OUTPUT DISCHARGE

A 470Ω (typical) output discharge will dissipate stored charge and leakage current on OUT when the TPS20xxC is in UVLO or disabled. The pull-down circuit will lose bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V.

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits such as the TPS20xxC will have the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turn on). Theoretically, the peak voltage is 2 times the applied. The second cause is due to the abrupt reduction of output short circuit current when the TPS20xxC turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS20xxC output is shorted. Applications with large input inductance (e.g. connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current-limit speed of the TPS20xxC to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1µF to 22µF adjacent to the TPS20xxC input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS20xxC has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120 µF minimum output capacitance is required. Typically a 150 µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, a minimum of 10 µF ceramic capacitance on the output is recommended. The voltage undershoot should be controlled to less than 1.5 V for 10 µs.

POWER DISSIPATION AND JUNCTION TEMPERATURE

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS20xxC. The system designer can control choices of package, proximity to other power dissipating devices, and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. The lower junction temperatures achieved by soldering the pad improve the efficiency and reliability of both TPS20xxC parts and the system. The following examples were used to determine the θ_{JA}Custom thermal impedances noted in the THERMAL INFORMATION table. They were based on use of the JEDEC high-k circuit board construction (2 signal and 2 plane) with 4, 1oz. copper weight, layers.

While it is recommended that the DGN package PAD be soldered to circuit board copper fill and vias for low thermal impedance, there may be cases where this is not desired. For example, use of routing area under the IC. The TPS20xxC will operate properly with the pad not connected to GND. θ_{JA} for a 4 layer board with the pad not soldered is approximately 141°C/W for the 0.5-A and 1-A rated parts and 139°C/W for the 1.5-A and 2-A rated parts. These values may be used in Equation 1 below to determine the maximum junction temperature.

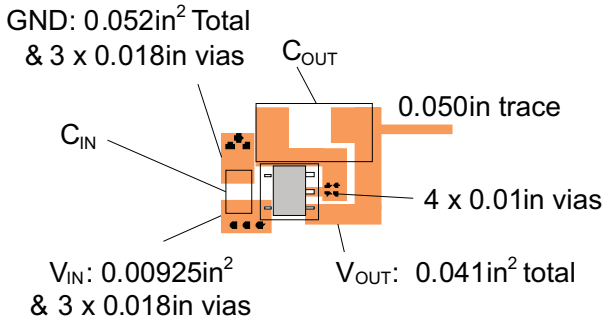


Figure 41. DBV Package PCB Layout Example

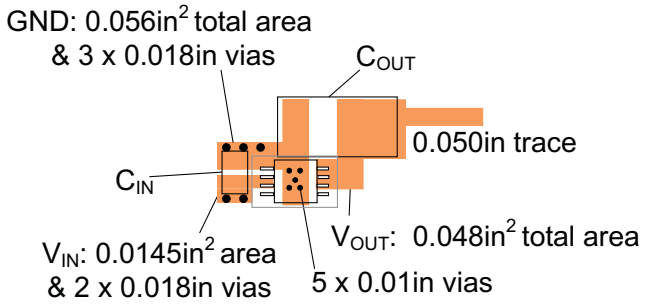


Figure 42. DGN Package PCB Layout Example

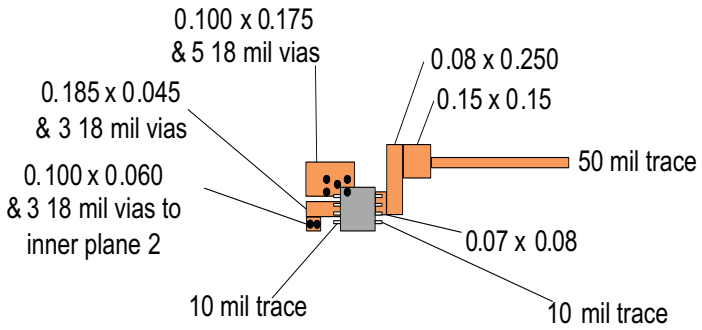


Figure 43. DGK Package PCB Layout Example

The following procedure requires iteration because power loss is due to the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(ON)}$ at 125°C from the TYPICAL CHARACTERISTICS, and the preferred package thermal resistance for the preferred board construction from the THERMAL INFORMATION table.

$$T_J = T_A + ((I_{OUT2} \times R_{DS(ON)}) \times \theta_{JA}) \quad (1)$$

Where:

I_{OUT} = rated OUT pin current (A)
$R_{DS(ON)}$ = Power switch on-resistance at an assumed T_J (Ω)
T_A = Maximum ambient temperature (°C)
T_J = Maximum junction temperature (°C)
θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction and/or package with lower θ_{JA} .

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Changed the TPS2051C, TPS2065C, and TPS2069C Devices Status From: Preview To: Active 1
- Corrected pinout numbers for the 5-PIN PACKAGE 6

Changes from Revision A (July 2011) to Revision B **Page**

- Added the DGK Package Information throughout the data sheet 1
- Changed title of Figure 15 From: NEW FIG To: TPS2065C 50 Ω Short Circuit 8

Changes from Revision B (September 2011) to Revision C **Page**

- Changed TPS2000C (MSOP-8) status From: Preview To: Active in Table 1 1
- Changed From: PXF1 To: PXFI and From: PSG1 To: PXGI in the DEVICE INFORMATION table MOSP-8 (DGK) column 2
- Changed the θJACustom 2 A Rated DGK value from N/A to 110.3 2
- Added Figure 43 - DGK Package PCB Layout Example 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2000CDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
TPS2000CDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
TPS2000CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2000CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2001CDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
TPS2001CDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
TPS2001CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2001CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2051CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2051CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2065CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2065CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2065CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2065CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2069CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2069CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:

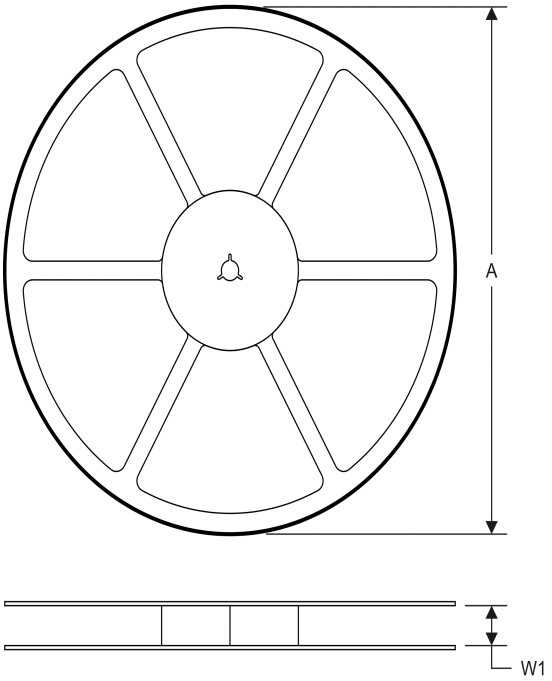
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

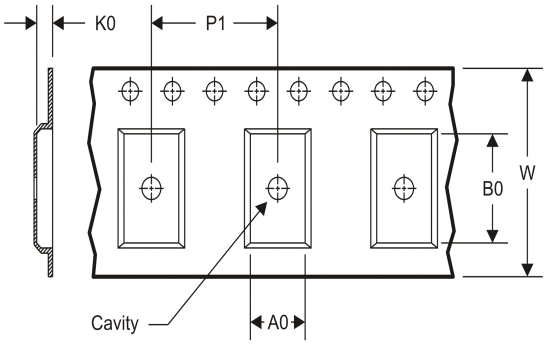
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

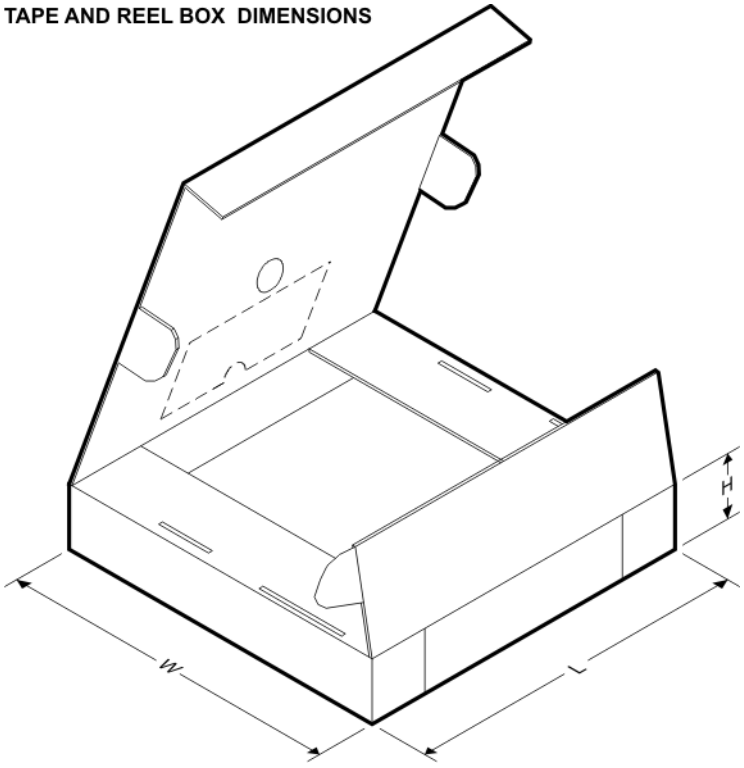
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2000CDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2000CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2000CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2001CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2051CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2065CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2069CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

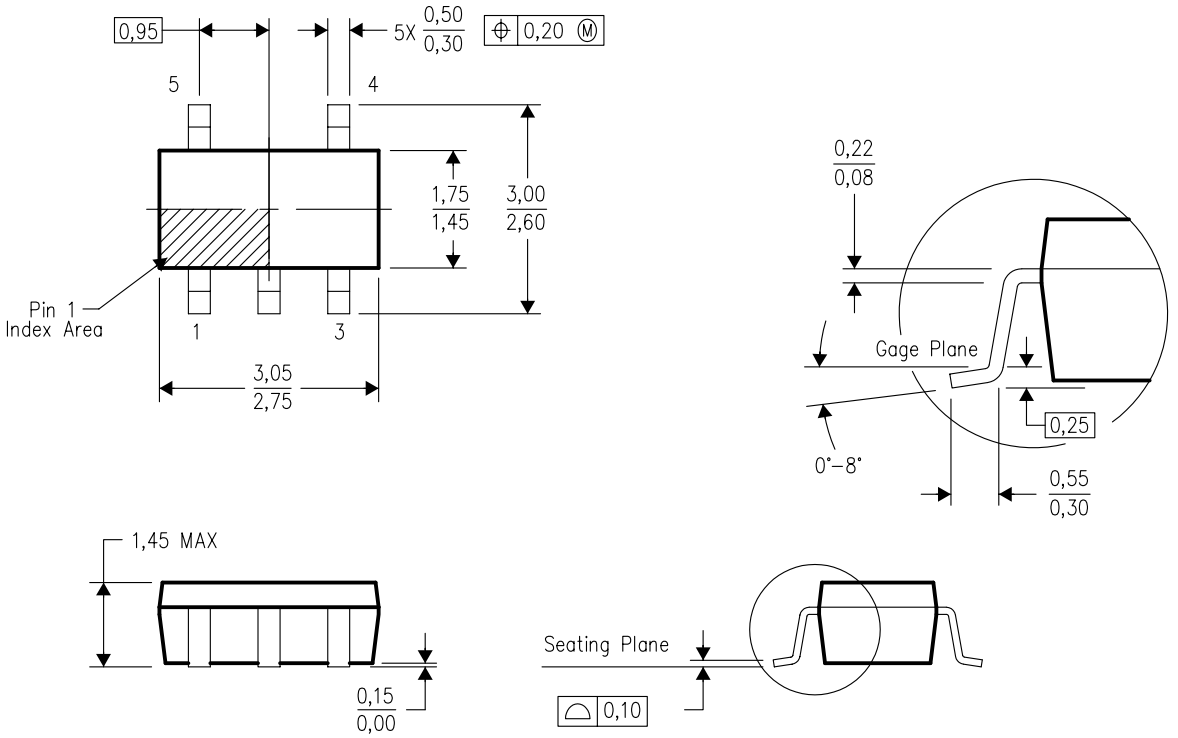
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2000CDGKR	MSOP	DGK	8	2500	366.0	364.0	50.0
TPS2000CDGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2000CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2001CDGKR	MSOP	DGK	8	2500	366.0	364.0	50.0
TPS2001CDGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2001CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2051CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2065CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2069CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2069CDGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0

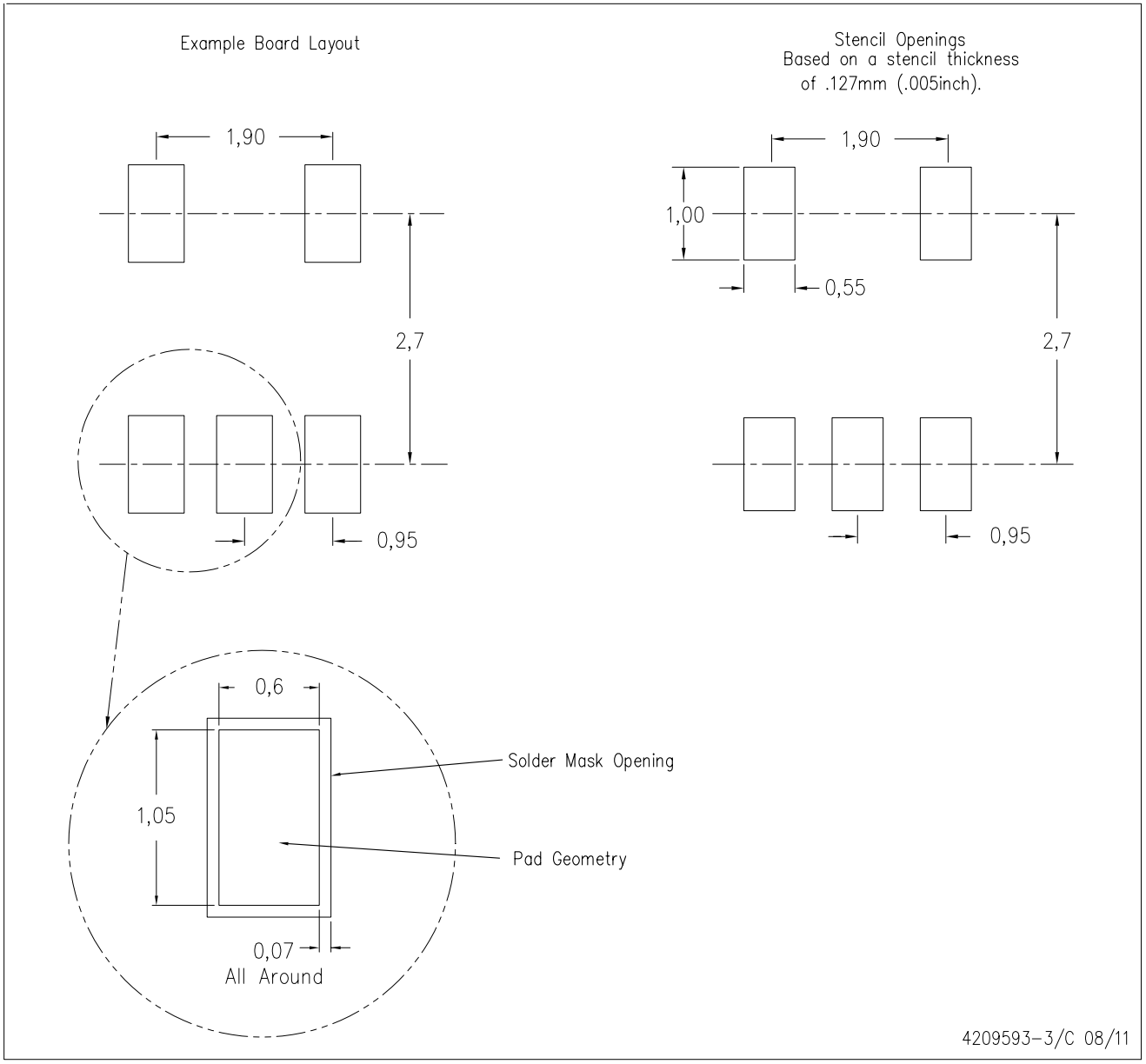
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

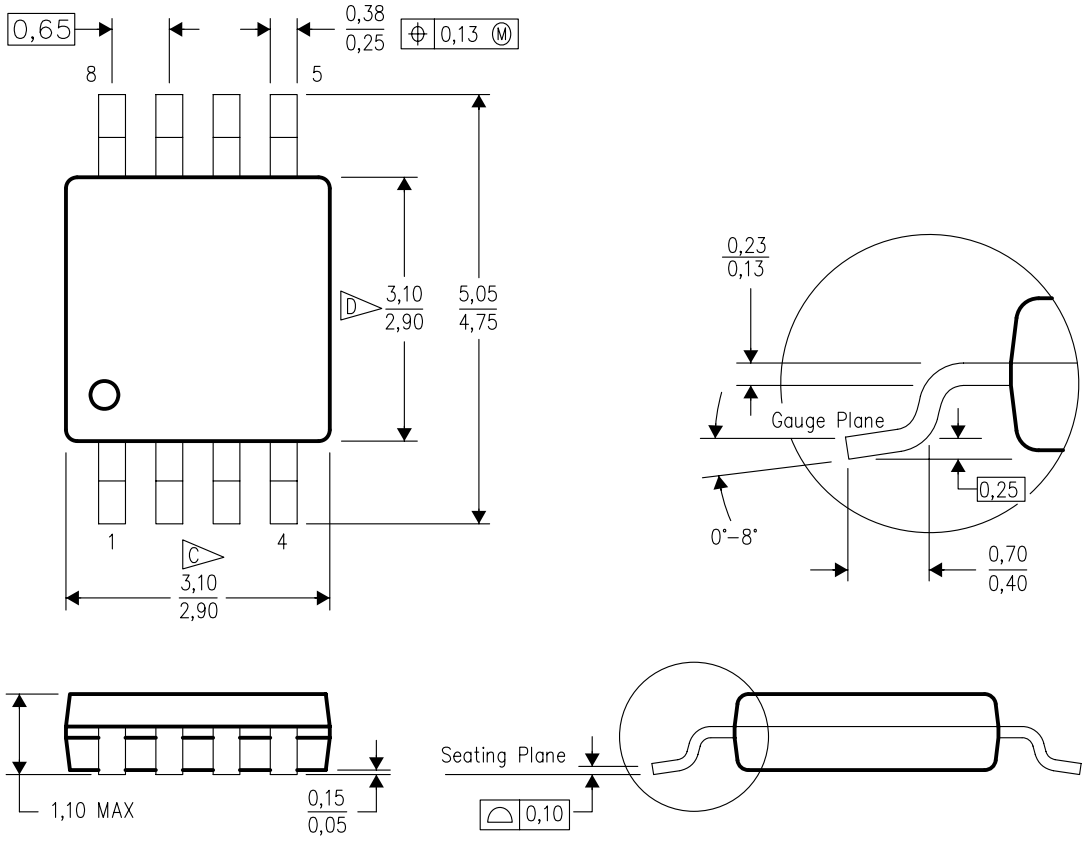
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

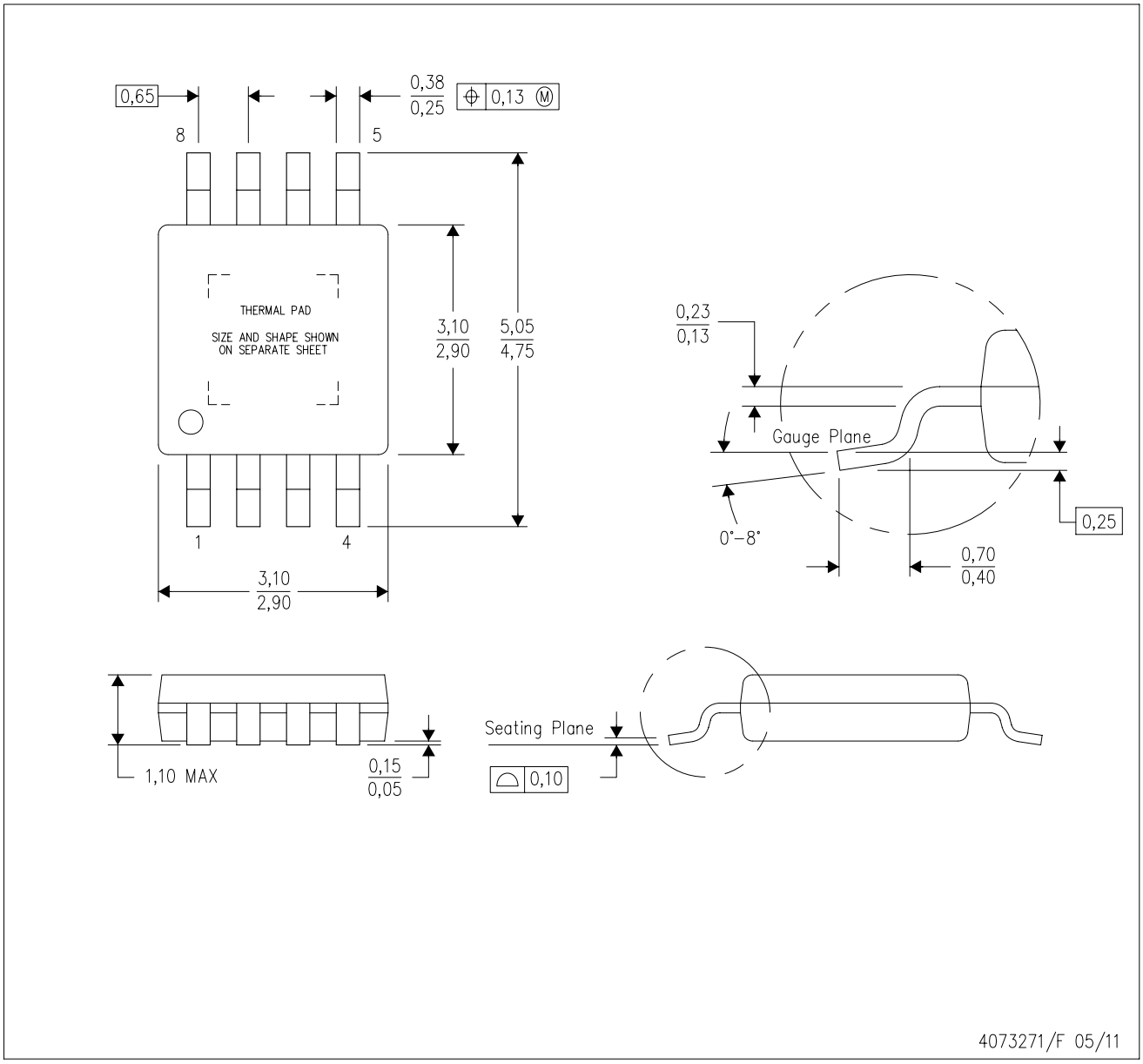
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

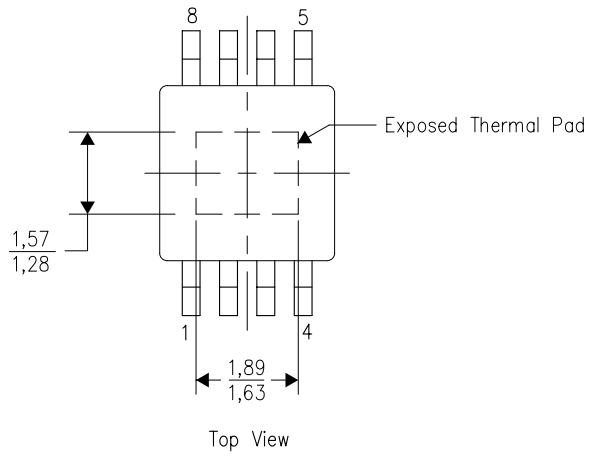
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

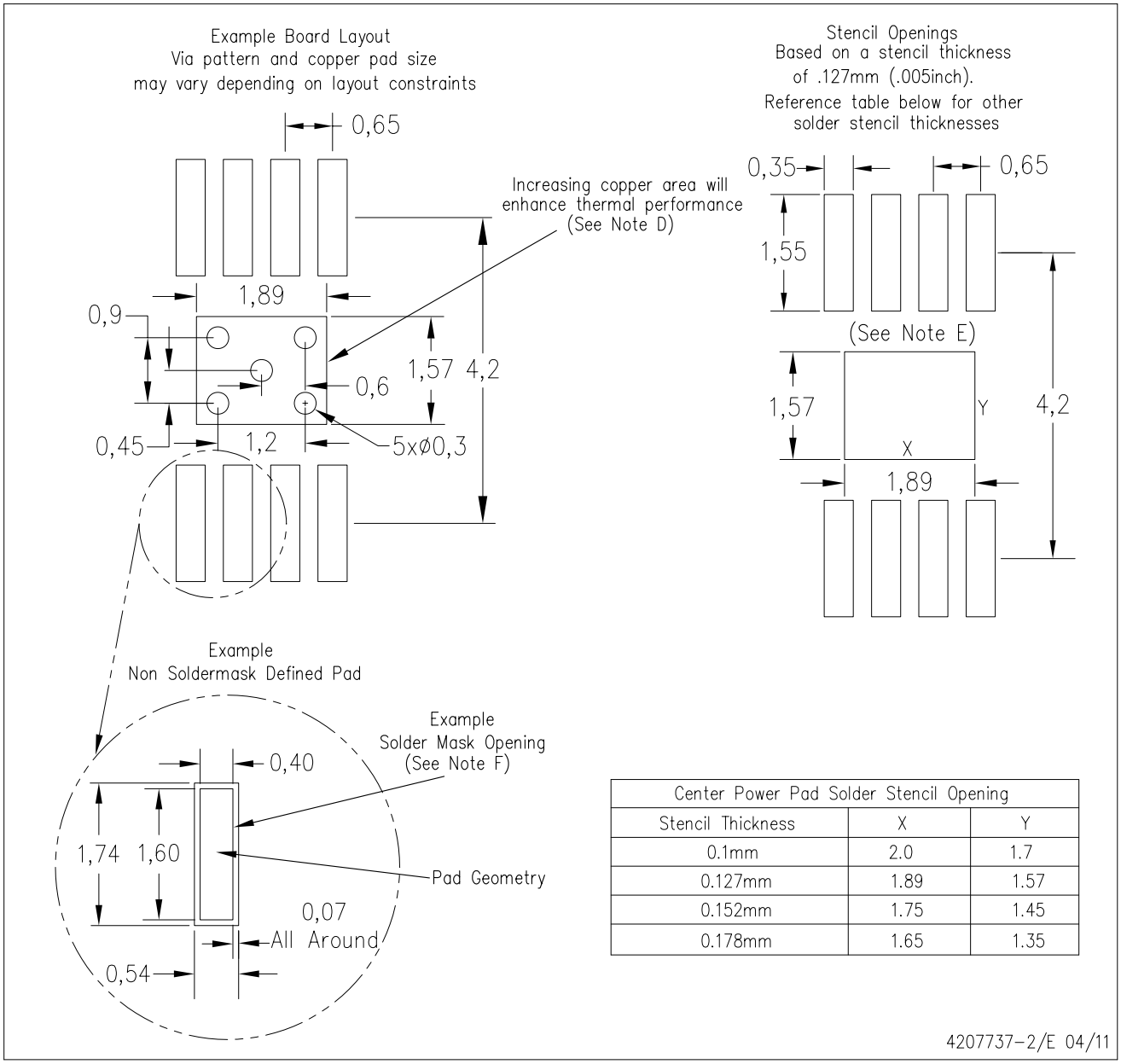
Exposed Thermal Pad Dimensions

4206323–2/H 05/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/E 04/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

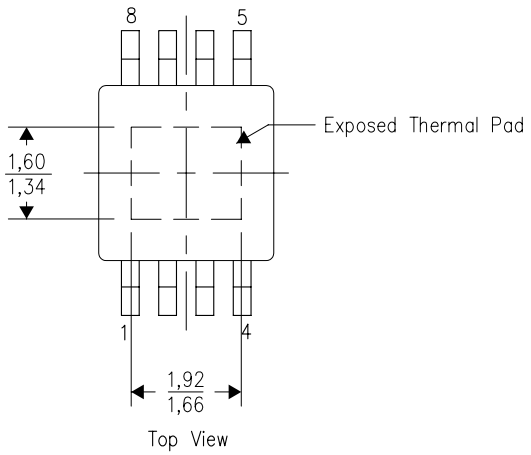
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323–4/H 05/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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