256-TAPS DUAL CHANNEL DIGITAL POTENTIOMETER WITH SPI INTERFACE AND NON-VOLATILE MEMORY

Check for Samples: TPL0202

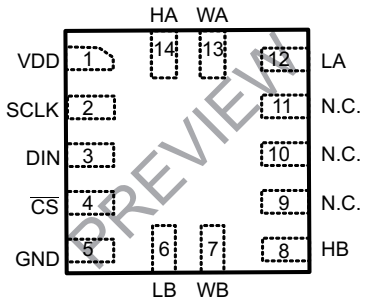
FEATURES

- **Dual Channel, 256-Position Resolution**
- **Non-volatile Memory Stores Wiper Settings**
- **2mm x 2mm, 14-pin MicroQFN or 3mm x 3mm, 16-pin QFN Packages**
- **10 kΩ End-to-End Resistance (TPL0202-10)**
- **Fast Power-up Response Time: <100µs**
- **±1 LSB INL, ±0.5 LSB DNL (Voltage-Divider Mode)**
- **12 ppm/°C Ratiometric Temperature Coefficient**
- **SPI-Compatible Serial Interface**
- **2.7 V to 5.5 V Single-Supply Operation**
- **Operating Temperature Range From -40°C to +85°C**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human Body Model (A114-B, Class II)**

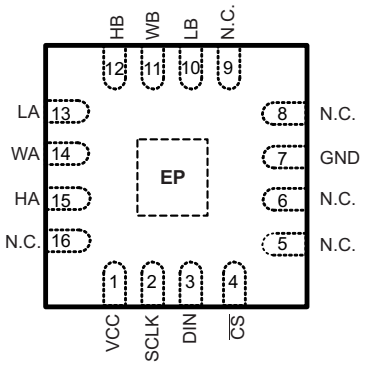
APPLICATIONS

- **Adjustable Gain Amplifiers and Offset Trimming**
- **Adjustable Power Supplies**
- **Precision Calibration of Set Point Thresholds**
- **Sensor Trimming and Calibration**
- **Mechanical Potentiometer Replacement**

MicroQFN - RUC PACKAGE
(TOP VIEW)



QFN - RTE PACKAGE
(TOP VIEW)



DESCRIPTION

The TPL0202 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0202-10 has an end-to-end resistance of 10kΩ.

The TPL0202 has non-volatile memory (EEPROM) which can be used to store the wiper position. The internal registers of the TPL0202 can be accessed using a SPI-compatible digital interface.

The TPL0202 is available in a 14-pin MicroQFN (2mm x 2mm) and 16-pin QFN (3mm x 3mm) package with a specified temperature range of -40°C to +85°C.

ORDERING INFORMATION

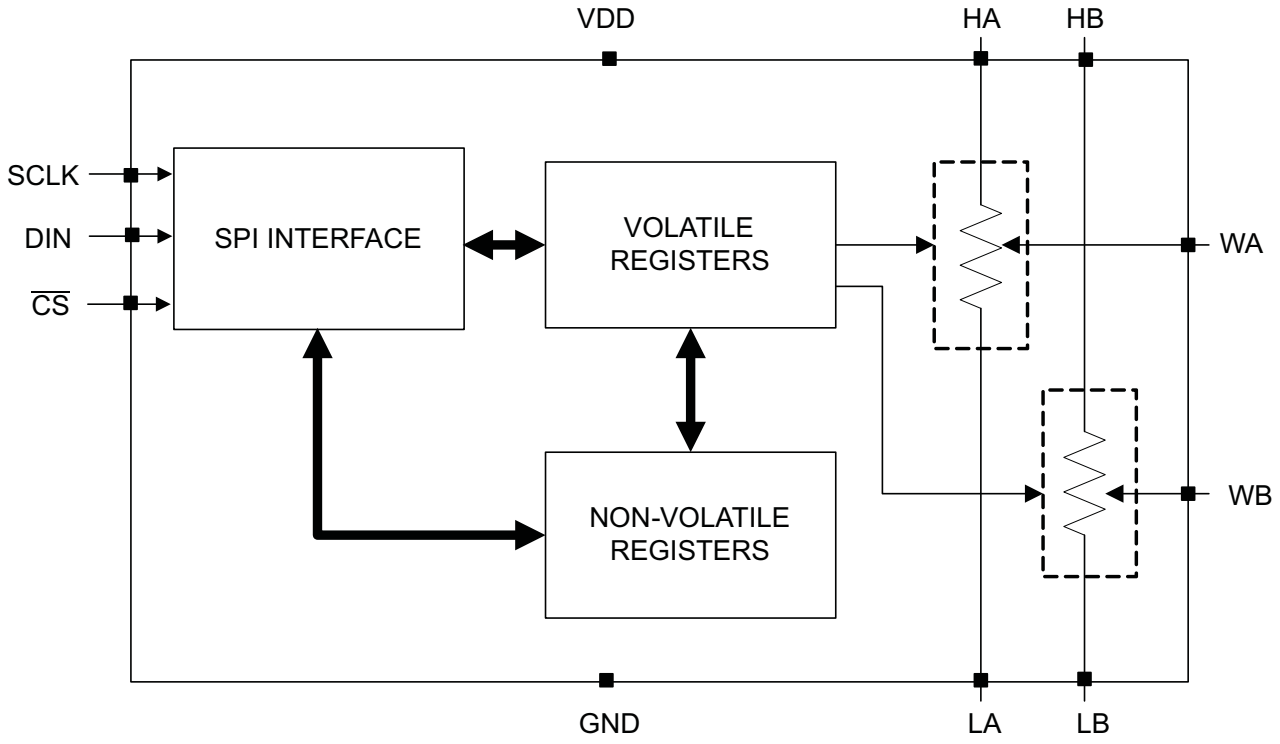
T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RTE	Tape and reel	TPL0202-10MRTER	ZUR
	QFN – RUC		TPL0202-10RUCR	TBD

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. Summary of Features

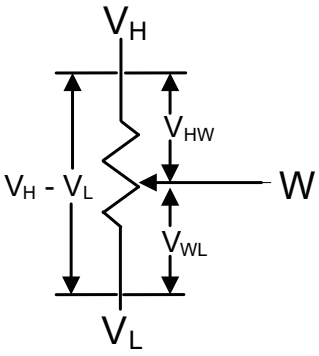
Feature	TPL0202-10
# of Potentiometers	2
Digital Interface	SPI
Steps	256
Wiper Memory	Non-Volatile
Taper	Linear
End-to-end Resistance	10kΩ
End-to-end Resistance Tolerance	20%
Wiper Resistance	25 Ω (typ)
Smallest Package Size	MicroQFN (RUC): 4 mm^2

FUNCTIONAL BLOCK DIAGRAM



DIGITAL POTENTIOMETER CONFIGURATIONS

VOLTAGE DIVIDER MODE

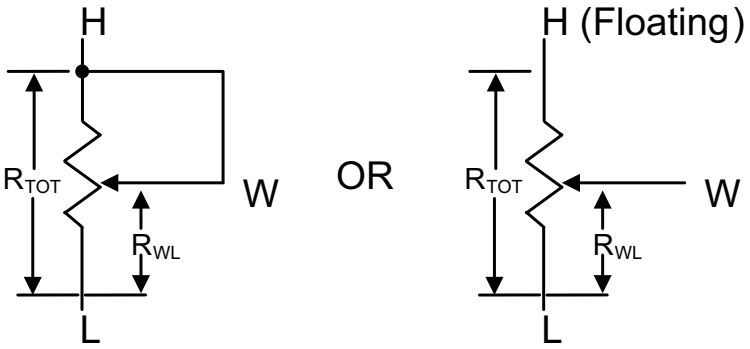


$V_{HW} = (V_H – V_L) \times (1 – (D/256))$

$V_{WL} = (V_H – V_L) \times D/256$

Where D = Decimal Value of Wiper Code

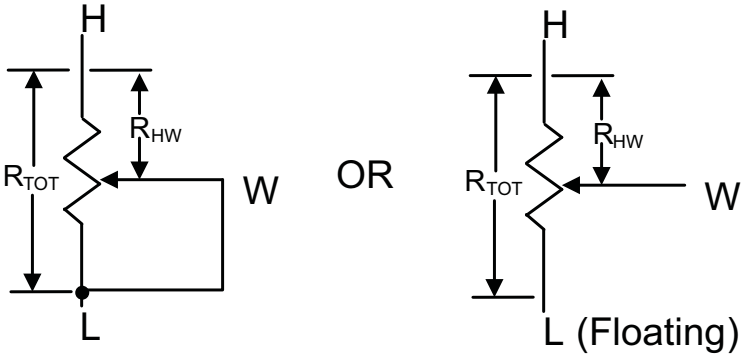
RHEOSTAT MODE A



$R_{WL} = R_{TOT} \times D/256$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE B



$R_{HW} = R_{TOT} \times (1 – (D/256))$

Where D = Decimal Value of Wiper Code

Figure 1. DPOT Configurations

Table 2. PIN DESCRIPTION TABLE

16 RTE		I/O	DESCRIPTION	14 RUC		I/O	DESCRIPTION
NO.	NAME			NO.	NAME		
1	N.C.		Not internally connected	1	VDD	Power	Supply Voltage
2	SCLK	Input	SPI Clock	2	SCLK	Input	SPI Clock
3	DIN	Input	SPI Input	3	DIN	Input	SPI Input
4	$\overline{CS}$	Input	SPI Chip Select (Active Low)	4	$\overline{CS}$	Input	SPI Chip Select (Active Low)
5	N.C.		Not internally connected	5	GND	Ground	Ground
6	N.C.		Not internally connected	6	LB	I/O	Low terminal of Potentiometer B
7	GND	Ground	Ground	7	WB	I/O	Wiper terminal of Potentiometer B
8	N.C.		Not internally connected	8	HB	I/O	High terminal of Potentiometer B
9	N.C.		Not internally connected	9	N.C.		Not internally connected
10	LB	I/O	Low terminal of Potentiometer B	10	N.C.		Not internally connected
11	WB	I/O	Wiper terminal of Potentiometer B	11	N.C.		Not internally connected
12	HB	I/O	High terminal of Potentiometer B	12	LA	I/O	Low terminal of Potentiometer A
13	LA	I/O	Low terminal of Potentiometer A	13	WA	I/O	Wiper terminal of Potentiometer A
14	WA	I/O	Wiper terminal of Potentiometer A	14	HA	I/O	High terminal of Potentiometer A
15	HA	I/O	High terminal of Potentiometer A				
16	N.C		Not internally connected				
EP	EP		Exposed Thermal Pad. Can be connected to GND or left unconnected.				

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{DD,GND}$			2.7	5.5	V
V_H, V_L, V_W	Terminal Voltage Range		0	V_{DD}	V
V_{IH}	Voltage Input High (SCLK, DIN, CS)	V_{DD} = 3.6 V to 5.5 V	2.4	5.5	V
		V_{DD} = 2.7 V to 3.6 V	0.7 × V_{DD}	5.5	
V_{IL}	Voltage Input Low (SCLK, DIN, CS)		0	0.8	V
I_W	Wiper Current			±2	mA
T_A	Ambient Temperature		–40	85	°C

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD} to GND	Supply voltage range		–0.3	7	V
All other pins to GND			–0.3	V_{DD} + 0.3	
I_L I_W I_H	Pulse Current			±20	mA
	Continuous Current	TPL0202-10		±2	mA
θ_{JA}	Package Thermal Impedance(4)	RTE package		56.4	°C/W
		RUC package		216.7	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

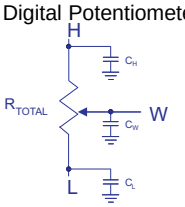
V_{DD} = 2.7V to 5.5V, T_A=-40°C to 85°C (unless otherwise noted). Typical values are at V_{DD}=5V, T_A=25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TOT}	End-to-end Resistance (Between H and L Terminals)		8	10	12	kΩ
V_H, V_L	Terminal voltage range		0		V_{DD}	V
R_H, R_L	Terminal resistance			60	200	Ω
R_W	Wiper resistance			25	100	Ω
C_H, C_L (1)(2)	Terminal capacitance			22		pF
C_W (1)(2)	Wiper capacitance			18		pF
I_{LKG}	Terminal Leakage Current	V_H = V_{SS} to V_{DD}, V_L = Floating OR V_L = V_{SS} to V_{DD}, V_H = Floating		0.1	1	µA
TC_R	Resistance temperature coefficient	Input Code = 0x80h		132		ppm/°C
$R_{TOT,MATCH}$	Channel-to-channel resistance match			0.1		%
Voltage Divider Mode						
INL (3)(4)	Integral non-linearity		–1		1	LSB
DNL (3)(5)	Differential non-linearity		–0.5		0.5	LSB
ZS_{ERROR} (6)(7)	Zero-scale error		0	2	5	LSB
FS_{ERROR} (6)(8)	Full-scale error		–5	–2	0	LSB
V_{MATCH} (6)(9)	Channel-to-Channel matching	Wiper at the same tap position, same voltage all H and the same voltage at all L terminals	–2		2	LSB
TC_V	Ratiometric temperature coefficient	Wiper set at mid-scale		12		ppm/°C
BW	Bandwidth	Wiper set at mid-scale C_{LOAD} = 10 pF		2000		kHz
T_{SW}	Wiper setting time			0.4		µS
THD	Total harmonic distortion	V_H = 1 V_{RMS} at 1 kHz, V_L = V_{DD}/2, Measurement at W		0.03		%
X_{TALK}	Crosstalk	f_H = 1 kHz, V_L = GND, Measurement at W		–94		dB

(1) Terminal and Wiper Capacitance extracted from self admittance of three port network measurement

$$Y_{ii} = \frac{I_i}{V_i}\Big|_{V_k=0 \text{ for } k\neq i}$$

(2) Digital Potentiometer Macromodel



(3) LSB = ($V_{MEAS[code\ 255]}$ – $V_{MEAS[code\ 0]}$) / 255
(4) INL = (($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ 0]}$) / LSB) - [code x]
(5) DNL = (($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ x-1]}$) / LSB) – 1
(6) IDEAL_LSB = (V_H-V_L) / 256
(7) ZS_{ERROR} = $V_{MEAS[code\ 0]}$ / IDEAL_LSB
(8) FS_{ERROR} = [($V_{MEAS[code\ 255]}$ – (V_H-V_L)) / IDEAL_LSB] + 1
(9) V_{MATCH} = ($V_{MEAS\_A[code\ x]}$ – $V_{MEAS\_B[code\ x]}$) / IDEAL_LSB

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, T_A=-40°C to 85°C (unless otherwise noted). Typical values are at V_{DD}=5V, T_A=25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RHEOSTAT MODE (Measurements between W and L with H not connected, or between W and H with L not connected)						
RINL (10)(11)	Integral non-linearity		–1.5		1.5	LSB
RDNL (10)(12)	Differential non-linearity		–0.5		0.5	LSB
R_{OFFSET} (13)(14)	Offset		0	2.5	7	LSB
R_{MATCH} (13)(15)	Channel-to-Channel matching		–2		2	LSB
RBW	Bandwidth	Code = 0x00h, L Floating, Input applied to W, Measure at H, C_{LOAD} = 10 pF		400		kHz

(10) RLSB = ($R_{MEAS[code\ 255]}$ – $R_{MEAS[code\ 0]}$) / 255
(11) RINL =(($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ 0]}$) / RLSB) - [code x]
(12) RDNL =(($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ x-1]}$) / RLSB)– 1
(13) IDEAL_RLSB = R_{TOT} / 256
(14) R_{OFFSET} = $R_{MEAS[code\ 0]}$ / IDEAL_RLSB
(15) R_{MATCH} = ($R_{MEAS\_A[code\ x]}$ – $R_{MEAS\_B[code\ x]}$) / IDEAL_RLSB

OPERATING CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, V_H= V_{DD}, V_L= GND, T_A= -40°C to 85°C (unless otherwise noted). Typical values are at V_{DD}= 5V, T_A= 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(STBY)}$	V_{DD} supply current during standby	Digital Inputs = V_{DD} or GND		1	5	µA
I_{DD}	V_{DD} supply current during write cycle only	Digital Inputs = V_{DD} or GND			400	µA
I_{IN-DIG}	Digital pins leakage current (SCLK, DIN, $\overline{CS}$ inputs)		–1		1	µA
V_{POR}	Power-on recall voltage	Minimum V_{DD} at which memory recall occurs		2		V
EEPROM Specification						
	EEPROM endurance			100,000		Cycles
	EEPROM retention	T_A = 85 °C		100		Years
t_{BUSY}	Write NV register busy time			20		ms
t_{ACC}	Read NV register access time			40		ns
t_{WO}	Write wiper register to output delay			40		ns
t_D	Power-up Response Time (V_{DD} above V_{POR} to wiper register value recall completed)			35	100	µs
Serial Interface Specifications (SCLK, DIN, $\overline{CS}$ Inputs)						
V_{IH}	Input high voltage	V_{DD} = 3.6 V to 5.5 V	2.4		5.5	V
		V_{DD} = 2.7 V to 3.6 V	0.7 × V_{DD}		5.5	
V_{IL}	Input low voltage	SCLK, DIN, $\overline{CS}$ inputs	0		0.8	V
C_{IN}	Pin capacitance	SCLK, DIN, $\overline{CS}$ inputs		7		pF

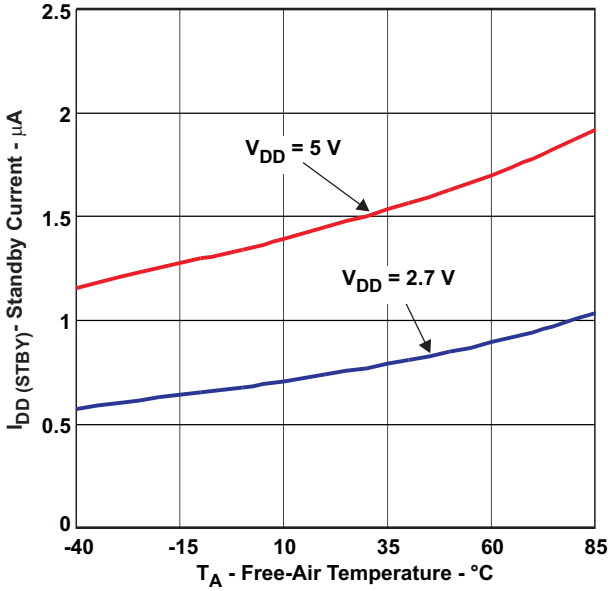
SPI INTERFACE TIMING REQUIREMENTS

V_{DD} = 2.7V to 5.5V, V_H= V_{DD}, V_L= GND, T_A= -40°C to 85°C (unless otherwise noted)

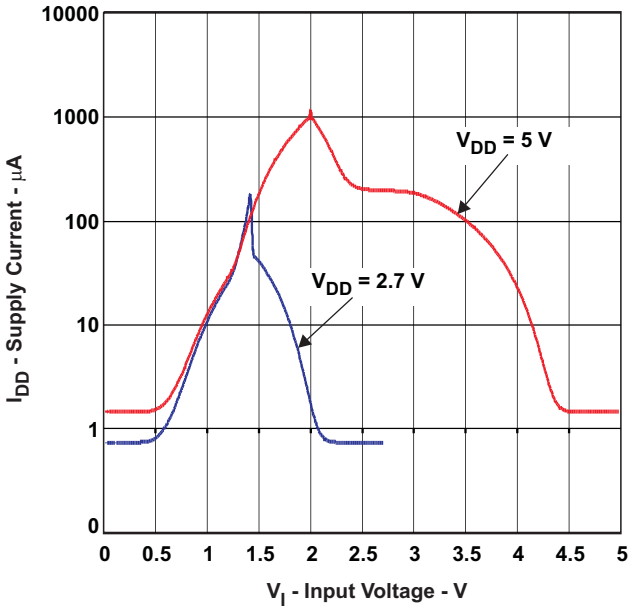
		MIN	TYP	MAX	UNIT
f_{SCLK}	SLCK frequency		5		MHz
t_{SCP}	SCLK period	200			ns
t_{SCH}	SCLK high time	80			ns
t_{SCL}	SCLK low time	80			ns
t_{CSS}	$\overline{CS}$ fall to SCLK rise setup time	80			ns
t_{CSH}	SCLK rise to $\overline{CS}$ hold time	0			ns
t_{DS}	DIN to SCLK setup time	50			ns
t_{DH}	DIN hold after SCLK rise to $\overline{CS}$ fall	0			ns
t_{CS0}	SCLK rise to $\overline{CS}$ fall	20			ns
t_{CS1}	$\overline{CS}$ rise to SCLK rise hold	80			ns
t_{CSW}	$\overline{CS}$ pulse width high	200			ns

TYPICAL PERFORMANCE CURVES

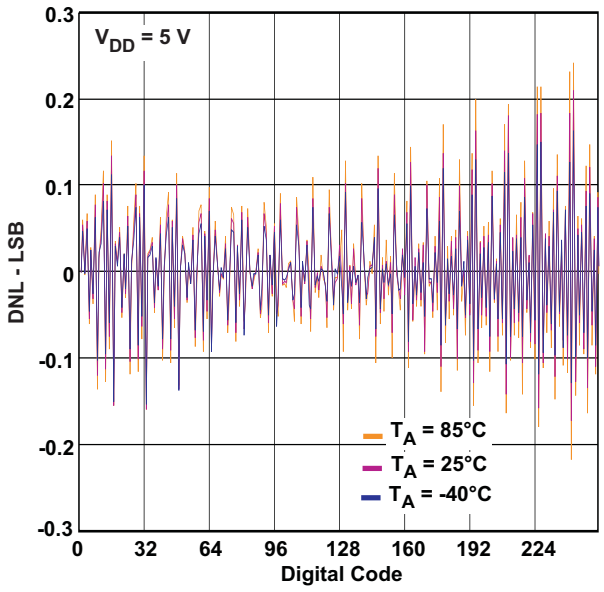
STANDBY CURRENT vs TEMPERATURE



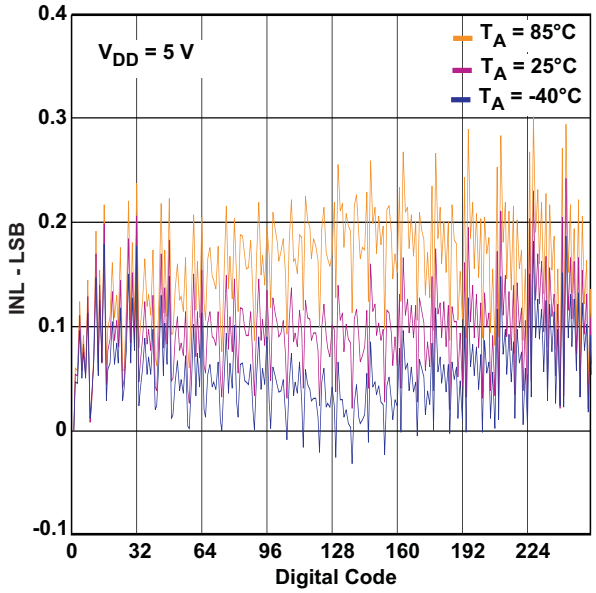
SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



VOLTAGE DIVIDER MODE DNL vs TEMPERATURE (V_{DD} = 5V)

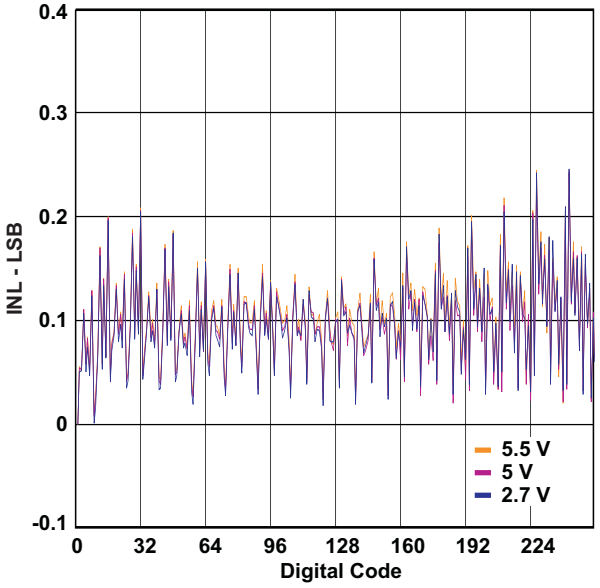


VOLTAGE DIVIDER MODE INL vs TEMPERATURE (V_{DD} = 5V)

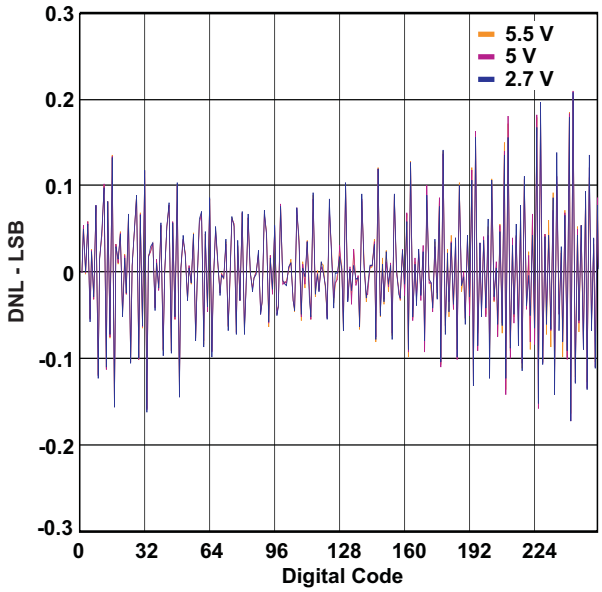


TYPICAL PERFORMANCE CURVES (continued)

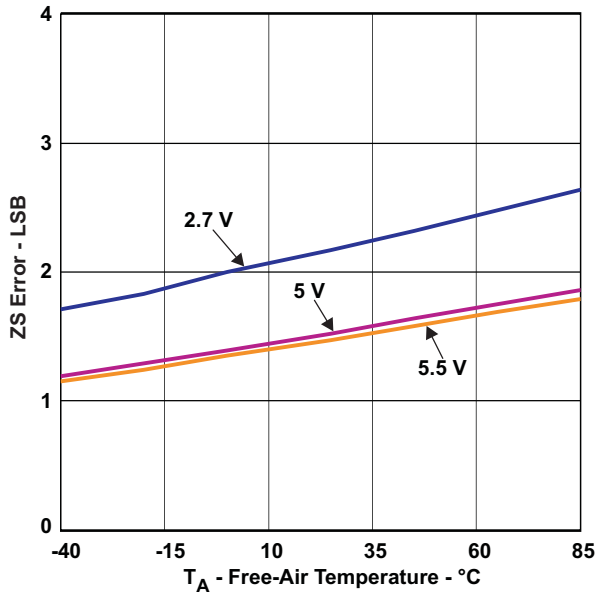
VOLTAGE DIVIDER MODE INL vs SUPPLY VOLTAGE (25°C)



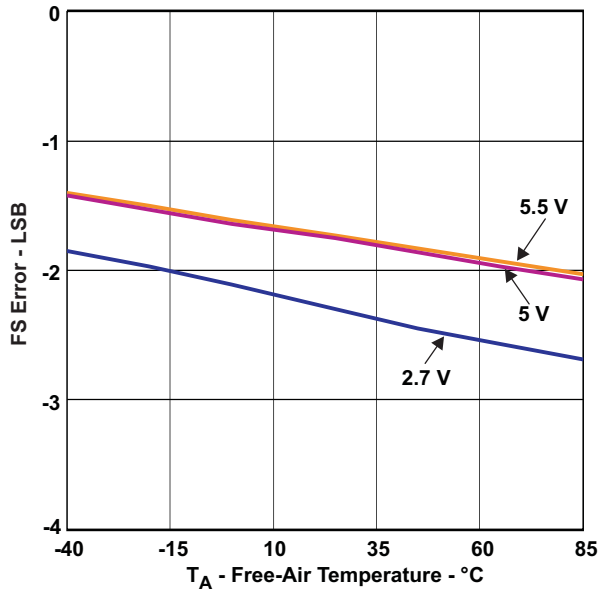
VOLTAGE DIVIDER MODE DNL vs SUPPLY VOLTAGE (25°C)



VOLTAGE DIVIDER MODE ZS ERROR vs TEMPERATURE

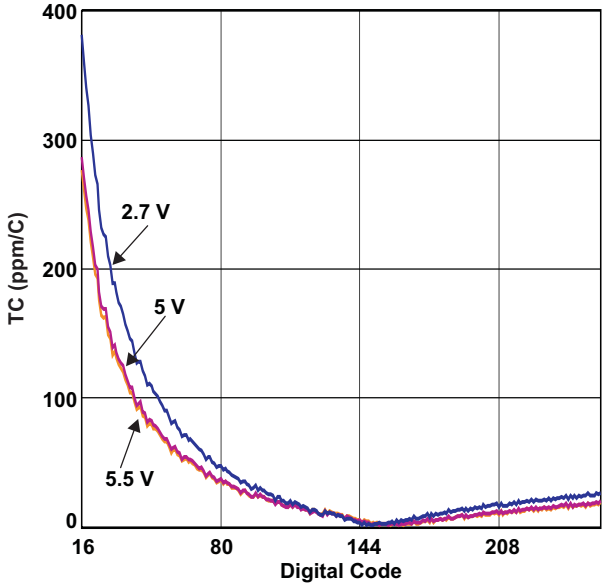


VOLTAGE DIVIDER MODE FS ERROR vs TEMPERATURE

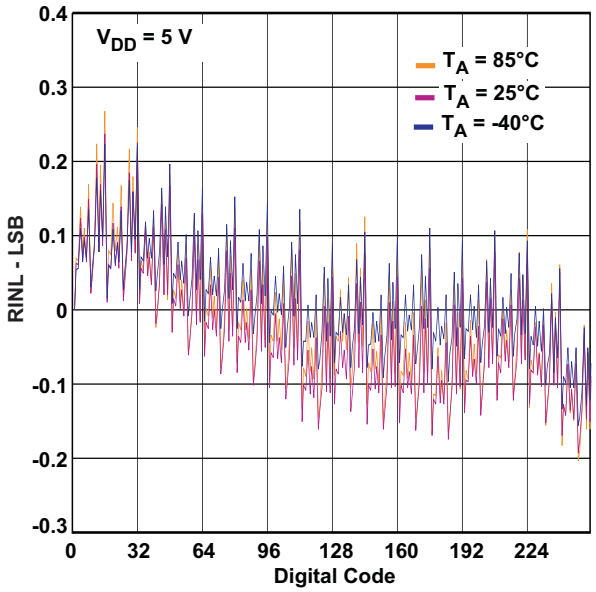


TYPICAL PERFORMANCE CURVES (continued)

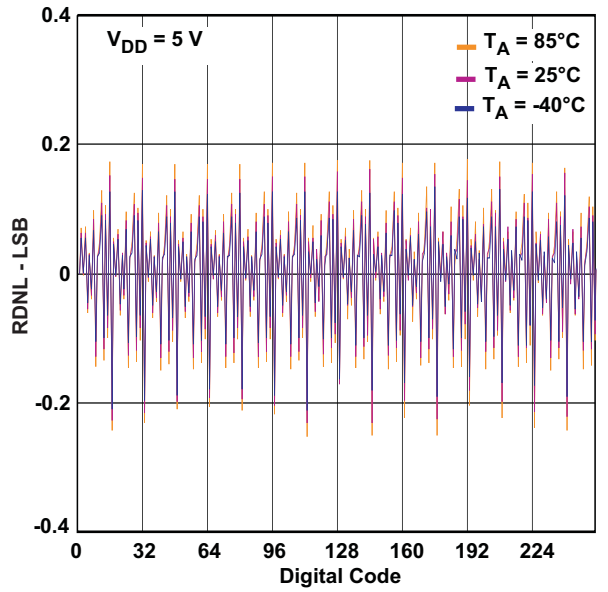
VOLTAGE DIVIDER MODE
vs
DIGITAL CODE



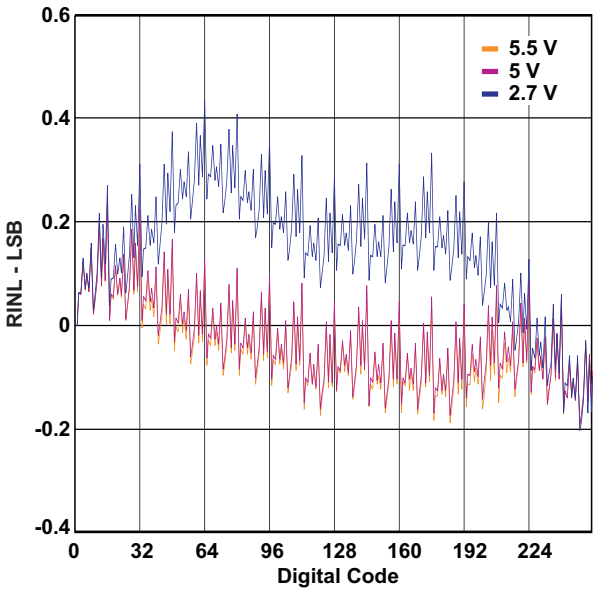
RHEOSTAT MODE RINL
vs
TEMPERATURE (V_{DD} = 5V)



RHEOSTAT MODE RDNL
vs
TEMPERATURE (V_{DD} = 5V)

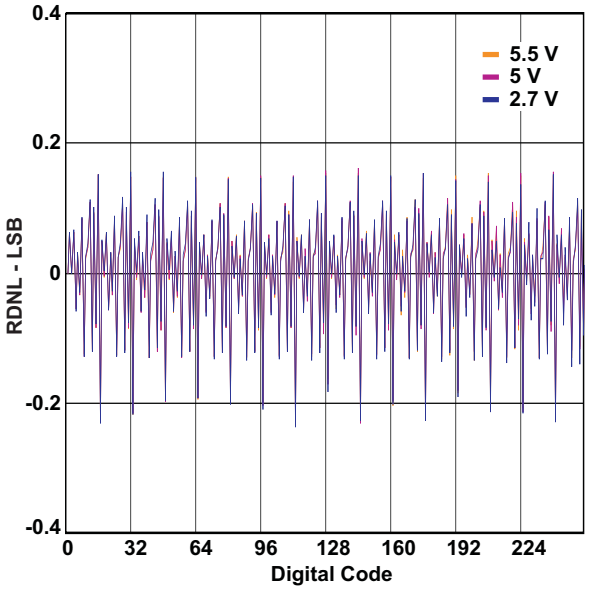


RHEOSTAT MODE RINL
vs
SUPPLY VOLTAGE (25°C)

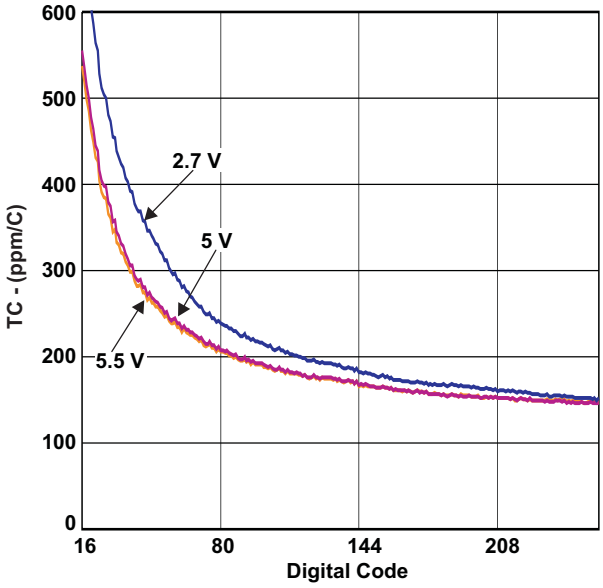


TYPICAL PERFORMANCE CURVES (continued)

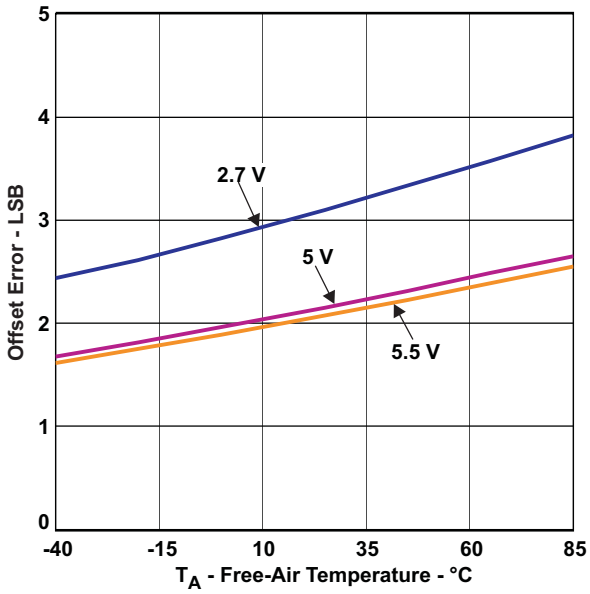
RHEOSTAT MODE RINL vs SUPPLY VOLTAGE (25°C)



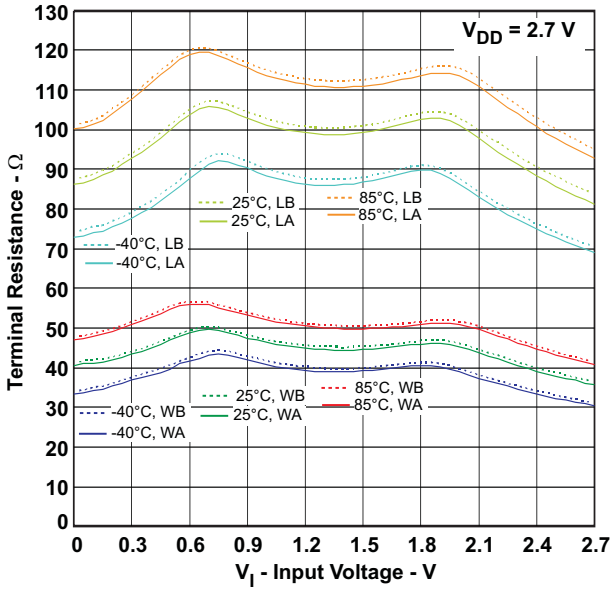
RHEOSTAT MODE TC vs DIGITAL CODE



RHEOSTAT MODE OFFSET ERROR vs TEMPERATURE

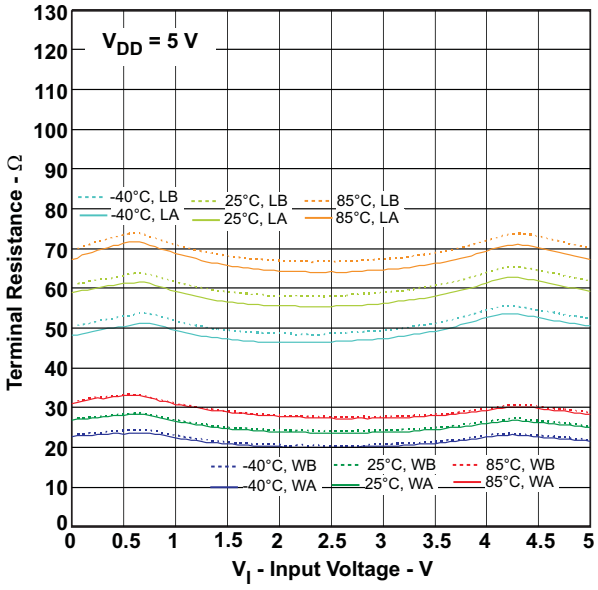


WIPER AND TERMINAL RESISTANCE (V_{DD} = 2.7V)

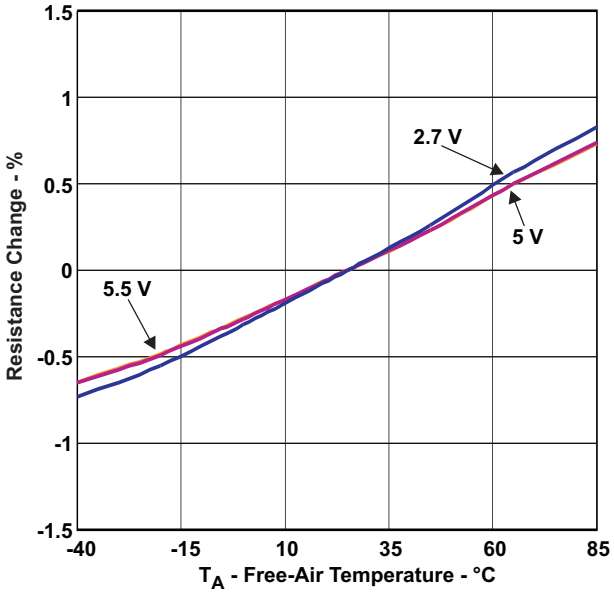


TYPICAL PERFORMANCE CURVES (continued)

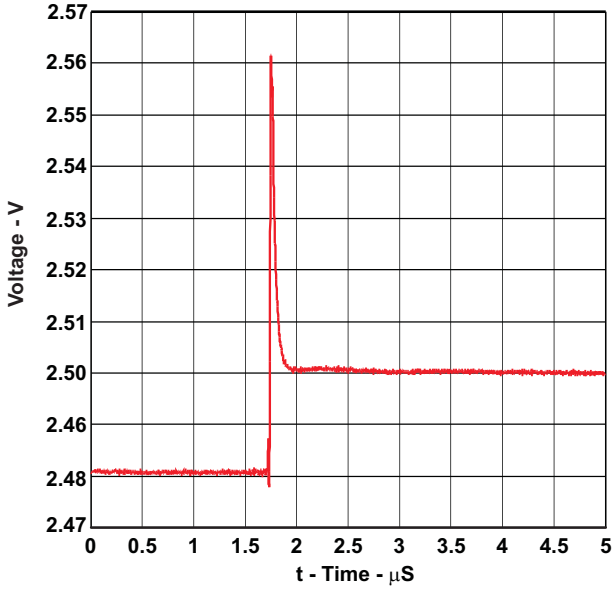
WIPER AND TERMINAL RESISTANCE (V_{DD} = 5V)



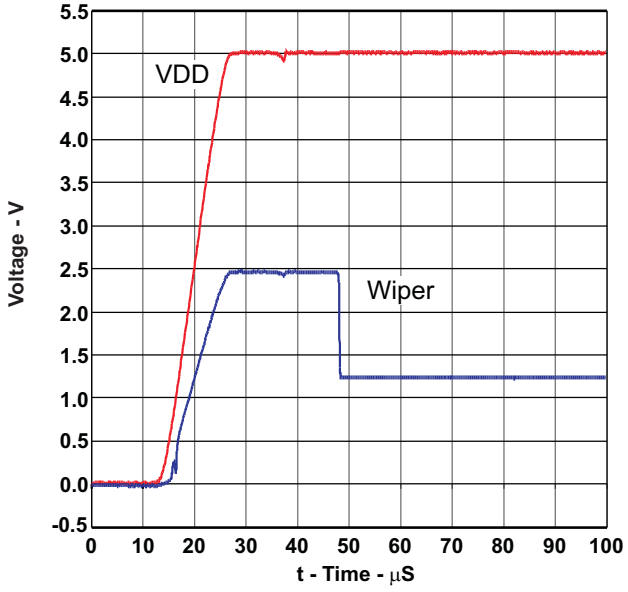
END-END RESISTANCE CHANGE vs TEMPERATURE



MIDSCALE WIPER GLITCH (CODE 7Fh to 80h)
V_{DD}= 5V, V_H= V_{DD}, V_L= GND, C_{LOAD}= 10pF



T_{POR} (POWER-UP RESPONSE TIME)
NON-VOLATILE MEMORY = 40h



SPI DIGITAL INTERFACE

The TPL0202 uses a 3-wire SPI-compatible serial data interface. This write-only interface has three inputs: chip-select ($\overline{CS}$), data clock (SCLK), and data input (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge. The WRITE commands (C1, C0 = 00 or 01) require 16 clock cycles to clock in the command, address, and data. The COPY commands (C1, C0 = 10 or 11) can use either eight clock cycles to transfer only command and address bits or 16 clock cycles, with the device disregarding 8 data bits. After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial data stream to avoid corruption of the data.

Register Map

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	–	–	C1	C0	–	–	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register B	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A and B	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register A	0	0	0	1	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register B	0	0	0	1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register A and B	0	0	0	1	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Copy Wiper Register A to NV Register A	0	0	1	0	0	0	0	1	–	–	–	–	–	–	–	–
Copy Wiper Register B to NV Register B	0	0	1	0	0	0	1	0	–	–	–	–	–	–	–	–
Copy Both Wiper Registers to NV Registers	0	0	1	0	0	0	1	1	–	–	–	–	–	–	–	–
Copy NV Register A to Wiper Register A	0	0	1	1	0	0	0	1	–	–	–	–	–	–	–	–
Copy NV Register B to Wiper Register A	0	0	1	1	0	0	1	0	–	–	–	–	–	–	–	–
Copy Both NV Registers to Wiper Registers	0	0	1	1	0	0	1	1	–	–	–	–	–	–	–	–

Digital Interface Format

The data format consists of three elements: command bits, address bits, and data bits. The command bits (C1 and C0) indicate the action to be taken such as changing or storing the wiper position. The address bits (A1 and A0) specify which potentiometer the command affects and the 8 data bits (D7 to D0) specify the wiper position.

Write-Wiper Register (Command 00)

Data written to the write-wiper registers (C1, C0 = 00) controls the wiper positions. The 8 data bits (D7 to D0) indicate the position of the wiper. If DIN = 0x00h, the wiper moves to the position closest to the L terminal. If DIN=0xFFh, the wiper moves to the position closest to the H terminal. This command writes data to the volatile RAM, leaving the NV registers unchanged. When the device powers up, the data stored in the NV registers transfers to the volatile wiper register, moving the wiper to the stored position

Write-NV Register (Command 01)

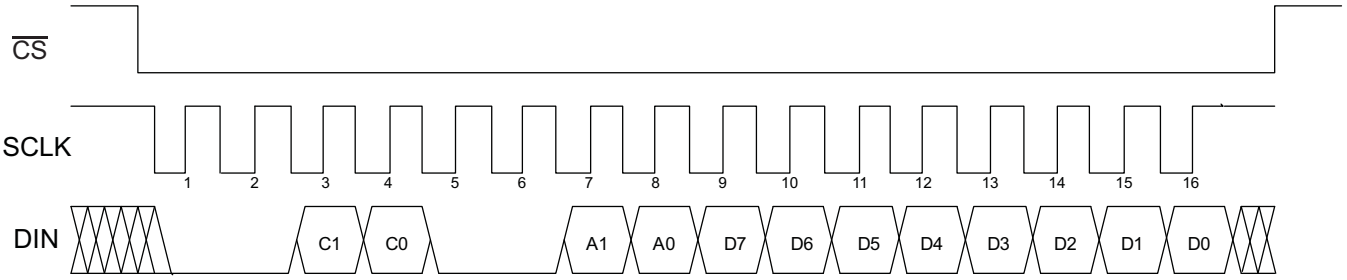
This command (C1, C0 = 01) stores the position of the wipers to the NV registers for use at power-up. Alternatively, the “copy wiper register to NV register” command can be used to store the position of the wipers to the NV registers. Writing to the NV registers does not affect the position of the wipers.

Copy Wiper Register to NV Register (Command 10)

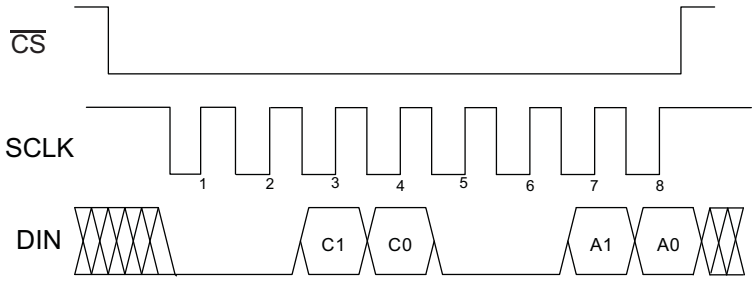
This command (C1, C0 = 10) stores the current position of the wiper to the NV register, for use at power-up. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0. Alternatively, the “write NV register” command can be used to store the current position of the wiper to the NV register.

Copy NV Register to Wiper Register (Command 11)

This command (C1, C0 = 11) restores the wiper position to the previously stored position in the NV register. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0.



A) 16-clock cycle Data Write Sequence



B) 8-clock cycle Data Move/Copy Sequence

Figure 2. Digital Interface Write Sequence

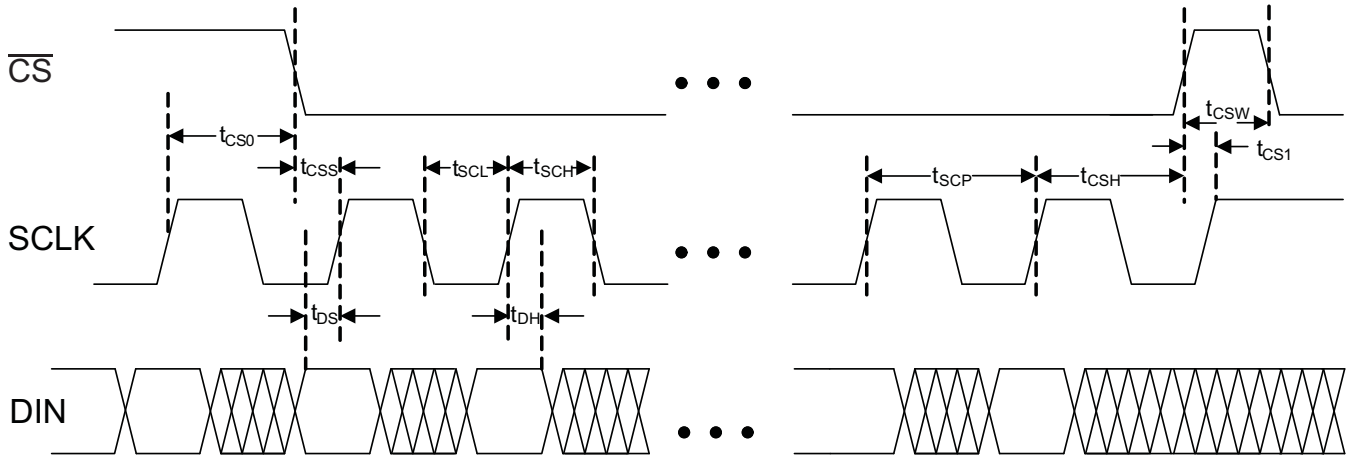


Figure 3. Digital Interface Timing Diagram

APPLICATION EXAMPLE

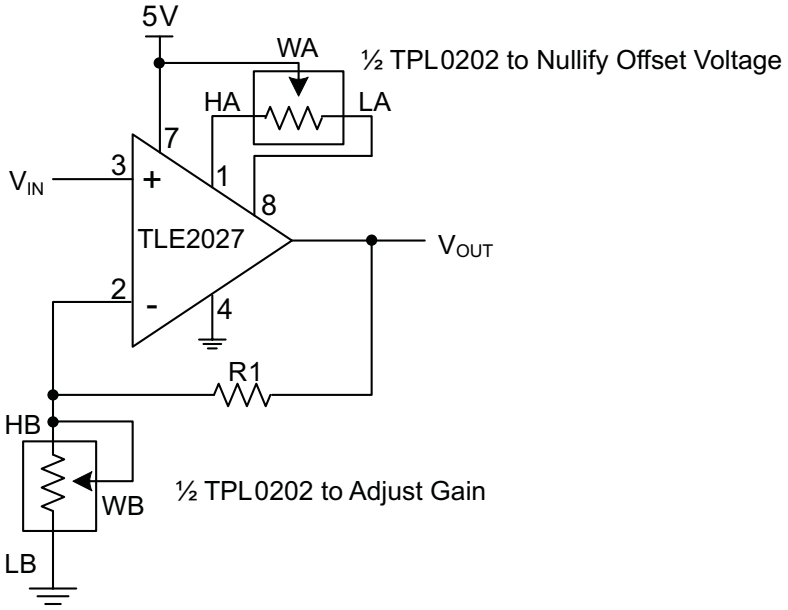
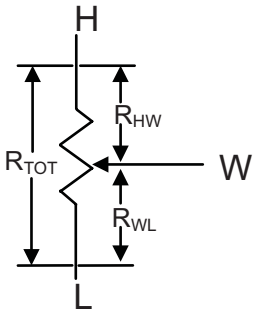


Figure 4. Offset Voltage and Gain Adjustment

IDEAL RESISTANCE VALUES



$R_{WL} = R_{TOT} \times D/256$

$R_{HW} = R_{TOT} \times (1 - (D/256))$

Where D = Decimal Value of Wiper Code

Below table shows the ideal values for DPOT with end-to End resistance of 10kΩ. The absolute values of resistance can vary significantly but the Ratio (Rhw/Rwl) is extremely accurate.

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
0	0	0.00	100.00	0.00
1	1	0.39	99.61	0.00
2	10	0.78	99.22	0.01
3	11	1.17	98.83	0.01
4	100	1.56	98.44	0.02
5	101	1.95	98.05	0.02
6	110	2.34	97.66	0.02
7	111	2.73	97.27	0.03
8	1000	3.13	96.88	0.03
9	1001	3.52	96.48	0.04
10	1010	3.91	96.09	0.04
11	1011	4.30	95.70	0.04
12	1100	4.69	95.31	0.05
13	1101	5.08	94.92	0.05
14	1110	5.47	94.53	0.06
15	1111	5.86	94.14	0.06
16	10000	6.25	93.75	0.07
17	10001	6.64	93.36	0.07
18	10010	7.03	92.97	0.08
19	10011	7.42	92.58	0.08
20	10100	7.81	92.19	0.08
21	10101	8.20	91.80	0.09
22	10110	8.59	91.41	0.09
23	10111	8.98	91.02	0.10
24	11000	9.38	90.63	0.10
25	11001	9.77	90.23	0.11
26	11010	10.16	89.84	0.11
27	11011	10.55	89.45	0.12
28	11100	10.94	89.06	0.12
29	11101	11.33	88.67	0.13
30	11110	11.72	88.28	0.13
31	11111	12.11	87.89	0.14
32	100000	12.50	87.50	0.14

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
33	100001	12.89	87.11	0.15
34	100010	13.28	86.72	0.15
35	100011	13.67	86.33	0.16
36	100100	14.06	85.94	0.16
37	100101	14.45	85.55	0.17
38	100110	14.84	85.16	0.17
39	100111	15.23	84.77	0.18
40	101000	15.63	84.38	0.19
41	101001	16.02	83.98	0.19
42	101010	16.41	83.59	0.20
43	101011	16.80	83.20	0.20
44	101100	17.19	82.81	0.21
45	101101	17.58	82.42	0.21
46	101110	17.97	82.03	0.22
47	101111	18.36	81.64	0.22
48	110000	18.75	81.25	0.23
49	110001	19.14	80.86	0.24
50	110010	19.53	80.47	0.24
51	110011	19.92	80.08	0.25
52	110100	20.31	79.69	0.25
53	110101	20.70	79.30	0.26
54	110110	21.09	78.91	0.27
55	110111	21.48	78.52	0.27
56	111000	21.88	78.13	0.28
57	111001	22.27	77.73	0.29
58	111010	22.66	77.34	0.29
59	111011	23.05	76.95	0.30
60	111100	23.44	76.56	0.31
61	111101	23.83	76.17	0.31
62	111110	24.22	75.78	0.32
63	111111	24.61	75.39	0.33
64	1000000	25.00	75.00	0.33
65	1000001	25.39	74.61	0.34
66	1000010	25.78	74.22	0.35
67	1000011	26.17	73.83	0.35
68	1000100	26.56	73.44	0.36
69	1000101	26.95	73.05	0.37
70	1000110	27.34	72.66	0.38
71	1000111	27.73	72.27	0.38
72	1001000	28.13	71.88	0.39
73	1001001	28.52	71.48	0.40
74	1001010	28.91	71.09	0.41
75	1001011	29.30	70.70	0.41
76	1001100	29.69	70.31	0.42
77	1001101	30.08	69.92	0.43
78	1001110	30.47	69.53	0.44
79	1001111	30.86	69.14	0.45
80	1010000	31.25	68.75	0.45

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
81	1010001	31.64	68.36	0.46
82	1010010	32.03	67.97	0.47
83	1010011	32.42	67.58	0.48
84	1010100	32.81	67.19	0.49
85	1010101	33.20	66.80	0.50
86	1010110	33.59	66.41	0.51
87	1010111	33.98	66.02	0.51
88	1011000	34.38	65.63	0.52
89	1011001	34.77	65.23	0.53
90	1011010	35.16	64.84	0.54
91	1011011	35.55	64.45	0.55
92	1011100	35.94	64.06	0.56
93	1011101	36.33	63.67	0.57
94	1011110	36.72	63.28	0.58
95	1011111	37.11	62.89	0.59
96	1100000	37.50	62.50	0.60
97	1100001	37.89	62.11	0.61
98	1100010	38.28	61.72	0.62
99	1100011	38.67	61.33	0.63
100	1100100	39.06	60.94	0.64
101	1100101	39.45	60.55	0.65
102	1100110	39.84	60.16	0.66
103	1100111	40.23	59.77	0.67
104	1101000	40.63	59.38	0.68
105	1101001	41.02	58.98	0.70
106	1101010	41.41	58.59	0.71
107	1101011	41.80	58.20	0.72
108	1101100	42.19	57.81	0.73
109	1101101	42.58	57.42	0.74
110	1101110	42.97	57.03	0.75
111	1101111	43.36	56.64	0.77
112	1110000	43.75	56.25	0.78
113	1110001	44.14	55.86	0.79
114	1110010	44.53	55.47	0.80
115	1110011	44.92	55.08	0.82
116	1110100	45.31	54.69	0.83
117	1110101	45.70	54.30	0.84
118	1110110	46.09	53.91	0.86
119	1110111	46.48	53.52	0.87
120	1111000	46.88	53.13	0.88
121	1111001	47.27	52.73	0.90
122	1111010	47.66	52.34	0.91
123	1111011	48.05	51.95	0.92
124	1111100	48.44	51.56	0.94
125	1111101	48.83	51.17	0.95
126	1111110	49.22	50.78	0.97
127	1111111	49.61	50.39	0.98
128	10000000	50.00	50.00	1.00

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
129	10000001	50.39	49.61	1.02
130	10000010	50.78	49.22	1.03
131	10000011	51.17	48.83	1.05
132	10000100	51.56	48.44	1.06
133	10000101	51.95	48.05	1.08
134	10000110	52.34	47.66	1.10
135	10000111	52.73	47.27	1.12
136	10001000	53.13	46.88	1.13
137	10001001	53.52	46.48	1.15
138	10001010	53.91	46.09	1.17
139	10001011	54.30	45.70	1.19
140	10001100	54.69	45.31	1.21
141	10001101	55.08	44.92	1.23
142	10001110	55.47	44.53	1.25
143	10001111	55.86	44.14	1.27
144	10010000	56.25	43.75	1.29
145	10010001	56.64	43.36	1.31
146	10010010	57.03	42.97	1.33
147	10010011	57.42	42.58	1.35
148	10010100	57.81	42.19	1.37
149	10010101	58.20	41.80	1.39
150	10010110	58.59	41.41	1.42
151	10010111	58.98	41.02	1.44
152	10011000	59.38	40.63	1.46
153	10011001	59.77	40.23	1.49
154	10011010	60.16	39.84	1.51
155	10011011	60.55	39.45	1.53
156	10011100	60.94	39.06	1.56
157	10011101	61.33	38.67	1.59
158	10011110	61.72	38.28	1.61
159	10011111	62.11	37.89	1.64
160	10100000	62.50	37.50	1.67
161	10100001	62.89	37.11	1.69
162	10100010	63.28	36.72	1.72
163	10100011	63.67	36.33	1.75
164	10100100	64.06	35.94	1.78
165	10100101	64.45	35.55	1.81
166	10100110	64.84	35.16	1.84
167	10100111	65.23	34.77	1.88
168	10101000	65.63	34.38	1.91
169	10101001	66.02	33.98	1.94
170	10101010	66.41	33.59	1.98
171	10101011	66.80	33.20	2.01
172	10101100	67.19	32.81	2.05
173	10101101	67.58	32.42	2.08
174	10101110	67.97	32.03	2.12
175	10101111	68.36	31.64	2.16
176	10110000	68.75	31.25	2.20

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
177	10110001	69.14	30.86	2.24
178	10110010	69.53	30.47	2.28
179	10110011	69.92	30.08	2.32
180	10110100	70.31	29.69	2.37
181	10110101	70.70	29.30	2.41
182	10110110	71.09	28.91	2.46
183	10110111	71.48	28.52	2.51
184	10111000	71.88	28.13	2.56
185	10111001	72.27	27.73	2.61
186	10111010	72.66	27.34	2.66
187	10111011	73.05	26.95	2.71
188	10111100	73.44	26.56	2.76
189	10111101	73.83	26.17	2.82
190	10111110	74.22	25.78	2.88
191	10111111	74.61	25.39	2.94
192	11000000	75.00	25.00	3.00
193	11000001	75.39	24.61	3.06
194	11000010	75.78	24.22	3.13
195	11000011	76.17	23.83	3.20
196	11000100	76.56	23.44	3.27
197	11000101	76.95	23.05	3.34
198	11000110	77.34	22.66	3.41
199	11000111	77.73	22.27	3.49
200	11001000	78.13	21.88	3.57
201	11001001	78.52	21.48	3.65
202	11001010	78.91	21.09	3.74
203	11001011	79.30	20.70	3.83
204	11001100	79.69	20.31	3.92
205	11001101	80.08	19.92	4.02
206	11001110	80.47	19.53	4.12
207	11001111	80.86	19.14	4.22
208	11010000	81.25	18.75	4.33
209	11010001	81.64	18.36	4.45
210	11010010	82.03	17.97	4.57
211	11010011	82.42	17.58	4.69
212	11010100	82.81	17.19	4.82
213	11010101	83.20	16.80	4.95
214	11010110	83.59	16.41	5.10
215	11010111	83.98	16.02	5.24
216	11011000	84.38	15.63	5.40
217	11011001	84.77	15.23	5.56
218	11011010	85.16	14.84	5.74
219	11011011	85.55	14.45	5.92
220	11011100	85.94	14.06	6.11
221	11011101	86.33	13.67	6.31
222	11011110	86.72	13.28	6.53
223	11011111	87.11	12.89	6.76
224	11100000	87.50	12.50	7.00

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
225	11100001	87.89	12.11	7.26
226	11100010	88.28	11.72	7.53
227	11100011	88.67	11.33	7.83
228	11100100	89.06	10.94	8.14
229	11100101	89.45	10.55	8.48
230	11100110	89.84	10.16	8.85
231	11100111	90.23	9.77	9.24
232	11101000	90.63	9.38	9.67
233	11101001	91.02	8.98	10.13
234	11101010	91.41	8.59	10.64
235	11101011	91.80	8.20	11.19
236	11101100	92.19	7.81	11.80
237	11101101	92.58	7.42	12.47
238	11101110	92.97	7.03	13.22
239	11101111	93.36	6.64	14.06
240	11110000	93.75	6.25	15.00
241	11110001	94.14	5.86	16.07
242	11110010	94.53	5.47	17.29
243	11110011	94.92	5.08	18.69
244	11110100	95.31	4.69	20.33
245	11110101	95.70	4.30	22.27
246	11110110	96.09	3.91	24.60
247	11110111	96.48	3.52	27.44
248	11111000	96.88	3.13	31.00
249	11111001	97.27	2.73	35.57
250	11111010	97.66	2.34	41.67
251	11111011	98.05	1.95	50.20
252	11111100	98.44	1.56	63.00
253	11111101	98.83	1.17	84.33
254	11111110	99.22	0.78	127.00
255	11111111	99.61	0.39	255.00

REVISION HISTORY

Changes from Revision B (August, 2011) to Revision C **Page**

- Updated QFN pin out diagram. 1
- Updated Pin Description Table. 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPL0202-10MRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPL0202-10RUCR	PREVIEW	QFN	RUC	14	3000	TBD	Call TI	Call TI	

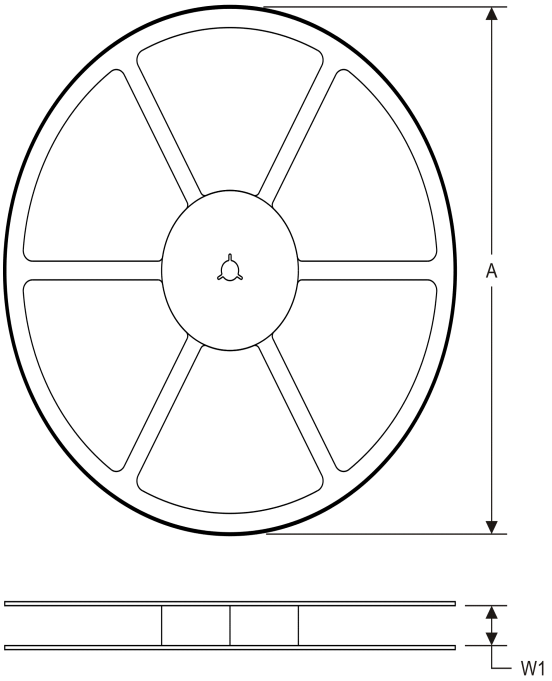
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

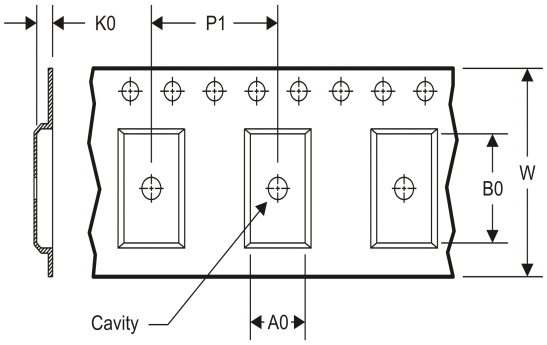
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



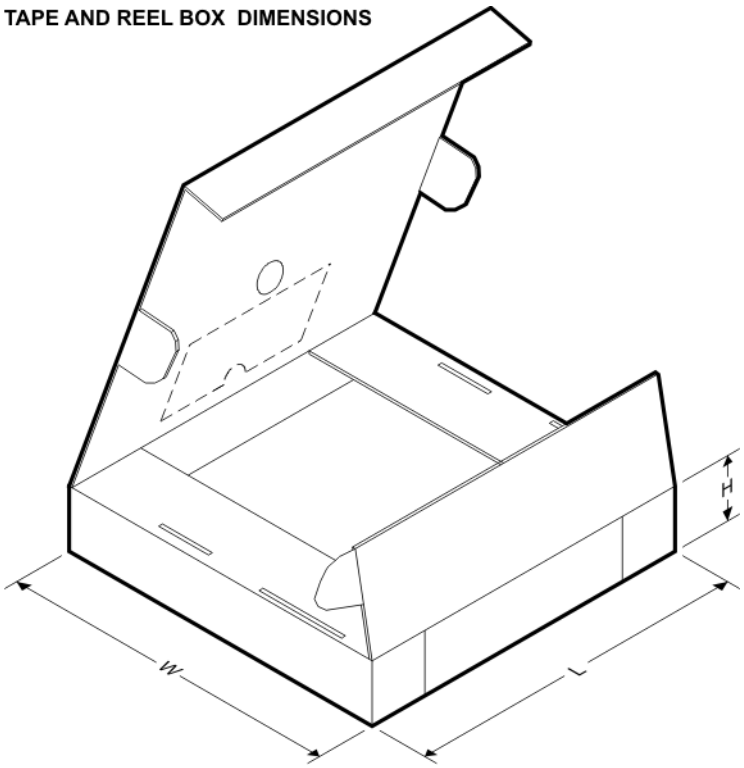
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0202-10MRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

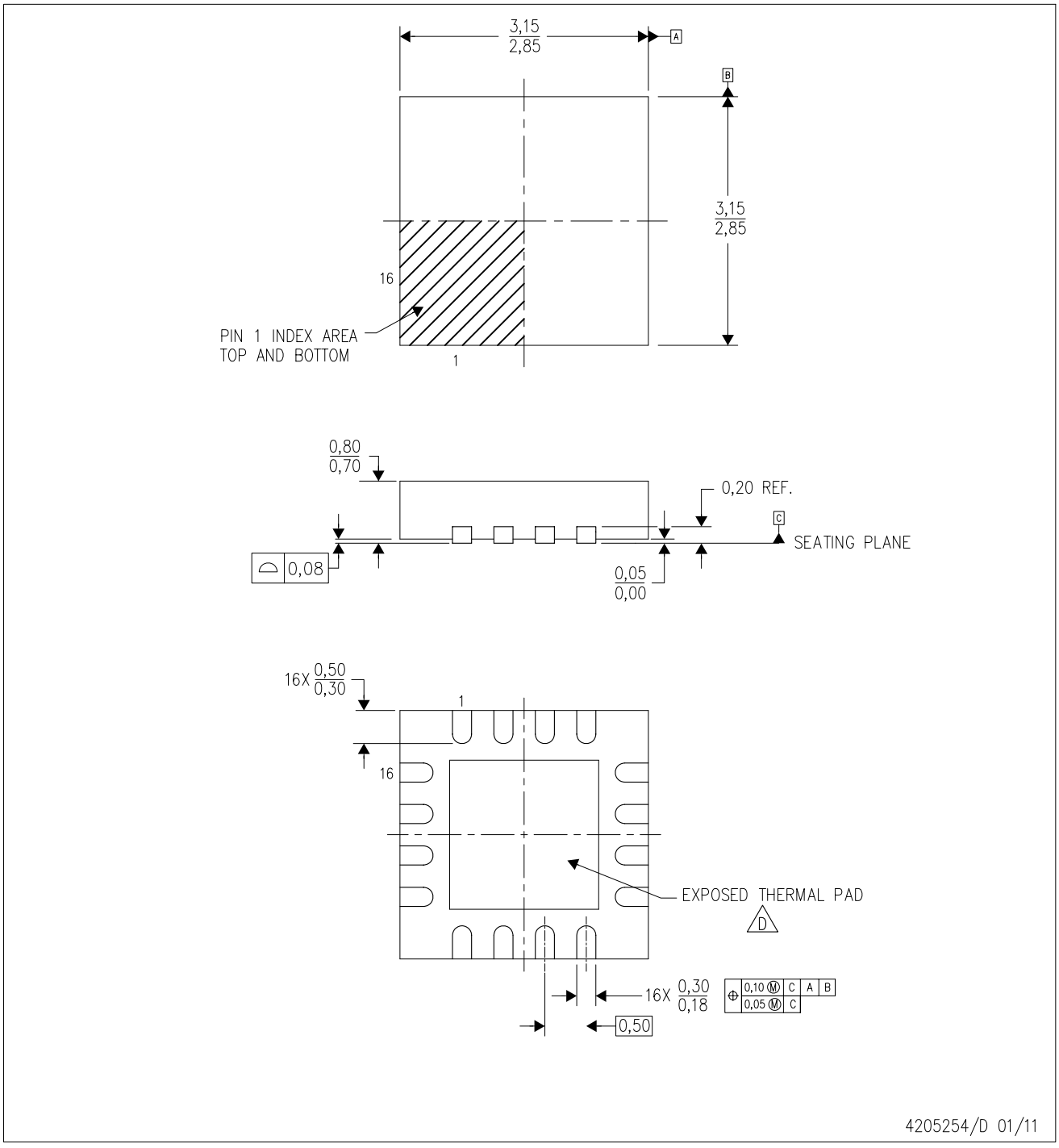
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0202-10MRTER	WQFN	RTE	16	3000	370.0	355.0	55.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

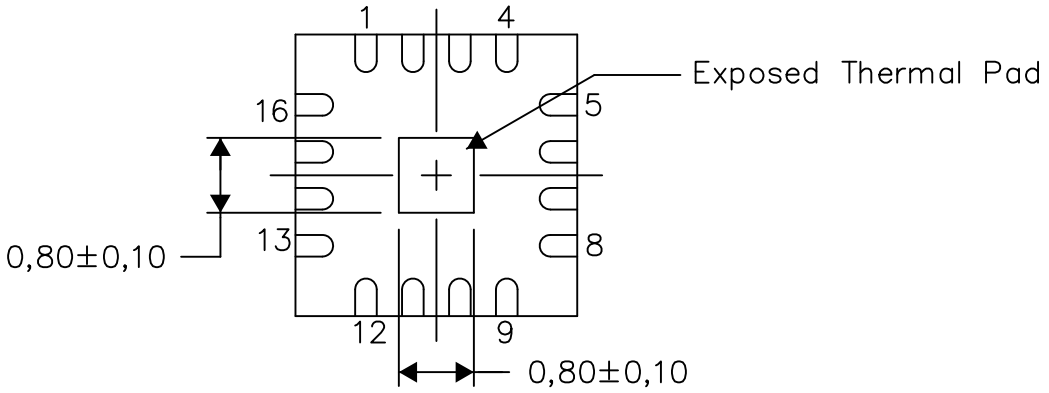
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



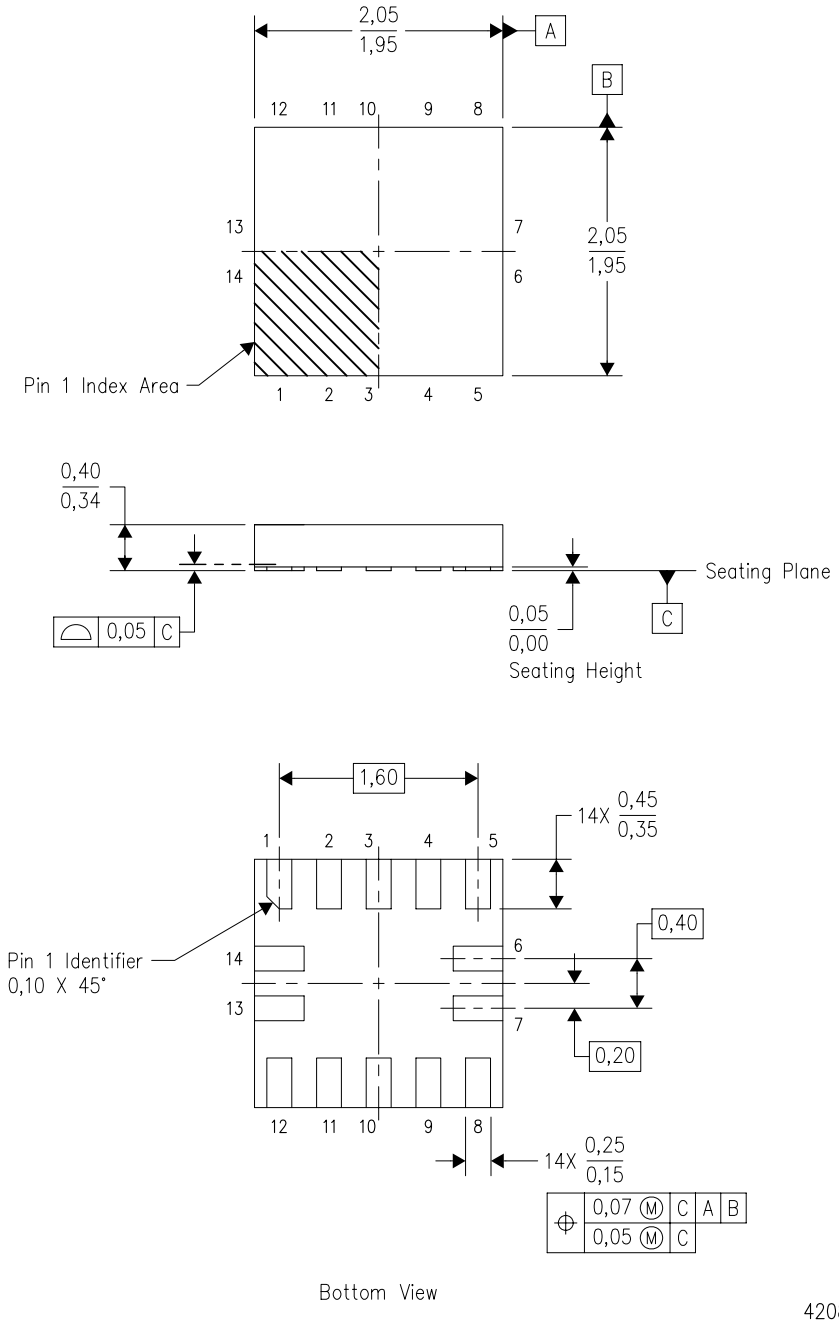
Bottom View

Exposed Thermal Pad Dimensions

4206446–6/J 05/12

NOTE: A. All linear dimensions are in millimeters

RUC (S–PX2QFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2GFE.

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