TPD7S019 7-Channel Integrated ESD Solution for VGA Port With Integrated Level Shifter and Matching Impedance

1 Features

- 7-Channel ESD Protection Includes ESD Protection, Level-Shifting, Buffering and Sync Impedance Matching
- Exceeds IEC61000-4-2 (Level 4) ESD Protection to Requirements on the External Pins
  - ±8-kV IEC 61000-4-2 Contact Discharge
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines (2.5 pF)
- 5-V Drivers for HSYNC and VSYNC Lines
- Integrated Impedance Matching Resistors on Sync Lines
- Bidirectional Level Shifting N-Channel FETs Provided for DDC_CLK and DDC_DATA Channels
- Flow-Through Single-In-Line Pin Mapping Ensures no Additional Board Layout Burden While Placing the ESD Protection Chip Near the Connector

2 Applications

- End Equipment:
  - Desktop and Notebook PCs
  - Set Top Boxes
  - TVs
- Interfaces:
  - VGA
  - DVI-I

3 Description

TPD7S019 device is an integrated electrostatic discharge (ESD) circuit protection solution for VGA and DVI-I connectors. It integrates transient voltage suppression (TVS) protection diodes for VIDEO, DDC and SYNC signals and meets the IEC61000-4-2 standard for ±8-kV contact ESD protection. The TVS diodes only add low capacitances to help signals run at high-speed. It also provides level shifting for the DDC signals saving external level-shifters. Two noninverting drivers on HSYNC and VSYNC convert TTL input levels to CMOS output levels and each buffer has a series termination resistor connected to the SYNC_OUT pin, eliminating the external termination resistors. Three supply lines control the power rails of the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs in mixed supply-voltage environments. TPD7S019 comes with two package options. The 16-pin RSV is compact and space-saving. The 16-pin DBQ package and pinout are optimized for easy board layout.

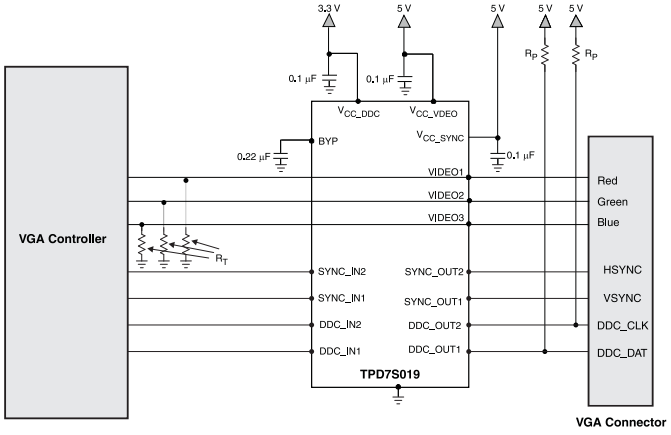
This ESD protection product is a good solution to protect the VGA and DVI-I ports for desktop and laptop PCs, set top boxes, TVs and monitors.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD7S019	SSOP (16)	4.90 mm × 3.90 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2012) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (August 2010) to Revision A — **Page**

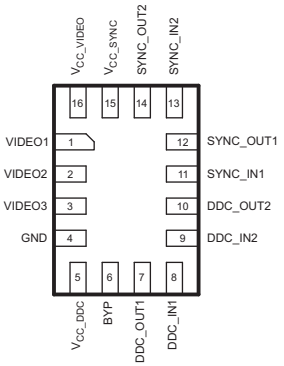
- Removed PREVIEW status from the RSV package ... 3

Changes from Revision A (March 2012) to Revision B — **Page**

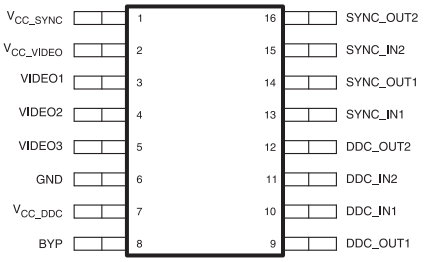
- Removed non released part descriptions from the datasheet. ... 1

5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



DBQ Package
16-Pin SSOP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBQ NO.	RSV NO.		
BYP	8	6	Power	Bypass pin. Using a 0.2-µF bypass capacitor will increase the ESD robustness of the system.
DDC_IN1 DDC_IN2	10 11	8 9	I	DDC signal input. Connects to the VGA controller side of one of the sync lines.
DDC_OUT1 DDC_OUT2	9 12	7 10	O	DDC signal output. Connects to the video connector side of one of the sync lines.
GND	6	4	–	Ground
SYNC_IN1 SYNC_IN2	13 15	11 13	I	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
SYNC_OUT1 SYNC_OUT2	14 16	12 14	O	Sync signal buffer output. Connects to the video connector side of one of the sync lines
VCC_DDC	7	5	Power	Isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates
VCC_SYNC	1	15	Power	Isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits
VCC_VIDEO	2	16	Power	Supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits
VIDEO1 VIDEO2 VIDEO3	3 4 5	1 2 3	ESD	High-speed ESD clamp input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC_VIDEO} V_{CC_DDC} V_{CC_SYNC}	Supply voltage			–0.5	6	V
$V_{IO(VIDEO)}$	IO voltage	VIDEOx pins		–0.5	V_{CC_VIDEO}	V
$V_{I(SYNC)}$	Input voltage	SYNC pins		–0.5	V_{CC_SYNC}	V
$V_{I(DDC)}$	Input voltage	DDC_INx pins		–0.5	6	V
$V_{O(DDC)}$	Output voltage	DDC_INx pins		–0.5	6	V
I_{IK}	Input clamp current	SYNC_INx, DDC_INx, VIDEOx	$V_I < 0$	–50		mA
I_{OK}	Output clamp current	SYNC_OUTx, DDC_OUTx	$V_O < 0$	–50		mA
I_O	Continuous output current	SYNC_OUTx		–24	24	mA
I_O	Continuous output current	DDC_INx to DDC_OUTx		–5	5	mA
	Continuous current through supply pins	VCC_VIDEO, VCC_SYNC, VCC_DDC		–50	50	mA
T_{stg}	Storage temperature			–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
TPD7S019 in RSV Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1, 2, 3, 4, 7, 10, 12, and 14	±2000	V
			Pins 1, 2, 3, 7, 10, 12, and 14	±15000	
			Pin 4	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 contact discharge	Pins 1, 2, 3, 7, 10, 12, and 14	±8000	
TPD7S019 in DBQ Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 3, 4, 5, 6, 9, 12, 14, and 16	±2000	V
			Pins 3, 4, 5, 9, 12, 14, and 16	±15000	
			Pin 6	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 contact discharge	Pins 3, 4, 5, 9, 12, 14, and 16	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	Supply voltage		0	5.5	V
$V_{IO(VIDEO)}$	IO voltage	VIDEOx pins	0	VCC_VIDEO	V
$V_{I(SYNC)}$	Input voltage	SYNC pins	0	VCC_SYNC	V
$V_{I(DDC)}$	Input voltage	DDC_INx pins	0	5.5	V
$V_{O(DDC)}$	Output voltage	DDC_INx Pins	0	5.5	V
T_A	Operating temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPD7S019		UNIT
		DBQ (SSOP)	RSV (UQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	124.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.0	52.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	53.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.9	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	53.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

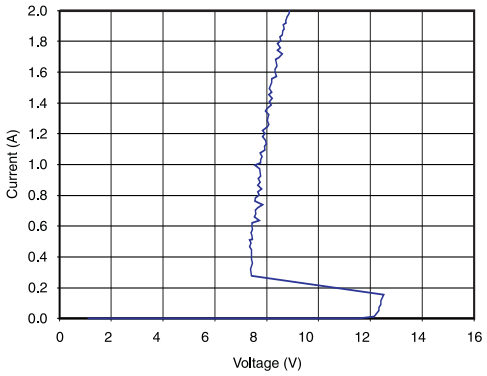
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC_VIDEO}	V_{CC_VIDEO} supply current	V_{CC_VIDEO} = 5 V, VIDEO inputs at V_{CC_VIDEO} or GND			1	10	µA
I_{CC_DDC}	V_{CC_DDC} supply current	V_{CC_DDC} = 5 V			1	10	µA
I_{CC_SYNC}	V_{CC_SYNC} supply current	V_{CC_SYNC} = 5 V,	SYNC inputs at GND or V_{CC_SYNC}, SYNC outputs unloaded		1	50	µA
			SYNC inputs at 3 V; SYNC outputs unloaded			2.0	mA
I_{IO_VIDEO}	VIDEO input/output pins	V_{IO_VIDEO} = 3 V			0.01	1.0	µA
I_{OFF}	DDC pin power down leakage current	V_{CC_DDC} ≤ 0.4 V, V_{DDC_OUT} = 5 V			0.01	1.0	µA
V_D	Diode forward voltage for lower clamp of VIDEO, DDC, SYNC output pins	I_D = 8 mA, lower clamp diode		–0.6	–0.8	–0.95	V
R_{DYN_VIDEO}	Dynamic resistance (VIDEO pins)	I = 1 A			1		Ω
V_{IH}	High-level SYNC logic input voltage	V_{CC_SYNC} = 5 V		2			V
V_{IL}	Low-level SYNC logic input voltage	V_{CC_SYNC} = 5 V				0.6	V
V_{OH}	High-level SYNC logic output voltage	I_{OH} = 0 mA, V_{CC_SYNC} = 5 V		4.85			V
V_{OH}	High-level SYNC logic output voltage	I_{OH} = -24 mA, V_{CC_SYNC} = 5 V		2			V
V_{OL}	Low-level SYNC logic output voltage	I_{OL} = 0 mA, V_{CC_SYNC} = 5 V				0.15	V
V_{OL}	Low-level SYNC logic output voltage	I_{OL} = 24 mA, V_{CC_SYNC} = 5 V				0.8	V
R_T	SYNC driver output resistance	V_{CC_SYNC} = 5 V, SYNC inputs at GND or 3 V			15		Ω
C_{IO_VIDEO}	IO capacitance of VIDEO pins	V_{IO} = 2.5 V, test frequency is 1 MHz			2.5	4	pF
t_{PLH}	SYNC driver L => H propagation delay	C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns				12	ns
t_{PHL}	SYNC driver H => L propagation delay	C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns				12	ns
t_R, t_F	SYNC driver output rise & fall times	C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns			4		ns
V_{BR}	VIDEO ESD diode break-down voltage	I_{IO} = 1 mA		9			V

6.6 Typical Characteristics



T_{rf} = 10 ns

Figure 1. TPD7S019-xx TLP VID1 to GND, Barth

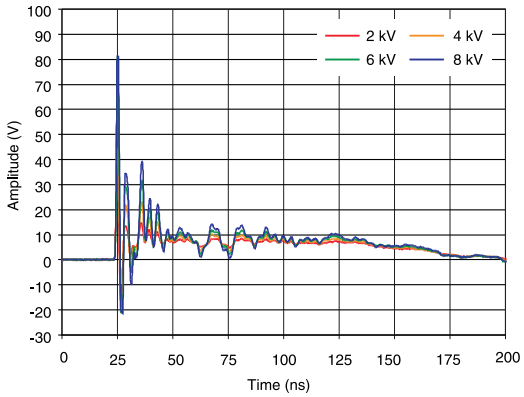


Figure 2. TPD7S019-xx IEC Clamping Waveforms Positive Contact

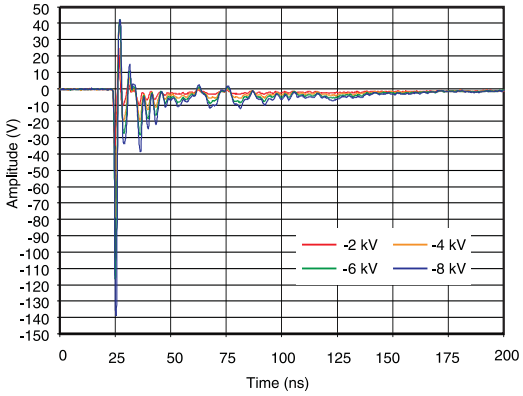
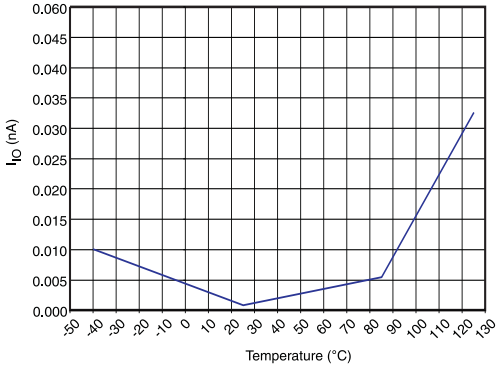
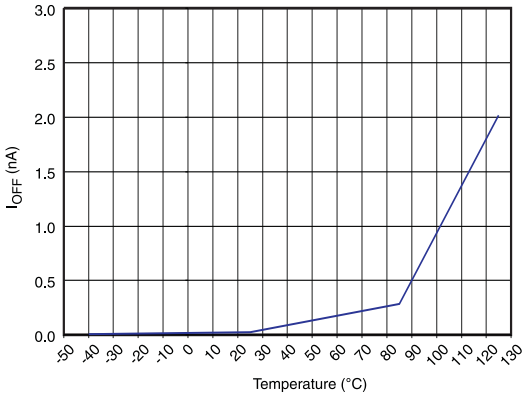


Figure 3. TPD7S019-xx IEC Clamping Waveforms Negative Contact



V_{CC_VIDEO} = 5 V

Figure 4. Leakage Current Trough VIDEO Pins



V_{CC_DDC} = 0 V

Figure 5. I_{OFF} (DDC_OUTx)

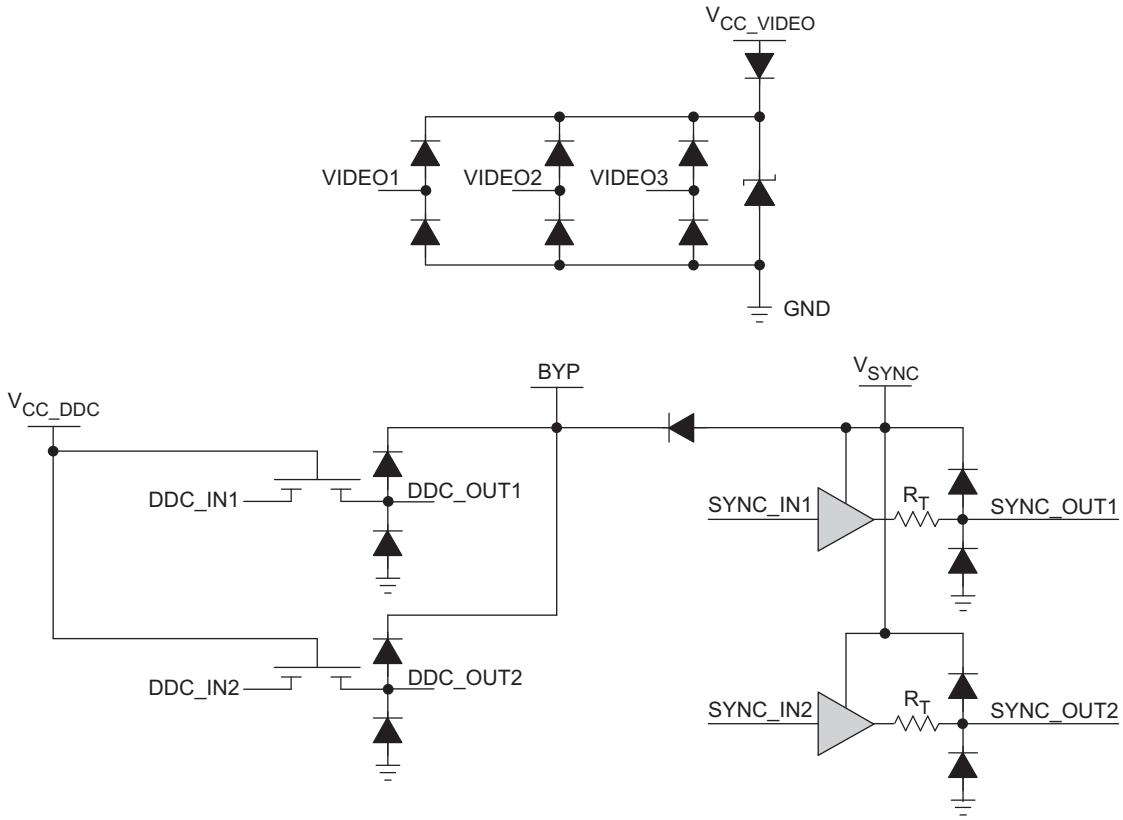
7 Detailed Description

7.1 Overview

The TPD7S019 is an integrated protection solution for VGA or DVI-I ports by providing high-speed ESD protection, level-shifting and signal buffering. The TVS protection diodes for VIDEO signals, DDC signals and SYNC signals provide robust ESD clamping that meets the IEC61000-4-2 standard for ±8-kV contact stress. The signals run at high speed is minimally affected by the low capacitance added to each signal line. The integrated level-shifters for the DDC signals help save external ICs. Two buffers on the HSYNC and VSYNC signals convert TTL input level to CMOS output level, and it saves external components by integrating series termination resistors connected to the SYNC_OUT pin. TPD7S019 takes in three signal rails to make the signals compatible with different voltages on VIDEO, DDC and SYNC. The two package options provide the latitude to choose between either small board area or easier layout and better signal integrity.

The end applications of this device include desktop and laptop PCs, set top boxes, TVs, and monitors.

7.2 Functional Block Diagram



7.3 Feature Description

TPD7S019 is an integrated protection solution for VGA and DVI-I ports. It has the low capacitance ESD TVS diodes for the VIDEO signals to ensure high speed data transmission. Level-shifting on the DDC lines translate signals on the cable to the level can be processed by downstream ICs. Buffers on the SYNC lines condition the signal levels and quality. The integrated termination resistors help reduce external devices. TPD7S019 exceeds IEC61000-4-2 (Level 4) ESD standard of ±8-kV contact discharge, making the system robust against system level ESD. The two package options provide the freedom to choose between a compact package or a flow through package.

7.4 Device Functional Modes

DDC level translators and SYNC signal buffers are active and the ESD cells on all the lines are untriggered when the recommended operating conditions are met. The bidirectional voltage-level translators provide noninverting level shifting from the system side to the connector side. Each connector side pin has an ESD clamp that triggers when voltages are above V_{BR} or below the lower diode's Vf. During ESD events, voltages as high as ±8-kV (contact ESD) can be directed to ground through the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10's of nano-seconds), these pins revert to a non-conductive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TPD7S019 provides IEC61000-4-2 Level 4 Contact ESD rating to the VGA or DVI-I port. The integrated voltage-level shifting, buffering and termination reduce the board space needed to implement the control lines functions.

8.2 Typical Application

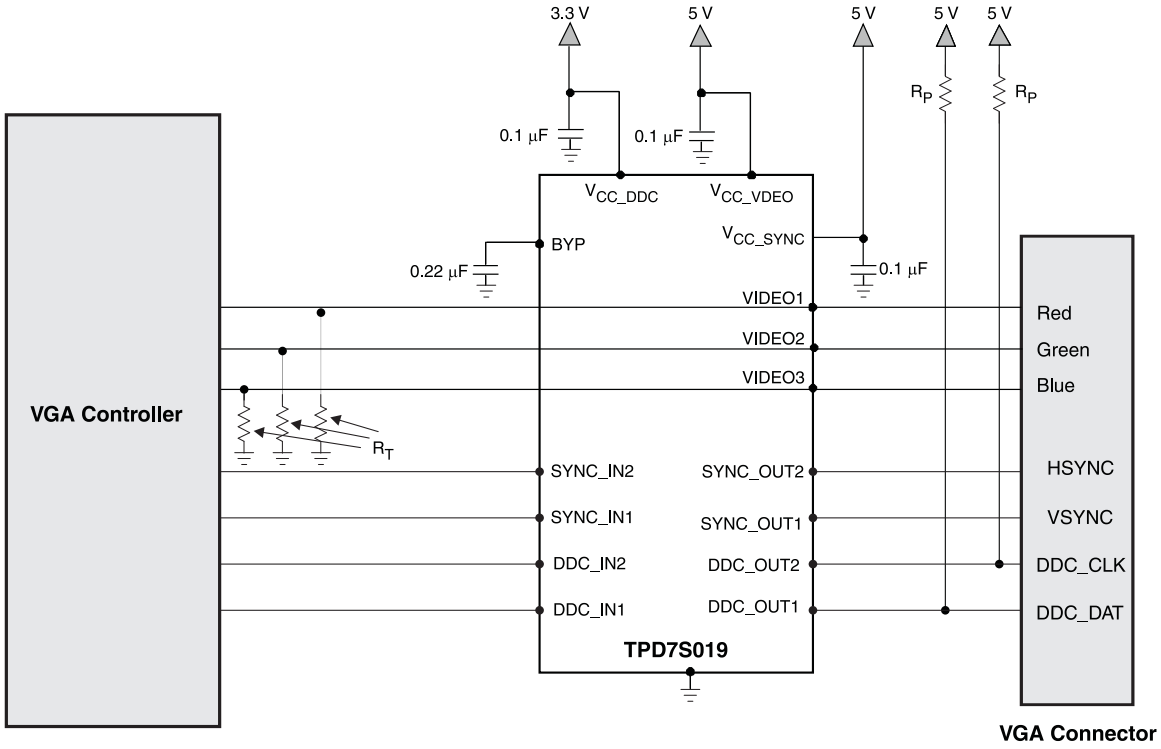


Figure 6. Typical Application Schematics With TPD7S019

8.2.1 Design Requirements

In this application, TPD7S019 will be used to protect the VGA port. Table 1 lists the system parameters.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Pull-up resistors on DDC lines	1.5 kΩ to 2 kΩ
Termination resistors on VIDEO lines	50 Ω to 75 Ω
VIDEO signals data rate	24 MHz to 388 MHz
Required IEC 61000-4-2 ESD Protection	±8 kV Contact

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM})
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode

For this application, the DDC signals will switch between 0 V and 5 V (with resistor pulling it up to 5-V power supply). The VIDEO and SYNC signal levels are between 0 V and V_{CC_VIDEO} / V_{CC_SYNC}. All signals are not exceeding the recommended values and the ESD cells on these pins will stay untriggered.

Depending on the resolution and the refresh rate of the display, the VIDEO (RGB) signals' bandwidth can be from 24 MHz to 388MHz. The line capacitances from the ESD cells are 2.5 pF typical which is only takes up a small portion of the total capacitance budget for the maximum frequency in this range.

±8-kV Contact ESD provided by TPD7S019 meets the ESD design goal of ±8 kV contact.

Put 1.5-kΩ to 2-kΩ pullup resistor on the DDC lines to be compliant with the I^2C standard. Termination resistors on VIDEO lines are 50 Ω to 75 Ω to match the impedance on board trace.

8.2.3 Application Curves

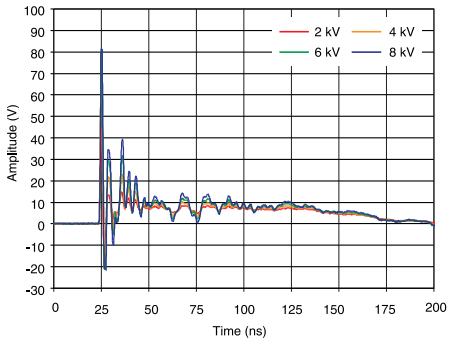


Figure 7. IEC 61000-4-2 Clamping Voltage, Positive Contact

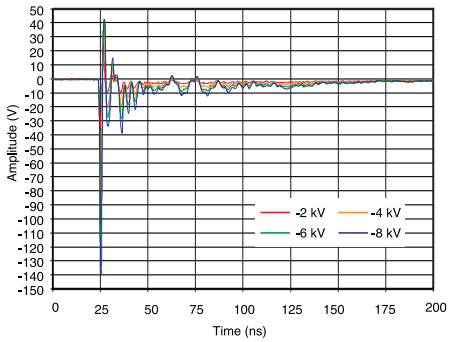


Figure 8. IEC 61000-4-2 Clamping Voltage, Negative Contact

9 Power Supply Recommendations

TPD7S019 has three power supply pins: VCC_DDC, VCC_SYNC and VCC_VIDEO. Depending on the system, the recommended voltage level of these three power supplies can be as high as 5.5 V.

10 Layout

10.1 Layout Guidelines

The optimum placement of this device is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Avoid using VIAs between the connecter and an I/O protection pin on TPD7S019.

Avoid 90º turns in traces since electric fields tend to build up on corners, increasing EMI coupling.

Minimize impedance on the path to GND for maximum ESD dissipation.

The capacitors on V_{CC_VIDEO}, V_{CC_DDC} and $V_{CC\_=SYNC}$ should be placed close to their respective pins.

The VIDEO lines internal protection circuits are the same and thus these pins are interchangeable for routing.

10.2 Layout Example

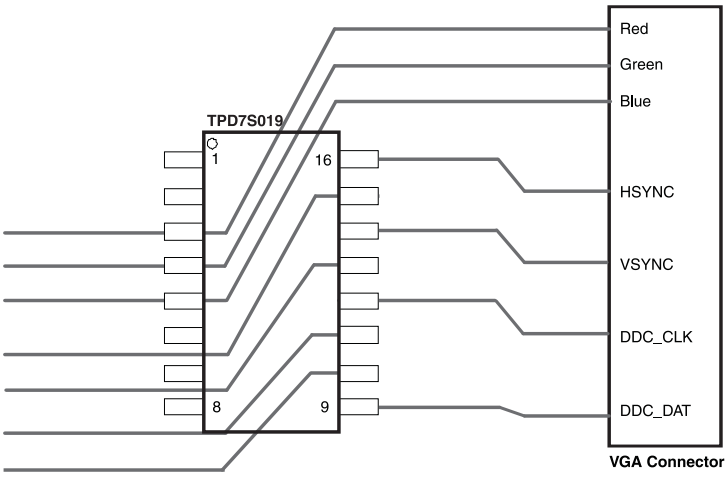


Figure 9. Simplified Layout With TPD7S019 (Only IO Lines are Shown)

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD7S019-15DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PQ19-15	Samples
TPD7S019-15RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZUS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

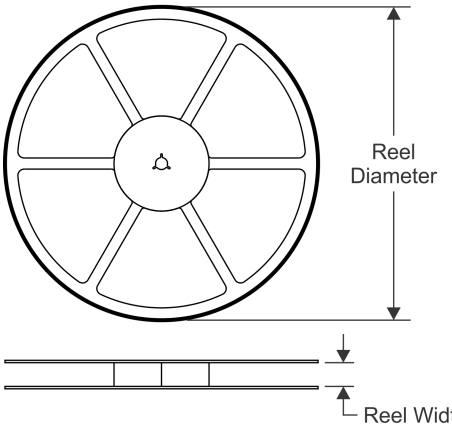
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

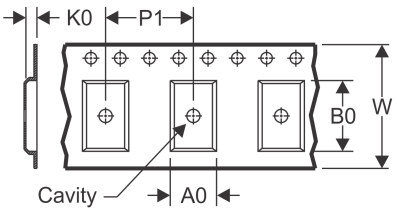
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

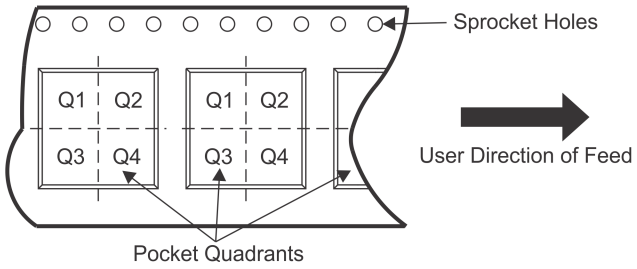


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

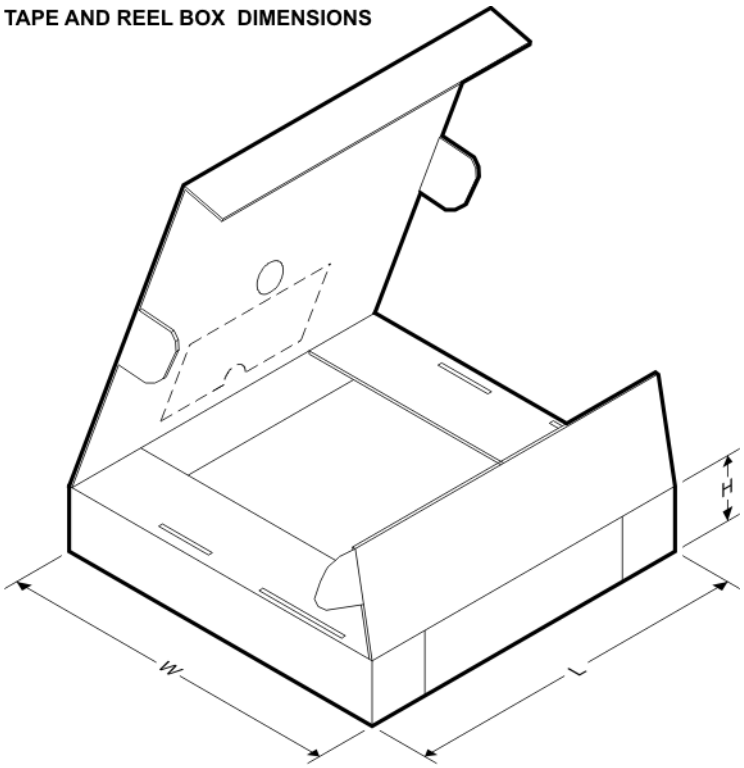
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD7S019-15DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPD7S019-15RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

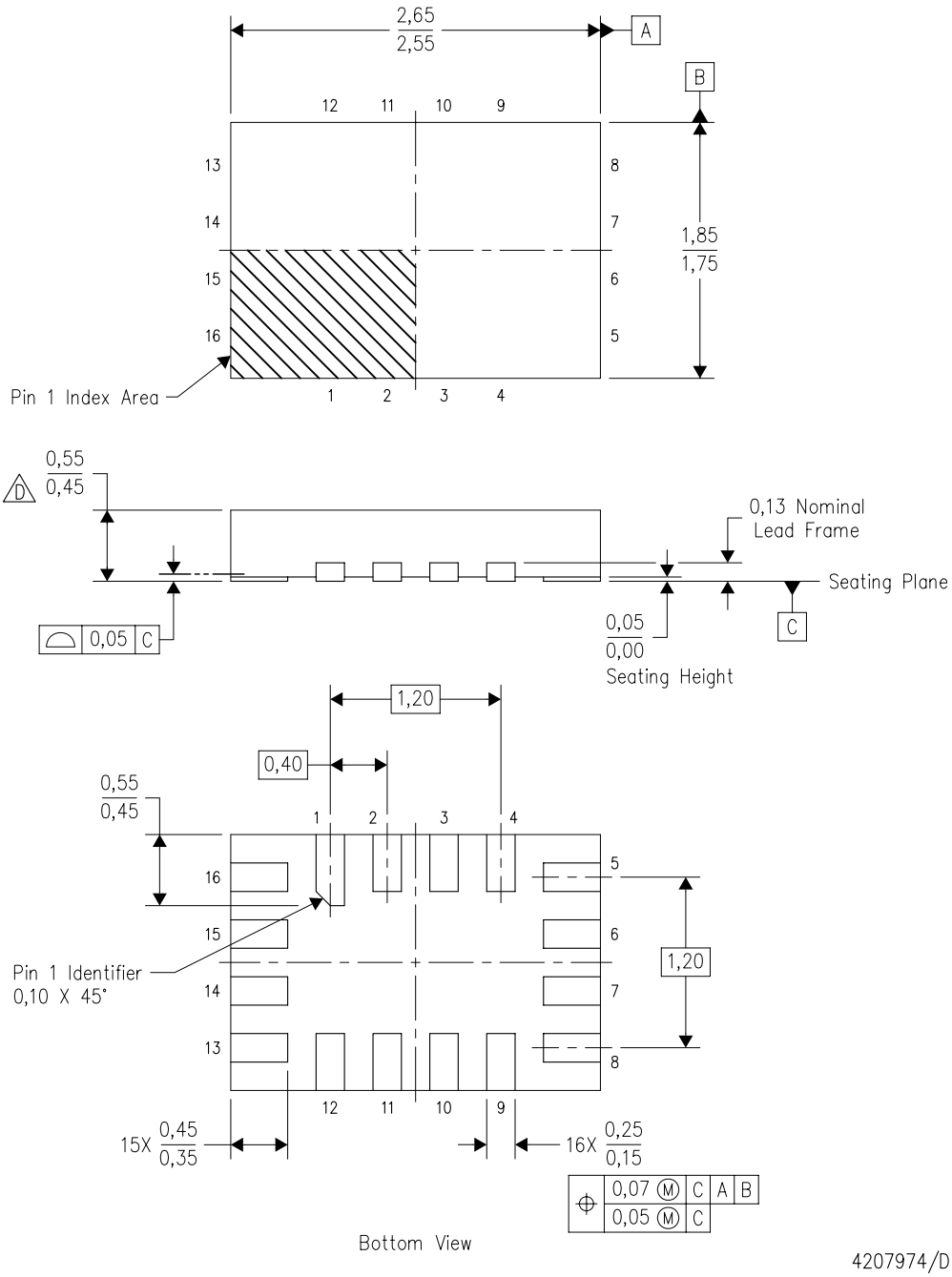
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

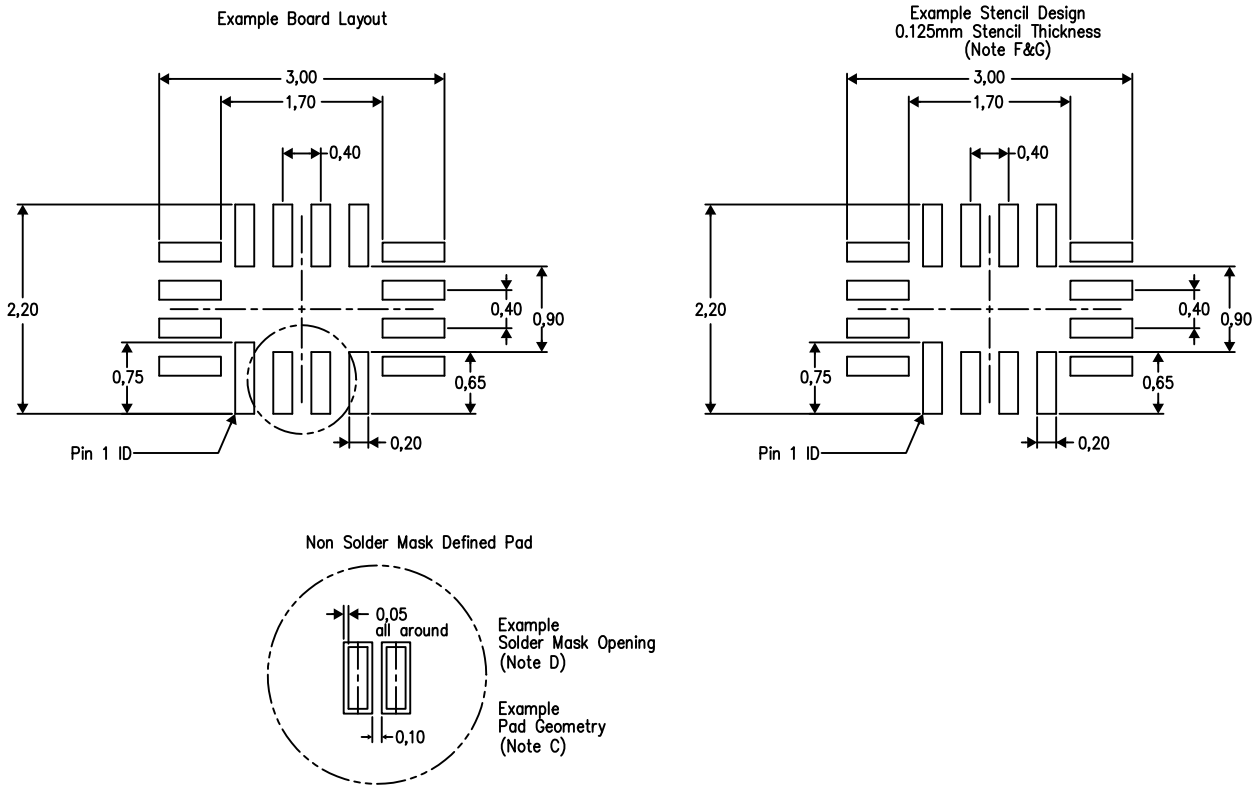
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD7S019-15DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TPD7S019-15RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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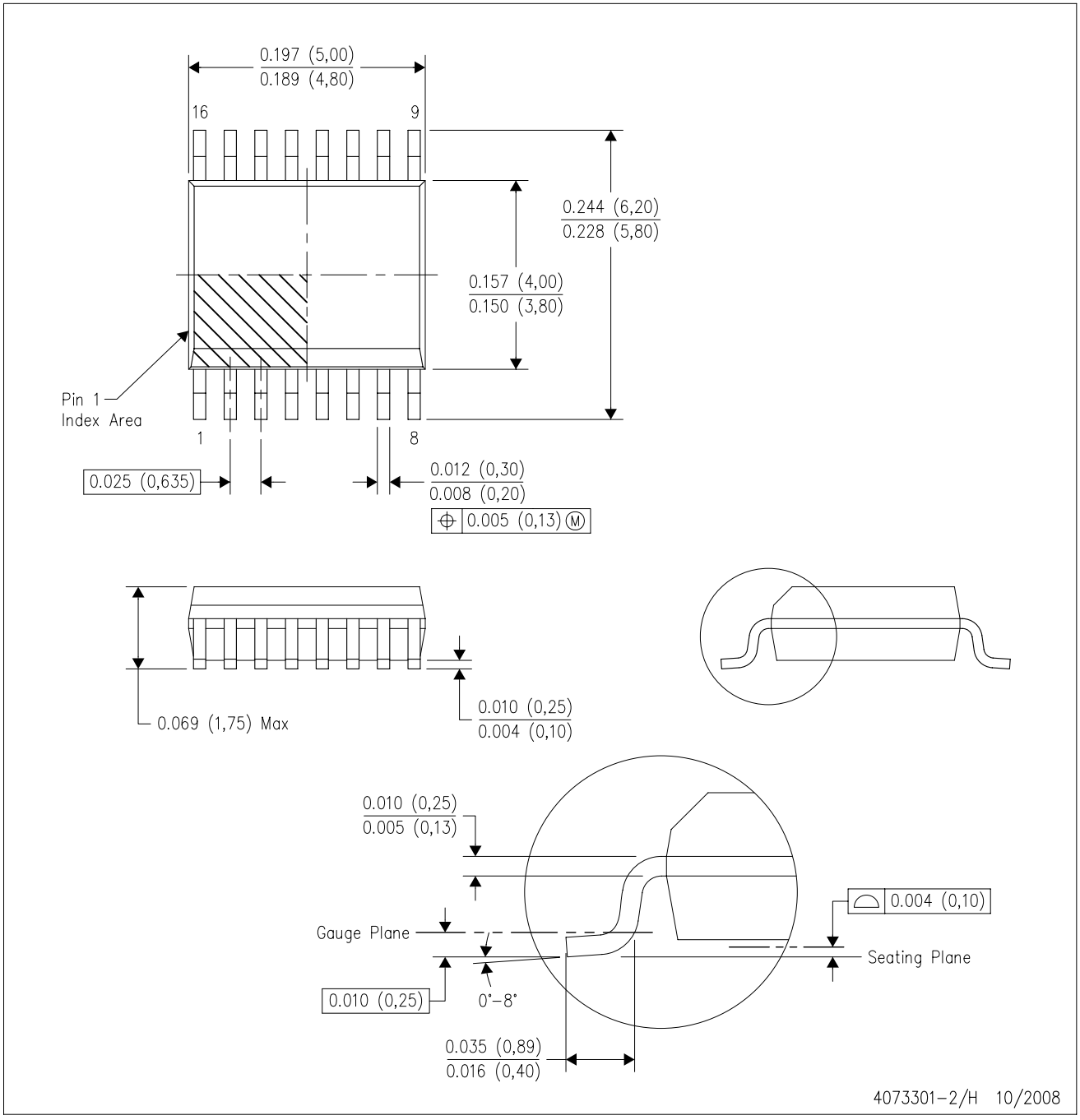
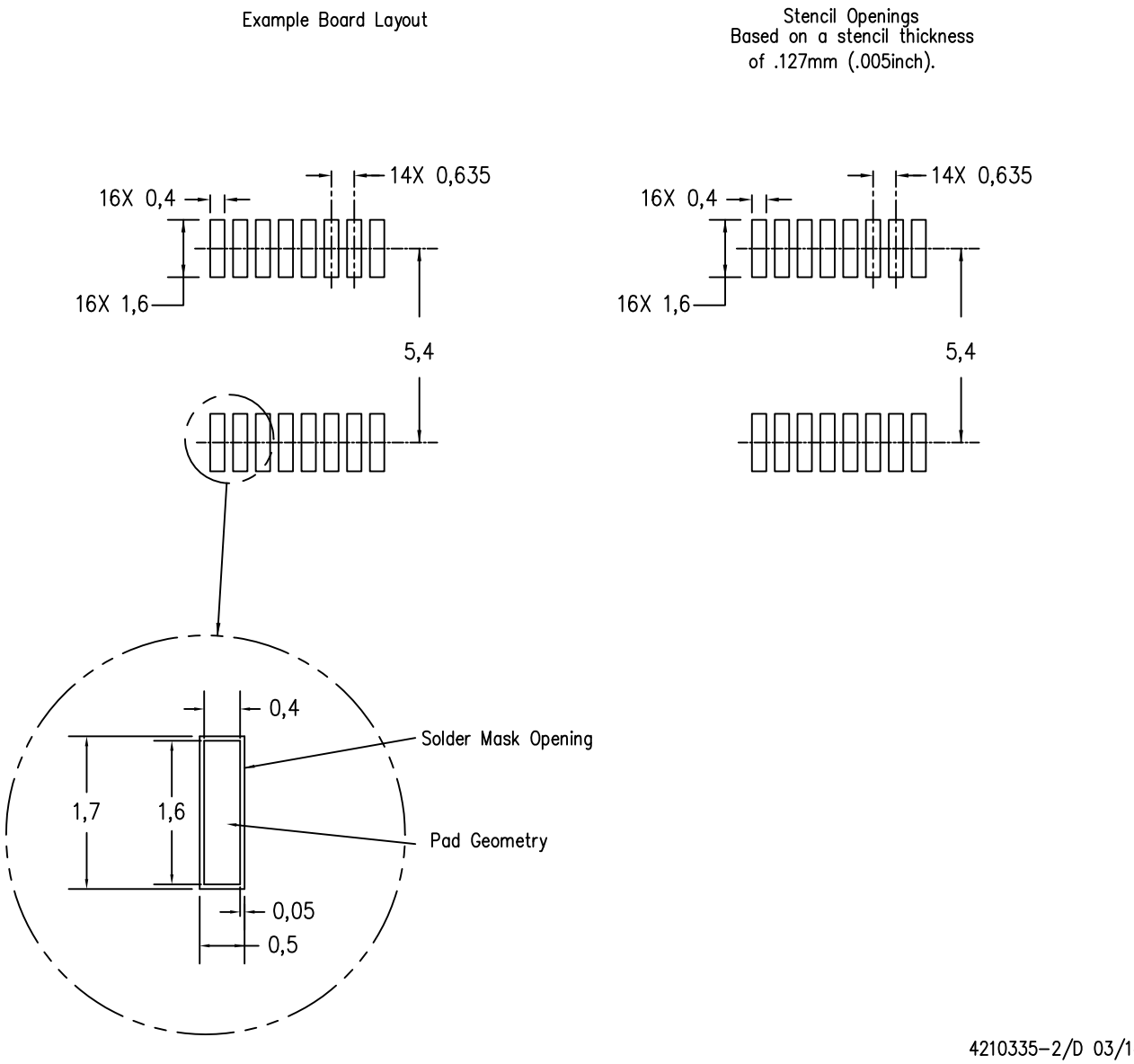
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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