

EMI FILTER WITH INTEGRATED V_{CC} CLAMP FOR SIM CARD INTERFACE

Check for Samples: [TPD3F303](#)

FEATURES

- Bidirectional EMI/RFI Filtering and Line Termination with Integrated ESD Protection
- Robust ESD Protection Exceeds IEC 61000-4-2 (Level 4)
 - ± 15 -kV Human-Body Model (HBM)
 - ± 15 -kV IEC 61000-4-2 (Contact Discharge)
 - ± 15 -kV IEC 61000-4-2 (Air-Gap Discharge)
- Breakdown voltage 6-V
- Low Noise C-R-C Filter Topology
- Integrated V_{CC} Clamp Eliminates the Need for External ESD Protection
- Space Saving DPV (0.5-mm Pitch), DQD Packages (0.4-mm Pitch)

APPLICATIONS

- Mobile handsets
- PDAs
- Video Consoles
- Portable Computers

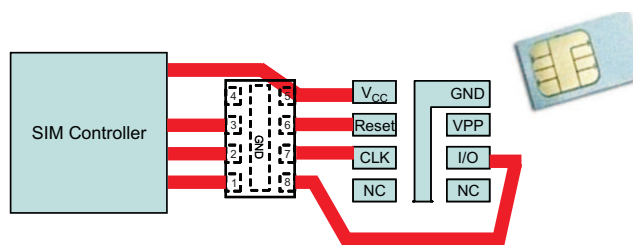
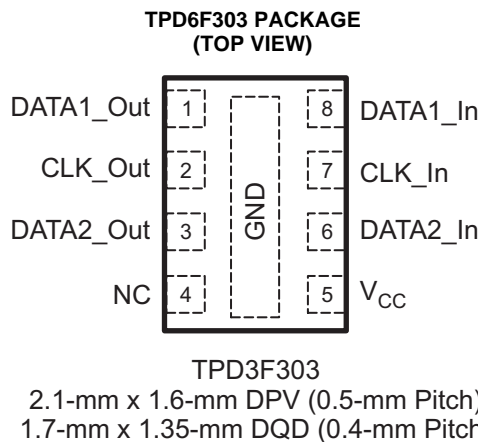


Figure 1. Board Layout with TPD3F303 at the SIM Card Interface

DESCRIPTION/ORDERING INFORMATION

The TPD3F303 is a 3-ch integrated EMI filter for SIM interface. This device integrates a V_{CC} clamp to provide system level ESD protection at the V_{CC} line. Termination resistor value of $47\ \Omega$ is included on the CLK line, while a $100\ \Omega$ termination is employed at the DATA and RST line.

The low-pass filter arrays reduce EMI emissions and provide system level ESD protection. Because of its small package and easy-to-use pin assignments, the TPD3F303 filter is suitable for a wide array of applications such as mobile handsets, PDAs, video consoles, notebook computers, etc.

The TPD3F303 is designed to suppress EMI/RFI noise in systems subjected to electromagnetic interferences. These filter series include an ESD protection circuitry which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4). The TPD3F303 is specified for -40°C to 85°C operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾ ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	8 – DPV	Tape and reel	TPD3F303DPVR	6SS
	8 – DQD	Tape and reel	TPD3F303DQDR	6SS

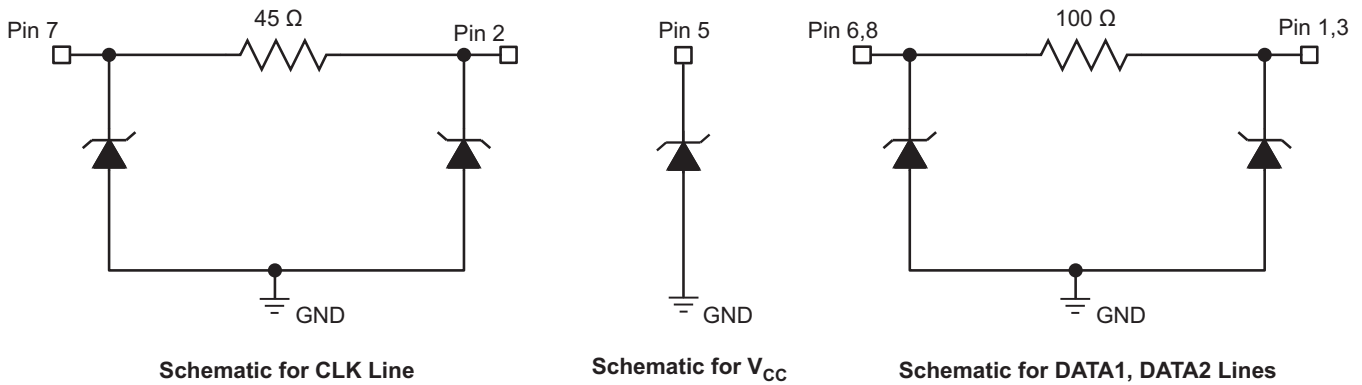
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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CIRCUIT DIAGRAMS



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	DPV/DQD PIN NO.		
DATA _x _IN, DATA _x _OUT	1, 3, 6, 8	Input, Output Pins	Data and Rest signals Input, Output pins. The DATA1 and DATA2 are symmetric circuits. They can be used interchangeably for either DATA or RESET pins based off board layout scheme.
CLK_OUT, CLK_IN V	2, 7	Input, Output Pins	Clock Input and Output signals.
V _{CC}	5	Power Clamp	ESD Clamp circuit for the V _{CC} pin.
NC	4	No Connect	Not connected to any internal circuit. Leave this pin floating.
GND	Central ground Pad	Ground	Ground connection for the EMI filter. It is very important to connect the device GND to the printed circuit board ground plane through Vias directly under the package.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	IO voltage tolerance		5.5	V
T _A	Operating free-air temperature range	-40	85	°C
T _{stg}	Storage temperature range	-55	155	°C
	IEC 61000-4-2 Contact Discharge		±15	KV
	IEC 61000-4-2 Air-gap Discharge		±15	KV
	Human Body Model ESD		±15	KV

(1) Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{clamp}	Clamp voltage	I _{IO} = ±2 A	IO pin to ground			±10	V
I _l	Leakage current	R _{PU} = Open	IO pin to ground			0.1	µA
R _{CLK}	CLK series resistors			40	47	55	Ω
R _{DAT_RST}	Data/RST series resistors			85	100	115	Ω
C _{Total}	IO Capacitance	V _{IO} = 0 V	IO Pins to GND	16	20	24	pF
V _{BR}	Break-down Voltage	I _{IO} = 1 mA		6			V
F _{-3dB}	-3 dB BW for DATA/RESET line	Z _{SOURCE} = 50 Ω Z _{LOAD} = 50 Ω			294		MHz

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F _{-3dB}	-3 dB BW for CLK line	Z _{SOURCE} = 50 Ω Z _{LOAD} = 50 Ω		308		MHz

TYPICAL OPERATING CHARACTERISTICS

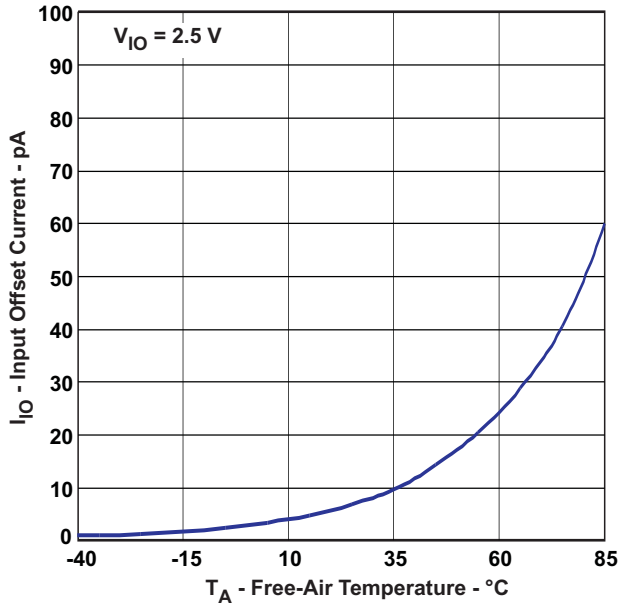


Figure 2. I_{IO} vs Temperature, $V_{IO} = 2.5V$

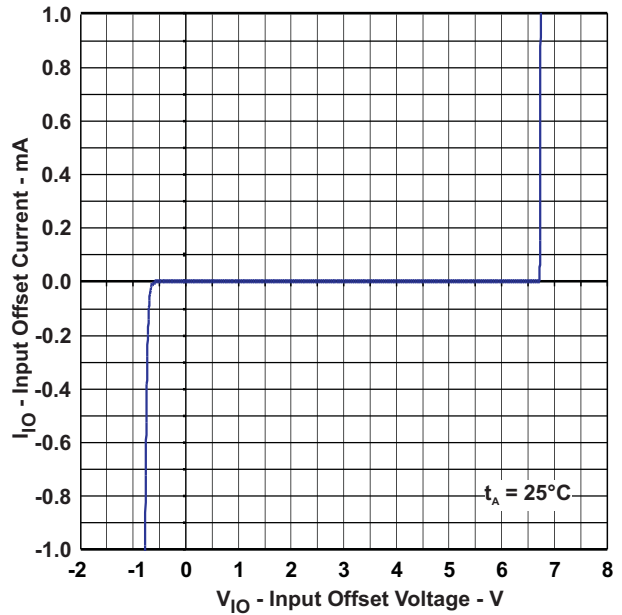


Figure 3. I_{IO} vs V_{IO}

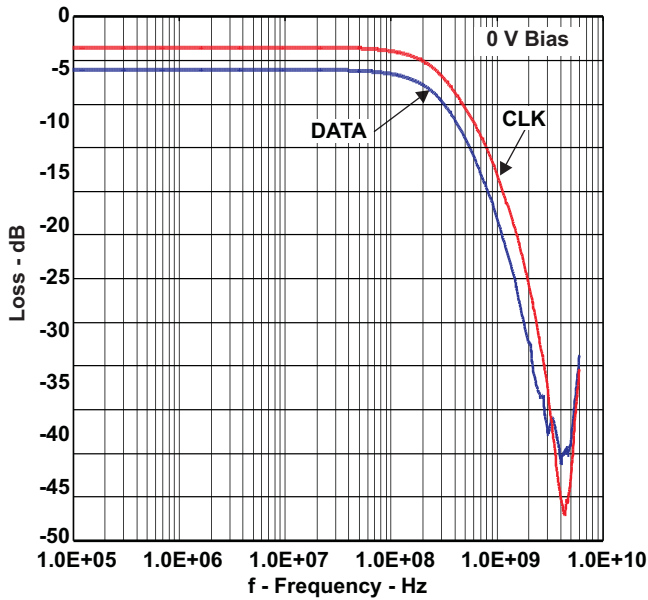


Figure 4. Frequency Response Data (0 V Bias)

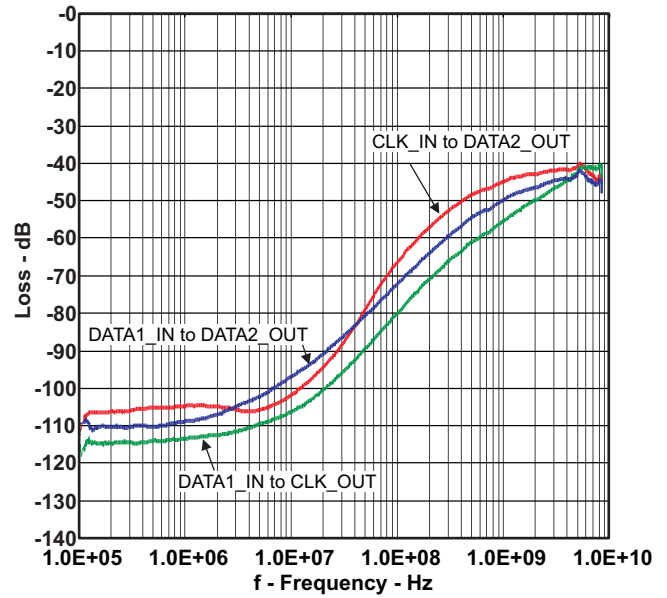


Figure 5. Channel-to-Channel Crosstalk

TYPICAL OPERATING CHARACTERISTICS (continued)

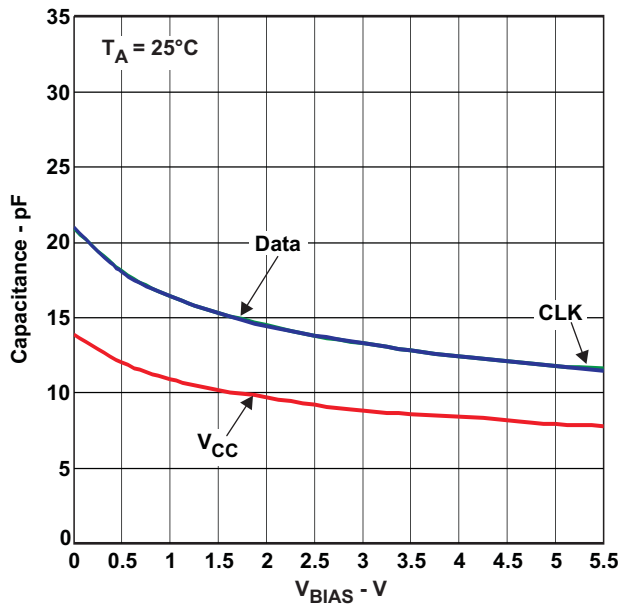


Figure 6. Capacitance vs V_{BIAS} , $t_A = 25^\circ\text{C}$

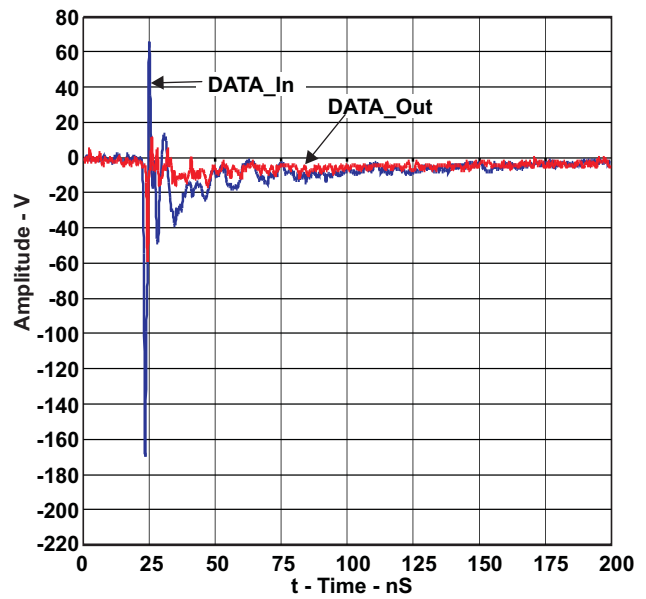


Figure 7. IEC Clamping Waveforms
-15 kV Contact, DATA1_In Stressed

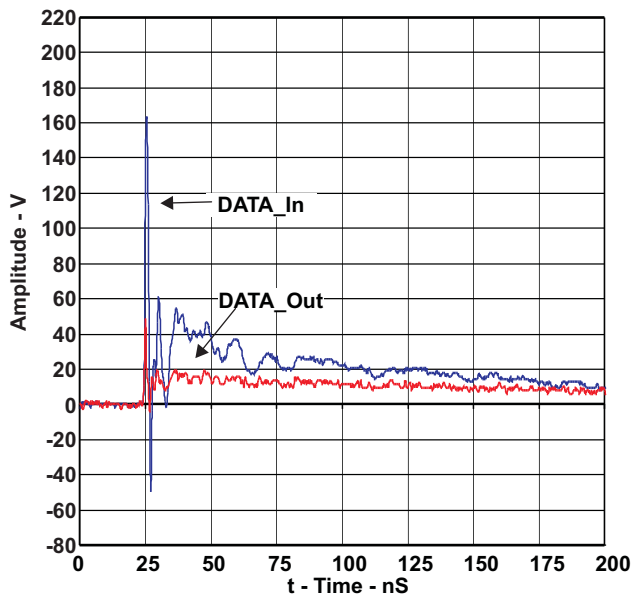


Figure 8. IEC Clamping Waveforms
+15 kV Contact, DATA1_In Stressed

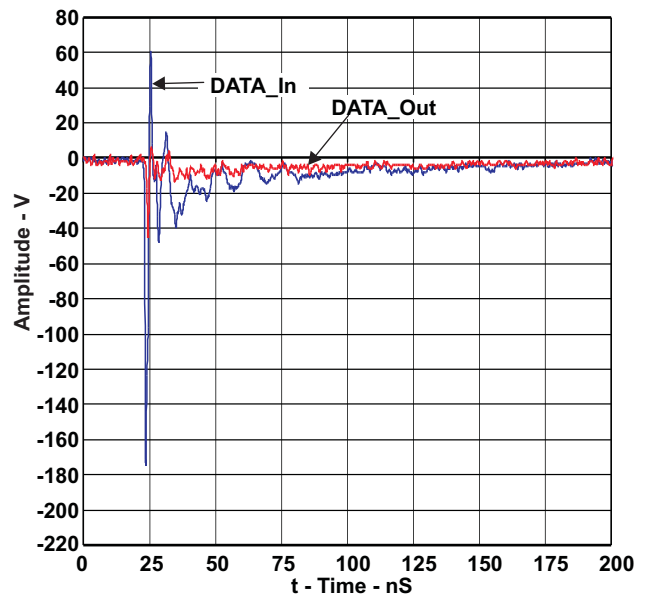
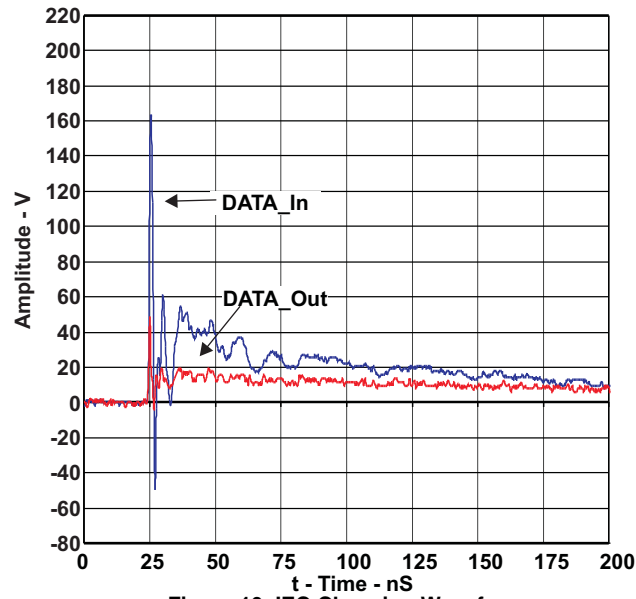


Figure 9. IEC Clamping Waveforms
-15 kV Contact, CLK_In Stressed

TYPICAL OPERATING CHARACTERISTICS (continued)



**Figure 10. IEC Clamping Waveforms
+15 kV Contact, CLK_In Stressed**

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPD3F303DPVR	ACTIVE	USON	DPV	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPD3F303DQDR	ACTIVE	WSON	DQD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3F303DPVR	USON	DPV	8	3000	180.0	8.4	1.84	2.32	0.78	4.0	8.0	Q1
TPD3F303DQDR	WSON	DQD	8	3000	180.0	8.4	1.65	2.0	0.95	4.0	8.0	Q1

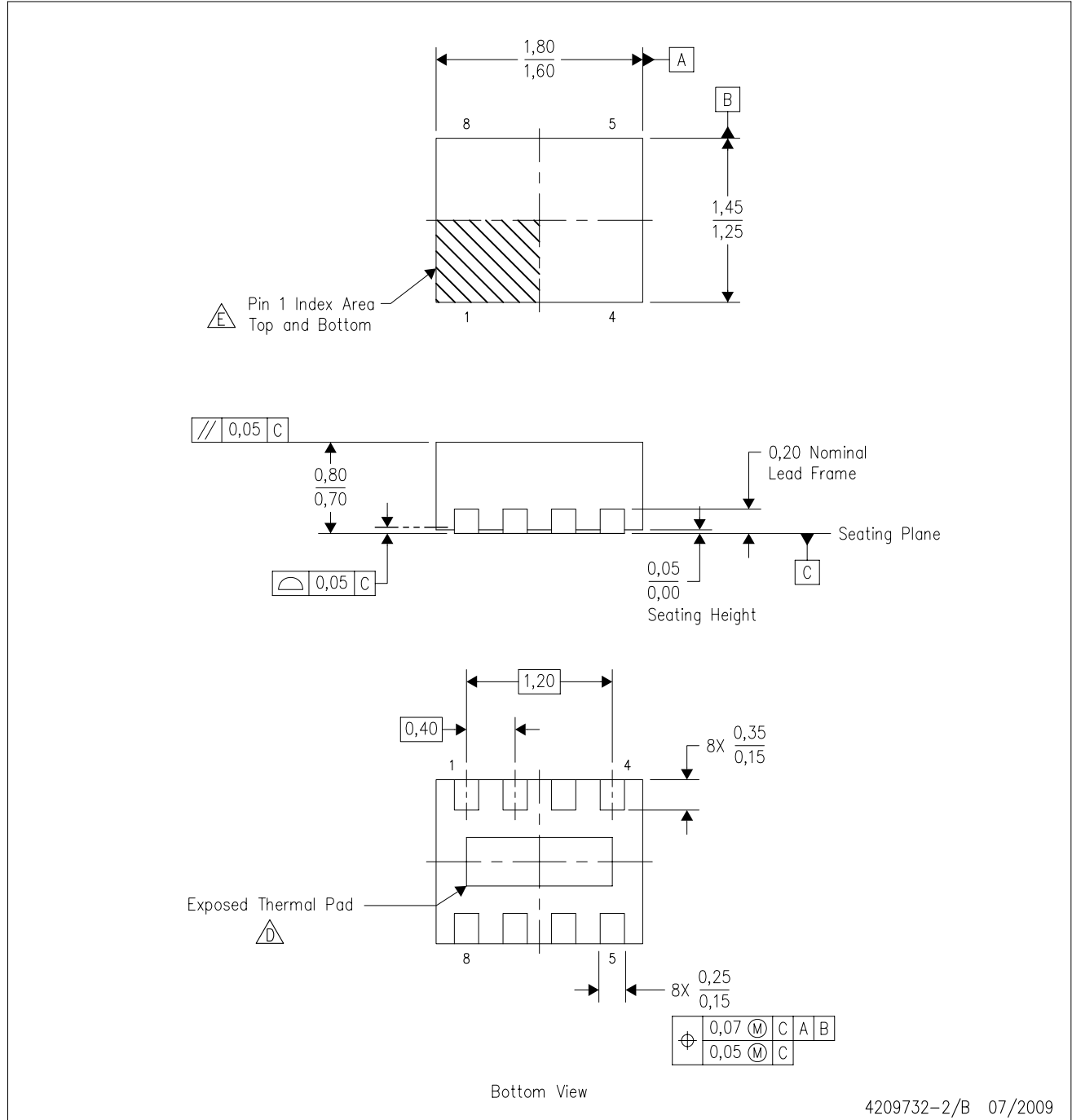
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3F303DPVR	USON	DPV	8	3000	202.0	201.0	28.0
TPD3F303DQDR	WSON	DQD	8	3000	202.0	201.0	28.0

DQD (R-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



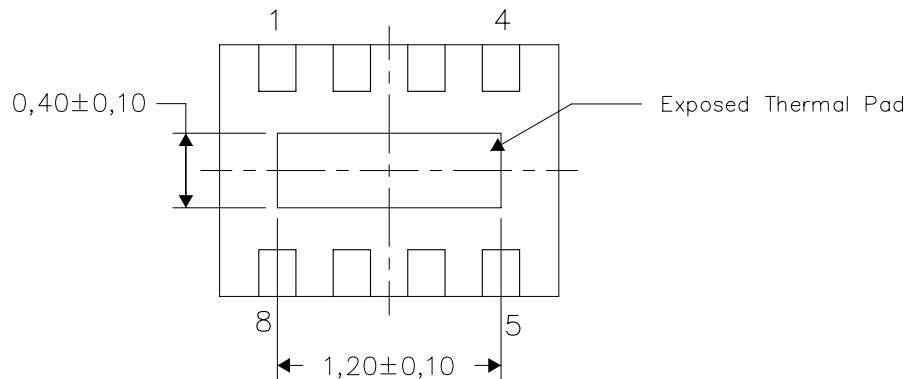
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

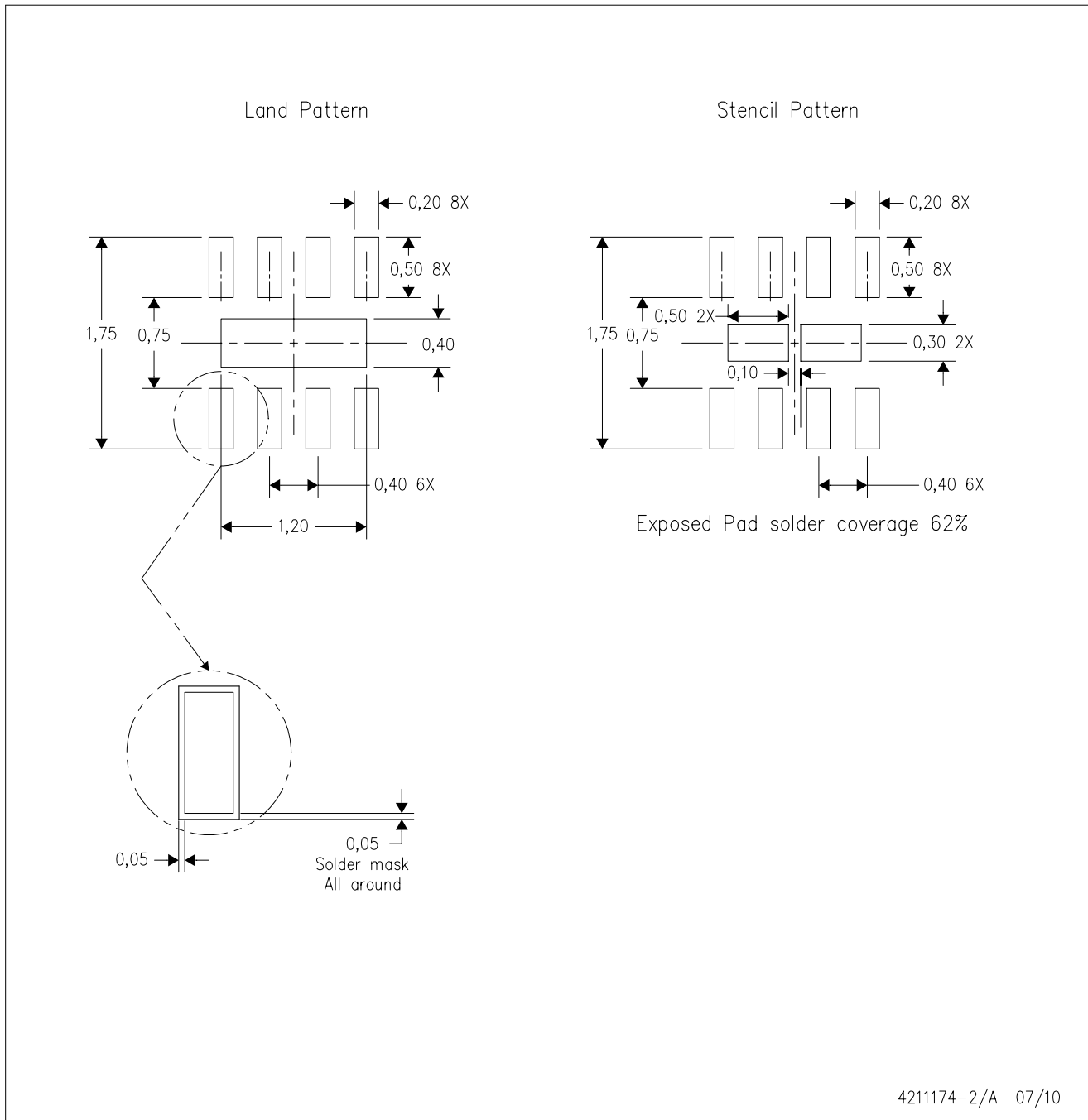
The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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