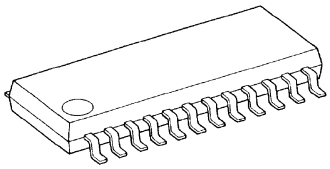
TOSHIBA Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD2005F

Low-Side Power Switch Array (8 Channels) for Motors, Solenoids, and Lamp Drivers

The TPD2005F is an 8-channel high-side switch array for vertical power MOS FET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.



SSOP24-P-300-1.00C

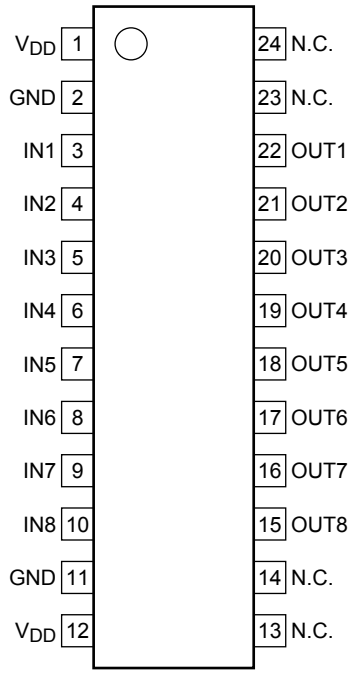
Weight: 0.29g (typ.)

Features

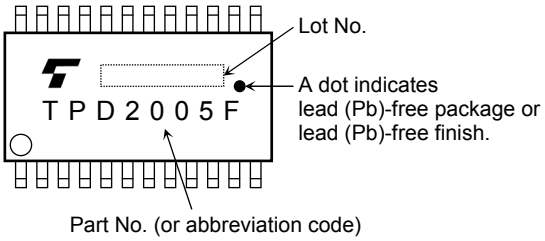
- A high-side switch array incorporating an N-channel power MOS FET (1.2 Ωmax.) and an 8-channel charge pump
- Can directly drive a power load from a microprocessor.
- Built-in protection against thermal shutdown protection and overcurrent protection
- 8-channel access enables space-saving design
- High operating voltage : 40 V
- Low on resistance : 1.2 Ωmax. (@V_{DD} = 12 V, I_O = 0.5 A (per channel))
- Supports parallel operation.
- Low operating current : 5 mA max. (@V_{DD} = 40 V, V_{IN} = 0 V)
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

Pin Assignment

(top view)

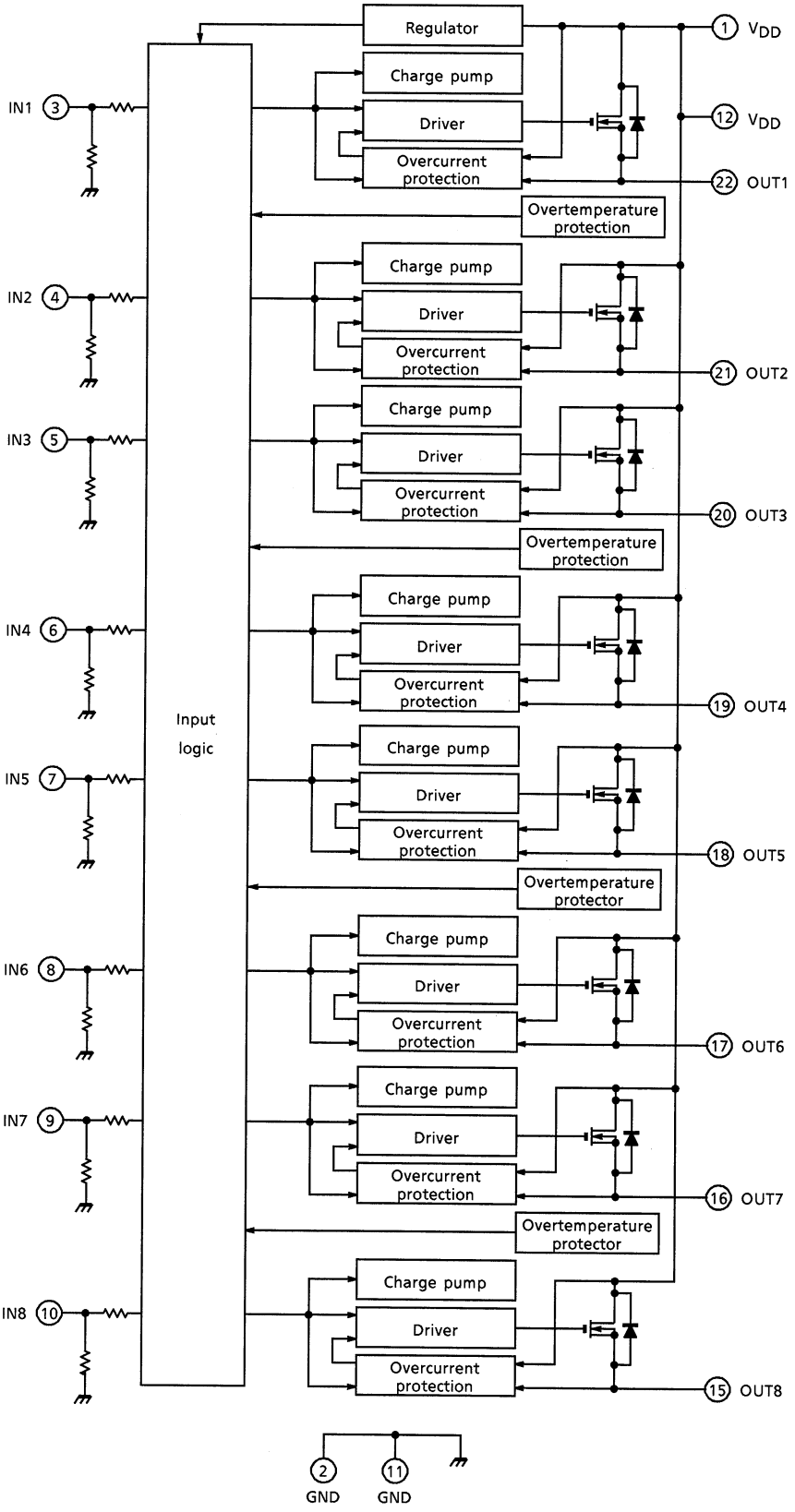


Marking



Note: Due to its MOS structure, this product is sensitive to static electricity.

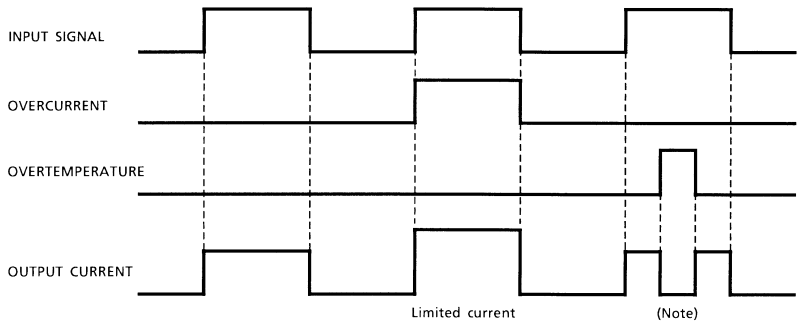
Block Diagram



Pin Description

Pin No.	Symbol	Description
1	V_{DD}	Power supply pin; in common with the pin No.12 internally.
2	GND	GND pin; in common with the pin No.11 internally.
3	IN1	Control input pin for channel 1 and built-in pull-down resistor (100 kΩ typ.)
4	IN2	Control input pin for channel 2 and built-in pull-down resistor (100 kΩ typ.)
5	IN3	Control input pin for channel 3 and built-in pull-down resistor (100 kΩ typ.)
6	IN4	Control input pin for channel 4 and built-in pull-down resistor (100 kΩ typ.)
7	IN5	Control input pin for channel 5 and built-in pull-down resistor (100 kΩ typ.)
8	IN6	Control input pin for channel 6 and built-in pull-down resistor (100 kΩ typ.)
9	IN7	Control input pin for channel 7 and built-in pull-down resistor (100 kΩ typ.)
10	IN8	Control input pin for channel 8 and built-in pull-down resistor (100 kΩ typ.)
11	GND	GND pin; in common with the pin No.2 internally.
12	V_{DD}	Power supply pin; in common with the pin No.1 internally.
13	N.C.	—
14	N.C.	—
15	OUT8	Output pin for channel 8
16	OUT7	Output pin for channel 7
17	OUT6	Output pin for channel 6
18	OUT5	Output pin for channel 5
19	OUT4	Output pin for channel 4
20	OUT3	Output pin for channel 3
21	OUT2	Output pin for channel 2
22	OUT1	Output pin for channel 1
23	N.C.	—
24	N.C.	—

Timing Chart



Note: The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

Truth Table

Input Signal	Output Signal	State
L	L	Normal
H	H	
L	L	Overcurrent
H	Internally limited	
L	L	Overtemperature
H	L	

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	45	V
Input voltage	V_{IN}	− 0.5 ~ 7	V
Drain-source voltage	V_{DS}	60	V
Output current	I_O	Internally limited	A
Power dissipation (operating all channels, ta = 25°C)	P_T	0.8	W
		1.2 (Note)	
Single pulse avalanche energy	E_{AS}	10	mJ
Operating temperature	T_{opr}	− 40 ~ 85	°C
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	− 55 ~ 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance junction to ambient (Operating all channels, Ta = 25°C)	$\Sigma R_{th\ (j\text{-}a)}$	156.3	°C / W
		104.2 (Note)	

Note: 60 mm × 60 mm × 1.6 mm when a device is mounted on a glass epoxy PCB (DC).

Electrical Characteristics
(Unless otherwise specified, V_{DD} = 8 ~ 40V, T_j = 25°C)

Characteristic		Symbol	Test Cir-cuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V_{DD}	—	—	8	—	40	V
Supply current		I_{DD}	—	V_{DD} = 40 V, V_{IN} = 0 V	—	—	5	mA
Input voltage	"L" level	V_{IL}	—		—	—	1.5	V
	"H" level	V_{IH}	—		3.5	—	—	
Input current		I_{IL}	—	V_{DD} = 24 V, V_{IN} = 0 V	−10	—	10	μA
		I_{IH}	—	V_{DD} = 24 V, V_{IN} = 5V	—	50	200	
On resistance		$R_{DS\ (ON)}$	—	V_{DD} = 12 V, I_O = 0.5 A	—	0.9	1.2	Ω
Output leakage current		I_{OL}	—	V_{DD} = 40 V, V_{IN} = 0 V	—	—	100	μA
Overcurrent protection		I_S	—	—	1	—	3	A
Thermal shutdown		T_{SD}	—	—	—	160	—	°C
		ΔT_{SD}	—	—	—	10	—	
Switching time		t_{ON}	1	V_{DD} = 12 V, R_L = 24Ω	—	11	200	μs
		t_{OFF}			—	4	50	

Description of Protector Circuit

(1) Overtemperature Protection

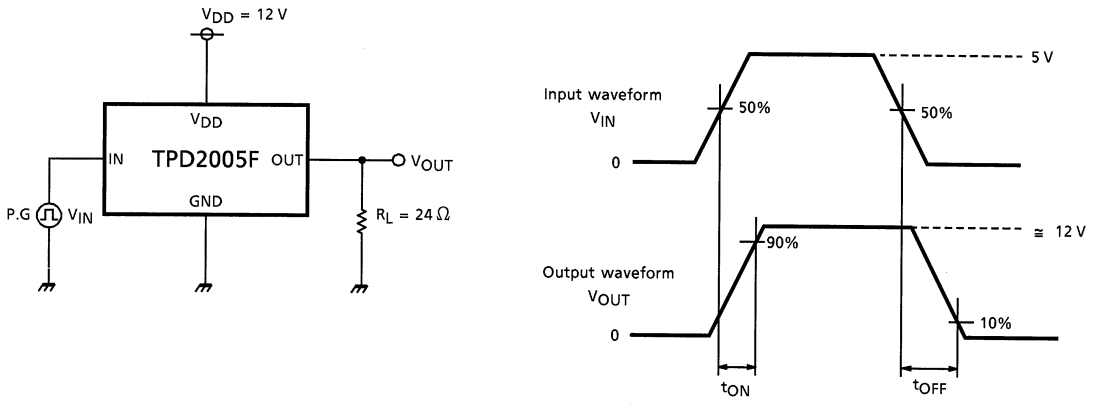
- There are four built-in overheating detector circuits, one each for channels 1 and 2; channels 3 and 4; channels 5 and 6; and channels 7 and 8, respectively. The circuit logic is such that, when any of the four detectors detects overheating, the circuit turns off the output of both its channels(for example, both channels 1 and 2).
- The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

(2) Overcurrent Protection

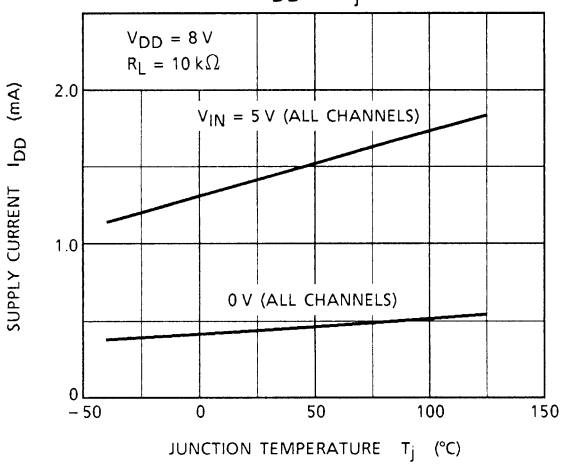
- When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

Test Circuit

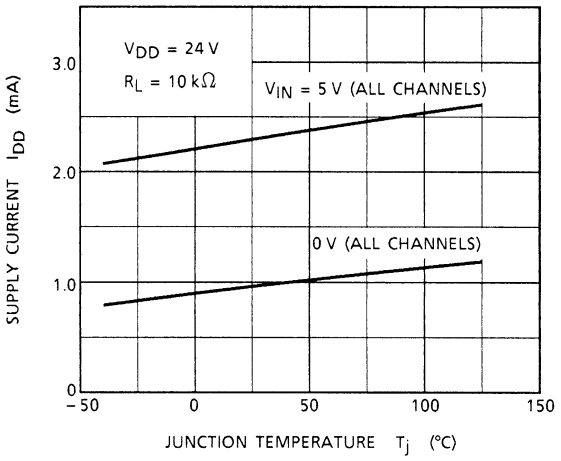
Switching Time



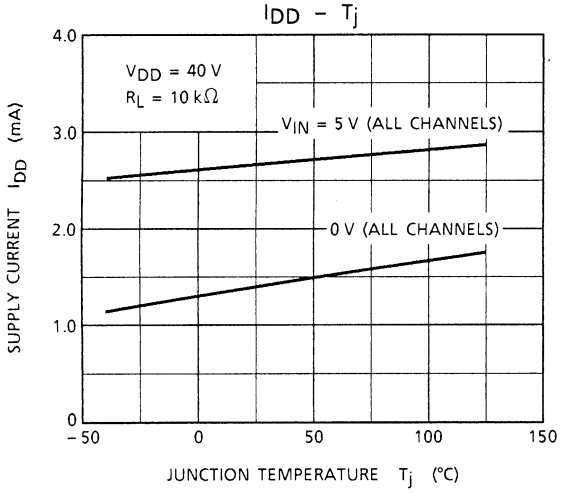
I_{DD} – T_j



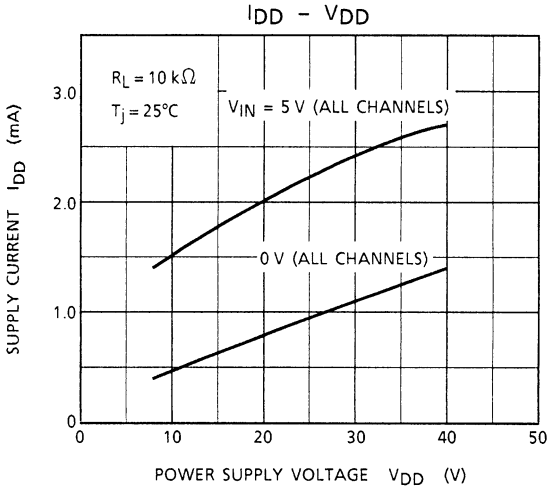
I_{DD} – T_j



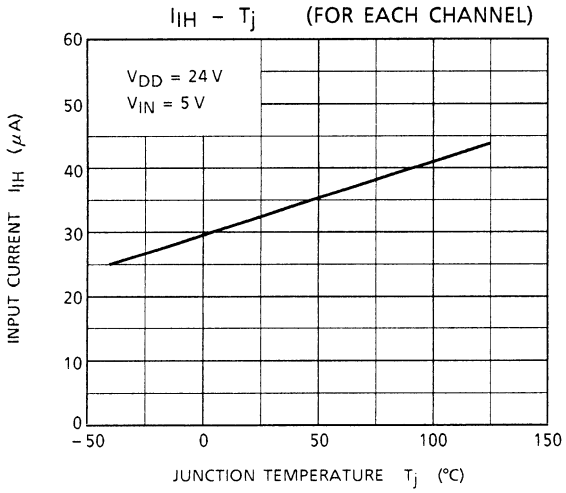
I_{DD} – T_j



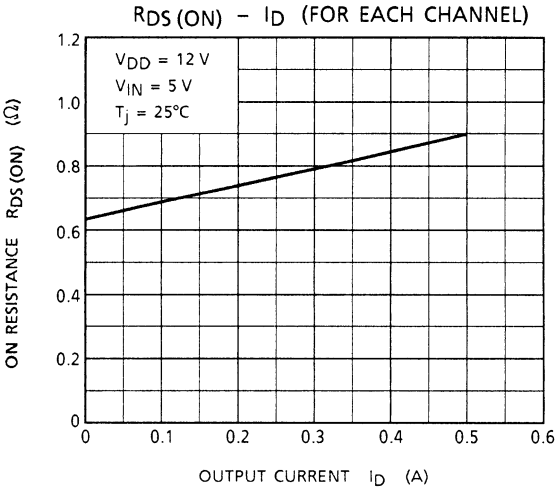
I_{DD} – V_{DD}



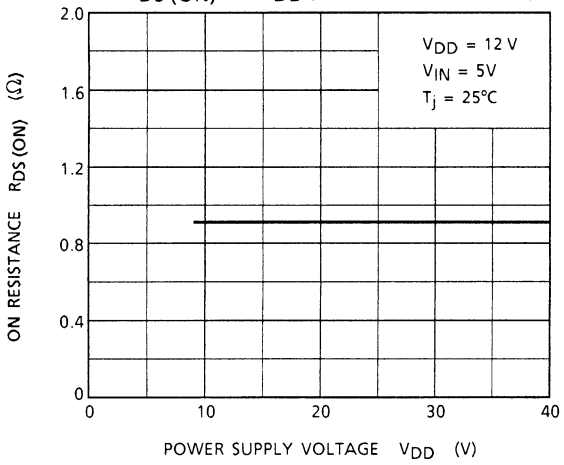
I_{IH} – T_j (FOR EACH CHANNEL)



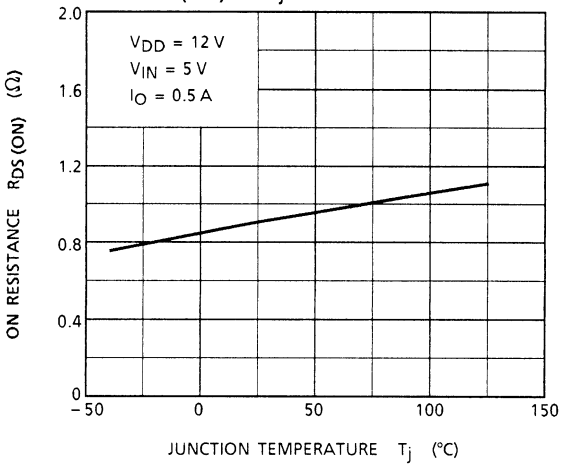
$R_{DS\,(ON)}$ – I_D (FOR EACH CHANNEL)



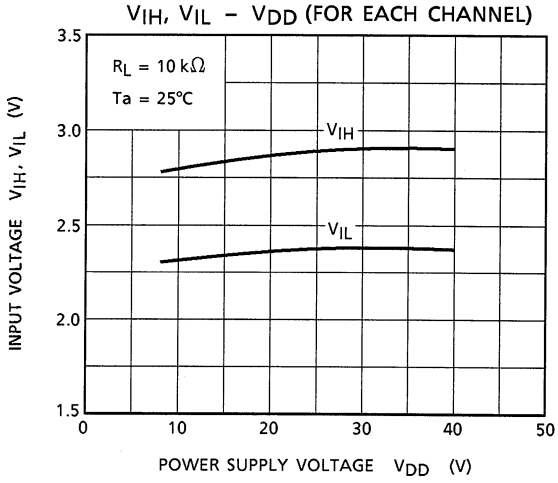
$R_{DS\,(ON)}$ – V_{DD} (FOR EACH CHANNEL)



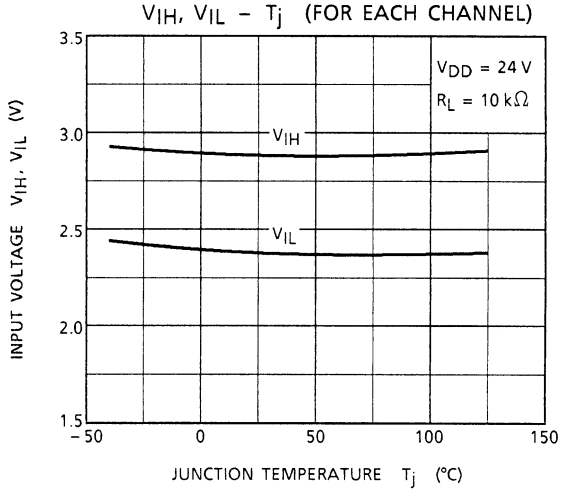
$R_{DS\,(ON)}$ – T_j (FOR EACH CHANNEL)



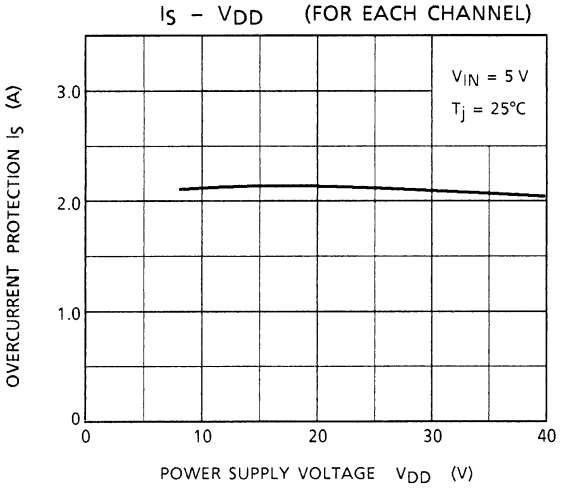
V_{IH}, V_{IL} – V_{DD} (FOR EACH CHANNEL)



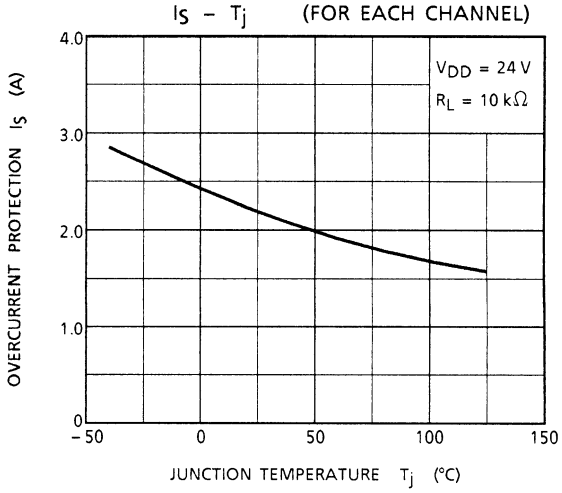
V_{IH}, V_{IL} – T_j (FOR EACH CHANNEL)



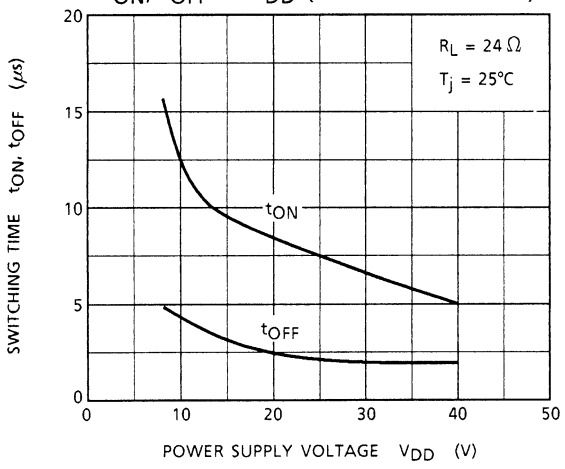
I_S – V_{DD} (FOR EACH CHANNEL)



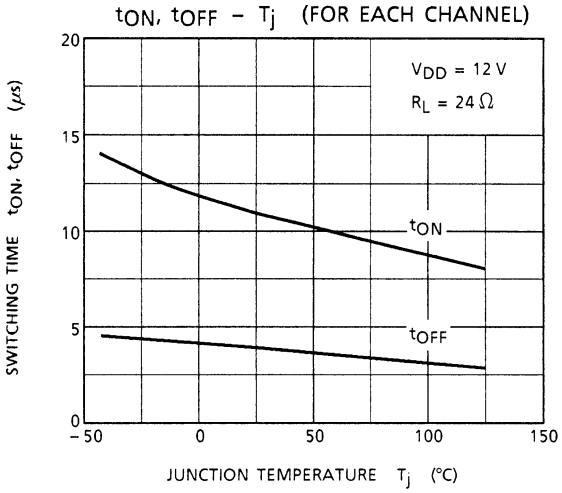
I_S – T_j (FOR EACH CHANNEL)



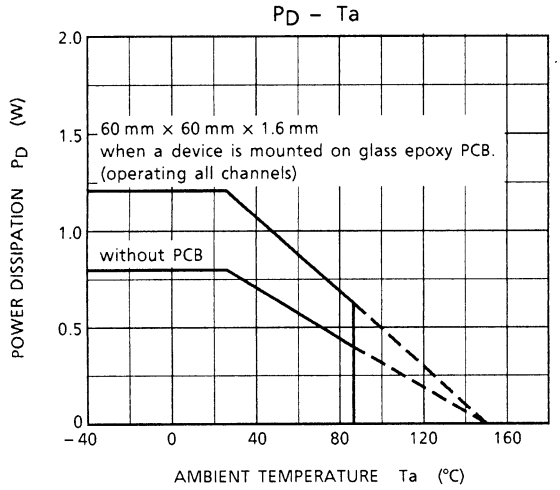
t_{ON}, t_{OFF} – V_{DD} (FOR EACH CHANNEL)



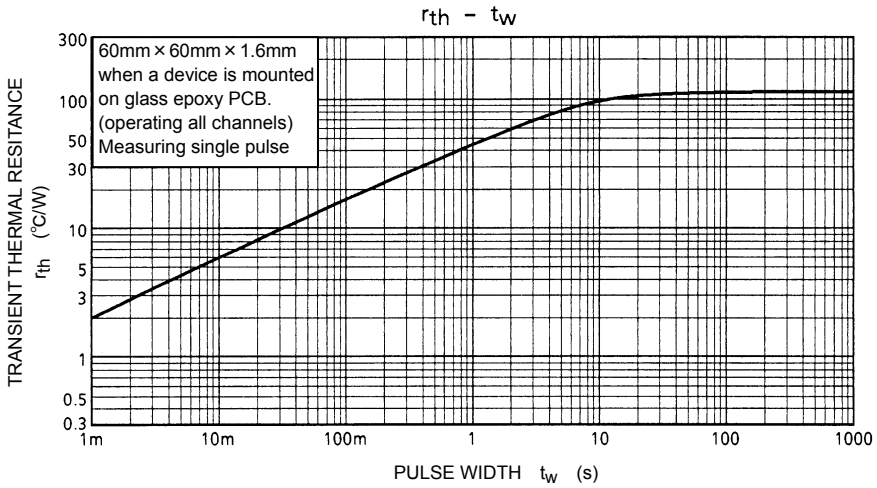
t_{ON}, t_{OFF} – T_j (FOR EACH CHANNEL)



P_D – Ta



r_{th} – t_w



Caution on Usage

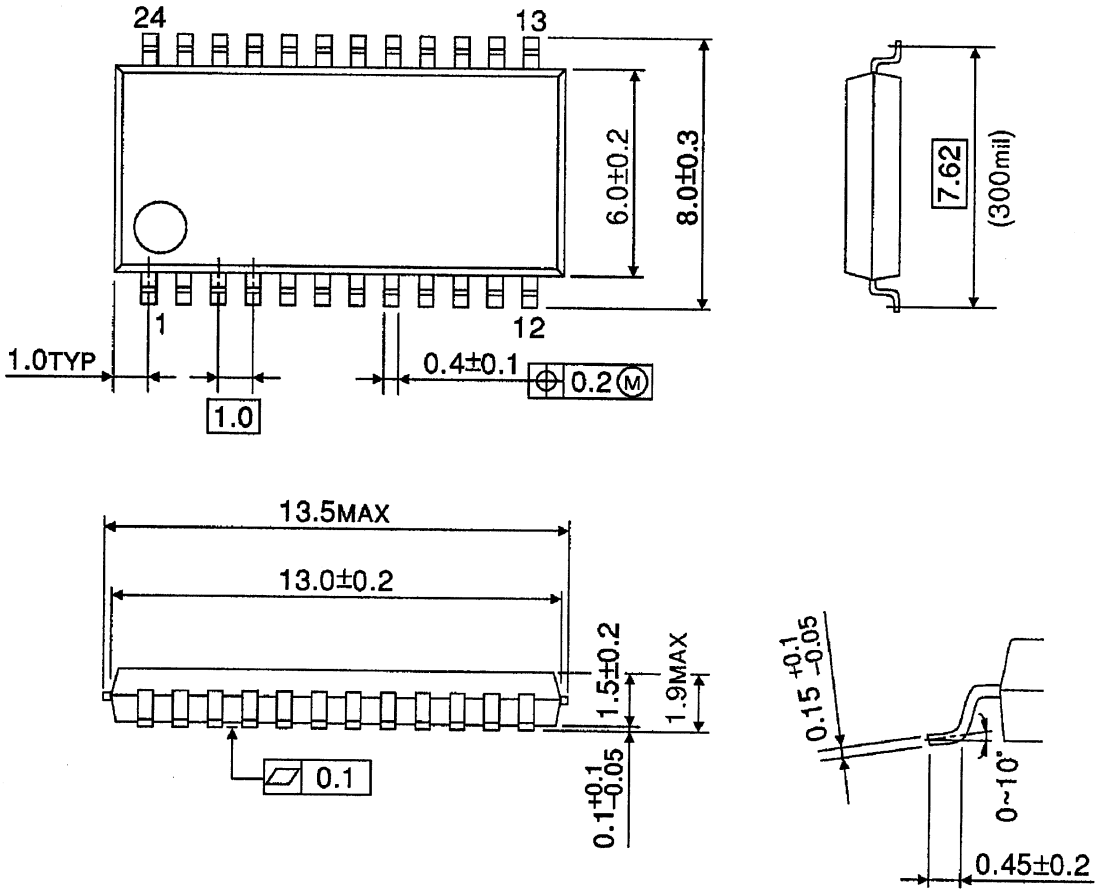
1. As protection against reverse connection of batteries is not provided, take protective measures using external circuits.
2. As a negative bias protector circuit is not built into the output pins, if negative bias is applied to the output pins, be sure to connect a freewheel diode between OUT and GND.

Moisture-Proof Packing

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within 48 hours.
Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.
Standard tape packing quantity: 2000 devices / reel (EL1)

Package Dimensions

SSOP24-P-300-1.00C Unit: mm



Weight: 0.29g (typ.)

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20070701-EN

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