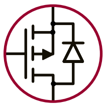


P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low threshold (-2.4V max.)
- High input impedance
- Low input capacitance (95pF typical)
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces - ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
TP0604N3-G	3-Lead TO-92	1000/Bag
TP0604N3-G P002	3-Lead TO-92	2000/Reel
TP0604N3-G P003		
TP0604N3-G P005		
TP0604N3-G P013		
TP0604N3-G P014		
TP2404NW	Die in wafer form	---
TP2404NJ	Die on adhesive tape	---
TP2404ND	Die in waffle pack	---

For packaged products, -G indicates package is RoHS compliant ('Green').
TO-92 taping specifications and winding styles per EIA-468 Standard.
Devices in Wafer / Die form are RoHS compliant ('Green').
Refer to Die Specification VF57 for layout and dimensions.

Absolute Maximum Ratings

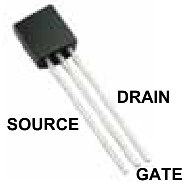
Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	$-55^{O}C$ to $+150^{O}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Summary

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)	$V_{GS(th)}$ (max) (V)
-40	2.0	-2.0	-2.4

Pin Configuration



TO-92 (N3)

Product Marking

SiTP
0 6 0 4
YYWW

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (A)	I_D (pulsed) (A)	Power Dissipation @T_A = 25°C (W)	θ_{ja} (°C/W)	I_{DR}† (A)	I_{DRM} (A)
TO-92	-0.43	-4.2	0.74	132	-0.43	-4.2

Notes:

† I_D (continuous) is limited by max rated T_j .

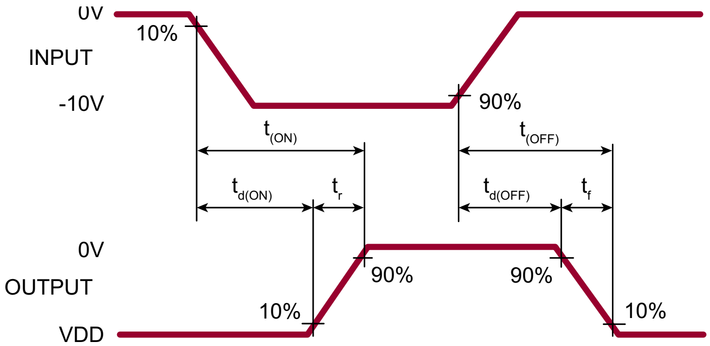
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

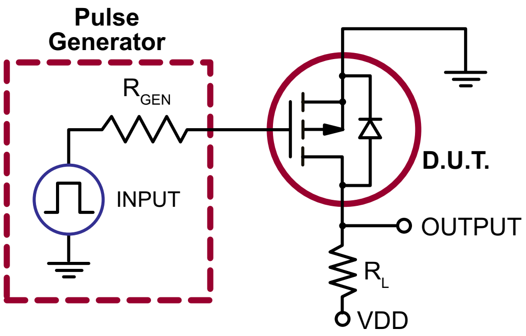
Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-40	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D= -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.0	-4.5	mV/°C	V_{GS} = V_{DS}, I_D= -1.0mA
I_{GSS}	Gate body leakage	-	-	-100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current	-0.4	-0.6	-	A	V_{GS} = -5.0V, V_{DS} = -20V
		-2.0	-3.3	-		V_{GS} = -10V, V_{DS} = -20V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	3.5	Ω	V_{GS} = -5.0V, I_D = -250mA
		-	1.5	2.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.2	%/°C	V_{GS} = -10V, I_D = -1.0A
G_{FS}	Forward transductance	400	600	-	mmho	V_{DS} = -20V, I_D = -1.0A
C_{ISS}	Input capacitance	-	95	150	pF	V_{GS} = 0V, V_{DS} = -20V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	85	120		
C_{RSS}	Reverse transfer capacitance	-	35	60		
$t_{d(ON)}$	Turn-on delay time	-	5.0	8.0	ns	V_{DD} = -20V, I_D = -1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	7.0	18		
$t_{d(OFF)}$	Turn-off delay time	-	10	15		
t_f	Fall time	-	6.0	19		
V_{SD}	Diode forward voltage drop	-	-1.3	-2.0	V	V_{GS} = 0V, I_{SD} = -1.5A
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -1.5A

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300μs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

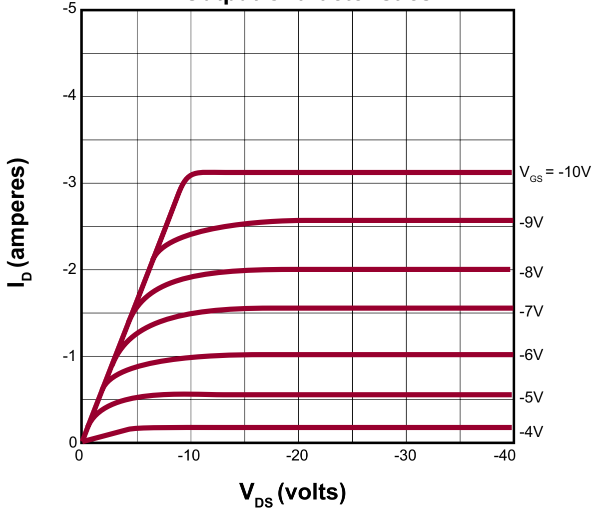
Switching Waveforms and Test Circuit



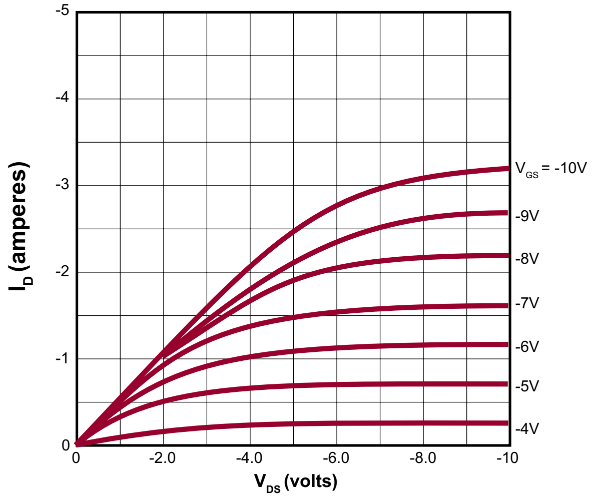


Typical Performance Curves

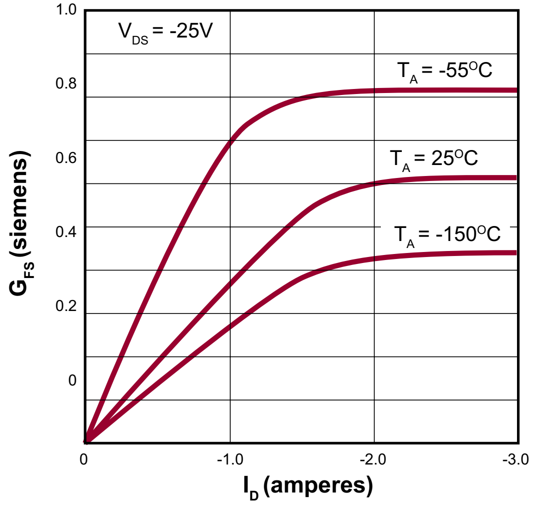
Output Characteristics



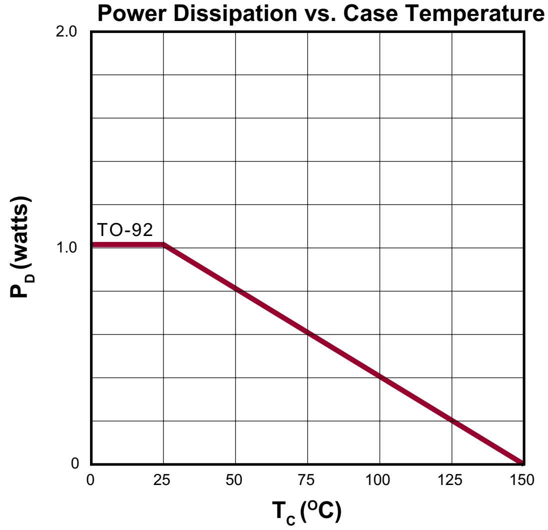
Saturation Characteristics



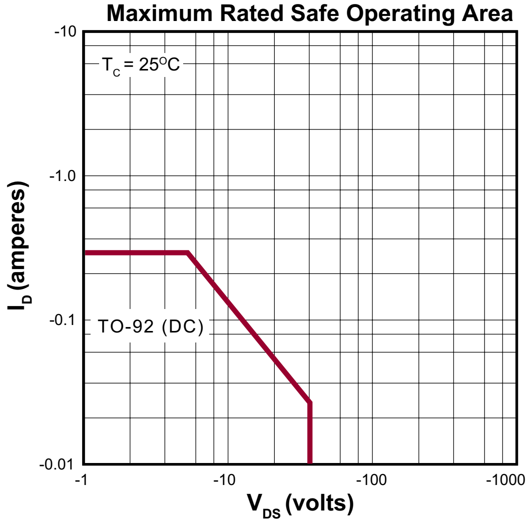
Transconductance vs. Drain Current



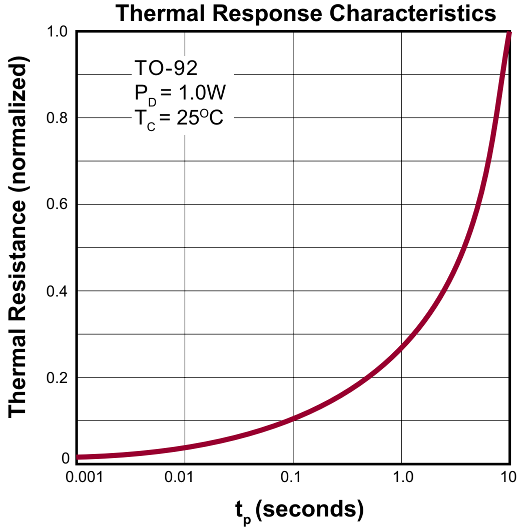
Power Dissipation vs. Case Temperature



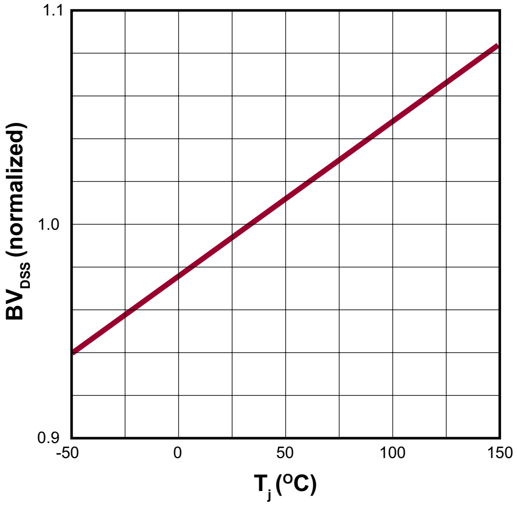
Maximum Rated Safe Operating Area

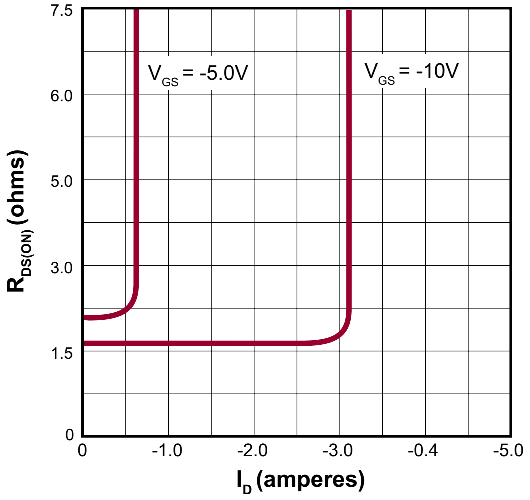


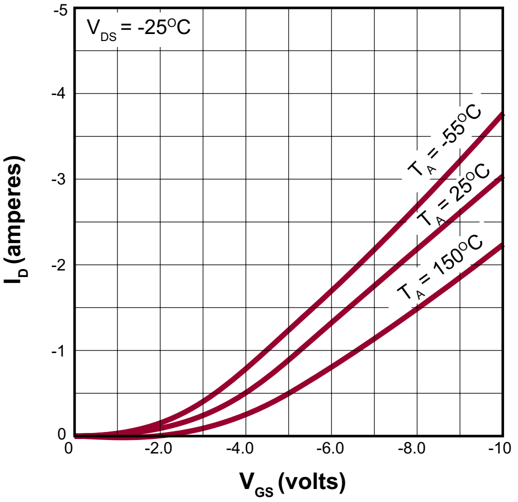
Thermal Response Characteristics

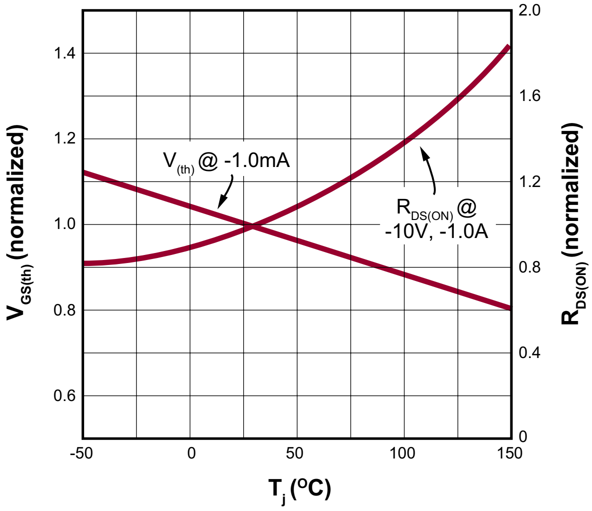


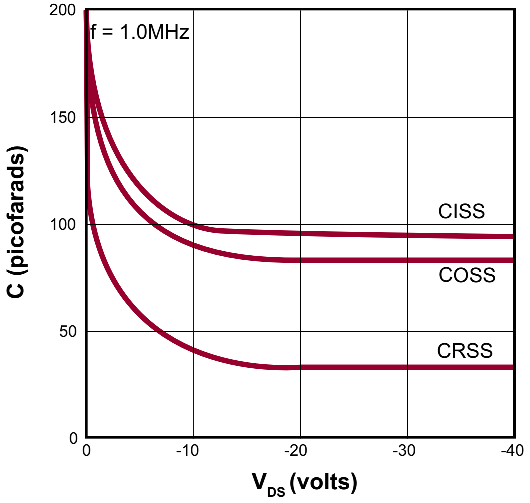
Typical Performance Curves *(cont.)*

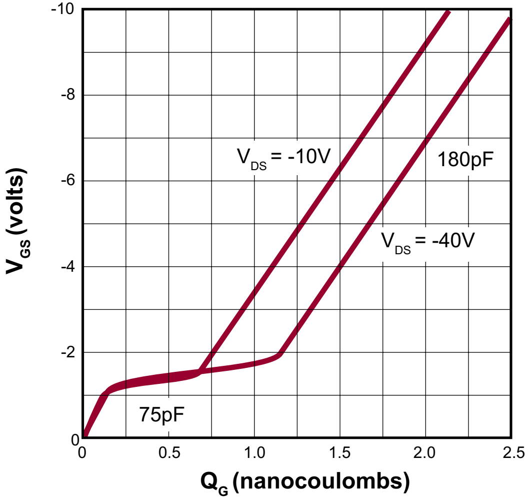

BV$_{DSS}$ Variation with Temperature


On-Resistance vs. Drain Current

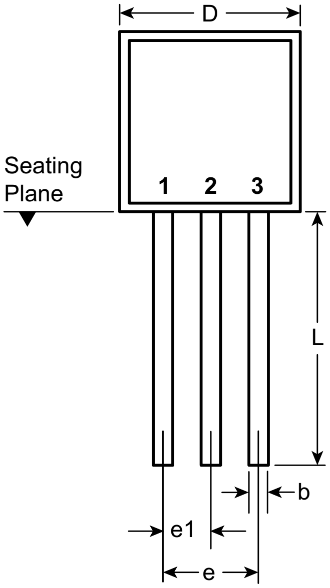

Transfer Characteristics


V$_{(th)}$ and R$_{DS}$ Variation with Temperature

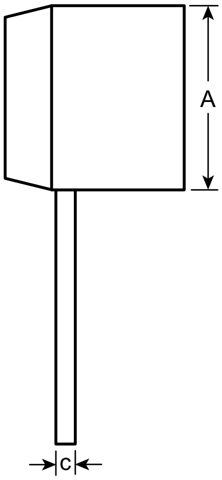

Capacitance vs. Drain-to-Source Voltage


Gate Drive Dynamic Characteristics

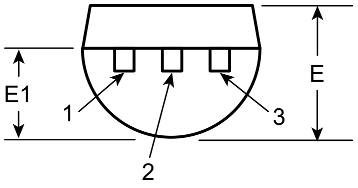
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)