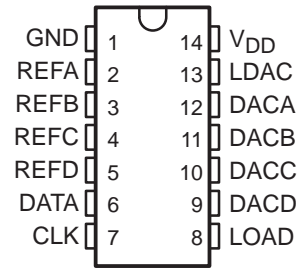


TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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- Four 8-Bit Voltage Output DACs
- 3-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable for 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low-Power Consumption
- Half-Buffered Output

D OR N PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLV5620C and TLV5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND; and, the DACs are monotonic. The device is simple to use, because it runs from a single supply of 3 V to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5620C and TLV5620I is over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs update simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLV5620C is characterized for operation from 0°C to 70°C. The TLV5620I is characterized for operation from -40°C to 85°C. The TLV5620C and TLV5620I do not require external trimming.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLV5620CD	TLV5620CN
-40°C to 85°C	TLV5620ID	TLV5620IN



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

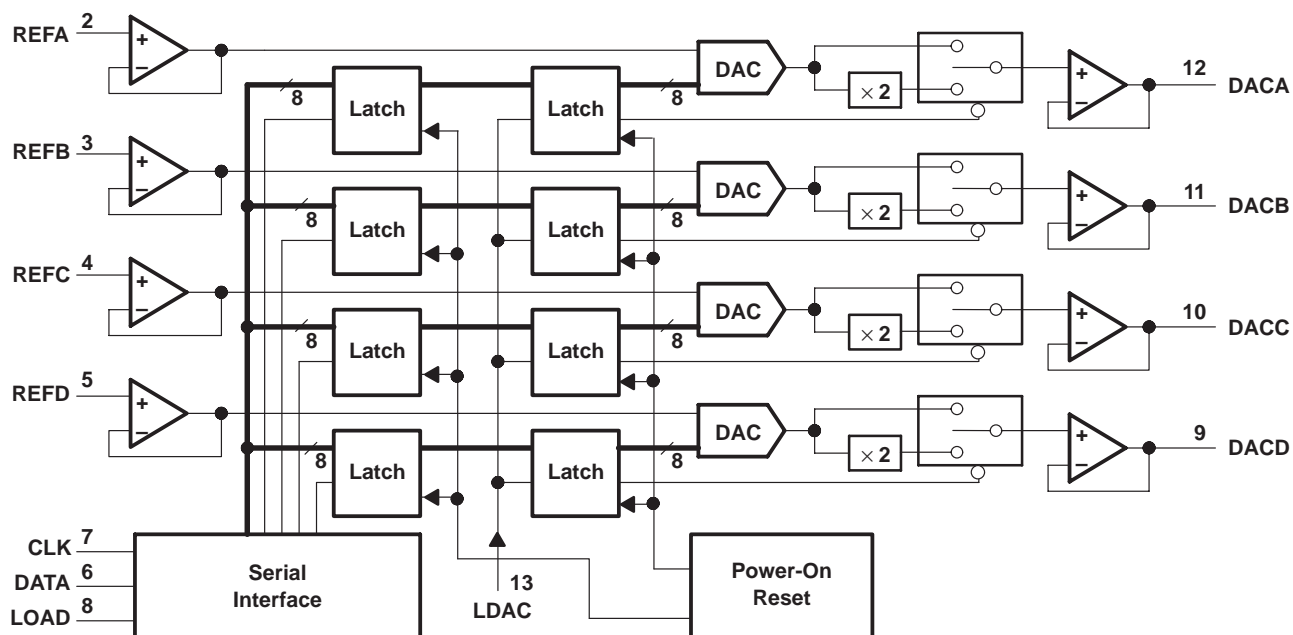
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When this signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial interface load control. When the LDAC terminal is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the analog output range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the analog output range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the analog output range.
VDD	14	I	Positive supply voltage

detailed description

The TLV5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first. Data transfers using two 8-clock-cycle periods are shown in Figures 3 and 4.

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

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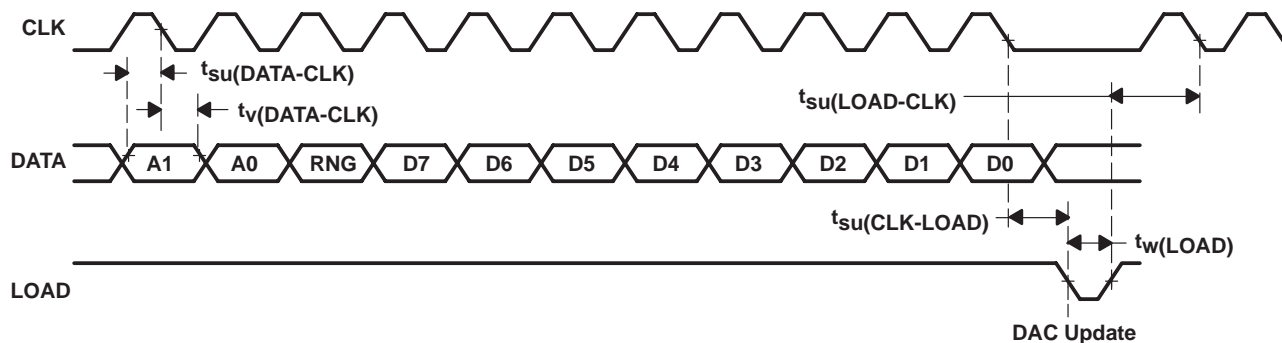


Figure 1. LOAD-Controlled Update (LDAC = Low)

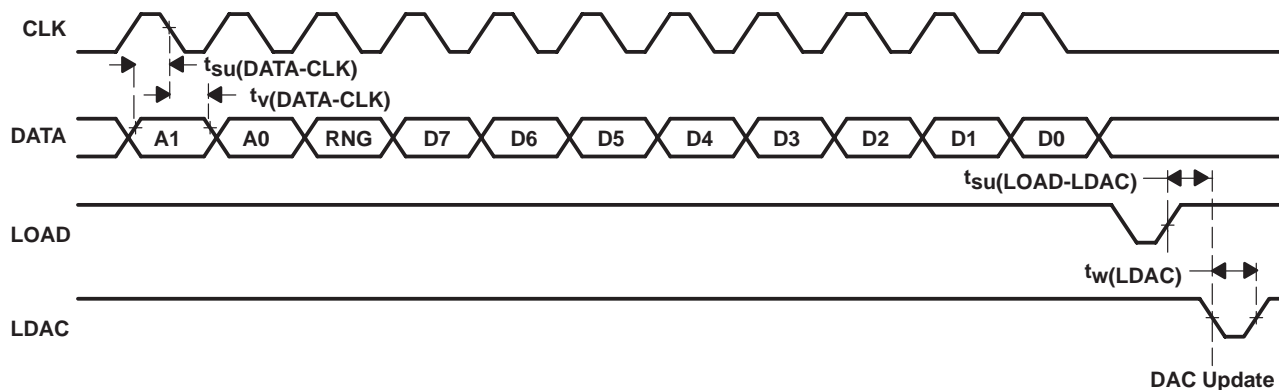


Figure 2. LDAC-Controlled Update



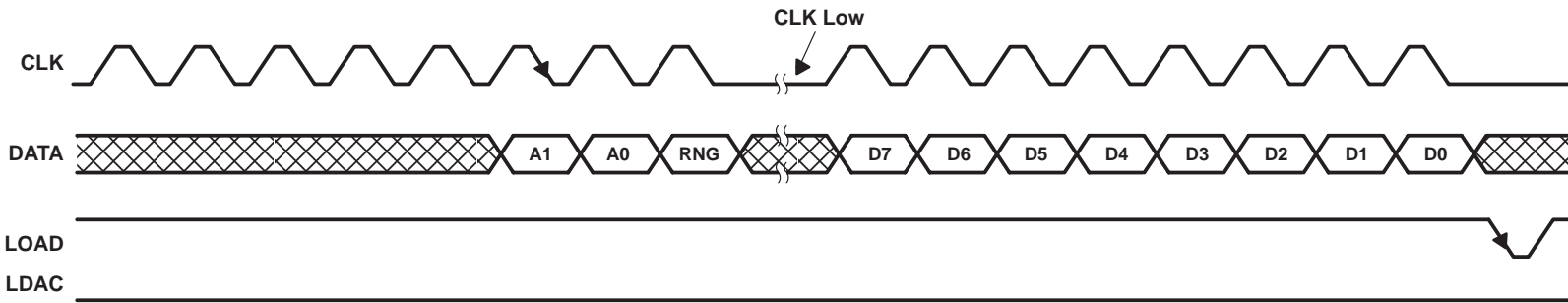


Figure 3. Load Controlled Update Using 8-Bit Serial Word (LDAC = Low)

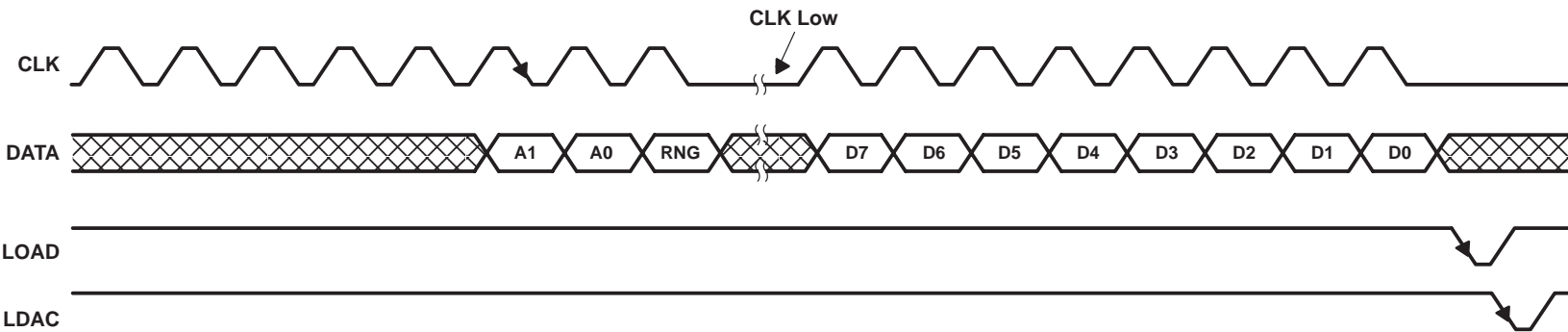


Figure 4. LDAC Controlled Update Using 8-Bit Serial Word

TLV5620C, TLV5620I

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linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

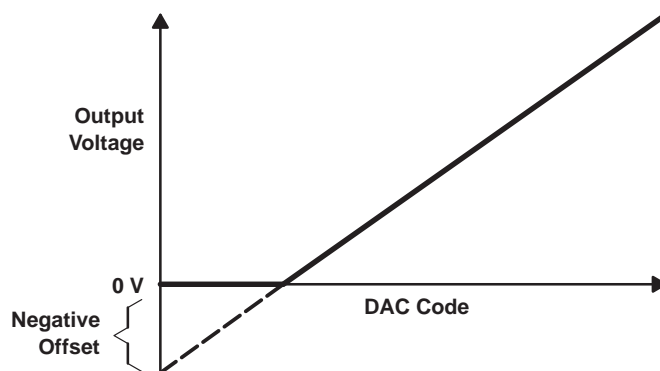


Figure 5. Effect of Negative Offset (Single Supply)

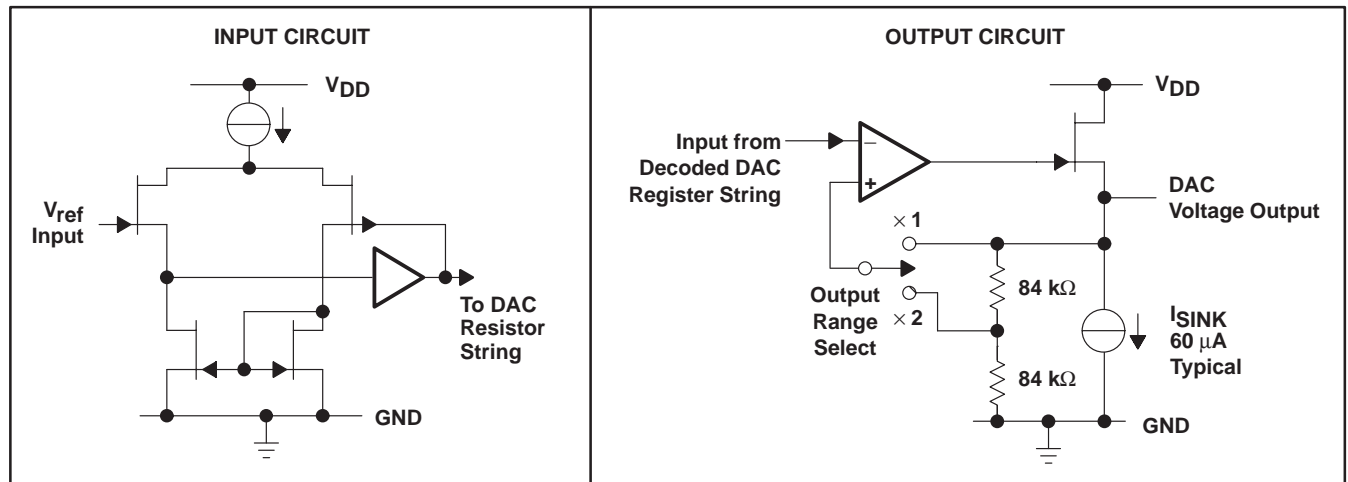
This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range	$GND - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Reference input voltage range, V_{ID}	$GND - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Operating free-air temperature range, T_A : TLV5620C	0°C to 70°C
TLV5620I	-40°C to 85°C
Storage temperature range, T_{stg}	-50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3.3	5.25	V
High-level input voltage, V_{IH}	$0.8 V_{DD}$			V
Low-level input voltage, V_{IL}	0.8			V
Reference voltage, V_{ref} [A B C D], x1 gain	$V_{DD} - 1.5$			V
Load resistance, R_L	10			$\text{k}\Omega$
Setup time, data input, $t_{su}(\text{DATA-CLK})$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $\text{CLK}\downarrow$, $t_v(\text{DATA-CLK})$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su}(\text{CLK-LOAD})$ (see Figure 1)	50			ns
Setup time, $\text{LOAD}\uparrow$ to $\text{CLK}\downarrow$, $t_{su}(\text{LOAD-CLK})$ (see Figure 1)	50			ns
Pulse duration, LOAD, $t_w(\text{LOAD})$ (see Figure 1)	250			ns
Pulse duration, LDAC, $t_w(\text{LDAC})$ (see Figure 2)	250			ns
Setup time, $\text{LOAD}\uparrow$ to $\text{LDAC}\downarrow$, $t_{su}(\text{LOAD-LDAC})$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLV5620C	0	70	$^\circ\text{C}$
	TLV5620I	-40	85	

TLV5620C, TLV5620I

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electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V to }3.6\text{ V}$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$			± 10	μA
I_{IL}	Low-level input current	$V_I = 0\text{ V}$			± 10	μA
$I_{O(\text{sink})}$	Output sink current	Each DAC output	20			μA
$I_{O(\text{source})}$	Output source current		1			mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	$V_{DD} = 3.3\text{ V}$			2	mA
I_{ref}	Reference input current	$V_{DD} = 3.3\text{ V}$, $V_{ref} = 1.5\text{ V}$			± 10	μA
E_L	Linearity error (end point corrected)	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 1			± 1	LSB
E_D	Differential linearity error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 2			± 0.9	LSB
E_{ZS}	Zero-scale error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 3	0		30	mV
	Zero-scale error temperature coefficient	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 4		10		$\mu\text{V}/^\circ\text{C}$
E_{FS}	Full-scale error	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 5			± 60	mV
	Full-scale error temperature coefficient	$V_{ref} = 1.25\text{ V}$, $\times 2$ gain, See Note 6		± 25		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

- NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output ($V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$.
6. Full-scale error temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varying the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V to }3.6\text{ V}$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Output settling time	To $\pm 0.5\text{ LSB}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 9		10		μs
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	$\text{CLK} = 1\text{-MHz}$ square wave measured at DACA-DACD		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES: 9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within $\pm 0.5\text{ LSB}$ starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz .
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz .
12. Reference bandwidth is the -3 dB bandwidth with an input at $V_{ref} = 1.25\text{ V}$ dc + 2 V_{PP} and with a digital input code of full-scale.



PARAMETER MEASUREMENT INFORMATION

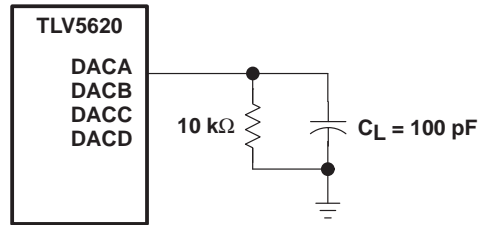
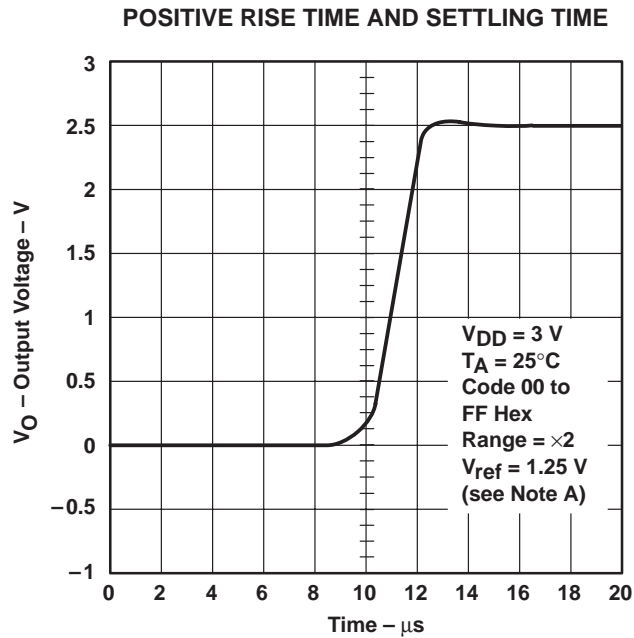


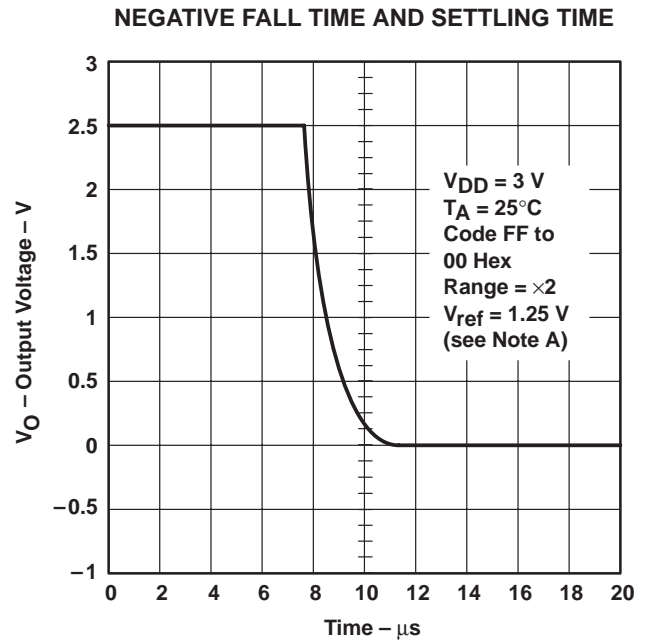
Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS



NOTE A: Rise time = 2.05 μ s, positive slew rate = 0.96 V/ μ s, settling time = 4.5 μ s.

Figure 7



NOTE A: Fall time = 4.25 μ s, negative slew rate = 0.46 V/ μ s, settling time = 8.5 μ s.

Figure 8

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TYPICAL CHARACTERISTICS

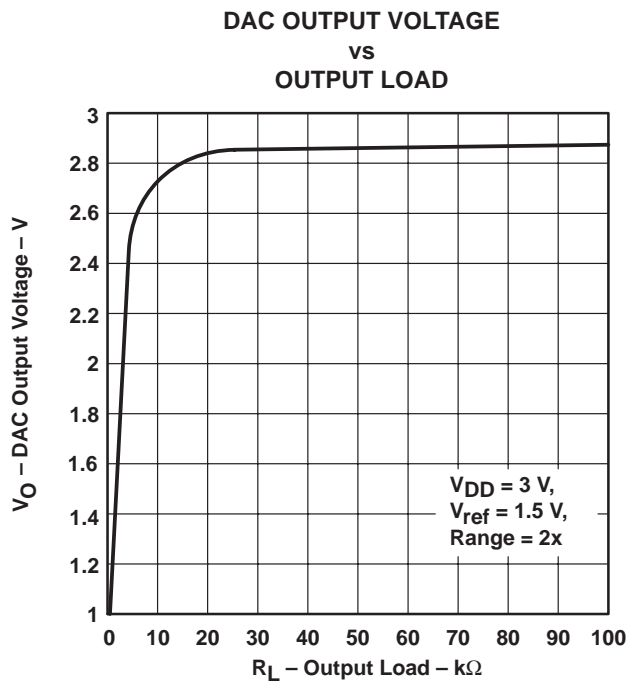


Figure 9

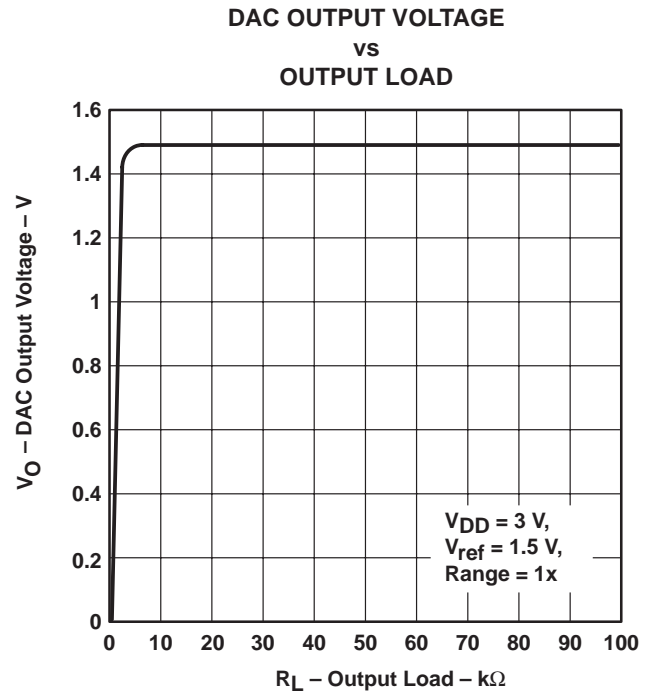


Figure 10

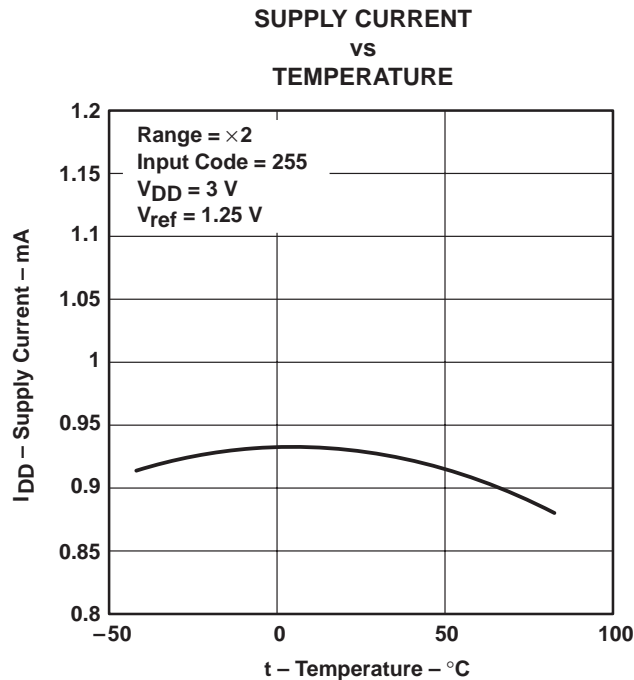
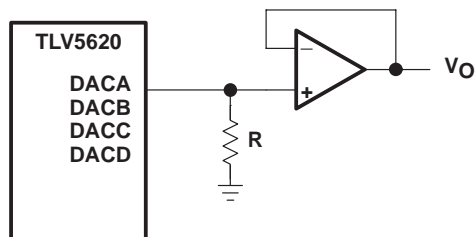


Figure 11

APPLICATION INFORMATION



NOTE A: Resistor R \geq 10 k Ω

Figure 12. Output Buffering Scheme

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV5620CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5620C	Samples
TLV5620CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5620C	Samples
TLV5620CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5620C	Samples
TLV5620CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5620C	Samples
TLV5620CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV5620CN	Samples
TLV5620CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV5620CN	Samples
TLV5620ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5620I	Samples
TLV5620IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5620I	Samples
TLV5620IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5620I	Samples
TLV5620IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5620I	Samples
TLV5620IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLV5620IN	Samples
TLV5620INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLV5620IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5620IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5620IDR	SOIC	D	14	2500	367.0	367.0	38.0

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