TLV320AIC3268 Low Power Stereo Audio Codec With 105dB DAC, DirectPath Headphone and Class-D Speaker Amplifier and Integrated miniDSP

1 Features

- 105dB SNR for Stereo Audio DAC to Differential Lineout
- 95dB SNR for Stereo Line Input to Audio ADC
- 8-192kHz Playback and Record
- 24 mW output power from DirectPath™ Headphone Driver
- 121 mW output power from Differential Receiver Output Driver
- Class-D Speaker Driver with
  - 1.45 W (8Ω, 5V, 10% THDN)
  - 1.15 W (8Ω, 5V, 1% THDN)
- Differential or Single-Ended Stereo Line Outputs
- Eight Single-Ended or 4 Fully-Differential Analog Inputs
- Analog Microphone Inputs, and Up to 4 Simultaneous Digital Microphone Channels
- Extensive Signal Processing Options
- Fully-programmable Enhanced miniDSP
- Three Independent Digital Audio Serial Interfaces with Separate I/O Power Voltages
  - TDM and mono PCM support on all Audio Serial Interfaces (ASI)
  - 8-channel Input and Output on ASI 1
- Programmable PLL, plus Low-Frequency Clocking
- Programmable 12-Bit SAR ADC
- SPI and I^2C Control Interfaces

2 Applications

- Low Power Portable Audio Devices
- Consumer Audio Devices
- Infotainment Systems

3 Description

The TLV320AIC3268 (AIC3268) provides users with an integrated method to implement an audio system with multiple digital and analog audio streams as sources, and multiple output devices such as high-powered audio amplifiers. The integrated miniDSP allows users to differentiate their products by enabling customization of signal processing on the audio streams. The low power consumption of this device is ideal for systems that are battery operated or that operate in a constrained power consumption environment.

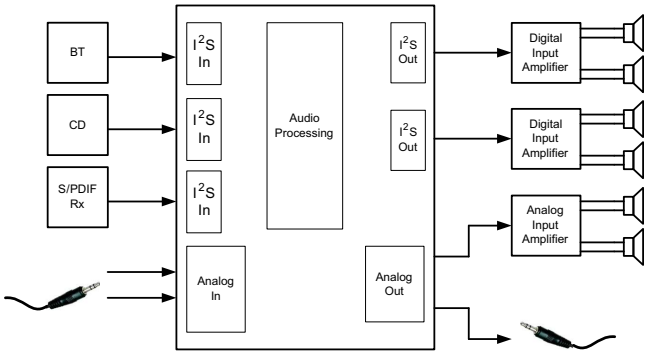
The AIC3268 is an integrated, low-power, low-voltage stereo audio codec and also features four digital microphone inputs, plus programmable outputs, predefined and parameterizable signal processing blocks and an integrated PLL. Extensive register-based control of power, input and output channel configuration, gains, effects, terminal-multiplexing and clocks are included, allowing the device to be precisely targeted to its application.

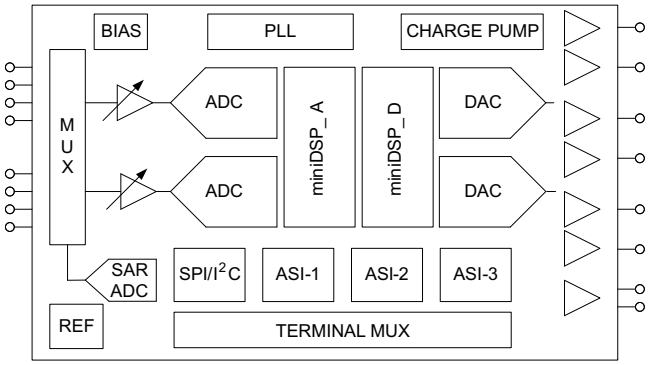
The AIC3268 supports a range of applications from mono 8kHz voice to stereo 192kHz music, making it ideal for wide variety of low power battery-operated and consumer audio applications.

Device Information

DEVICE NAME	PACKAGE	BODY SIZE
TLV320AIC3268	VQFN (64)	9mm × 9mm

4 Simplified Diagrams





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5 Revision History

Changes from Revision Initial Release (January 2014) to Revision A	Page
• Changed to Production Data document status	1
• Converted to new data sheet format	1

6 Terminal Configuration and Functions

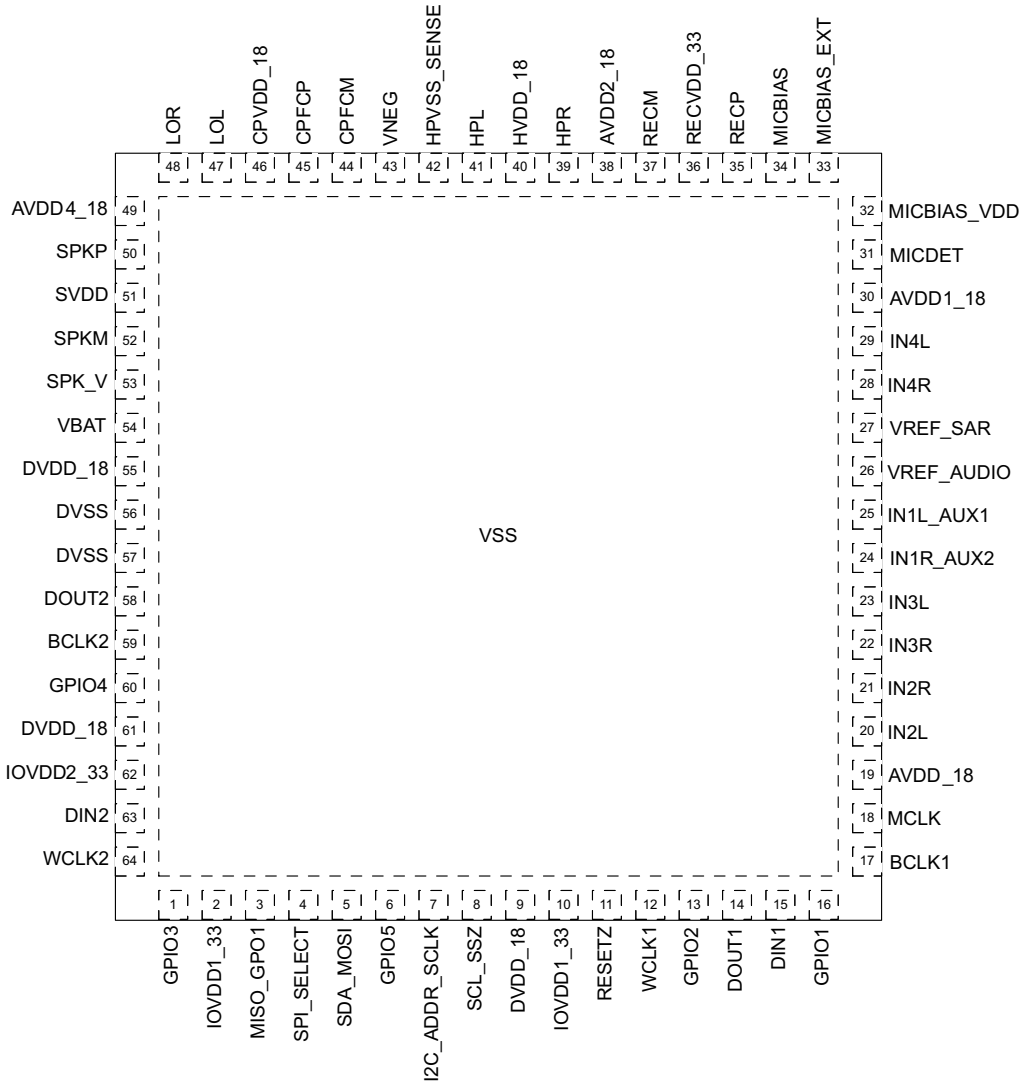


Figure 1. QFN-64(RGC) Package Terminal Assignments (Top View)

Terminal Functions – 64 Terminal QFN (RGC) Package

QFN (RGC) TERMINAL NUMBER	NAME	I,O,IO,P	POWER DOMAIN	DESCRIPTION
1	GPIO3	IO	IOVDD2	Multi Function Digital IO 3 See Table 47
2	IOVDD1_33	P	IOVDD1	Digital I/O Buffer Supply 1 (Not internally connected to terminal no. 10)
3	MISO_GPO1	O	IOVDD1	Multi Function Digital Output 1 Primary: (SPI_SELECT = 1) SPI Serial Data Output Secondary: (SPI_SELECT = 0) See Table 46

Terminal Functions – 64 Terminal QFN (RGC) Package (continued)

QFN (RGC) TERMINAL NUMBER	NAME	I,O,IO,P	POWER DOMAIN	DESCRIPTION
4	SPI_SELECT	I	IOVDD1	Control Interface Select SPI_SELECT = '1' : SPI interface selected SPI_SELECT = '0' : I2C interface selected
5	SDA_MOSI	IO	IOVDD1	Primary: (SPI_SELECT = '1') SPI interface mode serial data input Secondary: (SPI_SELECT = '0') I2C interface mode serial data
6	GPIO5	IO	IOVDD1	Multi Function Digital IO 5 See Table 47
7	I2C_ADDR_SCLK	I	IOVDD1	Primary: (SPI_SELECT = '1') SPI Serial Clock Secondary: (SPI_SELECT = '0') I2C Address Bit (I2C_ADDR)
8	SCL_SSZ	IO	IOVDD1	Primary: (SPI_SELECT = '1') SPI Chip Select Secondary: (SPI_SELECT = '0') I2C Clock
9	DVDD_18	P	Digital	1.8V Digital Power Supply (Not internally connected to terminal no. 55)
10	IOVDD1_33	P	IOVDD1	Digital IO Buffer Supply 1 (Not internally connected to terminal no. 2)
11	$\overline{\text{RESET}}$	I		Active Low Reset
12	WCLK1	IO	IOVDD1	Primary: Audio Serial Data Bus 1 Word Clock Secondary: See Table 46
13	GPIO2	IO	IOVDD1	Multi Function Digital IO 2 See Table 47
14	DOUT1	O	IOVDD1	Primary: Audio Serial Data Bus 1 Data Output Secondary: See Table 46
15	DIN1	I	IOVDD1	Primary: Audio Serial Data Bus 1 Data Input Secondary: See Table 46
16	GPIO1	IO	IOVDD1	Multi Function Digital IO 1 See Table 47
17	BCLK1	IO	IOVDD1	Primary: Audio Serial Data Bus 1 Bit Clock Secondary: See Table 46
18	MCLK	I	IOVDD1	Master Clock Input
19	AVDD_18	P	Analog	1.8V Analog Power Supply
20	IN2L	I	Analog	Analog Input 2 Left
21	IN2R	I	Analog	Analog Input 2 Right
22	IN3R	I	Analog	Analog Input 3 Right
23	IN3L	I	Analog	Analog Input 3 Left

Terminal Functions – 64 Terminal QFN (RGC) Package (continued)

QFN (RGC) TERMINAL NUMBER	NAME	I,O,IO,P	POWER DOMAIN	DESCRIPTION
24	IN1R_AUX2	I	Analog	Analog Input 1 Right Auxilliary 2 Input to SAR ADC (Special Function: Right Channel High Impedance Input for Capacitive Sensor Measurement)
25	IN1L_AUX1	I	Analog	Analog Input 1 Left Auxilliary 1 Input to SAR ADC (Special Function: Left Channel High Impedance Input for Capacitive Sensor Measurement)
26	VREF_AUDIO	I	Analog	Analog Reference Voltage Filter Output
27	VREF_SAR	IO	Analog	SAR ADC Voltage Reference Input or SAR ADC Internal Voltage Reference Bypass Capacitor Terminal
28	IN4R	I	Analog	Analog Input 4 Right
29	IN4L	I	Analog	Analog Input 4 Left
30	AVDD1_18	P	Analog	1.8V Analog Power Supply
31	MICDET	IO	Analog	Headset Detection Terminal
32	MICBIAS_VDD	P	Analog	Power Supply for Micbias
33	MICBIAS_EXT	O	Analog	Output Bias Voltage for Headset Microphone
34	MICBIAS	O	Analog	Output Bias Voltage for on-board Microphones
35	RECP	O	Analog	Receiver Driver P side Output
36	RECVDD_33	P	Analog	3.3V Power Supply for Receiver Driver
37	RECM	O	Analog	Receiver Driver M side Output
38	AVDD2_18	P	Analog	1.8V Analog Power Supply
39	HPR	O	Analog	Right Headphone Output
40	HVDD_18	P	Analog	Headphone Amplifier Power Supply
41	HPL	O	Analog	Left Headphone Output
42	HPVSS_SENSE	I	Analog	Headphone Ground Sense Terminal
43	VNEG	IO	Analog	Charge Pump Negative Supply
44	CPFCM	IO	Analog	Charge Pump Flying Capacitor M Terminal
45	CPFCP	IO	Analog	Charge Pump Flying Capacitor P Terminal
46	CPVDD_18	P	Analog	Power Supply Input for Charge Pump
47	LOL	O	Analog	Left Line Output
48	LOR	O	Analog	Right Line Output
49	AVDD4_18	P	Analog	1.8V Analog Power Supply for Speaker Amplifier
50	SPKP	O	Speaker	P side Speaker Amplifier Output
51	SVDD	P	Speaker	Speaker Amplifier Output Stage Power Supply
52	SPKM	O	Speaker	M side Speaker Amplifier Output
53	SPK_V	P	Speaker	Speaker Amplifier Output Stage Power Supply (Connect to SVDD through a resistor)
54	VBAT	I	Speaker	Battery Monitor Voltage Input
55	DVDD_18	P	Digital	1.8V Digital Power Supply (Not internally connected to terminal no. 9 and 61)
56	DVSS	P	Digital	Digital Ground (Not internally connected to terminal no. 57 and Thermal Pad)
57	DVSS	P	Digital	Digital Ground (Not internally connected to terminal no. 56 and Thermal Pad)
58	DOUT2	O	IOVDD2	Primary: Audio Serial Data Bus 2 Data Output Secondary: See Table 47

Terminal Functions – 64 Terminal QFN (RGC) Package (continued)

QFN (RGC) TERMINAL NUMBER	NAME	I,O,IO,P	POWER DOMAIN	DESCRIPTION
59	BCLK2	IO	IOVDD2	Primary: Audio Serial Bus 2 Bit Clock Secondary: See Table 47
60	GPIO4	IO	IOVDD2	Multi Function Digital IO 4 See Table 47
61	DVDD_18	P	Digital	1.8V Digital Power Supply (Not internally connected to terminal no. 55)
62	IOVDD2_33	P	IOVDD2	Digital IO Buffer Supply 2
63	DIN2	I	IOVDD2	Primary: Audio Serial Data Bus 2 Data Input Secondary: See Table 47
64	WCLK2	IO	IOVDD2	Primary: Audio Serial Data Bus 2 Word Clock Secondary: See Table 47
THERMAL PAD	VSS	P	Ground	Internal Device Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 to VSS respectively(2)		–0.3 to 2.2	V
RECVDD_33 to VSS		–0.3 to 3.9	V
DVDD_18 to VSS		–0.3 to 2.2	V
IOVDD1_33, IOVDD2_33 to VSS		–0.3 to 3.9	V
HVDD_18 to VSS		–0.3 to 2.2	V
CPVDD_18 to VSS		–0.3 to 2.2	V
SVDD, SPK_V, MICBIAS_VDD to VSS(3)		–0.3 to 6.0	V
Digital Input voltage to VSS		VSS – 0.3 to IOVDDx + 0.3	V
Analog input voltage to VSS		VSS – 0.3 to AVDDx_18 + 0.3	V
VBAT to VSS		–0.3 to 6	V
Junction temperature (T_J Max)		115	°C
QFN-64 package (RGC)	Power dissipation	(T_J Max – T_A) / θ_{JA}	W

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) It's recommended to keep all AVDDx_18 supplies within ±50 mV of each other.
(3) It's recommended to keep SVDD and SPK_V supplies within ±50 mV of each other.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–55	125	°C
ESD	HBM		2000	V
	CDM		500	

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18	Power Supply Voltage Range	Referenced to VSS respectively(1) It is recommended to connect each of these supplies to a single supply rail.	1.5(2)	1.8	1.95	V
RECVDD_33		Referenced to VSS	1.65(3)	3.3	3.6	
IOVDD1_33, IOVDD2_33		Referenced to VSS	1.1		3.6	
DVDD_18	Power Supply Voltage Range	Referenced to VSS	1.26(4)	1.8	1.95	
CPVDD_18	Power Supply Voltage Range	Referenced to VSS	1.26	1.8	1.95	V
HVDD_18		Referenced to VSS	1.5(3)	1.8	1.95	
SVDD(1)	Power Supply Voltage Range	Referenced to VSS(1)	2.7		5.5	V
SPK_V(1)	Power Supply Voltage Range	Referenced to VSS(1)	2.7		5.5	V
MICBIAS_VDD	Power Supply Voltage Range	Referenced to VSS	2.7		5.5	V
VREF_SAR	External voltage reference for SAR	Referenced to VSS		1.8	AVDDx_18	V

(1) AVDDx_18 are within ±0.05 V of each other. SVDD and SPK_V are within ±0.05 V of each other.
(2) For optimal performance with CM=0.9V, min AVDDx_18 = 1.8V.
(3) Minimum voltage for HVDD_18 and RECVDD_33 should be greater than or equal to AVDDx_18.
(4) At DVDD_18 values lower than 1.65V, the PLL and SAR ADC do not function.

Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
	PLL Input Frequency(5)	Clock divider uses fractional divide (D > 0), P=1, PLL_CLKIN_DIV=1, DVDD_18 ≥ 1.65V	10		20	MHz
		Clock divider uses integer divide (D = 0), P=1, PLL_CLKIN_DIV=1, DVDD_18 ≥ 1.65V	0.512		20	MHz
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; IOVDD1_33 ≥ 1.65V			50	MHz
		MCLK; Master Clock Frequency; IOVDD1_33 ≥ 1.1V			33	
SCL	SCL Clock Frequency				400	kHz
LOL, LOR	Stereo line output load resistance		0.6	10		kΩ
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω
SPKP-SPKM	Speaker output load resistance	Differential	7.2	8		Ω
RECP-RECM	Receiver output resistance	Differential	24.4	32		Ω
C_{IN}	Charge pump input capacitor (CPVDD to CPVSS terminals)			10		µF
C_O	Charge pump output capacitor (VNEG terminal)	Type X7R		2.2		µF
C_F	Charge pump flying capacitor (CPFCP to CPFCM terminals)	Type X7R		2.2		µF
TOPR	Operating Temperature Range		–40		85	°C

(5) The PLL Input Frequency refers to clock frequency after PLL_CLKIN_DIV divider. Frequencies higher than 20MHz can be sent as an input to this PLL_CLKIN_DIV and reduced in frequency prior to input to the PLL.

7.4 Thermal Information

THERMAL METRIC(1)		TLV320AIC3268 RGC TERMINALS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	19.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	5.3	
θ_{JB}	Junction-to-board thermal resistance(4)	2.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	2.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics, SAR ADC

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAR ADC Inputs						
Analog Input	Input voltage range	IN1L/AUX1 or IN1R/AUX2 Selected	0		VREF_SAR	V
	Input capacitance, C_{SAR_IN}			25		pF
	Input leakage current			1		µA
Battery Input	VBAT Input voltage range	VBAT (Battery measurement) selected(1)	2.2		5.5	V
	VBAT Input impedance			5		kΩ
	VBAT Input leakage current	VBAT (Battery measurement) not selected		1		µA
SAR ADC Conversion						
	Resolution	Programmable: 8-bit, 10-bit, 12-bit	8		12	Bits
12-bit	Integral Linearity	IN1L/AUX1 routed to SAR ADC, 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion Clock = Internal Oscillator / 4, External Reference = 1.8V(2)		±0.7		LSB
	Differential Linearity			±0.7		LSB
	Offset error			0.7		LSB
	Gain error			±0.01		%
12-bit	Integral Linearity	IN1L/AUX1 routed to SAR ADC, 12-bit resolution, SAR ADC clock = 12MHz External Clock, Conversion Clock = External Clock / 4, External Reference = 1.8V(2)		±0.7		LSB
	Differential Linearity			±0.7		LSB
	Offset error			0.5		LSB
	Gain error			-0.01		%
8-bit	Integral Linearity	IN1L/AUX1 routed to SAR ADC, 8-bit resolution, SAR ADC clock = 12MHz External Clock, Conversion Clock = External Clock, External Reference = 1.8V(2)		±0.04		LSB
	Differential Linearity			±0.04		LSB
	Offset error			±0.5		LSB
	Gain error			0.2		%
Battery Measurement	Accuracy	VBAT is routed to SAR ADC, 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion Clock = Internal Oscillator / 4, Internal Reference = 1.25V		-1		%
	Offset error			±2.1		LSB
	Gain error			-0.8		%
Voltage Reference - VREF_SAR						
	Voltage range	Internal VREF_SAR		1.25±0.05		V
		External VREF_SAR	1.25		AVDDx_18	V
	Decoupling Capacitor		1			µF

(1) When VBAT is not being sampled/converted. When VBAT is being sampled, effective input impedance to GND is 5.24kΩ.
(2) When utilizing External SAR reference, this external reference should be restricted $V_{EXT\_SAR\_REF} \leq$ AVDD_18 and AVDD2_18.

7.6 Electrical Characteristics, ADC

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC (Single Ended)					
Input signal level (0dB)	CM = 0.9V		0.5		V_{RMS}
	CM = 0.75V		0.375		
Device Setup	1kHz sine wave input, Single-ended Configuration IN2R to Right ADC and IN2L to Left ADC, R_{in} = 20kΩ, f_s = 48kHz, AOSR = 128, MCLK = 256*f_s, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				

Electrical Characteristics, ADC (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio, A-weighted (1) (2)	Inputs ac-shorted to ground	85	94		dB
		IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac-shorted to ground IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac-shorted to ground		94		
		IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac-shorted to ground IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac-shorted to ground CM=0.75V, AVDD_18,AVDDx_18=1.5V		92		
DR	Dynamic range A-weighted (1) (2)	IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC –60dBr full-scale input		94		dB
		IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC –60dBr full-scale input, CM=0.75V, AVDD_18,AVDDx_18=1.5V		92		
THD+N	Total Harmonic Distortion plus Noise	–3 dBr full-scale signal		-88	-75	dB
		IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC –3dBr full-scale signal		-88		
		IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC –3dBr full-scale signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		-85		
	Gain Error	IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC -3dBr full-scale signal		±0.1		dB
		IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC -3dBr full-scale signal, CM=0.75V, AVDD_18, AVDDx_18=1.5V		-0.1		
	Output Offset	IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac shorted to ground IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac shorted to ground		-1518		LSB
		IN1R, IN2R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac shorted to ground IN1L, IN2L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac shorted to ground CM=0.75V, AVDD_18, AVDDx_18=1.5V		-1766		
	Inter Channel Gain Error Mismatch	-3dBr full scale signal		± 0.1		dB

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with pre-analyzer 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, ADC (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Inrter Channel Separation	-3dBr full scale signal		110		dB
	Input Terminal Crosstalk	-3dBr full scale signal on IN2L and IN2R, IN2L and IN2R not internally routed. IN1L routed to Left ADC and ac-coupled to ground, IN1R routed to Right ADC and ac-coupled to ground		104		dB
PSRR	Power Supply Rejection Ratio	217Hz, 100mVpp signal on AVDD_18, AVDDx_18, HPVDD_18, CPVDD_18, IOVDDx_18, DVDD_18		59		dB
		1kHz, 100mVpp signal on AVDD_18, AVDDx_18, HPVDD_18, CPVDD_18, IOVDDx_18, DVDD_18		59		
	ADC Analog Programmable Gain Amplifier, Gain Range	IN1L, IN1R, IN2L, IN2R, IN3L, IN3R inputs, R_{in}=10kΩ	0		47.5	dB
		All Inputs, Rin=20K	-6		41.5	
		IN1L, IN1R, IN2L, IN2R, IN3L, IN3R inputs, R_{in}=40kΩ	-12		35.5	
	ADC Analog Programmable Gain Amplifier, Gain Step Size			0.5		dB
AUDIO ADC (Differential)						
	Input signal level (0dB)	CM=0.9V		1.0		V_{RMS}
		CM=0.75V		0.75		
	Device Setup	1kHz sine wave input, Differential Configuration IN1L, IN1R routed to Right ADC and IN2L, IN2R routed to Left ADC R_{in} = 20kΩ, f_s = 48kHz, CM=0.9V AOSR = 128, MCLK = 256*f_s, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted (3) (4)	Inputs ac-shorted to ground	87	95		dB
		Inputs ac-shorted to ground, CM=0.75V, AVDD_18, AVDDx_18=1.5V		92		
DR	Dynamic range A-weighted (3) (4)	–60dBr full scale signal		95		dB
		–60dBr full scale signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		92		
THD+N	Total Harmonic Distortion plus Noise	–3dBr full scale		–89	-76	dB
		–3dBr full scale, CM=0.75V, AVDD_18, AVDDx_18=1.5V		-85		
	Gain Error	–3dBr full scale		±0.02		dB
		–3dBr full scale, CM=0.75V, AVDD_18, AVDDx_18=1.5V		±0.1		
	Inter Channel Gain Error Mismatch	–3dBr full scale		0.1		dB
		–3dBr full scale, CM=0.75V, AVDD_18, AVDDx_18=1.5V		0.2		
	Output Offset	Inputs ac-shorted to ground		-2053		LSB
		Inputs ac-shorted to ground, CM=0.75V, AVDD_18, AVDDx_18=1.5V		-2198		
	Inter Channel Seperation	-3dBr full scale signal		111		dB
	Input Terminal Crosstalk	-3dBr input on IN2L, IN2R. IN2L, IN2R internally not routed.IN1L, IN1R differentially routed to Right ADC ac-shorted to ground. -3dBr on IN2L, IN2R. IN2L,IN2R internally not routed.IN3L, IN3R differentially routed to Left ADC ac-shorted to ground.		117		dB
PSRR	Power Supply Rejection Ratio	217Hz, 100mVpp signal on AVDD_18, AVDDx_18, HPVDD_18, CPVDD_18, IOVDDx_18, DVDD_18		53		dB
		1kHz, 100mVpp signal on AVDD_18, AVDDx_18, HPVDD_18, CPVDD_18, IOVDDx_18, DVDD_18		53		

(3) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(4) All performance measurements done with pre-analyzer 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, ADC (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common Mode Rejection Ratio	IN1L, IN1R shorted together and routed to Right ADC. IN2L, IN2R shorted together and routed to Left ADC. 350mVrms signal on shorted pairs		68		dB
	ADC Analog Programmable Gain Amplifier, Gain Range	All Inputs, R_{in}=10kΩ	6		53.5	dB
		All Inputs, R_{in}=20kΩ	0		47.5	
		All Inputs, R_{in}=40kΩ	-6		41.5	
	ADC Analog Programmable Gain Amplifier, Gain Step Size			0.5		dB

7.7 Electrical Characteristics, Bypass Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO RECEIVER AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 32Ω (differential), 56pF Output CM=1.65V IN1L routed to RECP and IN1R routed to RECM Channel Gain=0dB, 1kHz input signal				
	Full scale differential input voltage (0dBr)			1		V_{RMS}
	Voltage Gain			1		V/V
	Gain Error	-3dBr input signal		–0.6		dB
	Noise, A-weighted(1)	IN1L and IN1R ac-shorted to ground		12		$µV_{RMS}$
THD+N	Total Harmonic Distortion plus Noise	-3dBr input signal		-90		dB
ANALOG BYPASS TO HEADPHONE AMPLIFIER (GROUND-CENTERED CIRCUIT CONFIGURATION), PGA MODE						
	Device Setup	Load = 16Ω (single-ended), 1nF IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to HPL and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to HPR R_{in} = 20K, Channel Gain = 0dB				
	Full scale input voltage (0dBr)			0.5		V_{RMS}
	Voltage Gain			1		V/V
	Gain Error	-3dBr input signal		-0.8		dB
	Noise, A-weighted(1)	IN1L and IN1R ac-shorted to ground		10.3		$µV_{RMS}$
THD+N	Total Harmonic Distortion plus Noise	-3dBr input signal		-71		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE						
	Device Setup	Load = 10KΩ (single-ended), 56pF Output CM=0.9V IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to LOL and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to LOR R_{in} = 20K, Channel Gain = 0dB				
	Full scale input voltage (0dBr)			0.5		V_{RMS}

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Bypass Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Voltage Gain			1		V/V
	Gain Error	-1dBr input signal		–0.9		dB
	Noise, A-weighted (2)	IN1L and IN1R ac-shorted to ground		6		μV_{RMS}
THD+N	Total Harmonic Distortion plus Noise	-3dBr input signal		-87		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 10KΩ (single-ended), 56pF Output CM=0.9V IN1L routed to LOL and IN1R routed to LOR Channel Gain = 0dB				
	Full scale input voltage (0dBr)			0.5		V_{RMS}
	Voltage Gain			1		V/V
	Gain Error	-3dBr input signal		-0.4		dB
	Noise, A-weighted(2)	IN1L and IN1R ac-shorted to ground		3		μV_{RMS}
THD+N	Total Harmonic Distortion plus Noise	-3dBr input signal		-95		dB

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

7.8 Electrical Characteristics, Microphone Interface

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS (MICBIAS or MICBIAS_EXT)					
Bias voltage	Micbias Mode 0, No Load Current		1.8		V
	Micbias Mode 1, Load Current = 8mA	1.85	2.0	2.15	V
	Micbias Mode 4, No Load Current(1)		2.9		V
	Micbias Mode 5, No Load Current(1)		3.0		V
	Micbias Mode 0, No Load Current, CM=0.75V, AVDD_18, AVDDx_18=1.5V		1.50		V
	Micbias Mode 1, No Load Current, CM=0.75V, AVDD_18, AVDDx_18=1.5V		1.7		V
	Micbias Mode 4, No Load Current, CM=0.75V, AVDD_18, AVDDx_18=1.5V		2.4		V
	Micbias Mode 5, No Load Current, CM=0.75V, AVDD_18, AVDDx_18=1.5V		2.5		V
Output Noise	Micbias Mode 1, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		6.4		μV_{RMS}
Current Sourcing	Micbias Mode 0, 1, 4, or 5		8		mA

(1) With Common Mode voltage of 0.9V, the MICBIAS_VDD voltage must be at minimum 3.05V to utilize Micbias Mode 4, and minimum of 3.2V to utilize Micbias Mode 5. With Common Mode voltage of 0.75V, the corresponding MICBIAS_VDD voltage must be minimum of 2.65V and 2.75V respectively.

Electrical Characteristics, Microphone Interface (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR Power Supply Rejection Ratio(2)	217Hz, 100mV$_{pp}$ signal on AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33, Micbias Mode 1		51		dB
	217Hz, 100mVpp signal on MICBIAS_VDD, CM=0.9V, Micbias Mode 1		93		dB
	1kHz, 100mVpp signal on AVDDx_18, DVDD_18, IOVDDx, CM=0.9V, Micbias Mode 1		51		dB
	1kHz, 100mVpp signal on MICBIAS_VDD, CM=0.9V, Micbias Mode 1		88		dB

(2) PSRR is specified as 20*log$_{10}$(V_{sup}/V_{out}), where Vsup is the signal applied on the power supply and V_{out} is the measured analog output. For ADC, V_{out} is given as equivalent analog input signal which produces the same level of digital output signal.

7.9 Electrical Characteristics, Audio DAC Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10kΩ (single-ended), 56pF CM=0.9V DOSR = 128, MCLK=256* f_s Channel Gain = 0dB Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dBr)			0.5		V_{RMS}
		CM = 0.75V, AVDD_18, AVDDx_18 = 1.5V		0.375		
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	88	102		dB
		All zeros fed to DAC input, CM=0.75V, AVDD_18,AVDDx_18=1.5V		99		
DR	Dynamic range, A-weighted (1) (2)	–60dBFS input signal		102		dB
		–60dBFS input signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		99		
THD+N	Total Harmonic Distortion plus Noise	–3dBFS input signal		–93	-72	dB
		–3dBFS input signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		-91		
	DAC Gain Error	–3dBFS input signal		±0.01		dB
		–3dBFS input signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		0.1		
	Inter Channel Gain Mismatch	–3dBFS input signal		± 0.0		dB
		–3dBFS input signal, CM=0.75V, AVDD_18,AVDDx_18=1.5V		±0.0		
	DAC Mute Attenuation	Digital Volume Control is Muted		126		dB
	DAC channel separation	–3dBFS, 1kHz signal, between left and right Line out		114		dB

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power Supply Rejection Ratio(3)	217Hz, 100mVpp signal applied to AVDD_18, AVDDx_18, HVDD_18,CPVDD_18,IOVDDx_33,DVDD_18		74		dB
		1kHz, 100mVpp signal applied to AVDD_18, AVDDx_18,HVDD_18,CPVDD_18,IOVDDx_33,DVDD_18		73		dB
R_L	Output Resistive Load(4)	Resistance to ground	9	10		kΩ
AUDIO DAC – STEREO DIFFERENTIAL LINE OUTPUT						
	Device Setup	Load = 10kΩ (differential), 56pF between RECP,RECMM and LOL,LOR Left DAC routed directly to RECP,RECM, Right DAC routed to LOL,LOR Output CM=0.9V DOSR = 128, MCLK=256* f_S Channel Gain = 0dB Processing Block = PRB_P1, Power Tune = PTM_P4 RECVDD_33, AVDD_18, AVDDx_18=1.8V				
	Full scale output voltage (0dBr)			1		V_{RMS}
		CM = 0.75V, AVDD_18, AVDDx_18, RECVDD_33=1.5V		0.75		
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	92	105		dB
		All zeros fed to DAC input, CM=0.75V, AVDD_18, AVDDx_18, RECVDD_33=1.5V		103		
DR	Dynamic range, A-weighted (5) (6)	–60dBFS input signal		105		dB
		–60dBFS input full-scale signal, CM=0.75V, AVDD_18, AVDDx_18, RECVDD_33=1.5V		102		
THD+N	Total Harmonic Distortion plus Noise	–3dBFS input signal		-94	-75	dB
		–3dBFS input signal, CM=0.75V, AVDD_18, AVDDx_18, RECVDD_33=1.5V		-92		
	DAC Gain Error	–3dBFS input signal		±0.03		dB
		–3dBFS input signal, CM=0.75V, AVDD_18, AVDDx_18, RECVDD_33=1.5V		±0.04		
	Inter Channel Gain Mismatch	-3dBFS input signal		0.0		dB
	Output Offset	All zero's fed to DAC Input		±0.5		mV
		All zero's fed to DAC Input, CM=0.75V AVDD_18, AVDDx_18, RECVDD_33=1.5V		±0.4		
	DAC Mute Attenuation	Digital Volume Control is Muted		126		dB
PSRR	Power Supply Rejection Ratio(7)	217kHz, 100mVpp signal applied to AVDD_18, AVDDx_18, RECVDD_33, HVDD_18, CPVDD_18, IOVDDx_33, DVDD_18		93		dB
		1kHz, 100mVpp signal applied to AVDD_18, AVDDx_18, RECVDD_33, HVDD_18, CPVDD_18, IOVDDx_33, DVDD_18		92		dB

(3) PSRR is specified as $20*\log_{10}(V_{sup}/V_{out})$, where Vsup is the signal applied on the power supply and V_{out} is the measured analog output. For ADC, V_{out} is given as equivalent analog input signal which produces the same level of digital output signal.
(4) Minimum resistive load and Maximum capacitive load are specified by design.
(5) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(6) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(7) PSRR is specified as $20*\log_{10}(V_{sup}/V_{out})$, where Vsup is the signal applied on the power supply and V_{out} is the measured analog output. For ADC, V_{out} is given as equivalent analog input signal which produces the same level of digital output signal.

Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Output Resistive Load (8)	Resistance between LOL , LOR and RECP, RECM	9	10		kΩ
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (GROUND-CENTERED CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 1nF DOSR = 128, MCLK=256* f_S Channel Gain = 0dB Processing Block = PRB_P1, Power Tune = PTM_P3 Headphone Output Strength=100%				
	Full-scale Output voltage (0dBr)			0.5		V_{RMS}
		CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (9) (10)	All zeros fed to DAC input	88	94		dB
		All zeros fed to DAC input CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		93		dB
DR	Dynamic range, A-weighted (9) (10)	–60dBFS input signal		95		dB
		–60dBFS input signal CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		94		dB
THD+N	Total Harmonic Distortion plus Noise	–3dBFS input signal		-69	-60	dB
		–3dBFS input signal CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		-71		dB
	DAC Gain Error	–3dBFS input signal		±0.1		dB
		–3dBFS input signal CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		0.2		dB
	Inter Channel Gain Mismatch	–3dBFS input signal		±0.1		dB
		–3dBFS input signal CM=0.75V, AVDD_18,AVDDx_18,HVDD_18,CPVDD_18=1.5V		±0.1		dB
	DAC Mute Attenuation	Analog Volume Control is Muted		139		dB
	DAC channel separation	Between HPL, HPR at –3dBFS input signal		80		dB
	Output Offset	All zeros fed to DAC		±0.1		mV
PSRR	Power Supply Rejection Ration (11)	217Hz, 100mVpp signal applied to AVDD_18,AVDDx_18,HVDD_18,CPVDD_18,IOVDDx_33,DVDD_18		67		dB
		1kHz, 100mVpp signal applied to AVDD_18,AVDDx_18,HVDD_18,CPVDD_18,IOVDDx_33,DVDD_18		70		dB
	Power Delivered	THD+N=0.1%		17		mW
		THD+N=1%, Headphone Gain=5dB		24		mW
		THD+N=0.1%, R_L=32Ω		8		mW
		THD+N=1%, Headphone Gain=5dB, R_L=32Ω		21		mW

(8) Minimum resistive load and Maximum capacitive load are specified by design.
(9) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(10) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(11) PSRR is specified as $20*\log_{10}(V_{sup}/V_{out})$, where Vsup is the signal applied on the power supply and V_{out} is the measured analog output. For ADC, V_{out} is given as equivalent analog input signal which produces the same level of digital output signal.

Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Output Load(12)	Resistive Load to ground	14.4	16		Ω
AUDIO DAC – MONO DIFFERENTIAL RECEIVER OUTPUT						
	Device Setup	Load = 32Ω (differential), 56pF Output CM=1.65V DOSR = 128, MCLK=256* f_s Left DAC routed to RECP, RECM, Channel (Receiver Driver) Gain = 6dB for full scale output signal Processing Block = PRB_P4, Power Tune = PTM_P4				
	Full scale output voltage (0dBr)			2		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(13) (14)	All zeros fed to DAC input	90	102		dB
DR	Dynamic range, A-weighted (13) (14)	–60dBFS input signal		103		dB
THD+N	Total Harmonic Distortion plus Noise	–3dBFS input signal		-91	-70	dB
PSRR	Power Supply Rejection Ratio(11)	217Hz, 100mVpp signal applied to AVDD_18, AVDD1x_18,HVDD_18, CPVDD_18,IOVDDx_33,DVDD_18		62		dB
		1kHz, 100mVpp 217Hz signal applied to AVDD_18, AVDD1x_18,HVDD_18, CPVDD_18,IOVDDx_33,DVDD_18		59		
		1kHz, 100mVpp signal applied on RECVDD_33		89		
	Output Offset	All zero's fed to DAC, Offset Correction Enabled		±0.5		mV
	Power Delivered	THD+N ≤ 0.1%		72		mW
		THD+N ≤ 1%		121 mW		

(12) Minimum resistive load and Maximum capacitive load are specified by design.
(13) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(14) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

7.10 Electrical Characteristics, Class-D Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8Ω (Differential), 33µH					
Device Setup	BTL Load = 8Ω, 33µH between SPKP and SPKM Lineout routed to Class-D PRB_P1, PTM_P4, DOSR=128, MCLK=256*FS				
Output voltage	0dBFS input signal, Class-D gain=12dB, THD+N ≤ –20dB		2.7		V_{RMS}
	SVDD=5.0V 0dBFS input signal, Class-D gain=12dB, THD+N ≤ –20dB		3.5		
Idle Channel Noise	Class-D gain=6dB(1)		45	140	μV_{RMS}
	SVDD=5.0V Class-D gain=6dB(1)		46		

(1) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Class-D Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion + noise	-3dBFS input signal, Class-D gain=6dB			-68		dB
	Output Offset	All zero's fed to DAC, Class-D gain=6dB			±12.1		mV
PSRR	Power-supply rejection ratio(2)	217Hz, 200 mVp-p signal on SVDD, Class-D gain=6dB			64		dB
		1kHz, 200 mVp-p signal on SVDD, Class-D gain=6dB			64		dB
	Mute attenuation	Analog Mute Only			104		dB
P_O	Maximum output power	THD+N = 1%, f = 1 kHz, Class-D gain = 12 dB	SVDD = 3.6 V		0.65		W
			SVDD = 4.2 V		0.81		
			SVDD = 5.0 V		1.15		
		THD+N = 10%, f = 1 kHz, Class-D gain = 12 dB	SVDD = 3.6 V		0.74		
			SVDD = 4.2 V		1.02		
			SVDD = 5.0 V		1.45		
	Over Temperature Protection Trip Point(3)				>104		C
	Over Temperature Protection Hysterisis(3)				20		C
	Over Current Trip Threshold(4)				>850		mA

(2) PSRR is specified as 20*$\log_{10}(V_{sup}/V_{out})$, where Vsup is the signal applied on the power supply and V_{out} is the measured analog output. For ADC, V_{out} is given as equivalent analog input signal which produces the same level of digital output signal.
(3) Over Temperature and Over Current Protection parameters are indicative values from design. Over Temperature trip point can be very heavily influenced by thermal properties of the actual PCB.
(4) Over Temperature and Over Current Protection parameters are indicative values from design. Over Temperature trip point can be very heavily influenced by thermal properties of the actual PCB.

7.11 Electrical Characteristics, Misc.

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE - VREF_AUDIO					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Decoupling Capacitor			1		µF
Bias Current	Reference forcefully powered on.		101		µA
miniDSP					
miniDSP clock frequency - ADC	DVDD_18 = 1.26V			37.5	MHz
	DVDD_18 = 1.65V			63	
	DVDD_18 = 1.71V			69	
miniDSP clock frequency - DAC	DVDD_18 = 1.26V			35.0	MHz
	DVDD_18 = 1.65V			59.0	
	DVDD_18 = 1.71V			62.5	
Shutdown Power					
Device Setup	Coarse AVdd supply turned off, All External analog supplies powered and set available, No external digital input is toggled, register values are retained.				

Electrical Characteristics, Misc. (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P(total)	Sum of all supply currents, all supplies at 1.8 V except for SVDD = SPK_V = MICBIAS_VDD = 3.6 V and RECVDD_33 = 3.3 V		1.4		µW
I(DVDD_18)			0.02		µA
I(IOVDD1_33, IOVDD2_33)			0.17		µA
I(AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18, HVDD_18, CPVDD_18)			0.13		µA
I(RECVDD_33)			0.01		µA
I(SVDD, SPK_V, MICBIAS_VDD)			0.22		µA
Active Power					
Device Setup	f_S=48ksps, PLL disabled, Device is I^2S slave, Stereo ADC record, AGC disabled PTM_R4,PRB_P1				
I(DVDD_18)			4		mA
I(IOVDD1_18,IOVDD2_18)			28		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			6.9		mA
I(RECVDD_33)			0		µA
I(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA
Device Setup	f_S=8ksps, PLL disabled, Device is I2S slave, Stereo ADC record, AGC disabled PTM_R4,PRB_P1				
I(DVDD_18)			0.9		mA
I(IOVDD1_18,IOVDD2_18)			5		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			6.7		mA
I(RECVDD_33)			0		µA
I(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA
Device Setup	f_S=48ksps, PLL disabled; Device is I2S slave Stereo DAC Playback on Stereo Single-ended Lineout; PTM_P4; PRB_P1; All zeros on I2S input; DAC Modualtor excited; Input CM=0.9V				
I(DVDD_18)			4.8		mA
I(IOVDD1_18,IOVDD2_18)			6		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			1.9		mA
I(RECVDD_33)			0		µA
(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA
Device Setup	f_S=48ksps, PLL disabled; Device is I2S slave Stereo DAC Playback on Stereo Differential Lineout; PTM_P4; PRB_P1; All zeros on I2S input; DAC Modualtor excited; Input CM=0.9V				
I(DVDD_18)			5.3		mA

Electrical Characteristics, Misc. (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(IOVDD1_18,IOVDD2_18)			7		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			2.3		mA
I(RECVDD_33)			2		mA
I(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA
Device Setup	f_S=48ksps, PLL disabled; Device is I2S slave Stereo DAC Playback on Headphones (Ground Centered Mode); PTM_P4; PRB_P1; All zeros on I2S input; DAC Modualtor excited; Input CM=0.9V				
I(DVDD_18)			5.2		mA
I(IOVDD1_18,IOVDD2_18)			6		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			6.4		mA
I(RECVDD_33)			0		µA
I(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA
Device Setup	f_S=48ksps, PLL disabled; Device is I2S slave Mono DAC Playback on Speaker Amp ; PTM_P4; PRB_P1; All zeros on I2S input; DAC Modualtor excited; Input CM=0.9V				
I(DVDD_18)			3.3		mA
I(IOVDD1_18,IOVDD2_18)			5		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			1.9		mA
I(RECVDD_33)			0		µA
I(SVDD, SPK_V,MICBIAS_VDD)			6.7		mA
Device Setup	f_S=48ksps, PLL disabled; Device is I2S slave Mono DAC Playback on Receiver Amp ; PTM_P4; PRB_P1; All zeros on I2S input; DAC Modualtor excited; Input CM=0.9V, Receiver Amp Output CM=1.65V				
I(DVDD_18)			3.1		mA
I(IOVDD1_18,IOVDD2_18)			6		µA
I(AVDD1_18, AVDD2_18, AVDD4_18,AVDD_18, HVDD_18, CPVDD_18)			1.4		mA
I(RECVDD_33)			2.3		mA
I(SVDD, SPK_V,MICBIAS_VDD)			0.2		µA

7.12 Electrical Characteristics, Logic Levels, IOVDDx

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital IO (When SPI_SELECT = '1', all terminals, When SPI_SELECT = '0', all terminals except SCL, SDA)						
LOGIC FAMILY				**CMOS**		
V_{IH}	Logic Level	I_{IH} = 5 µA, IOVDDx_33 > 1.65V	0.7 × IOVDDx_33			V
		I_{IH} = 5µA, 1.2V ≤ IOVDDx_33 <1.65V	0.9 × IOVDDx_33			V
		I_{IH} = 5µA, IOVDDx_33 < 1.2V	IOVDDx_33			V
V_{IL}		I_{IL} = 5 µA, IOVDDx_33 > 1.65V	–0.3		0.3 × IOVDDx_33	V
		I_{IL} = 5µA, 1.2V ≤ IOVDDx_33 <1.65V			0.1 × IOVDDx_33	V
		I_{IL} = 5µA, IOVDDx_33 < 1.2V			0	V
V_{OH}		I_{OH} = 3mA load, IOVDDx_33 > 1.65V	0.8 × IOVDDx_33			V
		I_{OH} = 1mA load, IOVDDx_33 < 1.65V	0.8 × IOVDDx_33			V
V_{OL}		I_{OL} = 3mA load, IOVDDx_33 > 1.65V			0.2 × IOVDDx_33	V
		I_{OL} = 1mA load, IOVDDx_33 < 1.65V			0.2 × IOVDDx_33	V
	Capacitive Load			10		pF
Digital IO (SCL, SDA when SPI_SELECT = '0')						
LOGIC FAMILY				**OPEN DRAIN**		
V_{IH}			0.7 × IOVDD1_33			V
V_{IL}			–0.3		0.3 × IOVDD1_33	V
V_{OL}		I_{OL} = 3mA load, IOVDD1_33 > 2V			0.4	V
		I_{OL} = 2mA load, IOVDD1_33 ≤ 2V			0.2 × IOVDD1_33	V

7.13 Interface Timing

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface 1, Audio Serial Interface 2 and Audio Serial Interface 3.

7.13.1 Typical Timing Characteristics — Audio Data Serial Interface Timing (I^2S)

WCLK represents WCLK1 terminal for Audio Serial Interface 1, WCLK2 terminal for Audio Serial Interface 2 and Word Clock for Audio Serial Interface 3. **BCLK** represents BCLK1 terminal for Audio Serial Interface 1, BCLK2 for Audio Serial Interface 2 and Bit Clock for Audio Serial Interface 3. **DOUT** represents DOUT1 terminal for Audio Serial Interface 1, DOUT2 for Audio Serial Interface 2 and Data Out for Audio Serial Interface 3. **DIN** represents DIN1 terminal for Audio Serial Interface 1, DIN2 for Audio Serial Interface 2 and Data In for Audio Serial Interface 3. Specifications are at 25° C with DVDD_18 = 1.8V.

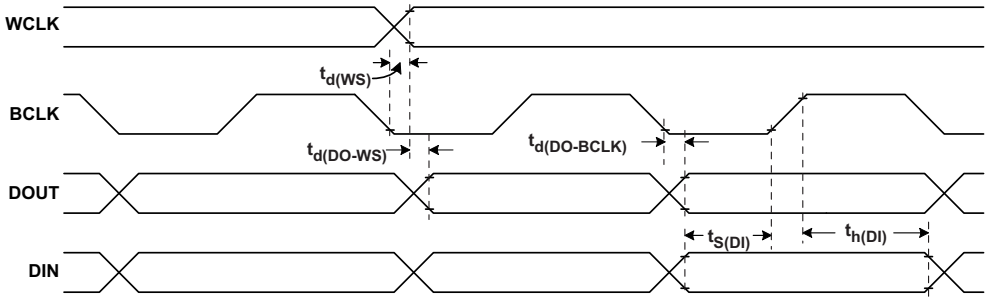


Figure 2. I^2S,LJF,RJF Timing in Master Mode

Table 1. I^2S,LJF,RJF Timing in Master Mode (see Figure 2)

PARAMETER		IOVDDx=1.8V		IOVDDx=3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		23		17	ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		28		23	ns
t_d (DO-BCLK)	BCLK to DOUT delay		25		19	ns
t_s(DI)	DIN setup	7		8		ns
t_h(DI)	DIN hold	5		5		ns
t_r	BCLK Rise time		7		5	ns
t_f	BCLK Fall time		10		6	ns

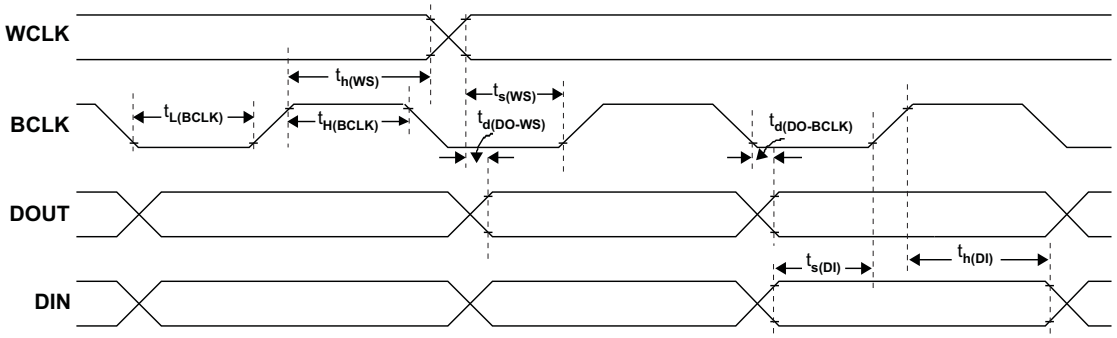


Figure 3. I^2S,LJF,RJF Timing in Slave Mode

Table 2. I^2S,LJF,RJF Timing in Slave Mode (see Figure 3)

PARAMETER		IOVDDx=1.8V		IOVDDx=3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	34		30		ns
t_L (BCLK)	BCLK low period	34		30		
t_s (WS)	WCLK setup	7		7		
t_h (WS)	WCLK hold	5		5		
t_d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		28		24	
t_d (DO-BCLK)	BCLK to DOUT delay		26		21	
t_s(DI)	DIN setup	5		5		
t_h(DI)	DIN hold	5		5		
t_r	BCLK Rise time		5		4	
t_f	BCLK Fall time		5		4	

7.13.2 Typical DSP Timing Characteristics

Specifications are at 25° C with DVDD_18 = 1.8 V.

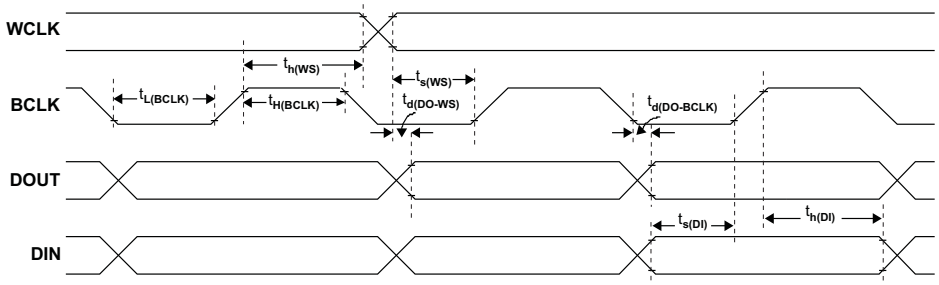


Figure 4. DSP,Mono PCM Timing in Master Mode

Table 3. DSP,Mono PCM Timing in Master Mode (see Figure 4)

PARAMETER		IOVDDx=1.8V		IOVDDx=3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay		22		17	ns
t_d (DO-BCLK)	BCLK to DOUT delay		25		19	ns
t_s(DI)	DIN setup	5		5		ns
t_h(DI)	DIN hold	5		5		ns
t_r	BCLK Rise time		7		5	ns
t_f	BCLK Fall time		10		6	ns

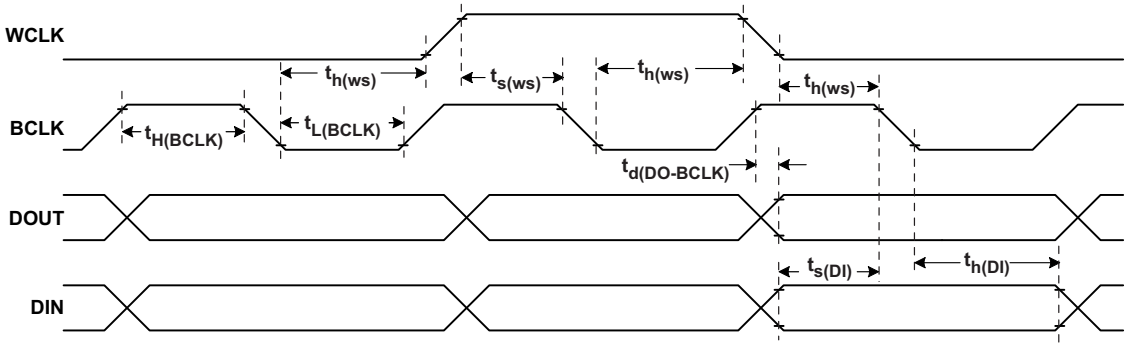


Figure 5. DSP/Mono PCM Timing in Slave Mode

Table 4. DSP,Mono PCM Timing in Slave Mode (see Figure 5)

PARAMETER		IOVDDx=1.8V		IOVDDx=3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	31		25		ns
t_L (BCLK)	BCLK low period	31		25		ns
t_s(WS)	WCLK setup	6		6		ns
t_h(WS)	WCLK hold	5		5		ns
t_d (DO-BCLK)	BCLK to DOUT delay		26		20	ns
t_s(DI)	DIN setup	5		5		ns
t_h(DI)	DIN hold	5		5		ns
t_r	BCLK Rise time		5		4	ns
t_f	BCLK Fall time		5		4	ns

7.13.3 I²C Interface Timing

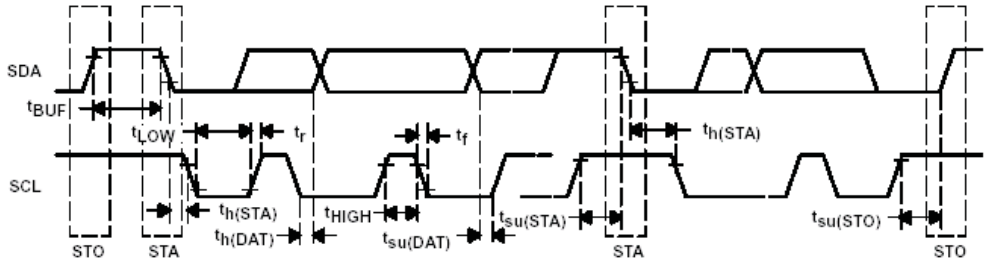


Figure 6. I²C Interface Timing Diagram

Table 5. I²C Interface Timing (see Figure 6)

PARAMETER		Standard-Mode		Fast-Mode		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0		0.8		µs
t_{LOW}	LOW period of the SCL clock	4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL clock	4.0		0.6		µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7		0.8		µs
$t_{HD;DAT}$	Data hold time: For I2C bus devices	0	3.45	0	0.9	µs
$t_{SU;DAT}$	Data set-up time	250		100		ns
t_r	SDA and SCL Rise Time		1000	$20 + 0.1C_b$	300	ns
t_f	SDA and SCL Fall Time		300	$20 + 0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.8		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

7.13.4 SPI Interface Timing

$\overline{SS}$ = SCL terminal, **SCLK** = I2C_ADDR_SCLK terminal, **MISO** = GPO1 terminal, and **MOSI** = SDA terminal. Specifications are at 25° C with DVDD_18 = 1.8V.

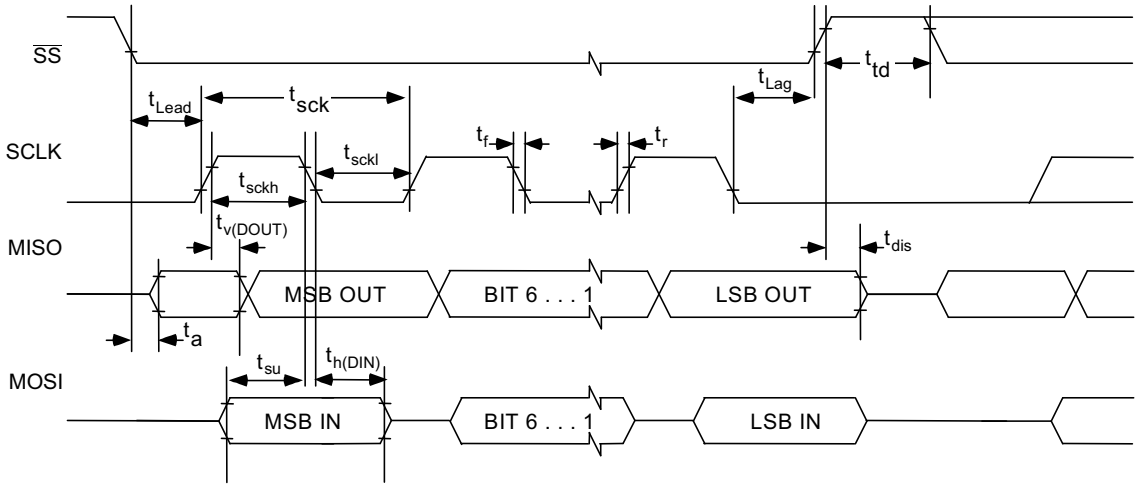


Figure 7. SPI Interface Timing Diagram

Table 6. SPI Interface Timing

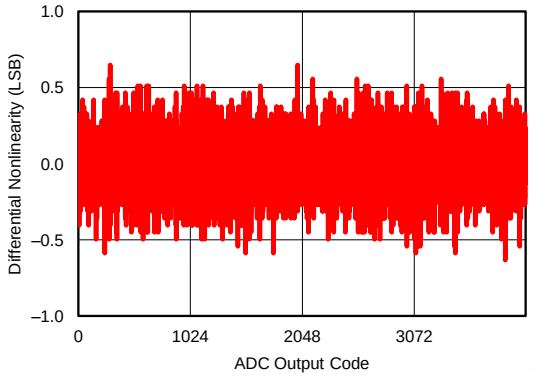
PARAMETER		IOVDD1=1.8V		IOVDD1=3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_{sck}	SCLK Period	48		40		ns
t_{sckh}	SCLK Pulse width High	24		20		ns
t_{sckl}	SCLK Pulse width Low	24		20		ns
t_{lead}	$\overline{SS}$ Lead Time	24		20		ns
t_{lag}	$\overline{SS}$ Lag Time	24		20		ns
$t_{d;seqxfr}$	Sequential Transfer Delay	20		20		ns
t_a	Slave DOUT (MISO) access time		19		13	ns
t_{dis}	Slave DOUT (MISO) disable time		20		13	ns
t_{su}	DIN (MOSI) data setup time	8		7		ns
$t_{h;DIN}$	DIN (MOSI) data hold time	9		7		ns
$t_{v;DOUT}$	DOUT (MISO) data valid time		19		15	ns
t_r	SCLK Rise Time		4		4	ns
t_f	SCLK Fall Time		4		4	ns

7.14 Typical Characteristics

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD_18, IOVDDx_33 = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO terminals; PLL disabled, Device CM = 0.9V unless otherwise noted.

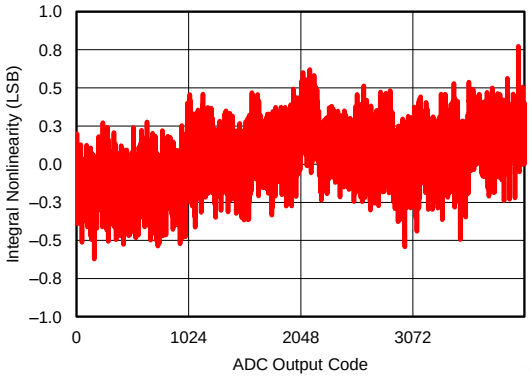
Typical Characteristics (continued)

7.14.1 SAR ADC Performance



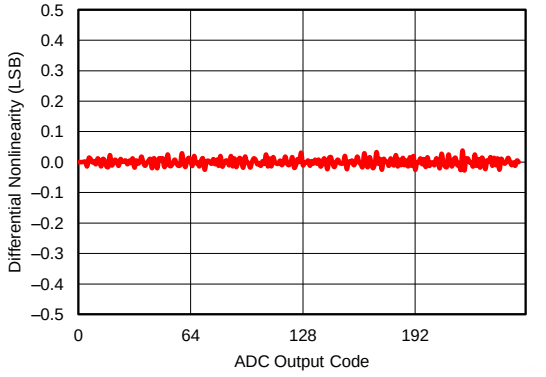
12-bit resolution
Internal Oscillator divide by 4
External Reference

Figure 8. SAR ADC, DNL versus Output Code



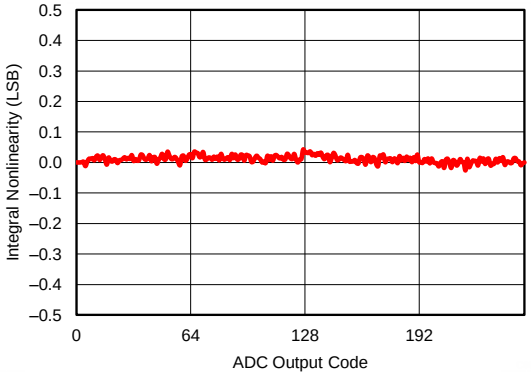
12-bit resolution
Internal Oscillator divide by 4
External Reference

Figure 9. SAR ADC, INL versus Output Code



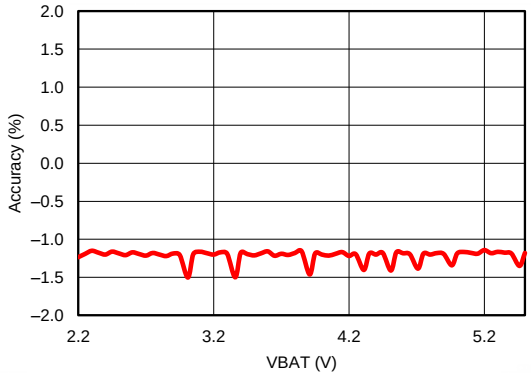
8-bit resolution
12MHz External Conversion Clock
External Reference

Figure 10. SAR ADC, DNL versus Output Code



8-bit resolution
12MHz External Conversion Clock
External Reference

Figure 11. SAR ADC, INL versus Output Code

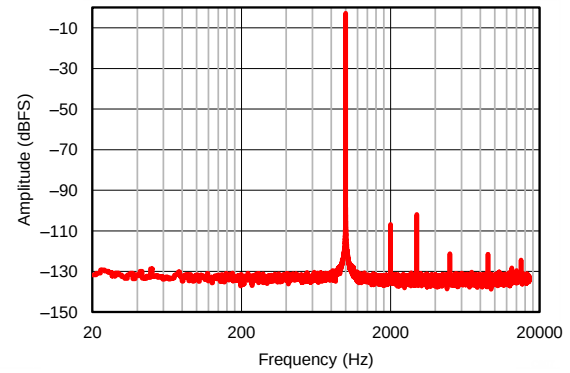


12-bit resolution
Internal Oscillator Clock Divider by 4
Interal Reference

Figure 12. Battery Measurement, Accuracy versus VBAT Input Voltage

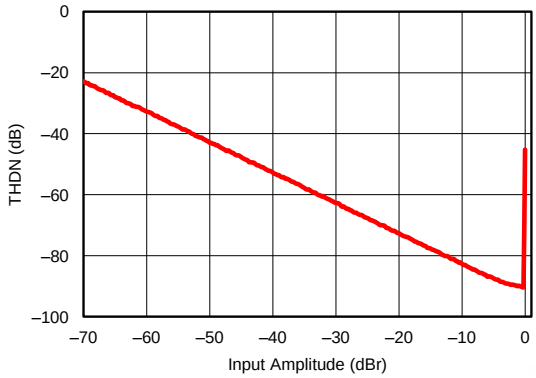
Typical Characteristics (continued)

7.14.2 Audio ADC Performance



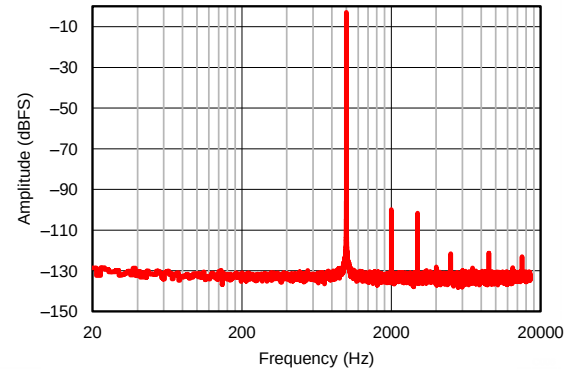
Differential Input R_{in}=20kΩ CM=0.9V
Channel Gain=0dB Input Amplitude=-3dBr

Figure 13. Audio ADC, Output Amplitude versus Frequency



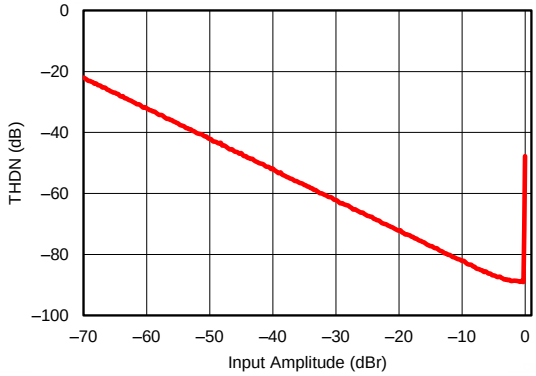
Differential Input R_{in}=20kΩ CM=0.9V
Channel Gain=0dB

Figure 14. Audio ADC, Total Harmonic Distortion + Noise versus Input Amplitude



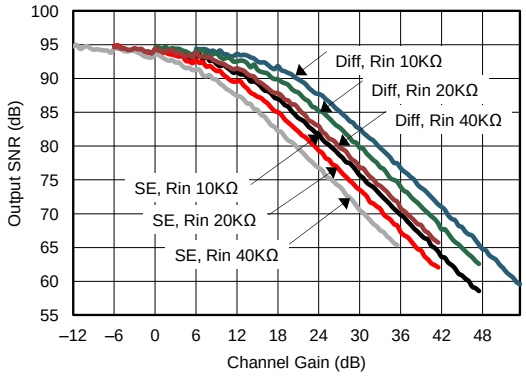
Single-ended Input R_{in}=20kΩ CM=0.9V
Channel Gain=0dB Input Amplitude=-3dBr

Figure 15. Audio ADC, Output Amplitude versus Frequency



Single-ended Input R_{in}=20kΩ CM=0.9V
Channel Gain=0dB

Figure 16. Audio ADC, Total Harmonic Distortion + Noise versus Input Amplitude

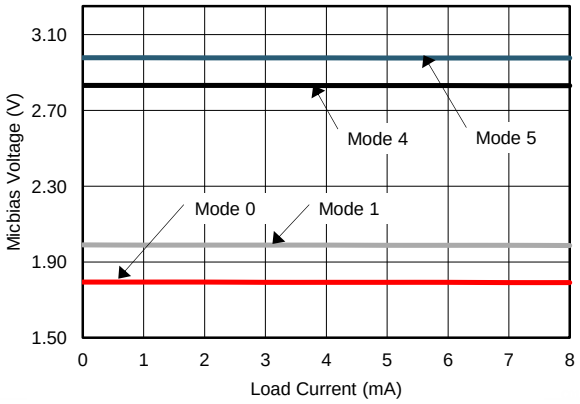


Differential and Single-ended Inputs R_{in}=10kΩ
20kΩ and 40kΩ CM=0.9V

Figure 17. Audio ADC, Output SNR versus Channel Gain (Analog)

Typical Characteristics (continued)

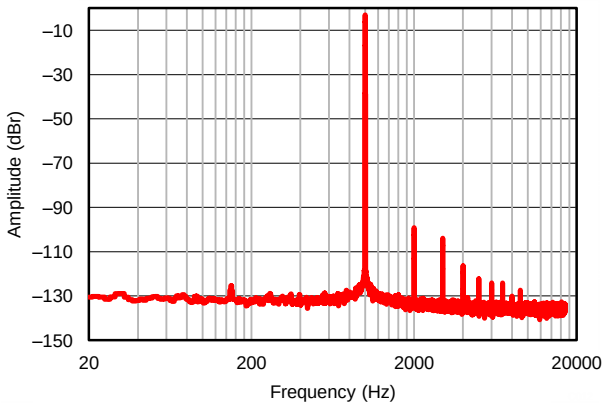
7.14.3 MICBIAS Performance



MICBIAS_VDD at 200mV above programmed output voltage
CM=0.9V

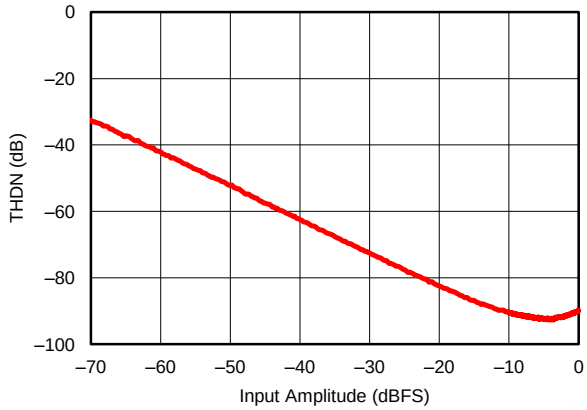
Figure 18. Micbias, Output Voltage versus Load Current

7.14.4 Audio DAC to Line Out Performance



Differential Line Out R_{load}=10kΩ CM=0.9V
RECVDD_33=1.8V Input Amplitude=-3dBFS

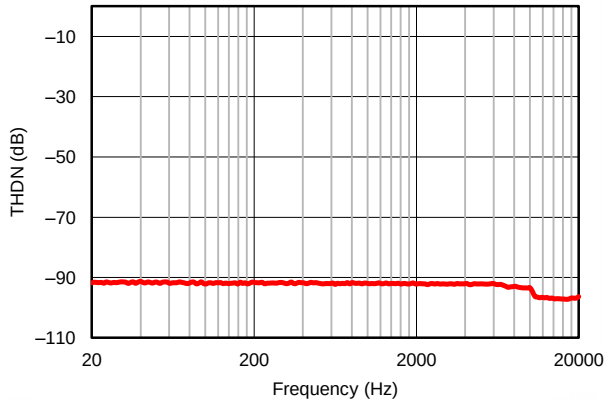
Figure 19. DAC Playback on Line Out Amplifier, Output Amplitude versus Frequency



Differential Line Out R_{load}=10kΩ CM=0.9V
RECVDD_33=1.8V

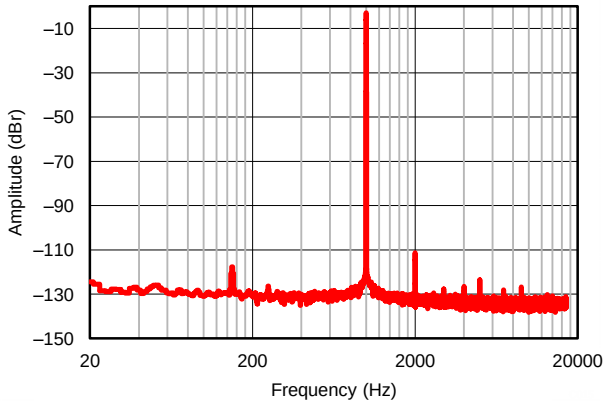
Figure 20. DAC Playback on Line Out Amplifier, Total Harmonic Distortion + Noise versus Input Amplitude

Typical Characteristics (continued)



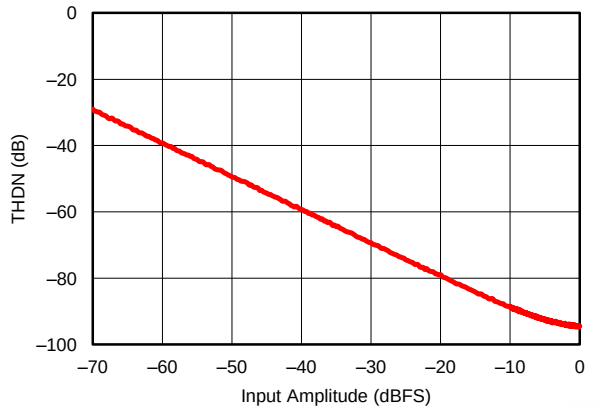
Differential Line Out R_{load}=10kΩ CM=0.9V
RECVDD_33=1.8V
Input Amplitude=-3dBFS

Figure 21. DAC Playback on Line Out Amplifier, Total Harmonic Distortion + Noise versus Input Frequency



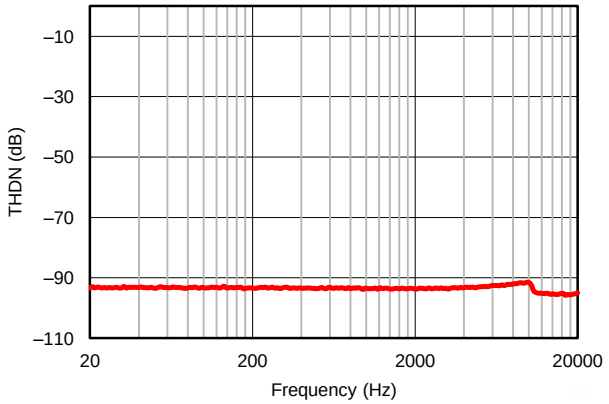
Single-ended Line Out R_{load}=10kΩ CM=0.9V
Input Amplitude=-3dBFS

Figure 22. DAC Playback on Line Out Amplifier, Output Amplitiude versus Frequency



Single-ended Line Out R_{load}=10kΩ CM=0.9V

Figure 23. DAC Playback on Line Out Amplifier, Total Harmonic Distortion + Noise versus Input Amplitude

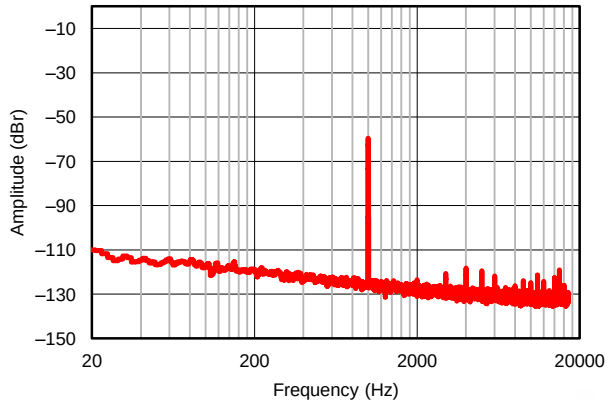


Single-ended Line Out R_{load}=10kΩ CM=0.9V
Input Amplitude=-3dBFS

Figure 24. DAC Playback on Line Out Amplifier, Total Harmonic Distortion + Noise versus Input Frequency

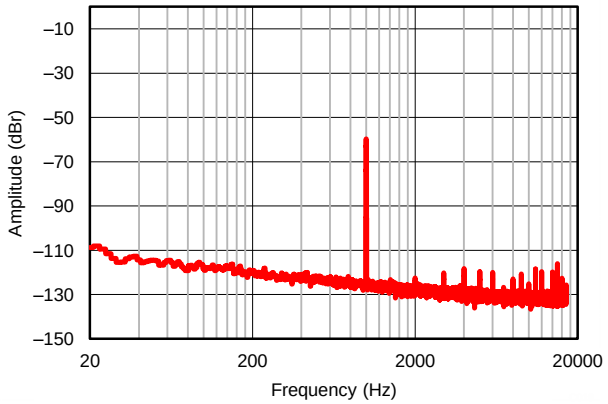
Typical Characteristics (continued)

7.14.5 Audio DAC to Headphone Performance



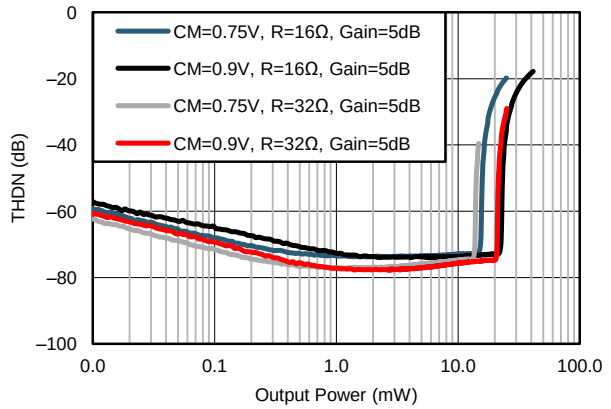
Input Amplitude=-60dBFS R_{load}=16Ω

Figure 25. DAC Playback on Headphone Amplifier, Output Amplitude versus Frequency



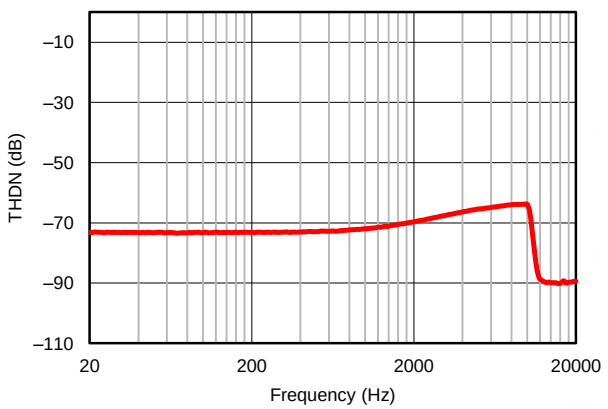
Input Amplitude=-60dBFS R_{load}=32Ω

Figure 26. DAC Playback on Headphone Amplifier, Output Amplitude versus Frequency



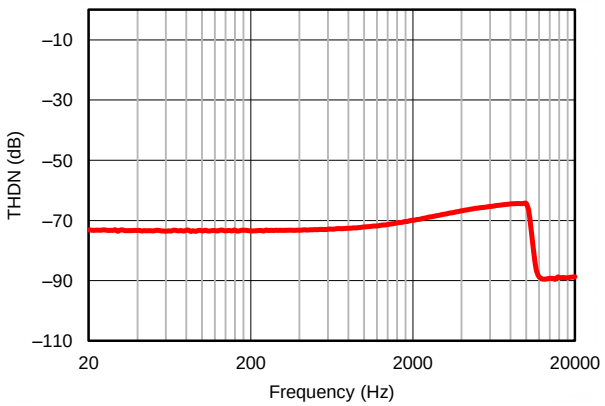
Headphone Gain=5dB R_{load}=16Ω and 32Ω
Device CM=0.75V and 0.9V

Figure 27. DAC Playback on Headphone Amplifier, Total Harmonic Distortion + Noise versus Output Power



Headphone Gain=0dB Device CM=0.9V R_{load}=16Ω
Input Amplitude=-3dBFS

Figure 28. DAC Playback on Headphone Amplifier, Total Harmonic Distortion + Noise versus Input Frequency

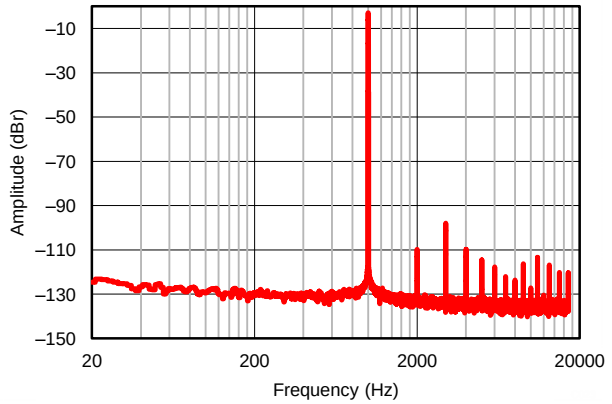


Headphone Gain=0dB Device CM=0.9V R_{load}=32Ω
Input Amplitude=-3dBFS

Figure 29. DAC Playback on Headphone Amplifier, Total Harmonic Distortion + Noise versus Input Frequency

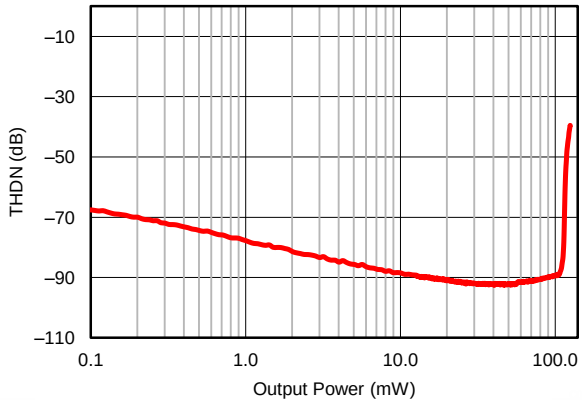
Typical Characteristics (continued)

7.14.6 Audio DAC to Receiver Performance



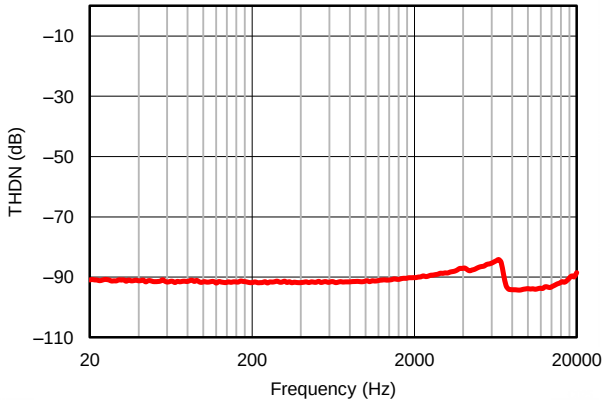
Receiver Gain=6dB Device CM=0.9V R_{load}=32Ω
Input Amplitude=-3dBFS Output CM=1.65V

Figure 30. DAC Playback on Receiver Amplifier, Output Amplitude versus Input Frequency



Receiver Gain=6dB Device CM=0.9V R_{load}=32Ω
Output CM=1.65V

Figure 31. DAC Playback on Receiver Amplifier, Total Harmonic Distortion + Noise versus Output Power

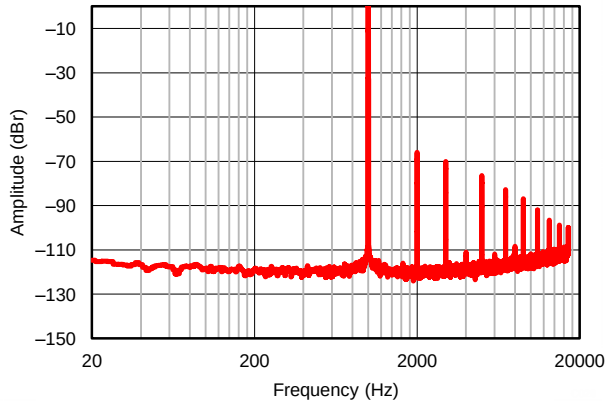


Receiver Gain=6dB Device CM=0.9V R_{load}=32Ω
Input Amplitude=-3dBFS Output CM=1.65V

Figure 32. DAC Playback on Receiver Amplifier, Total Harmonic Distortion + Noise versus Input Frequency

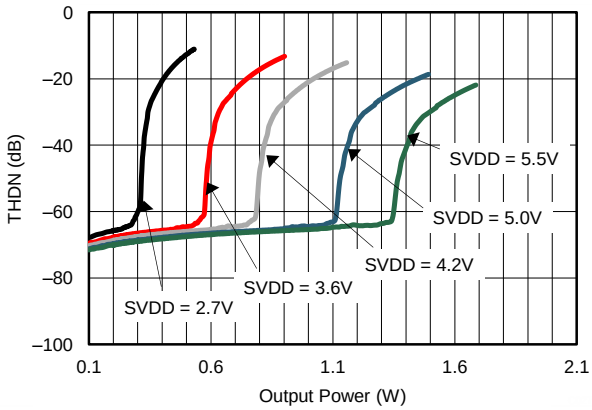
Typical Characteristics (continued)

7.14.7 Class-D Driver Performance



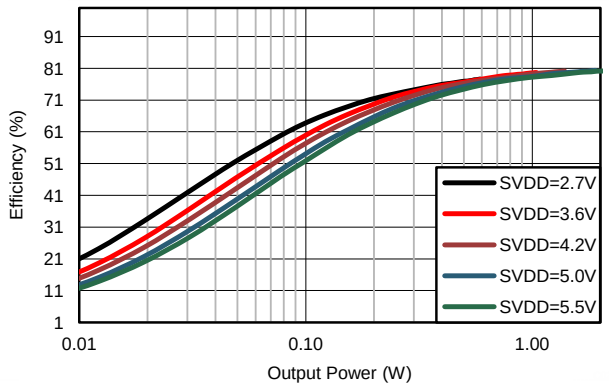
Input Amplitude=-3dBFS R_{load}=8Ω
Speaker Gain=6dB

Figure 33. DAC Playback on Speaker Amplifier, Output Amplitude versus Frequency



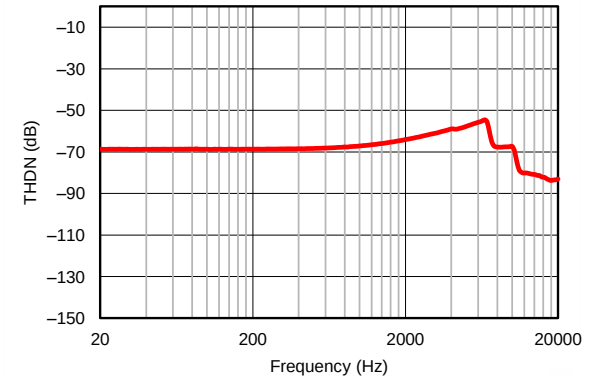
Speaker Gain=12dB R_{load}=8Ω
SVDD=2.7V, 3.6V, 4.2V, 5.0V and 5.5V

Figure 34. DAC Playback on Speaker Amplifier, Total Harmonic Distortion + Noise versus Output Power



SVDD=2.7V, 3.6V, 4.2V, 5.0V and 5.5V
R_{load}=8Ω

Figure 35. DAC Playback on Speaker Amplifier, Efficiency versus Output Power



Speaker Gain=6dB R_{load}=8Ω
Input Amplitude=-3dBFS

Figure 36. DAC Playback on Speaker Amplifier, Total Harmonic Distortion versus Input Frequency

8 Detailed Description

8.1 Overview

The TLV320AIC3268 (AIC3268) is a flexible, highly-integrated, low-power, low-voltage stereo audio codec. The AIC3268 features four digital microphone inputs, plus programmable outputs, PowerTune capabilities, enhanced fully-programmable miniDSP, predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital audio interfaces. Extensive register-based control of power, input and output channel configuration, gains, effects, terminal-multiplexing and clocks are included, allowing the device to be precisely targeted to its application.

The record path of the TLV320AIC3268 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations which cover single-ended and differential setups, as well as floating or mixing input signals. It also provides a digitally-controlled stereo microphone preamplifier and integrated microphone bias. The record path can also be configured for up to two stereo (that is up to 4) simultaneous digital microphone Pulse Density Modulation (PDM) interfaces typically used at 64Fs or 128Fs.

The playback path offers signal processing blocks for filtering and effects; headphone, line, receiver, and Class-D speaker output; flexible mixing of DAC; and analog input signals as well as programmable volume controls. The playback path contains two high-power DirectPath™ headphone output drivers which eliminate the need for ac coupling capacitors. A built in charge pump generates the negative supply for the ground centered headphone drivers. These headphone output drivers can be configured in multiple ways, including stereo, and mono BTL. The playback path also features stereo lineout drivers, which can be configured either for single-ended operation or differential output operation for high performance systems. In addition, playback audio can be routed to an integrated Class-D speaker driver or a differential receiver amplifier.

The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320AIC3268 can address both cases.

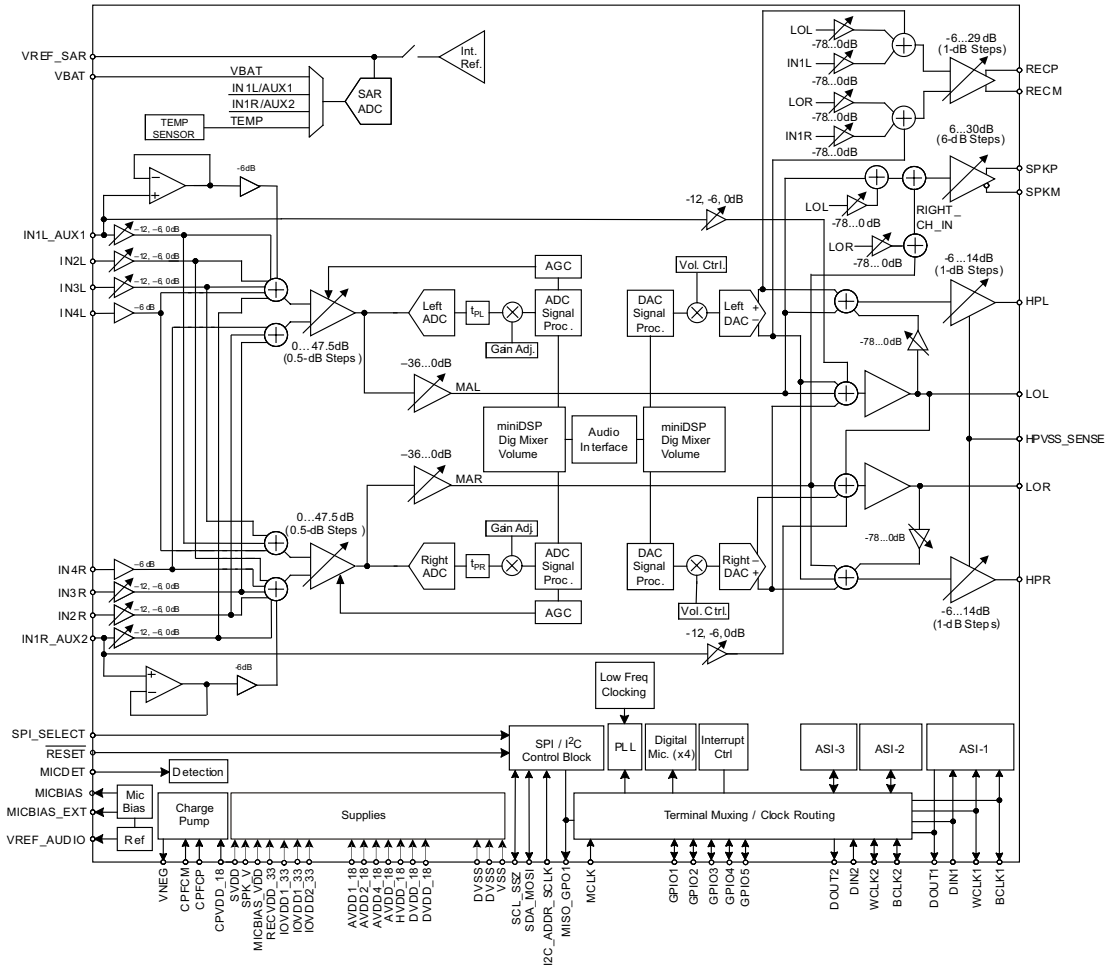
The required internal clock of the TLV320AIC3268 can be derived from multiple sources, including the MCLK terminal, the BCLK1 terminal, the BCLK2 terminal, several general purpose IO terminals or the output of the internal PLL, where the input to the PLL again can be derived from similar terminals. Although using the internal fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz. To enable even lower clock frequencies, an integrated low-frequency clock multiplier can also be used as an input to the PLL.

The TLV320AIC3268 has a 12-bit SAR ADC converter that supports system voltage measurements. These system voltage measurements can be sourced from three dedicated analog inputs (IN1L/AUX1, IN1R/AUX2 or VBAT terminals), or, alternatively, an on-chip temperature sensor that can be read by the SAR ADC.

The device also features three full Digital Audio Serial Interfaces, each supporting I2S, DSP/TDM, RJF, LJF, and mono PCM formats. This enables three simultaneous digital playback and record paths to three independent digital audio buses or chips. Each of the Digital Audio Serial Interfaces can be run using separate power voltages to enable easy integration with separate chips with different IO voltages.

The device is available in the 9mm x 9mm x 0,9mm 64-terminal QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Audio I/O

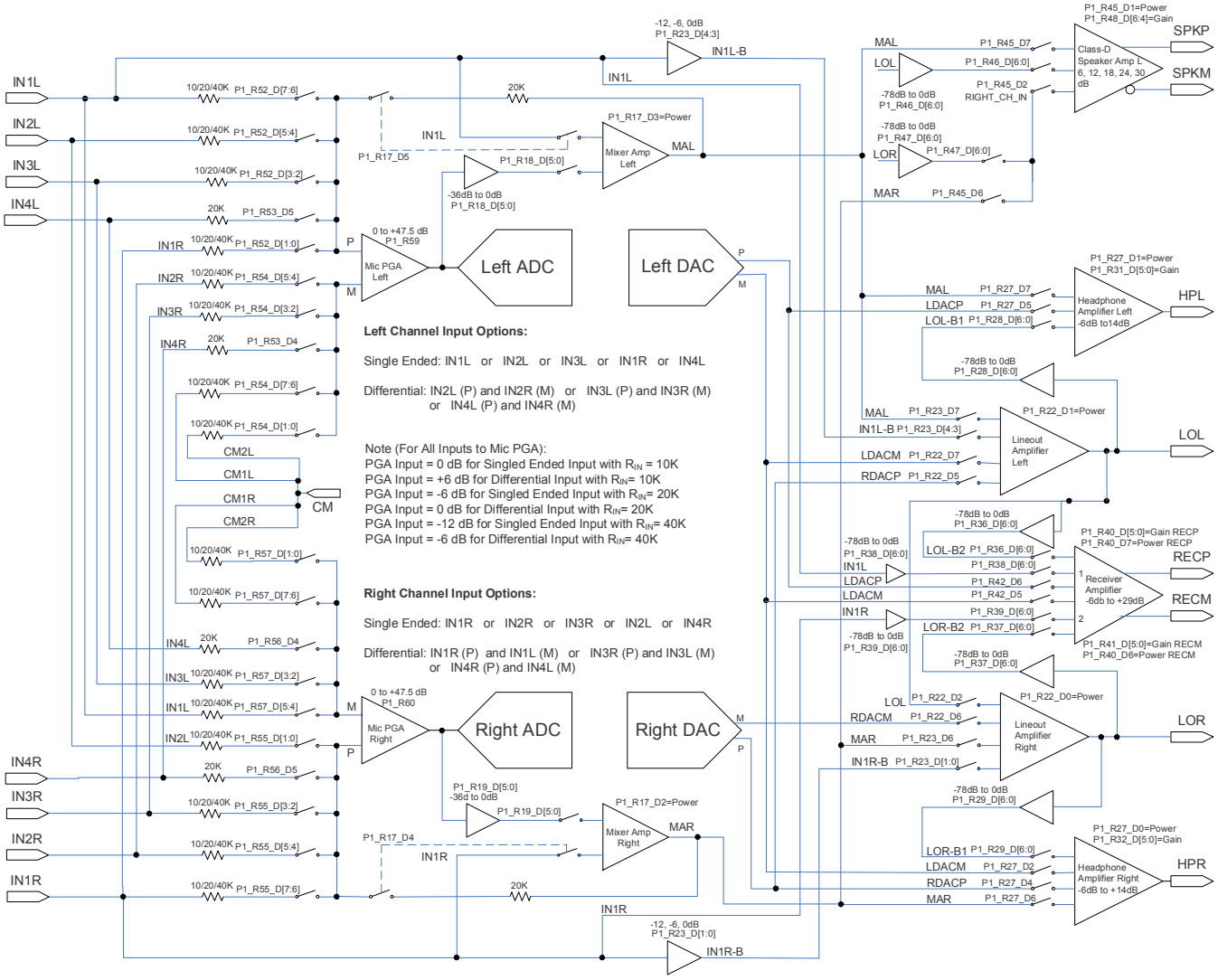


Figure 37. Analog Routing Diagram

8.3.1.1 Analog Low Power Bypass

The TLV320AIC3268 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input terminal to an amplifier driving an analog output terminal. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode. In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the left lineout amplifier (LOL) and IN1R to LOR. Additionally, line-level signals can be routed directly from these analog inputs to the amplifier.

8.3.1.2 Headphone Outputs

The stereo headphone drivers on terminals HPL and HPR can drive loads with impedances down to 16Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large dc-blocking capacitors.

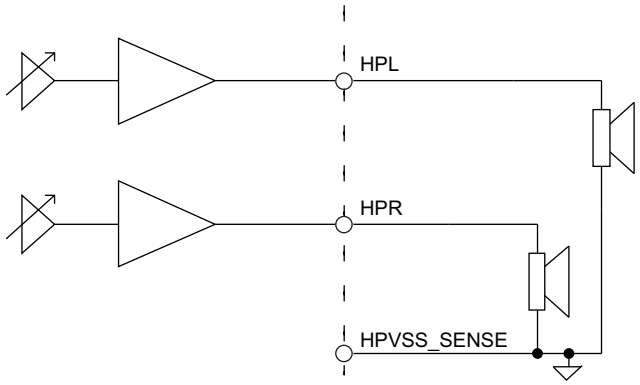


Figure 38. TLV320AIC3268 Ground-Centered Headphone Output

8.3.1.2.1 Using the Headphone Amplifier

The headphone drivers are capable of driving a mixed combination of DAC signal, left and right ADC PGA signal, and LOL and LOR output signals by configuring B0_P1_R27-R29. The ADC PGA signals can be attenuated up to 36dB before routing to headphone drivers by configuring B0_P1_R18 and B0_P1_R19. The line-output signals can be attenuated up to 78dB before routing to headphone drivers by configuring B0_P1_R28 and B0_P1_R29. The level of the DAC signal can be controlled using the digital volume control of the DAC by configuring B0_P0_R64-R66. To control the output-voltage swing of headphone drivers, the headphone driver volume control provides a range of –6.0dB to +14.0dB in steps of 1dB. These can be configured by programming B0_P1_R27, B0_P1_R31, and B0_P1_R32. In addition, finer volume controls are also available when routing LOL or LOR to the headphone drivers by controlling B0_P1_R27-R28. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Register B0_P1_R9_D[6:5] allows the headphone output stage to be scaled to tradeoff power delivered vs quiescent power consumption. (1)

8.3.1.2.2 Ground-Centered Headphone Amplifier Configuration

Among the other advantages of the ground-centered connection is inherent freedom from turn-on transients that can cause audible pops, sometimes at uncomfortable volumes.

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

8.3.1.2.2.1 Circuit Topology

The power supply hook up scheme for the ground centered configuration is shown in HVDD_18 terminal supplies the positive side of the headphone amplifier. CPVDD_18 terminal supplies the charge pump which in turn supplies the negative side of the headphone amplifier. Two capacitors are required for the charge pump circuit to work. These capacitors should be X7R rated.

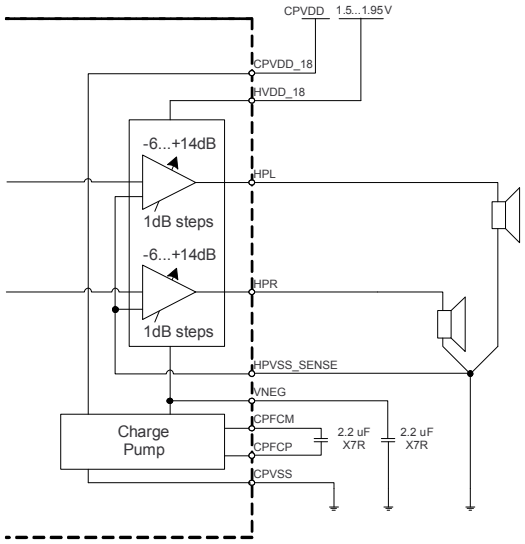


Figure 39. Ground-Centered Headphone Connections

8.3.1.2.2.2 Charge Pump Setup and Operation

The built in charge pump draws charge from the CPVDD_18 supply, and by switching the external capacitor between CPFCP and CPFCM, generates the negative voltage on VNEG terminal. The charge-pump circuit uses the principles of switched-capacitor charge conservation to generate the VNEG supply in a very efficient fashion.

To turn on the charge pump circuit when headphone drivers are powered, program B0_P1_R35_D[1:0] to "'00". When the charge pump circuit is disabled, VNEG acts as a ground terminal, allowing unipolar configuration of the headphone amps. By default, the charge pump is disabled. The switching rate of the charge pump can be controlled by B0_P1_R33. Because the charge pump can demand significant inrush currents from the supply, it is important to have a capacitor connected in close proximity to the CPVDD_18 and CPVSS terminals of the device. At 500kHz clock rate this requires approximately a 10µF capacitor. The ESR and ESL of the capacitor must be low to allow fast switching currents.

The ground-centered mode of operation is enabled by configuring B0_P1_R31_D7 to "1". Note that the HPL and HPR gain settings are ganged in Ground-Cetered Mode of operation (B0_P1_R32_D7 = "1"). The HPL and HPR gain settings cannot be ganged if using the Stereo Unipolar Configuration.

8.3.1.2.2.3 Output Power Optimization

The device can be optimized for a specific output-power range. The charge pump and the headphone driver circuitry can be reduced in power so less overall power is consumed. The headphone driver power can be programmed in B0_P1_R9. The control of charge pump switching current is programmed in B0_P1_R34_D[4:2].

8.3.1.2.2.4 Offset Correction and Start-Up

The TLV320AIC3268 offers an offset-correction scheme that is based on calibration during power up. This scheme minimizes the differences in DC voltage between HPVSS_SENSE and HPL/HPR outputs.

The offset calibration happens after the headphones are powered up in ground-centered configuration. All other headphone configurations like signal routings, gain settings and mute removal must be configured before headphone powerup. Any change in these settings while the headphones are powered up may result in additional offsets and are best avoided.

The offset-calibration block has a few programmable parameters that the user must control. The user can either choose to calibrate the offset only for the selected input routing or all input configurations. The calibration data is stored in internal memory until the next hardware reset or until AVDDx power is removed.

Programming B0_P1_R34_D[1:0] as "10" causes the offset to be calibrated for the selected input mode. Programming B0_P1_R34_D[1:0] as “11” causes the offset to be calibrated for all possible configurations. All related blocks must be powered while doing offset correction.

Programming B0_P1_R34_D[1:0] as “00” (default) disables the offset correction block. While the offset is being calibrated, no signal should be applied to the headphone amplifier, that is the DAC should be kept muted and analog bypass routing should be kept at the highest attenuation.

8.3.1.3 Stereo Line Outputs

The TLV320AIC3268 features stereo line level drivers which can be configured in either fully differential configuration (RECP, RECM and LOL, LOR) or single-ended configuration (LOL and LOR).The stereo line level drivers can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common mode of line level drivers can be configured to equal the analog input common-mode setting, either 0.75V or 0.9V. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal, and signal mixing is register-programmable.

8.3.1.3.1 Line Out Amplifier Configurations

The TLV320AIC3268 can support stereo differential lineout as shown in Figure 40 for stereo DAC playback.

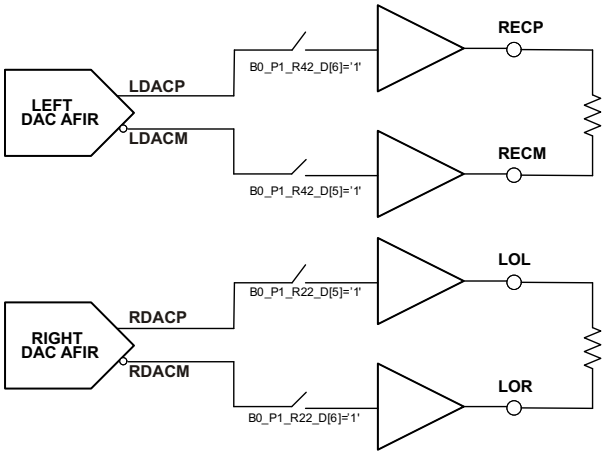


Figure 40. Stereo Differential Line-out

In this mode, the output common-mode setting of the receiver amplifier should be kept the same as the input common mode by programming B0_P1_R8_D[1:0]="00". Also, in this mode the receiver driver gain should be kept at 0dB by programming B0_P1_R40_D[5:0] and B0_P1_R41_D[5:0] as "000000". The RECVDD_33 supply should be connected to the AVDDx_18 power rails for symmetricity.

The TLV320AIC3268 can also support stereo single-ended line outputs as shown in Figure 41 for stereo DAC playback.

Signal mixing can be configured by programming B0_P1_R22 and B0_P1_R23. To route the output of Left DAC and Right DAC for stereo single-ended output, as shown in Figure 41, LDACM can be routed to LOL driver by setting B0_P1_R22_D7 = ‘1’, and RDACM can be routed to LOR driver by setting B0_P1_R22_D6 = ‘1’. Alternatively, stereo single-ended signals can also be routed through the mixer amplifiers by configuring B0_P1_R23_D[7:6]. For lowest-power operation, stereo single-ended signals can also be routed in direct terminal bypass with possible gains of 0dB, -6dB, or -12dB by configuring B0_P1_R23_D[4:3] and B0_P1_R23_D[1:0]. While each of these two bypass cases could be used in a stereo single-ended configuration, a mono differential input signal could also be used.

The output of the stereo line out drivers can also be routed to the stereo headphone drivers, with 0dB to -72dB gain controls in steps of 0.5dB on each headphone channel. This enables the DAC output or bypass signals to be simultaneously played back to the stereo headphone drivers as well as stereo line- level drivers. This routing and volume control is achieved in B0_P1_R28 and B0_P1_R29.

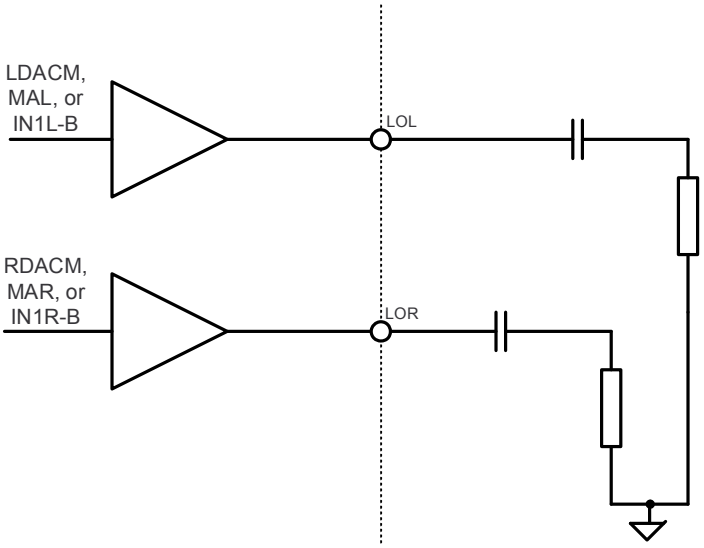


Figure 41. Stereo Single-Ended Line-out

Additionally, the two line-level drivers can be configured to act as a mono differential line level driver by routing the output of LOL to LOR (B0_P1_R22_D2 = '1'). This differential signal takes either LDACM, MAL, or IN1L-B as a single-ended mono signal and creates a differential mono output signal on LOL and LOR.

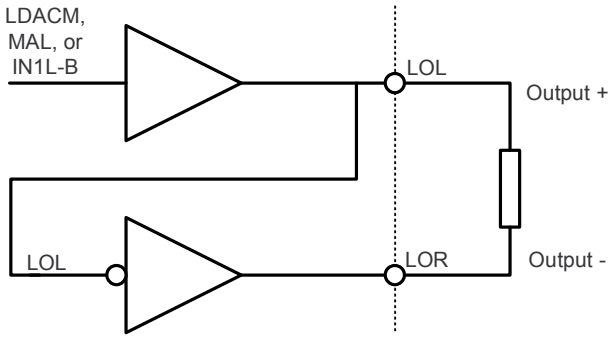


Figure 42. Single Channel Input to Differential Line-out

8.3.1.4 Differential Receiver Output

The differential receiver amplifier output spans the RECP and RECM terminals and can drive a 32Ω receiver driver. he receiver driver can drive up to a 1Vrms output signal.

The differential receiver driver is capable of driving a mixed combination of DAC signal through the Line Out amplifiers and the line-bypass from analog input IN1L and IN1R. Routing and volume level setting of the IN1L and IN1R input signals to the Positive and Negative driver is controlled by B0_P1_R38 and B0_P1_R39 respectively. These two registers enable fine tuning of the inputs to the receiver driver by allowing up to 78dB of attenuation. A single volume control can be utilized for both inputs by setting B0_P1_R39_D7. Routing and volume level setting of the LOL and LOR signals to the positive and negative inputs of the differential receiver driver is controlled by B0_P1_R36 and B0_P1_R37 respectively. These two registers enable fine tuning of the separate positive and negative differential signals by allowing up to 78dB of attenuation. A single volume control can be utilized for both inputs by setting B0_P1_R37_D7. Routing of LDACP and LDACM signals to the Positive and Negative driver is controlled by B0_P1_R42_D6 and B0_P1_R42_D5 respectively.

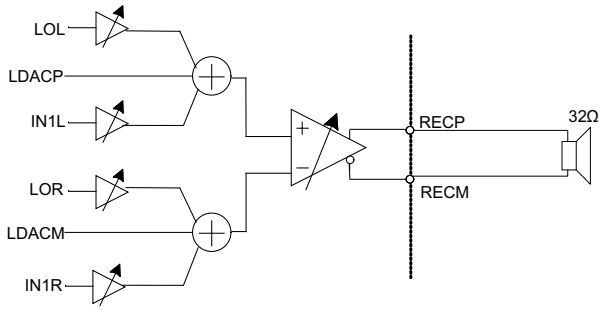


Figure 43. Receiver Differential Output

The receiver driver can be powered on by writing 11 to B0_P1_R40_D[7:6]. The positive driver gain and muting can be controlled by writing to B0_P1_R40_D[5:0], and the negative driver gain can be controlled by writing to B0_P1_R41_D[5:0], with each amplifier providing -6dB to 29dB gains in steps of 1dB. A single volume control can be utilized for the differential receiver output drivers by setting B0_P1_R41_D7 to '1'.

The TLV320AIC3268 has an overcurrent/short-circuit protection feature for the receiver drivers that is always enabled to provide protection. If the output is shorted, this overcurrent condition either shuts down the output stage (if B0_P1_R10_D0 = 1) or starts to limit the amount of current (if B0_P1_R10_D0 = 0). The default condition for the receiver driver is current-limiting mode. In case of a short circuit, for automatic latching shutdown, the output is disabled and a status flag is provided as read-only bits B0_P0_R44_D7 for RECP and on B0_P0_R44_D6 for RECM.

The receiver driver also has an offset calibration for minimizing start-up transients. By default, this feature is enabled at every power-up by setting B0_P1_R42_D[4:3] to '01'. The status of the offset calibration can be read through the Receiver Offset Calibration Flag (B0_P1_R42_D7). Offset calibration should only be disabled if this driver is utilized as a second single-ended headphone configuration (that is, should not be utilized in differential configuration).

8.3.1.5 Class-D Speaker Outputs

The integrated Class-D speaker driver (SPKP, SPKN) is capable of driving an 8Ω differential load. The speaker driver can be powered directly from the power supply (2.7V to 5.5V) on the SVDD terminal, however the voltage (including spike voltage) must be limited below the Absolute Maximum Voltage of 6.0V.

The speaker driver capable of supplying 0.74 W at 10% THD+N with a 3.6-V power supply and 1.45 W at 10% THD+N with a 5.0V power supply. Separate left and right channels can be sent to the Class-D driver through the Lineout signal path, or from the mixer amplifiers in the ADC bypass. Additionally, the analog mixer before the Speaker amplifier can sum the left and right audio signals for monophonic playback.

The speaker driver is capable of driving a mixed combination of DAC signal through the Line Out amplifiers and the left and right ADC PGA signal. The ADC PGA signals can be routed to the speaker drivers by setting B0_P1_R45_D7 (Left Mixer amplifier to Speaker) and B0_P1_R45_D6 (Right Mixer amplifier to Speaker), and these signals can be attenuated up to 36dB before this routing to the speakers by configuring B0_P1_R18 and B0_P1_R19. Routing and volume level setting of the LOL and LOR signals to the speaker driver is controlled by B0_P1_R46 and B0_P1_R47 respectively. These two registers enable fine tuning of the separate stereo signals by allowing up to 78dB of attenuation. To play the stereo DAC signals through the Line Out amplifiers to the speaker, the DAC signals should be routed to the LOL/LOR drivers by setting B0_P1_R22_D[7:6]. The level of these DAC signal can also be controlled using the digital volume control of the DAC signal (B0_P0_R65 and B0_P0_R66).

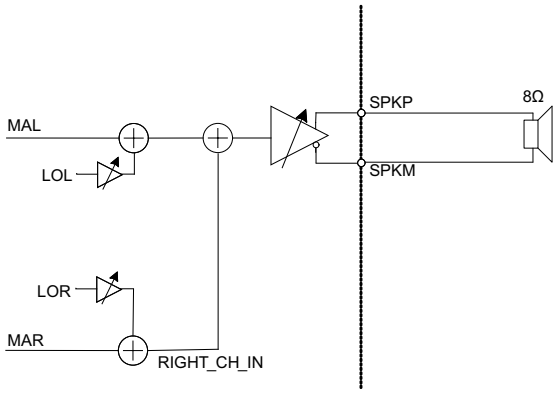


Figure 44. Speaker Output

The class-D speaker driver can be powered on by writing to B0_P1_R45_D1. The driver gain can be controlled by writing to B0_P1_R48_D[6:4], and it can be muted by writing '000' to these bits.

The TLV320AIC3268 has a short-circuit protection feature for the speaker driver that is always enabled to provide protection. If the output is shorted, the output stage shuts down on the overcurrent condition. (Current limiting is not an available option for the higher-current speaker driver output stage.) In case of a short circuit, the output is disabled and a status flag is provided as a read-only bit on B0_P0_R44_D7. If shutdown occurs due to an overcurrent condition, then the device requires a reset to re-enable the output stage. Resetting can be done in two ways. First, the device master reset can be used, which requires either toggling the RESET terminal or using the software reset. If master reset is used, it resets all of the registers. Second, a dedicated speaker power-stage reset can be used that keeps all of the other device settings. The speaker power-stage reset is done by setting B0_P1_R45_D1. If the fault condition has been removed, then the device returns to normal operation. If the fault is still present, then another shutdown occurs. Repeated resetting (more than three times) is not recommended, as this could lead to overheating.

The TLV320AIC3268 has an overtemperature thermal-protection (OTP) feature for the speaker driver which is always enabled to provide protection. If the device is overheated, then the output stops switching. When the device cools down, the device resumes switching. An overtemperature status flag is provided as a read-only bit on B0_P0_R45_D7, and this status flag can be routed to INT1 interrupt (B0_P0_R48_D1 = '1') or INT2 interrupt (B0_P0_R49_D1 = '1'). The OTP feature is for self-protection of the device. If die temperature can be controlled at the system/board level, then overtemperature does not occur.

To minimize battery current leakage, the SVDD voltage levels should not be less than the AVDDx_18 voltage levels.

8.3.2 ADC / Digital Microphone Interface

The TLV320AIC3268 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter and a programmable miniDSP. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3268 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs
- 8 analog inputs which can be mixed or multiplexed in single-ended or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

- Automatic gain control (AGC)

In addition to the standard set of ADC features the TLV320AIC3268 also offers the following special functions:

- Built in microphone biases
- Four-channel digital microphone interface
  - Allows 4 total microphones
  - Up to 4 digital microphones
  - Up to 2 analog microphones
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive coefficient update mode

8.3.2.1 ADC Signal Routing

As shown in Figure 37, the TLV320AIC3268 includes eight analog inputs which can be configured as either 4 stereo single-ended pairs or 4 fully-differential pairs. These terminals connect through series resistors and switches to the virtual ground terminals of two fully-differential amplifiers (one per ADC/PGA channel). By turning on only one set of switches per amplifier at a time, the inputs can be effectively multiplexed to each ADC PGA channel. By turning on multiple sets of switches per amplifier at a time, audio sources can be mixed. The TLV320AIC3268 supports the ability to mix up to five single-ended analog inputs or up to three fully-differential analog inputs into each ADC PGA channel.

In most applications, high input impedance is desired for analog inputs. However when used in conjunction with high gain as in the case of microphone inputs, the higher input impedance results in higher noise or lower dynamic range. The TLV320AIC3268 allows the user the flexibility of choosing the input impedance from 10kΩ, 20kΩ and 40kΩ. When multiple inputs are mixed together, by choosing different input impedances, level adjustment can be achieved. For example, if one input is selected with 10kΩ input impedance and the second input is selected with 20kΩ input impedance, then the second input is attenuated by half as compared to the first input. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting. Also, note that this input-level configurability is available on IN1L, IN1R, IN2L, IN2R, IN3L, and IN3R; for IN4L and IN4R, this input impedance is fixed at 20kΩ.

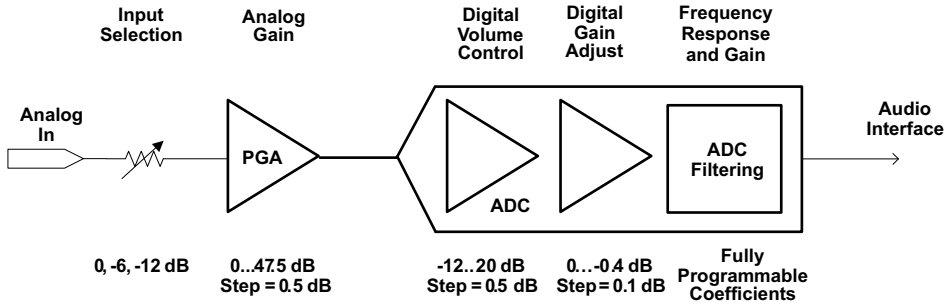
Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal amplifiers, resulting in saturation and clipterminalg of the mixed output signal. Whenever mixing is being implemented, the system designer is advised to take adequate precautions to avoid such a saturation from occurring. In general, the mixed signal should not exceed 0dB.

Typically, voice or audio signal inputs are capacitively coupled to the device. This allows the device to independently set the common mode of the input signals to values chosen by register control of B0_P1_R8_D2 to either 0.9V or 0.75V. The correct value maximizes the dynamic range across the entire analog supply range. Failure to capacitively connect the input to the device can cause high offset due to mismatch in source common-mode and device common-mode setting. In extreme cases it could also saturate the analog channel, causing distortion.

8.3.2.1.1 High Impedance Input Mode

The TLV320AIC3268 supports a special high impedance input mode on terminals IN1L/AUX1 and IN1R/AUX2 to enable interfacing with sensors having high output impedance. By programming B0_P1_R17_D[5] and B0_P1_R17_D[4] to '1' IN1L/AUX1 and IN1R/AUX2 can be used in high impedance mode respectively. While using this mode, IN1L/AUX1 and IN1R/AUX2 should not be routed to Left and Right ADC PGA's or B0_P1_R52_D[7:6], B0_P1_R52_D[1:0], B0_P1_R55_D[7:6] and B0_P1_R57_D[5:4] should be programmed as "00". While using this mode the signal should be externally biased around a common mode which is close to the device common mode programmed via B0_P1_R8_D[2]. When using high impedance mode, routing of MAL and MAR amplifiers to Speaker Amplifier and Lineout Drivers is not supported.

8.3.2.2 ADC Gain Setting



When the gain of the ADC Channel is kept at 0dB and the common mode set to 0.75V, a single-ended input of $0.375V_{RMS}$ results in a full-scale digital signal at the output of ADC channel. Similarly, when the gain is kept at 0dB, and common mode is set to 0.9V, a single-ended input of $0.5V_{RMS}$ results in a full-scale digital signal at the output of the ADC channel. However various block functions control the gain through the channel. The gain applied by the PGA is described in Table 7. Additionally, the digital volume control adjusts the gain through the channel as described in Digital Volume Control. A finer level of gain adjustment is possible and described in Fine Digital Gain Adjustment. The decimation filters A, B and C along with the delta-sigma modulator contribute to a DC gain of 1.0 through the channel.

8.3.2.2.1 Analog Programmable Gain Amplifier (PGA)

The TLV320AIC3268 features a built-in low-noise PGA for boosting low-level signals, such as direct microphone inputs, to full-scale to achieve high SNR. This PGA can provide a gain in the range of 0dB to 47.5dB for single-ended inputs or 6dB to 53.5dB for fully-differential inputs (gain calculated w.r.t. input impedance setting of 10kΩ, 20kΩ input impedance will result in 6dB lower and 40kΩ will result in 12dB lower gain). This gain can be user controlled by writing to B0_P1_R59 and B0_P1_R60. In the AGC mode this gain can also be automatically controlled by the built-in hardware AGC.

Table 7. Analog PGA vs Input Configuration

Book 0, Page 1, Register 59, D[6:0] (B0_P1_R59_D[6:0]) Book 0, Page 1, Register 60, D[6:0] B0_P1_R60_D[6:0]	EFFECTIVE GAIN APPLIED BY PGA					
	SINGLE-ENDED			DIFFERENTIAL		
	R_{IN} = 10kΩ	R_{IN} = 20kΩ	R_{IN} = 40kΩ	R_{IN} = 10kΩ	R_{IN} = 20kΩ	R_{IN} = 40kΩ
000 0000	0 dB	–6 dB	-12 dB	6.0 dB	0 dB	–6.0 dB
000 0001	0.5 dB	–5.5 dB	–11.5 dB	6.5 dB	0.5 dB	-5.5 dB
000 0010	1.0 dB	–5.0 dB	–11.0 dB	7.0 dB	7.5 dB	–5.0 dB
…	…	…	…	…	…	…
101 1110	47.0 dB	41.0 dB	35.0 dB	53.0 dB	47.0 dB	41.0 dB
101 1111	47.5 dB	41.5 dB	35.5 dB	53.5 dB	47.5 dB	41.5 dB

The gain changes are implemented with an internal soft-stepterminalg algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register value (see registers B0_P0_R81_D[1:0]). This soft-stepterminalg ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and at power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag B0_P0_R36_D7 and B0_P0_R36_D3 is set whenever the gain applied by the PGA equals the desired value set by the register. The soft-stepterminalg control can also be disabled by programming B0_P0_R81_D[1:0].

8.3.2.2.2 Digital Volume Control

The TLV320AIC3268 also has a digital volume-control block with a range from -12dB to +20dB in steps of 0.5dB. It is set by programming B0_P0_R83 and B0_P0_R84 respectively for left and right channels.

Table 8. Digital Volume Control for ADC

Desired Gain (dB)	Left / Right Channel B0_P0_R83 and B0_P0_R84, D[6:0]
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (Default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, the soft-stepterminalg feature is used to avoid audible artifacts. The soft-stepterminalg rate can be set to either 1 or 2 gain steps per sample. Soft-stepterminalg can also be entirely disabled. This soft-stepterminalg is configured via B0_P0_R81_D[1:0], and is common to soft-stepterminalg control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to -12.0dB before powering down. Due to the soft-stepterminalg control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320AIC3268 gives feedback to the user, through read-only flags B0_P0_R36_D7 for Left Channel and B0_P0_R36_D3 for the right channel.

8.3.2.2.3 Fine Digital Gain Adjustment

Additionally, the gains in each of the channels is finely adjustable in steps of 0.1dB. This is useful when trying to match the gain between channels. By programming B0_P0_R82, the gain can be adjusted from 0dB to -0.4dB in steps of 0.1dB. This feature, in combination with the regular digital volume control allows the gains through the left and right channels be matched in the range of -0.5dB to +0.5dB with a resolution of 0.1dB.

8.3.2.2.4 AGC

The TLV320AIC3268 includes Automatic Gain Control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Since the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

1. **Target Level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC3268 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the TLV320AIC3268 reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipterminalg at the occurrence of loud sounds.
2. **Attack Time** sets how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. Wide range of attack time programmability is supported in terms of number of samples (that is, number of ADC sample frequency clock cycles).
3. **Decay Time** sets how quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. Wide range of decay time programmability is supported in terms of number of samples (that is, number of ADC sample frequency clock cycles).
4. **Gain Hysteresis** is the hysteresis applied to the required gain calculated by the AGC function while changing its mode of operation from attack to decay or vice-versa. For example, while attacking the input signal, if the current applied gain by the AGC is *x*dB, and suddenly because of input level going down, the new calculated required gain is *y*dB, then this gain is applied provided *y* is greater than *x* by the value set in Gain Hysteresis. This feature avoids the condition when the AGC function can fluctuate between a very narrow band of gains leading to audible artifacts. The Gain Hysteresis can be adjusted or disabled by the user.

5. **Noise threshold** sets the level below which if the input signal level falls, the AGC considers it as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise is not 'gained up' in the absence of speech. Noise threshold level in the AGC algorithm is programmable from -30dB to -90 dB of full-scale. When AGC Noise Threshold is set to –70dB, –80db, or –90dB, the microphone input Max PGA applicable setting must be greater than or equal to 11.5dB, 21.5dB, or 31.5dB respectively. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When utilizing the AGC noise threshold, it is recommended to configure the 1st order IIR filter as a high-pass filter to achieve best performance. The noise (or silence) detection feature can be entirely disabled by the user.
6. **Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA can be programmed from 0 dB to 58 dB in steps of 0.5 dB.
7. **Hysteresis**, as the name suggests, sets a window around the Noise Threshold which must be exceeded to either detect that the recorded signal is indeed noise or signal. If initially the energy of the recorded signal is greater than the Noise Threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the Noise Threshold by a value given by Hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the Noise Threshold by a value given by the Hysteresis setting. In order to prevent the AGC from jumterminalg between noise and signal states, (which can happen when the energy of recorded signal is very close to the Noise threshold) a non-zero hysteresis value should be chosen. The Hysteresis feature can also be disabled.
8. **Debounce Time (Noise and Signal)** sets the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set Noise Threshold, then the AGC does not increase the input gain to achieve the Target Level. However, to handle audible artifacts which can occur when the energy of the input signal is very close to the Noise Threshold, the AGC checks if the energy of the recorded signal is less than the Noise Threshold for a time greater than the Noise Debounce Time. Similarly the AGC starts increasing the input-signal gain to reach the Target Level when the calculated energy of the input signal is greater than the Noise Threshold. Again, to avoid audible artifacts when the input-signal energy is very close to Noise Threshold, the energy of the input signal needs to continuously exceed the Noise Threshold value for the Signal Debounce Time. If the debounce times are kept very small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the Debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to Noise Threshold. Both noise and signal debounce time can be disabled.
9. The **AGC Noise Threshold Flag** is a read-only flag indicating that the input signal has levels lower than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.
10. **Gain Applied by AGC** is a ready-only register setting which gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This, along with the Target Setting, can be used to determine the input signal level. In a steady state situation Target Level (dB) = Gain Applied by AGC (dB) + Input Signal Level (dB) When the AGC noise threshold flag is set, then the status of gain applied by AGC should be ignored.
11. The **AGC Saturation Flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
12. The **ADC Saturation Flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.
13. An **AGC low-pass filter** is used to help find the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low pass filter is in the form of a first-order IIR filter. Three 8-bit registers are used to form the 24-bit digital coefficient as shown on the register map. In this way, a total of 9 registers are programmed to form the 3 IIR coefficients. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (1)$$

Where:

Coefficient N0 can be programmed by writing into B40_P1_R12, B40_P1_R13, and B40_P1_R14.

Coefficient N1 can be programmed by writing into B40_P1_R16, B40_P1_R17, and B40_P1_R18.

Coefficient D1 can be programmed by writing into B40_P1_R20, B40_P1_R21, and B40_P1_R22.

N0, N1 and D1 are 24-bit 2's complement numbers and their default values implement a low-pass filter with cut-off at 0.002735*ADC_FS .

See Table 9 for various AGC programming options. AGC can be used only if analog microphone input is routed to the ADC channel.

Table 9. AGC Parameter Settings

Function	Control Register Left ADC	Control Register Right ADC	Bits
AGC enable	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D7
Target Level	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D[6:4]
Gain Hysteresis	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D[1:0]
Hysteresis	Book 0, Page 0, Register 87 (B0_P0_R87)	Book 0, Page 0, Register 95 (B0_P0_R95)	D[7:6]
Noise threshold	Book 0, Page 0, Register 87 (B0_P0_R87)	Book 0, Page 0, Register 95 (B0_P0_R95)	D[5:1]
Max PGA applicable	Book 0, Page 0, Register 88 (B0_P0_R88)	Book 0, Page 0, Register 96 (B0_P0_R96)	D[6:0]
Time constants (attack time)	Book 0, Page 0, Register 89 (B0_P0_R89)	Book 0, Page 0, Register 97 (B0_P0_R97)	D[7:0]
Time constants(decay time)	Book 0, Page 0, Register 90 (B0_P0_R90)	Book 0, Page 0, Register 98 (B0_P0_R98)	D[7:0]
Debounce time (Noise)	Book 0, Page 0, Register 91 (B0_P0_R91)	Book 0, Page 0, Register 99 (B0_P0_R99)	D[4:0]
Debounce time (Signal)	Book 0, Page 0, Register 92 (B0_P0_R92)	Book 0, Page 0, Register 100 (B0_P0_R100)	D[3:0]
Gain applied by AGC	Book 0, Page 0, Register 93 (B0_P0_R93)	Book 0, Page 0, Register 101 (B0_P0_R101)	D[7:0] (Read Only)
AGC Noise Threshold Flag	Book 0, Page 0, Register 45 (B0_P0_R45) (sticky flag), Book 0, Page 0, Register 47 (B0_P0_R47) (non-sticky flag)	Book 0, Page 0, Register 45 (B0_P0_R45) (sticky flag), Book 0, Page 0, Register 47 (B0_P0_R47) (non-sticky flag)	D[6:5] (Read Only)
AGC Saturation flag	Book 0, Page 0, Register 36 (B0_P0_R36) (sticky flag)	Book 0, Page 0, Register 36 (B0_P0_R36) (sticky flag)	D5, D1 (Read Only)
ADC Saturation flag	Book 0, Page 0, Register 42 (B0_P0_R42) (sticky flag), Book 0, Page 0, Register 43 (B0_P0_R43) (non-sticky flag)	Book 0, Page 0, Register 42 (B0_P0_R42) (sticky flag), Book 0, Page 0, Register 43 (B0_P0_R43) (non-sticky flag)	D[3:2] (Read Only)

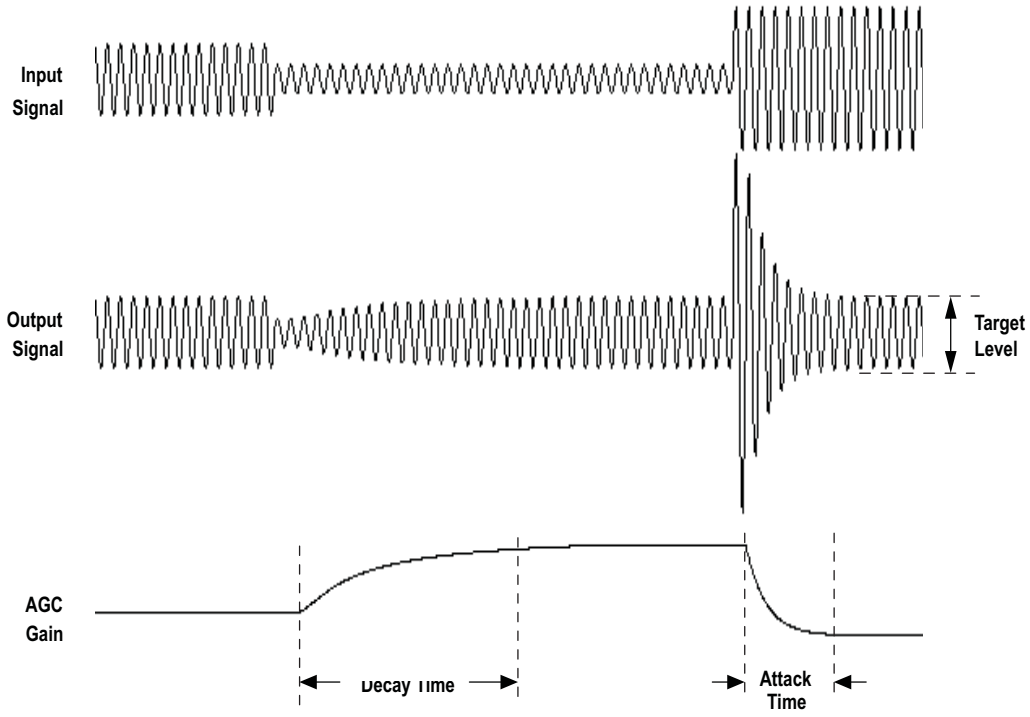


Figure 45. AGC Characteristics

The TLV320AIC3268 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

8.3.2.3 ADC Processing Blocks

The TLV320AIC3268 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

Table 10 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- AGC

Additional signal processing functions are acheived by programming the miniDSP. For specific details on available processing functions, please contact Texas Instruments.

The processing blocks are tuned for mono or stereo use cases and can achieve high anti-alias filtering. The available first order IIR, has fully user programmable coefficients.

Table 10. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1(1)	Stereo	A	Yes	0	No	128,64,32,16,8,4	7
PRB_R4	Left	A	Yes	0	No	128,64,32,16,8,4	4

(1) Default

8.3.2.4 ADC Processing Blocks – Details

8.3.2.4.1 1st order IIR, AGC, Filter A

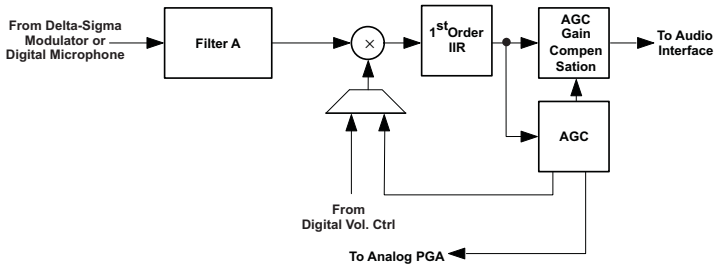


Figure 46. Signal Chain for PRB_R1 and PRB_R4

8.3.2.5 User Programmable Filters

The built-in processing block in TLV320AIC3268 has a user programmable first order IIR filter. This filter can be used for dc-blocking purposes. The user programmable coefficients allow the user to control the cut-off frequency of the high pass filter.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see Table 56.

8.3.2.5.1 1st Order IIR Section

The transfer function for the first order IIR Filter is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (2)$$

The frequency response for the 1st order IIR Section with default coefficients is flat at a gain of 0dB. Details on ADC coefficient default values are given in Table 56.

Table 11. ADC 1st order IIR Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
1st Order IIR	N0	C4 (B40_P1_R24-R26)	C36 (B40_P2_R32-R34)
	N1	C5 (B40_P1_R28-R30)	C37 (B40_P2_R36-R38)
	D1	C6 (B40_P1_R32-R34)	C39 (B40_P2_R40-R42)

8.3.2.6 Decimation Filter

The TLV320AIC3268 offers 3 different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR*f_S to the final output sampling rate of f_S. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B and C.

8.3.2.6.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance the oversampling ratio must be set to 128. Using AOSR of 64 for sampling rates up to 48kHz, gives lower power consumption, but degrades the signal to noise ratio (SNR).

Filter A can also be used for 96kHz at an AOSR of 64.

Table 12. ADC Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 f_S	0.062	dB
Filter Gain Stop Band	0.55…64f_S	–73	dB
Filter Group Delay		17/f_S	Sec.
Pass Band Ripple, 8 ksps	0…0.39 f_S	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 f_S	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 f_S	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 f_S	0.062	dB
Filter Gain Stop Band	0.55…32f_S	–73	dB
Filter Group Delay		17/f_S	Sec.
Pass Band Ripple, 8 ksps	0…0.39 f_S	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 f_S	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 f_S	0.05	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.1	dB

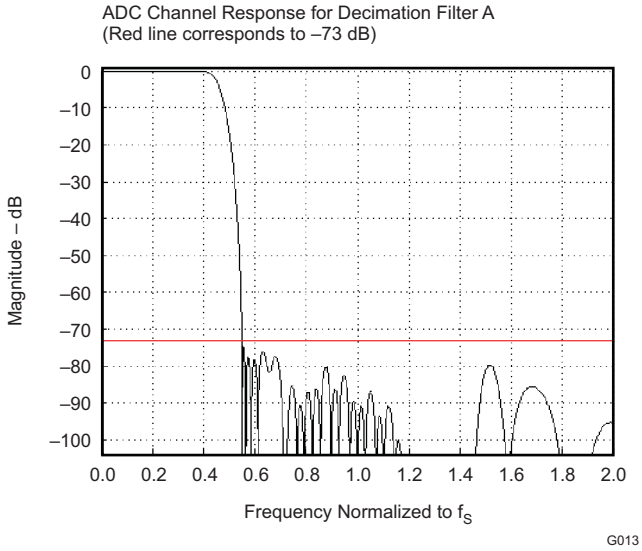


Figure 47. ADC Decimation Filter A, Frequency Response

8.3.2.6.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96kHz at a oversampling ratio of 64.

Table 13. ADC Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39f_S	±0.077	dB
Filter Gain Stop Band	0.60f_S…32f_S	–46	dB
Filter Group Delay		11/f_S	Sec.
Pass Band Ripple, 8 ksps	0…0.39f_S	0.076	dB
Pass Band Ripple, 44.1 ksps	0…0.39f_S	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39f_S	0.06	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.11	dB

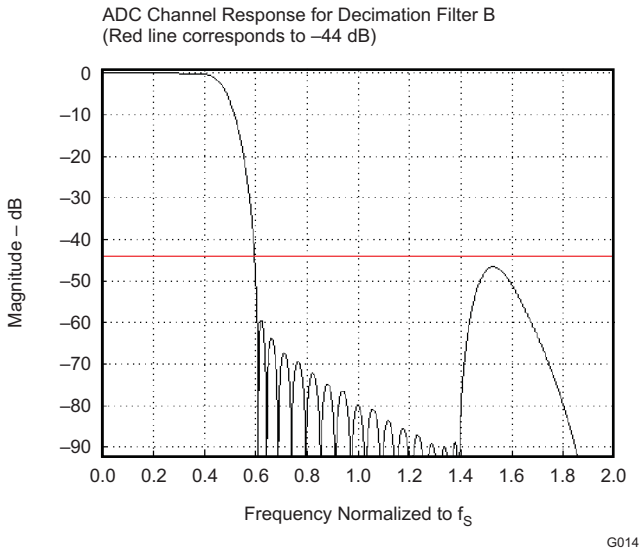


Figure 48. ADC Decimation Filter B, Frequency Response

8.3.2.6.3 Decimation Filter C

Filter type C along with AOSR of 32 is specially designed for 192ksps operation for the ADC. The pass band which extends up to 0.11*f_S (corresponds to 21kHz), is suited for audio applications.

Table 14. ADC Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11f_S	0…0.11f_S	±0.033	dB
Filter Gain from 0.28f_S to 16f_S	0.28f_S…16f_S	–60	dB
Filter Group Delay		11/f_S	Sec.
Pass Band Ripple, 8 ksps	0…0.11f_S	0.033	dB
Pass Band Ripple, 44.1 ksps	0…0.11f_S	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11f_S	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11f_S	0.032	dB
Pass Band Ripple, 192 ksps	0…20kHz	0.086	dB

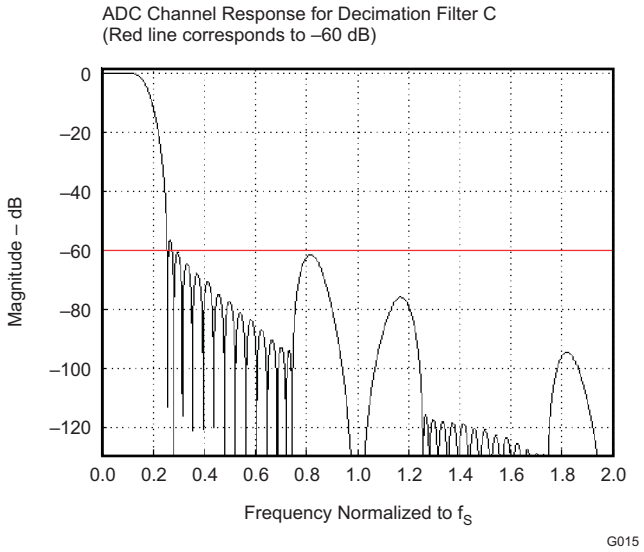


Figure 49. ADC Decimation Filter C, Frequency Response

8.3.2.7 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface once every cycle of Fs,ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

8.3.2.8 ADC Special Functions

8.3.2.8.1 Power Tune Modes

As a part of PowerTune strategy, the analog performance of ADC can be adjusted. As a consequence the power consumption on AVDDx_18 supplies can be traded off with the speed of operation (ADC_MOD_CLK) and performance.

The TLV320AIC3268 supports 4 different power tune modes for ADC, PTM_R1, PTM_R2, PTM_R3 and PTM_R4, which can be set by programming B0_P1_R61_D[7:6]. The PTM_R4 is the default mode and gives the best performance for ADC with AOSR=128 and ADC_FS up to 48ksps. At lower speeds of ADC_MOD_CLK (AOSR*ADC_FS) lower PTM modes can be used for the benefit of lower power consumption, for example for AOSR=64 and ADC_FS=8ksps, PTM_R1 can be used. Using lower PTM modes for higher frequencies of ADC_MOD_CLK can result in reduction of peak amplitude of analog inputs where the distortion performance sets in. In general , PTM_R1 is recommended till ADC_MOD_CLK up to 0.768MHz, PTM_R2 for ADC_MOD_CLK up to 1.536MHz and PTM_R3 for ADC_MOD_CLK up to 3.072MHz. In applications where power consumption is not very critical, PTM_R4 is recommended to be used for best performance.

8.3.2.8.2 Microphone Bias

The TLV320AIC3268 has two built-in low noise Microphone Bias terminals for electret-condenser microphones: MICBIAS and MICBIAS_EXT. Typically, MICBIAS is utilized for onboard microphones, while MICBIAS_EXT provides a microphone bias for inserted headsets. Each bias amplifier can support up to 8mA of load current to support multiple microphones. Each bias amplifier has been designed to provide a combination of high PSRR, low noise and programmable bias voltages to allow the user to fine tune the biasing to specific microphone combinations. To support a wide range of bias voltages, the bias amplifier can work off either a low analog supply or the higher AVDD3_33 analog supply.To support a wide range of bias voltages, the MICBIAS and MICBIAS_EXT voltage are generated through an onchip low-dropout regulator. Thus, programmed voltages should be 300mV below MICBIAS_VDD.

Table 15. MICBIAS Voltage Control

MICBIAS Mode	B0_P1_R51_D[2:0]	B0_P1_R8_D2	Minimum MICBIAS_VDD Voltage	MICBIAS Output Voltage (without load)
	000	0 or 1	2.7V	Grounded
	001	0 or 1	2.7V	Tristated (use only if external bias utilized)
MICBIAS Mode 0	010	0	2.7V	1.80V
MICBIAS Mode 0	010	1	2.7V	1.50V
MICBIAS Mode 1	011	0	2.7V	2.00V
MICBIAS Mode 1	011	1	2.7V	1.67V
MICBIAS Mode 4	110	0	3.05V	2.85V
MICBIAS Mode 4	110	1	2.7V	2.37V
MICBIAS Mode 5	111	0	3.2V	3.00V
MICBIAS Mode 5	111	1	2.7V	2.50V

Table 16. MICBIAS_EXT Voltage Control

MICBIAS_EXT Mode	B0_P1_R51_D[6:4]	B0_P1_R8_D2	Minimum MICBIAS_VDD Voltage	MICBIAS Voltage (without load)
	000	0 or 1	2.7V	Grounded
	001	0 or 1	2.7V	Tristated (use only if external bias utilized)
MICBIAS_EXT Mode 0	010	0	2.7V	1.80V
MICBIAS_EXT Mode 0	010	1	2.7V	1.50V
MICBIAS_EXT Mode 1	011	0	2.7V	2.00V
MICBIAS_EXT Mode 1	011	1	2.7V	1.67V

Table 16. MICBIAS_EXT Voltage Control (continued)

MICBIAS_EXT Mode	B0_P1_R51_D[6:4]	B0_P1_R8_D2	Minimum MICBIAS_VDD Voltage	MICBIAS Voltage (without load)
MICBIAS_EXT Mode 4	110	0	3.05V	2.85V
MICBIAS_EXT Mode 4	110	1	2.7V	2.37V
MICBIAS_EXT Mode 5	111	0	3.2V	3.00V
MICBIAS_EXT Mode 5	111	1	2.7V	2.50V

8.3.2.8.3 Digital Microphone Function

In addition to supporting analog microphones, the TLV320AIC3268 also interfaces to digital microphones.

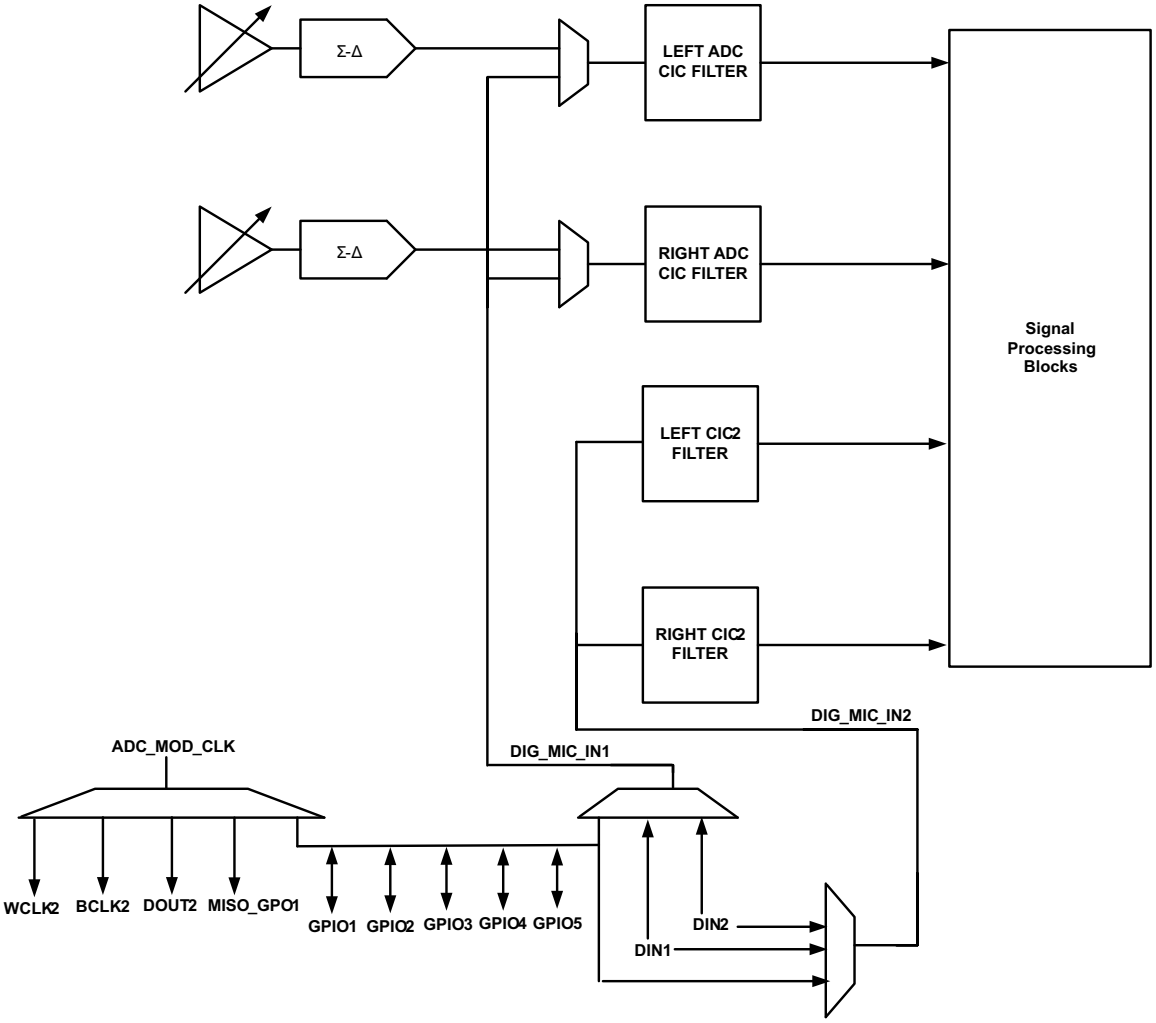


Figure 50. Digital Microphone in TLV320AIC3268

The TLV320AIC3268 outputs internal clock ADC_MOD_CLK on several digital IO terminals. This clock can act as DigMic Clock. The generation of ADC_MOD_CLK is described in Figure 58. The digital microphone data can be accepted on several terminals on both the rising edge as well as the falling edge of the DigMic Clock. Table 17 describes the various ways in which digital microphone interface can be implemented using the several terminal options available in TLV320AIC3268. The TLV320AIC3268 supports two stereo channels of digital microphone. The stereo Digital Mic 1 channel can be muxed with the ADC modulator for analog inputs. The

additional stereo Digital Mic 2 channel is seperately supported. Both these channels use the same DigMic Clock. The Digital Mic 1 channel can be processed either by the built in processing available in PRB_Rx modes or be custom processed in miniDSP. The Digital Mic 2 channel can be processed by using the miniDSP. Each data line configured for digital microphone data can support either mono data or stereo data by using both edges of DigMic Clock. Some of the common digital microphone features as listed in Table 17.

Table 17. Digital Microphone Features

Digital Microphone Feature	Register
Digital Mic 1 enabled for Left ADC CIC Filter	B0_P0_R81_D[5:4]=01
Digital Mic 1 enabled for Right ADC CIC Filter	B0_P0_R81_D[3:2]=01
Digital Mic 2 enabled for Left CIC2 Filter	B0_P0_R112_D[5:4]=01
Digital Mic 2 enabled for Right CIC2 Filter	B0_P0_R112_D[3:2]=01
Digital Mic 1 left channel data valid clock edge control	B0_P4_R100_D[7]
Digital Mic 1 right channel data valid clock edge control	B0_P4_R100_D[6]
Digital Mic 2 left channel data valid clock edge control	B0_P4_R100_D[3]
Digital Mic 2 right channel data valid clock edge control	B0_P4_R100_D[2]
Digital Mic 1 left channel data terminal selection	B0_P4_R101_D[7:4]
Digital Mic 1 right channel data terminal selection	B0_P4_R101_D[3:0]
Digital Mic 2 left channel data terminal selection	B0_P4_R102_D[7:4]
Digital Mic 2 right channel data terminal selection	B0_P4_R102_D[3:0]

Since the digital microphone signals do not pass through the ADC PGA block, the hardware AGC should not be enabled while using digital microphone inputs for left and right ADC channels.

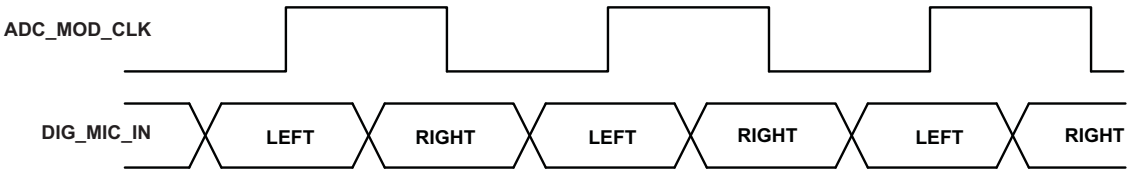


Figure 51. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

Figure 52 is a typical circuit diagram showing one possibility for connecting digital microphones. All terminal assignment options for digital microphones are described in Rows E and J of the terminal muxing tables in and (located in Multifunction Terminals). Depending on the performance of the digital microphone (for example PSRR) and the noise level on the IOVDDx_33 power supply, some additional filtering may be needed for Vmic near the digital microphone for best performance.

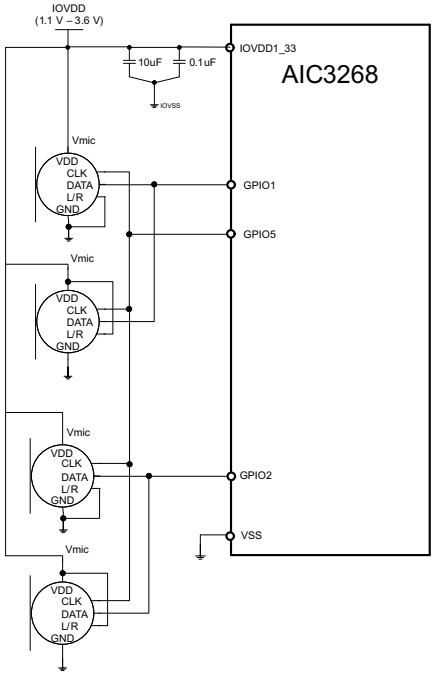


Figure 52. Typical Digital Microphone External Circuitry

8.3.2.8.4 Channel-to-Channel Phase Adjustment

The TLV320AIC3268 has a built-in feature to fine-adjust the phase between the stereo ADC record signals. The phase compensation is particularly helpful to adjust delays when using dual microphones for noise cancellation and other processing. This delay can be controlled in fine amounts in the following fashion.

Delay(7:0) = B0_P0_R85_D[7:0]

Where

$$RIGHT\_ADC\_PHASE\_COMP(t) = RIGHT\_ADC\_OUT(t - t_{pr}) \quad (3)$$

where

$$t_{pr} = \frac{(Delay(4:0) + Delay(6:5) * AOSR * k_f)}{AOSR * ADC\_FS} \quad (4)$$

Where k_f is a function of the decimation filter:

Decimation Filter Type	k_f
A	0.25
B	0.5
C	1

and

$$LEFT\_ADC\_PHASE\_COMP(t) = LEFT\_ADC\_OUT(t - t_{pl}) \quad (5)$$

Where

$$t_{pl} = \frac{Delay(7)}{ADC\_FS} \quad (6)$$

This feature is available for stereo analog inputs or Digital Mic 1 channel.

8.3.2.8.5 Fast Charging AC Capacitors

The value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage. To enable quick charging, the TLV320AIC3268 has modes to speed up the charging of the coupling capacitor. These are controlled by the values in B0_P1_R122_D[1:0].

8.3.2.8.6 Anti Thump

For normal voice or audio recording, the analog input terminals of the TLV320AIC3268, must be AC-coupled to isolate the DC-common mode voltage of the driving circuit from the common-mode voltage of the TLV320AIC3268.

When the analog inputs are not selected for any routing, the input terminals are 3-stated and the voltage on the terminals is undefined. When the unselected inputs are selected for any routing, the input terminals must charge from the undefined voltage to the input common-mode voltage. This charging signal can cause audible artifacts. In order to avoid such artifacts the TLV320AIC3268 also incorporates anti-thump circuitry to allow connection of unused inputs to the common-mode level. This feature is disabled by default, and can be enabled by writing the appropriate values into B0_P1_R58_D[7:0]. The use of this feature in combination with the PTM_R1 setting in B0_P0_R61 when the ADC channel is powered down causes the additional current consumption of 700µA from AVDDx_18 and 125µA from DVDDx_18 in the sleep mode.

8.3.2.8.7 Adaptive Filtering

After the ADC is running, the filter coefficients are locked and cannot be accessed for read or write. However the TLV320AIC3268 offers an adaptive filter mode as well. Setting B40_P0_R1_D2=1 turns on double buffering of the coefficients. In this mode filter coefficients can be updated through the host and activated without stopterminalg and restarting the ADC, enabling advanced adaptive filtering applications.

To support double buffering, all coefficients are stored in two buffers (Buffer A and B). When the ADC is running and adaptive filtering mode is turned on, setting the control bit B40_P0_R1_D0=1 switches the coefficient buffers at the next start of a sampling period. The bit reverts to 0 after the switch occurs. At the same time, the flag B40_P0_R1_D1 toggles.

The flag in B40_P0_R1_D1 indicates which of the two buffers is actually in use.

For B40_P0_R1_D1=0: Buffer A is in use by the ADC engine. For B40_P0_R1_D1=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the ADC, regardless to which buffer the coefficients have been written.

ADC running	Flag, B40_P0_R1_D1	Coefficient Buffer in use	Writing to	Will update
No	0	None	C4, Buffer A	C4, Buffer A
No	0	None	C4, Buffer B	C4, Buffer B
Yes	0	Buffer A	C4, Buffer A	C4, Buffer B
Yes	0	Buffer A	C4, Buffer B	C4, Buffer B
Yes	1	Buffer B	C4, Buffer A	C4, Buffer A
Yes	1	Buffer B	C4, Buffer B	C4, Buffer A

8.3.3 DAC

The TLV320AIC3268 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3268 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3268 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3268 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Usable in single-ended stereo or differential mono mode
  - Analog volume setting with a range of -6 to +14 dB
- Line-out amplifiers
  - Usable in streo single-ended or stereo differential modes
- Class-D speaker amplifier
  - Usable with left, right, or monophonic mix modes
  - Analog volume control with a settings of +6, +12, +18, +24, and +30 dB
- 1 Receiver amplifier
  - Usable in mono differential mode
  - Analog volume setting with a range of -6 to +29 dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function

In addition to the standard set of DAC features the TLV320AIC3268 also offers the following special features:

- Digital auto mute
- Adaptive coefficient update mode

In addition to the above signal processing functions, extensive algorithms are available by programming the miniDSP. For specific details on available algorithms, please contact Texas Instruments.

8.3.3.1 DAC Processing Blocks

The TLV320AIC3268 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

Table 18 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters

The processing blocks can be chosen based on mono or stereo playback requirement and need for additional filtering for frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 18. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P1 (1)	A	Stereo	No	2	No	No	No	8
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P6	A	Left	Yes	6	No	No	No	5

(1) Default

8.3.3.2 DAC Processing Blocks – Details

8.3.3.2.1 2 Biquads, Interpolation Filter A

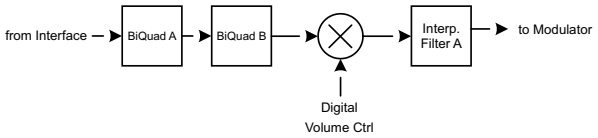


Figure 53. Signal Chain for PRB_P1 (Stereo)

8.3.3.2.2 6 Biquads, 1st order IIR, Interpolation Filter A or B

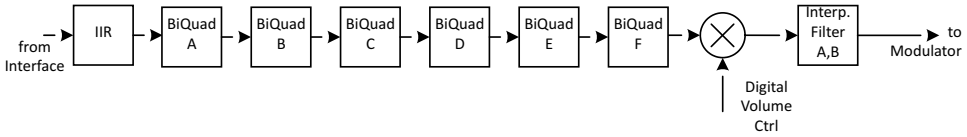


Figure 54. Signal Chain for PRB_P3 (Stereo) and PRB_P6 (Left)

8.3.3.3 User Programmable Filters

The TLV320AIC3268 allows either 3 or 6 user programmable BiQuad filters in DAC channel. Some processing blocks also support a first order IIR filter for dc-blocking.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive coefficient update mode is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering please see Adaptive Filtering.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see DAC Defaults.

8.3.3.3.1 1st-Order IIR Section

The IIR is of first-order and its transfer function is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (7)$$

The frequency response for the 1st order IIR Section with default coefficients is flat. Details on DAC coefficient default values are given in DAC Defaults.

Table 19. DAC IIR Filter Coefficients

Filter	Filter Coefficient	DAC Coefficient Left Channel	DAC Coefficient Right Channel
1st Order IIR	N0	C1 (B80_P1_R12-R14)	C36 (B80_P3_R32-R34)
	N1	C2 (B80_P3_R16-R18)	C37 (B80_P3_R36-R38)
	D1	C3 (B80_P3_R20-R22)	C38 (B80_P3_R40-R42)

8.3.3.3.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2 * N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2 * D_1 z^{-1} - D_2 z^{-2}} \quad (8)$$

The frequency response for each biquad section with default coefficients is flat at a gain of 0dB. Details on DAC coefficient default values are given in DAC Defaults.

Table 20. DAC Biquad Filter Coefficients

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD A	N0	C4 (B80_P1_R24-R26)	C39 (B80_P2_R44-R46)
	N1	C5 (B80_P1_R28-R30)	C40 (B80_P2_R48-R50)
	N2	C6 (B80_P1_R32-R34)	C41 (B80_P2_R52-R54)
	D1	C7 (B80_P1_R36-R38)	C42 (B80_P2_R56-R58)
	D2	C8 (B80_P1_R40-R42)	C43 (B80_P2_R60-R62)
BIQUAD B	N0	C9 (B80_P1_R44-R46)	C44 (B80_P2_R64-R66)
	N1	C10 (B80_P1_R48-R50)	C45 (B80_P2_R68-R70)
	N2	C11 (B80_P1_R52-R54)	C46 (B80_P2_R72-R74)
	D1	C12 (B80_P1_R56-R58)	C47 (B80_P2_R76-R78)
	D2	C13 (B80_P1_R60-R62)	C48 (B80_P2_R80-R82)
BIQUAD C	N0	C14 (B80_P1_R64-R66)	C49 (B80_P2_R84-R86)
	N1	C15 (B80_P1_R68-R70)	C50 (B80_P2_R88-R90)
	N2	C16 (B80_P1_R72-R74)	C51 (B80_P2_R92-R94)
	D1	C17 (B80_P1_R76-R78)	C52 (B80_P2_R96-R98)
	D2	C18 (B80_P1_R80-R82)	C53 (B80_P2_R100-R102)
BIQUAD D	N0	C19 (B80_P1_R84-R86)	C54 (B80_P2_R104-R106)
	N1	C20 (B80_P1_R88-R90)	C55 (B80_P2_R108-R110)
	N2	C21 (B80_P1_R92-R94)	C56 (B80_P2_R112-R114)
	D1	C22 (B80_P1_R96-R98)	C57 (B80_P2_R116-R118)
	D2	C23 (B80_P1_R100-R102)	C58 (B80_P2_R120-R122)
BIQUAD E	N0	C24 (B80_P1_R104-R106)	C59 (B80_P2_R124-R126)
	N1	C25 (B80_P1_R108-R110)	C60 (B80_P3_R8-R10)
	N2	C26 (B80_P1_R112-R114)	C61 (B80_P3_R12-R14)
	D1	C27 (B80_P1_R116-R118)	C62 (B80_P3_R16-R18)
	D2	C28 (B80_P1_R120-R122)	C63 (B80_P3_R20-R22)
BIQUAD F	N0	C29 (B80_P1_R124-R126)	C64 (B80_P3_R24-R26)
	N1	C30 (B80_P2_R8-R10)	C65 (B80_P3_R28-R30)
	N2	C31 (B80_P2_R12-R14)	C66 (B80_P3_R32-R34)
	D1	C32 (B80_P2_R16-R18)	C67 (B80_P3_R36-R38)
	D2	C33 (B80_P2_R20-R22)	C68 (B80_P3_R40-R42)

8.3.3.4 Interpolation Filters

8.3.3.4.1 Interpolation Filter A

Filter A is designed for an Fs up to 48ksps with a flat passband of 0kHz–20kHz.

Table 21. DAC Interpolation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45f_S	±0.015	dB
Filter Gain Stop Band	0.55Fs… 7.455f_S	–65	dB
Filter Group Delay		21/f_S	s

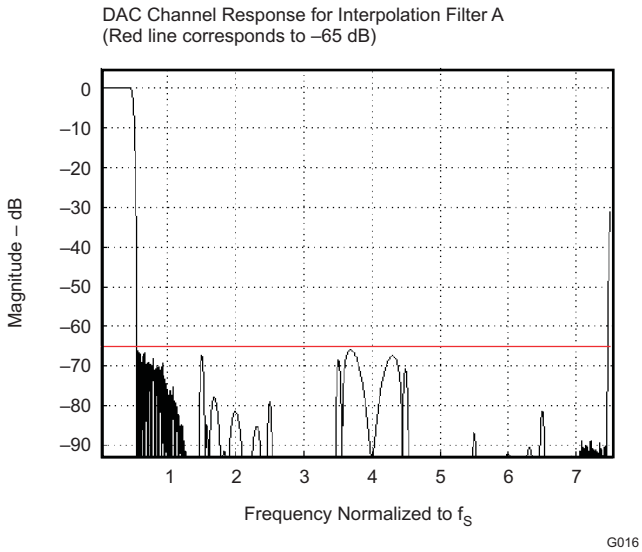


Figure 55. DAC Interpolation Filter A, Frequency Response

8.3.3.4.2 Interpolation Filter B

Filter B is specifically designed for an Fs of above 96ksps. Thus, the flat pass-band region easily covers the required audio band of 0-20kHz.

Table 22. DAC Interpolation Filter B, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45f_S	±0.015	dB
Filter Gain Stop Band	0.55Fs… 3.45f_S	–58	dB
Filter Group Delay		18/f_S	s

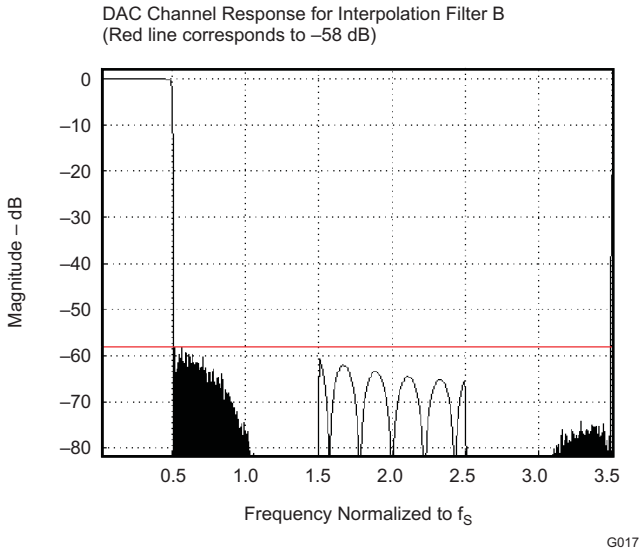


Figure 56. Channel Interpolation Filter B, Frequency Response

8.3.3.4.3 Interpolation Filter C

Filter C is specifically designed for the 192ksps mode. The pass band extends up to 0.40*Fs (corresponds to 80kHz), more than sufficient for audio applications.

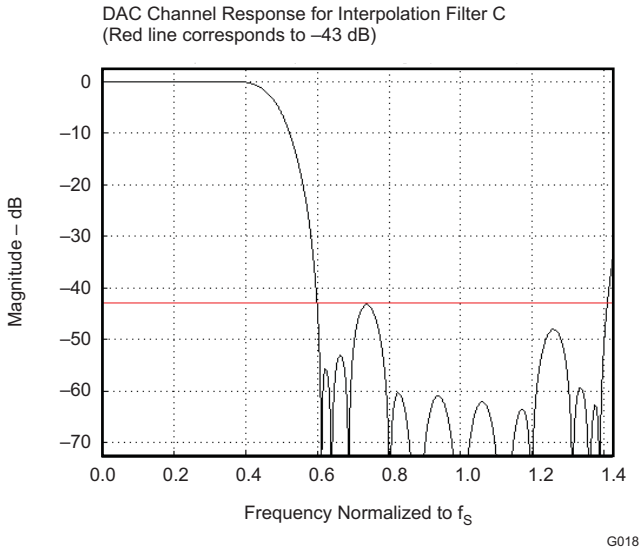


Figure 57. DAC Interpolation Filter C, Frequency Response

Table 23. DAC Interpolation Filter C, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.35f_S	±0.03	dB
Filter Gain Stop Band	0.60Fs… 1.4f_S	–43	dB
Filter Group Delay		13/f_S	s

8.3.3.5 DAC Gain Setting

8.3.3.5.1 PowerTune Modes

As part of the PowerTune strategy, the analog properties of the DAC are adjusted. As a consequence, the full-scale signal swing achieved at the headphone outputs must be adjusted.

Please see Table 24 for the proper gain compensation values across the different combinations.

Table 24. DAC Gain versus PowerTune Modes

DAC PowerTune Mode Control	PowerTune Mode	Headphone Gain	
Page 1,Register 3/4, Bits D4-D2)		CM = 0.75V, Gain for 375mV$_{RMS}$ output swing at 0dB full scale input	CM = 0.9V, Gain for 500mV$_{RMS}$ output swing at 0dB full scale input
000	PTM_P3, PTM_P4	0	0
001	PTM_P2	4	4
010	PTM_P1	14	14

8.3.3.5.2 Digital Volume Control

The TLV320AIC3268 signal processing blocks incorporate a digital volume control block that can control the volume of the playback signal from +24dB to –63.5dB in steps of 0.5dB. These can be controlled by writing to B0_P0_R65 and B0_P0_R66. The volume control of left and right channels by default can be controlled independently, but by programming B0_P0_R64_D[1:0], they can be made interdependent. The volume changes are soft-stepped in steps of 0.5dB to avoid audible artifacts during gain change. The rate of soft-stepping can be controlled by programming B0_P0_R63_D[1:0] to either one step per frame (DAC_FS) or one step per 2 frames. The soft-stepping feature can also be entirely disabled. During soft-stepping the value of the actual applied gain would differ from the programmed gain in register. The TLV320AIC3268 gives a feedback to the user in form of register readable flag to indicate that soft-stepping is currently in progress. The flags for left and right channels can be read back by reading B0_P0_R38_D4 and B0_P0_R38_D0 respectively. A value of 0 in these flags indicates a soft-stepping operation in progress, and a value of 1 indicates that soft-stepping has completed. A soft-stepping operation comes into effect during a) power-up, when the volume control soft-steps from –63.5dB to programmed gain value b) volume change by user when DAC is powered up and c) power-down, when the volume control block soft-steps to –63.5dB before powering down the channel.

8.3.3.6 DAC Special Functions

8.3.3.6.1 Digital Auto Mute

The TLV320AIC3268 also incorporates a special feature, in which the DAC channel is auto-muted when a continuous stream of DC-input is detected. When using PRB_Px modes, the Data Input 1 (L1,R1) ports of miniDSP_D are monitoted for DC-inputs. Signals routed to Data Input 1 port is controlled by configuring B0_P4_R118_D[5:4].By default, this feature is disabled. It can be enabled by writing a non-000 value into B0_P0_R64_D[6:4]. The non-zero value controls the duration of continuous stream of DC-input before which the auto-mute feature takes effect. This feature is especially helpful for eliminating high-frequency-noise power being delivered into the load even during silent periods of speech or music.

8.3.3.6.2 Adaptive Filtering

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However, the TLV320AIC3268 offers an adaptive filter mode as well, and the DAC contains two separate adaptive filter coefficient banks (Primary Adaptive Bank in Book 80, and Secondary Adaptive Bank in Book 82). Setting B80_P0_R1_D2=1 for the Primary Adaptive Bank will turn on double buffering of the coefficients. Similarly, setting B82_P0_R1_D2=1 will turn on double buffering of the coefficients in the Secondary Adaptive Bank. In this mode, filter coefficients can be updated through the host, and activated without stopping and restarting the DAC. This enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (Buffers A and B). When the DAC is running and adaptive filtering mode is turned on, setting the control bit B80_P0_R1_D0=1 (B82_P0_R1_D0=1 if using Secondary Bank) switches the coefficient buffers at the next start of a sampling period. This bit is set back to 0 after the switch occurs. At the same time, the flag B80_P0_R1_D1 (B82_P0_R1_D1 if using Secondary Bank) toggles.

The flag in B80_P0_R1_D1 indicates which of the two buffers in the Primary Bank is actually in use.

B80_P0_R1_D1=0: Buffer A is in use by the DAC engine, Bit D1=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless to which buffer the coefficients have been written.

DAC running	B80_P0_R1_D1 for Primary Bank (B82_P0_R1_D1 for Secondary Bank)	Coefficient Buffer in use	Writing to	Will update
No	0	None	C1, Buffer A	C1, Buffer A
No	0	None	C1, Buffer B	C1, Buffer B
Yes	0	Buffer A	C1, Buffer A	C1, Buffer B
Yes	0	Buffer A	C1, Buffer B	C1, Buffer B
Yes	1	Buffer B	C1, Buffer A	C1, Buffer A
Yes	1	Buffer B	C1, Buffer B	C1, Buffer A

The user programmable coefficients C1 to C70 are defined on B80_P1-P3 for Buffer A and B80_P9-P11 for Buffer B. For the Secondary Bank, the coefficients are located on similar pages on Book 82.

8.3.4 Clock Generation and PLL

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output terminal and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3268.

The ADC_CLKIN and DAC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections.

The TLV320AIC3268 supports a wide range of options for generating clocks for the ADC and DAC sections as well as the interface and other control blocks as shown in Figure 58. The clocks for the ADC and the DAC require a source reference clock. In the TLV320AIC3268 the ADC and DAC clock-trees can have different root clocks. These clocks can be provided on a variety of device terminals such as MCLK, BCLK1, BCLK2, GPIO1, GPIO2 and GPIO3, and the onchip high-frequency reference clock (HF_REF_CLK) and high-frequency oscillator clock (HF_OSC_CLK) can also be provided as sources. The source reference clock for the ADC can be chosen by programming the ADC_CLKIN value on B0_P0_R4_D[3:0]. The source reference clock for the DAC can be chosed by programming the DAC_CLKIN value on B0_P0_R4_D[7:4]. The ADC_CLKIN and DAC_CLKIN can then be routed through highly flexible clock dividers shown in Figure 58 to generate the various clocks required for the ADC, DAC, and miniDSP sections. In the event that the desired audio miniDSP clocks cannot be generated from the reference clocks coming from the device terminals listed above, the TLV320AIC3268 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from ADC_CLKIN and DAC_CLKIN, the TLV320AIC3268 provides several programmable clock dividers to help achieve a variety of sampling rates for the ADC and DAC, as well as clocks for the miniDSP sections.

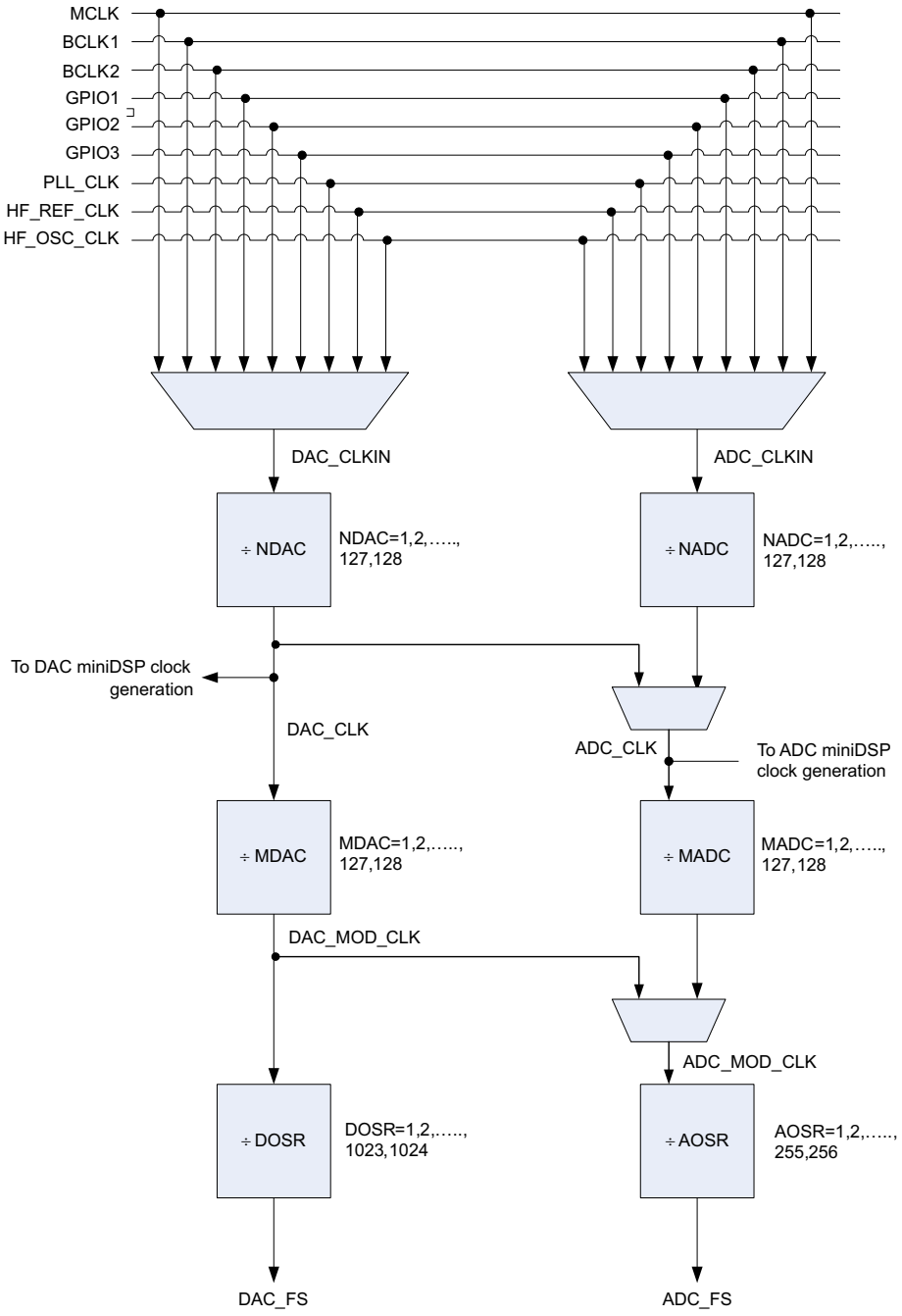


Figure 58. Clock Distribution Tree

The DAC and ADC clocks are obtained as follows:

$$DAC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MDAC \times DOSR} \quad (9)$$

$$DAC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MDAC} \quad (10)$$

$$ADC\_f_S = \frac{ADC\_CLKIN}{NADC \times MADC \times AOSR} \quad (11)$$

$$ADC\_MOD\_CLK = \frac{ADC\_CLKIN}{NADC \times MADC} \quad (12)$$

The MUX settings in the ADC clock tree allow alternative clock settings:

$$ADC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MADC \times AOSR}$$

or

$$ADC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MDAC \times AOSR} \quad (13)$$

$$ADC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MADC}$$

or

$$ADC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MDAC} \quad (14)$$

By default ADC_CLK = DAC_CLK and ADC_MOD_CLK = DAC_MOD_CLK.

Table 25. DAC CLKIN and ADC CLKIN Clock Dividers

Divider	Bits	Range
NDAC	B0_P0_R11_D[6:0]	1, 2, … 127, 128
MDAC	B0_P0_R12_D[6:0]	1, 2, … 127, 128
DOSR	B0_P0_R13_D[1:0] and B0_P0_R14_D[7:0]	1, 2, … 1023, 1024
NADC	B0_P0_R18_D[6:0]	1, 2, … 127, 128
MADC	B0_P0_R19_D[6:0]	1, 2, … 127, 128
AOSR	B0_P0_R20_D[7:0]	1, 2, … 255, 256

The registers used for DAC and ADC clock selection are listed in Table 26.

Table 26. DAC and ADC Clock Selectors

Selector	Bits	Inputs
DAC_CLKIN	B0_P0_R4_D[7:4]	MCLK1, MCLK2, BCLK1, GPIO1, PLL_CLK, BCLK2, GPI1, HR_REF_CLK, HF_OSC_CLK, GPIO2, GPI2
ADC_CLKIN	B0_P0_R4_D[3:0]	MCLK1, MCLK2, BCLK1, GPIO1, PLL_CLK, BCLK2, GPI1, HR_REF_CLK, HF_OSC_CLK, GPIO2, GPI2
ADC_CLK	B0_P0_R18_D7	NDAC output (DAC_CLK), NADC output
ADC_MOD_CLK	B0_P0_R19_D7	MDAC output (DAC_MOD_CLK), MADC output

The DAC Modulator is clocked by DAC_MOD_CLK. For proper power-up of the DAC Channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (B0_P0_R11_D7=1 and B0_P0_R12_D7=1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in B0_P0_R37_D7 for the Left DAC and B0_P0_R37_D3 for the Right DAC. When both flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider.

The ADC modulator is clocked by ADC_MOD_CLK. For proper power-up of the ADC Channel, these clocks are enabled by the NADC and MADC clock dividers (B0_P0_R18_D7=1 and B0_P0_R19_D7=1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NADC and MADC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in B0_P0_R36_D6 for the Left ADC and B0_P0_R36_D2 for the Right ADC. When both flags indicate power-down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK is derived from the NDAC divider output, the NDAC must be kept powered up till the power-down status flags for ADC do not indicate that the ADC is still in the process of powering down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_FS is needed (that is when WCLK is generated by TLV320AIC3268 or AGC is enabled) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, all the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.

The TLV320AIC3268 also has options for routing some of the internal clocks to the output terminals of the device to be used as general purpose clocks in the system.

For example, the TLV320AIC3268 can be configured to drive the bit clock signals ASI1_BCLK_OUT, ASI2_BCLK_OUT, and ASI3_BCLK_OUT on the three serial interfaces as shown in Figure 59.

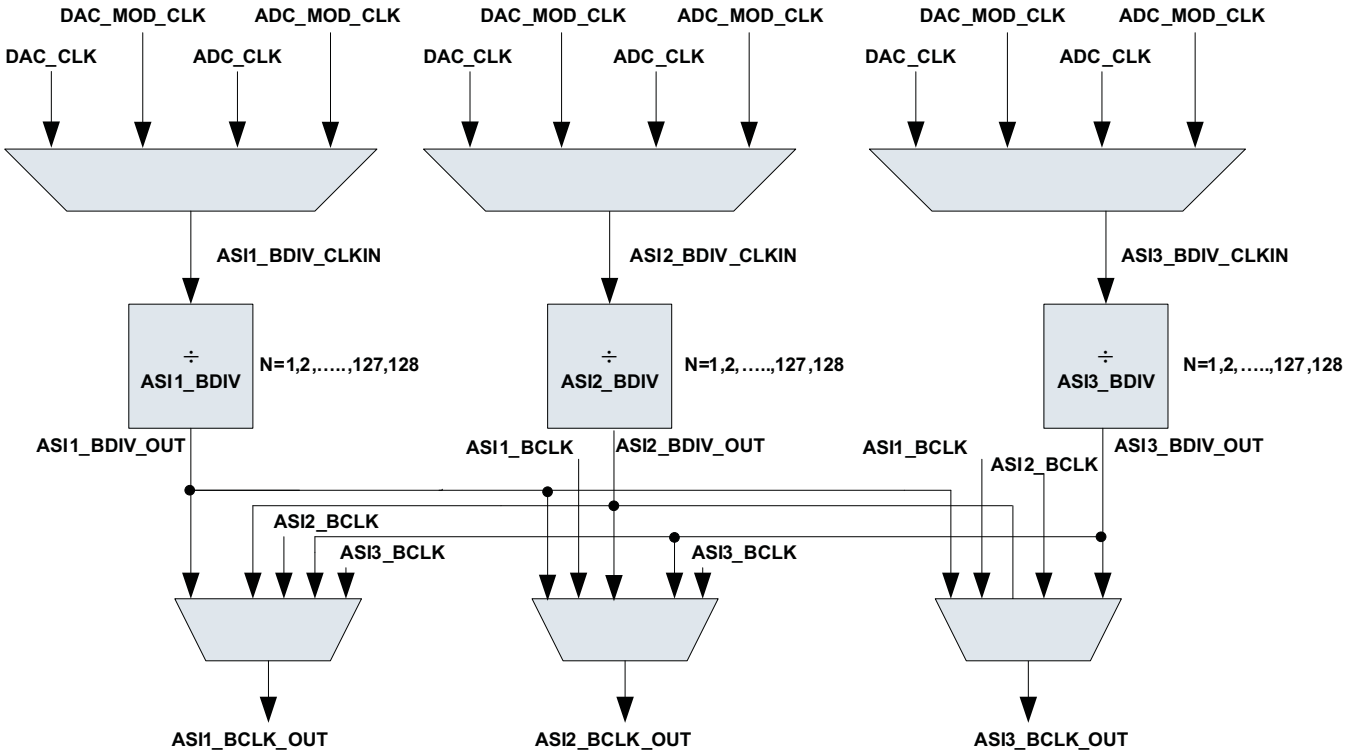


Figure 59. Bit Clock Output Options for ASI1, ASI2, and ASI3

When TLV320AIC3268 is configured to drive ASI1_BCLK_OUT, the clock signal can be selected via B0_P4_R14_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI2_BCLK Input, or ASI3_BCLK Input.

When TLV320AIC3268 is configured to drive ASI2_BCLK_OUT, the clock signal can be selected via B0_P4_R30_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK Input, or ASI3_BCLK Input.

When TLV320AIC3268 is configured to drive ASI3_BCLK_OUT, the clock signal can be selected via B0_P4_R46_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, or ASI2_BCLK.

ASI1_BDIV_OUT is a divided value of ASI1_BDIV_CLKIN, where the division value can be programmed in B0_P4_R12_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R12_D7. The ASI1_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI1_BDIV_CLKIN mux in B0_P4_R11_D[1:0].

ASI2_BDIV_OUT is a divided value of ASI2_BDIV_CLKIN, where the division value can be programmed in B0_P4_R28_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R28_D7. The ASI2_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI2_BDIV_CLKIN mux in B0_P4_R27_D[1:0].

ASI3_BDIV_OUT is a divided value of ASI3_BDIV_CLKIN, where the division value can be programmed in B0_P4_R44_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R44_D7. The ASI3_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI3_BDIV_CLKIN mux in B0_P4_R43_D[1:0].

The TLV320AIC3268 can also be configured to provide the world clocks for ASI1, ASI2, and ASI3 as shown in Figure 60.

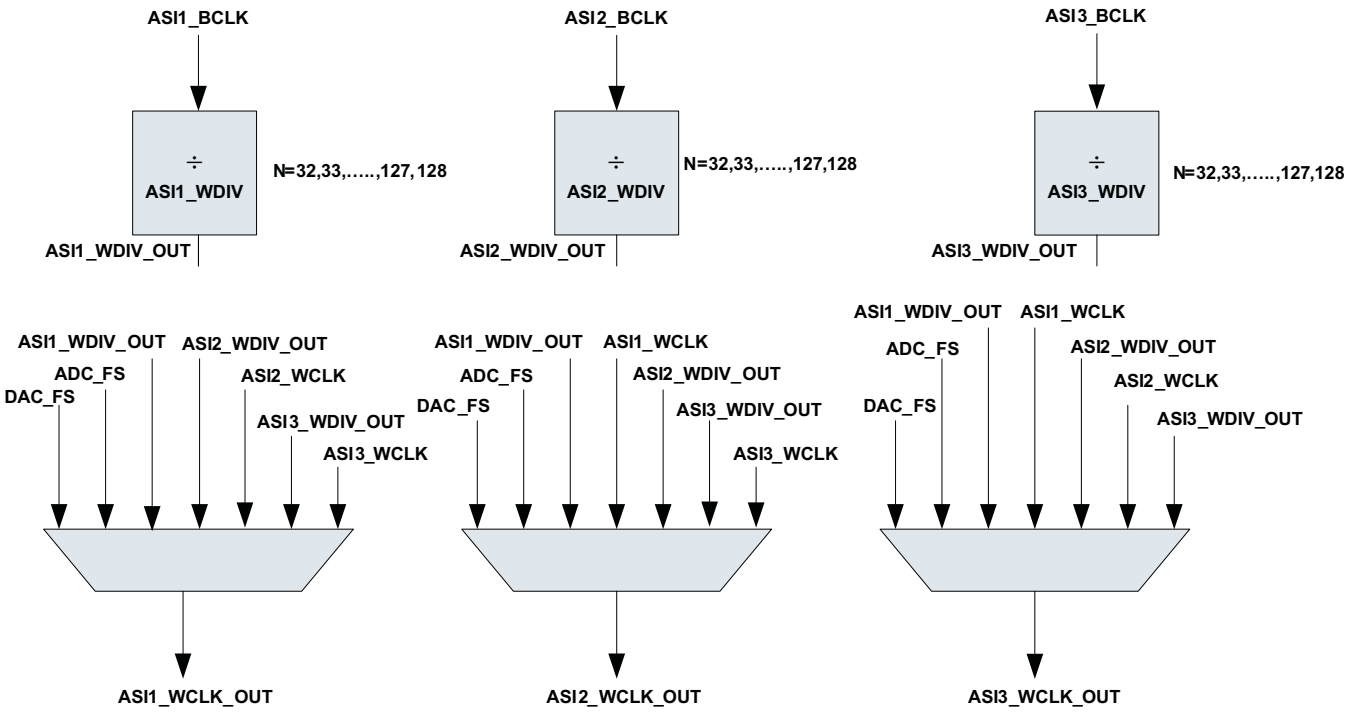


Figure 60. Word Clock Options for ASI1, ASI2, and ASI3

ASI1_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI2_WCLK Input, and ASI3_WCLK Input using B0_P4_R14_D[2:0]. ASI1_WDIV_OUT is driven as a divided value of ASI1_BCLK, where the division can be programmed in B0_P4_R13_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R13_D7.

ASI2_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI1_WCLK Input, and ASI3_WCLK Input using B0_P4_R30_D[2:0]. ASI2_WDIV_OUT is driven as a divided value of ASI2_BCLK, where the division can be programmed in B0_P4_R29_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R29_D7.

ASI3_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI1_WCLK Input, and ASI2_WCLK Input using B0_P4_R46_D[2:0]. ASI3_WDIV_OUT is driven as a divided value of ASI3_BCLK, where the division can be programmed in B0_P4_R45_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R45_D7.

The bit clock and work clock dividers are summarized in Table 27. The bit clock and word clock selectors are summarized in Table 28.

Table 27. ASI1, ASI2, and ASI3 Bit and Word Clock Dividers

Divider	Bits	Range
ASI1_BDIV	B0_P4_R12_D[6:0]	1, 2, … 127, 128

Table 27. ASI1, ASI2, and ASI3 Bit and Word Clock Dividers (continued)

Divider	Bits	Range
ASI2_BDIV	B0_P4_R28_D[6:0]	1, 2, … 127, 128
ASI3_BDIV	B0_P4_R44_D[6:0]	1, 2, … 127, 128
ASI1_WDIV	B0_P4_R13_D[6:0]	32, 33, … 127, 128
ASI2_WDIV	B0_P4_R29_D[6:0]	32, 33, … 127, 128
ASI3_WDIV	B0_P4_R45_D[6:0]	32, 33, … 127, 128

Table 28. ASI1, ASI2, and ASI3 Bit and Word Clock Selection

Selector	Bits	Inputs
ASI1_BCLK_OUT	B0_P4_R14_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI2_BCLK, ASI3_BCLK
ASI2_BCLK_OUT	B0_P4_R30_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, ASI3_BCLK
ASI3_BCLK_OUT	B0_P4_R46_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, ASI2_BCLK
ASI1_BDIV_CLKIN	B0_P4_R11_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI2_BDIV_CLKIN	B0_P4_R27_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI3_BDIV_CLKIN	B0_P4_R43_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI1_WCLK_OUT	B0_P4_R14_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI2_WCLK, ASI3_WCLK
ASI2_WCLK_OUT	B0_P4_R30_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI1_WCLK, ASI3_WCLK
ASI3_WCLK_OUT	B0_P4_R46_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI1_WCLK, ASI2_WCLK

Additionally a general purpose clock CLKOUT can be driven out on DOUT1, WCLK2, BCLK2, GPIO1, GPIO2, or GPO1 according to the settings in Table 29.

Table 29. CLKOUT Selection

Clock Output	Bits
DOUT1	B0_P4_R67_D[4:1] = ’0011’
WCLK2	B0_P4_R69_D[5:2] = ’0100’
BCLK2	B0_P4_R70_D[5:2] = ’0100’
GPIO1	B0_P4_R86_D[6:2] = ’00100’
GPIO2	B0_P4_R87_D[6:2] = ’00100’
MISO_GPO1	B0_P4_R96_D[4:1] = ”0011’

This clock can be a divided down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to B0_P0_R22_D[6:0], and this CDIV clock divider can be powered on by setting B0_P4_R22_D7. The CDIV_CLKIN can itself be programmed as one of the clocks among the list shown in Figure 61. This can be controlled by programming the mux in B0_P0_R21_D[3:0].

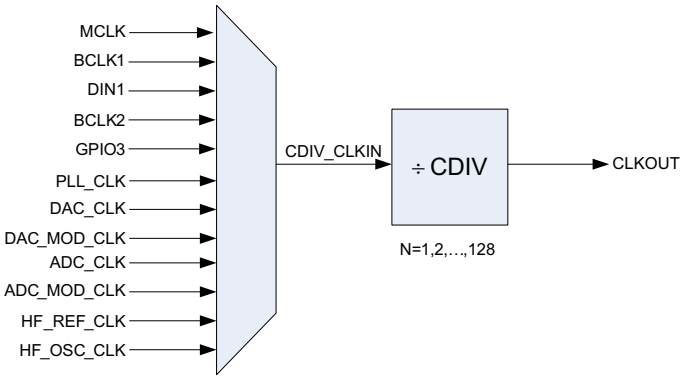


Figure 61. General Purpose Clock Output Options

Table 30. Maximum TLV320AIC3268 Clock Frequencies

	DVDD_18 ≥ 1.26V	DVDD_18 ≥ 1.65V	DVDD_18 ≥ 1.71V
ADC_CLKIN	50MHz	137MHz	137MHz
DAC_CLKIN	50MHz	137MHz	137MHz
ADC_CLK	50MHz	70MHz	70MHz
ADC_miniDSP_CLK	37.5MHz	63.0MHz	69.0MHz
ADC_MOD_CLK	6.758MHz	6.758MHz	6.758MHz
ADC_FS	0.192MHz	0.192MHz	0.192MHz
DAC_CLK	50.0MHz	70MHz	70MHz
DAC_miniDSP_CLK	35.0MHz	59.0MHz	62.5MHz
DAC_MOD_CLK	6.758MHz	6.758MHz	6.758MHz
DAC_FS	0.192MHz	0.192MHz	0.192MHz
ASI1_BDIV_CLKIN, ASI2_BDIV_CLKIN, ASI3_BDIV_CLKIN	50MHz	70MHz	70MHz
CDIV_CLKIN	50MHz	137MHz	137MHz

8.3.4.1 PLL

The TLV320AIC3268 has an on-chip PLL to generate the clock frequency for the audio ADC, DAC, and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL Clocking and muxing is shown in Figure 62.

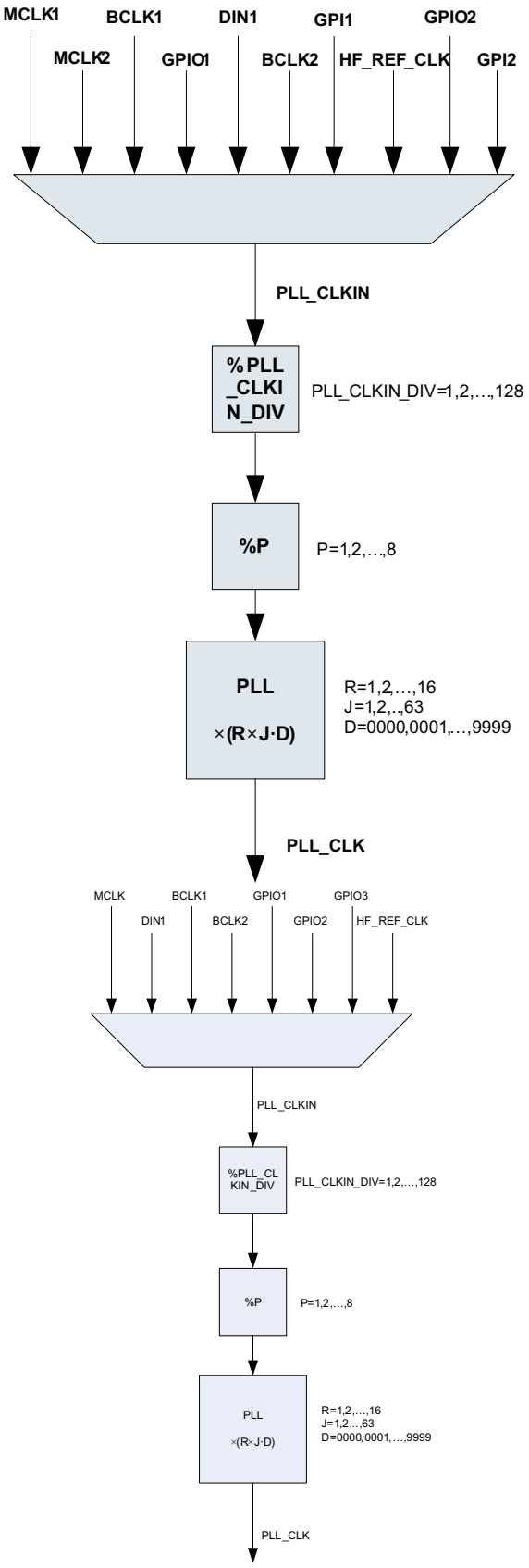


Figure 62. PLL Clocking and Mux

The PLL input supports clocks varying from 512kHz to 20MHz and is register programmable to enable generation of required sampling rates with fine resolution. The PLL can be turned on by writing to B0_P0_R6_D7. When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation PLL_CLK = (PLL_CLKIN x R x J.D)/(PxPLL_CLKIN_DIV)

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{PxPLL\_CLKIN\_DIV} \quad (15)$$

R = 1, 2, … 16.

J = 1, 2, 3, 4,… 63, and D = 0, 1, 2, 3, 4, … 9999

P = 1, 2, 3, 4, … 8

PLL_CLKIN_DIV = 1, 2, … 128.

R, J, D, P, and PLL_CLKIN_DIV are register programmable.

The PLL can be programmed via B0_P0_R6-R10. The PLL can be turned on via B0_P0_R6_D7. The variable P can be programmed via B0_P0_R6_D[6:4]. The default register value for P is 1. The variable R can be programmed via B0_P0_R6_D[3:0]. The default register value for R is 1. The variable J can be programmed via B0_P0_R7_D[5:0]. The default register value for J is 4. The variable D is 12-bits, programmed into two registers. The MSB portion can be programmed via B0_P0_R8_D[5:0], and the LSB portion is programmed via B0_P0_R9_D[7:0]. The default register value for D is 0. The PLL_CLKIN_DIV value can be programmed via B0_P0_R10_D[6:0]. The default register value for PLL_CLKIN_DIV is 1.

When the PLL is enabled the following conditions must be satisfied

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512\,kHz \le \frac{PLL\_CLKIN}{P \times PLL\_CLKIN\_DIV} \le 20\,MHz \quad (16)$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10\,MHz \le \frac{PLL\_CLKIN}{P \times PLL\_CLKIN\_DIV} \le 20\,MHz \quad (17)$$

In the TLV320AIC3268 the PLL_CLK supports a wide range of output clock values, based on register settings and power-supply conditions.

Table 31. PLL_CLK Frequency Range

AVdd	PLL Mode B0_P0_R5_D6	Min PLL_CLK frequency (MHz)	Max PLL_CLK frequency (MHz)
≥1.5V	0	80	103
	1	95	110
≥1.65V	0	80	118
	1	92	123
≥1.80V	0	80	132
	1	92	137

The PLL can be powered up independently from the ADC and DAC blocks, and can also be used as a general purpose PLL by selecting its output as an input to the General Purpose Output Clock mux (enabling routing to a variety of digital output terminals). After powering up the PLL, PLL_CLK is available typically after 10ms. The PLL output frequency is controlled by J.D and R dividers

PLL Divider	Bits
J	B0_P0_R7_D[5:0]
D	B0_P0_R8_D[5:0] and B0_P0_R9_D[7:0]
R	B0_P0_R6_D[3:0]

The D-divider value is 14-bits wide and is controlled by 2 registers. For proper update of the D-divider value, B0_P0_R8 must be programmed first followed immediately by B0_P0_R9. Unless the write to B0_P0_R9 is completed, the new value of D will not take effect.

The clocks for codec and various signal processing blocks, ADC_CLKIN and DAC_CLKIN can be generated from MCLK, BCLK1, GPIO1, BCLK2, GPIO3, HF_REF_CLK, HF_OSC_CLK, GPIO2, GPIO6, BCLK3 or PLL_CLK (B0_P0_R4_D[7:0]).

If the ADC_CLKIN and/or the DAC_CLKIN are derived from the PLL, then the PLL must be powered up first and powered down last.

Table 32 lists several example cases of typical MCLK rates and how to program the PLL to achieve a sample rate Fs of either 44.1kHz or 48kHz.

Table 32. PLL Example Configurations

Fs = 44.1kHz											
MCLK (MHz)	**PLL_CLKIN_DIV**	**PLLP**	**PLLR**	**PLLJ**	**PLLD**	**MADC**	**NADC**	**AOSR**	**MDAC**	**NDAC**	**DOSR**
2.8224	1	1	3	10	0	3	5	128	3	5	128
5.6448	1	1	3	5	0	3	5	128	3	5	128
12	1	1	1	7	560	3	5	128	3	5	128
13	1	1	2	4	2336	13	3	64	4	6	104
16	1	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	1	4	4100	3	5	128	3	5	128
48	1	4	1	7	560	3	5	128	3	5	128
Fs = 48kHz											
2.048	1	1	3	14	0	2	7	128	7	2	128
3.072	1	1	4	7	0	2	7	128	7	2	128
4.096	1	1	3	7	0	2	7	128	7	2	128
6.144	1	1	2	7	0	2	7	128	7	2	128
8.192	1	1	4	3	0	2	8	128	4	4	128
12	1	1	1	7	1680	2	7	128	7	2	128
16	1	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	1	4	4800	2	7	128	7	2	128
48	1	4	1	7	1680	2	7	128	7	2	128

8.3.4.2 Low Frequency Reference Clock

To extend the frequency locking range of the on-chip PLL to an external clock at low frequencies, a clock frequency multiplier is used to generate its output clock with the frequency K times of its input reference clock frequency for the PLL to lock, where K is a 28-bit value of the control register bits {B0_P0_R25_D[3:0], B0_P1_R26, B0_P0R27, B0_P0_R28}. The reference clock source can be selected with the control register bits, B0_P0_R24_D[7:4]. The clock routing for the low frequency clock is shown in Figure 63.

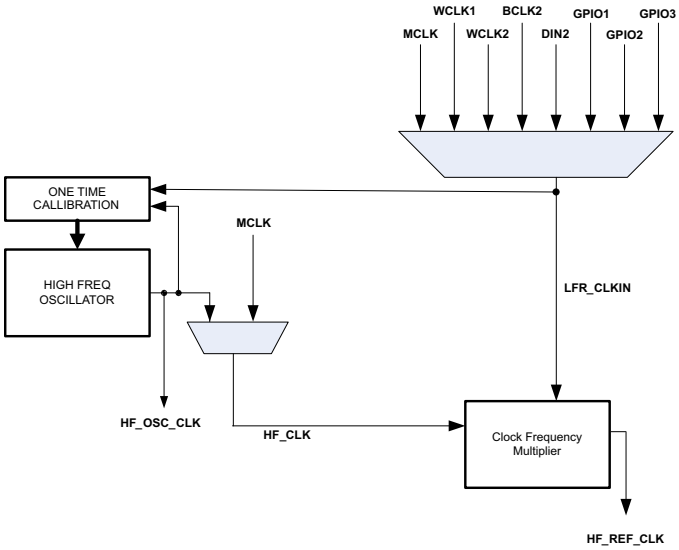


Figure 63. Low-Frequency Clocking

The output clock, HF_REF_CLOCK, is generated by delta-sigma modulation with a high frequency clock, HF_CLK. The source of HF_CLK can be setup by programming the control bits, B0_P0_R24_R[3:0]. If the on-chip high frequency oscillator clock, HF_OSC_CLK, is selected as the source, it is recommended to calibrate the oscillator clock by following the proper calibration procedure before turning on the clock multiplier.

The HF_OSC_CLK can have large device-to-device variation of its default frequency. For proper functioning, the HF_OSC_CLK can be calibrated with respect to the LFR_CLKIN. This calibration happens at power-up of the block when this feature is enabled (HF_OSC_CLK is used by any other function). By default this calibration is enabled and if so desired can be disabled by writing B0_P0_R29_D5 = '0'. For calibrating the HF_OSC_CLK the 26-bit ratio of frequencies (Desired HF_OSC_CLK freq / Frequency of LFR_CLKIN) can be programmed in B0_P0_R29_D[1:0], B0_P0_R30_D[7:0], B0_P0_R31_D[7:0], and B0_P0_R32_D[7:0]. This ratio must be programmed before enabling this block. Also, the LFR_CLKIN must be present when the HF_OSC_CLK is enabled, and the LFR_CLKIN frequency should be less than 50 kHz. This calibration is an approximate calibration, and the frequency of HF_OSC_CLK will approximately equal Programmed Ratio * LFR_CLKIN frequency. The error can be approx ±7MHz. The desired frequency should ideally be kept between 50MHz and 57.5MHz for good audio performance. Once the calibration is over, the calibrated clock will be available for use by other blocks. The HF_OSC_CLK has an additional programmability by which this block can be used even when AVDD1_18 supply is not powered up. This can be useful when a free running clock is required when AVDD1_18 is not powered as no other analog blocks may be powered up. This feature can be controlled by B0_P0_R29_D6.

For a better quality of the PLL clock, the clock multiplier output should be set at higher frequency by choosing a higher multiplication value of K, if there are multiple options. But the multiplied frequency should not be higher than ¼ times of HF_REF_CLK frequency and the frequency has to be within the PLL locking range, 10-20MHz for D≠0 and 512kHz – 20MHz for D=0. To select HF_REF_CLK as the PLL reference, B0_P0_R5_D[5:2] should be set as '0110'.

8.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TLV320AIC3268 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with a good PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF_AUDIO terminal to analog ground (VSS).

To achieve low power consumption, this audio reference block is powered down when all analog blocks inside the device are powered down. In this condition, the VREF_AUDIO terminal is 3-stated. On powerup of any analog block, the audio reference block is also powered up and the VREF_AUDIO terminal settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF_AUDIO terminal). This time is approximately equal to 1 second when using a 1µF decoupling capacitor. In the event that a faster power-

up is required, either the audio reference block can be kept powered up (even when no other analog block is powered up) by programming B0_P1_R122_D2 = 1. However, in this case, an additional 100µA of current from AVDDx_18 is consumed. Additionally, to achieve a faster powerup, a fast-charge option is also provided where the charging time can be controlled between 40ms and 120ms by programming B0_P1_R122_D[1:0]. By default, the fast charge option is enabled.

In addition, the TLV320AIC3268 can also generate a separate 1.25V DC reference which is utilized by the SAR ADC for measurement. This SAR reference voltage must also be filtered externally using a minimum 1µF capacitor connected from the VREF_SAR terminal to analog ground (AVSS).

To achieve low power consumption, this SAR reference block is powered down by default when SAR conversations are not occurring. The system could utilize this reference voltage outside of SAR ADC conversions by powering it continuously by programming B0_P3_R6_D5 =0.

8.3.6 SAR ADC

This section describes how to use the SAR ADC for the functions:

- Temperature measurement
- Battery measurement
- Auxiliary voltage measurement

The analog inputs of the TLV320AIC3268 are shown in Figure 64.

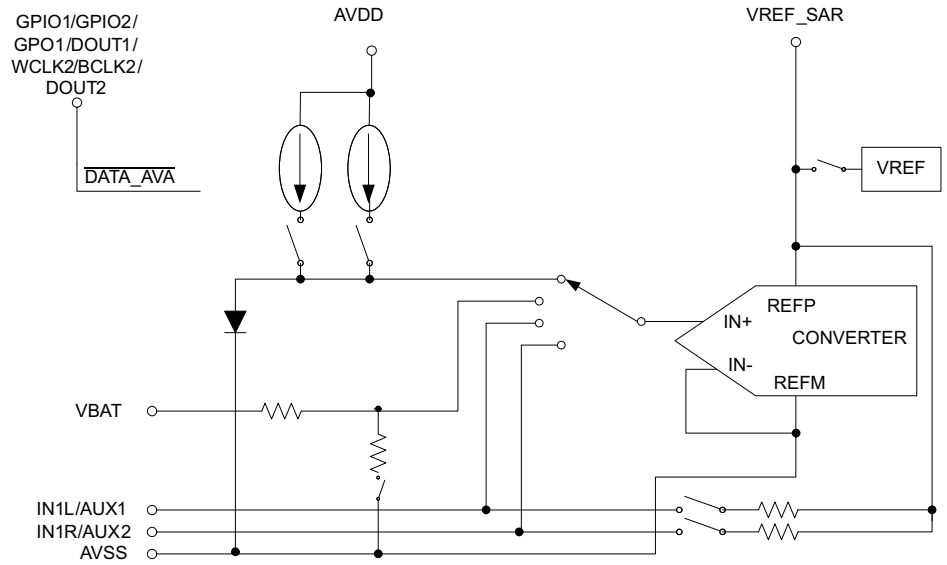


Figure 64. Simplified Diagram of the SAR ADC Analog Input Section

The ADC is controlled by an ADC control register (B0_P3_R3_D[7:0]). Several modes of operation are possible, depending on the bits set in the control register. Channel selection, scan operation, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the following sections for each type of analog input. The results of conversions made are stored in the appropriate result register.

The SAR ADC can be powered down forcefully by writing to B0_P3_R2_D7. Overall SAR configuration and mode is controlled by writing to B0_P3_R3_D[7:0].

Voltage Reference

The TLV320AIC3268 can use an internal voltage reference of 1.25V or an external reference through the reference control register (B0_P3_R6). The internal reference voltage should only be used in the single-ended mode for battery monitoring, for temperature measurement, and for using the auxiliary inputs.

The TLV320AIC3268 may use an external voltage reference (B0_P3_R6). In many systems, a 2.5V reference is supplied; however, this device supports a reference voltage up to the AVDDx_18 level. The external reference should be a low-noise signal and accordingly, depending on the application, it might need some R-C filtering at the VREF_SAR terminal.

This voltage reference should only be used in the single-ended mode for measuring the auxiliary inputs (IN1L/AUX1, IN1R/AUX2, and VBAT).

Variable Resolution

The TLV320AIC3268 provides three different resolutions for the ADC: 8, 10, or 12 bits. Lower resolutions are often practical for measurements such as system voltages. Performing the conversions at lower resolution reduces the amount of time it takes for the ADC to complete its conversion process, which lowers power consumption. The ADC resolution can be programmed by writing to B0_P3_R2_D[6:5].

Data Format

The TLV320AIC3268 output data is unsigned binary format and can be read from two 8-bit registers over the Control interface (SPI or I^2C). The SAR ADC's output data is MSB zero appended to make a 16-bit word.

8.3.6.1 Conversion Clock and Conversion Time

The TLV320AIC3268 contains an internal oscillator (LF_OSC_CLK), which is used to drive the state machines inside the device that perform the many functions of the part. MCLK is also available as a high frequency clock source. The clock source (LF_OSC_CLK or divided down MCLK) is selected by writing to B0_P3_R17_D7. When using the high frequency clock source MCLK , the clock divider B0_P3_R17_D[6:0] should be programmed to result in output clock pulses to be larger than 40ns. This clock (ADC_SAR_Clock) is further divided down to provide a clock to run the SAR ADC. The division ratio for this clock is set by writing to B0_P3_R2_D[4:3]. The ability to change the conversion clock rate allows the user to choose the optimal value for the resolution, speed, and power. If the division value is used as 1 , the ADC is limited to 8-bit resolution, division value of 2 is suitable for 10-bit resolution; 12-bit resolution requires the division value to be set as 4 or 8(recommended).

Similarly, the internal delay timers operate on clocks derived from either the LF_OSC_CLK or MCLK. The clock selection is controlled by writing to B0_P0_R23_D7. When using MCLK as the clock source the clock divider B0_P0_R23_D[6:0] should be programmed to have the resultant output clock to be approximately 1MHz in frequency. To avoid asynchronous issues, the system should use the same value for both B0_P0_R23_D7 and B0_P3_R17_D7.

Details for clock selection can be seen in Figure 65.

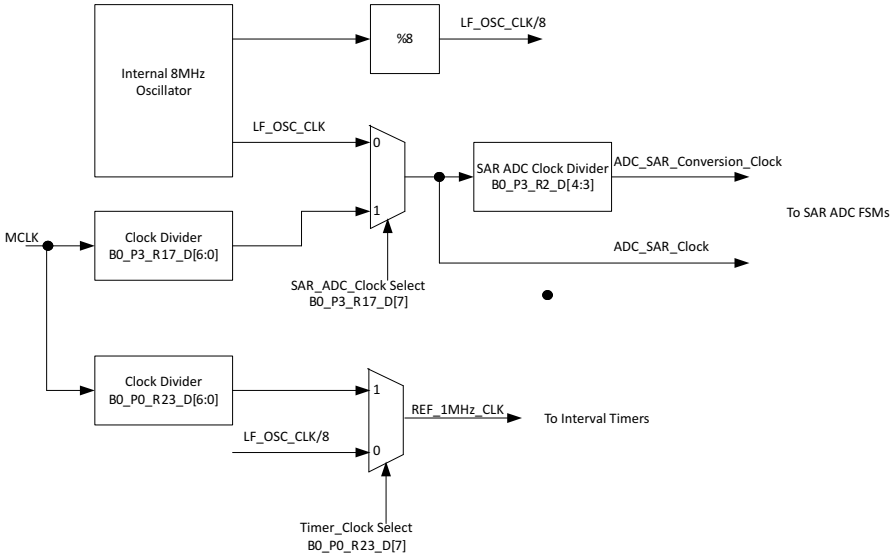


Figure 65. SAR ADC and Interval Timer Clock Select

Regardless of the conversion clock speed, the internal clock runs nominally at 8.2 MHz. The conversion time of the TLV320AIC3268 depends on several functions. While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles are needed for proper sampling of the signal. Conversion time can vary, depending on the mode in which the TLV320AIC3268 is used. Throughout this document, internal and conversion clock cycles are used to describe the times that many functions take to execute. Considering the total system design, these times must be taken into account by the user.

The ADC uses either the internal MCLK signal or the internal oscillator for the SAR conversions.

8.3.6.2 Data Available - INT1 or INT2 Programmed as $\overline{\text{DATA\_AVA}}$

The interrupt signals INT1 and INT2 can be programmed by writing to B0_P0_R50_D[7:6] (INT1) or B0_P0_R50_D[5:4] (INT2). These terminals function as the $\overline{\text{DATA\_AVA}}$ signal. To enable the SAR data available interrupt, B0_P3_R3_D[1:0] must be programmed to '01'. The $\overline{\text{DATA\_AVA}}$ signal and interrupts INT1 and INT2 can be mapped to GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, or DOUT2.

8.3.6.3 Temperature Measurement

In some applications, such as battery charging, a measurement of ambient temperature is required. The temperature measurement technique used in the TLV320AIC3268 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_j) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_j voltage and then monitoring the variation of that voltage as the temperature changes.

The TLV320AIC3268 offers two modes of temperature measurement. The first mode requires a single reading to predict the ambient temperature. A diode, as shown in Figure 66, is used during this measurement cycle. This voltage is typically 600 mV at 25°C with a 20µA current through it. The absolute value of this diode voltage can vary a few millivolts. The temperature coefficient of this voltage is typically 2 mV/°C. During the final test of the end product, the diode voltage at a known room temperature is stored in nonvolatile memory. Further calibration can be done to calculate the precise temperature coefficient of the particular device. This method has a temperature resolution of approximately 0.4°C/LSB and accuracy of approximately ±3°C with two-temperature calibration. Figure 67 and Figure 68 show typical plots with single and two-temperature calibration, respectively.

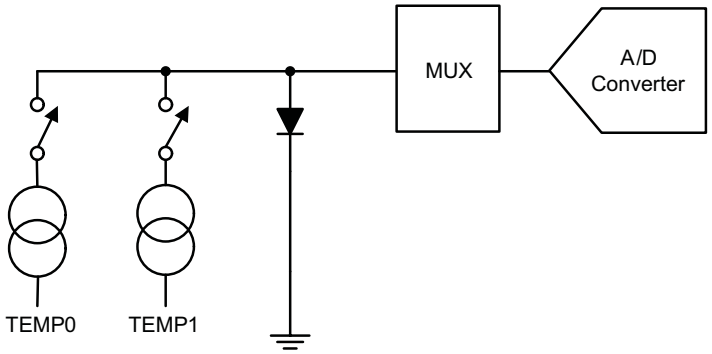


Figure 66. Functional Block Diagram of Temperature-Measurement Mode

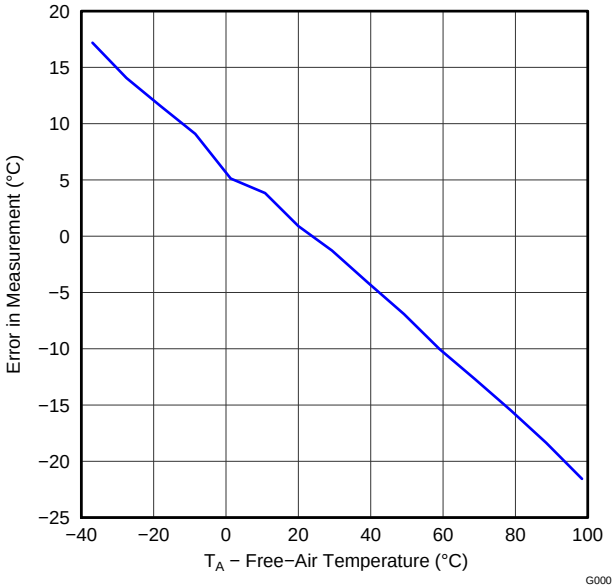


Figure 67. Typical Plot of Single-Measurement Method After Calibrating for Offset at Room Temperature

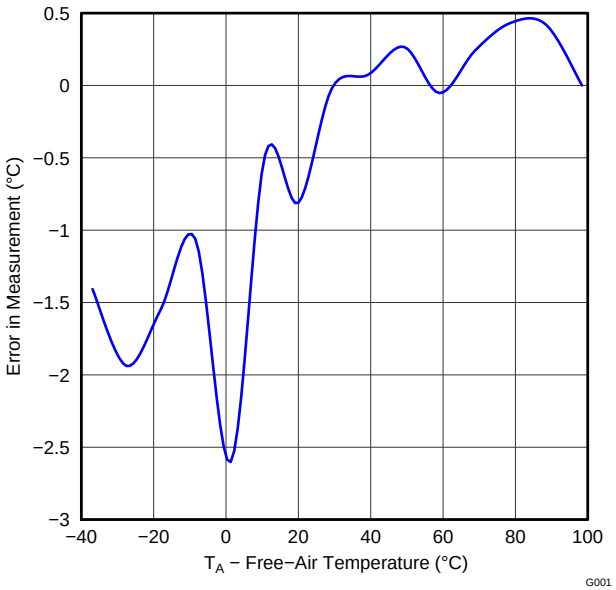


Figure 68. Typical Plot of Single-Measurement Method After Calibrating for Offset and Gain at Two Temperatures

The second mode uses a two-measurement (differential) method. This mode requires a second conversion with a current 82 times larger. The voltage difference between the first (TEMP1) and second (TEMP2) conversion, using 82 times the bias current, is represented by:

$$V_{(Temp1 - Temp2)} = \frac{kT}{q} \times \ln(N) \tag{18}$$

where

N is the current ratio = 82
k = Boltzmann's constant (1.38054×10^{-23} electron volts/Kelvin)
q = the electron charge (1.602189×10^{-19} C)

T = the temperature in degrees Kelvin

The equation for the relation between differential code and temperature may vary slightly from device to device and can be calibrated at final system test by the user. This method provides resolution of approximately 2°C/LSB and accuracy of approximately ±6°C after calibrating at room temperature. A plot of typical calibration error for this method is shown in Figure 69.

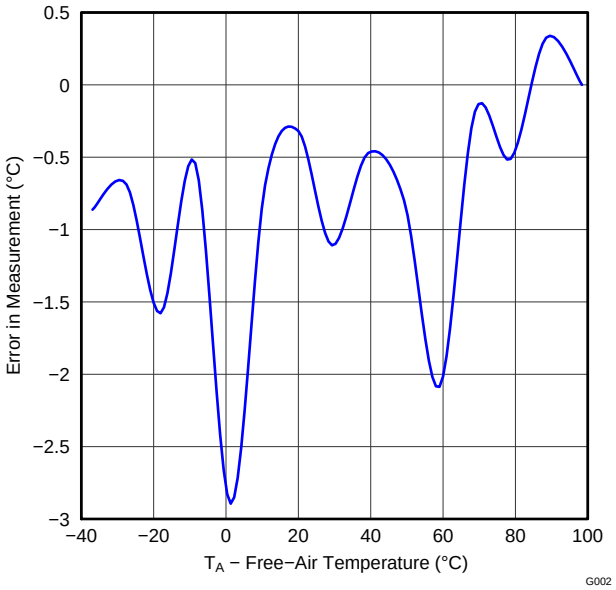


Figure 69. Typical Plot of Differential Measurement Method After Calibrating for Offset and Gain at Two Temperatures

The TLV320AIC3268 supports programmable auto-temperature measurement mode, which can be enabled by setting B0_P3_R19_D4. In this mode, the TLV320AIC3268 can auto-start the temperature measurement after a programmable interval. The user can program minimum and maximum threshold values through a register. In the case of temperature measurements, these thresholds are controlled in B0_P3_R30-R33. If the measurement goes outside the threshold range, the TLV320AIC3268 sets a flag in read-only B0_P3_R21, which is cleared after the flag is read. The TLV320AIC3268 can also be configured to send an active-high interrupt over INT1 or INT2 by setting bits in B0_P0_R50. The duration of the interrupt is approximately 2 ms, if B0_P0_R51_D[7:6] = '00' or B0_P0_R51_D[5:4] = '00', or these interrupt signals can be configured for alternate output signals. See Interrupt Generation and Diagnostic Flags for more details on interrupt generation.

Temperature measurement can only be done in host-controlled mode.

8.3.6.4 Auxiliary Battery-Voltage Measurement for VBAT

The TLV320AIC3268 can be used to measure battery voltage up to 6V. This measurement can made using the VBAT terminal, which has a voltage divider (divide by 5), as seen in Figure 64. This analog prescaler is available on the terminal to allow higher voltages to be measured by the SAR ADC. This battery measurement function is supported in 8-bit, 10-bit, and 12-bit modes.

To enable the battery-voltage measurement mode, write a '0110' to B0_P3_R3_D[5:2].

Because the ADC code is 1/5 of the actual voltage value applied at VBAT, the correct value can be found by multiplying the ADC code by 5. For low voltages of VREF_SAR, this function can support voltages from 0 to (5 × VREF_SAR), where the upper voltage limit for VBAT is 6V, and is also limited by the value listed in the *Absolute Maximum Ratings* table in the TLV320AIC3268 data sheet.

In the battery-voltage measurement mode, the conversion results in an ADC output code of B, where the voltage at the input terminal (VBAT) can be calculated as:

$$V_{BAT} = \frac{B}{2^N} \times (5 \times VREF\_SAR) \quad (19)$$

where:

N is the programmed resolution of the SAR ADC.

VREF_SAR is the applied external reference voltage.

For an example of a script for battery voltages on VBAT, download the Example Scripts zip file from the TLV320AIC3268 product page.

8.3.6.5 Auxiliary Voltage Measurements

The TLV320AIC3268 can be used to measure voltage on IN1L/AUX1 and IN1R/AUX2 terminals. This voltage measurement function is supported in 8-bit, 10-bit, and 12-bit modes.

For IN1L/AUX1 and IN1R/AUX2:

If the conversion results in an ADC output code of B, then the voltage at the input terminals (IN1L/AUX1 and IN1R/AUX2) can be calculated as:

$$V_{PIN} = \frac{B}{2^N} \times VREF\_SAR \tag{20}$$

where:

N is the programmed resolution of the SAR ADC.

VREF_SAR is the applied external reference voltage.

For an example of a script for reading voltages on IN1L, download the Example Scripts zip file from the TLV320AIC3268 product page.

The TLV320AIC3268 supports a special mode of conversion on IN1L/AUX1 and IN1R/AUX2 terminals called the resistance measurement mode. This mode is useful for measuring the value of an external resistance connected to this terminal. Conversion for IN1L/AUX1 input works in resistance measurement mode by writing '1' to B0_P3_R19_D2 and conversion for IN1R/AUX2 works in resistance measurement mode by writing '1' to B0_P3_R19_D1.

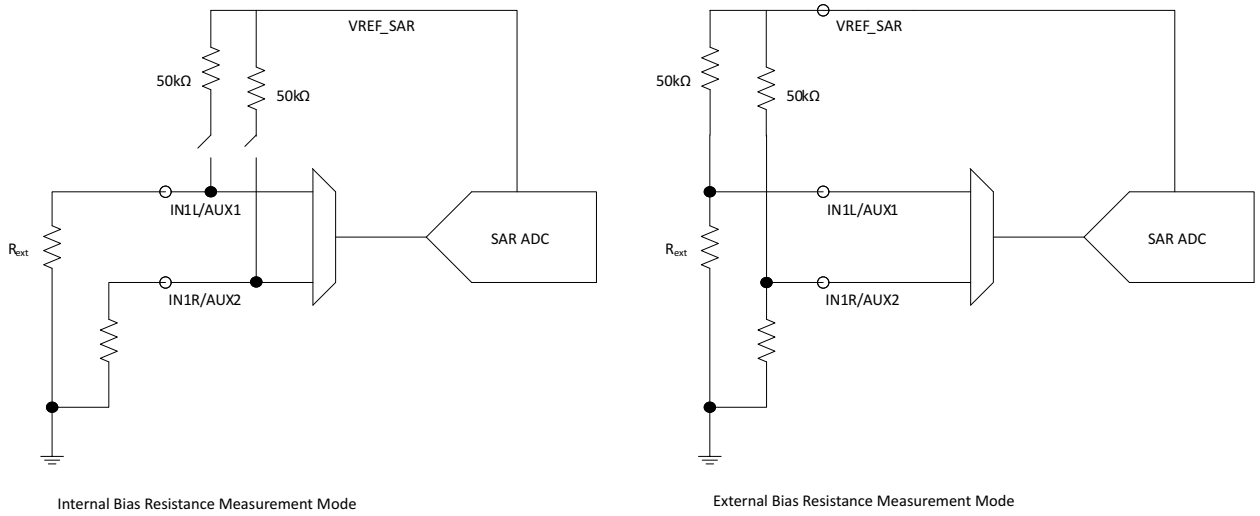


Figure 70. Resistance measurement mode for IN1L/AUX1 and IN1R/AUX2

The resistance measurement mode works in two ways. In Internal Bias Resistance measurement mode the value of external resistance R_{ext} is measured as a ratio with internal bias resistance which is nominally of 50kΩ value. The value of R_{ext} is calculated by Equation 21. This value is useful to measure external resistance without any external components. The internal bias resistance will however exhibit device to device variation and should thus be used where a very high accuracy measurement is not required.

R_{ext}=ADCOUT.50000/(2^N-ADCOUT)

(1) Where N is the resolution of the SAR ADC

(2) Where bias resistor is 50kΩ. The equation will scale for a different value of bias resistor. (21)

The resistance measurement mode can be also enabled to work with external bias resistor by writing '1' to B0_P3_R19_D0. When using this mode, an external bias resistor of 50kΩ should be connected between VREF_SAR and IN1L/AUX1 or IN1R/AUX2 terminals. This mode enables a higher accuracy conversion by using a higher accuracy bias resistance. The value of R_{ext} is determined by Equation 21.

8.3.6.6 Auto Scan

If making voltage measurements on one or many of the inputs from IN1L/AUX1, IN1R/AUX2, VBAT and TEMP1 (or TEMP2) is desired on a continuous basis, then the auto-scan mode can be used. This mode causes the TLV320AIC3268 to sample and convert each of selected inputs in a repetetive manner with programmed intervals. The set of inputs that can be selected are programmed by configuring B0_P3_R19_D[7:4]. Auto scan can be set up by writing "1001" to B0_P3_R3_D[5:2]. Programming B0_P3_R15_D[3:0], allows a programmable interval delay to be introduced between successive conversions of the set of inputs selected for covnersion.

See *Conversion Time Calculations for the TLV320AIC3268*, Host-Controlled Auto Scan Mode for conversion-time calculations and timing diagrams.

8.3.6.7 Port Scan

If making voltage measurements on the inputs IN1L/AUX1, IN1R/AUX2, and VBAT is desired on a periodic basis, then the port-scan mode can be used. This mode causes the TLV320AIC3268 to sample and convert each of the auxiliary inputs once. At the end of this cycle, all of the auxiliary result registers contain the updated values. Thus, with one write to the TLV320AIC3268, the host can cause three different measurements to be made. Port scan can be set up by writing "1011" to B0_P3_R3_D[5:2].

See *Conversion Time Calculations for the TLV320AIC3268*, *Port-Scan Operation*, Port-Scan Operation, for conversion-time calculations and timing diagrams.

8.3.6.8 Buffer Mode

The TLV320AIC3268 supports a programmable buffer mode for all conversions (VBAT, IN1L/AUX1, IN1R/AUX2, TEMP1, TEMP2). Buffer mode is implemented using a circular FIFO with a depth of 64. The number of interrupts required to be serviced by a host processor can be reduced significantly in buffer mode. Buffer mode can be enabled using B0_P3_R13_D7.

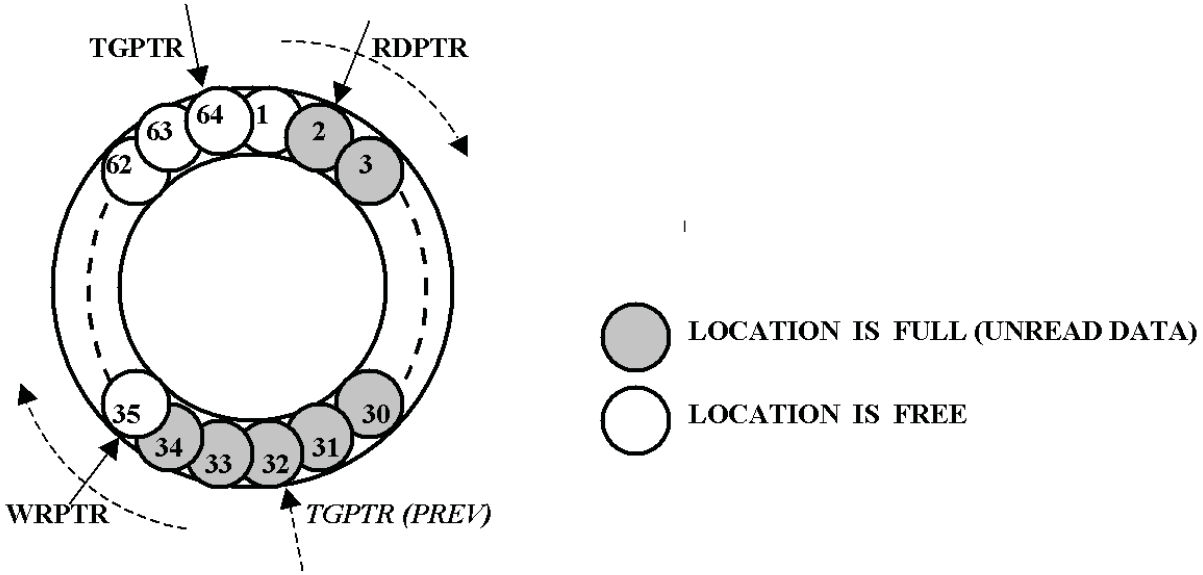


Figure 71. Circular Buffer

Converted data is automatically written into the FIFO. To control the writing, reading and interrupt process, a write pointer (WRPTR), a read pointer (RDPTR), and a trigger pointer (TGPTR) are used. The read pointer always shows the location that is read next. The write pointer indicates the location in which the next converted data is to be written. The trigger pointer indicates the location at which an interrupt is generated if the write pointer reaches that location. Trigger level is the number of the data values needed to be present in the FIFO before generating an interrupt. Figure 71 shows the case when the trigger level is programmed as 32. On resetting the buffer mode, RDPTR moves to location 1, WRPTR moves to location 1, and TGPTR moves to a location equal to the programmed trigger level.

The user can select the input or input sequence to be converted by writing to B0_P3_R3_D[5:2]. The converted values are written in a predefined sequence to the circular buffer. The user has flexibility to program a specific trigger level in order to choose the configuration which best fits the application. When the number of converted data values written in FIFO becomes equal to the programmed trigger level, then the device generates an interrupt signal on INT1 or INT2. In buffer mode, the user should program this terminal as Data Available. In buffer mode, conversions (VBAT, IN1L/AUX1, IN1R/AUX2, TEMP1, TEMP2) are allowed only in host-controlled mode.

Buffer mode can be used in single-shot conversion or continuous-conversion mode.

In single-shot conversion mode, once the number of data values written reaches the programmed trigger level, the TLV320AIC3268 generates an interrupt and waits for the user to start reading. As soon as the user starts reading the first data value from the last converted set, the TLV320AIC3268 clears the interrupt and starts a new set of conversions, and the trigger pointer is incremented by the programmed trigger level. An interrupt is generated again when the trigger condition is satisfied.

In continuous-conversion mode, once the number of data values written reaches the programmed trigger level, the TLV320AIC3268 generates an interrupt. It immediately starts a new set of conversions, and the trigger pointer is incremented by the programmed trigger level. An interrupt is cleared either by writing the next converted data value into the FIFO or by starting to read from the FIFO.

Depending on how the user is reading data, the FIFO can become empty or full. If the user is trying to read data even if the FIFO is empty, then RDPTR keeps pointing to same location. If the FIFO becomes full, then the next location is overwritten with newly converted data values, and the read pointer is incremented by one.

While reading the FIFO, the TLV320AIC3268 provides FIFO-empty and -full status flags along with the data. The user can also read a status flag from B0_P3_R13_D[1:0]. See Table 33 for buffer-mode control and Table 34 for buffer-mode 16-bit read-data format.

Table 33. SAR/Buffer Mode Data Read Control (B0_P3_R18_D[7:5])(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: SPI interface is used for SAR/buffer data reading. 1: I^2C interface is used for SAR/buffer data reading.
D6	R/W	0	0: SAR/buffer data update is automatically halted (to avoid simultaneous buffer read and write operations) based on internal detection logic. Valid only for SPI interface. 1: SAR/buffer data update is held using software control (B0_P3_R18_D5).
D5	R/W	0	0: SAR/buffer data update is enabled all the time (valid only if B0_P3_R18_D6 = 1). 1: SAR/buffer data update is stopped so that user can read the last updated data without any data corruption (valid only if B0_P3_R18_D6 = 1).

(1) To enable buffer mode, write a 1 to B0_P3_R13_D7.

Table 34. Buffer Mode 16-Bit Read Data Format (B0_P252_R1 and B0_P252_R2)

BUFFER READ DATA BIT	NAME	RESET VALUE	DESCRIPTION	COMMENT
D15	FUF	0	Buffer-Full flag - This flag indicates that all the 64 locations of the buffer contain unread data.	B0_P252_R1_D7
D14	EMF	1	Buffer-Empty flag - This flag indicates that there is no un-read data available in FIFO. This is generated while reading the last converted data.	B0_P252_R1_D6
D13		X	Reserved	B0_P252_R1_D5

Table 34. Buffer Mode 16-Bit Read Data Format (B0_P252_R1 and B0_P252_R2) (continued)

BUFFER READ DATA BIT	NAME	RESET VALUE	DESCRIPTION	COMMENT
D12	ID	X	Data identification: 0 = VBAT or IN1R/AUX2 data in R11-R0 1= IN1L/AUX1 or TEMP data in R11-R0 Order for writing data in buffer when multiple inputs are selected: For autoscan conversion: IN1L/AUX1 (if selected), IN1R/AUX2 (if selected), VBAT, TEMP1 or TEMP2 (if selected) For port-scan conversion: IN1L/AUX1, IN1R/AUX2, VBAT	B0_P252_R1_D4
D11-D8	R11-R8	X	Converted data (MSB, 4 bits)	B0_P252_R1_D[3:0]
D7-D0	R7-R0	X	Converted data (LSB, 8 bits)	B0_P252_R2_D[7:0]

8.3.6.8.1 Buffer Mode Access through I²C for TLV320AIC3268

To enable faster data access, SPI protocol is preferred, but if I²C is required, note the following.

- In continuous buffer mode:
  - Only one measurement type, that is choice of IN1L, IN1R, VBAT, TEMP1 or TEMP2, can be used.
- In single-shot mode:
  - Multiple measurement types can be stored in the buffer consecutively.
  - The I²C read must completely empty the buffer. In other words, the number of bytes read must be equal to the trigger-level multiplied by 2 (for 2 bytes per converted data). If the buffer is empty, this will be reflected by bit B0_P252_R1_D6=1 in the last measurement read.
  - The I²C read must empty the buffer in a single call. Note that some I²C drivers may break auto-increment instructions into multiple, smaller calls. This can cause the SAR buffer to return invalid data, so the SAR trigger level must be less than or equal to the max I²C auto-increment size divided by 2.
- If 64 elements (128 bytes) are read, the last byte will be invalid data since I²C allows a maximum of 127 bytes.

8.3.6.9 Reading AUX Data in Non-Buffer Mode From SPI

Reading from the TLV320AIC3268 is done by using the protocol called out in Figure 72.

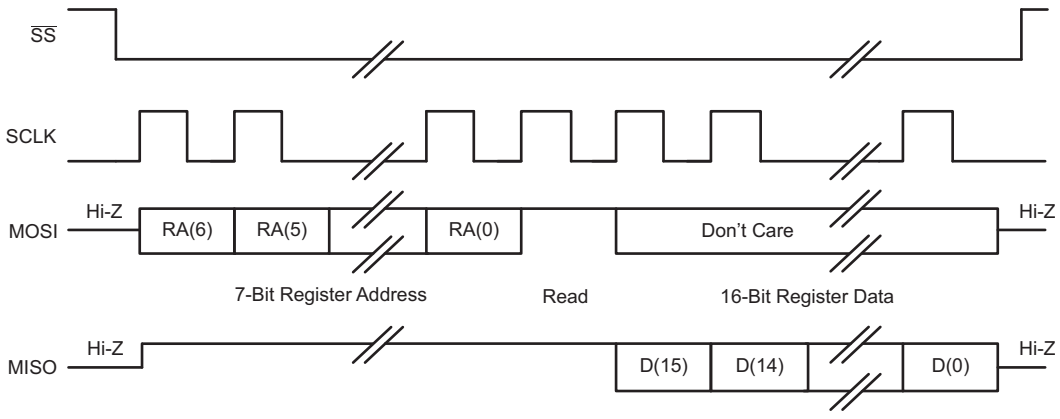


Figure 72. 16-Bit Data-Read Timing, 24 Clocks per 16-Bit Data Read, 8-Bit Bus Interface

This protocol uses a 24-clock sequence to get a 16-bit data read. Set the INT1 or INT2 interrupt for monitoring the data-available status by writing '01' to B0_P3_R3_D[1:0]. Reading is normally done when the interrupt is low (data is available for reading). Status from the ADC conversion can be read from B0_P3_R9. If bit D6 is 0, then the ADC is actively converting, so a BUSY status is read. If bit D5 is set, then some data is now available for reading. Next, reading from a status register on B0_P3_R10 lets us know if data is available for IN1L/AUX1, IN1R/AUX2, or VBAT. If bit D7 is set, then IN1L/AUX1 data can be read. If bit D6 is set, then IN1R/AUX2 data can be read. If bit D5 is set, then VBAT data can be read.

The first 7 bits in the read sequence are for the first register address of the two sequential 8-bit registers. The next bit is high, which specifies that a read operation follows; then the 16 remaining clocks are used to get the 16-bit data that is read out in the order of D15–D0. The register address specified in the first seven clocks of the 24-clock sequence reads out as bits D15–D8, where D15 is the MSB of the byte, then the register number is incremented by 1 and the data is read from D7–D0, where D7 is the MSB of that byte. (For reading data for IN1L/AUX1, use B0_P3_R54 and B0_P3_R55; for reading data for IN1R/AUX2, use B0_P3_R56 and B0_P3_R57; and for reading data for VBAT, use B0_P3_R58 and B0_P3_R59.) From this cycle, the first 16-bit data word has been read. This sequence can be repeated to read further values of IN1L/AUX1, IN1R/AUX2, and VBAT data.

8.3.6.10 Auto Threshold Detect

The SAR ADC in TLV320AIC3268 has a special auto threshold detect feature where the device can detect a conversion exceeding the pre-programmed minimum and maximum thresholds for the input. Upon such a detection the TLV320AIC3268 can interrupt the host processor. This feature is useful as it allows the host to be immediately informed about out of range conditions, without the host having to poll for converted values. Upon receiving an interrupt, the host can read the flag register to find the input which exceeded the maximum or minimum threshold. The register settings for Auto Threshold Detect feature are described in Table 35.

Table 35. Threshold Detect Settings

Parameter	IN1L/AUX1	IN1R/AUX2	TEMP
Maximum Threshold check enable	B0_P3_R22_D[4]='1'	B0_P3_R26_D[4]='1'	B0_P3_R30_D[4]='1'
Maximum Threshold Code	B0_P3_R22_D[3:0], B0_P3_R23_D[7:0]	B0_P3_R26_D[3:0], B0_P3_R27_D[7:0]	B0_P3_R30_D[3:0], B0_P3_R31_D[7:0]
Minimum Threshold check enable	B0_P3_R24_D[4]='1'	B0_P3_R28_D[4]='1'	B0_P3_R32_D[4]='1'
Minimum Threshold Code	B0_P3_R24_D[3:0], B0_P3_R25_D[7:0]	B0_P3_R28_D[3:0], B0_P3_R29_D[7:0]	B0_P3_R32_D[3:0], B0_P3_R33_D[7:0]
Maximum Threshold Flag	B0_P3_R21_D5	B0_P3_R21_D3	B0_P3_R21_D1
Minimum Threshold Flag	B0_P3_R21_D4	B0_P3_R21_D2	B0_P3_R21_D0
INT1 interrupt on Threshold exceed	B0_P0_R50_D7		
INT2 interrupt on Threshold exceed	B0_P0_R50_D5		

8.3.6.11 Conversion Time Calculations for the TLV320AIC3268

This section discusses conversion time calculations for temperature, auxiliary, and battery measurements for TLV320AIC3268.

The timing signals can be programmed by B0_P3_R3. INT1 or INT2 can be programmed as $\overline{\text{DATA\_AVA}}$ by programming B0_P0_R50_D[7:4]. $\overline{\text{DATA\_AVA}}$ can also be sent to GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, or DOUT2.

Table 36. Parameters for calculating Conversion Times

Parameter	Definition
N_{avg}	SAR ADC output is provided after averaging over N_{avg}samples. Averaging is controlled by B0_P3_R2_D[2:0] where 000 => Mean Filter, N_{avg}=1 001 => Mean Filter, N_{avg}=4 010 => Mean Filter, N_{avg}=8 011 => Mean Filter, N_{avg}=16 100 => Median Filter, N_{avg}=1 101 => Median Filter, N_{avg}=5 110 => Median Filter, N_{avg}=9 111 => Median Filter, N_{avg}=15

Table 36. Parameters for calculating Conversion Times (continued)

Parameter	Definition
N_{inp}	Number of inputs to be converted for scan conversion, for example, for Scan mode N_{inp}=1 and Port-Scan mode N_{inp}=3
N_{bits}	Resolution of SAR ADC. Can be set to 8, 10 or 12bits by programming B0_P3_R2_D[6:5]
t_{clk}	Clock period of ADC_SAR_CLK. See Figure 65
t_{conv}	Clock period of ADC_SAR_Conversion_Clock. See Figure 65
t_{ref}	Power up stabilization time for internal reference. This is configured by programming B0_P3_R6_D[3:2] where 00 => t_{ref} = 0 01 => t_{ref} = 8000*t_{clk} 10 => t_{ref} = 32000*t_{clk} 11 => t_{ref} = 64000*t_{clk}
t_{del}	Programmable interval delay timer used for Auto-Scan Mode. Configured by programming B0_P3_R15_D[3:0]. This is the programmable interval delay between two consecutive conversions sets. A conversion set it the set of inputs that have been enabled in Auto-Scan mode.
n_1	n_1 = 6 for SAR_ADC_CLK_DIV=2 for 8-bit conversion mode. SAR_ADC_CLK_DIV is programmed in B0_P3_R2_D[4:3]=00. n_1 = 7 for all other values of SAR_ADC_CLK_DIV
n_2	n_2 = 11 for TEMP1 conversion mode n_2 = 387 for IN1L/AUX1 , IN1R/AUX2 conversions in resistance mode. n_2 = 0 for all other conversions
n_3	n_3 = 0 if external reference is used for SAR_ADC. B0_P3_R6_D[7] = '0' n_3 = 3 if internal reference is used and always powered up. B0_P3_R6_D[7]='1' and B0_P3_R6_D[5]='0' n_3 = 1 + t_{ref}/t_{clk} for all other conversions
n_4	n_4=0, if programmable interval delay timer is diabled or B0_P3_R15_D[3] = '0' n_4=7, if programmable interval delay timer is enabled or B0_P3_R15_D[3] = '1'

8.3.6.11.1 Host-Controlled Scan Mode

The time needed to make one single conversion for VBAT, IN1L/AUX1, IN1R/AUX2, TEMP1 (or TEMP2) is given by

$$T_{cycle}=N_{avg}.\{(N_{bits}+ 1).t_{conv} + (n_1+ 13).t_{clk}\} + N_{avg}.n_2.t_{clk} + (n_3 + 17).t_{clk}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) The programmable delay t_{REF} scales accordingly based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

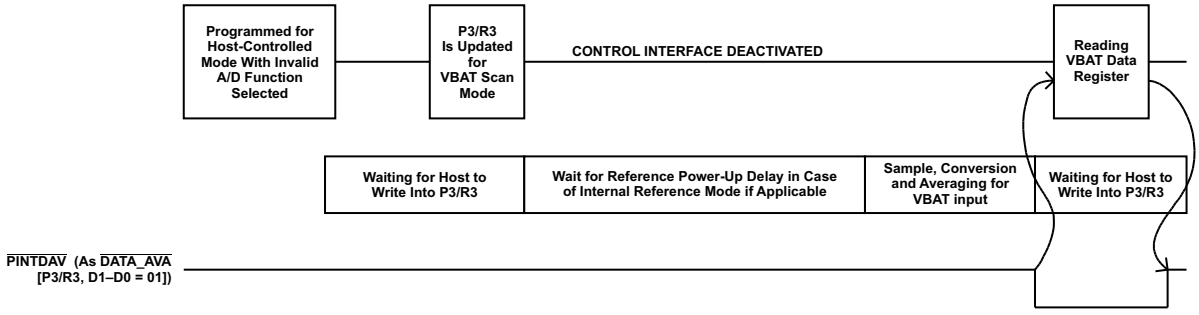


Figure 73. Host-Controlled VBAT Scan Mode

8.3.6.11.2 Host-Controlled Auto Scan Mode

The time needed for one cycle of Auto Scan Mode is given by:

$$T_{cycle}=N_{inp}.N_{avg}.\{(N_{bits}+ 1).t_{conv} + (n_1+ 13).t_{clk}\} + N_{avg}.n_2.t_{clk} + N_{inp}.9.t_{clk} + (n_3 + n_4).t_{clk} + t_{del}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) This equation is valid only from the second conversion onward.

(3) All the programmable delays, t_{DEL} and t_{REF}, scale accordingly based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

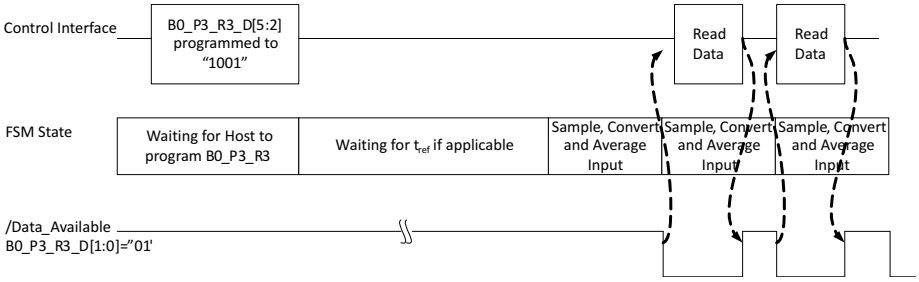


Figure 74. Host-Controlled Auto Scan Mode

8.3.6.11.3 Port-Scan Operation

The time needed to complete one set of Port-Scan conversions is given by:

$$T_{cycle}=3.N_{avg}.\{(N_{bits}+1).t_{conv} + (n_1+13).t_{clk}\} + (n_3+35).t_{clk}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) The programmable delay t_{REF} scales based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

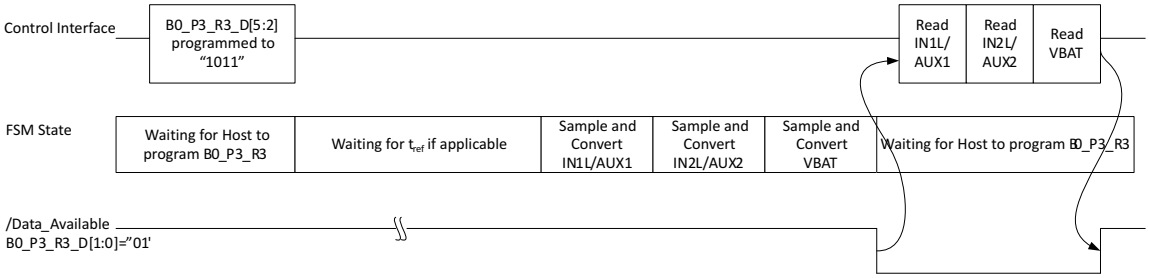


Figure 75. Host-Controlled Port Scan Mode

8.3.7 Headset Detection

The TLV320AIC3268 includes extensive capability to monitor a headphone, microphone, or headset jack to find if a plug has been inserted into the jack, and if inserted find the nature of headset or headphone inserted in the jack. The device also includes the capability to detect a button press for actions such as starting a call with headset button press. The figures below show the circuit configuration to enable this feature for stereo headphones and stereo headset with microphone and button, as well as mono headset with and without microphone. It is recommended to use IN1L or IN1R for external headset microphones.

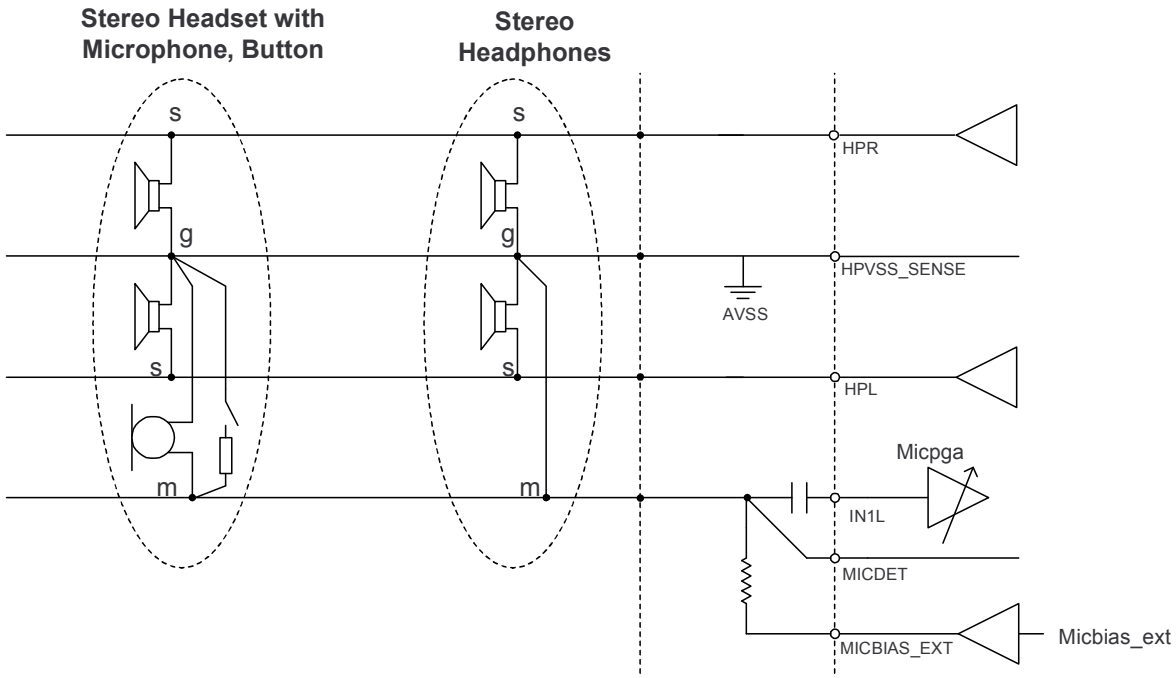


Figure 76. Jack Connections for Detection of Stereo Headsets

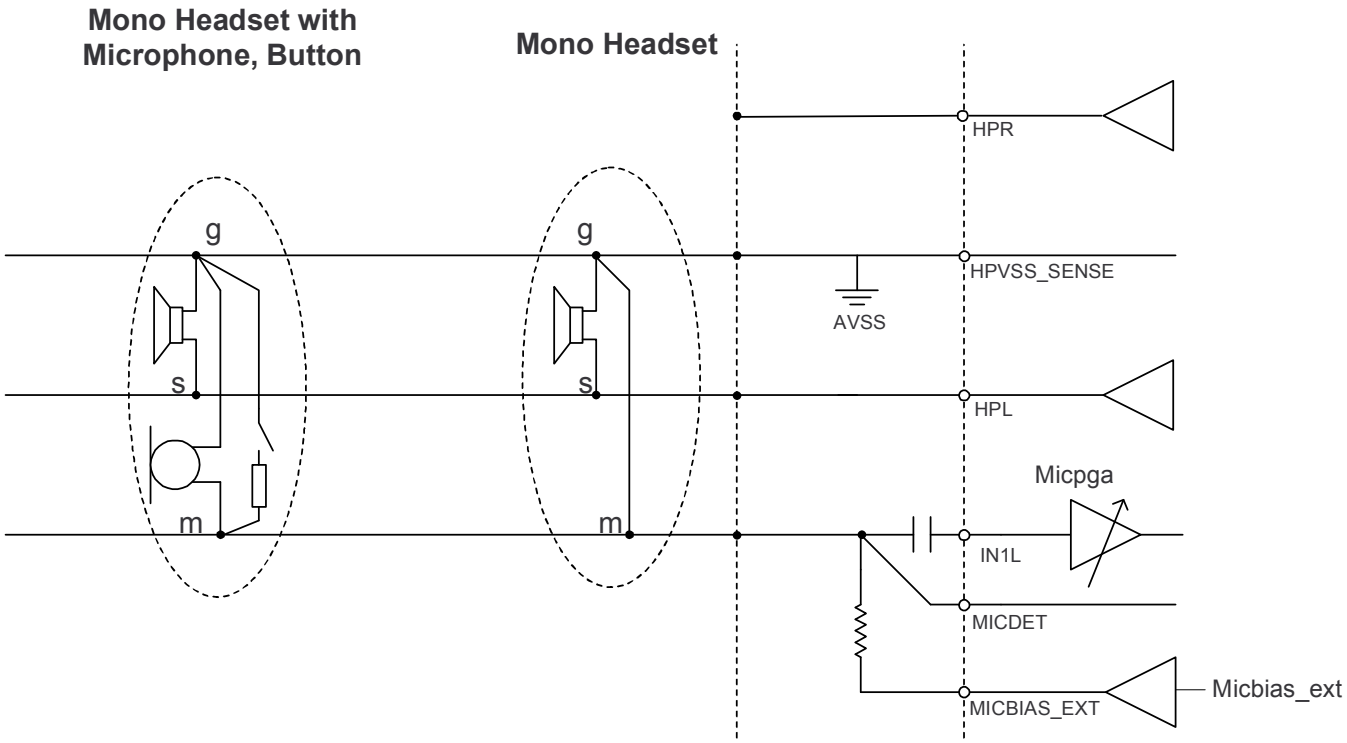


Figure 77. Jack Connections for Detection of Mono Headsets

This feature is enabled by programming B0_P0_R67_D7. In order to avoid false detections due to mechanical vibrations in headset jacks or microphone buttons, a debounce function is provided for glitch rejection. For the case of headset insertion/removal, a debounce function with a range of 16ms - 512ms is provided. This can be programmed via B0_P0_R67_D[4:2]. For improved button-press detection, the debounce function has a range of 8ms to 32ms by programming B0_P0_R67_D[1:0].

The TLV320AIC3268 also provides feedback to user when a button press, or a headset insertion/removal event is detected through register readable flags as well as an interrupt on the IO terminals. The value in B0_P0_R46_D[5:4] provides the instantaneous state of button press and headset insertion. B0_P0_R44_D5 is a sticky (latched) flag that is set when the button-press event is detected. B0_P0_R44_D4 is a sticky flag that is set when the headset insertion or removal event is detected. These sticky flags are set by the event occurrence, and are reset only when read. This requires polling B0_P0_R44. To avoid polling and the associated overhead, the TLV320AIC3268 also provides an interrupt feature where the events can trigger the INT1 and/or INT2 interrupts. These interrupt events can be routed to one of the digital output terminals. Please see Interrupt Generation and Diagnostic Flags for details on interrupts (INT1 and INT2) and Interrupt Generation and Diagnostic Flags for details on digital terminal routing.

As shown in Figure 76 and Figure 77, the TLV320AIC3268 not only detects a headset insertion event, but also distinguishes between the different headsets inserted, such as stereo headphones, stereo cellular headsets with microphone, mono headsets with microphone, and mono headset without microphone. After the headset-detection event, the user can read B0_P0_R37_D[5:4] and B0_P0_R37_D[1:0] to determine the type of headset inserted.

Table 37. Headset Detection Types

Headset Type	Microphone Detection	Headset Detection
Stereo Headphones without Microphone	B0_P0_R37_D[5:4] = 01	B0_P0_R37_D[1:0] = 10
Stereo Headset with Microphone	B0_P0_R37_D[5:4] = 11	B0_P0_R37_D[1:0] = 10
Mono Headset without Microphone	B0_P0_R37_D[5:4] = 01	B0_P0_R37_D[1:0] = 01
Mono Headset with Microphone	B0_P0_R37_D[5:4] = 11	B0_P0_R37_D[1:0] = 01

For proper detection of these different types, it is important to follow the guidelines in Table 38.

Table 38. Detection Specifications for Microphone, Button, Headset

Parameter	Minimum	Typical	Maximum	Unit
Headphone load resistance	16		300	Ω
Key switch resistance (includes all jack-to-plug contact resistances)			2	Ω
Effective capacitance between MICDET and ground			150	pF
Microphone effective resistance	0.8		8	kΩ
Micbias_ext resistor for microphone detection	2.09	2.2	2.31	kΩ

Table 39. Headset Detection Block Registers

Register	Description
B0_P0_R67_D7	Headset Detection Enable/Disable
B0_P0_R67_D[4:2]	Debounce Programmability for Headset Detection
B0_P0_R67_D[1:0]	Debounce Programmability for Button Press
B0_P0_R44_D5	Sticky Flag for Button Press Event
B0_P0_R44_D4	Sticky Flag for Headset Insertion or Removal Event
B0_P0_R46_D5	Status Flag for Button Press Event
B0_P0_R46_D4	Status Flag for Headset Insertion and Removal
B0_P0_R37_D[5:4] and B0_P0_R37_D[1:0]	Flags for type of Headset Detected
B0_P1_R119 and B0_P1_R120	Headset Detection Tuning Registers

The headset detection block requires AVDDx_18 and AVDD3_33 to be powered. In addition, the weak connection of AVDDx_18 to DVDD_18 should be disabled (B0_P1_R1_D3="0"), and External Analog Supplies should be enabled (B0_P1_R1_D2="0"). The headset detection feature in the TLV320AIC3268 is achieved with a very low power overhead, requiring less than 30µA of additional current from AVDDx_18 supplies.

8.3.8 Interrupt Generation and Diagnostic Flags

The TLV320AIC3268 an trigger interrupts to the host processor for events that require host processor intervention. This avoids polling the status-flag registers continuously. The TLV320AIC3268 has two defined interrupts; INT1 and INT2 that can be configured by programming Page 0, Register 48 and 49. A user can configure the interrupts INT1 and INT2 to be triggered by one or many events such as:

- Headset Detection
- Button Press
- Noise Detected by AGC
- Over-current Condition in Headphones
- Data Overflow in ADC and DAC Processing Blocks and Filters
- Over-temperature Condition in Speaker Drivers
- SAR ADC Data Available or Exceeding Threshold

Each of these INT1 and INT2 interrupts can be routed to output terminals like GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, and DOUT2 by configuring B0_P4_R67-R96. Table 40 displays how to individually configure the INT1 or INT2 interrupts.

Table 40. Register Settings for Interrupt Routing

Terminal	INT1	INT2
GPIO1	B0_P4_R86_D[5:2] = 0101	B0_P4_R86_D[5:2] = 0110
GPIO2	B0_P4_R87_D[5:2] = 0101	B0_P4_R87_D[5:2] = 0110
GPO1	B0_P4_R96_D[5:2] = 0100	B0_P4_R96_D[5:2] = 0101
DOUT1	B0_P4_R67_D[4:1] = 0100	B0_P4_R67_D[4:1] = 0101
WCLK2	B0_P4_R69_D[5:2] = 0101	B0_P4_R69_D[5:2] = 0110
BCLK2	B0_P4_R70_D[5:2] = 0101	B0_P4_R70_D[5:2] = 0101
DOUT2	B0_P4_R71_D[4:1] = 0100	B0_P4_R71_D[4:1] = 0101

These interrupt signals can either be configured as a single pulse, a series of pulses, or a change in output level by programming B0_P0_R51_D[7:6] and B0_P0_R51_D[5:4]. If the user configures the interrupts as a series of pulses, the events will trigger the start of pulses that will stop when the flag registers in B0_P0_R42, B0_P0_R44, B0_P0_R45 are read by the user to determine the cause of the interrupt. Similarly, if the user configures the interrupts as an active-high, level-based interrupt generated from these sticky flags, the interrupt port will reset low when the flag registers in B0_P0_R42, B0_P0_R44, B0_P0_R45 are read by the user.

When the interrupts are configured for multiple events simultaneously, the user can read associated flags to determine the triggering events. Sometimes upon reading the Primary Flag Registers, additional Secondary Flag Registers may have to be read back to resolve the triggering event. For example, on receiving an interrupt, the user can read Primary Flag Registers B0_P0_R44 and B0_P0_R45. If B0_P0_R44_D[7] is '1', it indicates an over-current condition on one of HPL, RECP or SPK drivers has happened. To determine which of the three drivers had an over-current condition, the Secondary Flag Register B0_P1_R69 should be read back. Table 41 provides details of Primary Flag Registers and Secondary Flag Registers which can be used to resolve events causing the interrupts.

Table 41. Flags for Interrupt

Primary Flag Register	Secondary Flag Register	Type	FLAG Details
B0_P0_R42_D[7]		Sticky	Left DAC Overflow Flag
B0_P0_R42_D[6]		Sticky	Right DAC Overflow Flag
B0_P0_R42_D[5]		Sticky	DAC Barrel Shifter Overflow Flag
B0_P0_R42_D[3]		Sticky	Left ADC Overflow Flag

Table 41. Flags for Interrupt (continued)

Primary Flag Register	Secondary Flag Register	Type	FLAG Details
B0_P0_R42_D[2]		Sticky	Right ADC Overflow Flag
B0_P0_R42_D[1]		Sticky	ADC Barrel Shifter Overflow Flag
B0_P0_R44_D[7]		Sticky	Over Current Flag for HPL, RECP and SPK Drivers
	B0_P1_R69_D[7]	Sticky	Over Current Flag for RECP Driver
	B0_P1_R69_D[6]	Sticky	Over Current Flag for HPL Driver
	B0_P1_R69_D[5]	Sticky	Over Current Flag for SPK Driver
B0_P0_R44_D[6]		Sticky	Over Current Flag for HPR and RECM
B0_P0_R44_D[5]		Sticky	Button Press Flag
B0_P0_R44_D[4]		Sticky	Headset Insertion/Removal Detected Flag
	B0_P0_R37_D[5:4]	Status	Mic Presence on Inserted Headset Status
	B0_P0_R37_D[1:0]	Status	Headphone Load Status
B0_P0_R44_D[1]		Sticky	miniDSP_D Standard Interrupt Port Flag
B0_P0_R44_D[0]		Sticky	miniDSP_D Auxilliary Interrupt Port Flag
B0_P0_R45_D[7]		Sticky	SPK Driver Over Temperature Flag
B0_P0_R45_D[6]		Sticky	Left AGC Noise Detect Flag
B0_P0_R45_D[5]		Sticky	Right AGC Noise Detect Flag
B0_P0_R45_D[4]		Sticky	miniDSP_A Standard Interrupt Port Flag
B0_P0_R45_D[3]		Sticky	miniDSP_A Auxilliary Interrupt Port Flag
B0_P0_R50_D[2]		Sticky	SAR ADC Data Available Flag
	B0_P0_R9_D[5]	Status	SAR ADC Data Available Status
	B0_P0_R10_D[7]	Status	SAR ADC IN1L/AUX1 New Converted Data Available Status
	B0_P0_R10_D[6]	Status	SAR ADC IN1R/AUX2 New Converted Data Available Status
	B0_P0_R10_D[5]	Status	SAR ADC VBAT New Converted Data Available Status
	B0_P0_R10_D[1]	Status	SAR ADC TEMP1 New Converted Data Available Status
	B0_P0_R10_D[0]	Status	SAR ADC TEMP2 New Converted Data Available Status
B0_P0_R50_D[1]		Sticky	SAR ADC Threshold Exceed Flag
	B0_P3_R21_D[5]	Status	SAR ADC IN1L/AUX1 Max. Threshold Compare Status
	B0_P3_R21_D[4]	Status	SAR ADC IN1L/AUX1 Min. Threshold Compare Status
	B0_P3_R21_D[3]	Status	SAR ADC IN1R/AUX2 Max. Threshold Compare Status
	B0_P3_R21_D[2]	Status	SAR ADC IN1R/AUX2 Min. Threshold Compare Status
	B0_P3_R21_D[1]	Status	SAR ADC TEMP Max. Threshold Compare Status
	B0_P3_R21_D[0]	Status	SAR ADC TEMP Min. Threshold Compare Status

In addition to the interrupt flags, the TLV320AIC3268 features additional status flags which are very helpful for diagnostics since they enable reporting of the status of various internal blocks of the device. Table 42 provides list of the other flags available in TLV320AIC3268.

Table 42. Miscellaneous Flags

Flag Register	Type	FLAG Details
B0_P0_R36_D[7]	Status	Left ADCPGA Gain Status
B0_P0_R36_D[6]	Status	Left ADC Power Status
B0_P0_R36_D[5]	Sticky	Left AGC Gain Saturation Flag
B0_P0_R36_D[3]	Status	Right ADCPGA Gain Status
B0_P0_R36_D[2]	Status	Right ADC Power Status
B0_P0_R36_D[1]	Sticky	Right AGC Gain Saturation Flag
B0_P0_R37_D[7]	Status	Left DAC Power Status
B0_P0_R37_D[3]	Status	Right DAC Power Status

Table 42. Miscellaneous Flags (continued)

Flag Register	Type	FLAG Details
B0_P0_R38_D[6]	Status	Left DAC Volume Control Mute Status
B0_P0_R38_D[4]	Status	Left DAC Volume Control Soft-stepping Status
B0_P0_R38_D[2]	Status	Right DAC Volume Control Mute Status
B0_P0_R38_D[0]	Status	Right DAC Volume Control Soft-stepping Status
B0_P1_R62_D[1]	Status	Left ADCPGA Gain Status
B0_P1_R62_D[0]	Status	Right ADCPGA Gain Status
B0_P1_R63_D[7]	Status	HPL Driver Gain Status
B0_P1_R63_D[6]	Status	HPR Driver Gain Status
B0_P1_R63_D[5]	Status	RECP Driver Gain Status
B0_P1_R63_D[4]	Status	RECM Driver Gain Status
B0_P1_R64_D[7]	Status	LOL to HPL Volume Control Status
B0_P1_R64_D[6]	Status	LOR to HPR Volume Control Status
B0_P1_R64_D[5]	Status	LOL to RECP Volume Control Status
B0_P1_R64_D[4]	Status	LOR to RECM Volume Control Status
B0_P1_R64_D[3]	Status	LOL to SPK Volume Control Status
B0_P1_R64_D[0]	Status	Charge Pump Power Status
B0_P1_R65_D[7]	Status	IN1L to RECP Volume Control Status
B0_P1_R65_D[6]	Status	IN1R to RECM Volume Control Status
B0_P1_R65_D[5]	Status	Left ADCPGA to MAL Volume Control Status
B0_P1_R65_D[4]	Status	Right ADCPGA to MAR Volume Control Status
B0_P1_R66_D[7]	Status	LOL Driver Power Up Status
B0_P1_R66_D[6]	Status	LOR Driver Power Up Status
B0_P1_R66_D[5]	Status	HPL Driver Power Up Status
B0_P1_R66_D[4]	Status	HPR Driver Power Up Status
B0_P1_R66_D[3]	Status	RECP Driver Power Up Status
B0_P1_R66_D[2]	Status	RECM Driver Power Up Status
B0_P1_R66_D[1]	Status	SPK Driver Power Up Status

Sticky Flags are useful for reporting events which could be intermittent. These flags are set by the triggering events like over-current detect but are reset only when the flag register is read back the user. Status Flags on the other hand are useful for reporting events which are steady state in nature like power-up status of a block. The flag value reflects the triggering event's status when the register is being read by the user.

8.3.9 Interfaces

8.3.9.1 Control Interfaces

The TLV320AIC3268 control interface supports SPI or I^2C communication protocols. For SPI, the SPI_SELECT terminal should be tied high; for I^2C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

8.3.9.1.1 I^2C Control Mode

The TLV320AIC3268 supports the I^2C control protocol, and will respond by default (I2C_ADDR_SCLK grounded) to the 7-bit I^2C address of 0011000. With the one I^2C address terminal, I2C_ADDR_SCLK, the device can be configured to respond to one of two 7-bit I^2C addresses, 0011000 or 0011001. The full 8-bit I^2C address can be calculated as:

8-Bit I^2C Address = "001100" + I2C_ADDR_SCLK + R/W

Example: to write to the TLV320AIC3268 with I2C_ADDR_SCLK = 1 the 8-Bit I^2C Address is "001100" + I2C_ADDR_SCLK + R/W = "00110010" = 0x32

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the TLV320AIC3268 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver's shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3268 can also respond to and acknowledge a General Call, which consists of the master issuing a command with a slave address byte of 00H. This feature is disabled by default, but can be enabled via B0_P0_R115_D5.

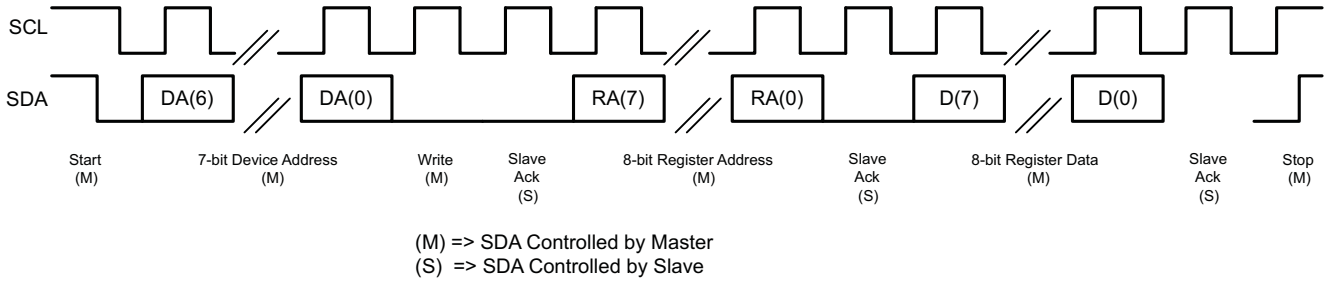


Figure 78. I²C Write

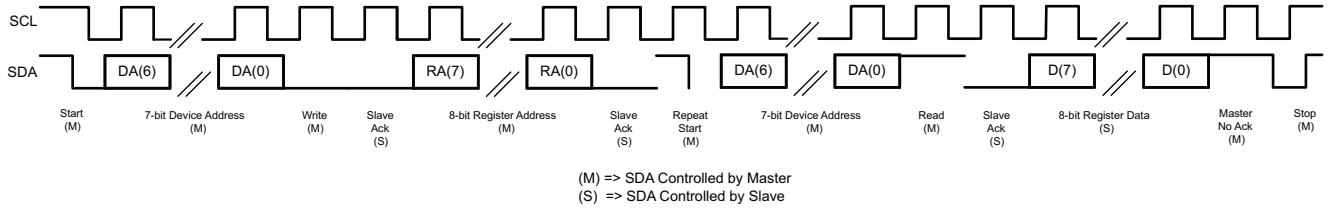


Figure 79. I²C Read

In the case of an I²C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I²C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

8.3.9.1.2 SPI Digital Interface

In the SPI control mode, the TLV320AIC3268 uses the terminals SCL_SSZ as $\overline{SS}$, I2C_ADDR_SCLK as SCLK, MISO_GPO1 as MISO, SDA_MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0) and clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3268) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI terminal under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI terminal, a byte shifts out on the MISO terminal to the master shift register.

The TLV320AIC3268 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI terminal and the slave begins driving its MISO terminal on the first serial clock edge. The SSZ terminal can remain low between transmissions; however, the TLV320AIC3268 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TLV320AIC3268 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI terminal of the part prior to the data for that register. The command is structured as shown in Table 43. The first 7 bits specify the address of the register which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction

of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI terminal and contains the data to be written to the register. Reading of registers is accomplished in a similar fashion. The 8-bit command word sends the 7-bit register address, followed by the R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO terminal during the second 8 SCLK clocks in the frame.

Table 43.

COMMAND WORD

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

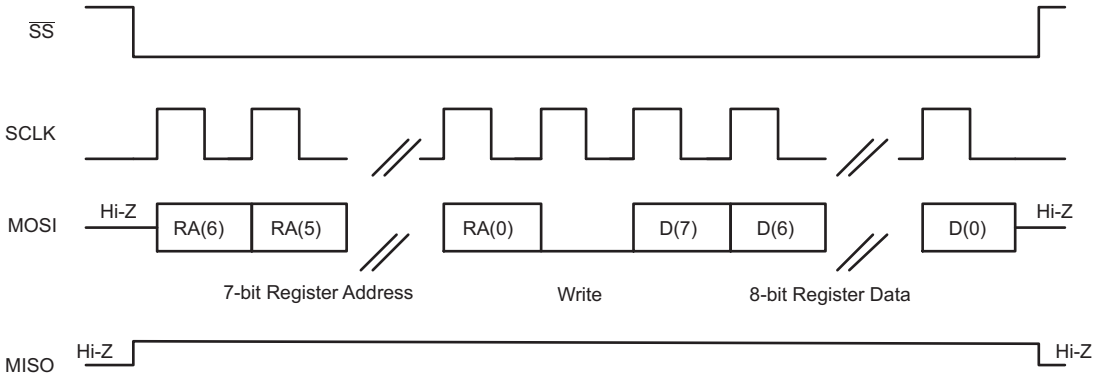


Figure 80. SPI Timing Diagram for Register Write

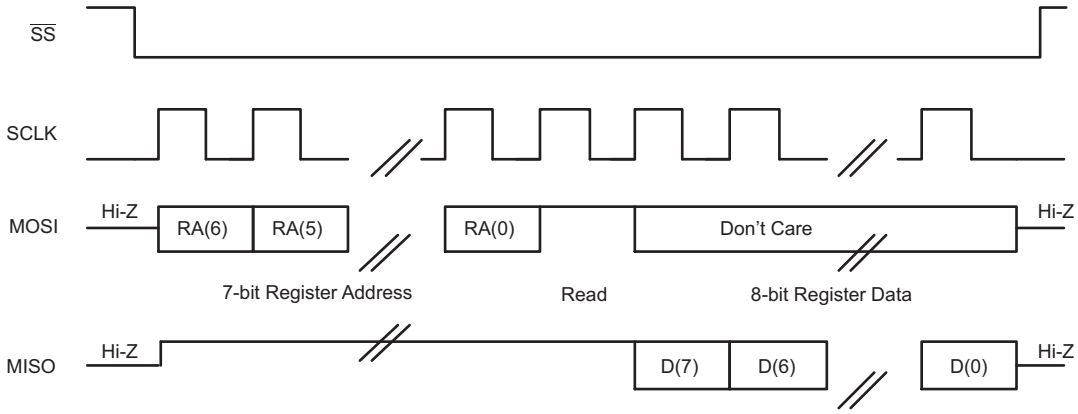


Figure 81. SPI Timing Diagram for Register Read

8.3.9.2 Digital Audio Interfaces

The TLV320AIC3268 features three digital audio data serial interfaces, or audio buses. These three interfaces can be run simultaneously, thereby enabling reception and transmission of digital audio for or to three separate devices. A common example of usage of multiple digital audio serial interfaces is to allow connections with application processor, bluetooth chipset, digital input Class-D amplifiers and so forth. By utilizing the TLV320AIC3268 as the center of the audio processing in a portable audio system, mixing of voice and music audio is greatly simplified. In addition, the miniDSP can be utilized to greatly enhance the portable device experience by providing advanced audio processing to both communication and media audio streams simultaneously.

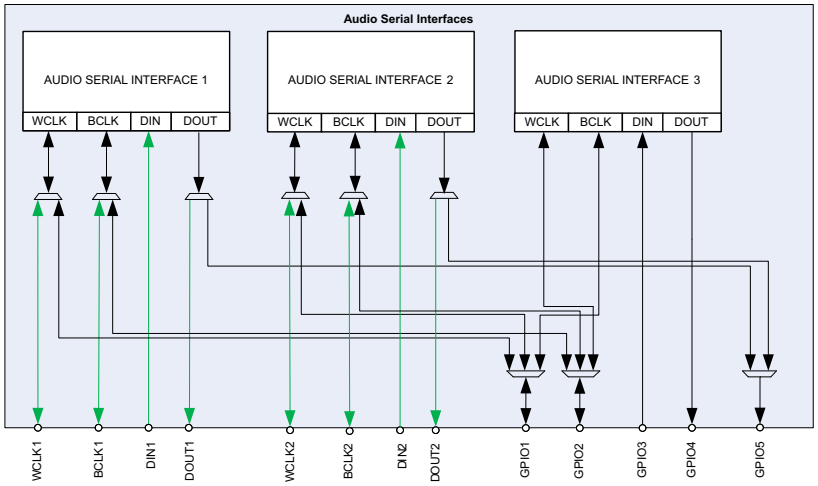


Figure 82. Typical Multiple Connections to Three Audio Serial Interfaces

Each audio bus on the TLV320AIC3268 is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master or slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

Each of the three audio buses of the TLV320AIC3268 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate word clocks.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3268s may share the same audio bus. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate bit clocks.

The TLV320AIC3268 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks.

The TLV320AIC3268 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen.

The TLV320AIC3268 further includes programmability to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the terminals associated with the interface are put into a 3-state output condition.

By default, when the word-clocks and bit-clocks are generated by the TLV320AIC3268, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

The TLV320AIC3268 contains advanced Digital Audio interfaces features to enable:

- Connections of Multiple Digital Audio interfaces
- 6-wire Digital Audio interfaces for separate uplink/downlink clocks or ADC/DAC clocks

- Multi-channel, Multiple terminal operation

8.3.9.2.1 Connecting Multiple Audio Digital Interfaces

The TLV320AIC3268 enables connections to multiple audio data buses. Figure 82 shows a typical example of utilizing the digital terminals on the device to connect to four separate 4-wire digital audio buses, with up to three of these 4-wire buses receiving and sending digital audio data simultaneously. This configuration can be utilized when using I^2C for control of the device. If only 3 total audio interface connections are needed (that is, a fourth audio bus does not need to be muxed into Audio Serial Interface 1), either I^2C or SPI control can be used. (Further details on SPI control and terminals utilized can be found in SPI Digital Interface and Table 47.)

To configure each of the three audio serial interfaces, both the audio interface and the terminals should be set up for appropriate routing of the signals. Audio Serial Interface 1 configuration registers are located in B0_P4_R1-R16 and B0_P4_R49-R52. Audio Serial Interface 2 configuration registers are located in B0_P4_R17-R32 and B0_P4_R53-R54. Audio Serial Interface 3 configuration registers are located in B0_P4_R33-R48 and B0_P4_R55-R56. The terminal muxing registers are located in B0_P4_R65-R96. Table 44 displays the appropriate register settings needed to implement the Audio Serial Interface configuration found in Figure 82.

Table 44. Register Settings for Typical Multiple Audio Digital Interface Connections

TERMINAL	Interface Control (Codec Interface is Slave)	Interface Control (Codec Interface is Master)	Terminal Control (Codec Interface as Slave)	Terminal Control (Codec Interface as Master)
Audio Serial Interface 1 Word Clock to WCLK1 Terminal	B0_P4_R10_D[7:5] = 000	B0_P4_R10_D[7:5] = 001	B0_P4_R65_D[5:2] = 0001	
Audio Serial Interface 1 Bit Clock to BCLK1 Terminal	B0_P4_R10_D[4:2] = 000	B0_P4_R10_D[4:2] = 001	N/A	
Audio Serial Interface 1 Data Input to DIN1 Terminal	B0_P4_R49_D[4:0] = 00001 (default) B0_P4_R8_D[7:4] = 0101 (default) (ASI1-to-DAC datapath)		B0_P4_R68_D[6:5] = 01 (default)	
Audio Serial Interface 1 Data Output to DOUT1 Terminal	B0_P4_R15_D[1:0] = 00 (default) B0_P4_R7_D[2:0] = 001 (default)		B0_P4_R67_D[4:1] = 0001 (default)	
Audio Serial Interface 2 Word Clock to WCLK2 Terminal	B0_P4_R26_D5 = 0 (default)	B0_P4_R26_D5 = 1	B0_P4_R69_D[5:2] = 0001 (default)	
Audio Serial Interface 2 Bit Clock to BCLK2 Terminal	B0_P4_R26_D2 = 0 (default)	B0_P4_R26_D2 = 1	B0_P4_R70_D[5:2] = 0001 (default)	
Audio Serial Interface 2 Data Input to DIN2 Terminal	B0_P4_R24_D[7:4] = 0101 (ASI2-to-DAC datapath)		B0_P4_R72_D[6:5] = 01	
Audio Serial Interface 2 Data Output to DOUT2 Terminal	B0_P4_R23_D[2:0] = 101 (ADC-to-ASI2 routing - Port 2), B0_P4_R31_D[1:0] = 00 (default)		B0_P4_R71_D[4:1] = 0001 (default)	
Audio Serial Interface 3 Word Clock to GPIO2 Terminal	B0_P4_R55_D[6:5] = 10		B0_P4_R87_D[6:2] = 10100	B0_P4_R87_D[6:2] = 00001
Audio Serial Interface 3 Bit Clock to GPIO1 Terminal	B0_P4_R55_D[2:0] = 001		B0_P4_R86_D[6:2] = 10101	B0_P4_R86_D[6:2] = 00001

Table 44. Register Settings for Typical Multiple Audio Digital Interface Connections (continued)

TERMINAL	Interface Control (Codec Interface is Slave)	Interface Control (Codec Interface is Master)	Terminal Control (Codec Interface as Slave)	Terminal Control (Codec Interface as Master)
Audio Serial Interface 3 Data Input to GPIO3 Terminal	B0_P4_R40_D[7:4] = 0101 (ASI3-to-DAC datapath)		B0_P4_R88_D[6:2] = 11101	
Audio Serial Interface 3 Data Output to GPIO4 Terminal	B0_P4_R39_D[2:0] = 110 (ADC-to-ASI3 routing - Port 3) B0_P4_R47_D[1:0] = 00 (default)		B0_P4_R89_D[6:2] = 11101	

Since each interface can be configured separately as master or slave, the appropriate settings are displayed for both possible configurations for each of the three audio serial interfaces. When in master mode, the bit clock and work clock source can be derived from a variety of sources, and more details on the possible sources of these clocks can be found in the Clock Generation and PLL section.

8.3.9.2.2 Six-Wire Digital Audio Interface

The six-wire audio interface mode allows independent configuration of receive and transmit word and bit clocks for the device. The TLV320AIC3268 supports six-wire audio interface on ASI1 and ASI2. The six-wire inteface mode is available in all interface formats such as I2S, LJF, RJF, DSP and PCM modes. Due to terminal limitations, only one of ASI1 or ASI2 can operate in six-wire mode at a time.

When ASI1 operates in six-wire mode, WCLK1 functions as DAC_WCLK or receive word clock, BCLK1 functions as DAC_BCLK or receive bit clock. The tranmist word clock and transmit bit clock function can get supported on any of the pair of terminals amongst GPIO1, GPIO2, GPIO3 or GPIO4.

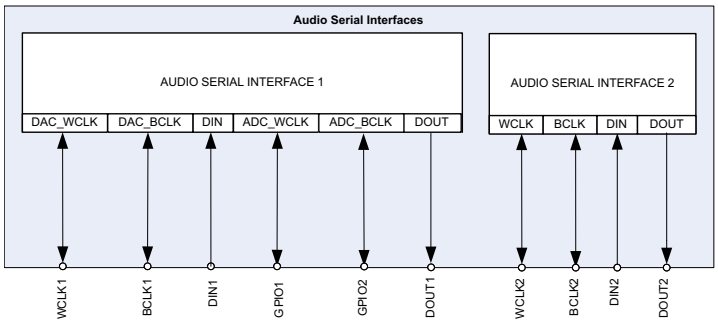


Figure 83. Six-Wire Audio Serial Interface with ASI1

When ASI2 operates in six-wire mode, WCLK1 functions as DAC_WCLK or receive word clock, BCLK1 functions as DAC_BCLK or receive bit clock. The tranmist word clock and transmit bit clock function can get supported on any of the pair of terminals amongst GPIO1, GPIO2, GPIO3 or GPIO4.

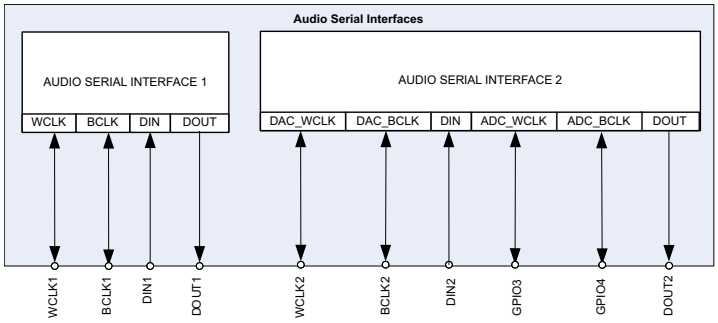


Figure 84. Six-Wire Audio Serial Interface with ASI2

The details of register settings to enable six-wire interface mode are shown in Table 51.

8.3.9.2.3 Multiple Channel, Multiple Terminal Setup

The TLV320AIC3268 also enables connections of up to four stereo pairs (8 total channels) of input and output data on Audio Serial Interface 1. These eight bidirectional channels are all synchronized to a single word clock (WCLK1) and bit clock (BCLK1). Figure 85 displays a typical configuration for this multi-channel setup.

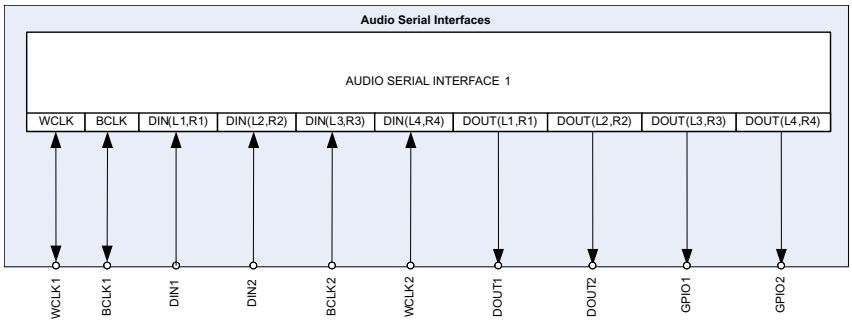


Figure 85. Multi-channel, Multi-Terminal Inputs and Outputs to Audio Serial Interface 1

Table 45. Register Settings for Replacing ASI2 and ASI3 with Multi-Channel Connections

Terminal	Interface Control	Terminal Control
Audio Serial Interface 1 DIN_1 Input to DIN1 Terminal	To configure to 8 channels - B0_P4_R4_D[7:6] = 11 To configure multiterminal mode - B0_P4_R6_D[7] = 1 To configure input routings for DIN1 - B0_P4_R49_D[4:0] = 00001 To configure input routings for DIN2 - B0_P4_R50_D[4:0] = 00010 To configure input routings for BCLK2 - B0_P4_R51_D[4:0] = 01100 To configure input routings for WCLK2 - B0_P4_R51_D[4:0] = 01110	B0_P4_R68_D[6:5] = 01 (default)
Audio Serial Interface 1 DIN_2 Input to DIN2 (1)terminal		B0_P4_R72_D[6:5] = 01 (default)
Audio Serial Interface 1 DIN_3 Input to BCLK2(1) terminal		B0_P4_R70_D[5:2] = 1110
Audio Serial Interface 1 DIN_4 Input to WCLK2(1) terminal		B0_P4_R69_D[5:2] = 1111
Audio Serial Interface 1 DOUT_1 Input to DOUT1 terminal	To configure to 8 channels - B0_P4_R4_D[7:6] = 11 To configure multiterminal mode - B0_P4_R6_D[7] = 1	B0_P4_R67_D[4:1] = 0001 (default)
Audio Serial Interface 1 DOUT_2 Input to DOUT2(1) terminal		B0_P4_R71_D[4:1] = 1101
Audio Serial Interface 1 DOUT_3 Input to GPIO1 terminal		B0_P4_R86_D[6:2] = 01110
Audio Serial Interface 1 DOUT_4 Input to GPIO2 terminal		B0_P4_R87_D[6:2] = 01111

(1) BCLK2, WCLK2, DIN2 and DOUT2 terminals are with respect to IOVDD2 supply therefore using with ASI-1 in multiterminal 8-ch mode requires either shorting IOVDD1 and IOVDD2 with same voltage level or putting on-board level-shifter for the above signals.

The configuration shown in Figure 85 can be used with either I^2C or SPI for control interface. In this configuration ASI2 and ASI3 cannot be used. Other combinations with reduced channels or I^2C only control interface allow simultaneous use of ASI2 or ASI3 by choosing different set of terminals. For details of various functions supported on terminals, see Table 47.

8.3.9.2.4 Audio Formats

Each Audio Serial Interface supports left or right-justified, I^2S, DSP, or mono PCM modes. In addition, time-division multiplexing (TDM) can be implemented in each of these formats to enable multi-channel operation.

8.3.9.2.4.1 Right Justified Mode

Audio Serial Interface 1 can be put into Right Justified Mode by programming B0_P4_R1_D[7:5] = 010. Audio Serial Interface 2 can be put into Right Justified Mode by programming B0_P4_R17_D[7:5] = 010. Audio Serial Interface 3 can be put into Right Justified Mode by programming B0_P4_R33_D[7:5] = 010. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

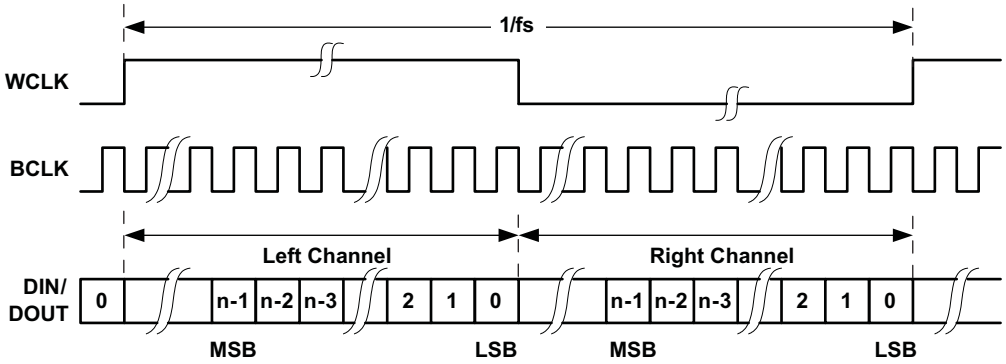


Figure 86. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

8.3.9.2.4.2 Left Justified Mode

Audio Serial Interface 1 can be put into Left Justified Mode by programming B0_P4_R1_D[7:5] = 011. Audio Serial Interface 2 can be put into Left Justified Mode by programming B0_P4_R17_D[7:5] = 011. Audio Serial Interface 3 can be put into Left Justified Mode by programming B0_P4_R33_D[7:5] = 011. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

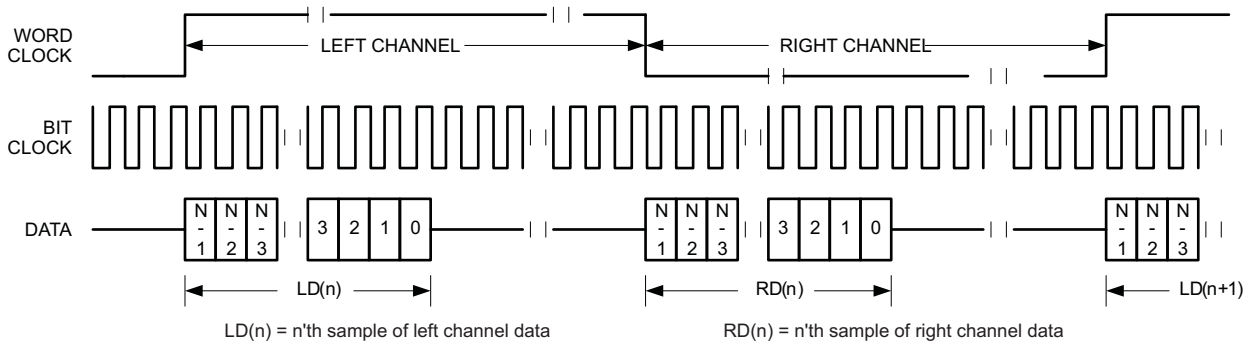


Figure 87. Timing Diagram for Left-Justified Mode

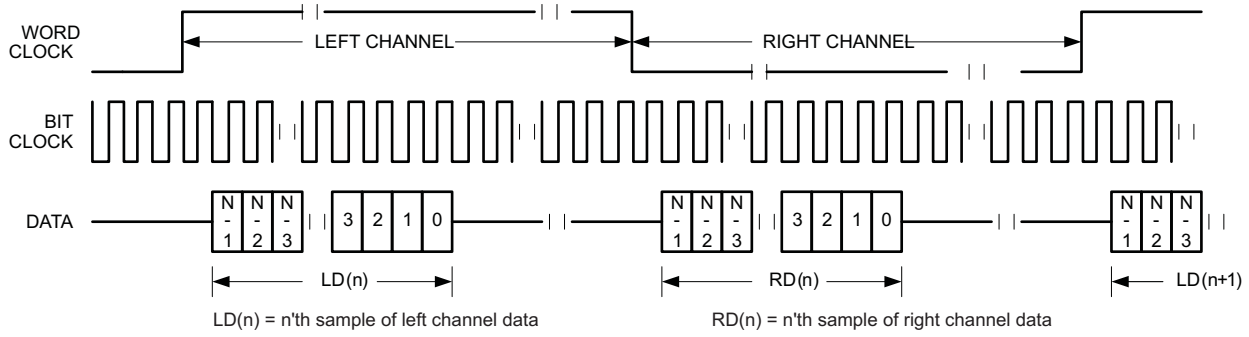


Figure 88. Timing Diagram for Left-Justified Mode with Offset=1

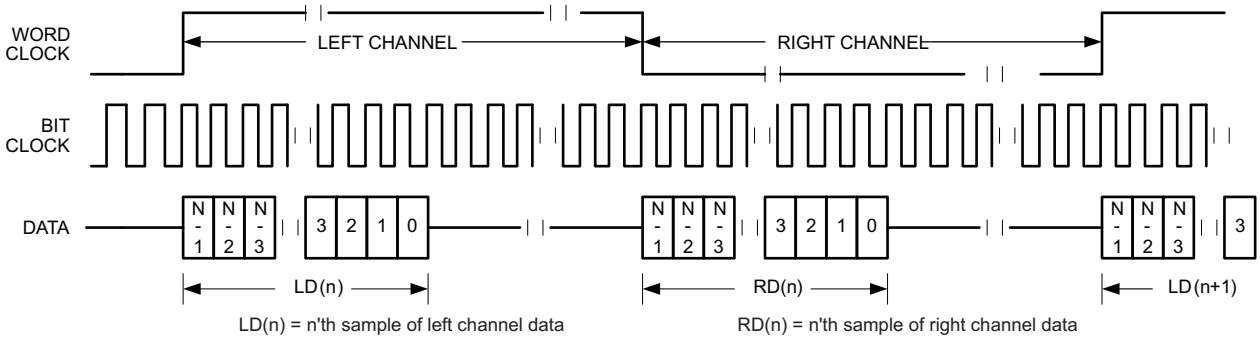


Figure 89. Timing Diagram for Left-Justified Mode with Offset=0 and Inverted Bit Clock

For Left-Justified mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

8.3.9.2.4.3 I²S Mode

Audio Serial Interface 1 can be put into I²S Mode by programming B0_P4_R1_D[7:5] = 000. Audio Serial Interface 2 can be put into I²S Mode by programming B0_P4_R17_D[7:5] = 000. Audio Serial Interface 3 can be put into I²S Mode by programming B0_P4_R33_D[7:5] = 000. In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

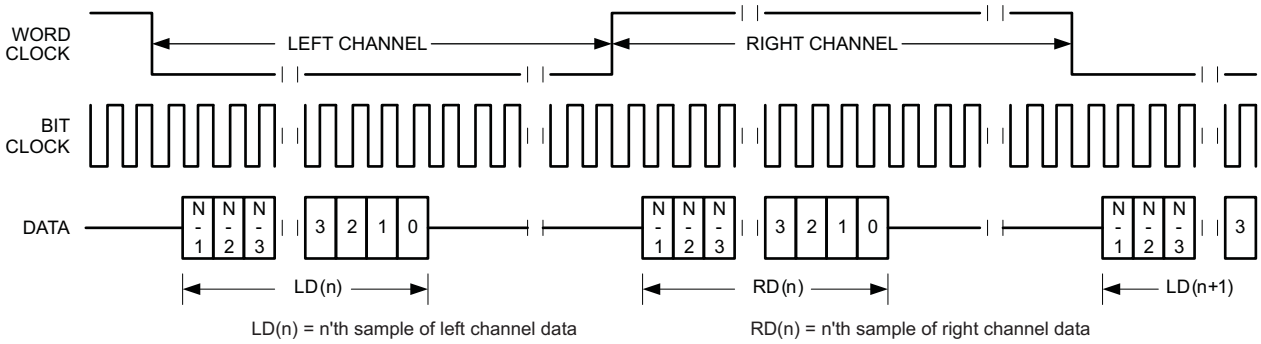


Figure 90. Timing Diagram for I²S Mode

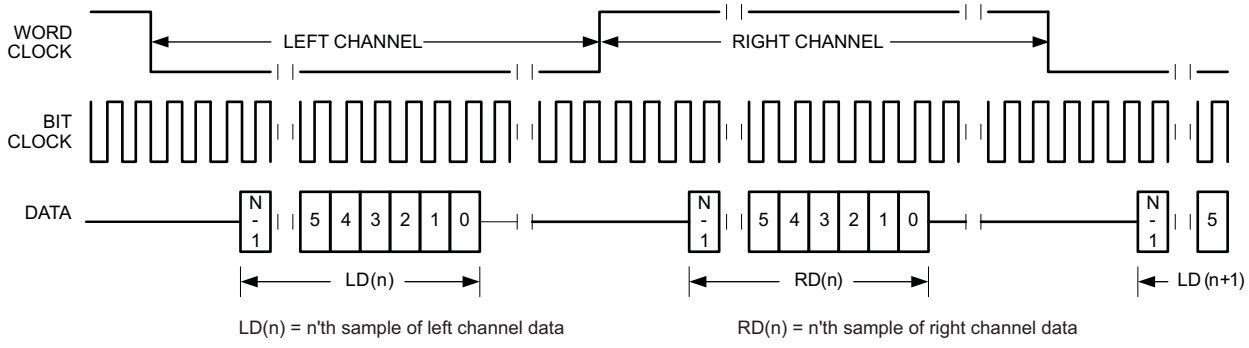


Figure 91. Timing Diagram for I²S Mode with Offset=2

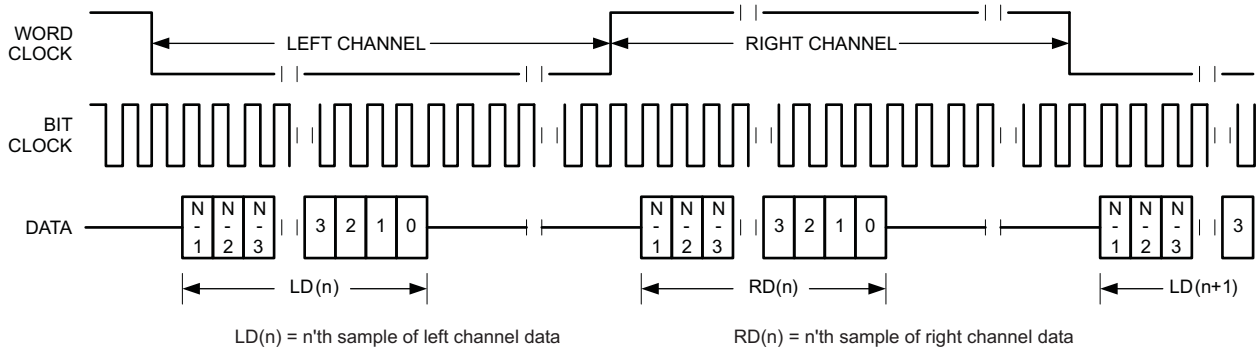


Figure 92. Timing Diagram for I²S Mode with Offset=0 and Bit Clock Inverted

For I²S mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

8.3.9.2.4.4 DSP Mode

Audio Serial Interface 1 can be put into DSP Mode by programming B0_P4_R1_D[7:5] = 001. Audio Serial Interface 2 can be put into DSP Mode by programming B0_P4_R17_D[7:5] = 001. Audio Serial Interface 3 can be put into DSP Mode by programming B0_P4_R33_D[7:5] = 001. In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

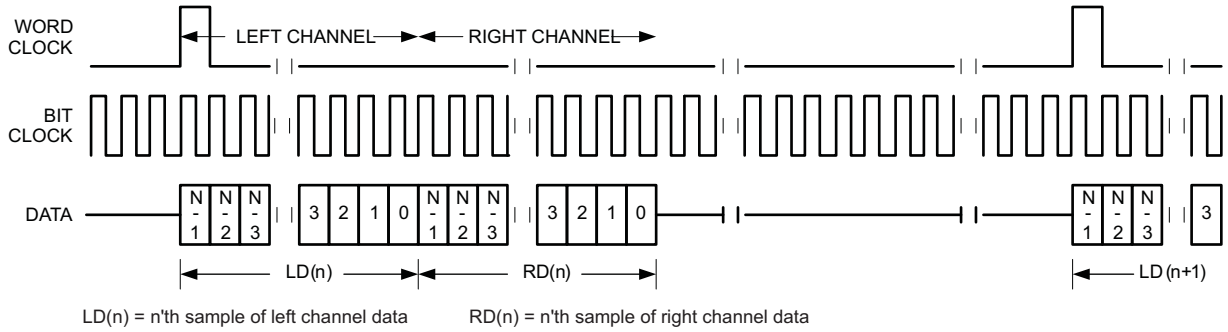


Figure 93. Timing Diagram for DSP Mode

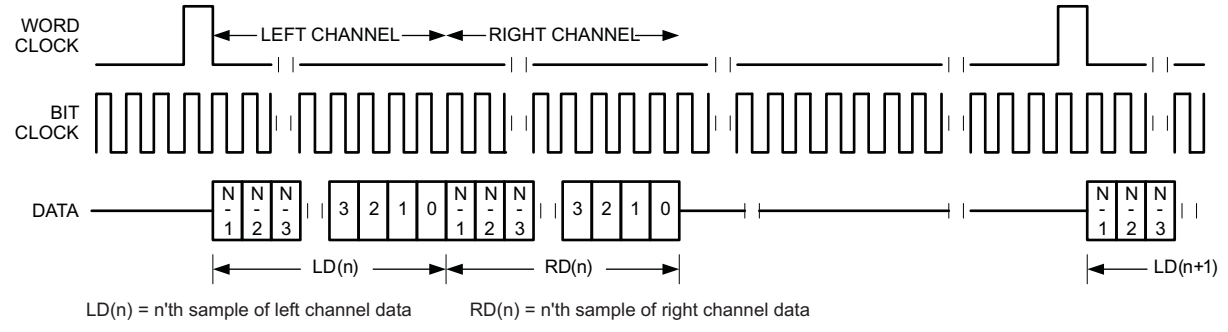


Figure 94. Timing Diagram for DSP Mode with Offset = 1

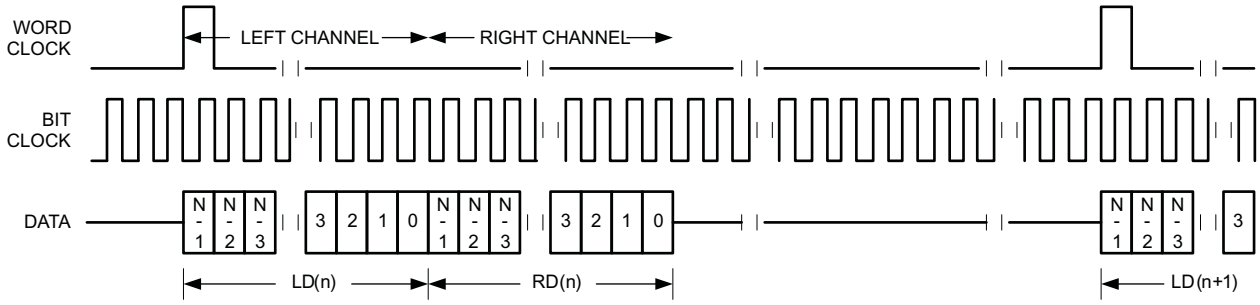


Figure 95. Timing Diagram for DSP Mode with Offset = 0 and Bit Clock Inverted

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

8.3.9.2.4.5 Mono PCM Mode

Audio Serial Interface 1 can be put into Mono PCM Mode by programming B0_P4_R1_D[7:5] = 100. Audio Serial Interface 2 can be put into DSP Mode by programming B0_P4_R17_D[7:5] = 100. Audio Serial Interface 3 can be put into DSP Mode by programming B0_P4_R33_D[7:5] = 100. In mono PCM mode, the rising edge of the word clock starts the data transfer of the single channel of data. Each data bit is valid on the falling edge of the bit clock.

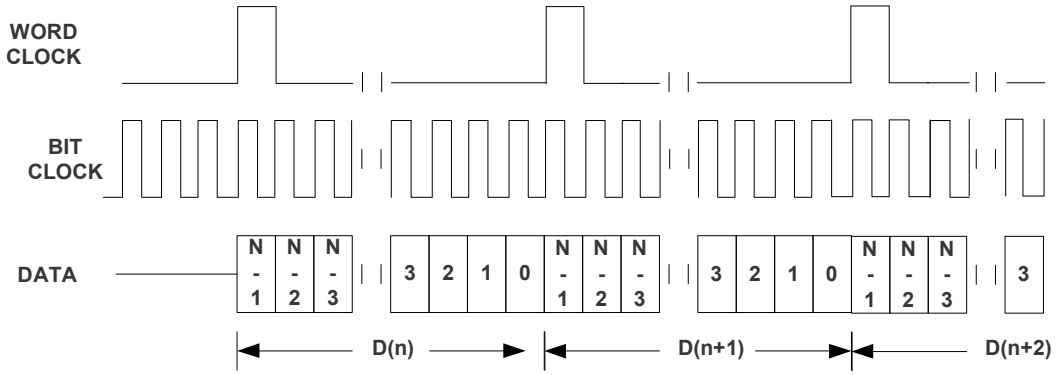


Figure 96. Timing Diagram for Mono PCM Mode

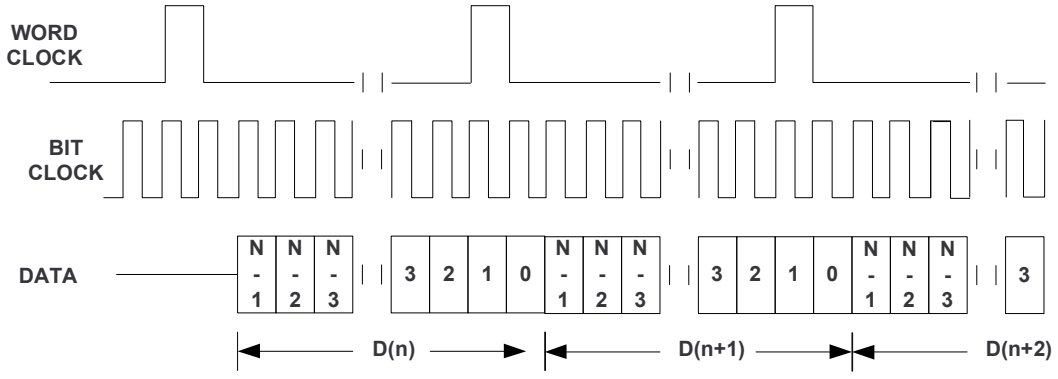


Figure 97. Timing Diagram for Mono PCM Mode with Offset=2

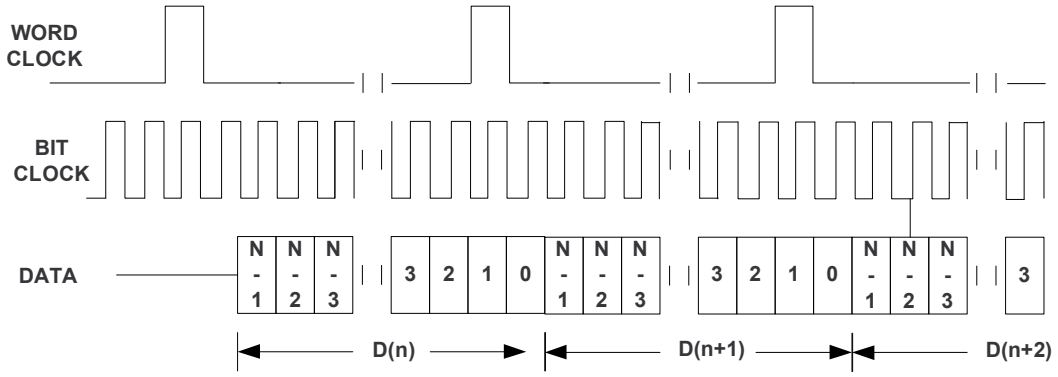


Figure 98. Timing Diagram for Mono PCM Mode with Offset=2 and Bit Clock Inverted

For mono PCM mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

8.3.9.2.5 Multi-channel Configurations

The TLV320AIC3268 can utilize TDM techniques to enable several multi-channel system scenarios. First, multiple codecs can transmit/receive on a single digital audio interface bus. Second, multiple stereo pairs can be sent and received by a single TLV320AIC3268 on a single 4-wire digital audio interface bus. Lastly, up to 4 individual stereo data pairs to/from the TLV320AIC3268 can be routed to individual DIN and DOUT lines in the system which are synchronized to a single BCLK and WCLK.

8.3.9.2.5.1 Single Host, Multiple Audio Codecs

Using the offset programmability and the DOUT line 3-state feature, the TLV320AIC3268 enables the flexibility where multiple TLV320AIC3268 devices can be interfaced together and can communicate to a host/multimedia processor using a single digital audio serial interface. Figure 99 displays a typical configuration where M devices are connected to a single host processor.

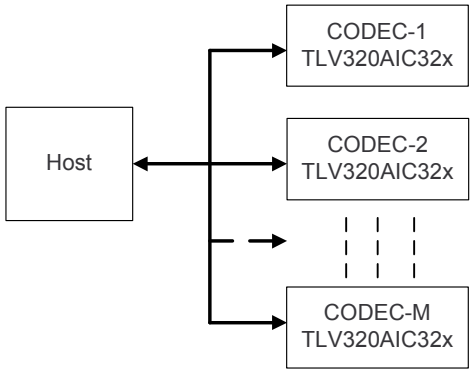


Figure 99. Interfacing Multiple TLV320AIC3268 Devices Using Single I^2S Interface

By changing the programmable offset for each device, the bit clock in each frame where the data begins can be changed, and the serial data output driver (DOUT) also can be programmed to a 3-state mode during all bit clocks except when valid data is being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected based on the programmed offset.

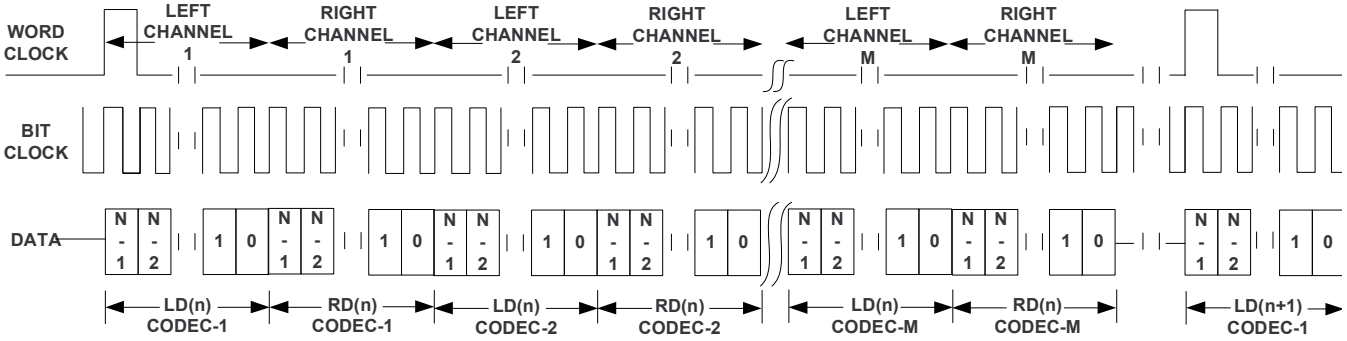


Figure 100. DSP Timing for Multiple Devices Interfaced Together, Sequential Left/Right Pairs

The digital audio serial interface timing diagram for the interface in Figure 99 is shown in Figure 100. In this particular configuration, the TLV320AIC3268 (or any other TLV320AIC32x codec) is programmed for DSP mode with N-bit word length per channel. The offset programmed for the Codec-1 is 0, for Codec-2 it is 2N, and likewise, the offset programmed for the Codec-M is (M-1) x 2N. In this TDM mode, the number of bit-clocks per frame should be greater than M*2N. The TLV320AIC3268 allows a maximum offset of 255 bit clocks, and this enables connections of up to 4 codecs for 32-bit stereo data and 8 codecs for 16-bit stereo data.

For each of the three individual Digital Audio interfaces, this offset controls when data is received and sent by these interfaces. For Audio Serial Interface 1, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R2. For Audio Serial Interface 2, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R18. For Audio Serial Interface 3, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R34. When utilized in DSP mode, each of these offsets will set the start of the left channel, with the right channel data immediately following the LSB of the left channel.

8.3.9.2.5.1.1 Time Slot Mode

In addition, Audio Serial Interface 1 can also control the offset of the right channel with respect to the end of the left channel of data. This is achieved by enabling Time Slot Mode (setting B0_P4_R8_D0) and configuring the Right Channel Offset 2 (in the range of 0 to 255 bit clocks) in B0_P4_R3. Thus, the Right Channel Offset 2 control allows us to place the right channel anywhere in the frame after the left channel, and this functionality can be utilized in each of the audio formats (DSP, left or right-justified, or I^2S).

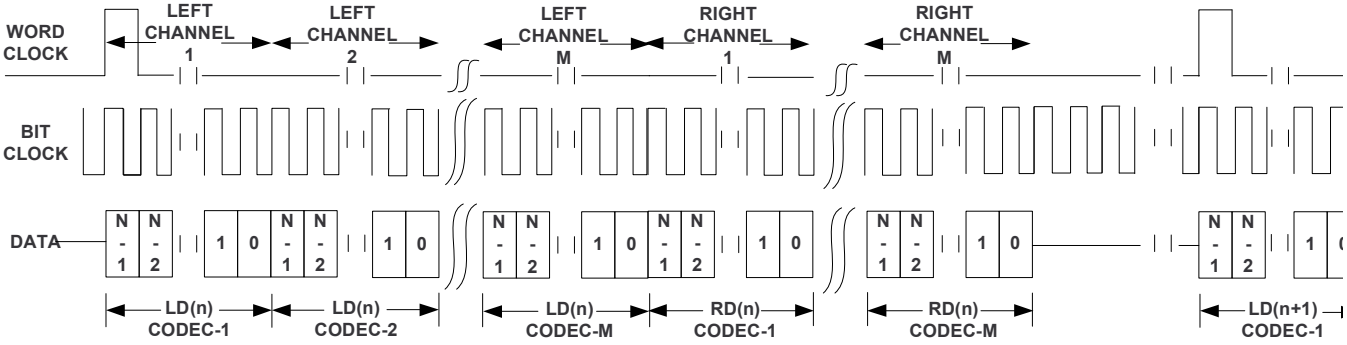


Figure 101. DSP Timing for Multiple Devices Interfaced Together, Grouped Left Channels and Right Channels

By utilizing Time Slot Mode, the individual left and right channels can be grouped together, as shown in Figure 101. Assuming each channel contains N bits in this example, Codec-1 would have an offset1=0 and offset2=M*N, Codec-2 would have an offset1=N and offset2=M*N, and likewise, Codec-M would have an offset1=(M-1)*N and offset2=M*N.

8.3.9.2.5.2 Multiple Channel Operation, Single Data Lines (Audio Serial Interface 1)

The TLV320AIC3268 can receive and send multiple stereo pairs on a single 4-wire digital audio interface bus. This particularly useful when sending multi-channel audio data to the miniDSP for stereo downmix and playback over the integrated stereo headphones, speakers, or line-outs. Alternatively, the host could utilize the audio miniDSP engine as a multi-channel audio co-processor. This multi-channel operation is only available on Audio Serial Interface 1, and this is enabled by increasing the number of available channels in B0_P4_R4_D[7:6] to greater than 1 stereo pair. By increasing the number of stereo pairs, the interface essentially lengthens the data length for each channel. Thus, the first half of the X channels are interpreted as Left Channels, while the second half of X channels are interpreted as Right Channels. Once these channels are inside the miniDSP, they can be interpreted as any channel for surround processing. Figure 102 shows the timing for X channels of data utilizing DOUT1 and DIN1 data lines.

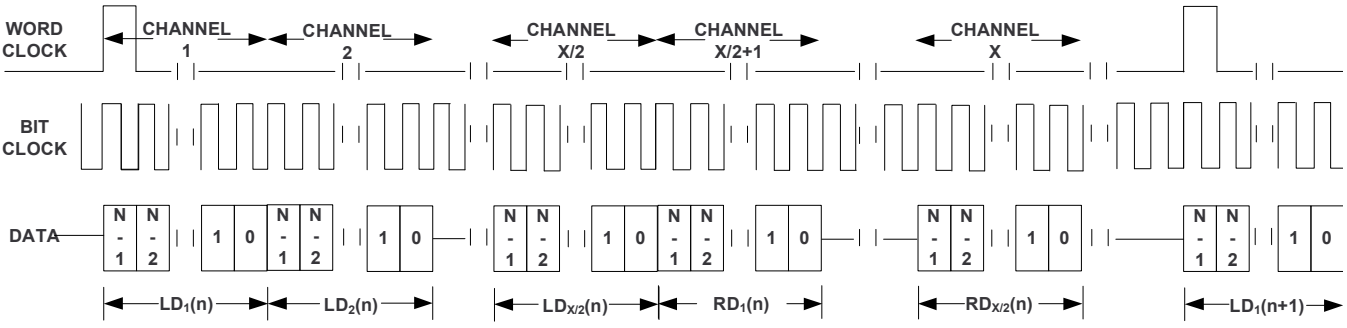


Figure 102. DSP Timing for Multi-channel Mode, Single DOUT and DIN Lines

Because Audio Serial Interface 1 interprets the first X/2 channels as Left data, the last X/2 "Right" channels can be shifted utilizing Time Slot Mode. Figure 103 shows how, in DSP mode, the start of the first X/2 channels can be delayed by one bit clock (by setting offset1=1 in B0_P4_R2), while the last X/2 "Right" channels can be delayed by two bit clocks after the end of the first X/2 "Left" channels.

For this multi-channel DSP mode, the number of bit-clocks per frame should be greater than M times the programmed word-length of the data, where M is the total number of channels set in B0_P4_R4_D[7:6]. Also the sum of the two programmed offset values should be less than the number of bit-clocks per frame by at least M times the programmed word-length of the data.

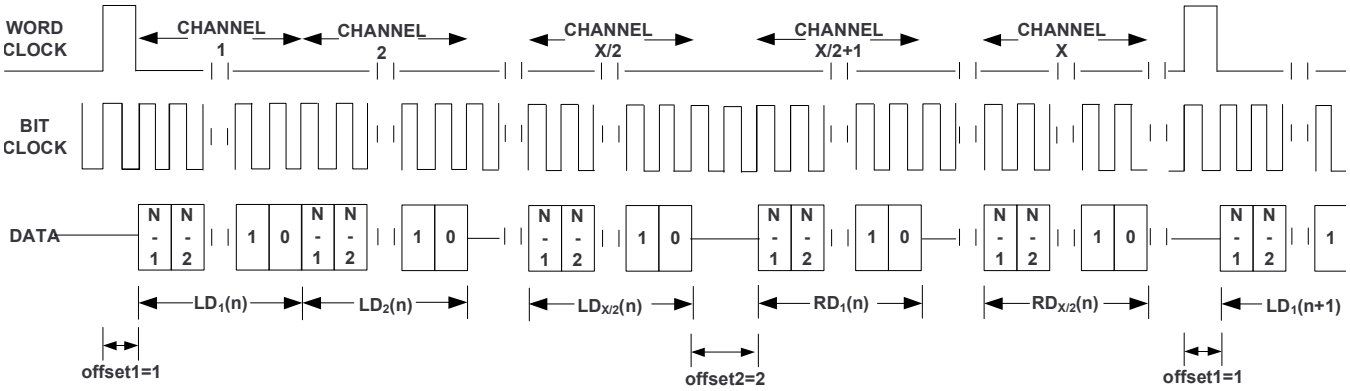


Figure 103. DSP Timing for Multi-channel Mode, Single DOUT and DIN Lines

8.3.9.2.5.3 Multiple Channel Operation, Multiple Data Lines (Audio Serial Interface 1)

The TLV320AIC3268 can receive or send up to 4 individual stereo data pairs can be routed to individual DIN and DOUT lines in the system which are synchronized to a single BCLK and WCLK. This multi-channel, multi-terminal operation is only available on Audio Serial Interface 1. The multi-terminal mode is enabled by setting B0_P4_R6_D7 to 1. In addition to routing the channels to/from the interface, the individual terminals also need to be configured (refer to Table 46 and Table 47 for possible digital terminal muxing setups). Just as in the multi-channel, single-terminal case, the audio serial interface should configure the appropriate number of channels by writing to B0_P4_R4_D[7:6]. Figure 104 shows an example of multi-channel, multi-terminal mode using 4 stereo data pairs (8 channels) in DSP format.

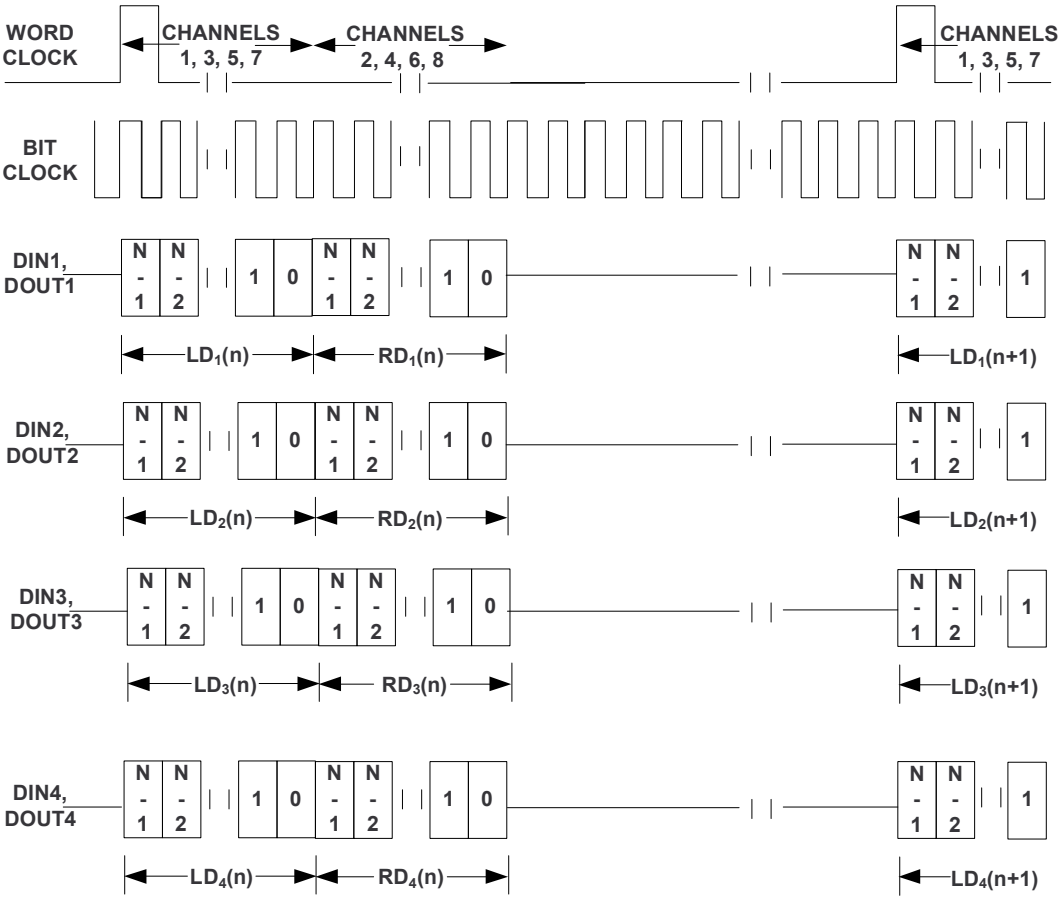


Figure 104. DSP Timing for Multi-channel Mode, Four Data Lines

For this multi-channel DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, any programmed offset1 value (for shift of start of left channel) should be less than the number of bit-clocks per frame by at least twice the programmed word-length of the data.

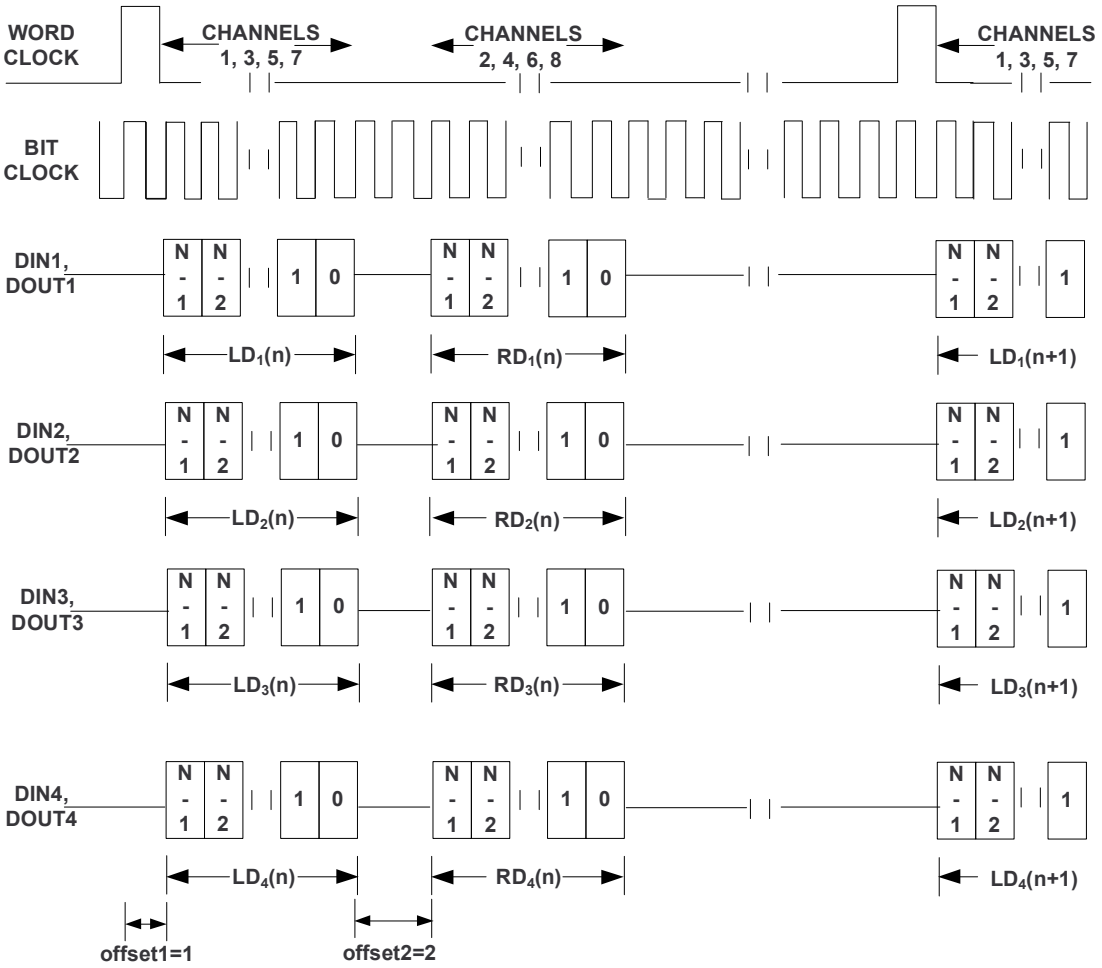


Figure 105. DSP Timing for Multi-channel Mode, Time Slot Mode, Four Data Lines with Offset1=1 and Offset2=2

By enabling Time Slot Mode, the start of the left and right channels on each data line can be controlled by offset1 and offset2. In other words, offset1 would control the start of all four left channels in Figure 105, and offset2 would delay the start of all right channels after the end of the left channels' LSB. For this multi-channel, multi-terminal DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the sum of the two programmed offset values should be less than the number of bit-clocks per frame by at least twice the programmed word-length of the data.

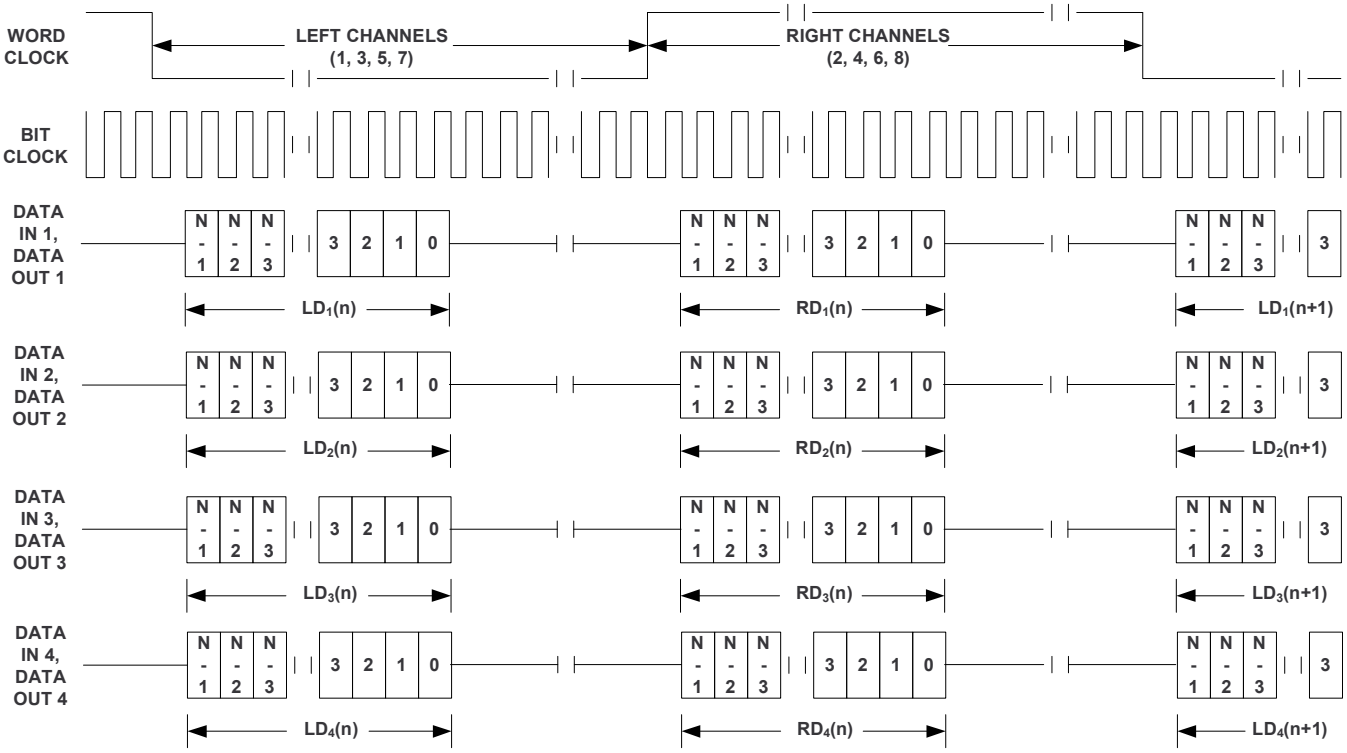


Figure 106. I²S Timing for Multi-channel Mode, Four Data Lines

On Audio Serial Interface 1, any format (DSP, left or right-justified, or I²S) can be utilized in multi-channel, multi-terminal mode. Figure 106 shows an example of multi-channel, multi-terminal mode using 4 stereo data pairs (8 channels) in I²S format.

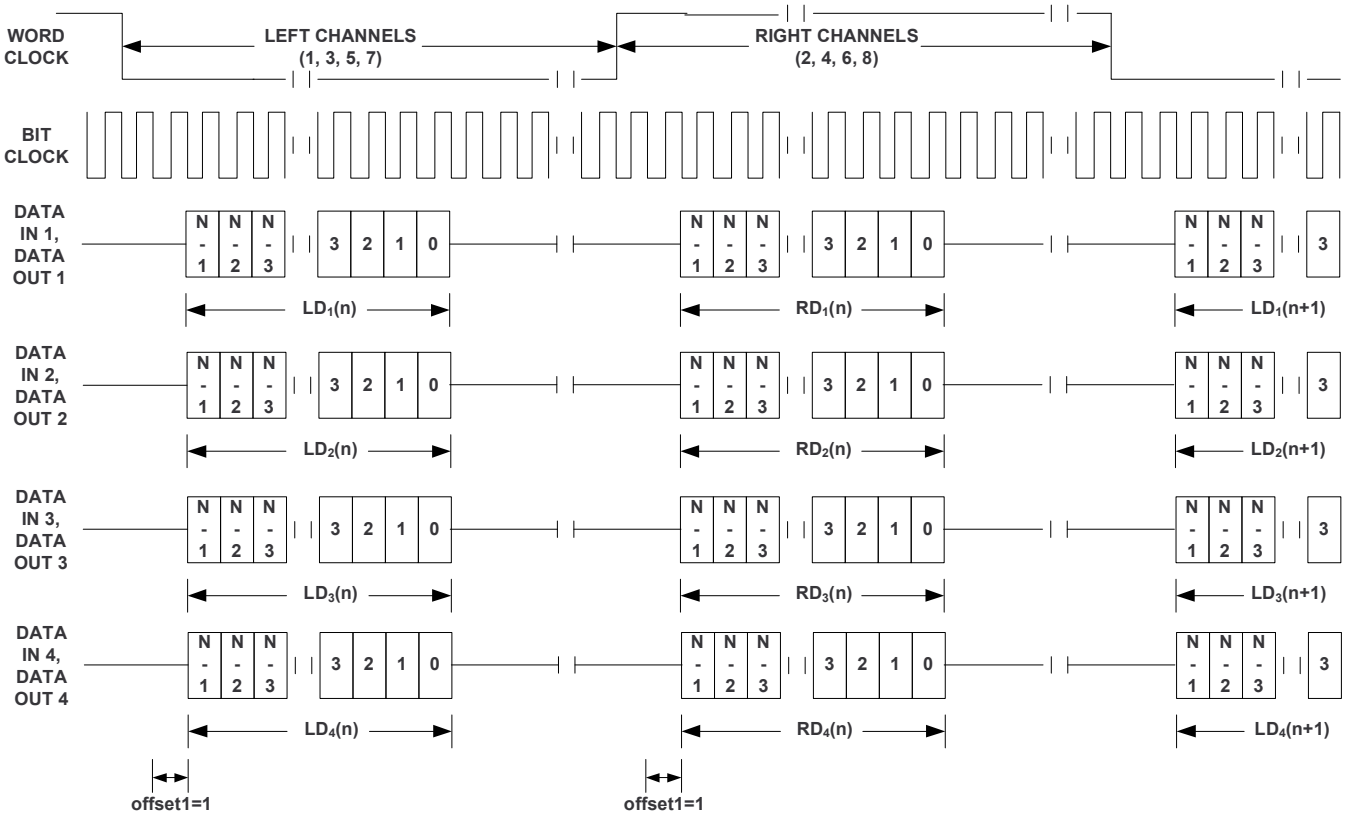


Figure 107. I²S Timing for Multi-channel Mode, Four Data Lines with Offset1=1

For I²S multi-channel, multi-terminal mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

8.3.10 miniDSP

The TLV320AIC3268 features two fully programmable miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very-low group delay DSP algorithms. Each miniDSP can run up to 1229 instructions on every audio sample at a 48kHz sample rate. The two cores can run fully synchronized and can exchange data. The miniDSPs in TLV320AIC3268 enable advanced sound enhancement algorithms on an audio device.

The TLV320AIC3268 features two fully programmable miniDSP cores and three ASI ports. The miniDSP_A is capable of generating 8 channels of audio data, which can either be routed to the ASIs to be output from the device or routed back to the miniDSP_D for a loopback function. Similarly the miniDSP_D can take in audio data from multiple ASIs or the miniDSP_A.

The miniDSP_A can generate 8 channels of data called the miniDSP_A_DataOutput[1:8]. The miniDSP_A_DataOutput[1,2,3,...,8] are also referred to as miniDSP_A_DataOutput[L1,R1,L2,...,R4]. When the device is used in pre-programmed PRB modes only miniDSP_A_DataOutput[1:2] are generated by the device for stereo modes and only miniDSP_A_DataOutput[1] is generated in the mono modes.

The miniDSP_D features 3 input ports called miniDSP_D_DataInput_1, miniDSP_D_DataInput_2 and miniDSP_D_DataInput_3. The input port miniDSP_D_DataInput_1 features 8 channels, miniDSP_D_DataInput_1[1:8], also referred to as miniDSP_D_DataInput_1[L1,R1,...,R4]. In the pre-programmed stereo PRB modes only miniDSP_D_DataInput_1[1:2] are processed and other input ports are ignored. Similarly for the pre-programmed mono PRB modes only miniDSP_D_DataInput[1] is processed. The input port miniDSP_D_DataInput_2 features 2 channels called miniDSP_D_DataInput_2[1:2] also referred to as

miniDSP_D_DataInput_2[L1,R1]. The input port miniDSP_D_DataInput_3 also features 2 channels of audio data called miniDSP_D_DataInput_3[1:2] also referred to as miniDSP_D_DataInput_3[L1,R1]. Signal routing to miniDSP_D_DataInput_1[1:8] is controlled by programming B0_P4_R118_D[5:4]. Signal routing to miniDSP_D_DataInput_2[1,2] is controlled by programming B0_P4_R118_D[3:2]. Signal routing to miniDSP_D_DataInput_3[1,2] is controlled by programming B0_P4_R118_D[1:0].

The audio serial port ASI1, can take in 8 channels of audio data. By default the miniDSP_A_DataOutput[1:8] is routed to ASI1_DataOutput. By programming B0_P4_R7_D[2:0], the default programming can be changed to one of ASI1_DataInput[1:8], ASI2_DataInput[1:2] or ASI3_DataInput[1:2] to acheive ASI to ASI loopback. Similarly the serial output of ASI1 is routed to ASI1_DOUT by default but by programming B0_P4_R15_D[1:0], this can be changed to route ASI1_DIN, ASI2_DIN or ASI3_DIN to achieve terminal-to-terminal loopback between ASIs. The ASI1's parallel output ASI1_DataInput can be routed to any of the miniDSP_D input ports.

The audio serial port ASI2 and ASI3, can take in 2 channels of audio data each. By default the inputs to ASI2_DataOutput[1:2] and ASI3_DataOutput[1:2] are disabled. By programming B0_P4_R23_D[2:0], one of miniDSP_A_DataOutput[1:2], miniDSP_A_DataOutput[3:4], ASI1_DataInput[1:2], ASI2_DataInput[1:2] or ASI3_DataInput[1:2] can be routed to ASI2_DataOutput[1:2]. Similarly by programming B0_P4_R39_D[2:0], one of miniDSP_A_DataOutput[1:2], miniDSP_A_DataOutput[5:6], ASI1_DataInput[1:2], ASI2_DataInput[1:2] or ASI3_DataInput[1:2] can be routed to ASI3_DataOutput[1:2]. The ASI2_DataInput and ASI3_DataInput can be routed to any of the miniDSP_D input ports.

The serial output ASI2_DOUT can be configured to route serial output of ASI2 or loop back ASI1_DIN, ASI2_DIN or ASI3_DIN. This feature is controlled by configuring B0_P4_R31_D[1:0]. The serial output of ASI3_DOUT can be configured to route serial output of ASI3 or loop back ASI1_DIN, ASI2_DIN or ASI3_DIN. This feature is controlled by configuring B0_P4_R47_D[1:0].

The signal routing between ASIs and miniDSPs is shown in Figure 108.

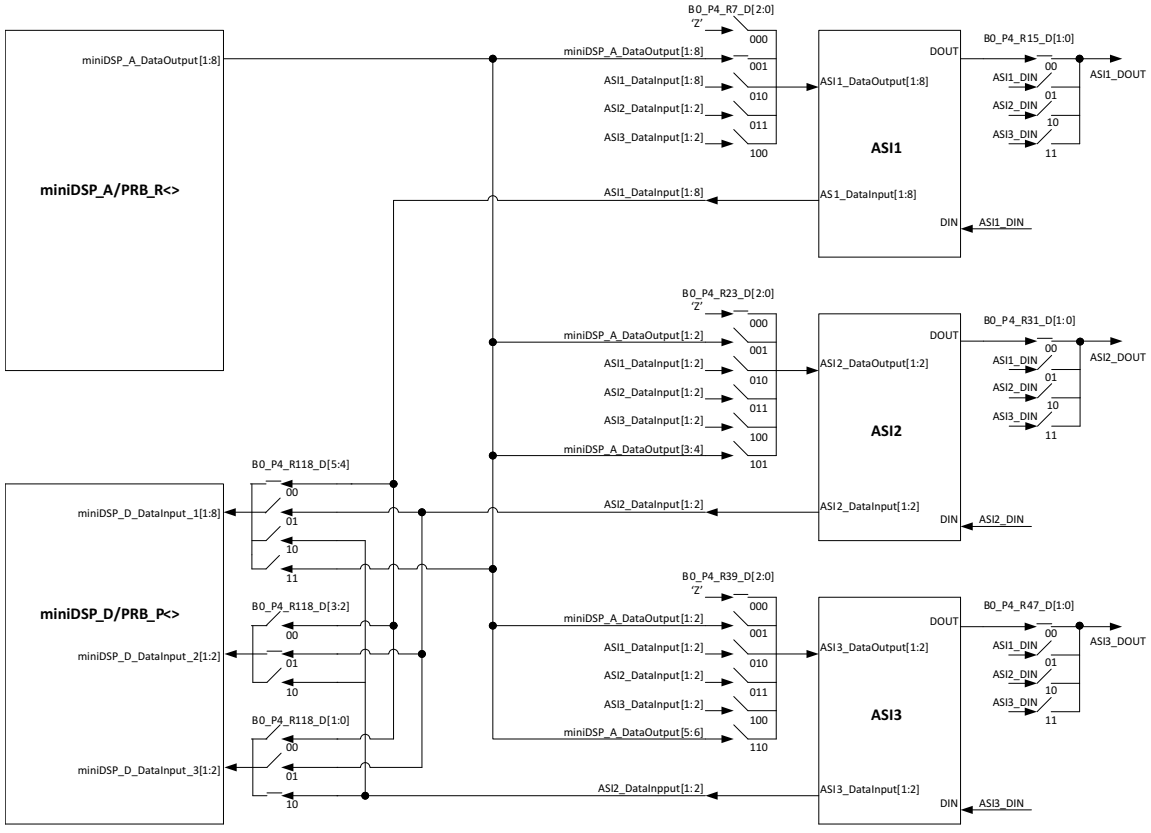


Figure 108. Audio Routing Between ASI ports,÷ miniDSP

8.3.11 Device Connections

8.3.11.1 Digital Terminals

Only a small number of digital terminals are dedicated to a single function; whenever possible, the digital terminals have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function terminals are hardware-control terminals $\overline{\text{RESET}}$ and SPI_SELECT terminal. Depending on the state of SPI_SELECT, four terminals SCL_SSZ, SDA_MOSI, MISO_GPO1, and I2C_ADDR_SCLK are configured for either I^2C or SPI protocol. Only in I^2C mode, I2C_ADDR_SCLK provide two possible I^2C addresses for the TLV320AIC3268, while this terminal receives the SPI SCLK when the device is set to SPI mode.

Other digital IO terminals can be configured for various functions via register control.

8.3.11.2 Analog Terminals

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input terminals to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in the Analog Routing Diagram.

8.3.11.3 Multifunction Terminals

Table 46 and Table 47 show the possible allocation of terminals for specific functions. The PLL input, for example, can be programmed to be any of 7 terminals (MCLK, BCLK1, DIN1, BCLK2,GPIO1, GPIO2, GPIO3).

Table 46. Multifunction Terminal Assignments for Terminals SDA_MOSI, SCL_SSZ, I2C_ADDR_SCLK,MISO_GPO1,MCLK, WCLK1, BCLK1, DIN1, and DOUT1

	Terminal Function	SDA_ MOSI (1)	SCL_ SSZ (2)	I2C_ ADDR_ SCLK (3)	MISO_ GPO1 (4)	MCLK (5)	WCLK1 (6)	BCLK1 (7)	DIN1 (8)	DOUT1 (9)
A	I2C Clock		E(1)							
B	I2C Data	E(1)								
C	I2C Address (LSB)			E(1)						
D	SPI Chip Select		E(1)							
E	SPI Clock			E(1)						
F	SPI Slave Data Input	E(1)								
G	SPI Slave Data Output				E(1), D(2)					
H	Word Clock Input,Output for ASI1						S(3),D(2)			
I	Word Clock Input, Output for ASI2									
J	Word Clock Input, Output for ASI3									
K	Bit Clock Input, Output for ASI1							S(3),D(2)		
L	Bit Clock Input, Output for ASI2									
M	Bit Clock Input, Output for ASI3									
N	DOUT for ASI1 All Channels									E(1),D(2)
O	DOUT for ASI1 (L1, R1)				E(1)					E(1),D(2)
P	DOUT for ASI1 (L2, R2)				E(1)					
Q	DOUT for ASI1 (L3, R3)				E(1)					
R	DOUT for ASI1 (L4, R4)				E(1)					
S	DOUT for ASI2									
T	DOUT for ASI3									
U	DIN for ASI1 All Channels								E(1),D(2)	
V	DIN for ASI1 (L1, R1)								E(1),D(2)	

Table 46. Multifunction Terminal Assignments for Terminals SDA_MOSI, SCL_SSZ, I2C_ADDR_SCLK,MISO_GPO1,MCLK, WCLK1, BCLK1, DIN1, and DOUT1 (continued)

	Terminal Function	SDA_ MOSI (1)	SCL_ SSZ (2)	I2C_ ADDR_ SCLK (3)	MISO_ GPO1 (4)	MCLK (5)	WCLK1 (6)	BCLK1 (7)	DIN1 (8)	DOUT1 (9)
W	DIN for ASI1 (L2, R2)									
X	DIN for ASI1 (L3, R3)									
Y	DIN for ASI1 (L4, R4)									
Z	DIN for ASI2									
AA	DIN for ASI3									
AB	ASI1 ADC BCLK Input, Output									
AC	ASI2 ADC BCLK Input, Output									
AD	ASI1 ADC WCLK Input, Output									
AE	ASI2 ADC WCLK Input, Output									
AF	ADC_MOD_CLK Output				E(1)					
AG	Digmic Data 1								E(1)	
AH	Digmic Data 2								E(1)	
AI	Input to PLL_CLKIN					S(3),D(2)		S(3)	S(3)	
AJ	Input to ADC_CLKIN					S(3),D(2)		S(3)		
AK	Input to DAC_CLKIN					S(3),D(2)		S(3)		
AL	Input to CDIV_CLKIN					S(3),D(2)		S(3)	S(3)	
AM	Input to LFR_CLKIN					S(3),D(2)	S(3)			
AN	Input to HF_CLKIN					S(3)				
AO	Input to REF_1MHz_CLK					S(3)				
AP	CLKOUT Output				E(1)		E(1)			E(1)
AQ	Bit Bang Input									
AR	Bit Bang Output									
AS	INT1 Output				E(1)					E(1)
AT	INT2 Output				E(1)					E(1)
AU	Interrupt for miniDSP									
AV	SAR ADC Interrupt				E(1)					E(1)
AW	General Purpose Output				E(1)					E(1)
AX	General Purpose Input								E(1)	

(1) E: The terminal is **exclusively** used for this function, no other function can be implemented with the same terminal (such as if DOUT1 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

(2) D: The terminal is the **default** selection for the function

(3) S: This terminal can be **simultaneously** used with other functions marked S for the same terminal. (such as MCLK terminal could be chosen to drive the PLL, ADC Clock, DAC Clock, CDIV Clock, LFR Clock, HF Clock, and REF_1MHz_CLK inputs simultaneously)

(4) MISO_GPO1 can only be utilized for functions defined in this table when part utilizes I^2C for control. In SPI mode, this terminal serves as MISO.

Table 47. Multifunction Terminal Assignments for Terminals WCLK2, BCLK2, DIN2, DOUT2, GPIO1, GPIO2, GPIO3, GPIO4 and GPIO5

	Terminal Function	WCLK2 (10)	BCLK2 (11)	DIN2 (12)	DOUT2 (13)	GPIO1 (14)	GPIO2 (15)	GPIO3 (16)	GPIO4 (17)	GPIO5 (18)
A	I2C Clock									
B	I2C Data									
C	I2C Address (LSB)									
D	SPI Chip Select									
E	SPI Clock									
F	SPI Slave Data Input									
G	SPI Slave Data Output									
H	Word Clock Input, Output for ASI1					S(3)				

Table 47. Multifunction Terminal Assignments for Terminals WCLK2, BCLK2, DIN2, DOUT2, GPIO1, GPIO2, GPIO3, GPIO4 and GPIO5 (continued)

	Terminal Function	WCLK2 (10)	BCLK2 (11)	DIN2 (12)	DOUT2 (13)	GPIO1 (14)	GPIO2 (15)	GPIO3 (16)	GPIO4 (17)	GPIO5 (18)
I	Word Clock Input, Output for ASI2	S(3),D(2)				S(3)				
J	Word Clock Input, Output for ASI3						S(3)			
K	Bit Clock Input, Output for ASI1						S(3)			
L	Bit Clock Input, Output for ASI2		S(3),D(2)				S(3)			
M	Bit Clock Input, Output for ASI3					S(3)				
N	DOUT for ASI1 All Channels									E(1)
O	DOUT for ASI1 (L1, R1)									
P	DOUT for ASI1 (L2, R2)				E(1)		E(1)			
Q	DOUT for ASI1 (L3, R3)		E(1)			E(1)	E(1)			
R	DOUT for ASI1 (L4, R4)	E(1)				E(1)	E(1)			
S	DOUT for ASI2				E(1),D(2)					E(1)
T	DOUT for ASI3								E(1)	
U	DIN for ASI1 All Channels									
V	DIN for ASI1 (L1, R1)									
W	DIN for ASI1 (L2, R2)			E(1)			E(1)	E(1)		
X	DIN for ASI1 (L3, R3)		E(1)			E(1)	E(1)	E(1)		E(1)
Y	DIN for ASI1 (L4, R4)	E(1)				E(1)	E(1)	E(1)		E(1)
Z	DIN for ASI2			E(1),D(2)						
AA	DIN for ASI3							E(1)		
AB	ADC BCLK1 Input, Output					E(1)	E(1)	E(1)	E(1)	
AC	ADC BCLK2 Input, Output					E(1)	E(1)	E(1)	E(1)	
AD	ADC WCLK1 Input, Output					E(1)	E(1)	E(1)	E(1)	
AE	ADC WCLK2 Input, Output					E(1)	E(1)	E(1)	E(1)	
AF	ADC_MOD_CLK Output	E(1)	E(1)		E(1)	E(1)	E(1)	E(1)	E(1)	E(1)
AG	Digmic Data 1			E(1)		E(1)	E(1)	E(1)	E(1)	E(1)
AH	Digmic Data 2			E(1)		E(1)	E(1)	E(1)	E(1)	E(1)
AI	Input to PLL_CLKIN		S(3)			S(3)	S(3)	S(3)		
AJ	Input to ADC_CLKIN		S(3)			S(3)	S(3)	S(3)		
AK	Input to DAC_CLKIN		S(3)			S(3)	S(3)	S(3)		
AL	Input to CDIV_CLKIN		S(3)					S(3)		
AM	Input to LFR_CLKIN	S(3)	S(3)	E(1)		S(3)	S(3)	S(3)		
AN	Input to HF_CLKIN									
AO	Input to REF_1MHz_CLK									
AP	CLKOUT Output	E(1)	E(1)			E(1)	E(1)			
AQ	Bit Bang Input					E(1)	E(1)	E(1)	E(1)	
AR	Bit Bang Output					E(1)	E(1)	E(1)	E(1)	
AS	INT1 Output	E(1)	E(1)		E(1)	E(1)	E(1)			
AT	INT2 Output	E(1)	E(1)		E(1)	E(1)	E(1)			
AU	Interrupt for miniDSP					E(1)	E(1)	E(1)		
AV	SAR ADC Interrupt	E(1)	E(1)		E(1)	E(1)	E(1)			
AW	General Purpose Output	E(1)	E(1)		E(1)	E(1)	E(1)			
AX	General Purpose Input	E(1)	E(1)	E(1)		E(1)	E(1)	E(1)	E(1)	

(1) E: The terminal is **exclusively** used for this function, no other function can be implemented with the same terminal (such as if DOUT1 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

(2) D: The terminal is the **default** selection for the function

(3) S: This terminal can be **simultaneously** used with other functions marked S for the same terminal. (such as MCLK terminal could be chosen to drive the PLL, ADC Clock, DAC Clock, CDIV Clock, LFR Clock, HF Clock, and REF_1MHz_CLK inputs simultaneously)

See Register Settings for Multifunction Terminals for details on register configuration of multi-function terminals.

8.3.11.3.1 Register Settings for Multifunction Terminals

Table 48 summarizes the register settings that must be applied to configure the terminal assignments for general inputs and outputs, interrupts, clocking outputs, and digital microphones. In Table 48, the letter/number combination represents the row and the column number from and in bold type.

Please be aware that more settings may be necessary to obtain a full functionality matching the application requirement.

Table 48. Multifunction Terminal Register Configuration - General Inputs/Outputs, Interrupts

	Description	Required Register Setting		Description	Required Register Setting
AQ14	Bit Bang input for miniDSP on GPIO1	B0_P4_R86_D[6:2]=00001; Value stored to B0_P4_R107_D[0]	AQ15	Bit Bang input for miniDSP on GPIO2	B0_P4_R87_D[6:2]=00001; Value stored to B0_P4_R107_D[1]
AQ16	Bit Bang input for miniDSP on GPIO3	B0_P4_R88_D[6:2]=00001; Value stored to B0_P4_R107_D[2]	AQ17	Bit Bang input for miniDSP on GPIO4	B0_P4_R89_D[6:2]=00001; Value stored to B0_P4_R107_D[3]
AR14	Host controlled Bit Bang output from miniDSP on GPIO1	B0_P4_R86_D[6:2]=01011; B0_P4_R113_D[6]=0; Value written in B0_P4_R104_D[0]	AR14	miniDSP_D controlled Bit Bang output from miniDSP on GPIO1	B0_P4_R86_D[6:2]=01011; B0_P4_R113_D[6]=1;
AR15	Host controlled Bit Bang output from miniDSP on GPIO2	B0_P4_R87_D[6:2]=01011; B0_P4_R113_D[6]=0; Value written in B0_P4_R104_D[1]	AR15	miniDSP_D controlled Bit Bang output from miniDSP on GPIO2	B0_P4_R87_D[6:2]=01011; B0_P4_R113_D[6]=1;
AR16	Host controlled Bit Bang output from miniDSP on GPIO3	B0_P4_R88_D[6:2]=01011; B0_P4_R113_D[6]=0; Value written in B0_P4_R104_D[2]	AR16	miniDSP_D controlled Bit Bang output from miniDSP on GPIO3	B0_P4_R88_D[6:2]=01011; B0_P4_R113_D[6]=1;
AR17	Host controlled Bit Bang output from miniDSP on GPIO4	B0_P4_R89_D[6:2]=01011; B0_P4_R113_D[6]=0; Value written in B0_P4_R104_D[3]	AR17	miniDSP_D controlled Bit Bang output from miniDSP on GPIO4	B0_P4_R89_D[6:2]=01011; B0_P4_R113_D[6]=1;
AS4	INT1 interrupt output on MISO_GPO1	B0_P4_R96_D[4:1]=0100; Configure B0_P0_R51_D[7:6]	AS9	INT1 interrupt output on DOUT1	B0_P4_R67_D[4:1]=0100; Configure B0_P0_R51_D[7:6]
AS9	INT1 interrupt output on WCLK2	B0_P4_R69_D[5:2]=0101; Configure B0_P0_R51_D[7:6]	AS11	INT1 interrupt output on BCLK2	B0_P4_R70_D[5:2]=0101; Configure B0_P0_R51_D[7:6]
AS13	INT1 interrupt output on DOUT2	B0_P4_R71_D[4:1]=0100; Configure B0_P0_R51_D[7:6]	AS14	INT1 interrupt output on GPIO1	B0_P4_R86_D[6:2]=00101; Configure B0_P0_R51_D[7:6]
AS15	INT1 interrupt output on GPIO2	B0_P4_R87_D[6:2]=00101; Configure B0_P0_R51_D[7:6]	AS16	INT1 interrupt output on GPIO3	B0_P4_R88_D[6:2]=00101; Configure B0_P0_R51_D[7:6]
AS17	INT1 interrupt output on GPIO4	B0_P4_R89_D[6:2]=00101; Configure B0_P0_R51_D[7:6]	AT4	INT2 interrupt output on MISO_GPO1	B0_P4_R96_D[4:1]=0101; Configure B0_P0_R51_D[5:4]
AT9	INT2 interrupt output on DOUT1	B0_P4_R67_D[4:1]=0101; Configure B0_P0_R51_D[5:4]	AT9	INT2 interrupt output on WCLK2	B0_P4_R69_D[5:2]=0110; Configure B0_P0_R51_D[5:4]
AT11	INT2 interrupt output on BCLK2	B0_P4_R70_D[5:2]=0110; Configure B0_P0_R51_D[5:4]	AT13	INT2 interrupt output on DOUT2	B0_P4_R71_D[4:1]=0101; Configure B0_P0_R51_D[5:4]
AT14	INT2 interrupt output on GPIO1	B0_P4_R86_D[6:2]=00110; Configure B0_P0_R51_D[5:4]	AT15	INT2 interrupt output on GPIO2	B0_P4_R87_D[6:2]=00110; Configure B0_P0_R51_D[5:4]
AT16	INT2 interrupt output on GPIO3	B0_P4_R88_D[6:2]=00110; Configure B0_P0_R51_D[5:4]	AT17	INT2 interrupt output on GPIO4	B0_P4_R89_D[6:2]=00110; Configure B0_P0_R51_D[5:4]
AU12	ISR interrupt for miniDSP_A on DIN2	B0_P4_R72_D[6:5]=01; B100_P0_R58_D[2:0]=100; Configure B100_P0_R58_D[4]	AU12	ISR interrupt for miniDSP_D on DIN2	B0_P4_R72_D[6:5]=01; B120_P0_R58_D[2:0]=100; Configure B120_P0_R58_D[4]
AU14	ISR interrupt for miniDSP_A on GPIO1	B0_P4_R86_D[6:2]=00001; B100_P0_R58_D[2:0]=001; Configure B100_P0_R58_D[4]	AU14	ISR interrupt for miniDSP_D on GPIO1	B0_P4_R86_D[6:2]=00001; B120_P0_R58_D[2:0]=001; Configure B120_P0_R58_D[4]
AU15	ISR interrupt for miniDSP_A on GPIO2	B0_P4_R87_D[6:2]=00001; B100_P0_R58_D[2:0]=010; Configure B100_P0_R58_D[4]	AU15	ISR interrupt for miniDSP_D on GPIO2	B0_P4_R72_D[6:2]=00001; B120_P0_R58_D[2:0]=010; Configure B120_P0_R58_D[4]
AV4	SAR ADC Interrupt on MISO_GPO1	B0_P4_R96_D[4:1]=0110; Configure B0_P3_R3_D[1:0]	AV9	SAR ADC Interrupt on DOUT1	B0_P4_R67_D[4:1]=0110; Configure B0_P3_R3_D[1:0]
AV10	SAR ADC Interrupt on WCLK2	B0_P4_R69_D[5:2]=1001; Configure B0_P3_R3_D[1:0]	AV11	SAR ADC Interrupt on BCLK2	B0_P4_R70_D[5:2]=1001; Configure B0_P3_R3_D[1:0]
AV13	SAR ADC Interrupt on DOUT2	B0_P4_R71_D[4:1]=0110; Configure B0_P3_R3_D[1:0]	AV14	SAR ADC Interrupt on GPIO1	B0_P4_R86_D[6:2]=01001; Configure B0_P3_R3_D[1:0]
AV15	SAR ADC Interrupt on GPIO2	B0_P4_R87_D[6:2]=01001; Configure B0_P3_R3_D[1:0]	AW4	General Purpose Output on MISO_GPO1	B0_P4_R96_D[4:1]=0010; Output value write to B0_P4_R96_D[0]

Table 48. Multifunction Terminal Register Configuration - General Inputs/Outputs, Interrupts (continued)

	Description	Required Register Setting		Description	Required Register Setting
AW9	General Purpose Output on DOUT1	B0_P4_R67_D[4:1]=0010; Output value write to B0_P4_R67_D[0]	AW10	General Purpose Output on WCLK2	B0_P4_R69_D[5:2]=0011; Output value write to B0_P4_R69_D[0]
AW11	General Purpose Output on BCLK2	B0_P4_R70_D[5:2]=0011; Output value write to B0_P4_R70_D[0]	AW13	General Purpose Output on DOUT2	B0_P4_R71_D[4:1]=0010; Output value write to B0_P4_R71_D[0]
AW14	General Purpose Output on GPIO1	B0_P4_R86_D[6:2]=00011; Output value write to B0_P4_R86_D[0]	AW15	General Purpose Output on GPIO2	B0_P4_R87_D[6:2]=00011; Output value write to B0_P4_R87_D[0]
AX9	General Purpose Input on DIN1	B0_P4_R68_D[6:5]=10; Input value available in B0_P4_R68_D[4]	AX10	General Purpose Input on WCLK2	B0_P4_R69_D[5:2]=0010; Input value available in B0_P4_R69_D[1]
AX11	General Purpose Input on BCLK2	B0_P4_R70_D[5:2]=0010; Input value available in B0_P4_R70_D[1]	AX13	General Purpose Input on DIN2	B0_P4_R72_D[6:5]=10; Input value available in B0_P4_R72_D[4]
AX14	General Purpose Input on GPIO1	B0_P4_R86_D[6:2]=00010; Input value available in B0_P4_R86_D[1]	AX15	General Purpose Input on GPIO2	B0_P4_R87_D[6:2]=00010; Input value available in B0_P4_R87_D[1]

Table 49 summarizes the register settings that must be applied to configure the terminal assignments for clocking inputs and outputs from the device. In Table 49, the letter/number combination represents the row and the column number from and in bold type.

Please be aware that more settings may be necessary to obtain a full functionality matching the application requirement.

Table 49. Multifunction Terminal Register Configuration - Clocking Inputs/Outputs

	Description	Required Register Setting		Description	Required Register Setting
AI5	PLL_CLKIN input on MCLK	B0_P0_R5_D[5:2]=0000;	AI7	PLL_CLKIN input on BCLK1	B0_P0_R5_D[5:2]=0001;
AI8	PLL_CLKIN input on DIN1	B0_P0_R5_D[5:2]=0011; B0_P4_R68_D[6:5]=01;	AI11	PLL_CLKIN input on BCLK2	B0_P0_R5_D[5:2]=0100; B0_P4_R70_D[5:2]=0010;
AI14	PLL_CLKIN input on GPIO1	B0_P0_R5_D[5:2]=0010; B0_P4_R86_D[6:2]=00001;	AI15	PLL_CLKIN input on GPIO2	B0_P0_R5_D[5:2]=0111; B0_P4_R87_D[6:2]=00001;
AI16	PLL_CLKIN input on GPIO3	B0_P0_R5_D[5:2]=0101; B0_P4_R88_D[6:2]=00001;	AJ5	ADC_CLKIN input on MCLK	B0_P0_R4_D[3:0]=0000;
AJ7	ADC_CLKIN input on BCLK1	B0_P0_R4_D[3:0]=0001;	AJ11	ADC_CLKIN input on BCLK2	B0_P0_R4_D[3:0]=0100; B0_P4_R70_D[5:2]=0010;
AJ14	ADC_CLKIN input on GPIO1	B0_P0_R4_D[3:0]=0010; B0_P4_R86_D[6:2]=00001;	AJ15	ADC_CLKIN input on GPIO2	B0_P0_R4_D[3:0]=1001; B0_P4_R87_D[6:2]=00001;
AJ16	ADC_CLKIN input on GPIO3	B0_P0_R4_D[3:0]=0101; B0_P4_R88_D[6:2]=00001;	AK5	DAC_CLKIN input on MCLK	B0_P0_R4_D[7:4]=0000;
AK7	DAC_CLKIN input on BCLK1	B0_P0_R4_D[7:4]=0001;	AK11	DAC_CLKIN input on BCLK2	B0_P0_R4_D[7:4]=0100; B0_P4_R70_D[5:2]=0010;
AK14	DAC_CLKIN input on GPIO1	B0_P0_R4_D[7:4]=0010; B0_P4_R86_D[6:2]=00001;	AK15	DAC_CLKIN input on GPIO2	B0_P0_R4_D[7:4]=1001; B0_P4_R87_D[6:2]=00001;
AK16	DAC_CLKIN input on GPIO3	B0_P0_R4_D[7:4]=0101; B0_P4_R88_D[6:2]=00001;	AL5	CDIV_CLKIN input on MCLK	B0_P0_R21_D[4:0]=0000;
AL7	CDIV_CLKIN input on BCLK1	B0_P0_R21_D[4:0]=0001;	AL8	CDIV_CLKIN input on DIN1	B0_P0_R21_D[4:0]=0010; B0_P4_R68_D[6:5]=01;
AL11	CDIV_CLKIN input on BCLK2	B0_P0_R21_D[4:0]=1000; B0_P4_R70_D[5:2]=0010;	AL16	CDIV_CLKIN input on GPIO3	B0_P0_R21_D[4:0]=1001; B0_P4_R88_D[6:2]=00001;
AM5	LFR_CLKIN input on MCLK	B0_P0_R24_D[7:4]=0000;	AM6	LFR_CLKIN input on WCLK1	B0_P0_R24_D[7:4]=0001;
AM10	LFR_CLKIN input on WCLK2	B0_P0_R24_D[7:4]=0011; B0_P4_R69_D[5:2]=0010;	AM11	LFR_CLKIN input on BCLK2	B0_P0_R24_D[7:4]=0100; B0_P4_R70_D[5:2]=0010;
AM12	LFR_CLKIN input on DIN2	B0_P0_R24_D[7:4]=0110; B0_P4_R72_D[6:5]=01;	AM14	LFR_CLKIN input on GPIO1	B0_P0_R24_D[7:4]=0010; B0_P4_R86_D[6:2]=00001;
AM15	LFR_CLKIN input on GPIO2	B0_P0_R24_D[7:4]=1000; B0_P4_R87_D[6:2]=00001;	AM16	LFR_CLKIN input on GPIO3	B0_P0_R24_D[7:4]=0101; B0_P4_R88_D[6:2]=00001;
AN5	HF_CLK input on MCLK	B0_P0_R24_D[3:0]=0000;	AO5	REF_1MHz_CLK input on MCLK	B0_P0_R23_D[7]=1;
AP4	CLKOUT output on MISO	B0_P4_R96_D[4:1]=0011; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]	AP6	CLKOUT output on WCLK1	B0_P4_R65_D[5:2]=0100; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]
AP9	CLKOUT output on DOUT1	B0_P4_R67_D[4:1]=0011; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]	AP10	CLKOUT output on WCLK2	B0_P4_R69_D[5:2]=0100; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]
AP11	CLKOUT output on BCLK2	B0_P4_R70_D[5:2]=0100; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]	AP14	CLKOUT output on GPIO1	B0_P4_R86_D[6:2]=00100; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]
AP15	CLKOUT output on GPIO2	B0_P4_R87_D[6:2]=00100; Configure B0_P0_R21_D[4:0] and B0_P0_R22_D[7:0]			

Table 50 summarizes the register settings that must be applied to configure the terminal assignments for digital microphone feature in the device. In Table 50, the letter/number combination represents the row and the column number from and in bold type.

Please be aware that more settings may be necessary to obtain a full functionality matching the application requirement.

Table 50. Multifunction Terminal Register Configuration - Digital Microphone

	Description	Required Register Setting		Description	Required Register Setting
AF4	ADC_MOD_CLK (DigMic clock) on MISO_GPO1	B0_P4_R96_D[4:1]=0111;	AF10	ADC_MOD_CLK (DigMic clock) on WCLK2	B0_P4_R69_D[5:2]=1010;
AF11	ADC_MOD_CLK (DigMic clock) on BCLK2	B0_P4_R70_D[5:2]=1010;	AF13	ADC_MOD_CLK (DigMic clock) on DOUT2	B0_P4_R71_D[4:1]=1010;
AF14	ADC_MOD_CLK (DigMic clock) on GPIO1	B0_P4_R86_D[6:2]=01010;	AF15	ADC_MOD_CLK (DigMic clock) on GPIO2	B0_P4_R87_D[6:2]=01010;
AF16	ADC_MOD_CLK (DigMic clock) on GPIO3	B0_P4_R88_D[6:2]=01010;	AF17	ADC_MOD_CLK (DigMic clock) on GPIO4	B0_P4_R89_D[6:2]=01010;
AF18	ADC_MOD_CLK (DigMic clock) on GPIO5	B0_P4_R90_D[6:2]=01010;			
AG8	Digital Mic 1 Left channel data on DIN1 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=1000; B0_P4_R68_D[6:5] = 01;	AG8	Digital Mic 1 Left channel data on DIN1 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=1000; B0_P4_R68_D[6:5] = 01;
AG8	Digital Mic 1 Right channel data on DIN1 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=1000; B0_P4_R68_D[6:5] = 01;	AG8	Digital Mic 1 Right channel data on DIN1 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=1000; B0_P4_R68_D[6:5] = 01;
AG12	Digital Mic 1 Left channel data on DIN2 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=1001; B0_P4_R72_D[6:5] = 01;	AG12	Digital Mic 1 Left channel data on DIN2 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=1001; B0_P4_R72_D[6:5] = 01;
AG12	Digital Mic 1 Right channel data on DIN2 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=1001; B0_P4_R72_D[6:5] = 01;	AG12	Digital Mic 1 Right channel data on DIN2 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=1001; B0_P4_R72_D[6:5] = 01;
AG14	Digital Mic 1 Left channel data on GPIO1 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=0000; B0_P4_R86_D[6:2] = 00001;	AG14	Digital Mic 1 Left channel data on GPIO1 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=0000; B0_P4_R86_D[6:2] = 00001;
AG14	Digital Mic 1 Right channel data on GPIO1 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=0000; B0_P4_R86_D[6:2] = 00001;	AG14	Digital Mic 1 Right channel data on GPIO1 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=0000; B0_P4_R86_D[6:2] = 00001;
AG15	Digital Mic 1 Left channel data on GPIO2 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=0001; B0_P4_R87_D[6:2] = 00001;	AG15	Digital Mic 1 Left channel data on GPIO2 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=0001; B0_P4_R87_D[6:2] = 00001;
AG15	Digital Mic 1 Right channel data on GPIO2 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=0001; B0_P4_R87_D[6:2] = 00001;	AG15	Digital Mic 1 Right channel data on GPIO2 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=0001; B0_P4_R87_D[6:2] = 00001;
AG16	Digital Mic 1 Left channel data on GPIO3 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=0010; B0_P4_R88_D[6:2] = 00001;	AG16	Digital Mic 1 Left channel data on GPIO3 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=0010; B0_P4_R88_D[6:2] = 00001;
AG16	Digital Mic 1 Right channel data on GPIO3 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=0010; B0_P4_R88_D[6:2] = 00001;	AG16	Digital Mic 1 Right channel data on GPIO3 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=0010; B0_P4_R88_D[6:2] = 00001;
AG17	Digital Mic 1 Left channel data on GPIO4 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=0011; B0_P4_R89_D[6:2] = 00001;	AG17	Digital Mic 1 Left channel data on GPIO4 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=0011; B0_P4_R89_D[6:2] = 00001;
AG17	Digital Mic 1 Right channel data on GPIO4 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=0011; B0_P4_R89_D[6:2] = 00001;	AG17	Digital Mic 1 Right channel data on GPIO4 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=0011; B0_P4_R89_D[6:2] = 00001;
AG18	Digital Mic 1 Left channel data on GPIO5 latched on rising edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[7:4]=0100; B0_P4_R90_D[6:2] = 00001;	AG18	Digital Mic 1 Left channel data on GPIO5 latched on falling edge of DigMic clock	B0_P0_R81_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[7:4]=0100; B0_P4_R90_D[6:2] = 00001;
AG18	Digital Mic 1 Right channel data on GPIO5 latched on rising edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R101_D[3:0]=0100; B0_P4_R90_D[6:2] = 00001;	AG18	Digital Mic 1 Right channel data on GPIO5 latched on falling edge of DigMic clock	B0_P0_R81_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R101_D[3:0]=0100; B0_P4_R90_D[6:2] = 00001;

Table 50. Multifunction Terminal Register Configuration - Digital Microphone (continued)

	Description	Required Register Setting		Description	Required Register Setting
AH8	Digital Mic 2 Left channel data on DIN1 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=1000; B0_P4_R68_D[6:5] = 01; Configure miniDSP_A	AH8	Digital Mic 2 Left channel data on DIN1 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=1000; B0_P4_R68_D[6:5] = 01; Configure miniDSP_A
AH8	Digital Mic 2 Right channel data on DIN1 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=1000; B0_P4_R68_D[6:5] = 01; Configure miniDSP_A	AH8	Digital Mic 2 Right channel data on DIN1 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=1000; B0_P4_R68_D[6:5] = 01; Configure miniDSP_A
AH12	Digital Mic 2 Left channel data on DIN2 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=1001; B0_P4_R72_D[6:5] = 01; Configure miniDSP_A	AH12	Digital Mic 2 Left channel data on DIN2 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=1001; B0_P4_R72_D[6:5] = 01; Configure miniDSP_A
AH12	Digital Mic 2 Right channel data on DIN2 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=1001; B0_P4_R72_D[6:5] = 01; Configure miniDSP_A	AH12	Digital Mic 2 Right channel data on DIN2 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=1001; B0_P4_R72_D[6:5] = 01; Configure miniDSP_A
AH14	Digital Mic 2 Left channel data on GPIO1 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=0000; B0_P4_R86_D[6:2] = 00001; Configure miniDSP_A	AH14	Digital Mic 2 Left channel data on GPIO1 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=0000; B0_P4_R86_D[6:2] = 00001; Configure miniDSP_A
AH14	Digital Mic 2 Right channel data on GPIO1 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=0000; B0_P4_R86_D[6:2] = 00001; Configure miniDSP_A	AH14	Digital Mic 2 Right channel data on GPIO1 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=0000; B0_P4_R86_D[6:2] = 00001; Configure miniDSP_A
AH15	Digital Mic 2 Left channel data on GPIO2 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=0001; B0_P4_R87_D[6:2] = 00001; Configure miniDSP_A	AH15	Digital Mic 2 Left channel data on GPIO2 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=0001; B0_P4_R87_D[6:2] = 00001; Configure miniDSP_A
AH15	Digital Mic 2 Right channel data on GPIO2 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=0001; B0_P4_R87_D[6:2] = 00001; Configure miniDSP_A	AH15	Digital Mic 2 Right channel data on GPIO2 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=0001; B0_P4_R87_D[6:2] = 00001; Configure miniDSP_A
AH16	Digital Mic 2 Left channel data on GPIO3 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=0010; B0_P4_R88_D[6:2] = 00001; Configure miniDSP_A	AH16	Digital Mic 2 Left channel data on GPIO3 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=0010; B0_P4_R88_D[6:2] = 00001; Configure miniDSP_A
AH16	Digital Mic 2 Right channel data on GPIO3 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=0010; B0_P4_R88_D[6:2] = 00001; Configure miniDSP_A	AH16	Digital Mic 2 Right channel data on GPIO3 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=0010; B0_P4_R88_D[6:2] = 00001; Configure miniDSP_A
AH17	Digital Mic 2 Left channel data on GPIO4 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=0011; B0_P4_R89_D[6:2] = 00001; Configure miniDSP_A	AH17	Digital Mic 2 Left channel data on GPIO4 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=0011; B0_P4_R89_D[6:2] = 00001; Configure miniDSP_A
AH17	Digital Mic 2 Right channel data on GPIO4 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=0011; B0_P4_R89_D[6:2] = 00001; Configure miniDSP_A	AH17	Digital Mic 2 Right channel data on GPIO4 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=0011; B0_P4_R89_D[6:2] = 00001; Configure miniDSP_A
AH18	Digital Mic 2 Left channel data on GPIO5 latched on rising edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[7:4]=0100; B0_P4_R90_D[6:2] = 00001; Configure miniDSP_A	AH18	Digital Mic 2 Left channel data on GPIO5 latched on falling edge of DigMic clock	B0_P0_R112_D[5:4] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[7:4]=0100; B0_P4_R90_D[6:2] = 00001; Configure miniDSP_A
AH18	Digital Mic 2 Right channel data on GPIO5 latched on rising edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 0; B0_P4_R102_D[3:0]=0100; B0_P4_R90_D[6:2] = 00001; Configure miniDSP_A	AH18	Digital Mic 2 Right channel data on GPIO5 latched on falling edge of DigMic clock	B0_P0_R112_D[3:2] = 01; B0_P4_R100_D[7] = 1; B0_P4_R102_D[3:0]=0100; B0_P4_R90_D[6:2] = 00001; Configure miniDSP_A

Table 51 summarizes the register settings that must be applied to configure the terminal assignments for the audio serial interfaces. In Table 51, the letter/number combination represents the row and the column number from Table 46 and Table 47 in bold type.

Please be aware that more settings may be necessary to obtain a full audio serial interface definition matching the application requirement (for example B0_P4_R1-R16 for Audio Serial Interface 1, B0_P4_R17-R32 for Audio Serial Interface 2, and B0_P4_R33-R48 for Audio Serial Interface 3).

Table 51. Multifunction Terminal Register Configuration - Audio Serial Interfaces

	Description	Required Register Setting		Description	Required Register Setting
H6	ASI1 WCLK Output on WCLK1	B0_P4_R65_D[5:2]=0001; B0_P4_R10_D[7:5]=001; Configure B0_P4_R14_D[3:0]	H6	ASI1 WCLK Input on WCLK1	B0_P4_R65_D[5:2]=0001; B0_P4_R10_D[7:5]=000;
I10	ASI2 WCLK Output for WCLK2	B0_P4_R69_D[5:2]=0001; B0_P4_R26_D5=1; B0_P4_R53_D[6:4]=000; Configure B0_P4_R30_D[3:0]	I10	ASI2 WCLK Input for WCLK2	B0_P4_R69_D[5:2]=0010; B0_P4_R26_D5=0; B0_P4_R53_D[6:4]=000;
J15	ASI3 WCLK Output on GPIO2	B0_P4_R87_D[6:2]=10100; B0_P4_R55_D[6:4]=010; Configure B0_P4_R46_D[3:0]	J15	ASI3 WCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R55_D[6:4]=010;
K7	ASI1 BCLK Output on BCLK1	B0_P4_R10_D[4:2]=001; Configure B0_P4_R14_D[7:4]	K7	ASI1 BCLK Input on BCLK1	B0_P4_R10_D[4:2]=000
L11	ASI2 BCLK Output on BCLK2	B0_P4_R53_D[2:0]=000; B0_P4_R26_D2 = 1; B0_P4_R70_D[5:2]=0001; Configure B0_P4_R30_D[7:4]	L11	ASI2 BCLK Input on BCLK2	B0_P4_R53_D[2:0]=000; B0_P4_R26_D2=0; B0_P4_R70_D[5:2]=0001;
M14	ASI3 BCLK Output on GPIO1	B0_P4_R55_D[2:0]=001; B0_P4_R86_D[6:2=10101; Configure B0_P4_R46_D[7:4]	M14	ASI3 BCLK Input on GPIO1	B0_P4_R55_D[2:0]=001; B0_P4_R86_D[6:2=00001;
N9	Single terminal multi-channel ASI1 DOUT on DOUT1	B0_P4_R4_D[7:6]=00 or 01 or 10 or 11; B0_P4_R6_D[7]=0; B0_P4_R67_D[4:1]=0001;	O9	ASI1 DOUT (L1,R1) on DOUT1	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R67_D[4:1]=0001;
P4	ASI1 DOUT (L2,R2) on MISO_GPO1	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R96_D[4:1]=1101;	P13	ASI1 DOUT (L2,R2) on DOUT2	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R71_D[4:1]=1101;
P15	ASI1 DOUT (L2,R2) on GPIO2	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R87_D[6:2]=01101;	Q4	ASI1 DOUT (L3,R3) on MISO_GPO1	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R96_D[4:1]=1110;
Q11	ASI1 DOUT (L3,R3) on BCLK2	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R70_D[5:2]=1110;	Q14	ASI1 DOUT (L3,R3) on GPIO1	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R86_D[6:2]=01110;
Q15	ASI1 DOUT (L3,R3) on GPIO2	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]=1; B0_P4_R87_D[6:2]=01110;	R10	ASI1 DOUT (L4,R4) on WCLK2	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]=1; B0_P4_R69_D[5:2]=1111;
R14	ASI1 DOUT (L4,R4) on GPIO1	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]=1; B0_P4_R86_D[6:2]=01111;	R15	ASI1 DOUT (L4,R4) on GPIO2	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]=1; B0_P4_R87_D[6:2]=01111;
S13	ASI2 DOUT on DOUT2	B0_P4_R71_D[4:1]=0001;			
T17	ASI3 DOUT on GPIO4	B0_P4_R89_D[6:2]=11101;	U8	Single terminal multi-channel ASI1 DIN on DIN1	B0_P4_R4_D[7:6] = 00 or 01 or 10 or 11; B0_P4_R6_D[7]= 0; B0_P4_R68_D[6:5]=01;
V8	ASI1 DIN (L1,R1) on DIN1	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R49_D[4:0]=00001; B0_P4_R68_D[6:5]=01;	W12	ASI1 DIN (L2,R2) on DIN2	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R50_D[4:0]=00010; B0_P4_R72_D[6:5]=01;
W15	ASI1 DIN (L2,R2) on GPIO2	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R50_D[4:0]=00101;	W16	ASI1 DIN (L2,R2) on GPIO3	B0_P4_R4_D[7:6] = 01 or 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R50_D[4:0]=00110;
X11	ASI1 DIN (L3,R3) on BCLK2	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=01100; B0_P4_R70_D[5:2]=1110;	X14	ASI1 DIN (L3,R3) on GPIO1	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00100; B0_P4_R86_D[6:2]=01110;
X15	ASI1 DIN (L3,R3) on GPIO2	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00101; B0_P4_R87_D[6:2]=01110;	X16	ASI1 DIN (L3,R3) on GPIO3	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00110; B0_P4_R88_D[6:2]=01110;
X18	ASI1 DIN (L3,R3) on GPIO5	B0_P4_R4_D[7:6] = 10 or 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=01000; B0_P4_R90_D[6:2]=01110;	Y10	ASI1 DIN (L4,R4) on WCLK2	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=01110; B0_P4_R69_D[5:2]=1111;
Y14	ASI1 DIN (L4,R4) on GPIO1	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00100; B0_P4_R86_D[6:2]=01111;	Y15	ASI1 DIN (L4,R4) on GPIO2	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00101; B0_P4_R87_D[6:2]=01111;
Y16	ASI1 DIN (L4,R4) on GPIO3	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=00110; B0_P4_R88_D[6:2]=01111;	Y18	ASI1 DIN (L4,R4) on GPIO5	B0_P4_R4_D[7:6] = 11; B0_P4_R6_D[7]= 1; B0_P4_R51_D[4:0]=01000; B0_P4_R90_D[6:2]=01111;
Z12	ASI2 DIN on DIN2	B0_P4_R54_D[2:0]=000; B0_P4_R72_D[6:5]=01;	AA16	ASI3 DIN on GPIO3	B0_P4_R56_D[2:0]=011; B0_P4_R88_D[6:2]=11101;
AB14	ASI1 ADC BCLK output on GPIO1	B0_P4_R11_D[7]=1; B0_P4_R16_D[2:0]=001; B0_P4_R86_D[6:2]=10111; Configure B0_P4_R1115_D[7:4]	AB14	ASI1 ADC BCLK input on GPIO1	B0_P4_R16_D[2:0]=001; B0_P4_R86_D[6:2]=00001;

Table 51. Multifunction Terminal Register Configuration - Audio Serial Interfaces (continued)

	Description	Required Register Setting		Description	Required Register Setting
AB15	ASI1 ADC BCLK output on GPIO2	B0_P4_R11_D[7]=1; B0_P4_R16_D[2:0]=010; B0_P4_R87_D[6:2]=10111; Configure B0_P4_R115_D[7:4]	AB15	ASI1 ADC BCLK input on GPIO2	B0_P4_R16_D[2:0]=010; B0_P4_R87_D[6:2]=00001;
AB16	ASI1 ADC BCLK output on GPIO3	B0_P4_R11_D[7]=1; B0_P4_R16_D[2:0]=011; B0_P4_R88_D[6:2]=10111; Configure B0_P4_R115_D[7:4]	AB16	ASI1 ADC BCLK input on GPIO3	B0_P4_R16_D[2:0]=011; B0_P4_R88_D[6:2]=00001;
AB17	ASI1 ADC BCLK output on GPIO4	B0_P4_R11_D[7]=1; B0_P4_R16_D[2:0]=100; B0_P4_R89_D[6:2]=10111; Configure B0_P4_R115_D[7:4]	AB17	ASI1 ADC BCLK input on GPIO4	B0_P4_R16_D[2:0]=100; B0_P4_R89_D[6:2]=00001;
AC14	ASI2 ADC BCLK output on GPIO1	B0_P4_R27_D[7]=1; B0_P4_R32_D[2:0]=001; B0_P4_R86_D[6:2]=11001; Configure B0_P4_R116_D[7:4]	AC14	ASI2 ADC BCLK input on GPIO1	B0_P4_R32_D[2:0]=001; B0_P4_R86_D[6:2]=00001;
AC15	ASI2 ADC BCLK output on GPIO2	B0_P4_R27_D[7]=1; B0_P4_R32_D[2:0]=010; B0_P4_R87_D[6:2]=11001; Configure B0_P4_R116_D[7:4]	AC15	ASI2 ADC BCLK input on GPIO2	B0_P4_R32_D[2:0]=010; B0_P4_R87_D[6:2]=00001;
AC16	ASI2 ADC BCLK output on GPIO3	B0_P4_R27_D[7]=1; B0_P4_R32_D[2:0]=011; B0_P4_R88_D[6:2]=11001; Configure B0_P4_R116_D[7:4]	AC16	ASI2 ADC BCLK input on GPIO3	B0_P4_R32_D[2:0]=011; B0_P4_R88_D[6:2]=00001;
AC17	ASI2 ADC BCLK output on GPIO4	B0_P4_R27_D[7]=1; B0_P4_R32_D[2:0]=100; B0_P4_R89_D[6:2]=11001; Configure B0_P4_R116_D[7:4]	AC17	ASI2 ADC BCLK input on GPIO4	B0_P4_R32_D[2:0]=100; B0_P4_R89_D[6:2]=00001;
AD14	ASI1 ADC WCLK output on GPIO1	B0_P4_R11_D[6]=1; B0_P4_R16_D[6:4]=001; B0_P4_R86_D[6:2]=10110; Configure B0_P4_R115_D[3:0]	AD14	ASI1 ADC WCLK input on GPIO1	B0_P4_R16_D[6:4]=001; B0_P4_R86_D[6:2]=00001;
AD15	ASI1 ADC WCLK output on GPIO2	B0_P4_R11_D[6]=1; B0_P4_R16_D[6:4]=010; B0_P4_R87_D[6:2]=10110; Configure B0_P4_R115_D[3:0]	AD15	ASI1 ADC WCLK input on GPIO2	B0_P4_R16_D[6:4]=010; B0_P4_R87_D[6:2]=00001;
AD16	ASI1 ADC WCLK output on GPIO3	B0_P4_R11_D[6]=1; B0_P4_R16_D[6:4]=011; B0_P4_R88_D[6:2]=10110; Configure B0_P4_R115_D[3:0]	AD16	ASI1 ADC WCLK input on GPIO3	B0_P4_R16_D[6:4]=011; B0_P4_R88_D[6:2]=00001;
AD17	ASI1 ADC WCLK output on GPIO4	B0_P4_R11_D[6]=1; B0_P4_R16_D[6:4]=100; B0_P4_R89_D[6:2]=10110; Configure B0_P4_R115_D[3:0]	AD17	ASI1 ADC WCLK input on GPIO4	B0_P4_R16_D[6:4]=100; B0_P4_R89_D[6:2]=00001;
AE14	ASI2 ADC WCLK output on GPIO1	B0_P4_R27_D[6]=1; B0_P4_R32_D[6:4]=001; B0_P4_R86_D[6:2]=11000; Configure B0_P4_R116_D[3:0]	AE14	ASI2 ADC WCLK input on GPIO1	B0_P4_R32_D[6:4]=001; B0_P4_R86_D[6:2]=00001;
AE15	ASI2 ADC WCLK output on GPIO2	B0_P4_R27_D[6]=1; B0_P4_R32_D[6:4]=010; B0_P4_R87_D[6:2]=11000; Configure B0_P4_R116_D[3:0]	AE15	ASI2 ADC WCLK input on GPIO2	B0_P4_R32_D[6:4]=010; B0_P4_R87_D[6:2]=00001;
AE16	ASI2 ADC WCLK output on GPIO3	B0_P4_R27_D[6]=1; B0_P4_R32_D[6:4]=011; B0_P4_R88_D[6:2]=11000; Configure B0_P4_R116_D[3:0]	AE16	ASI2 ADC WCLK input on GPIO3	B0_P4_R32_D[6:4]=011; B0_P4_R88_D[6:2]=00001;
AE17	ASI2 ADC WCLK output on GPIO4	B0_P4_R27_D[6]=1; B0_P4_R32_D[6:4]=100; B0_P4_R89_D[6:2]=11000; Configure B0_P4_R116_D[3:0]	AE17	ASI2 ADC WCLK input on GPIO4	B0_P4_R32_D[6:4]=100; B0_P4_R89_D[6:2]=00001;

8.4 Device Functional Modes

Functions	Modes	Details
Analog Inputs	• Single Ended Input Mode • Differential Input Mode • High Input Impedance Mode • Low Input Impedance Mode	See ADC Signal Routing for details.
Audio Inputs	• Analog Inputs • Digital Microphone/PDM Input	See Digital Microphone Function for details.

Device Functional Modes (continued)

Line Output	• Single-ended Output Mode • Differential Output Mode	See Line Out Amplifier Configurations for details.
Signal Processing	• Built-in Processing Block (PRB) Mode • Programmable miniDSP Mode	See ADC Processing Blocks, DAC Processing Blocks and for details.
Digital Audio Interface	• WCLK and BCLK Master Mode • WCLK and BCLK Slave Mode • I2S Mode • LJF Mode • RJF Mode • DSP Mode • PCM Mode • TDM Mode	See Digital Audio Interfaces for details.
Control Interface	• SPI Mode • I2C Mode	See Control Interfaces for details.
SAR ADC	• Internal Reference Mode • External Reference Mode • Auxiliary Voltage Measurement Mode • Resistive Measurement Mode	See SAR ADC for details.
Interrupts	• Pulsed Mode • Level Mode	See Interrupt Generation and Diagnostic Flags for details.
Multifunction Terminals	• Terminal Muxing	See Multifunction Terminals for details.

8.5 Programming

To enable the TLV320AIC3268 in a particular application, it needs to be comfigured or programmed. Initialization Setup describes various configurations required to enable the device.

To enable use of miniDSP in configurable modes, PurePath tools are provided. Please contact Texas Instruments for more details.

8.6 Register Maps

8.6.1 Register Map Summary

Table 52. Summary of Register Map

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	0	0x00	0x00	0x00	Page Select Register
0	0	1	0x00	0x00	0x01	Software Reset Register
0	0	2-3	0x00	0x00	0x02-0x03	Reserved Registers
0	0	4	0x00	0x00	0x04	Clock Control Register 1, Clock Input Multiplexers
0	0	5	0x00	0x00	0x05	Clock Control Register 2, PLL Input Multiplexer
0	0	6	0x00	0x00	0x06	Clock Control Register 3, PLL P and R Values
0	0	7	0x00	0x00	0x07	Clock Control Register 4, PLL J Value
0	0	8	0x00	0x00	0x08	Clock Control Register 5, PLL D Values (MSB)
0	0	9	0x00	0x00	0x09	Clock Control Register 6, PLL D Values (LSB)
0	0	10	0x00	0x00	0x0A	Clock Control Register 7, PLL_CLKIN Divider
0	0	11	0x00	0x00	0x0B	Clock Control Register 8, NDAC Divider Values
0	0	12	0x00	0x00	0x0C	Clock Control Register 9, MDAC Divider Values
0	0	13	0x00	0x00	0x0D	DAC OSR Control Register 1, MSB Value
0	0	14	0x00	0x00	0x0E	DAC OSR Control Register 2, LSB Value

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	15-17	0x00	0x00	0x0F-0x11	Reserved Registers
0	0	18	0x00	0x00	0x12	Clock Control Register 10, NADC Values
0	0	19	0x00	0x00	0x13	Clock Control Register 11, MADC Values
0	0	20	0x00	0x00	0x14	ADC Oversampling (AOSR) Register
0	0	21	0x00	0x00	0x15	CLKOUT MUX
0	0	22	0x00	0x00	0x16	Clock Control Register 12, CLKOUT M Divider Value
0	0	23	0x00	0x00	0x17	Timer clock
0	0	24	0x00	0x00	0x18	Low Frequency Clock Generation Control
0	0	25	0x00	0x00	0x19	High Frequency Clock Generation Control 1
0	0	26	0x00	0x00	0x1A	High Frequency Clock Generation Control 2
0	0	27	0x00	0x00	0x1B	High Frequency Clock Generation Control 3
0	0	28	0x00	0x00	0x1C	High Frequency Clock Generation Control 4
0	0	29	0x00	0x00	0x1D	High Frequency Clock Trim Control 1
0	0	30	0x00	0x00	0x1E	High Frequency Clock Trim Control 2
0	0	31	0x00	0x00	0x1F	High Frequency Clock Trim Control 3
0	0	32	0x00	0x00	0x20	High Frequency Clock Trim Control 4
0	0	33-35	0x00	0x00	0x21-0x23	Reserved Registers
0	0	36	0x00	0x00	0x24	ADC Flag Register
0	0	37	0x00	0x00	0x25	DAC Flag Register
0	0	38	0x00	0x00	0x26	DAC Flag Register
0	0	39-41	0x00	0x00	0x27-0x29	Reserved Registers
0	0	42	0x00	0x00	0x2A	Sticky Flag Register 1
0	0	43	0x00	0x00	0x2B	Reserved Register
0	0	44	0x00	0x00	0x2C	Sticky Flag Register 2
0	0	45	0x00	0x00	0x2D	Sticky Flag Register 3
0	0	46-47	0x00	0x00	0x2E-0x2F	Reserved Register
0	0	48	0x00	0x00	0x30	INT1 Interrupt Control
0	0	49	0x00	0x00	0x31	INT2 Interrupt Control
0	0	50	0x00	0x00	0x32	SAR Control 1
0	0	51	0x00	0x00	0x33	Interrupt Format Control Register
0	0	52-59	0x00	0x00	0x34-0x3B	Reserved Registers
0	0	60	0x00	0x00	0x3C	DAC Processing Block and miniDSP Power Control
0	0	61	0x00	0x00	0x3D	ADC Processing Block Control
0	0	62	0x00	0x00	0x3E	Reserved Register
0	0	63	0x00	0x00	0x3F	Primary DAC Power and Soft-Stepping Control
0	0	64	0x00	0x00	0x40	Primary DAC Master Volume Configuration
0	0	65	0x00	0x00	0x41	Primary DAC Left Volume Control Setting
0	0	66	0x00	0x00	0x42	Primary DAC Right Volume Control Setting
0	0	67	0x00	0x00	0x43	Headset Detection
0	0	68	0x00	0x00	0x44	Reserved Register
0	0	69	0x00	0x00	0x45	Reserved Register

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	70	0x00	0x00	0x46	Reserved Register
0	0	71-80	0x00	0x00	0x47-0x50	Reserved Registers
0	0	81	0x00	0x00	0x51	ADC Channel Power Control
0	0	82	0x00	0x00	0x52	ADC Fine Gain Volume Control
0	0	83	0x00	0x00	0x53	Left ADC Volume Control
0	0	84	0x00	0x00	0x54	Right ADC Volume Control
0	0	85	0x00	0x00	0x55	ADC Phase Control
0	0	86	0x00	0x00	0x56	Left AGC Control 1
0	0	87	0x00	0x00	0x57	Left AGC Control 2
0	0	88	0x00	0x00	0x58	Left AGC Control 3
0	0	89	0x00	0x00	0x59	Left AGC Attack Time
0	0	90	0x00	0x00	0x5A	Left AGC Decay Time
0	0	91	0x00	0x00	0x5B	Left AGC Noise Debounce
0	0	92	0x00	0x00	0x5C	Left AGC Signal Debounce
0	0	93	0x00	0x00	0x5D	Left AGC Gain
0	0	94	0x00	0x00	0x5E	Right AGC Control 1
0	0	95	0x00	0x00	0x5F	Right AGC Control 2
0	0	96	0x00	0x00	0x60	Right AGC Control 3
0	0	97	0x00	0x00	0x61	Right AGC Attack Time
0	0	98	0x00	0x00	0x62	Right AGC Decay Time
0	0	99	0x00	0x00	0x63	Right AGC Noise Debounce
0	0	100	0x00	0x00	0x64	Right AGC Signal Debounce
0	0	101	0x00	0x00	0x65	Right AGC Gain
0	0	102-111	0x00	0x00	0x66-0x6F	Reserved Registers
0	0	112	0x00	0x00	0x70	Digital Microphone 2 Control
0	0	113-114	0x00	0x00	0x71-0x72	Reserved Registers
0	0	115	0x00	0x00	0x73	I2C Interface Miscellaneous Control
0	0	116-119	0x00	0x00	0x74-0x77	Reserved Registers
0	0	120	0x00	0x00	0x78	miniDSP Control Register access
0	0	121-126	0x00	0x00	0x79-0x7E	Reserved Registers
0	0	127	0x00	0x00	0x7F	Book Selection Register
0	1	0	0x00	0x01	0x00	Page Select Register
0	1	1	0x00	0x01	0x01	Power Configuration Register
0	1	2	0x00	0x01	0x02	Reserved Register
0	1	3	0x00	0x01	0x03	Left DAC PowerTune Configuration Register
0	1	4	0x00	0x01	0x04	Right DAC PowerTune Configuration Register
0	1	5-7	0x00	0x01	0x05-0x07	Reserved Registers
0	1	8	0x00	0x01	0x08	Common Mode Register
0	1	9	0x00	0x01	0x09	Headphone Output Driver Control
0	1	10	0x00	0x01	0x0A	Receiver Output Driver Control

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	1	11	0x00	0x01	0x0B	Headphone Output Driver De-pop Control
0	1	12	0x00	0x01	0x0C	Receiver Output Driver De-Pop Control
0	1	13-16	0x00	0x01	0x0D-0x10	Reserved Registers
0	1	17	0x00	0x01	0x11	Mixer Amplifier Control
0	1	18	0x00	0x01	0x12	Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control
0	1	19	0x00	0x01	0x13	Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control
0	1	20-21	0x00	0x01	0x14-0x15	Reserved Registers
0	1	22	0x00	0x01	0x16	Lineout Amplifier Control 1
0	1	23	0x00	0x01	0x17	Lineout Amplifier Control 2
0	1	24-26	0x00	0x01	0x18-0x1A	Reserved
0	1	27	0x00	0x01	0x1B	Headphone Amplifier Control 1
0	1	28	0x00	0x01	0x1C	Headphone Amplifier Control 2
0	1	29	0x00	0x01	0x1D	Headphone Amplifier Control 3
0	1	30	0x00	0x01	0x1E	Reserved Register
0	1	31	0x00	0x01	0x1F	HPL Driver Volume Control
0	1	32	0x00	0x01	0x20	HPR Driver Volume Control
0	1	33	0x00	0x01	0x21	Reserved Register
0	1	34	0x00	0x01	0x22	Reserved Register
0	1	35	0x00	0x01	0x23	Ground Centered Headphone Offset Correction Control
0	1	36	0x00	0x01	0x24	Receiver Amplifier Control 1
0	1	37	0x00	0x01	0x25	Receiver Amplifier Control 2
0	1	38	0x00	0x01	0x26	Receiver Amplifier Control 3
0	1	39	0x00	0x01	0x27	Receiver Amplifier Control 4
0	1	40	0x00	0x01	0x28	Receiver Amplifier Control 5
0	1	41	0x00	0x01	0x29	Receiver Amplifier Control 6
0	1	42	0x00	0x01	0x2A	Receiver Amplifier Control 7
0	1	43-44	0x00	0x01	0x2B-0x2C	Reserved Registers
0	1	45	0x00	0x01	0x2D	Speaker Amplifier Control 1
0	1	46	0x00	0x01	0x2E	Speaker Amplifier Control 2
0	1	47	0x00	0x01	0x2F	Speaker Amplifier Control 3
0	1	48	0x00	0x01	0x30	Speaker Amplifier Volume Controls
0	1	49-50	0x00	0x01	0x31-0x32	Reserved Registers
0	1	51	0x00	0x01	0x33	Microphone Bias Control
0	1	52	0x00	0x01	0x34	Input Select 1 for Left Microphone PGA P-Terminal
0	1	53	0x00	0x01	0x35	Input Select 2 for Left Microphone PGA P-Terminal
0	1	54	0x00	0x01	0x36	Input Select for Left Microphone PGA M-Terminal
0	1	55	0x00	0x01	0x37	Input Select 1 for Right Microphone PGA P-Terminal
0	1	56	0x00	0x01	0x38	Input Select 2 for Right Microphone PGA P-Terminal
0	1	57	0x00	0x01	0x39	Input Select for Right Microphone PGA M-Terminal
0	1	58	0x00	0x01	0x3A	Input Common Mode Control
0	1	59	0x00	0x01	0x3B	Left Microphone PGA Control

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	1	60	0x00	0x01	0x3C	Right Microphone PGA Control
0	1	61	0x00	0x01	0x3D	ADC PowerTune Configuration Register
0	1	62	0x00	0x01	0x3E	ADC Analog PGA Gain Flag Register
0	1	63	0x00	0x01	0x3F	DAC Analog Gain Flags Register 1
0	1	64	0x00	0x01	0x40	DAC Analog Gain Flags Register 2
0	1	65	0x00	0x01	0x41	Analog Bypass Gain Flags Register
0	1	66	0x00	0x01	0x42	Driver Power-Up Flags Register
0	1	67-68	0x00	0x01	0x43-0x44	Reserved Registers
0	1	69	0x00	0x01	0x45	Over current Flags
0	1	67-76	0x00	0x01	0x43-0x4C	Reserved Registers
0	1	77	0x00	0x01	0x4D	Reserved Registers
0	1	78-118	0x00	0x01	0x4E-0x76	Reserved Registers
0	1	119	0x00	0x01	0x77	Headset Detection Tuning Register 1
0	1	120	0x00	0x01	0x78	Headset Detection Tuning Register 2
0	1	121	0x00	0x01	0x79	Reserved Register
0	1	122	0x00	0x01	0x7A	Reference Powerup Control
0	1	123-127	0x00	0x01	0x7B-0x7F	Reserved Registers
0	3	0	0x00	0x03	0x00	Page Select Register
0	3	1	0x00	0x03	0x01	Reserved Register
0	3	2	0x00	0x03	0x02	Primary SAR ADC Control
0	3	3	0x00	0x03	0x03	Primary SAR ADC Conversion Mode
0	3	4-5	0x00	0x03	0x04-0x05	Reserved Registers
0	3	6	0x00	0x03	0x06	SAR Reference Control
0	3	7-8	0x00	0x03	0x07-0x08	Reserved Registers
0	3	9	0x00	0x03	0x09	SAR ADC Flags Register 1
0	3	10	0x00	0x03	0x0A	SAR ADC Flags Register 2
0	3	11-12	0x00	0x03	0x0B-0x0C	Reserved Registers
0	3	13	0x00	0x03	0x0D	SAR ADC Buffer Mode Control
0	3	14	0x00	0x03	0x0E	Reserved Register
0	3	15	0x00	0x03	0x0F	Scan Mode Timer Control
0	3	16	0x00	0x03	0x10	Reserved Register
0	3	17	0x00	0x03	0x11	SAR ADC Clock Control
0	3	18	0x00	0x03	0x12	SAR ADC Buffer Mode Data Read Control
0	3	19	0x00	0x03	0x13	SAR ADC Measurement Control
0	3	20	0x00	0x03	0x14	Reserved Register
0	3	21	0x00	0x03	0x15	SAR ADC Measurement Threshold Flags
0	3	22	0x00	0x03	0x16	IN1L Max Threshold Check Control 1
0	3	23	0x00	0x03	0x17	IN1L Max Threshold Check Control 2
0	3	24	0x00	0x03	0x18	IN1L Min Threshold Check Control 1
0	3	25	0x00	0x03	0x19	IN1L Min Threshold Check Control 2

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	3	26	0x00	0x03	0x1A	IN1R Max Threshold Check Control 1
0	3	27	0x00	0x03	0x1B	IN1R Max Threshold Check Control 2
0	3	28	0x00	0x03	0x1C	IN1R Min Threshold Check Control 1
0	3	29	0x00	0x03	0x1D	IN1R Min Threshold Check Control 2
0	3	30	0x00	0x03	0x1E	TEMP Max Threshold Check Control 1
0	3	31	0x00	0x03	0x1F	TEMP Max Threshold Check Control 2
0	3	32	0x00	0x03	0x20	TEMP Min Threshold Check Control 1
0	3	33	0x00	0x03	0x21	TEMP Min Threshold Check Control 2
0	3	34-53	0x00	0x03	0x22-0x35	Reserved Registers
0	3	54	0x00	0x03	0x36	IN1L Measurement Data (MSB)
0	3	55	0x00	0x03	0x37	IN1L Measurement Data (LSB)
0	3	56	0x00	0x03	0x38	IN1R Measurement Data (MSB)
0	3	57	0x00	0x03	0x39	IN1R Measurement Data (LSB)
0	3	58	0x00	0x03	0x3A	VBAT Measurement Data (MSB)
0	3	59	0x00	0x03	0x3B	VBAT Measurement Data (LSB)
0	3	60-65	0x00	0x03	0x3C-0x41	Reserved Registers
0	3	66	0x00	0x03	0x42	TEMP1 Measurement Data (MSB)
0	3	67	0x00	0x03	0x43	TEMP1 Measurement Data (LSB)
0	3	68	0x00	0x03	0x44	TEMP2 Measurement Data (MSB)
0	3	69	0x00	0x03	0x45	TEMP2 Measurement Data (LSB)
0	3	70-127	0x00	0x03	0x46-0x7F	Reserved Registers
0	4	0	0x00	0x04	0x00	Page Select Register
0	4	1	0x00	0x04	0x01	ASI1, Audio Bus Format Control Register
0	4	2	0x00	0x04	0x02	ASI1, Left Ch_Offset_1 Control Register
0	4	3	0x00	0x04	0x03	ASI1, Right Ch_Offset_2 Control Register
0	4	4	0x00	0x04	0x04	ASI1, Channel Setup Register
0	4	5	0x00	0x04	0x05	ASI1, ADC Audio Bus Format Control Register
0	4	6	0x00	0x04	0x06	Audio Serial Interface 1, Multi-Pin Mode
0	4	7	0x00	0x04	0x07	ASI1, ADC Input Control
0	4	8	0x00	0x04	0x08	ASI1, DAC Output Control
0	4	9	0x00	0x04	0x09	ASI1, Control Register 9, ADC Slot Tristate Control
0	4	10	0x00	0x04	0x0A	ASI1, WCLK and BCLK Control Register
0	4	11	0x00	0x04	0x0B	ASI1, Bit Clock N Divider Input Control
0	4	12	0x00	0x04	0x0C	ASI1, Bit Clock N Divider
0	4	13	0x00	0x04	0x0D	ASI 1, Word Clock N Divider
0	4	14	0x00	0x04	0x0E	ASI1, BCLK and WCLK Output
0	4	15	0x00	0x04	0x0F	ASI1, Data Output
0	4	16	0x00	0x04	0x10	ASI1, ADC Word Clock and Bit Clock Control
0	4	17	0x00	0x04	0x11	ASI2, Audio Bus Format Control Register
0	4	18	0x00	0x04	0x12	ASI2, Data Offset Control Register
0	4	19-20	0x00	0x04	0x13-0x14	Reserved Registers
0	4	21	0x00	0x04	0x15	ASI2, ADC Audio Bus Format Control Register

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	4	22	0x00	0x04	0x16	Reserved Register
0	4	23	0x00	0x04	0x17	ASI2, ADC Input Control
0	4	24	0x00	0x04	0x18	ASI 2, DAC Output Control
0	4	25	0x00	0x04	0x19	Reserved Register
0	4	26	0x00	0x04	0x1A	ASI2, Word Clock and Bit Clock Control Register
0	4	27	0x00	0x04	0x1B	ASI2, Bit Clock N Divider Input Control
0	4	28	0x00	0x04	0x1C	ASI2, Bit Clock N Divider
0	4	29	0x00	0x04	0x1D	ASI2, Word Clock N Divider
0	4	30	0x00	0x04	0x1E	ASI2, Bit Clock and Word Clock Output
0	4	31	0x00	0x04	0x1F	ASI2, Data Output
0	4	32	0x00	0x04	0x20	ASI2, ADC Word Clock and Bit Clock Control
0	4	33	0x00	0x04	0x21	ASI3, Audio Bus Format Control Register
0	4	34	0x00	0x04	0x22	ASI3, Data Offset Control Register
0	4	35-36	0x00	0x04	0x23-0x24	Reserved Registers
0	4	37	0x00	0x04	0x25	Reserved Register
0	4	38	0x00	0x04	0x26	Reserved Register
0	4	39	0x00	0x04	0x27	ASI3, ADC Input Control
0	4	40	0x00	0x04	0x28	ASI3, DAC Output Control
0	4	41	0x00	0x04	0x29	Reserved Register
0	4	42	0x00	0x04	0x2A	ASI3, Word Clock and Bit Clock Control Register
0	4	43	0x00	0x04	0x2B	ASI3, Bit Clock N Divider Input Control
0	4	44	0x00	0x04	0x2C	ASI3, Bit Clock N Divider
0	4	45	0x00	0x04	0x2D	ASI3, Word Clock N Divider
0	4	46	0x00	0x04	0x2E	ASI3, Bit Clock and Word Clock Output
0	4	47	0x00	0x04	0x2F	ASI3, Data Output
0	4	48	0x00	0x04	0x30	Reserved Register.
0	4	49	0x00	0x04	0x31	ASI1 L1, R1 Input Control
0	4	50	0x00	0x04	0x32	ASI1 L2, R2 Input Control
0	4	51	0x00	0x04	0x33	ASI1 L3, R3 Input Control
0	4	52	0x00	0x04	0x34	ASI1 L4, R4 Input Control
0	4	53	0x00	0x04	0x35	Reserved Register
0	4	54	0x00	0x04	0x36	ASI2, DIN Input Multiplexer Control
0	4	55	0x00	0x04	0x37	ASI3, Word Clock and Bit Clock Input Multiplexer Control
0	4	56	0x00	0x04	0x38	ASI3, DIN Input Multiplexer Control
0	4	57-64	0x00	0x04	0x39-0x40	Reserved Registers
0	4	65	0x00	0x04	0x41	WCLK1 (Input or Output) Pin Control
0	4	66	0x00	0x04	0x42	Reserved Register
0	4	67	0x00	0x04	0x43	DOUT1 (Output) Pin Control
0	4	68	0x00	0x04	0x44	DIN1 (Input) Pin Control
0	4	69	0x00	0x04	0x45	WCLK2 (Input or Output) Pin Control
0	4	70	0x00	0x04	0x46	BCLK2 (Input or Output) Pin Control
0	4	71	0x00	0x04	0x47	DOUT2 (Output) Pin Control
0	4	72	0x00	0x04	0x48	DIN2 (Input) Pin Control

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	4	73-74	0x00	0x04	0x49-0x4A	Reserved Register
0	4	75	0x00	0x04	0x4B	Reserved Register
0	4	76	0x00	0x04	0x4C	Reserved Register
0	4	77-85	0x00	0x04	0x4D-0x55	Reserved Registers
0	4	86	0x00	0x04	0x56	GPIO1 (Input or Output) Pin Control
0	4	87	0x00	0x04	0x57	GPIO2 (Input or Output) Pin Control
0	4	88	0x00	0x04	0x58	GPIO3 (Input or Output) Pin Control
0	4	89	0x00	0x04	0x59	GPIO4 (Input or Output) Pin Control
0	4	90	0x00	0x04	0x5A	GPIO5 (Input or Output) Pin Control
0	4	91	0x00	0x04	0x5B	Reserved Register
0	4	92-95	0x00	0x04	0x5C-0x5F	Reserved Registers
0	4	96	0x00	0x04	0x60	MISO_GPO1 (Output) Pin Control
0	4	97-99	0x00	0x04	0x61-0x63	Reserved Registers
0	4	100	0x00	0x04	0x64	Digital Microphone Clock Control
0	4	101	0x00	0x04	0x65	Digital Microphone 1 Input Pin Control
0	4	102	0x00	0x04	0x66	Digital Microphone 2 Input Pin Control
0	4	103	0x00	0x04	0x67	Reserved Register
0	4	104	0x00	0x04	0x68	Bit-Bang Output
0	4	105-106	0x00	0x04	0x69-0x6A	Reserved Registers
0	4	107	0x00	0x04	0x6B	Bit-Bang Input
0	4	108-112	0x00	0x04	0x6C-0x70	Reserved Registers
0	4	113	0x00	0x04	0x71	Bit-Bang miniDSP Output Control
0	4	114	0x00	0x04	0x72	Reserved Register
0	4	115	0x00	0x04	0x73	ASI1, ADC Bit Clock and ADC Word Clock Output
0	4	116	0x00	0x04	0x74	ASI2, ADC Bit Clock and ADC Word Clock Output
0	4	117	0x00	0x04	0x75	ASI3, ADC Bit Clock and ADC Word Clock Output
0	4	118	0x00	0x04	0x76	miniDSP Data Port Control
0	4	119	0x00	0x04	0x77	Digital Audio Engine Synchronization Control
0	4	120-127	0x00	0x04	0x78-0x7F	Reserved Registers
0	252	0	0x00	0xFC	0x00	Page Select Register
0	252	1	0x00	0xFC	0x01	SAR Buffer Mode Data (MSB) and Buffer Flags
0	252	2	0x00	0xFC	0x02	SAR Buffer Mode Data (LSB)
0	252	3-127	0x00	0xFC	0x03-0x7F	Reserved Registers
20	0	0	0x14	0x00	0x00	Page Select Register
20	0	1-126	0x14	0x00	0x01-0x7E	Reserved Registers
20	0	127	0x14	0x00	0x7F	Book Selection Register
20	1-26	0	0x14	0x01-0x1A	0x00	Page Select Register

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
20	1-26	1-7	0x14	0x01-0x1A	0x01-0x07	Reserved Registers
20	1-26	8-127	0x14	0x01-0x1A	0x08-0x7F	ADC Fixed Coefficients C(0:767)
40	0	0	0x28	0x00	0x00	Page Select Register
40	0	1	0x28	0x00	0x01	ADC Adaptive CRAM Configuration Register
40	0	2-126	0x28	0x00	0x02-0x7E	Reserved Registers
40	0	127	0x28	0x00	0x7F	Book Selection Register
40	1-17	0	0x28	0x01-0x11	0x00	Page Select Register
40	1-17	1-7	0x28	0x01-0x11	0x01-0x07	Reserved Registers
40	1-17	8-127	0x28	0x01-0x11	0x08-0x7F	ADC Adaptive Coefficients C(0:509)
40	18	0	0x28	0x12	0x00	Page Select Register
40	18	1-7	0x28	0x12	0x01-0x07	Reserved Registers
40	18	8-15	0x28	0x12	0x08-0x0F	ADC Adaptive Coefficients C(510:511)
40	18	16-127	0x28	0x12	0x10-0x7F	Reserved Registers
60	0	0	0x3C	0x00	0x00	Page Select Register
60	0	1-126	0x3C	0x00	0x01-0x7E	Reserved Registers
60	0	127	0x3C	0x00	0x7F	Book Selection Register
60	1-35	0	0x3C	0x01-0x23	0x00	Page Select Register
60	1-35	1-7	0x3C	0x01-0x23	0x01-0x07	Reserved Registers
60	1-35	8-127	0x3C	0x01-0x23	0x08-0x7F	DAC Fixed Coefficients C(0:1023)
80	0	0	0x50	0x00	0x00	Page Select Register
80	0	1	0x50	0x00	0x01	DAC Adaptive Coefficient Bank 1 Configuration Register
80	0	2-126	0x50	0x00	0x02-0x7E	Reserved Registers
80	0	127	0x50	0x00	0x7F	Book Selection Register
80	1-17	0	0x50	0x01-0x11	0x00	Page Select Register
80	1-17	1-7	0x50	0x01-0x11	0x01-0x07	Reserved Registers
80	1-17	8-127	0x50	0x01-0x11	0x08-0x7F	DAC Adaptive Coefficient Bank 1 C(0:509)
80	18	0	0x50	0x12	0x00	Page Select Register
80	18	1-7	0x50	0x12	0x01-0x07	Reserved Registers
80	18	8-15	0x50	0x12	0x08-0x0F	DAC Adaptive Coefficient Bank 1 C(510:511)
80	18	16-127	0x50	0x12	0x10-0x7F	Reserved Registers
82	0	0	0x52	0x00	0x00	Page Select Register

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
82	0	1	0x52	0x00	0x01	DAC Adaptive Coefficient Bank 2 Configuration Register
82	0	2-126	0x52	0x00	0x02-0x7E	Reserved Registers
82	0	127	0x52	0x00	0x7F	Book Selection Register
82	1-17	0	0x52	0x01-0x11	0x00	Page Select Register
82	1-17	1-7	0x52	0x01-0x11	0x01-0x07	Reserved Registers
82	1-17	8-127	0x52	0x01-0x11	0x08-0x7F	DAC Adaptive Coefficient Bank 2 C(0:509)
82	18	0	0x52	0x12	0x00	Page Select Register
82	18	1-7	0x52	0x12	0x01-0x07	Reserved Registers
82	18	8-15	0x52	0x12	0x08-0x0F	DAC Adaptive Coefficient Bank 2 C(510:511)
82	18	16-127	0x52	0x12	0x10-0x7F	Reserved Registers
100	0	0	0x64	0x00	0x00	Page Select Register
100	0	1-46	0x64	0x00	0x01-0x2E	Reserved Registers
100	0	47	0x64	0x00	0x2F	Non-Programmable Override Options
100	0	48	0x64	0x00	0x30	ADC miniDSP_A Instruction Control Register 1
100	0	49	0x64	0x00	0x31	ADC miniDSP_A Instruction Control Register 2
100	0	50	0x64	0x00	0x32	ADC miniDSP_A CIC Input and Decimation Ratio Control Register
100	0	51-59	0x64	0x00	0x33-0x3B	Reserved Registers
100	0	60	0x64	0x00	0x3C	ADC miniDSP_A Secondary CIC Input Control
100	0	61	0x64	0x00	0x3D	miniDSP_A to Audio Serial Interface Handoff Control
100	0	62-126	0x64	0x00	0x3E-0x7E	Reserved Registers
100	0	127	0x64	0x00	0x7F	Book Selection Register
100	1-52	0	0x64	0x01-0x34	0x00	Page Select Register
100	1-52	1-7	0x64	0x01-0x34	0x01-0x07	Reserved Registers
100	1-52	8-127	0x64	0x01-0x34	0x08-0x7F	miniDSP_A Instructions
120	0	0	0x78	0x00	0x00	Page Select Register
120	0	1-46	0x78	0x00	0x01-0x2E	Reserved Registers
120	0	47	0x78	0x00	0x2F	Non-Programmable Override Options
120	0	48	0x78	0x00	0x30	DAC miniDSP_D Instruction Control Register 1
120	0	49	0x78	0x00	0x31	DAC miniDSP_D Instruction Control Register 2
120	0	50	0x78	0x00	0x32	DAC miniDSP_D Interpolation Factor Control Register
120	0	51-126	0x78	0x00	0x33-0x7E	Reserved Registers
120	0	127	0x78	0x00	0x7F	Book Selection Register
120	1-103	0	0x78	0x01-0x67	0x00	Page Select Register

Register Maps (continued)

Table 52. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
120	1-103	1-7	0x78	0x01-0x67	0x01-0x07	Reserved Registers
120	1-103	8-127	0x78	0x01-0x67	0x08-0x7F	miniDSP_D Instructions

8.6.2 Book 0 Page 0

Book 0 / Page 0 / Register 0: Page Select Register - 0x00 / 0x00 / 0x00 (B0_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 0 / Page 0 / Register 1: Software Reset Register - 0x00 / 0x00 / 0x01 (B0_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R	0000 000	Reserved. Write only reset values.
D0	R/W	0	Self clearing software reset bit 0: Don't care 1: Self clearing software reset

Book 0 / Page 0 / Register 2-3: Reserved Registers - 0x00 / 0x00 / 0x02-0x03 (B0_P0_R2-3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 0 / Page 0 / Register 4: Clock Control Register 1, Clock Input Multiplexers - 0x00 / 0x00 / 0x04 (B0_P0_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	DAC_CLKIN Selection Control 0000: DAC_CLKIN = MCLK (Device Pin) **** Refer to the clocking diagram 0001: DAC_CLKIN = BCLK1 (Device Pin) **** Refer to the clocking diagram 0010: DAC_CLKIN = GPIO1 (Device Pin) **** Refer to the clocking diagram 0011: DAC_CLKIN = PLL_CLK (Generated On-Chip) **** Refer to the clocking diagram 0100: DAC_CLKIN = BCLK2 (Device Pin) **** Refer to the clocking diagram 0101: DAC_CLKIN = GPIO3 (Device Pin) **** Refer to the clocking diagram 0110: DAC_CLKIN = HF_REF_CLK **** Refer to the clocking diagram 0111: DAC_CLKIN = HF_OSC_CLK **** Refer to the clocking diagram 1000: Reserved. Do not use. 1001: DAC_CLKIN = GPIO2 (Device Pin) **** Refer to the clocking diagram 1010: Reserved. Do not use. 1011-1111: Reserved. Do not use.

Book 0 / Page 0 / Register 4: Clock Control Register 1, Clock Input Multiplexers - 0x00 / 0x00 / 0x04 (B0_P0_R4) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	ADC_CLKIN Selection Control 0000: ADC_CLKIN = MCLK (Device Pin) **** Refer to the clocking diagram 0001: ADC_CLKIN = BCLK1 (Device Pin) **** Refer to the clocking diagram 0010: ADC_CLKIN = GPIO1 (Device Pin) **** Refer to the clocking diagram 0011: ADC_CLKIN = PLL_CLK (Generated On-Chip) **** Refer to the clocking diagram 0100: ADC_CLKIN = BCLK2 (Device Pin) **** Refer to the clocking diagram 0101: ADC_CLKIN = GPIO3 (Device Pin) **** Refer to the clocking diagram 0110: ADC_CLKIN = HF_REF_CLK **** Refer to the clocking diagram 0111: ADC_CLKIN = HF_OSC_CLK **** Refer to the clocking diagram 1000: Reserved. Do not use. 1001: ADC_CLKIN = GPIO2 (Device Pin) **** Refer to the clocking diagram 1010: Reserved. Do not use. 1011-1111: Reserved. Do not use.

Book 0 / Page 0 / Register 5: Clock Control Register 2, PLL Input Multiplexer - 0x00 / 0x00 / 0x05 (B0_P0_R5)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	0	PLL Clock Range Selection Control 0: Low PLL Clock Range 1: High PLL Clock Range
D5-D2	R/W	00 00	PLL_CLKIN Selection Control 0000: PLL_CLKIN = MCLK (Device Pin) 0001: PLL_CLKIN = BCLK1 (Device Pin) 0010: PLL_CLKIN = GPIO1 (Device Pin) 0011: PLL_CLKIN = DIN1 (can be used for the system where DAC is not used) 0100: PLL_CLKIN = BCLK2 (Device Pin) 0101: PLL_CLKIN = GPIO3 (Device Pin) 0110: PLL_CLKIN = HF_REF_CLK **** Refer to the clocking diagram 0111: PLL_CLKIN = GPIO2 (Device Pin) **** Refer to the clocking diagram 1000-1001: Reserved. Do not use. 1010-1111: Reserved. Do not use.
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 0 / Register 6: Clock Control Register 3, PLL P and R Values - 0x00 / 0x00 / 0x06 (B0_P0_R6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Power Control 0: PLL Power Down 1: PLL Power Up
D6-D4	R/W	001	PLL Divider P Control 000: P=8 001: P=1 010: P=2 011: P=3 100: P=4 101: P=5 110: P=6 111: P=7
D3-D0	R/W	0001	PLL Multiplier R Control 0000: R = 16 0001: R = 1 0010: R = 2 ... 1110: R = 14 1111: R = 15

Book 0 / Page 0 / Register 7: Clock Control Register 4, PLL J Value - 0x00 / 0x00 / 0x07 (B0_P0_R7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Reserved. Write only reset values.
D5-D0	R/W	00 0100	PLL Multiplier J 00 0000: Reserved. Do not use. 00 0001: J=1 00 0010: J=2 … 11 1110: J=62 11 1111: J=63

Book 0 / Page 0 / Register 8: Clock Control Register 5, PLL D Values (MSB) - 0x00 / 0x00 / 0x08 (B0_P0_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D0	R/W	00 0000	PLL D Value MSB 6 Bits of 14-Bit Fraction 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 ... 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000 ... 11 1111 1111 1111: Do not use Note: This register will be updated only when the B0_P0_R9 is written immediately after B0_P0_R8

Book 0 / Page 0 / Register 9: Clock Control Register 6, PLL D Values (LSB) - 0x00 / 0x00 / 0x09 (B0_P0_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	PLL D Value LSB 8 Bits of 14-Bit Fraction 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 ... 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000 ...11 1111 1111 1111: Do not use Note: B0_P0_R9 should be written immediately after B0_P0_R8.

Book 0 / Page 0 / Register 10: Clock Control Register 7, PLL_CLKIN Divider - 0x00 / 0x00 / 0x0A (B0_P0_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0001	PLL_CLKIN Divider (Generates Input Clock for PLL P Divider) 000 0000: PLL_CLKIN Divider = 128 000 0001: PLL_CLKIN Divider = 1 000 0010: PLL_CLKIN Divider = 2 ... 111 1110: PLL_CLKIN Divider = 126 111 1111: PLL_CLKIN Divider = 127

Book 0 / Page 0 / Register 11: Clock Control Register 8, NDAC Divider Values - 0x00 / 0x00 / 0x0B (B0_P0_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NDAC Divider Power Control 0: NDAC divider powered down 1: NDAC divider powered up

Book 0 / Page 0 / Register 11: Clock Control Register 8, NDAC Divider Values - 0x00 / 0x00 / 0x0B (B0_P0_R11) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0001	NDAC Value 000 0000: NDAC=128 000 0001: NDAC=1 000 0010: NDAC=2 ... 111 1110: NDAC=126 111 1111: NDAC=127 Note: Please check the clock frequency requirements in the Overview section

Book 0 / Page 0 / Register 12: Clock Control Register 9, MDAC Divider Values - 0x00 / 0x00 / 0x0C (B0_P0_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MDAC Divider Power Control 0: MDAC divider powered down 1: MDAC divider powered up
D6-D0	R/W	000 0001	MDAC Value 000 0000: MDAC=128 000 0001: MDAC=1 000 0010: MDAC=2 ... 111 1110: MDAC=126 111 1111: MDAC=127 Note: Please check the clock frequency requirements in the Overview section

Book 0 / Page 0 / Register 13: DAC OSR Control Register 1, MSB Value - 0x00 / 0x00 / 0x0D (B0_P0_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1-D0	R/W	00	DAC OSR (DOSR) Control DAC OSR(MSB) and DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 ... 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register is updated when B0_P0_R14 is written to immediately after B0_P0_R13.

Book 0 / Page 0 / Register 14: DAC OSR Control Register 2, LSB Value - 0x00 / 0x00 / 0x0E (B0_P0_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1000 0000	DAC OSR (DOSR) Control DAC OSR(MSB) and DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 ... 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register should be written immediately after B0_P0_R13.

Book 0 / Page 0 / Register 15-17: Reserved Registers - 0x00 / 0x00 / 0x0F-0x11 (B0_P0_R15-17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 18: Clock Control Register 10, NADC Values - 0x00 / 0x00 / 0x12 (B0_P0_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NADC Clock Divider Power Control 0: NADC divider powered down, ADC_CLK is same as DAC_CLK 1: NADC divider powered up
D6-D0	R/W	000 0001	NADC Value 000 0000: NADC=128 000 0001: NADC=1 ... 111 1110: NADC=126 111 1111: NADC=127

Book 0 / Page 0 / Register 19: Clock Control Register 11, MADC Values - 0x00 / 0x00 / 0x13 (B0_P0_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MADC Clock Divider Power Control 0: MADC divider powered down, ADC_MOD_CLK is same as DAC_MOD_CLK 1: MADC divider powered up
D6-D0	R/W	000 0001	MADC Value 000 0000: MADC=128 000 0001: MADC=1 ... 111 1110: MADC=126 111 1111: MADC=127

Book 0 / Page 0 / Register 20: ADC Oversampling (AOSR) Register - 0x00 / 0x00 / 0x14 (B0_P0_R20)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001: ADC AOSR = 1 0000 0010: ADC AOSR = 2 ... 0010 0000: ADC AOSR=32 (Use with ADC Filter Type C) ... 0100 0000: AOSR=64 (Use with ADC Filter Type A or B) ... 1000 0000: AOSR=128 (Use with ADC Filter Type A) ... 1111 1110: ADC AOSR = 254 1111 1111: ADC AOSR = 255 Note: If the ADC miniDSP will be used for signal processing ADC (B0_P0_R61) AOSR should be an integral multiple of ADC DECIM factor.

Book 0 / Page 0 / Register 21: CLKOUT MUX - 0x00 / 0x00 / 0x15 (B0_P0_R21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0000	00000: CDIV_CLKIN = MCLK (Device Pin) 00001: CDIV_CLKIN = BCLK1 (Device Pin) 00010: CDIV_CLKIN = DIN1 (Can be used for the systems where DAC is not required) 00011: CDIV_CLKIN = PLL_CLK (Generated On-Chip) 00100: CDIV_CLKIN = DAC_CLK (Generated On-Chip) 00101: CDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 00110: CDIV_CLKIN = ADC_CLK (Generated On-Chip) 00111: CDIV_CLKIN = ADC_MOD_MCLK (Generated On-Chip) 01000: CDIV_CLKIN = BCLK2 (Device Pin) 01001: CDIV_CLKIN = GPIO3 (Device Pin) 01010: CDIV_CLKIN = High Frequency Reference Clock Generated On-Chip using HF_OSC_CLK and LFR_CLKIN 01011: CDIV_CLKIN = High Frequency Oscillator Clock (Generated On-Chip) 01100-11111: Reserved. Do not use.

Book 0 / Page 0 / Register 22: Clock Control Register 12, CLKOUT M Divider Value - 0x00 / 0x00 / 0x16 (B0_P0_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	CLKOUT M Divider Power Control 0: CLKOUT M divider powered down 1: CLKOUT M divider powered up
D6-D0	R/W	000 0001	CLKOUT M Divider Value 000 0000: CLKOUT M divider = 128 000 0001: CLKOUT M divider = 1 000 0010: CLKOUT M divider = 2 ... 111 1110: CLKOUT M divider = 126 111 1111: CLKOUT M divider = 127 Note: Please check the clock frequency requirments in the application overview section.

Book 0 / Page 0 / Register 23: Timer clock - 0x00 / 0x00 / 0x17 (B0_P0_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	This timer clock of 1MHz is used for multiple purpose like all the interrupt generation for GPIO1, GPIO2, debounce logic, and headset detection. Select the 1MHz Timer Clock Source 0: REF_1MHZ_CLK = LF_OSC_CLK / 8 1: REF_1MHZ_CLK = MCLK / M (M as defined in D6:0 below)
D6-D0	R/W	000 0001	MCLK Divider (M) Used to Generate REF_1MHZ_CLK 000 0000: M = 128 000 0001: M = 1 000 0010: M = 2 … 111 1110: M = 126 111 1111: M = 127

Book 0 / Page 0 / Register 24: Low Frequency Clock Generation Control - 0x00 / 0x00 / 0x18 (B0_P0_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	0000: LFR_CLKIN (Low frequency reference clock) = MCLK (Device Pin) 0001: LFR_CLKIN = WCLK1 (Device Pin) 0010: LFR_CLKIN = GPIO1 (Device Pin) 0011: LFR_CLKIN = WCLK2 (Device Pin) 0100: LFR_CLKIN = BCLK2 (Device Pin) 0101: LFR_CLKIN = GPIO3 (Device Pin) 0110: LFR_CLKIN = DIN2 (Device Pin) 0111: Reserved. Do not use. 1000: LFR_CLKIN = GPIO2 (Device Pin) 1001: Reserved. Do not use. 1010-1111: Reserved. Do not use.
D3-D0	R/W	1111	0000: HF_CLKIN (High frequency clock) = MCLK (Device Pin) 0001 - 1110: Reserved. Do not use. 1111: HF_CLKIN = HF_OSC_CLK

Book 0 / Page 0 / Register 25: High Frequency Clock Generation Control 1 - 0x00 / 0x00 / 0x19 (B0_P0_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	1	High Frequency Reference Clock Settling Flag 0: High Frequency Reference Clock is Settled 1: High Frequency Reference Clock is not Settled
D6	R	0	High Frequency Reference Clock Modulator Overflow Flag 0: High Frequency Reference Clock Modulator Overflow has not occurred 1: High Frequency Reference Clock Modulator Overflow has occurred

Book 0 / Page 0 / Register 25: High Frequency Clock Generation Control 1 - 0x00 / 0x00 / 0x19 (B0_P0_R25) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	HF_REF_CLK Lock Ready Threshold 00: 2048 reference clock cycles 01: 512 reference clock cycles 10: 32 reference clock cycles 11: 8 reference clock cycles
D3-D0	R/W	0000	Ratio(27:24): Upper 4-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

Book 0 / Page 0 / Register 26: High Frequency Clock Generation Control 2 - 0x00 / 0x00 / 0x1A (B0_P0_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Ratio(23:16): Next 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

Book 0 / Page 0 / Register 27: High Frequency Clock Generation Control 3 - 0x00 / 0x00 / 0x1B (B0_P0_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 1000	Ratio(16:8): Next 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

Book 0 / Page 0 / Register 28: High Frequency Clock Generation Control 4 - 0x00 / 0x00 / 0x1C (B0_P0_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0110 1010	Ratio(7:0): Lower 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

Book 0 / Page 0 / Register 29: High Frequency Clock Trim Control 1 - 0x00 / 0x00 / 0x1D (B0_P0_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	High Frequency Oscillator Calibration Flag 0: Calibration is not complete 1: Calibration is complete
D6	R/W	0	High Frequency Oscillator Voltage Source Control 0: AVDDx_18 1: DVDD_18
D5	R/W	1	High Frequency Oscillator Calibration Enable Control 0: Calibration is disabled 1: Calibration is enabled
D4-D2	R	0 00	Reserved. Write only reset values.
D1-D0	R/W	00	Ratio(25:24): Upper 2 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

Book 0 / Page 0 / Register 30: High Frequency Clock Trim Control 2 - 0x00 / 0x00 / 0x1E (B0_P0_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Ratio(23:16): Next 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

Book 0 / Page 0 / Register 31: High Frequency Clock Trim Control 3 - 0x00 / 0x00 / 0x1F (B0_P0_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0110	Ratio(15:8): Next 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

Book 0 / Page 0 / Register 32: High Frequency Clock Trim Control 4 - 0x00 / 0x00 / 0x20 (B0_P0_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 1010	Ratio(7:0): Lower 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

Book 0 / Page 0 / Register 33-35: Reserved Registers - 0x00 / 0x00 / 0x21-0x23 (B0_P0_R33-35)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 36: ADC Flag Register - 0x00 / 0x00 / 0x24 (B0_P0_R36)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status Flag 0: Gain Applied in Left ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Left ADC PGA is equal to Programmed Gain in Control Register
D6	R	0	Left ADC Power Status Flag 0: Left ADC Powered Down 1: Left ADC Powered Up
D5	R	0	Left AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Left AGC is not saturated 1: Gain in Left ADC is equal to maximum allowed gain in Left AGC
D4	R	0	Reserved. Write only reset values.
D3	R	0	Right ADC PGA Status Flag 0: Gain Applied in Right ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Right ADC PGA is equal to Programmed Gain in Control Register
D2	R	0	Right ADC Power Status Flag 0: Right ADC Powered Down 1: Right ADC Powered Up
D1	R	0	Right AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Right AGC is not saturated 1: Gain in Right ADC is equal to maximum allowed gain in Right AGC
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 37: DAC Flag Register - 0x00 / 0x00 / 0x25 (B0_P0_R37)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: Left DAC Powered Down 1: Left DAC Powered Up
D6	R	0	Reserved. Write only reset values.
D5-D4	R	00	00: Jack is not inserted 01: Jack is inserted without Microphone 10: Reserved. Do not use. 11: Jack is inserted with Microphone
D3	R	0	0: Right DAC Powered Down 1: Right DAC Powered Up
D2	R	0	Reserved. Write only reset values.
D1-D0	R	00	00: Headset is not inserted 01: Jack is inserted with mono-HS (Ground-Centered or Capless Headphone Mode Only) 10: Jack is inserted with stereo-HS (Ground-Centered or Capless Headphone Mode Only) 11: Reserved. Do not use.

Book 0 / Page 0 / Register 38: DAC Flag Register - 0x00 / 0x00 / 0x26 (B0_P0_R38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	1	Reserved
D6	R	1	0: Primary Left DAC PGA is not muted 1: Primary Left DAC PGA is muted
D5	R	0	Reserved
D4	R	0	0: Primary Left DAC PGA , Applied Gain /= Programmed Gain 1: Primary Left DAC PGA , Applied Gain = Programmed Gain
D3	R	1	Reserved
D2	R	1	0: Primary Right DAC PGA is not muted 1: Primary Right DAC PGA is muted
D1	R	0	Reserved
D0	R	0	0: Primary Right DAC PGA , Applied Gain /= Programmed Gain 1: Primary Right DAC PGA , Applied Gain = Programmed Gain

Book 0 / Page 0 / Register 39-41: Reserved Registers - 0x00 / 0x00 / 0x27-0x29 (B0_P0_R39-41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only default values.

Book 0 / Page 0 / Register 42: Sticky Flag Register 1 - 0x00 / 0x00 / 0x2A (B0_P0_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left DAC 1: Overflow has happened in Left DAC since last read of this register
D6	R	0	Right DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right DAC 1: Overflow has happened in Right DAC since last read of this register
D5	R	0	miniDSP_D Barrel Shifter Output Overflow Sticky Flag. Flag is reset on register reading
D4	R	0	Reserved.
D3	R	0	Left ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left ADC 1: Overflow has happened in Left ADC since last read of this register
D2	R	0	Right ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right ADC 1: Overflow has happened in Right ADC since last read of this register
D1	R	0	miniDSP_A Barrel Shifter Output Overflow Sticky Flag. Flag is reset on register reading
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 43: Reserved Register - 0x00 / 0x00 / 0x2B (B0_P0_R43)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved Register

Book 0 / Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x00 / 0x2C (B0_P0_R44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No Short Circuit detected at HPL or SPL or RECP driver. 1: Short Circuit is detected at HPL or SPL or RECP driver. (will be cleared when the register is read)
D6	R	0	0: No Short Circuit detected at HPR or SPR or RECM driver. 1: Short Circuit is detected at HPR or SPR or RECM driver. (will be cleared when the register is read)

Book 0 / Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x00 / 0x2C (B0_P0_R44) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected (will be cleared when the register is read)
D4	R	0	Headset Insertion or Removal Detect Flag 0: Insertion or Removal event not detected 1: Insertion or Removal event detected (will be cleared when the register is read)
D3-D2	R	00	Reserved.
D1	R	0	miniDSP_D Standard Interrupt Port Output. This is a sticky bit
D0	R	0	miniDSP_D Auxilliary Interrupt Port Output. This is a sticky bit

Book 0 / Page 0 / Register 45: Sticky Flag Register 3 - 0x00 / 0x00 / 0x2D (B0_P0_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No over-temperature detected by Speaker driver. 1: Over-temperature detected by Speaker driver. (will be cleared when the register is read)
D6	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D5	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D4	R	0	miniDSP_A Standard Interrupt Port Output. This is a sticky bit
D3	R	0	miniDSP_A Auxilliary Interrupt Port Output. This is a sticky bit
D2-D0	R	000	Reserved.

Book 0 / Page 0 / Register 46-47: Reserved Register - 0x00 / 0x00 / 0x2E-0x2F (B0_P0_R46-47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved Register

Book 0 / Page 0 / Register 48: INT1 Interrupt Control - 0x00 / 0x00 / 0x30 (B0_P0_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT1 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT1 interrupt 1: Headset Insertion even will generate a INT1 interrupt
D6	R/W	0	INT1 Interrupt for Button Press Event 0: Button Press event will not generate a INT1 interrupt 1: Button Press event will generate a INT1 interrupt
D5	R/W	0	Reserved. Write only default value
D4	R/W	0	INT1 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT1 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT1 interrupt. Read B0_P0_R45 to distinguish between Left or Right Channel
D3	R/W	0	INT1 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT1 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT1 interrupt. Read B0_P0_R44 to distinguish between HPL and HPR
D2	R/W	0	INT1 Interrupt for miniDSP-generated interrupt or overflow event 0: Engine generated interrupts and Overflow flags do not result in a INT1 interrupt 1: Engine generated interrupts and Overflow flags will result in a INT1 interrupt. Read B0_P0_R42 to distinguish between miniDSP_A or miniDSP_D interrupt
D1	R/W	0	0: SPK over-tempeature detected Interrupt is not used in the generation of INT1 Interrupt 1: SPK over-tempeature detected Interrupt is used in the generation of INT1 Interrupt

Book 0 / Page 0 / Register 48: INT1 Interrupt Control - 0x00 / 0x00 / 0x30 (B0_P0_R48) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 49: INT2 Interrupt Control - 0x00 / 0x00 / 0x31 (B0_P0_R49)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT2 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT2 interrupt 1: Headset Insertion even will generate a INT2 interrupt
D6	R/W	0	INT2 Interrupt for Button Press Event 0: Button Press event will not generate a INT2 interrupt 1: Button Press event will generate a INT2 interrupt
D5	R/W	0	Reserved. Write only default value
D4	R/W	0	INT2 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT2 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT2 interrupt. Read B0_P0_R45 to distinguish between Left or Right Channel
D3	R/W	0	INT2 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT2 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT2 interrupt. Read B0_P0_R44 to distinguish between HPL and HPR
D2	R/W	0	INT2 Interrupt for miniDSP-generated interrupt or overflow event 0: Engine generated interrupts and Overflow flags do not result in a INT2 interrupt 1: Engine generated interrupts and Overflow flags will result in a INT2 interrupt. Read B0_P0_R42 to distinguish between miniDSP_A or miniDSP_D interrupt
D1	R/W	0	0: SPK over-tempeature detected Interrupt is not used in the generation of INT2 Interrupt 1: SPK over-tempeature detected Interrupt is used in the generation of INT2 Interrupt
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 50: SAR Control 1 - 0x00 / 0x00 / 0x32 (B0_P0_R50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: If SAR measurement data out of threshold range, interrupt is not used in the generation of INT1 Interrupt. 1: If SAR measurement data out of threshold range, interrupt is used in the generation of INT1 Interrupt.
D6	R/W	0	0: SAR Data Available Interrupt is not used in the generation of INT1 Interrupt. 1: SAR Data Available Interrupt is used in the generation of INT1 Interrupt.
D5	R/W	0	0: SAR measurement data out of threshold range Interrupt is not used in the generation of INT2 Interrupt. 1: SAR measurement data out of threshold range Interrupt is used in the generation of INT2 Interrupt.
D4	R/W	0	0: SAR Data Available Interrupt is not used in the generation of INT2 Interrupt. 1: SAR Data Available Interrupt is used in the generation of INT2 Interrupt.
D3	R	0	Reserved. Write only default values.
D2	R	0	SAR Data Available Sticky Flag (will be cleared when the register is read) 0: No SAR Data Available for read. 1: SAR Data Available for read.
D1	R	0	SAR Data Threshold Sticky Flag (will be cleared when the register is read) 0: SAR data is within threshold program. 1: SAR data is out of programmed threshold range.
D0	R	0	Reserved. Write only default values.

Book 0 / Page 0 / Register 51: Interrupt Format Control Register - 0x00 / 0x00 / 0x33 (B0_P0_R51)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	INT1 pulse control 00: INT1 is active high interrupt of 1 pulse of minimum 2ms duration 01: INT1 is active high interrupt of multiple pulses, each of minimum duration 2ms and a total period of 4ms. To stop the pulse train, read B0_P0_R42, B0_P0_R44, or B0_P0_R45 10: INT1 is active high, level-based interrupt generated out of sticky bits in Flag registers. To clear this interrupt, read B0_P0_R42, B0_P0_R44, or B0_P0_R45. 11: INT1 is active high, level-based interrupt generated out of instantaneous value of interrupt port.
D5-D4	R/W	00	INT2 pulse control 00: INT2 is active high interrupt of 1 pulse of approx. 2ms duration 01: INT2 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read B0_P0_R42, B0_P0_R44, or B0_P0_R45 10: INT2 is active high, level-based interrupt generated out of sticky bits in Flag registers. To clear this interrupt, read B0_P0_R42, B0_P0_R44, or B0_P0_R45. 11: INT2 is active high, level-based interrupt generated out of instantaneous value of interrupt port.
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 52-59: Reserved Registers - 0x00 / 0x00 / 0x34-0x3B (B0_P0_R52-59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 0 / Register 60: DAC Processing Block and miniDSP Power Control - 0x00 / 0x00 / 0x3C (B0_P0_R60)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: miniDSP_A and miniDSP_D are independently powered up 1: miniDSP_A and miniDSP_D are powered up together. Useful when there is data transfer between miniDSP_A and miniDSP_D
D6	R/W	0	miniDSP_D Power Configuration 0: miniDSP_D is powered down with DAC Channel Power Down 1: miniDSP_D is powered up if ADC Channel is powered up
D5	R	0	Reserved. Write only reset values.
D4-D0	R/W	0 0001	0 0000: The miniDSP_D will be used for signal processing 0 0001: DAC Signal Processing Block PRB_P1 0 0010: Do not use. 0 0011: DAC Signal Processing Block PRB_P3 0 0100-0 0101: Do not use. 0 0110: DAC Signal Processing Block PRB_P6 0 0111-1 1111: Do not use.

Book 0 / Page 0 / Register 61: ADC Processing Block Control - 0x00 / 0x00 / 0x3D (B0_P0_R61)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0001	0 0000: The miniDSP_A will be used for signal processing 0 0001: ADC Singal Processing Block PRB_R1 0 0010-0 0011: Do not use. 0 0100: ADC Signal Processing Block PRB_R4 0 0101-1 1111: Do not use.

Book 0 / Page 0 / Register 62: Reserved Register - 0x00 / 0x00 / 0x3E (B0_P0_R62)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 63: Primary DAC Power and Soft-Stepping Control - 0x00 / 0x00 / 0x3F (B0_P0_R63)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left DAC channel is powered-down 1: Left DAC channel is powered-up
D6	R/W	0	0: Right DAC channel is powered-down 1: Right DAC channel is powered-up
D5-D2	R	00 00	Reserved. Write only reset values.
D1-D0	R/W	00	00: DAC channel volume control soft-stepping is enabled for one-step per Fs 01: DAC channel volume control soft-stepping is enabled for one-step per 2Fs 10: DAC channel volume control soft-stepping is disabled 11: Reserved. Do not use.

Book 0 / Page 0 / Register 64: Primary DAC Master Volume Configuration - 0x00 / 0x00 / 0x40 (B0_P0_R64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right Modulator Output Control 0: When Right DAC Channel is powered down, the data is zero. 1: When Right DAC Channel is powered down, the data is inverted version of Left DAC Modulator Output. Can be used when differential mono output is used
D6-D4	R/W	000	DAC Auto Mute Control 000: Auto Mute disabled 001: DAC is auto muted if input data is DC for more than 100 consecutive inputs 010: DAC is auto muted if input data is DC for more than 200 consecutive inputs 011: DAC is auto muted if input data is DC for more than 400 consecutive inputs 100: DAC is auto muted if input data is DC for more than 800 consecutive inputs 101: DAC is auto muted if input data is DC for more than 1600 consecutive inputs 110: DAC is auto muted if input data is DC for more than 3200 consecutive inputs 111: DAC is auto muted if input data is DC for more than 6400 consecutive inputs
D3	R/W	1	Left DAC Channel Mute Control 0: Left DAC Channel not muted 1: Left DAC Channel muted
D2	R/W	1	Right DAC Channel Mute Control 0: Right DAC Channel not muted 1: Right DAC Channel muted
D1-D0	R/W	00	DAC Master Volume Control 00: Left and Right Channel have independent volume control 01: Left Channel Volume is controlled by Right Channel Volume Control setting 10: Right Channel Volume is controlled by Left Channel Volume Control setting 11: Reserved. Do not use

Book 0 / Page 0 / Register 65: Primary DAC Left Volume Control Setting - 0x00 / 0x00 / 0x41 (B0_P0_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Left DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use. 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB ... 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use.

Book 0 / Page 0 / Register 66: Primary DAC Right Volume Control Setting - 0x00 / 0x00 / 0x42 (B0_P0_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Right DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use. 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB ... 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use.

Book 0 / Page 0 / Register 67: Headset Detection - 0x00 / 0x00 / 0x43 (B0_P0_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset Detection Disabled 1: Headset Detection Enabled
D6-D5	R	00	Reserved. Write only reset values.
D4-D2	R/W	0 00	Headset Detection Debounce Programmability 000: Debounce Time = 16ms 001: Debounce Time = 32ms 010: Debounce Time = 64ms 011: Debounce Time = 128ms 100: Debounce Time = 256ms 101: Debounce Time = 512ms 110-111: Reserved. Do not use Note: All times are typical values
D1-D0	R/W	00	Headset Button Press Debounce Programmability 00: Debounce disabled 01: Debounce Time = 8ms 10: Debounce Time = 16ms 11: Debounce Time = 32ms Note: All times are typical values

Book 0 / Page 0 / Register 68: Reserved Register - 0x00 / 0x00 / 0x44 (B0_P0_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0110 1111	Reserved. Write only reset values.

Book 0 / Page 0 / Register 69: Reserved Register - 0x00 / 0x00 / 0x45 (B0_P0_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0011 1000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 70: Reserved Register - 0x00 / 0x00 / 0x46 (B0_P0_R70)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	

Book 0 / Page 0 / Register 71-80: Reserved Registers - 0x00 / 0x00 / 0x47-0x50 (B0_P0_R71-80)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Do not write

Book 0 / Page 0 / Register 81: ADC Channel Power Control - 0x00 / 0x00 / 0x51 (B0_P0_R81)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Channel ADC Power Control 0: Left Channel ADC power down 1: Left Channel ADC power up
D6	R/W	0	Right Channel ADC Power Control 0: Right Channel ADC power down 1: Right Channel ADC power up
D5-D4	R/W	00	Left Channel Digital Microphone Power Control 00: Left Channel ADC not configured for Digital Microphone 01: Left Channel ADC configured for Digital Microphone 10: Left Channel DAC Modulator output fed thru ADC CIC Filter (Loopback) 11: Reserved. Do not use.
D3-D2	R/W	00	Right Channel Digital Microphone Power Control 00: Right Channel ADC not configured for Digital Microphone 01: Right Channel ADC configured for Digital Microphone 10: Right Channel DAC Modulator output fed thru ADC CIC Filter (Loopback) 11: Reserved. Do not use.
D1-D0	R/W	00	ADC Volume Control Soft-Stepping Control 00: ADC Volume Control changes by 1 gain step per ADC Word Clock 01: ADC Volume Control changes by 1 gain step per two ADC Word Clocks 10: ADC Volume Control Soft-Stepping disabled 11: Reserved. Do not use

Book 0 / Page 0 / Register 82: ADC Fine Gain Volume Control - 0x00 / 0x00 / 0x52 (B0_P0_R82)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC Channel Mute Control 0: Left ADC Channel Un-Mute 1: Left ADC Channel Mute
D6-D4	R/W	000	Left ADC Channel Fine Gain Adjust 000: Left ADC Channel Fine Gain = 0 dB 111: Left ADC Channel Fine Gain = -0.1 dB 110: Left ADC Channel Fine Gain = -0.2 dB 101: Left ADC Channel Fine Gain = -0.3 dB 100: Left ADC Channel Fine Gain = -0.4 dB 001-011: Reserved. Do not use.
D3	R/W	1	Right ADC Channel Mute Control 0: Right ADC Channel Un-Mute 1: Right ADC Channel Mute
D2-D0	R/W	000	Right ADC Channel Fine Gain Adjust 000: Right ADC Channel Fine Gain = 0 dB 111: Right ADC Channel Fine Gain = -0.1 dB 110: Right ADC Channel Fine Gain = -0.2 dB 101: Right ADC Channel Fine Gain = -0.3 dB 100: Right ADC Channel Fine Gain = -0.4 dB 001-011: Reserved. Do not use.

Book 0 / Page 0 / Register 83: Left ADC Volume Control - 0x00 / 0x00 / 0x53 (B0_P0_R83)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 83: Left ADC Volume Control - 0x00 / 0x00 / 0x53 (B0_P0_R83) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0000	Left ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use. 110 1000: Left ADC Channel Volume = -12.0 dB 110 1001: Left ADC Channel Volume = -11.5 dB 110 1010: Left ADC Channel Volume = -11.0 dB … 111 1111: Left ADC Channel Volume = -0.5 dB 000 0000: Left ADC Channel Volume = 0.0 dB 000 0001: Left ADC Channel Volume = 0.5 dB ... 010 0110: Left ADC Channel Volume = 19.0 dB 010 0111: Left ADC Channel Volume = 19.5 dB 010 1000: Left ADC Channel Volume = 20.0 dB 010 1001-111 1111: Reserved. Do not use.

Book 0 / Page 0 / Register 84: Right ADC Volume Control - 0x00 / 0x00 / 0x54 (B0_P0_R84)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0000	Right ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use. 110 1000: Right ADC Channel Volume = -12.0 dB 110 1001: Right ADC Channel Volume = -11.5 dB 110 1010: Right ADC Channel Volume = -11.0 dB … 111 1111: Right ADC Channel Volume = -0.5 dB 000 0000: Right ADC Channel Volume = 0.0 dB 000 0001: Right ADC Channel Volume = 0.5 dB ... 010 0110: Right ADC Channel Volume = 19.0 dB 010 0111: Right ADC Channel Volume = 19.5 dB 010 1000: Right ADC Channel Volume = 20.0 dB 010 1001-111 1111: Reserved. Do not use.

Book 0 / Page 0 / Register 85: ADC Phase Control - 0x00 / 0x00 / 0x55 (B0_P0_R85)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ADC Phase Compensation Control 1000 0000-1111 1111: Left ADC Channel Data is delayed with respect to Right ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section. 0000 0000: Left and Right ADC Channel data are not delayed with respect to each other 0000 0001-0111 1111: Right ADC Channel Data is delayed with respect to Left ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section.

Book 0 / Page 0 / Register 86: Left AGC Control 1 - 0x00 / 0x00 / 0x56 (B0_P0_R86)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left Channel AGC Disabled 1: Left Channel AGC Enabled

Book 0 / Page 0 / Register 86: Left AGC Control 1 - 0x00 / 0x00 / 0x56 (B0_P0_R86) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D4	R/W	000	Left Channel AGC Target Level Setting 000: Left Channel AGC Target Level = -5.5 dBFS 001: Left Channel AGC Target Level = -8.0 dBFS 010: Left Channel AGC Target Level = -10. 0dBFS 011: Left Channel AGC Target Level = -12.0 dBFS 100: Left Channel AGC Target Level = -14.0 dBFS 101: Left Channel AGC Target Level = -17.0 dBFS 110: Left Channel AGC Target Level = -20.0 dBFS 111: Left Channel AGC Target Level = -24.0 dBFS
D3-D2	R	00	Reserved. Write only reset values.
D1-D0	R/W	00	Left Channel AGC Gain Hysteresis Control 00: Left Channel AGC Gain Hysteresis is disabled 01: Left Channel AGC Gain Hysteresis is +/-0.5 dB 10: Left Channel AGC Gain Hysteresis is +/-1.0 dB 11: Left Channel AGC Gain Hysteresis is +/-1.5 dB

Book 0 / Page 0 / Register 87: Left AGC Control 2 - 0x00 / 0x00 / 0x57 (B0_P0_R87)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Left Channel AGC Hysteresis Setting 00: Left Channel AGC Hysteresis is 1.0 dB 01: Left Channel AGC Hysteresis is 2.0 dB 10: Left Channel AGC Hysteresis is 4.0 dB 11: Left Channel AGC Hysteresis is disabled
D5-D1	R/W	0 0000	Left Channel AGC Noise Threshold 0 0000: Left Channel AGC Noise Gate disabled 0 0001: Left Channel AGC Noise Threshold is -30 dB 0 0010: Left Channel AGC Noise Threshold is -32 dB 0 0011: Left Channel AGC Noise Threshold is -34 dB ... 1 1101: Left Channel AGC Noise Threshold is -86 dB 1 1110: Left Channel AGC Noise Threshold is -88 dB 1 1111: Left Channel AGC Noise Threshold is -90 dB
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 88: Left AGC Control 3 - 0x00 / 0x00 / 0x58 (B0_P0_R88)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	111 1111	Left Channel AGC Maximum Gain Setting 000 0000: Left Channel AGC Maximum Gain = 0.0 dB 000 0001: Left Channel AGC Maximum Gain = 0.5 dB 000 0010: Left Channel AGC Maximum Gain = 1.0 dB ... 111 1110: Left Channel AGC Maximum Gain = 63.0 dB 111 1111: Left Channel AGC Maximum Gain = 63.5 dB

Book 0 / Page 0 / Register 89: Left AGC Attack Time - 0x00 / 0x00 / 0x59 (B0_P0_R89)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Left Channel AGC Attack Time Setting 0 0000: Left Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Left Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Left Channel AGC Attack Time = 5*32 ADC Word Clocks ... 1 1101: Left Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Left Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Left Channel AGC Attack Time = 63*32 ADC Word Clocks

Book 0 / Page 0 / Register 89: Left AGC Attack Time - 0x00 / 0x00 / 0x59 (B0_P0_R89) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	Left Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

Book 0 / Page 0 / Register 90: Left AGC Decay Time - 0x00 / 0x00 / 0x5A (B0_P0_R90)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Left Channel AGC Decay Time Setting 0 0000: Left Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Left Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Left Channel AGC Decay Time = 5*512 ADC Word Clocks ... 1 1101: Left Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Left Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Left Channel AGC Decay Time = 63*512 ADC Word Clocks
D2-D0	R/W	000	Left Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

Book 0 / Page 0 / Register 91: Left AGC Noise Debounce - 0x00 / 0x00 / 0x5B (B0_P0_R91)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0000	Left Channel AGC Noise Debounce Time Setting 0 0001: Left Channel AGC Noise Debounce Time = 0 0 0010: Left Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Left Channel AGC Noise Debounce Time = 8 ADC Word Clocks ... 0 1010: Left Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Left Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Left Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Left Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Left Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Left Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Left Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

Book 0 / Page 0 / Register 92: Left AGC Signal Debounce - 0x00 / 0x00 / 0x5C (B0_P0_R92)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 92: Left AGC Signal Debounce - 0x00 / 0x00 / 0x5C (B0_P0_R92) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	Left Channel AGC Signal Debounce Time Setting 0001: Left Channel AGC Signal Debounce Time = 0 0010: Left Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Left Channel AGC Signal Debounce Time = 8 ADC Word Clocks ... 1001: Left Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Left Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Left Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Left Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Left Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Left Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Left Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

Book 0 / Page 0 / Register 93: Left AGC Gain - 0x00 / 0x00 / 0x5D (B0_P0_R93)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Left Channel AGC Gain 1110 1000: Left Channel AGC Gain = -12.0dB 1110 1001: Left Channel AGC Gain = -11.5dB 1110 1010: Left Channel AGC Gain = -11.0dB ... 0000 0000: Left Channel AGC Gain = 0.0dB ... 0111 1101: Left Channel AGC Gain = 62.5dB 0111 1110: Left Channel AGC Gain = 63.0dB 0111 1111: Left Channel AGC Gain = 63.5dB

Book 0 / Page 0 / Register 94: Right AGC Control 1 - 0x00 / 0x00 / 0x5E (B0_P0_R94)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right Channel AGC Disabled 1: Right Channel AGC Enabled
D6-D4	R/W	000	Right Channel AGC Target Level Setting 000: Right Channel AGC Target Level = -5.5 dBFS 001: Right Channel AGC Target Level = -8.0 dBFS 010: Right Channel AGC Target Level = -10.0 dBFS 011: Right Channel AGC Target Level = -12.0 dBFS 100: Right Channel AGC Target Level = -14.0 dBFS 101: Right Channel AGC Target Level = -17.0 dBFS 110: Right Channel AGC Target Level = -20.0 dBFS 111: Right Channel AGC Target Level = -24.0 dBFS
D3-D2	R	00	Reserved. Write only reset values.
D1-D0	R/W	00	Right Channel AGC Gain Hysteresis Control 00: Right Channel AGC Gain Hysteresis is disabled 01: Right Channel AGC Gain Hysteresis is +-0.5 dB 10: Right Channel AGC Gain Hysteresis is +-1.0 dB 11: Right Channel AGC Gain Hysteresis is +-1.5 dB

Book 0 / Page 0 / Register 95: Right AGC Control 2 - 0x00 / 0x00 / 0x5F (B0_P0_R95)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Right Channel AGC Hysteresis Setting 00: Right Channel AGC Hysteresis is 1.0dB 01: Right Channel AGC Hysteresis is 2.0dB 10: Right Channel AGC Hysteresis is 4.0dB 11: Right Channel AGC Hysteresis is disabled

Book 0 / Page 0 / Register 95: Right AGC Control 2 - 0x00 / 0x00 / 0x5F (B0_P0_R95) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D1	R/W	00 000	Right Channel AGC Noise Threshold 0 0000: Right Channel AGC Noise Gate disabled 0 0001: Right Channel AGC Noise Threshold is -30dB 0 0010: Right Channel AGC Noise Threshold is -32dB 0 0011: Right Channel AGC Noise Threshold is -34dB ... 1 1101: Right Channel AGC Noise Threshold is -86dB 1 1110: Right Channel AGC Noise Threshold is -88dB 1 1111: Right Channel AGC Noise Threshold is -90dB
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 96: Right AGC Control 3 - 0x00 / 0x00 / 0x60 (B0_P0_R96)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	111 1111	Right Channel AGC Maximum Gain Setting 000 0000: Right Channel AGC Maximum Gain = 0.0dB 000 0001: Right Channel AGC Maximum Gain = 0.5dB 000 0010: Right Channel AGC Maximum Gain = 1.0dB ... 111 1110: Right Channel AGC Maximum Gain = 63.0dB 111 1111: Right Channel AGC Maximum Gain = 63.5dB

Book 0 / Page 0 / Register 97: Right AGC Attack Time - 0x00 / 0x00 / 0x61 (B0_P0_R97)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Right Channel AGC Attack Time Setting 0 0000: Right Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Right Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Right Channel AGC Attack Time = 5*32 ADC Word Clocks ... 1 1101: Right Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Right Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Right Channel AGC Attack Time = 63*32 ADC Word Clocks
D2-D0	R/W	000	Right Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

Book 0 / Page 0 / Register 98: Right AGC Decay Time - 0x00 / 0x00 / 0x62 (B0_P0_R98)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0 0000	Right Channel AGC Decay Time Setting 0 0000: Right Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Right Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Right Channel AGC Decay Time = 5*512 ADC Word Clocks ... 1 1101: Right Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Right Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Right Channel AGC Decay Time = 63*512 ADC Word Clocks

Book 0 / Page 0 / Register 98: Right AGC Decay Time - 0x00 / 0x00 / 0x62 (B0_P0_R98) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	Right Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

Book 0 / Page 0 / Register 99: Right AGC Noise Debounce - 0x00 / 0x00 / 0x63 (B0_P0_R99)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4-D0	R/W	0 0000	Right Channel AGC Noise Debounce Time Setting 0 0001: Right Channel AGC Noise Debounce Time = 0 0 0010: Right Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Right Channel AGC Noise Debounce Time = 8 ADC Word Clocks ... 0 1010: Right Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Right Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Right Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Right Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Right Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Right Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Right Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

Book 0 / Page 0 / Register 100: Right AGC Signal Debounce - 0x00 / 0x00 / 0x64 (B0_P0_R100)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3-D0	R/W	0000	Right Channel AGC Signal Debounce Time Setting 0001: Right Channel AGC Signal Debounce Time = 0 0010: Right Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Right Channel AGC Signal Debounce Time = 8 ADC Word Clocks ... 1001: Right Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Right Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Right Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Right Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Right Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Right Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Right Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

Book 0 / Page 0 / Register 101: Right AGC Gain - 0x00 / 0x00 / 0x65 (B0_P0_R101)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Right Channel AGC Gain 1110 1000: Left Channel AGC Gain = -12.0dB 1110 1001: Left Channel AGC Gain = -11.5dB 1110 1010: Left Channel AGC Gain = -11.0dB ... 0000 0000: Left Channel AGC Gain = 0.0dB ... 0111 1101: Left Channel AGC Gain = 62.5dB 0111 1110: Left Channel AGC Gain = 63.0dB 0111 1111: Left Channel AGC Gain = 63.5dB

Book 0 / Page 0 / Register 102-111: Reserved Registers - 0x00 / 0x00 / 0x66-0x6F (B0_P0_R102-111)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only default values.

Book 0 / Page 0 / Register 112: Digital Microphone 2 Control - 0x00 / 0x00 / 0x70 (B0_P0_R112)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: CIC2 Left Channel is disabled 1: CIC2 Left Channel is enabled
D6	R/W	0	0: CIC2 Right Channel is disabled 1: CIC2 Right Channel is enabled
D5-D4	R/W	00	00: CIC2 Left Channel not in use (B0_P0_R112_D7 is set to '0') 01: Digital Microphone is fed to CIC2 Left Channel 10: Left DAC Modulator output is fed to CIC2 Left Channel 11: Reserved. Do not use.
D3-D2	R/W	00	00: CIC2 Right Channel not in use (B0_P0_R112_D6 is set to '0') 01: Digital Microphone is fed to CIC2 Right Channel 10: Right DAC Modulator output is fed to CIC2 Right Channel 11: Reserved. Do not use.
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 0 / Register 113-114: Reserved Registers - 0x00 / 0x00 / 0x71-0x72 (B0_P0_R113-114)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 115: I2C Interface Miscellaneous Control - 0x00 / 0x00 / 0x73 (B0_P0_R115)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	I2C General Call Address Configuration 0: I2C General Call Address will be ignored 1: I2C General Call Address accepted
D4-D0	R	0 0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 116-119: Reserved Registers - 0x00 / 0x00 / 0x74-0x77 (B0_P0_R116-119)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Do not write.

Book 0 / Page 0 / Register 120: miniDSP Control Register access - 0x00 / 0x00 / 0x78 (B0_P0_R120)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: miniDSP does not have write access to control registers 1: miniDSP has write access to control registers
D6-D0	R/W	00 0000	Reserved. Write only default value

Book 0 / Page 0 / Register 121-126: Reserved Registers - 0x00 / 0x00 / 0x79-0x7E (B0_P0_R121-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Do not write

Book 0 / Page 0 / Register 127: Book Selection Register - 0x00 / 0x00 / 0x7F (B0_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.3 Book 0 Page 1

Book 0 / Page 1 / Register 0: Page Select Register - 0x00 / 0x01 / 0x00 (B0_P1_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

Book 0 / Page 1 / Register 1: Power Configuration Register - 0x00 / 0x01 / 0x01 (B0_P1_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R/W	1	0: Disable weak connection of AVDDx_18 with DVDD_18 1: AVDDx_18 is weakly connected to DVDD_18. Use when DVDD_18 is powered-up and AVDDx_18 is not externally powered-up.
D2	R/W	1	0: All the external analog supplies are available. 1: All the external analog supplies are not available.
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 2: Reserved Register - 0x00 / 0x01 / 0x02 (B0_P1_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 3: Left DAC PowerTune Configuration Register - 0x00 / 0x01 / 0x03 (B0_P1_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D2	R/W	0 00	Left DAC PTM Control 000: Left DAC in mode PTM_P3, PTM_P4 001: Left DAC in mode PTM_P2 010: Left DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 4: Right DAC PowerTune Configuration Register - 0x00 / 0x01 / 0x04 (B0_P1_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D2	R/W	0 00	Right DAC PTM Control 000: Right DAC in mode PTM_P3, PTM_P4 001: Right DAC in mode PTM_P2 010: Right DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 5-7: Reserved Registers - 0x00 / 0x01 / 0x05-0x07 (B0_P1_R5-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 8: Common Mode Register - 0x00 / 0x01 / 0x08 (B0_P1_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Soft-stepping of all the PGA are enabled for DAC channel. 1: Soft-stepping of all the PGA are disabled for DAC channel.
D6	R/W	0	0: Normal Mode 1: Soft-stepping time for all the PGA of DAC channel is doubled.
D5	R	0	Reserved. Write only reset values.
D4-D3	R/W	00	00: Output Common Mode for HP (valid only if the cap-coupled mode is enabled) Output Drivers = Input Common Mode 01: Output Common Mode for HP (valid only if the cap-coupled mode is enabled) Output Drivers = 1.25V 10: Output Common Mode for HP (valid only if the cap-coupled mode is enabled) Output Drivers = 1.5V 11: Output Common Mode for HP (valid only if the cap-coupled mode is enabled) Output Drivers = 1.65V
D2	R/W	0	0: Input Common Mode for full-chip (ADC and All Output Drivers except Receiver Output) = 0.9V 1: Input Common Mode for full-chip (ADC and All Output Drivers except Receiver Output) = 0.75V
D1-D0	R/W	00	00: Output Common Mode for REC Output Drivers = Input Common Mode 01: Output Common Mode for REC Output Drivers = 1.25V 10: Output Common Mode for REC Output Drivers = 1.5V 11: Output Common Mode for REC Output Drivers = 1.65V

Book 0 / Page 1 / Register 9: Headphone Output Driver Control - 0x00 / 0x01 / 0x09 (B0_P1_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D5	R/W	00	00: Headphone Driver Output Stage is 100%. 01: Headphone Driver Output Stage is 75%. 10: Headphone Driver Output Stage is 50%. 11: Headphone Driver Output Stage is 25%.
D4	R	1	Reserved. Write only reset values.
D3-D1	R/W	000	Debounce Programming for Glitch Rejection during Short Circuit Detection 000: 0us 001: 8us 010: 16us 011: 32us 100: 64us 101: 128us 110: 256us 111: 512us
D0	R/W	0	HPL and HPR Over Current Response Control 0: If Over Current Detected Limit the current delivered by HPL and HPR 1: If Over Current Detected Power-Down the HPL and HPR driver.

Book 0 / Page 1 / Register 10: Receiver Output Driver Control - 0x00 / 0x01 / 0x0A (B0_P1_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0001	Reserved. Write only reset values.

Book 0 / Page 1 / Register 10: Receiver Output Driver Control - 0x00 / 0x01 / 0x0A (B0_P1_R10) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D1	R/W	000	Debounce Programming for Glitch Rejection during Short Circuit Detection 000: 0us 001: 8us 010: 16us 011: 32us 100: 64us 101: 128us 110: 256us 111: 512us
D0	R/W	0	Receiver RECP and RECM Over-Current Response Control 0: If Over-Current Detected Limit the current. 1: If Over-Current Detected Power-Down the RECP and RECM driver

Book 0 / Page 1 / Register 11: Headphone Output Driver De-pop Control - 0x00 / 0x01 / 0x0B (B0_P1_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Headphone De-Pop Due to Input Offset Control (Note: Headphone depop control should only be used in unipolar configuration. This control should be disabled in Ground-Centered Headphone configuration.) 00: Disable 01: Enable (Duration = 50ms) 10: Enable (Duration = 100ms) 11: Enable (Duration = 200ms)
D5-D2	R/W	00 00	Headphone Output Driver De-Pop Control (Note: Headphone depop control should only be used in unipolar configuration. This control should be disabled in Ground-Centered Headphone configuration.) 0000: Disabled 0001: Enabled (Duration = 0.500*RC) 0010: Enabled (Duration = 0.625*RC) 0011: Enabled (Duration = 0.750*RC} 0100: Enabled (Duration = 0.875*RC) 0101: Enabled (Duration = 1.000*RC) 0110: Enabled (Duration = 2.000*RC) 0111: Enabled (Duration = 3.000*RC) 1000: Enabled (Duration = 4.000*RC) 1001: Enabled (Duration = 5.000*RC) 1010: Enabled (Duration = 6.000*RC) 1011: Enabled (Duration = 7.000*RC) 1100: Enabled (Duration = 8.000*RC) 1101: Enabled (Duration = 16.000*RC - do not use for Rchg=25K) 1110: Enabled (Duration = 24.000*RC - do not use for Rchg=25K) 1111: Enabled (Duration = 32.000*RC - do not use for Rchg=25K)
D1-D0	R/W	00	Headphone De-Pop Scheme Duration Based on RC Delay Control 00: Internal R = 25K typical and C is external cap.assumed to be 47uF 01: Internal R = 6K typical and C is external cap. assumed to be 47uF 10: Internal R = 2K typical and C is external cap. assumed to be 47uF 11: Reserved.

Book 0 / Page 1 / Register 12: Receiver Output Driver De-Pop Control - 0x00 / 0x01 / 0x0C (B0_P1_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Receiver De-Pop Due to Input Offset Control 00: Disable 01: Enable (Duration = 50ms) 10: Enable (Duration = 100ms) 11: Enable (Duration = 200ms)

Book 0 / Page 1 / Register 12: Receiver Output Driver De-Pop Control - 0x00 / 0x01 / 0x0C (B0_P1_R12) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D2	R/W	00 00	Receiver Output Driver De-Pop Control 0000: Disabled 0001: Enabled (Duration = 0.500*RC) 0010: Enabled (Duration = 0.625*RC) 0011: Enabled (Duration = 0.750*RC} 0100: Enabled (Duration = 0.875*RC) 0101: Enabled (Duration = 1.000*RC) 0110: Enabled (Duration = 2.000*RC) 0111: Enabled (Duration = 3.000*RC) 1000: Enabled (Duration = 4.000*RC) 1001: Enabled (Duration = 5.000*RC) 1010: Enabled (Duration = 6.000*RC) 1011: Enabled (Duration = 7.000*RC) 1100: Enabled (Duration = 8.000*RC) 1101: Enabled (Duration = 16.000*RC - do not use for Rchg=25K) 1110: Enabled (Duration = 24.000*RC - do not use for Rchg=25K) 1111: Enabled (Duration = 32.000*RC - do not use for Rchg=25K)
D1-D0	R/W	00	Receiver De-Pop Scheme Duration Based on RC Delay Control 00: Internal R = 25K typical and C is external cap.assumed to be 47uF 01: Internal R = 6K typical and C is external cap. assumed to be 47uF 10: Internal R = 2K typical and C is external cap. assumed to be 47uF 11: Reserved.

Book 0 / Page 1 / Register 13-16: Reserved Registers - 0x00 / 0x01 / 0x0D-0x10 (B0_P1_R13-16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 17: Mixer Amplifier Control - 0x00 / 0x01 / 0x11 (B0_P1_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN1L to Mixer Amplifier Left (MAL) Routing Control 0: IN1L input for high-impedance mode is not routed to MAL 1: IN1L input for high-impedance mode is routed to MAL
D4	R/W	0	IN1R to Mixer Amplifier Right (MAR) Routing Control 0: IN1R input for high-impedance mode is not routed to MAR 1: IN1R input for high-impedance mode is routed to MAR
D3	R/W	0	Mixer Amp Left (MAL) Power Control 0: MAL is powered down 1: MAL is powered up
D2	R/W	0	Mixer Amp Right (MAR) Power Control 0: MAR is powered down 1: MAR is powered up
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 18: Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control - 0x00 / 0x01 / 0x12 (B0_P1_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 18: Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control - 0x00 / 0x01 / 0x12 (B0_P1_R18) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1111	Left ADC PGA Output Routed to Left Mixer Amplifier (MAL) Volume Control: 00 0000: Volume Control = 0.0 dB 00 0001: Volume Control = -0.4 dB 00 0010: Volume Control = -0.9 dB 00 0011: Volume Control = -1.3 dB 00 0100: Volume Control = -1.8 dB 00 0101: Volume Control = -2.3 dB 00 0110: Volume Control = -2.9 dB 00 0111: Volume Control = -3.3 dB 00 1000: Volume Control = -3.9 dB 00 1001: Volume Control = -4.3 dB 00 1010: Volume Control = -4.8 dB 00 1011: Volume Control = -5.2 dB 00 1100: Volume Control = -5.8 dB 00 1101: Volume Control = -6.3 dB 00 1110: Volume Control = -6.6 dB 00 1111: Volume Control = -7.2 dB 01 0000: Volume Control = -7.8 dB 01 0001: Volume Control = -8.2 dB 01 0010: Volume Control = -8.5 dB 01 0011: Volume Control = -9.3 dB 01 0100: Volume Control = -9.7 dB 01 0101: Volume Control = -10.1 dB 01 0110: Volume Control = -10.6 dB 01 0111: Volume Control = -11.0 dB 01 1000: Volume Control = -11.5 dB 01 1001: Volume Control = -12.0 dB 01 1010: Volume Control = -12.6 dB 01 1011: Volume Control = -13.2 dB 01 1100: Volume Control = -13.8 dB 01 1101: Volume Control = -14.5 dB 01 1110: Volume Control = -15.3 dB 01 1111: Volume Control = -16.1 dB 10 0000: Volume Control = -17.0 dB 10 0001: Volume Control = -18.1 dB 10 0010: Volume Control = -19.2 dB 10 0011: Volume Control = -20.6 dB 10 0100: Volume Control = -22.1 dB 10 0101: Volume Control = -24.1 dB 10 0110: Volume Control = -26.6 dB 10 0111: Volume Control = -30.1 dB 10 1000: Volume Control = -36.1 dB 10 1001 - 11 1110: Reserved 11 1111: Left ADC PGA output is not routed to Left Mixer Amplifier (MAL)

Book 0 / Page 1 / Register 19: Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control - 0x00 / 0x01 / 0x13 (B0_P1_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Use the Right ADC PGA output routing setting to MAR as defined in this Register D5-D0 1: Use the Right ADC PGA output routing setting to MAR same as defined for Left ADC PGA in Page 1, Register 18, bits D5-D0 (previous register)
D6	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 19: Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control - 0x00 / 0x01 / 0x13 (B0_P1_R19) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1111	Right ADC PGA Output Routed to Right Mixer Amplifier Volume Control: 00 0000: Volume Control = 0.0 dB 00 0001: Volume Control = -0.4 dB 00 0010: Volume Control = -0.9 dB 00 0011: Volume Control = -1.3 dB 00 0100: Volume Control = -1.8 dB 00 0101: Volume Control = -2.3 dB 00 0110: Volume Control = -2.9 dB 00 0111: Volume Control = -3.3 dB 00 1000: Volume Control = -3.9 dB 00 1001: Volume Control = -4.3 dB 00 1010: Volume Control = -4.8 dB 00 1011: Volume Control = -5.2 dB 00 1100: Volume Control = -5.8 dB 00 1101: Volume Control = -6.3 dB 00 1110: Volume Control = -6.6 dB 00 1111: Volume Control = -7.2 dB 01 0000: Volume Control = -7.8 dB 01 0001: Volume Control = -8.2 dB 01 0010: Volume Control = -8.5 dB 01 0011: Volume Control = -9.3 dB 01 0100: Volume Control = -9.7 dB 01 0101: Volume Control = -10.1 dB 01 0110: Volume Control = -10.6 dB 01 0111: Volume Control = -11.0 dB 01 1000: Volume Control = -11.5 dB 01 1001: Volume Control = -12.0 dB 01 1010: Volume Control = -12.6 dB 01 1011: Volume Control = -13.2 dB 01 1100: Volume Control = -13.8 dB 01 1101: Volume Control = -14.5 dB 01 1110: Volume Control = -15.3 dB 01 1111: Volume Control = -16.1 dB 10 0000: Volume Control = -17.0 dB 10 0001: Volume Control = -18.1 dB 10 0010: Volume Control = -19.2 dB 10 0011: Volume Control = -20.6 dB 10 0100: Volume Control = -22.1 dB 10 0101: Volume Control = -24.1dB 10 0110: Volume Control = -26.6dB 10 0111: Volume Control = -30.1dB 10 1000: Volume Control = -36.1dB 10 1001 - 11 1110: Reserved 11 1111: Right ADC PGA output is not routed to Right Mixer Amplifer (MAR)

Book 0 / Page 1 / Register 20-21: Reserved Registers - 0x00 / 0x01 / 0x14-0x15 (B0_P1_R20-21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 22: Lineout Amplifier Control 1 - 0x00 / 0x01 / 0x16 (B0_P1_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC to LOL Driver Routing Control: 0: Left DAC is not routed to LOL driver. 1: Left DAC M-terminal is routed to LOL driver.
D6	R/W	0	Right DAC to LOR Driver Routing Control: 0: Right DAC is not routed to LOR driver. 1: Right DAC M-terminal is routed to LOR driver.

Book 0 / Page 1 / Register 22: Lineout Amplifier Control 1 - 0x00 / 0x01 / 0x16 (B0_P1_R22) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	Right DAC to LOL Driver Routing Control: 0: Right DAC is not routed to LOL driver. 1: Right DAC P-terminal is routed to LOL driver.(This is provided to support differential DAC output to LO and should be done only when B0_P1_R22_D6=1 and B0_P1_R27_D4=0)
D4-D3	R	0 0	Reserved. Write only reset values.
D2	R/W	0	LOL to LOR Driver Routing Control: 0: LOL output not routed to LOR driver. 1: LOL output routed to LOR driver.
D1	R/W	0	LOL Output Driver Power Control: 0: LOL output driver power-down 1: LOL output driver power-up
D0	R/W	0	LOR Output Driver Power Control: 0: LOR output driver power-down 1: LOR output driver power-up

Book 0 / Page 1 / Register 23: Lineout Amplifier Control 2 - 0x00 / 0x01 / 0x17 (B0_P1_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier to LOL Driver Routing Control: 0: MAL output is not routed to LOL driver. 1: MAL output is routed to LOL driver.
D6	R/W	0	Right Mixer Amplifier to LOR Driver Routing Control: 0: MAR output is not routed to LOR driver. 1: MAR output is routed to LOR driver.
D5	R	0	Reserved. Write only reset values.
D4-D3	R/W	0 0	IN1L Input to LOL Driver Routing and Gain Control: 00: IN1L input is not routed to LOL driver. 01: IN1L input is routed to LOL driver with gain = 0dB 10: IN1L input is routed to LOL driver with gain = -6dB 11: IN1L input is routed to LOL driver with gain = -12dB
D2	R	0	Reserved. Write only reset values.
D1-D0	R/W	00	IN1R Input to LOR Driver Routing and Gain Control: 00: IN1R input is not routed to LOR driver. 01: IN1R input is routed to LOR driver with gain = 0dB 10: IN1R input is routed to LOR driver with gain = -6dB 11: IN1R input is routed to LOR driver with gain = -12dB

Book 0 / Page 1 / Register 24-26: Reserved - 0x00 / 0x01 / 0x18-0x1A (B0_P1_R24-26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 27: Headphone Amplifier Control 1 - 0x00 / 0x01 / 0x1B (B0_P1_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier to HPL Driver Routing Control: 0: MAL output is not routed to HPL driver. 1: MAL output is routed to HPL driver.
D6	R/W	0	Right Mixer Amplifier to HPL Driver Routing Control: 0: MAR output is not routed to HPR driver. 1: MAR output is routed to HPR driver.
D5	R/W	0	Left DAC to HPL Driver Routing Control: 0: Left DAC is not routed to HPL driver. 1: Left DAC is routed to HPL driver.
D4	R/W	0	Right DAC to HPR Driver Routing Control: 0: Right DAC is not routed to HPR driver. 1: Right DAC is routed to HPR driver.

Book 0 / Page 1 / Register 27: Headphone Amplifier Control 1 - 0x00 / 0x01 / 0x1B (B0_P1_R27) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Left DAC to HPR Driver Routing Control: 0: Left DAC is not routed to HPR driver. 1: Left DAC M-terminal is routed to HPR driver. (This is provided to support differential DAC output for HP and should be done only when B0_P1_R27_D5=1 and B0_P1_R22_D7=0)
D1	R/W	0	HPL Output Driver Power Control: 0: HPL output driver is powered down 1: HPL output driver is powered up
D0	R/W	0	HPR Output Driver Power Control: 0: HPR output driver is powered down 1: HPR output driver is powered up

Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to HPL Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB

Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -33.1 dB 100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to HPL Driver (Default)

Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOR Output to HPR Driver Master Volume Control 0: LOL to HPL and LOR to HPR Volume are Independently Controlled 1: LOL to HPL and LOR to HPR Volume are Both Controlled by Page 1, Register 28, bits D6-D0

Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to HPR Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB

Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -33.1 dB 100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to HPR Driver (Default)

Book 0 / Page 1 / Register 30: Reserved Register - 0x00 / 0x01 / 0x1E (B0_P1_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 31: HPL Driver Volume Control - 0x00 / 0x01 / 0x1F (B0_P1_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Headphone Configuration: 0: Headphone driver is configured for unipolar or cap-coupled mode. 1: Headphone driver is configured for ground-centered mode. B0_P1_R8_D[4:3] should be set to "00".
D6	R	0	Reserved. Write only reset values.
D5-D0	R/W	11 1001	HPL Driver Gain Control: Do not change after HP amp power-up 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Output is Muted (Default) 11 1010: Gain = -6 dB 11 1011: Gain = -5 dB 11 1100: Gain = -4 dB 11 1101: Gain = -3 dB 11 1110: Gain = -2 dB 11 1111: Gain = -1 dB 00 0000: Gain = 0 dB 00 0001: Gain = 1 dB 00 0010: Gain = 2 dB 00 0011: Gain = 3 dB 00 0100: Gain = 4 dB 00 0101: Gain = 5 dB 00 0110: Gain = 6 dB 00 0111: Gain = 7 dB 00 1000: Gain = 8 dB 00 1001: Gain = 9 dB 00 1010: Gain = 10 dB 00 1011: Gain = 11 dB 00 1100: Gain = 12 dB 00 1101: Gain = 13 dB 00 1110: Gain = 14 dB 001111 - 111111: Reserved. Do not use.

Book 0 / Page 1 / Register 32: HPR Driver Volume Control - 0x00 / 0x01 / 0x20 (B0_P1_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Headphone Right (HPR) Driver Configuration: 0: Use the HPR driver volume setting as defined in B0_P1_R32_D[5:0]. (Only to be used in unipolar or cap-coupled configuration) 1: Use the HPR driver volume setting as defined as same as the HPL volume of B0_P1_R31_D[5:0].
D6	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 32: HPR Driver Volume Control - 0x00 / 0x01 / 0x20 (B0_P1_R32) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1001	HPR Driver Volume Control (Only used in Unipolar o rCap-Coupled Configuration): 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB 00 0011: Volume Control = 3 dB 00 0100: Volume Control = 4 dB 00 0101: Volume Control = 5 dB 00 0110: Volume Control = 6 dB 00 0111: Volume Control = 7 dB 00 1000: Volume Control = 8 dB 00 1001: Volume Control = 9 dB 00 1010: Volume Control = 10 dB 00 1011: Volume Control = 11 dB 00 1100: Volume Control = 12 dB 00 1101: Volume Control = 13 dB 00 1110: Volume Control = 14 dB 001111 - 111111: Reserved. Do not use.

Book 0 / Page 1 / Register 33: Reserved Register - 0x00 / 0x01 / 0x21 (B0_P1_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0010 1000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 34: Reserved Register - 0x00 / 0x01 / 0x22 (B0_P1_R34)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0011 1110	Reserved. Write only reset values.

Book 0 / Page 1 / Register 35: Ground Centered Headphone Offset Correction Control - 0x00 / 0x01 / 0x23 (B0_P1_R35)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	Ground Centered Headphone Offset Calibration 0: For ground-centered headphone amplifier, offset correction happens only for first power-up of amplifier after hardware reset 1: For ground-centered headphone amplifier, offset correction happens at every power-up of headphone amplifier
D4-D0	R	1 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to RECP Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to RECP Driver (Default)

Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOR Output to RECM Driver Master Volume Control 0: LOL to RECP and LOR to RECM Volume are Independently Controlled 1: LOL to RECP and LOR to RECM Volume are Both Controlled by B0_P1_R36_D[6:0]. Should only be used when load of receiver amplifier is differential.

Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to RECM Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to RECM Driver (Default)

Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	IN1L Input Routed to RECP Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: IN1L Input Not Routed to RECP Driver (Default)

Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Input to RECP and IN1R Input to RECM Driver Master Volume Control 0: IN1L to RECP and IN1R to RECM Volume are Independently Controlled 1: IN1L to RECP and INI1R to RECM Volume are Both Controlled by B0_P1_R38_D[6:0]. Should only be used when load of receiver amplifier is differential.

Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	IN1R Input Routed to RECM Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: IN1R Input Not Routed to RECM Driver (Default)

Book 0 / Page 1 / Register 40: Receiver Amplifier Control 5 - 0x00 / 0x01 / 0x28 (B0_P1_R40)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	RECP Output Driver Power Control 0: RECP Output Driver Power-Down 1: RECP Output Driver Power-Up
D6	R/W	0	RECM Output Driver Power Control 0: RECM Output Driver Power-Down 1: RECM Output Driver Power-Up

Book 0 / Page 1 / Register 40: Receiver Amplifier Control 5 - 0x00 / 0x01 / 0x28 (B0_P1_R40) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1001	RECP Driver Volume Control: 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB ... 01 1100: Volume Control = 28 dB 01 1101: Volume Control = 29 dB

Book 0 / Page 1 / Register 41: Receiver Amplifier Control 6 - 0x00 / 0x01 / 0x29 (B0_P1_R41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Receiver Master Volume Control 0: RECP and RECM Volume are Independently Controlled 1: RECP and RECM Volume are Both Controlled by B0_P1_R40_D[5:0]. Should only be used when load of receiver amplifier is differential.
D6	R	0	Reserved. Write only reset values.
D5-D0	R/W	11 1001	RECM Driver Volume Control: 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB ... 01 1100: Volume Control = 28 dB 01 1101: Volume Control = 29 dB

Book 0 / Page 1 / Register 42: Receiver Amplifier Control 7 - 0x00 / 0x01 / 0x2A (B0_P1_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Receiver Amplifier Offset Calibration Flag 0: Offset Calibration is Not Done 1: Offset Calibration is Done
D6	R/W	0	Left DAC Routing to RECP: 0: Left DAC is not routed to RECP 1: Left DAC P-terminal is routed to RECP
D5	R/W	0	Left DAC Routing to RECM: 0: Left DAC is not routed to RECM 1: Left DAC M-terminal is routed to RECM
D4-D3	R/W	0 1	Receiver Amplifier Offset Calibration Control 00: Offset calibration is disabled 01: Force calibrate for offset at receiver amp power-up for routings selected (Default) 10: Calibrate for offset at receiver amp power-up for selected routings only for the first-power-up of receiver amp. 11: Reserved
D2-D0	R/W	000	Reserved. Write only default value.

Book 0 / Page 1 / Register 43-44: Reserved Registers - 0x00 / 0x01 / 0x2B-0x2C (B0_P1_R43-44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 45: Speaker Amplifier Control 1 - 0x00 / 0x01 / 0x2D (B0_P1_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier (MAL) to Speaker Driver (SPK) Routing Control: 0: MAL output is not routed to SPK driver. 1: MAL output is routed to SPK driver.
D6	R/W	0	Right Mixer Amplifier (MAR) to Speaker Driver (SPK_RIGHT_CH_IN) Routing Control: 0: MAR output is not routed to SPK_RIGHT_CH_IN. 1: MAR output is routed to SPK_RIGHT_CH_IN.
D5-D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Mono Speaker Control: 0: SPK_RIGHT_CH_IN is not routed to Speaker Driver (SPK). 1: SPK_RIGHT_CH_IN is routed to Speaker Driver (SPK).
D1	R/W	0	Speaker Driver Power Control: 0: SPK Driver Power-Down 1: SPK Driver Power-Up
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to SPK Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to SPK Driver (Default)

Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOL Output to SPK and LOR Output to SPK_RIGHT_CH_IN Master Volume Control 0: LOL Output to SPK and LOR Output to SPK_RIGHT_CH_IN Volume are Independently Controlled 1: LOL Output to SPK and LOR Output to SPK_RIGHT_CH_IN Volume are Both Controlled by B0_P1_R46_D[6:0]

Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to SPK_RIGHT_CH_IN Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to SPK_RIGHT_CH_IN (Default)

Book 0 / Page 1 / Register 48: Speaker Amplifier Volume Controls - 0x00 / 0x01 / 0x30 (B0_P1_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0000	Speaker Amplifier (SPK) Volume Control: 000 0000: SPK Driver is Muted (Default) 001 0001: SPK Driver Volume = 6 dB 010 0001: SPK Driver Volume = 12 dB 011 0001: SPK Driver Volume = 18 dB 100 0001: SPK Driver Volume = 24 dB 101 0001: SPK Driver Volume = 30 dB Others: Reserved. Do not use.

Book 0 / Page 1 / Register 49-50: Reserved Registers - 0x00 / 0x01 / 0x31-0x32 (B0_P1_R49-50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 51: Microphone Bias Control - 0x00 / 0x01 / 0x33 (B0_P1_R51)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	External Mic Bias Power Control 0: MICBIAS_EXT Powered Down if Jack is not inserted. 1: MICBIAS_EXT Powered On and Off based only on P1_R51_D6, even if Jack is not inserted.
D6-D4	R/W	000	External Mic Bias Power and Voltage Control 000: MICBIAS_EXT is powered down with pull-down enabled 001: MICBIAS_EXT is powered down with tristate (this should only be used if external microphone bias is driven from external source 010: MICBIAS_EXT powered on with MICBIAS_EXT = 1.50 V (if Input Common Mode = 0.75 V) or 1.80 V (if Input Common Mode = 0.9 V). 011: MICBIAS_EXT powered on with MICBIAS_EXT = 1.67 V (if Input Common Mode = 0.75 V) or 2.00 V (if Input Common Mode = 0.9 V). 100-101: Do not use. 110: MICBIAS_EXT powered on with MICBIAS_EXT = 2.37 V (if Input Common Mode = 0.75 V) or 2.85 V (if Input Common Mode = 0.9 V). 111: MICBIAS_EXT powered on with MICBIAS_EXT = 2.50 V (if Input Common Mode = 0.75 V) or 3.00 V (if Input Common Mode = 0.9 V).
D3	R/W	0	0: MICBIAS_EXT is not powered up upon insertion if microphone is not detected on inserted jack 1: MICBIAS_EXT is powered up upon jack detect irrespective of whether microphone is detected or not
D2-D0	R/W	000	Mic Bias Power and Voltage Control 000: MICBIAS is powered down with pull-down enabled 001: MICBIAS is powered down with tristate (this should only be used if microphone bias is driven from external source) 010: MICBIAS powered on with MICBIAS = 1.50 V (if Input Common Mode = 0.75 V) or 1.80 V (if Input Common Mode = 0.9 V). 011: MICBIAS powered on with MICBIAS = 1.67 V (if Input Common Mode = 0.75 V) or 2.00 V (if Input Common Mode = 0.9 V). 100-101: Do not use. 110: MICBIAS powered on with MICBIAS = 2.37 V (if Input Common Mode = 0.75 V) or 2.85 V (if Input Common Mode = 0.9 V). 111: MICBIAS powered on with MICBIAS = 2.50 V (if Input Common Mode = 0.75 V) or 3.00 V (if Input Common Mode = 0.9 V).

Book 0 / Page 1 / Register 52: Input Select 1 for Left Microphone PGA P-Terminal - 0x00 / 0x01 / 0x34 (B0_P1_R52)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	IN1L to Left Mic PGA (P-Terminal) Selection Control 00: IN1L Not Selected 01: IN1L Selected (RIN = 10K) 10: IN1L Selected (RIN = 20K) 11: IN1L Selected (RIN = 40K)
D5-D4	R/W	00	IN2L to Left Mic PGA (P-Terminal) Selection Control 00: IN2L Not Selected 01: IN2L Selected (RIN = 10K) 10: IN2L Selected (RIN = 20K) 11: IN2L Selected (RIN = 40K)
D3-D2	R/W	00	IN3L to Left Mic PGA (P-Terminal) Selection Control 00: IN3L Not Selected 01: IN3L Selected (RIN = 10K) 10: IN3L Selected (RIN = 20K) 11: IN3L Selected (RIN = 40K)

Book 0 / Page 1 / Register 52: Input Select 1 for Left Microphone PGA P-Terminal - 0x00 / 0x01 / 0x34 (B0_P1_R52) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1-D0	R/W	00	IN1R to Left Mic PGA (P-Terminal) Selection Control 00: IN1R Not Selected 01: IN1R Selected (RIN = 10K) 10: IN1R Selected (RIN = 20K) 11: IN1R Selected (RIN = 40K) NOTE (For All Inputs to PGA): PGA Value = 0 dB for Singled Ended Input with RIN = 10K PGA Value = +6 dB for Differential Input with RIN = 10K PGA Value = -6 dB for Singled Ended Input with RIN = 20K PGA Value = 0 dB for Differential Input with RIN = 20K PGA Value = -12 dB for Singled Ended Input with RIN = 40K PGA Value = -6 dB for Differential Input with RIN = 40K

Book 0 / Page 1 / Register 53: Input Select 2 for Left Microphone PGA P-Terminal - 0x00 / 0x01 / 0x35 (B0_P1_R53)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN4L to Left Mic PGA (P-Terminal) Selection Control 00: IN4L Not Selected 01: IN4L Selected (RIN = 20K)
D4	R/W	0	IN4R to Left Mic PGA (M-Terminal) Selection Control 00: IN4R Not Selected 01: IN4R Selected (RIN = 20K)
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 54: Input Select for Left Microphone PGA M-Terminal - 0x00 / 0x01 / 0x36 (B0_P1_R54)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Internal Common Mode (CM1) to Left Mic PGA (M-Terminal) Selection Control 00: CM1 Not Selected 01: CM1 Selected (RIN = 10K) 10: CM1 Selected (RIN = 20K) 11: CM1 Selected (RIN = 40K)
D5-D4	R/W	00	IN2R to Left Mic PGA (M-Terminal) Selection Control 00: IN2R Not Selected 01: IN2R Selected (RIN = 10K) 10: IN2R Selected (RIN = 20K) 11: IN2R Selected (RIN = 40K)
D3-D2	R/W	00	IN3R to Left Mic PGA (M-Terminal) Selection Control 00: IN3R Not Selected 01: IN3R Selected (RIN = 10K) 10: IN3R Selected (RIN = 20K) 11: IN3R Selected (RIN = 40K)
D1-D0	R/W	00	Internal Common Mode (CM2) to Left Mic PGA (M-Terminal) Selection Control 00: CM2 Not Selected 01: CM2 Selected (RIN = 10K) 10: CM2 Selected (RIN = 20K) 11: CM2 Selected (RIN = 40K)

Book 0 / Page 1 / Register 55: Input Select 1 for Right Microphone PGA P-Terminal - 0x00 / 0x01 / 0x37 (B0_P1_R55)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	IN1R to Right Mic PGA (P-Terminal) Selection Control 00: IN1R Not Selected 01: IN1R Selected (RIN = 10K) 10: IN1R Selected (RIN = 20K) 11: IN1R Selected (RIN = 40K)
D5-D4	R/W	00	IN2R to Right Mic PGA (P-Terminal) Selection Control 00: IN2R Not Selected 01: IN2R Selected (RIN = 10K) 10: IN2R Selected (RIN = 20K) 11: IN2R Selected (RIN = 40K)
D3-D2	R/W	00	IN3R to Right Mic PGA (P-Terminal) Selection Control 00: IN3R Not Selected 01: IN3R Selected (RIN = 10K) 10: IN3R Selected (RIN = 20K) 11: IN3R Selected (RIN = 40K)
D1-D0	R/W	00	IN2L to Right Mic PGA (P-Terminal) Selection Control 00: IN2L Not Selected 01: IN2L Selected (RIN = 10K) 10: IN2L Selected (RIN = 20K) 11: IN2L Selected (RIN = 40K)

Book 0 / Page 1 / Register 56: Input Select 2 for Right Microphone PGA P-Terminal - 0x00 / 0x01 / 0x38 (B0_P1_R56)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN4R to Right Mic PGA (P-Terminal) Selection Control 00: IN4R Not Selected 01: IN4R Selected (RIN = 20K)
D4	R/W	0	IN4L to Right Mic PGA (M-Terminal) Selection Control 00: IN4L Not Selected 01: IN4L Selected (RIN = 20K)
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 57: Input Select for Right Microphone PGA M-Terminal - 0x00 / 0x01 / 0x39 (B0_P1_R57)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Internal Common Mode (CM1) to Right Mic PGA (M-Terminal) Selection Control 00: CM1 Not Selected 01: CM1 Selected (RIN = 10K) 10: CM1 Selected (RIN = 20K) 11: CM1 Selected (RIN = 40K)
D5-D4	R/W	00	IN1L to Right Mic PGA (M-Terminal) Selection Control 00: IN1L Not Selected 01: IN1L Selected (RIN = 10K) 10: IN1L Selected (RIN = 20K) 11: IN1L Selected (RIN = 40K)
D3-D2	R/W	00	IN3L to Right Mic PGA (M-Terminal) Selection Control 00: IN3L Not Selected 01: IN3L Selected (RIN = 10K) 10: IN3L Selected (RIN = 20K) 11: IN3L Selected (RIN = 40K)
D1-D0	R/W	00	Internal Common Mode (CM2) to Right Mic PGA (M-Terminal) Selection Control 00: CM2 Not Selected 01: CM2 Selected (RIN = 10K) 10: CM2 Selected (RIN = 20K) 11: CM2 Selected (RIN = 40K)

Book 0 / Page 1 / Register 58: Input Common Mode Control - 0x00 / 0x01 / 0x3A (B0_P1_R58)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D6	R/W	0	IN1R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D5	R/W	0	IN2L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D4	R/W	0	IN2R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D3	R/W	0	IN3L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D2	R/W	0	IN3R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D1	R/W	0	IN4L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D0	R/W	0	IN4R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode

Book 0 / Page 1 / Register 59: Left Microphone PGA Control - 0x00 / 0x01 / 0x3B (B0_P1_R59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Left MICPGA Gain is enabled 1: Left MICPGA Gain is set to 0dB
D6-D0	R/W	000 0000	Left MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB ... 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use.

Book 0 / Page 1 / Register 60: Right Microphone PGA Control - 0x00 / 0x01 / 0x3C (B0_P1_R60)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Right MICPGA Gain is enabled 1: Right MICPGA Gain is set to 0dB
D6-D0	R/W	000 0000	Right MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB ... 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use.

Book 0 / Page 1 / Register 61: ADC PowerTune Configuration Register - 0x00 / 0x01 / 0x3D (B0_P1_R61)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: PTM_R4 (Default) 01: PTM_R3 10: PTM_R2 11: PTM_R1
D5-D0	R/W	00 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 62: ADC Analog PGA Gain Flag Register - 0x00 / 0x01 / 0x3E (B0_P1_R62)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1	R	0	Left Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D0	R	0	Right Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume

Book 0 / Page 1 / Register 63: DAC Analog Gain Flags Register 1 - 0x00 / 0x01 / 0x3F (B0_P1_R63)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	HPR Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	RECP Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	RECM Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 64: DAC Analog Gain Flags Register 2 - 0x00 / 0x01 / 0x40 (B0_P1_R64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	LOL to HPL Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	LOR to HPR Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	LOL to RECP Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	LOR to RECM Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3	R	0	LOL to SPK Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D2	R	0	Reserved. Write only reset values.
D1	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 64: DAC Analog Gain Flags Register 2 - 0x00 / 0x01 / 0x40 (B0_P1_R64) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	0: Charge Pump is not Powered-Up 1: Charge Pump is Powered-Up

Book 0 / Page 1 / Register 65: Analog Bypass Gain Flags Register - 0x00 / 0x01 / 0x41 (B0_P1_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	IN1L to Receiver Left (RECP) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	IN1R to RECM Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	Left ADC PGA to Mixer Amp Left (MAL) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	Right ADC PGA to Mixer Amp Right (MAR) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 66: Driver Power-Up Flags Register - 0x00 / 0x01 / 0x42 (B0_P1_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Line Out Left Driver (LOL) Power-Up Flag 0: LOL Driver Powered Down 1: LOL Driver Powered Up
D6	R	0	Line Out Right Driver (LOR) Power-Up Flag 0: LOR Driver Powered Down 1: LOR Driver Powered Up
D5	R	0	Headphone Left Driver (HPL) Power-Up Flag 0: HPL Driver Powered Down 1: HPL Driver Powered Up
D4	R	0	Headphone Right Driver (HPR) Power-Up Flag 0: HPR Driver Powered Down 1: HPR Driver Powered Up
D3	R	0	Receiver Left Driver (RECP) Power-Up Flag 0: RECP Driver Powered Down 1: RECP Driver Powered Up
D2	R	0	Receiver Right Driver (RECM) Power-Up Flag 0: RECM Driver Powered Down 1: RECM Driver Powered Up
D1	R	0	Speaker Left Driver (SPK) Power-Up Flag 0: SPK Driver Powered Down 1: SPK Driver Powered Up
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 67-68: Reserved Registers - 0x00 / 0x01 / 0x43-0x44 (B0_P1_R67-68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 69: Over current Flags - 0x00 / 0x01 / 0x45 (B0_P1_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Receiver Driver Over Current Sticky Flag 0: No over current was detected on Receiver driver 1: Over Current was detected on Receiver driver
D6	R	0	Headphone Driver Over Current Sticky Flag 0: No over current was detected on Receiver driver 1: Over Current was detected on Receiver driver
D5	R	0	Speaker Driver Over Current Sticky Flag 0: No over current was detected on Speaker driver 1: Over Current was detected on Speaker driver
D4-D0	R	x xxxx	Reserved.

Book 0 / Page 1 / Register 67-76: Reserved Registers - 0x00 / 0x01 / 0x43-0x4C (B0_P1_R67-76)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 77: Reserved Registers - 0x00 / 0x01 / 0x4D (B0_P1_R77)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R	000 0000	Reserved. Write only reset values.
D0	R/W	0	Headphone Over Current Protection Enable 0: Default 1: Write '1' to enable headphone overcurrent protection

Book 0 / Page 1 / Register 78-118: Reserved Registers - 0x00 / 0x01 / 0x4E-0x76 (B0_P1_R78-118)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 1 / Register 119: Headset Detection Tuning Register 1 - 0x00 / 0x01 / 0x77 (B0_P1_R119)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	10	Headphone Load Detection Pulse Period. Detection pulse is used to identify the headphone load type after insertion is detected. 0: Detector pulse mode is disabled 1: Detector pulse mode period is enabled with period of 144 cycles of LF_OSC_CLK (typ. 18us) 2: Detector pulse mode period is enabled with period of 288 cycles of LF_OSC_CLK (default, typ. 36us) 3: Detector pulse mode period is enabled with period of 4608 cycles of LF_OSC_CLK (typ. 576us)
D5-D2	R/W	01 01	Headphone Load Detection Pulse High Duration. Detection pulse is used to identify the headphone load type after insertion is detected. 0000: Reserved. 0001: Detector pulse high duration is 1*Detector Pulse High Width Scale Factor*LF_OSC_CLK. See bit D1 for Detector Pulse High Width Scale Factor. 0010: Detector pulse high duration is 2*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0011: Detector pulse high duration is 3*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0100: Detector pulse high duration is 4*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0101: Detector pulse high duration is 5*Detector Pulse High Width Scale Factor*LF_OSC_CLK. (default) ... 1110: Detector pulse high duration is 14*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 1111: Detector pulse high duration is 15*Detector Pulse High Width Scale Factor*LF_OSC_CLK.
D1	R/W	0	Headphone Load Detection Pulse High Width Scale Factor 0: Headphone Load Detection Pulse High Width Scale Factor =1 1: Headphone Load Detection Pulse High Width Scale Factor =8

Book 0 / Page 1 / Register 119: Headset Detection Tuning Register 1 - 0x00 / 0x01 / 0x77 (B0_P1_R119) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	Headset Detection Pulse Auto configuration 0: Upon microphone insertion detection, the auto configuration of detection is enabled. This enables the detector pulse mode with period of 4608 cycles of the LF_OSC_CLK, and sets Detector Pulse High Width Scale Factor to 8. (default) 1: Upon microphone insertion detection, the auto configuration of detection is disabled. Therefor, detector pulse mode period and Detector Pulse High Width Scale Factor does not change upon insertion.

Book 0 / Page 1 / Register 120: Headset Detection Tuning Register 2 - 0x00 / 0x01 / 0x78 (B0_P1_R120)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0100	Headset Detection Pulse Width control. This pulse is used to detect button press and headset removal. 0000: Headset Detection Pulse Width is 1*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK, where Headphone Load Detector_Pulse_Period is set by B0_P1_R119_D[7:6]. 0001: Headset Detection Pulse Width is 1.5*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0010: Headset Detection Pulse Width is 2*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0011: Headset Detection Pulse Width is 2.5*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0100: Headset Detection Pulse Width is 3*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. (default) ... 1110: Headset Detection Pulse Width is 8*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 1111: Headset Detection Pulse Width is 8.5*(Headphone Load Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK.
D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Headphone Load Detection Range control 0: Headphone detection supported in the range of 16-Ohms to 300-Ohms. 1: Headphone detection supported in the range of 16-Ohms to 64-Ohms.
D1-D0	R/W	10	Headset Detection using microphone inputs on IN4L, IN4R control: 00: Reserved. Do not use. 01: IN4L, IN4R enabled for headset microphone inputs. 10: IN4L, IN4R disabled for headset microphone inputs. 11: Reserved. Do not use.

Book 0 / Page 1 / Register 121: Reserved Register - 0x00 / 0x01 / 0x79 (B0_P1_R121)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0011 0011	Reserved. Write only reset values.

Book 0 / Page 1 / Register 122: Reference Powerup Control - 0x00 / 0x01 / 0x7A (B0_P1_R122)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0 0000	Reserved. Write only reset values.
D2	R/W	0	0: Chip-Reference powered-up and powered-down internally based on other on-chip block requirements 1: Chip-Reference will be force-fully powered-up
D1-D0	R/W	01	Reserved. Write only reset values.

Book 0 / Page 1 / Register 123-127: Reserved Registers - 0x00 / 0x01 / 0x7B-0x7F (B0_P1_R123-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

8.6.4 Book 0 Page 3

Book 0 / Page 3 / Register 0: Page Select Register - 0x00 / 0x03 / 0x00 (B0_P3_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

Book 0 / Page 3 / Register 1: Reserved Register - 0x00 / 0x03 / 0x01 (B0_P3_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 2: Primary SAR ADC Control - 0x00 / 0x03 / 0x02 (B0_P3_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Normal Mode 1: Stop Conversion and power down SAR ADC
D6-D5	R/W	00	00: SAR ADC resolution = 12-bit 01: SAR ADC resolution = 8-bit 10: SAR ADC resolution = 10-bit 11: SAR ADC resolution = 12-bit
D4-D3	R/W	1 1	00: SAR ADC clock divider = 1 (Use for 8-bit resolution case only) 01: SAR ADC clock divider = 2 (Use for 8-bit/10-bit resolution case only) 10: SAR ADC clock divider = 4 (For better performance in 8-bit/10-bit resolution mode, this setting is recommended) 11: SAR ADC clock divider = 8 (For better performance in 12-bit resolution mode, this setting is recommended)
D2	R/W	0	0: Mean filter is used for on-chip data averaging (if enabled) 1: Median filter is used for on-chip data averaging (if enabled)
D1-D0	R/W	00	00: On-chip data averaging is disabled. 01: 4-data averaging in case mean filter / 5-data averaging in case of median filter. 10: 8-data averaging in case mean filter / 9-data averaging in case of median filter. 11: 16-data averaging in case mean filter / 15-data averaging in case of median filter.

Book 0 / Page 3 / Register 3: Primary SAR ADC Conversion Mode - 0x00 / 0x03 / 0x03 (B0_P3_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D2	R/W	00 00	Conversion Mode 0000: No Scan 0001 - 0101: Reserved. Do not use. 0110: VBAT Measurement 0111: IN1R Measurement 1000: IN1L Measurment 1001: Auto Scan. Sequence used is IN1L, IN1R, VBAT, TEMP1(or TEMP2). Each of these input can be enabled or disabled independently using register-19 and with that sequence will get modified accordingly. Scan continues until stop bit(D7 of reg-2) is sent or D5-D2 of this register is changed. 1010: TEMP1 Measurement 1011: PortScan : IN1L, IN1R, VBAT 1100: TEMP2 Measurement 1101 - 1111: Reserved. Do not use.
D1-D0	R/W	00	00: Interrupt Disabled 01: Interrupt = Data-Available (active LOW) 10-11: Reserved. Do not use.

Book 0 / Page 3 / Register 4-5: Reserved Registers - 0x00 / 0x03 / 0x04-0x05 (B0_P3_R4-5)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	x000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 6: SAR Reference Control - 0x00 / 0x03 / 0x06 (B0_P3_R6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	SAR Reference Selection 0: Use External Reference for SAR Measurement 1: Use Internal Reference (1.25V) for SAR Measurement
D6	R	0	Reserved. Write only reset values.
D5	R/W	1	SAR Internal Reference Power Options 0: Internal Reference powered forever for conversions 1: Internal Reference powered up or powered down automatically based on whether conversions are going on or not.
D4	R	0	Reserved. Write only reset values.
D3-D2	R/W	10	SAR Reference Stabilization Time Before Conversion 00: 0 ms 01: 1 ms 10: 4 ms 11: 8 ms
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 3 / Register 7-8: Reserved Registers - 0x00 / 0x03 / 0x07-0x08 (B0_P3_R7-8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 9: SAR ADC Flags Register 1 - 0x00 / 0x03 / 0x09 (B0_P3_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R	1	SAR Busy Flag 0: SAR ADC is Busy 1: SAR ADC is not Busy
D5	R	0	SAR Data Available Flag 0: No New Data Available 1: New Data is Available
D4-D0	R	0 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 10: SAR ADC Flags Register 2 - 0x00 / 0x03 / 0x0A (B0_P3_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	IN1L Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D6	R	0	IN1R Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D5	R	0	VBAT Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D4-D2	R	000	Reserved. Write only reset values.
D1	R	0	TEMP1 Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D0	R	0	TEMP2 Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)

Book 0 / Page 3 / Register 11-12: Reserved Registers - 0x00 / 0x03 / 0x0B-0x0C (B0_P3_R11-12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 13: SAR ADC Buffer Mode Control - 0x00 / 0x03 / 0x0D (B0_P3_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Buffer Mode Enable Select 0: Buffer mode is disabled and RDPTR, WRPTR and TGPTR are set to their default value. 1: Buffer mode is enabled.
D6	R/W	0	Buffer Conversion Mode Select 0: Buffer mode is enabled as continuous conversion mode. 1: Buffer mode is enabled as single shot mode.
D5-D3	R/W	00 0	Buffer Mode Conversion Trigger Level Select 000: Trigger Level for conversion = 8 converted data values 001: Trigger Level for conversion = 16 converted data values 010: Trigger Level for conversion = 24 converted data values 011: Trigger Level for conversion = 32 converted data values 100: Trigger Level for conversion = 40 converted data values 101: Trigger Level for conversion = 48 converted data values 110: Trigger Level for conversion = 56 converted data values 111: Trigger Level for conversion = 64 converted data values
D2	R	0	Reserved. Write only reset values.
D1	R	0	Buffer Full Flag 0: Buffer is not full 1: Buffer is full (buffer contains 64 unread converted data).
D0	R	1	Buffer Empty Flag 0: Buffer is not empty 1: Buffer is empty (there is no unread converted data in the buffer).

Book 0 / Page 3 / Register 14: Reserved Register - 0x00 / 0x03 / 0x0E (B0_P3_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 15: Scan Mode Timer Control - 0x00 / 0x03 / 0x0F (B0_P3_R15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0100	Reserved. Write only reset values.
D3	R/W	0	Programmable Delay for SAR Auto-Scan Enable 0: Disabled 1: Enabled
D2-D0	R/W	000	Programmable Interval Timer for Auto Scan delay 000: Delay = 1.12 min. 001: Delay = 3.36 min. 010: Delay = 5.59 min. 011: Delay = 7.83 min. 100: Delay = 10.01 min. 101: Delay = 12.30 min. 110: Delay = 14.54 min. 111: Delay = 16.78 min. (Note: Based on an 8 MHz Internal Oscillator or MCLK/DIV(Page-0, Reg-23) = 1MHz)

Book 0 / Page 3 / Register 16: Reserved Register - 0x00 / 0x03 / 0x10 (B0_P3_R16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 17: SAR ADC Clock Control - 0x00 / 0x03 / 0x11 (B0_P3_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	SAR ADC Clock Selection 0: Internal Oscillator 1: External MCLK
D6-D0	R/W	000 0001	MCLK to SAR ADC Clock Divider Selection 000 0000: MCLK Divider = 128 000 0001: MCLK Divider = 1 000 0010: MCLK Divider = 2 … 111 1110: MCLK Divider = 126 111 1111: MCLK Divider = 127

Book 0 / Page 3 / Register 18: SAR ADC Buffer Mode Data Read Control - 0x00 / 0x03 / 0x12 (B0_P3_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: SPI Interface is used for the SAR or Buffer data reading. 1: I2C Interface is used for the SAR or Buffer data reading.
D6	R/W	0	0: SAR data update is automatically halted (to avoid simultaneous buffer read and write operations) based on internal detection logic. Valid only for SPI interface. 1: SAR data update is held using software control (P3_R18_D5).
D5	R/W	0	0: SAR data update is enabled all the time (valid only if P3_R18_D6 = 1) 1: SAR data update is stopped so that user can read the last updated data without any data corruption (valid only if P3_R18_D6 = 1).
D4-D0	R	0 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 19: SAR ADC Measurement Control - 0x00 / 0x03 / 0x13 (B0_P3_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Automatic IN1L Measurement Enable 0: Disable 1: Enable
D6	R/W	0	Automatic IN1R Measurement Enable 0: Disable 1: Enable
D5	R/W	0	Automatic VBAT Measurement Enable 0: Disable 1: Enable
D4	R/W	0	Automatic TEMP Measurement Enable 0: Disable 1: Enable
D3	R/W	0	Automatic TEMP Measurement Sensor Selection 0: TEMP1 1: TEMP2
D2	R/W	0	IN1L Measurement Type Selection 0: Voltage Measurement 1: Resistance Measurement
D1	R/W	0	IN1R Measurement Type Selection 0: Voltage Measurement 1: Resistance Measurement
D0	R/W	0	Resistance Measurement Mode Selection 0: Internal Bias Resistance Measurment Mode 1: External Bias Resistance Measurment Mode

Book 0 / Page 3 / Register 20: Reserved Register - 0x00 / 0x03 / 0x14 (B0_P3_R20)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 21: SAR ADC Measurement Threshold Flags - 0x00 / 0x03 / 0x15 (B0_P3_R21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R	0	IN1L Measurement Max Threshold Flag 0: IN1L Measurement < Programmed Max Threshold Setting 1: IN1L Measurement >= Programmed Max Threshold Setting
D4	R	0	IN1L Measurement Min Threshold Flag 0: IN1L Measurement > Programmed Min Threshold Setting 1: IN1L Measurement <= Programmed Min Threshold Setting
D3	R	0	IN1R Measurement Max Threshold Flag 0: IN1R Measurement < Programmed Max Threshold Setting 1: IN1R Measurement >= Programmed Max Threshold Setting
D2	R	0	IN1R Measurement Min Threshold Flag 0: IN1R Measurement > Programmed Min Threshold Setting 1: IN1R Measurement <= Programmed Min Threshold Setting
D1	R	0	TEMP (TEMP1 or TEMP2) Measurement Max Threshold Flag 0: TEMP Measurement < Programmed Max Threshold Setting 1: TEMP Measurement >= Programmed Max Threshold Setting
D0	R	0	3

Book 0 / Page 3 / Register 22: IN1L Max Threshold Check Control 1 - 0x00 / 0x03 / 0x16 (B0_P3_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1L Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1L Max Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 23: IN1L Max Threshold Check Control 2 - 0x00 / 0x03 / 0x17 (B0_P3_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1L Max Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 24: IN1L Min Threshold Check Control 1 - 0x00 / 0x03 / 0x18 (B0_P3_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1L Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1L Min Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 25: IN1L Min Threshold Check Control 2 - 0x00 / 0x03 / 0x19 (B0_P3_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1L Min Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 26: IN1R Max Threshold Check Control 1 - 0x00 / 0x03 / 0x1A (B0_P3_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1R Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1R Max Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 27: IN1R Max Threshold Check Control 2 - 0x00 / 0x03 / 0x1B (B0_P3_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1R Max Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 28: IN1R Min Threshold Check Control 1 - 0x00 / 0x03 / 0x1C (B0_P3_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1R Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1R Min Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 29: IN1R Min Threshold Check Control 2 - 0x00 / 0x03 / 0x1D (B0_P3_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1R Min Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 30: TEMP Max Threshold Check Control 1 - 0x00 / 0x03 / 0x1E (B0_P3_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	TEMP (TEMP1 or TEMP2) Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1R Max Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 31: TEMP Max Threshold Check Control 2 - 0x00 / 0x03 / 0x1F (B0_P3_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	TEMP (TEMP1 or TEMP2) Max Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 32: TEMP Min Threshold Check Control 1 - 0x00 / 0x03 / 0x20 (B0_P3_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	TEMP (TEMP1 or TEMP2) Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	TEMP Min Threshold 12-bit Code (MSB 4-bits)

Book 0 / Page 3 / Register 33: TEMP Min Threshold Check Control 2 - 0x00 / 0x03 / 0x21 (B0_P3_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	TEMP (TEMP1 or TEMP2) Min Threshold 12-bit Code (LSB 8-bits)

Book 0 / Page 3 / Register 34-53: Reserved Registers - 0x00 / 0x03 / 0x22-0x35 (B0_P3_R34-53)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 54: IN1L Measurement Data (MSB) - 0x00 / 0x03 / 0x36 (B0_P3_R54)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of IN1L Measurement 16-bit Data

Book 0 / Page 3 / Register 55: IN1L Measurement Data (LSB) - 0x00 / 0x03 / 0x37 (B0_P3_R55)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of IN1L Measurement 16-bit Data

Book 0 / Page 3 / Register 56: IN1R Measurement Data (MSB) - 0x00 / 0x03 / 0x38 (B0_P3_R56)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of IN1R Measurement 16-bit Data

Book 0 / Page 3 / Register 57: IN1R Measurement Data (LSB) - 0x00 / 0x03 / 0x39 (B0_P3_R57)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of IN1R Measurement 16-bit Data

Book 0 / Page 3 / Register 58: VBAT Measurement Data (MSB) - 0x00 / 0x03 / 0x3A (B0_P3_R58)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of VBAT Measurement 16-bit Data

Book 0 / Page 3 / Register 59: VBAT Measurement Data (LSB) - 0x00 / 0x03 / 0x3B (B0_P3_R59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of VBAT Measurement 16-bit Data

Book 0 / Page 3 / Register 60-65: Reserved Registers - 0x00 / 0x03 / 0x3C-0x41 (B0_P3_R60-65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 3 / Register 66: TEMP1 Measurement Data (MSB) - 0x00 / 0x03 / 0x42 (B0_P3_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of TEMP1 Measurement 16-bit Data

Book 0 / Page 3 / Register 67: TEMP1 Measurement Data (LSB) - 0x00 / 0x03 / 0x43 (B0_P3_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of TEMP1 Measurement 16-bit Data

Book 0 / Page 3 / Register 68: TEMP2 Measurement Data (MSB) - 0x00 / 0x03 / 0x44 (B0_P3_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of TEMP1 Measurement 16-bit Data

Book 0 / Page 3 / Register 69: TEMP2 Measurement Data (LSB) - 0x00 / 0x03 / 0x45 (B0_P3_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of TEMP1 Measurement 16-bit Data

Book 0 / Page 3 / Register 70-127: Reserved Registers - 0x00 / 0x03 / 0x46-0x7F (B0_P3_R70-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

8.6.5 Book 0 Page 4

Book 0 / Page 4 / Register 0: Page Select Register - 0x00 / 0x04 / 0x00 (B0_P4_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table ""Summary of Memory Map" for details.

Book 0 / Page 4 / Register 1: ASI1, Audio Bus Format Control Register - 0x00 / 0x04 / 0x01 (B0_P4_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	ASI1, format selection 000: ASI1 Audio Interface = I2S 001: ASI1 Audio Interface = DSP 010: ASI1 Audio Interface = RJF 011: ASI1 Audio Interface = LJF 100: ASI1 Audio Interface = Mono PCM 101-111: Reserved. Do not use.
D4-D3	R/W	0 0	ASI1 Data Word Length Selection 00: ASI1 Data Word length = 16 bits 01: ASI1 Data Word length = 20 bits 10: ASI1 Data Word length = 24 bits 11: ASI1 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	DOUT1 High Impendance Output Control 0: DOUT1 will not be high impedance while ASI1 is active 1: DOUT1 will be high impedance after data has been transferred

Book 0 / Page 4 / Register 2: ASI1, Left Ch_Offset_1 Control Register - 0x00 / 0x04 / 0x02 (B0_P4_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI1 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

Book 0 / Page 4 / Register 3: ASI1, Right Ch_Offset_2 Control Register - 0x00 / 0x04 / 0x03 (B0_P4_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI1 Data Offset Value (Ch_Offset_2) relative to last bit of left channel (applicable only if slot mode enabled) 0000 0000: Data Offset 2 = 0 BCLK's 0000 0001: Data Offset 2= 1 BCLK's ... 1111 1110: Data Offset 2 = 254 BCLK's 1111 1111: Data Offset 2 = 255 BCLK's

Book 0 / Page 4 / Register 4: ASI1, Channel Setup Register - 0x00 / 0x04 / 0x04 (B0_P4_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	

Book 0 / Page 4 / Register 4: ASI1, Channel Setup Register - 0x00 / 0x04 / 0x04 (B0_P4_R4) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R	00	Reserved. Write only default values.
D3-D2	R/W	00	00: For DAC all the left and right channels are enabled 01: For DAC all the left channels are disabled 10: For DAC all the right channels are disabled. 11: For DAC all the left and right channel are disabled.
D1-D0	R/W	00	00: For ADC all the left and right channels are enabled 01: For ADC all the left channels are disabled 10: For ADC all the right channels are disabled. 11: For ADC all the left and right channel are disabled.

Book 0 / Page 4 / Register 5: ASI1, ADC Audio Bus Format Control Register - 0x00 / 0x04 / 0x05 (B0_P4_R5)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Primary Audio Serial ADC Interface Format Selection (This control is only valid if D2 bit = '1'.) 000: ASI1 ADC Audio Interface = I2S 001: ASI1 ADC Audio Interface = DSP 010: ASI1 ADC Audio Interface = RJF 011: ASI1 ADC Audio Interface = LJF 100: ASI1 ADC Audio Interface = Mono PCM 101-111: Reserved. Do not use.
D4-D3	R/W	0 0	Primary Audio Serial ADC Interface Data Word Length Selection (This control is only valid if D2 bit = '1'.) 00: ASI1 ADC Data Word length = 16 bits 01: ASI1 ADC Data Word length = 20 bits 10: ASI1 ADC Data Word length = 24 bits 11: ASI1 ADC Data Word length = 32 bits
D2	R/W	0	Primary Audio Serial ADC Six-Wire Format and Wordlength Enable 0: ASI1 ADC pathway uses same interface format and wordlength as in B0_P4_R1. 1: ASI1 ADC pathway use interface format defined in D[7:5] and wordlength defined in D[4:2] of this register.
D1-D0	R	00	Reserved. Write only default values.

Book 0 / Page 4 / Register 6: Audio Serial Interface 1, Multi-Pin Mode - 0x00 / 0x04 / 0x06 (B0_P4_R6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1 Data Input and Output Mode 0: Single Data Input Pin, Single Data Output Pin 1: Multiple Data Input Pin, Multiple Data Output Pin
D6-D0	R	000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 7: ASI1, ADC Input Control - 0x00 / 0x04 / 0x07 (B0_P4_R7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	001	ASI1 ADC Input Control 000: ASI1 digital audio output data source disabled (No serial data output on external ASI1 bus. ASI1 digital output is tri-stated.) 001: ASI1_DataOutput[1:8] is sourced from miniDSP_A_DataOutput[1:8] (ADC signal fed to ASI1.) 010: ASI1_DataOutput[1:8] is sourced from ASI1_DataInput[1:8] (ASI1-to-ASI1 loopback) 011: ASI1_DataOutput[1:2] is sourced from ASI2_DataInput[1:2] (ASI2-to-ASI1 loopback) 100: ASI1_DataOutput[1:2] is sourced from ASI3_DataInput[1:2] (ASI3-to-ASI1 loopback)

Book 0 / Page 4 / Register 8: ASI1, DAC Output Control - 0x00 / 0x04 / 0x08 (B0_P4_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	01	ASI1 Left DAC Datapath 00: ASI1 Left DAC Datapath = Off 01: ASI1 Left DAC Datapath = Left Data 10: ASI1 Left DAC Datapath = Right Data 11: ASI1 Left DAC Datapath = Mono Mix of Left and Right
D5-D4	R/W	01	ASI1 Right DAC Datapath 00: ASI1 Right DAC Datapath = Off 01: ASI1 Right DAC Datapath = Right Data 10: ASI1 Right DAC Datapath = Left Data 11: ASI1 Right DAC Datapath = Mono Mix of Left and Right
D3-D2	R	00	Reserved. Write only default values.
D1	R/W	0	0: Left and right channel slot-swapping is disabled for ADC datapath. 1: Left and right channel slot-swapping is enabled for ADC datapath.
D0	R/W	0	0: Time slot mode is disabled which means the position for left and right channels will be controlled by WCLK and offset1 programming controlled by B0_P4_R2. 1: Time slot mode is enabled which means the position for the left channels are controlled by WCLK and offset1 programming controlled by B0_P4_R2 and for right channel the relative offset with respect to last bit of left channel will be contolled by B0_P4_R3.

Book 0 / Page 4 / Register 9: ASI1, Control Register 9, ADC Slot Tristate Control - 0x00 / 0x04 / 0x09 (B0_P4_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC left channel <L4> slot is not tri-stated 1: ADC left channel <L4> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D6	R/W	0	0: ADC left channel <L3> slot is not tri-stated 1: ADC left channel <L3> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D5	R/W	0	0: ADC left channel <L2> slot is not tri-stated 1: ADC left channel <L2> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D4	R/W	0	0: ADC left channel <L1> slot is not tri-stated 1: ADC left channel <L1> slot is tri-stated. Must also set B0_P4_R1_D0='1'. (Note that, in multi-channel mode, this will tristate all Left channels. If individual Left channels need to be tri-stated, this can be achieved on the bus by disconnecting the output pin.)
D3	R/W	0	0: ADC left channel <R4> slot is not tri-stated 1: ADC left channel <R4> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D2	R/W	0	0: ADC left channel <R3> slot is not tri-stated 1: ADC left channel <R3> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D1	R/W	0	0: ADC left channel <R2> slot is not tri-stated 1: ADC left channel <R2> slot is tri-stated. Must also set B0_P4_R1_D0='1'. This should only be used in single-pin mode for ASI1 (that is cannot use multi-pin mode).
D0	R/W	0	0: ADC right channel <R1> slot is not tri-stated 1: ADC right channel <R1> slot is tri-stated. Must also set B0_P4_R1_D0='1'. (Note that, in multi-channel mode, this will tristate all Right channels. If individual Right channels need to be tri-stated, this can be achieved on the bus by disconnecting the output pin.)

Book 0 / Page 4 / Register 10: ASI1, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x0A (B0_P4_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	ASI1 Word Clock Direction Control 000: WCLK1 pin is Word Clock input to ASI1 001: WCLK1 pin is Word Clock output from ASI1 010-111: Reserved. Do not use.

Book 0 / Page 4 / Register 10: ASI1, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x0A (B0_P4_R10) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D2	R/W	0 00	ASI1 Bit Clock Direction Control 000: BCLK1 pin is Bit Clock input to ASI1 001: BCLK1 pin is Bit Clock output from ASI1 010-111: Reserved. Do not use.
D1	R/W	0	Primary Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	ASI1 Bit Clock and ASI1 Word Clock Power control 0: ASI1 Bit Clock and ASI1 Word Clock buffers are powered down when the codec is powered down or ASI 1 is inactive 1: ASI1 Bit Clock and ASI1 Word Clock buffers are powered up when they are used in clock generation even when the codec is powered down

Book 0 / Page 4 / Register 11: ASI1, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x0B (B0_P4_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1_ADC_BCLK_OUT configuration used for 6-wire mode with ADC Bit Clock as output: 0: ASI1_ADC_BCLK_OUT = ASI1_BCLK_OUT configured in B0_P4_R14_D[7:4]. 1: ASI1_ADC_BCLK_OUT can be different from ASI1_BCLK_OUT and is configured in B0_P4_R115_D[7:4].
D6	R/W	0	ASI1_ADC_WCLK_OUT configuration used for 6-wire mode with ADC Word Clock as output: 0: ASI1_ADC_WCLK_OUT = ASI1_WCLK_OUT configured in B0_P4_R14_D[3:0]. 1: ASI1_WCLK_OUT can be different from ASI1_WCLK_OUT and is configured in B0_P4_R115_D[3:0].
D5-D4	R	00	Reserved. Write only default values.
D3-D0	R/W	0000	ASI1 BDIV_CLKIN Multiplexer Control 0000: ASI1_BDIV_CLKIN = DAC_CLK 0001: ASI1_BDIV_CLKIN = DAC_MOD_CLK 0010: ASI1_BDIV_CLKIN = ADC_CLK 0011: ASI1_BDIV_CLKIN = ADC_MOD_CLK 0100: ASI1_BDIV_CLKIN = ASI1 Bit Clock Input Pin 0101: ASI1_BDIV_CLKIN = ASI2 Bit Clock Input Pin 0110: ASI1_BDIV_CLKIN = ASI3 Bit Clock Input Pin 0111: ASI1_BDIV_CLKIN = ASI1 ADC Bit Clock Input Pin (6-wire interface) 1000: ASI1_BDIV_CLKIN = ASI2 ADC Bit Clock Input Pin (6-wire interface) 1001-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 12: ASI1, Bit Clock N Divider - 0x00 / 0x04 / 0x0C (B0_P4_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1 BCLK N Divider Power Control 0: BCLK N divider powered down 1: BCLK N divider powered up
D6-D0	R/W	000 0001	ASI1 BCLK N Divider value 0000 0000: BCLK N divider = 128 0000 0001: BCLK N divider = 1 ... 1111 1110: BCLK N divider = 126 1111 1111: BCLK N divider = 127

Book 0 / Page 4 / Register 13: ASI 1, Word Clock N Divider - 0x00 / 0x04 / 0x0D (B0_P4_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1 WCLK Divider Power Control 0: Primary WCLK N divider is powered down 1: Primary WCLK N divider is powered up

Book 0 / Page 4 / Register 13: ASI 1, Word Clock N Divider - 0x00 / 0x04 / 0x0D (B0_P4_R13) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	010 0000	ASI1 WCLK N Divider value 000 0000: Primary WCLK divider N = 128 010 0000: Primary WCLK divider N = 32 010 0001: Primary WCLK divider N = 33 … 111 1110: Primary WCLK divider N = 126 111 1111: Primary WCLK divider N = 127

Book 0 / Page 4 / Register 14: ASI1, BCLK and WCLK Output - 0x00 / 0x04 / 0x0E (B0_P4_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	ASI1 Bit Clock Output Mux 0000: Bit Clock Output = ASI1 Bit Clock Divider Output 0001: Reserved. Do not use. 0010: Bit Clock Output = ASI2 Bit Clock Divider Output 0011: Bit Clock Output = ASI2 Bit Clock Input 0100: Bit Clock Output = ASI3 Bit Clock Divider Output 0101: Bit Clock Output = ASI3 Bit Clock Input 0110: Bit Clock Output = ASI1 ADC Bit Clock 0111: Bit Clock Output = ASI2 ADC Bit Clock 1000-1111: Reserved. Do not use.
D3-D0	R/W	0000	ASI1 Word Clock Output Mux 0000: Word Clock Output = Generated DAC_FS 0001: Word Clock Output = Generated ADC_FS 0010: Word Clock Output = ASI1 Word Clock Divider Output 0011: Reserved. Do not use. 0100: Word Clock Output = ASI2 Word Clock Divider Output 0101: Word Clock Output = ASI2 Word Clock Input 0110: Word Clock Output = ASI3 Word Clock Divider Output 0111: Word Clock Output = ASI3 Word Clock Input 1000: Word Clock Output = ASI1 ADC Word Clock 1001: Word Clock Output = ASI2 ADC Word Clock 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 15: ASI1, Data Output - 0x00 / 0x04 / 0x0F (B0_P4_R15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI1 Data Output Control 00: DOUT1 from Codec ASI1 Output 01: DOUT1 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT1 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT1 from ASI3 Data Input (Pin-to-Pin Loopback)

Book 0 / Page 4 / Register 16: ASI1, ADC Word Clock and Bit Clock Control - 0x00 / 0x04 / 0x10 (B0_P4_R16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	ASI1 ADC Word Clock Control for Six-Wire Interface 000: ADC Word Clock is same as DAC Word Clock (Default 4-wire Interface) 001: ADC Word Clock is input or output on GPIO1 010: ADC Word Clock is input or output on GPIO2 011: ADC Word Clock is input on GPIO3 100: ADC Word Clock is input on GPIO4 101-111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.

Book 0 / Page 4 / Register 16: ASI1, ADC Word Clock and Bit Clock Control - 0x00 / 0x04 / 0x10 (B0_P4_R16) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	ASI1 ADC Bit Clock Control for Six-Wire Interface 000: ADC Bit Clock is same as DAC Bit Clock (Default 4-wire Interface) 001: ADC Bit Clock is inputor output on GPIO1 010: ADC Bit Clock is input or output on GPIO2 011: ADC Bit Clock is input on GPIO3 100: ADC Bit Clock is input on GPIO4 101-111: Reserved. Do not use.

Book 0 / Page 4 / Register 17: ASI2, Audio Bus Format Control Register - 0x00 / 0x04 / 0x11 (B0_P4_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	ASI2, format selection 000: ASI2 Audio Interface = I2S 001: ASI2 Audio Interface = DSP 010: ASI2 Audio Interface = RJF 011: ASI2 Audio Interface = LJF 100: ASI2 Audio Interface = Mono PCM 101: Reserved. Do not use.
D4-D3	R/W	0 0	ASI2 Data Word Length Selection 00: ASI2 Data Word length = 16 bits 01: ASI2 Data Word length = 20 bits 10: ASI2 Data Word length = 24 bits 11: ASI2 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	ASI2 Data Output High Impendance Output Control 0: DOUT2 will not be high impedance while ASI2 is active 1: DOUT2 will be high impedance after data has been transferred

Book 0 / Page 4 / Register 18: ASI2, Data Offset Control Register - 0x00 / 0x04 / 0x12 (B0_P4_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI2 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

Book 0 / Page 4 / Register 19-20: Reserved Registers - 0x00 / 0x04 / 0x13-0x14 (B0_P4_R19-20)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 21: ASI2, ADC Audio Bus Format Control Register - 0x00 / 0x04 / 0x15 (B0_P4_R21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Secondary Audio Serial ADC Interface Format Selection (This control is only valid if D2 bit = '1'.) 000: ASI2 ADC Audio Interface = I2S 001: ASI2 ADC Audio Interface = DSP 010: ASI2 ADC Audio Interface = RJF 011: ASI2 ADC Audio Interface = LJF 100: ASI2 ADC Audio Interface = Mono PCM 101-111: Reserved. Do not use.

Book 0 / Page 4 / Register 21: ASI2, ADC Audio Bus Format Control Register - 0x00 / 0x04 / 0x15 (B0_P4_R21) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D3	R/W	0 0	Secondary Audio Serial ADC Interface Data Word Length Selection (This control is only valid if D2 bit = '1'.) 00: ASI2 ADC Data Word length = 16 bits 01: ASI2 ADC Data Word length = 20 bits 10: ASI2 ADC Data Word length = 24 bits 11: ASI2 ADC Data Word length = 32 bits
D2	R/W	0	Secondary Audio Serial ADC Six-Wire Format and Wordlength Enable 0: ASI2 ADC pathway uses same interface format and wordlength as in B0_P4_R17. 1: ASI2 ADC pathway use interface format defined in D[7:5] and wordlength defined in D[4:2] of this register.
D1-D0	R	00	Reserved. Write only default values.

Book 0 / Page 4 / Register 22: Reserved Register - 0x00 / 0x04 / 0x16 (B0_P4_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 23: ASI2, ADC Input Control - 0x00 / 0x04 / 0x17 (B0_P4_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	ASI2 ADC Input Control 000: ASI2 digital audio output data source disabled (No serial data output on external ASI2 bus. ASI2 digital output is tri-stated.) 001: ASI2_DigitalOutput[1:2] is sourced from miniDSP_A_DataOutput[1:2] 010: ASI2_DigitalOutput[1:2] is is sourced from ASI1 DataInput (ASI1-to-ASI2 loopback) 011: ASI2_DigitalOutput[1:2] is is sourced from ASI2 DataInput (ASI2-to-ASI1 loopback) 100: ASI2_DigitalOutput[1:2] is is sourced from ASI3 DataInput (ASI3-to-ASI1 digital loopback) 101: ASI2_DigitalOutput[1:2] is sourced from miniDSP_A_DataOutput[3:4] 110-111: Reserved. Do not use.

Book 0 / Page 4 / Register 24: ASI 2, DAC Output Control - 0x00 / 0x04 / 0x18 (B0_P4_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	ASI2 Left DAC Datapath 00: ASI2 Left DAC Datapath = Off 01: ASI2 Left DAC Datapath = Left Data 10: ASI2 Left DAC Datapath = Right Data 11: ASI2 Left DAC Datapath = Mono Mix of Left and Right
D5-D4	R/W	00	ASI2 Right DAC Datapath 00: ASI2 Right DAC Datapath = Off 01: ASI2 Right DAC Datapath = Right Data 10: ASI2 Right DAC Datapath = Left Data 11: ASI2 Right DAC Datapath = Mono Mix of Left and Right
D3-D0	R	0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 25: Reserved Register - 0x00 / 0x04 / 0x19 (B0_P4_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 26: ASI2, Word Clock and Bit Clock Control Register - 0x00 / 0x04 / 0x1A (B0_P4_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values.

Book 0 / Page 4 / Register 26: ASI2, Word Clock and Bit Clock Control Register - 0x00 / 0x04 / 0x1A (B0_P4_R26) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	ASI2 Word Clock Direction Control 0: WCLK2 pin is input to ASI2 1: WCLK2 pin is output from ASI2
D4-D3	R	0 0	Reserved. Write only default values.
D2	R/W	0	ASI2 Bit Clock Direction Control 0: BCLK2 pin is input to ASI2 Bit Clock 1: BCLK2 pin is output from ASI2 Bit Clock
D1	R/W	0	ASI2 Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	ASI2 Bit Clock and Word Clock Power control 0: ASI2 Bit Clock and Word Clock buffers are powered down when the codec is powered down or ASI2 is inactive 1: ASI2 Bit Clock and Word Clock buffers are powered up when they are used in clock generation even when the codec is powered down

Book 0 / Page 4 / Register 27: ASI2, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x1B (B0_P4_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI2_ADC_BCLK_OUT configuration used for 6-wire mode with ADC Bit Clock as output: 0: ASI2_ADC_BCLK_OUT = ASI2_BCLK_OUT configured in B0_P4_R30_D[7:4]. 1: ASI2_ADC_BCLK_OUT can be different from ASI2_BCLK_OUT and is configured in B0_P4_R116_D[7:4].
D6	R/W	0	ASI2_ADC_WCLK_OUT configuration used for 6-wire mode with ADC Bit Clock as output: 0: ASI2_ADC_WCLK_OUT = ASI2_WCLK_OUT configured in B0_P4_R30_D[3:0]. 1: ASI2_ADC_WCLK_OUT can be different from ASI2_WCLK_OUT and is configured in B0_P4_R116_D[3:0].
D5-D4	R	00	Reserved. Write only default values.
D1-D0	R/W	00	ASI2_BDIV_CLKIN Multiplexer Control 0000: ASI2_BDIV_CLKIN = DAC_CLK (Generated On-Chip) 0001: ASI2_BDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 0010: ASI2_BDIV_CLKIN = ADC_CLK (Generated On-Chip) 0011: ASI2_BDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip) 0100: ASI2_BDIV_CLKIN = ASI1 Bit Clock Input Pin 0101: ASI2_BDIV_CLKIN = ASI2 Bit Clock Input Pin 0110: ASI2_BDIV_CLKIN = ASI3 Bit Clock Input Pin 0111: ASI2_BDIV_CLKIN = ASI1 ADC Bit Clock Input Pin (6-wire interface) 1000: ASI2_BDIV_CLKIN = ASI2 ADC Bit Clock Input Pin (6-wire interface) 1001-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 28: ASI2, Bit Clock N Divider - 0x00 / 0x04 / 0x1C (B0_P4_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI2 BCLK Divider Power Control 0: Secondary BCLK N divider is powered down 1: Secondary BCLK N divider is powered up
D6-D0	R/W	000 0001	ASI2 BCLK N Divider value 000 0000: Secondary BCLK divider N = 128 000 0001: Secondary BCLK divider N = 1 000 0010: Secondary BCLK divider N = 2 … 111 1110: Secondary BCLK divider N = 126 111 1111: Secondary BCLK divider N = 127

Book 0 / Page 4 / Register 29: ASI2, Word Clock N Divider - 0x00 / 0x04 / 0x1D (B0_P4_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI2 WCLK Divider Power Control 0: Secondary WCLK N divider is powered down 1: Secondary WCLK N divider is powered up
D6-D0	R/W	010 0000	ASI2 WCLK N Divider value 000 0000: Secondary WCLK divider N = 128 010 0000: Secondary WCLK divider N = 32 010 0001: Secondary WCLK divider N = 33 … 111 1110: Secondary WCLK divider N = 126 111 1111: Secondary WCLK divider N = 127

Book 0 / Page 4 / Register 30: ASI2, Bit Clock and Word Clock Output - 0x00 / 0x04 / 0x1E (B0_P4_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0010	ASI2 Bit Clock Output Mux 0000: ASI2_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 0001: ASI2_BCLK_OUT = ASI1 Bit Clock Input (ASI1_BCLK) 0010: ASI2_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 0011: Reserved. Do not use. 0100: ASI2_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 0101: ASI2_BCLK_OUT = ASI3 Bit Clock Input (ASI3_BCLK) 0110: ASI2_BCLK_OUT = ASI1 ADC Bit Clock 0111: ASI2_BCLK_OUT = ASI2 ADC Bit Clock 1000-1111: Reserved. Do not use.
D2-D0	R/W	000	ASI2 Word Clock Output Mux 0000: ASI2_WCLK_OUT = Generated DAC_FS 0001: ASI2_WCLK_OUT = Generated ADC_FS 0010: ASI2_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 0011: ASI2_WCLK_OUT = ASI1 Word Clock Input (ASI1_WCLK) 0100: ASI2_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 0101: Reserved. Do not use. 0110: ASI2_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 0111: ASI2_WCLK_OUT = ASI3 Word Clock Input (ASI3_WCLK) 1000: ASI2_WCLK_OUT = ASI1 ADC Word Clock 1001: ASI2_WCLK_OUT = ASI2 ADC Word Clock 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 31: ASI2, Data Output - 0x00 / 0x04 / 0x1F (B0_P4_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI2 Data Output Control 00: DOUT2 from Codec ASI2 Output 01: DOUT2 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT2 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT2 from ASI3 Data Input (Pin-to-Pin Loopback)

Book 0 / Page 4 / Register 32: ASI2, ADC Word Clock and Bit Clock Control - 0x00 / 0x04 / 0x20 (B0_P4_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	ASI2 ADC Word Clock Control for Six-Wire Interface 000: ADC Word Clock is same as DAC Word Clock (Default 4-wire Interface) 001: ADC Word Clock is input or output on GPIO1 010: ADC Word Clock is input or output on GPIO2 011: ADC Word Clock is input on GPIO3 100: ADC Word Clock is input on GPIO4 101-111: Reserved. Do not use.

Book 0 / Page 4 / Register 32: ASI2, ADC Word Clock and Bit Clock Control - 0x00 / 0x04 / 0x20 (B0_P4_R32) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	ASI2 ADC Bit Clock Control for Six-Wire Interface 000: ADC Bit Clock is same as DAC Bit Clock (Default 4-wire Interface) 001: ADC Bit Clock is input or output on GPIO1 010: ADC Bit Clock is input or output on GPIO2 011: ADC Bit Clock is input on GPIO3 100: ADC Bit Clock is input on GPIO4 101-111: Reserved. Do not use.

Book 0 / Page 4 / Register 33: ASI3, Audio Bus Format Control Register - 0x00 / 0x04 / 0x21 (B0_P4_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	ASI3, format selection 000: ASI3 Audio Interface = I2S 001: ASI3 Audio Interface = DSP 010: ASI3 Audio Interface = RJF 011: ASI3 Audio Interface = LJF 100: ASI3 Audio Interface = Mono PCM 101-111: Reserved. Do not use.
D4-D3	R/W	0 0	ASI3, Data Word Length Selection 00: ASI3 Data Word length = 16 bits 01: ASI3 Data Word length = 20 bits 10: ASI3 Data Word length = 24 bits 11: ASI3 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	DOUT3 High Impendance Output Control 0: DOUT3 will not be high impedance while ASI1 is active 1: DOUT3 will be high impedance after data has been transferred

Book 0 / Page 4 / Register 34: ASI3, Data Offset Control Register - 0x00 / 0x04 / 0x22 (B0_P4_R34)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI3 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

Book 0 / Page 4 / Register 35-36: Reserved Registers - 0x00 / 0x04 / 0x23-0x24 (B0_P4_R35-36)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 37: Reserved Register - 0x00 / 0x04 / 0x25 (B0_P4_R37)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Reserved. Write only default values.
D4-D3	R/W	0 0	Reserved. Write only default values.
D2	R/W	0	Reserved. Write only default values.
D1-D0	R	00	

Book 0 / Page 4 / Register 38: Reserved Register - 0x00 / 0x04 / 0x26 (B0_P4_R38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 39: ASI3, ADC Input Control - 0x00 / 0x04 / 0x27 (B0_P4_R39)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	ASI3 ADC Input Control 000: ASI3 digital audio output data source disabled (No serial data output on external ASI3 bus. ASI3 digital output is tri-stated.) 001: ASI3_DataOutput[1:2] data is sourced from miniDSP_ADataOutput[1:2] 010: ASI3_DataOutput[1:2] is sourced from ASI1_DataInput[1:2] (ASI1-to-ASI3 loopback) 011: ASI3_DataOutput[1:2] is sourced from ASI2_DataInput[1:2] (ASI2-to-ASI3 loopback) 100: ASI3_DataOutput[1:2] is sourced from ASI3_DataInput[1:2] (ASI3-to-ASI3 loopback) 101: Reserved. Do not use. 110: ASI3_DataOutput[1:2] is sourced from miniDSP_A_DataOutput[5:6] 111: Reserved. Do not use.

Book 0 / Page 4 / Register 40: ASI3, DAC Output Control - 0x00 / 0x04 / 0x28 (B0_P4_R40)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	ASI3 Left DAC Datapath 00: ASI3 Left DAC Datapath = Off 01: ASI3 Left DAC Datapath = Left Data 10: ASI3 Left DAC Datapath = Right Data 11: ASI3 Left DAC Datapath = Mono Mix of Left and Right
D5-D4	R/W	00	ASI3 Right DAC Datapath 00: ASI3 Right DAC Datapath = Off 01: ASI3 Right DAC Datapath = Right Data 10: ASI3 Right DAC Datapath = Left Data 11: ASI3 Right DAC Datapath = Mono Mix of Left and Right
D3-D0	R	0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 41: Reserved Register - 0x00 / 0x04 / 0x29 (B0_P4_R41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 42: ASI3, Word Clock and Bit Clock Control Register - 0x00 / 0x04 / 0x2A (B0_P4_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	000000	Reserved. Write only default values.
D1	R/W	0	ASI3 Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	ASI3 Bit Clock and Word Clock Power control 0: ASI3 Bit Clock and ASI3 Word Clock buffers are powered down when the codec is powered down or ASI3 is inactive 1: ASI3 Bit Clock and Word Clock buffers are powered up when they are used in clock generation even when the codec is powered down

Book 0 / Page 4 / Register 43: ASI3, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x2B (B0_P4_R43)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only default values.
D6	R/W	0	Reserved. Write only default values.

Book 0 / Page 4 / Register 43: ASI3, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x2B (B0_P4_R43) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R	00	Reserved. Write only default values.
D3-D0	R/W	0000	ASI3_BDIV_CLKIN Multiplexer Control 0000: ASI3_BDIV_CLKIN = DAC_CLK (Generated On-Chip) 0001: ASI3_BDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 0010: ASI3_BDIV_CLKIN = ADC_CLK (Generated On-Chip) 0011: ASI3_BDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip) 0100: ASI3_BDIV_CLKIN = ASI1 Bit Clock Input Pin 0101: ASI3_BDIV_CLKIN = ASI2 Bit Clock Input Pin 0110: ASI3_BDIV_CLKIN = ASI3 Bit Clock Input Pin 0111: ASI3_BDIV_CLKIN = ASI1 ADC Bit Clock Input Pin (6-wire interface) 1000: ASI3_BDIV_CLKIN = ASI2 ADC Bit Clock Input Pin (6-wire interface) 1001-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 44: ASI3, Bit Clock N Divider - 0x00 / 0x04 / 0x2C (B0_P4_R44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI3 Bit Clock Divider Power Control 0: ASI3 Bit Clock N divider is powered down 1: ASI3 Bit Clock N divider is powered up
D6-D0	R/W	000 0001	ASI3 Bit Clock N Divider value 000 0000: ASI3 Bit Clock divider N = 128 000 0001: ASI3 Bit Clock divider N = 1 000 0010: ASI3 Bit Clock divider N = 2 … 111 1110: ASI3 Bit Clock divider N = 126 111 1111: ASI3 Bit Clock divider N = 127

Book 0 / Page 4 / Register 45: ASI3, Word Clock N Divider - 0x00 / 0x04 / 0x2D (B0_P4_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI3 Word Clock Divider Power Control 0: ASI3 Word Clock N divider is powered down 1: ASI3 Word Clock N divider is powered up
D6-D0	R/W	010 0000	ASI3 Word Clock N Divider value 000 0000: ASI3 Word Clock divider N = 128 010 0000: ASI3 Word Clock divider N = 32 010 0001: ASI3 Word Clock divider N = 33 … 111 1110: ASI3 Word Clock divider N = 126 111 1111: ASI3 Word Clock divider N = 127

Book 0 / Page 4 / Register 46: ASI3, Bit Clock and Word Clock Output - 0x00 / 0x04 / 0x2E (B0_P4_R46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0100	ASI3 Bit Clock Output Mux 0000: ASI3_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 0001: ASI3_BCLK_OUT = ASI1 Bit Clock Input (ASI1_BCLK) 0010: ASI3_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 0011: ASI3_BCLK_OUT = ASI2 Bit Clock Input (ASI2_BCLK) 0100: ASI3_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 0101: Reserved. Do not use. 0110: ASI3_BCLK_OUT = ASI1 ADC Bit Clock 0111: ASI3_BCLK_OUT = ASI2 ADC Bit Clock 1000-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 46: ASI3, Bit Clock and Word Clock Output - 0x00 / 0x04 / 0x2E (B0_P4_R46) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	ASI3 Word Clock Output Mux 0000: ASI3_WCLK_OUT = Generated DAC_FS 0001: ASI3_WCLK_OUT = Generated ADC_FS 0010: ASI3_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 0011: ASI3_WCLK_OUT = ASI1 Word Clock Input (ASI1_WCLK) 0100: ASI3_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 0101: ASI3_WCLK_OUT = ASI2 Word Clock Input (ASI2_WCLK) 0110: ASI3_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 0111: Reserved. Do not use. 1000: ASI3_WCLK_OUT = ASI1 ADC Word Clock 1001: ASI3_WCLK_OUT = ASI2 ADC Word Clock 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 47: ASI3, Data Output - 0x00 / 0x04 / 0x2F (B0_P4_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI3 Data Output Control 00: DOUT3 from Codec ASI 3 Output 01: DOUT3 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT3 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT3 from ASI3 Data Input (Pin-to-Pin Loopback)

Book 0 / Page 4 / Register 48: Reserved Register. - 0x00 / 0x04 / 0x30 (B0_P4_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 49: ASI1 L1, R1 Input Control - 0x00 / 0x04 / 0x31 (B0_P4_R49)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4-D0	R/W	0 0001	Stereo Pair 1 Input Control (Valid for both Stereo mode and Multi-pin mode) 00000: No input selected. Data will be all zeroes. 00001: Left and Right Channels will be from DIN1 for Stereo Mode (L1, R1 for Multipin Mode) 00010-11111: Reserved. Do not use.

Book 0 / Page 4 / Register 50: ASI1 L2, R2 Input Control - 0x00 / 0x04 / 0x32 (B0_P4_R50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4-D0	R/W	0 0000	Stereo Pair 2 Input Control (Valid for only Multi-pin mode. Do not use this register for single-pin or stereo mode.) 00000: No input selected. Data will be all zeroes. 00001: Reserved. Do not use. 00010-00100: Reserved. Do not use. 00101: L2, R2 Channels will be input from GPIO2 00110: L2, R2 Channels will be input from GPIO3 00111-11111: Reserved. Do not use.

Book 0 / Page 4 / Register 51: ASI1 L3, R3 Input Control - 0x00 / 0x04 / 0x33 (B0_P4_R51)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.

Book 0 / Page 4 / Register 51: ASI1 L3, R3 Input Control - 0x00 / 0x04 / 0x33 (B0_P4_R51) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D0	R/W	0 0000	Stereo Pair 3 Input Control (Valid for only Multi-pin mode. Do not use this register for single-pin or stereo mode.) 00000: No input selected. Data will be all zeroes. 00001-00011: Reserved. Do not use. 00100: L3, R3 Channels will be input from GPIO1 00101: L3, R3 Channels will be input from GPIO2 00110: L3, R3 Channels will be input from GPIO3 00111: Reserved. Do not use. 01000: L3, R3 Channels will be input from GPIO5 01001-11111: Reserved. Do not use.

Book 0 / Page 4 / Register 52: ASI1 L4, R4 Input Control - 0x00 / 0x04 / 0x34 (B0_P4_R52)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4-D0	R/W	0 0000	Stereo Pair 4 Input Control (Valid for only Multi-pin mode. Do not use this register for single-pin or stereo mode.) 00000: No input selected. Data will be all zeroes. 00001-00011: Reserved. Do not use. 00100: L4, R4 Channels will be input from GPIO1 00101: L4, R4 Channels will be input from GPIO2 00110: L4, R4 Channels will be input from GPIO3 00111: Reserved. Do not use. 01000: L4, R4 Channels will be input from GPIO5 01001-01101: Reserved. Do not use. 01110: L4, R4 Channels will be input from WCLK2 01111-11111: Reserved. Do not use.

Book 0 / Page 4 / Register 53: Reserved Register - 0x00 / 0x04 / 0x35 (B0_P4_R53)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 54: ASI2, DIN Input Multiplexer Control - 0x00 / 0x04 / 0x36 (B0_P4_R54)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	Reserved. Write only default values.

Book 0 / Page 4 / Register 55: ASI3, Word Clock and Bit Clock Input Multiplexer Control - 0x00 / 0x04 / 0x37 (B0_P4_R55)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	ASI3 Word Clock Control 000-001: Reserved. Do not use. 010: ASI3_WCLK is input or output on GPIO2 011-111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	ASI3 Bit Clock Control 000: Reserved. Do not use. 001: ASI3_BCLK is input or output on GPIO1 010-111: Reserved. Do not use.

Book 0 / Page 4 / Register 56: ASI3, DIN Input Multiplexer Control - 0x00 / 0x04 / 0x38 (B0_P4_R56)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	ASI3 Data Input Multiplexer Control 000-010: Reserved. Do not use. 011: ASI3_DIN is input on GPIO3. 110-111: Reserved. Do not use.

Book 0 / Page 4 / Register 57-64: Reserved Registers - 0x00 / 0x04 / 0x39-0x40 (B0_P4_R57-64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 65: WCLK1 (Input or Output) Pin Control - 0x00 / 0x04 / 0x41 (B0_P4_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values.
D5-D2	R/W	00 01	WCLK1 Pin Control 0000: Reserved. Do not use. 0001: WCLK1 is ASI1 Word Clock Input or Output. (Note: B0_P4_R10 defines ASI1 Word Clock routing.) 0010-0011: Reserved. Do not use. 0100: WCLK1 pin is CLKOUT output.
D1-D0	R	00	Reserved. Write only default values.

Book 0 / Page 4 / Register 66: Reserved Register - 0x00 / 0x04 / 0x42 (B0_P4_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

Book 0 / Page 4 / Register 67: DOUT1 (Output) Pin Control - 0x00 / 0x04 / 0x43 (B0_P4_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	1	DOUT1 Bus Keeper Control 0: DOUT1 Bus Keeper Enabled 1: DOUT1 Bus Keeper Disabled
D4-D1	R/W	0 001	DOUT1 Pin Control 0000: DOUT1 disabled 0001: DOUT1 is ASI1 Data Output 0010: DOUT1 is General Purpose Output 0011: DOUT1 is CLKOUT 0100: DOUT1 is INT1 0101: DOUT1 is INT2 0110: DOUT1 is SAR ADC interrupt as defined in B0_P3 0111-1111: Reserved. Do not use.
D0	R/W	0	DOUT1 as General Purpose Output 0: DOUT1 General Purpose Output is '0' 1: DOUT1 General Purpose Output is '1'

Book 0 / Page 4 / Register 68: DIN1 (Input) Pin Control - 0x00 / 0x04 / 0x44 (B0_P4_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 4 / Register 68: DIN1 (Input) Pin Control - 0x00 / 0x04 / 0x44 (B0_P4_R68) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D5	R/W	01	DIN1 Pin Control 00: DIN1 Disabled with input buffer powered down. 01: DIN1 Enabled with auto-power-down of input buffer if not actively used by the device. Applicable for DIN1 used as Data Input for ASI1, Digital Microphone Input, PLL_CLKIN and CDIV_CLKIN. 10: DIN1 Enabled with input buffer powered on. Required for DIN1 used as a General Purpose Input and applicable for DIN1 used as Data Input for ASI1, Digital Microphone Input, PLL_CLKIN and CDIV_CLKIN. 11: Reserved. Do not use
D4	R	X	DIN1 Input Pin State, used along with DIN1 as general purpose input
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 69: WCLK2 (Input or Output) Pin Control - 0x00 / 0x04 / 0x45 (B0_P4_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D2	R/W	00 01	WCLK2 Pin Control 0000: WCLK2 pin Disabled (Input and Output buffers powered down) 0001: WCLK2 pin acts as ASI Secondary WCLK as defined in B0_P4_R26_D5 0010: WCLK2 pin is used as General Purpose Input (GPI) or chip input for any other purpose. 0011: WCLK2 pin Output = General Purpose Output 0100: WCLK2 pin Output = CLKOUT Output 0101: WCLK2 pin Output = INT1 Interrupt Output 0110: WCLK2 pin Output = INT2 Interrupt Output 0111-1000: Reserved. Do not use. 1001: WCLK2 pin Output = SAR ADC interrupt as defined in B0_P3 1010: WCLK2 pin Output = ADC_MOD_CLK Output for digital microphone 1011-1110: Reserved. Do not use. 1111: WCLK2 pin Output = L4, R4 Data Ouput for ASI1 (Multi-pin mode only)
D1	R	X	WCLK2 Input Pin State, used along with WCLK2 as general purpose input
D0	R/W	0	WCLK2 as General Purpose Output 0: WCLK2 General Purpose Output is '0' 1: WCLK2 General Purpose Output is '1'

Book 0 / Page 4 / Register 70: BCLK2 (Input or Output) Pin Control - 0x00 / 0x04 / 0x46 (B0_P4_R70)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values
D5-D2	R/W	00 01	BCLK2 Pin Control 0000: BCLK2 pin Disabled (Input and Output buffers powered down) 0001: BCLK2 pin acts as ASI Secondary BCLK as defined in B0_P4_R26_D2 0010: BCLK2 pin is used as General Purpose Input (GPI) or chip input for any other purpose. 0011: BCLK2 pin Output = General Purpose Output 0100: BCLK2 pin Output = CLKOUT Output 0101: BCLK2 pin Output = INT1 Interrupt Output 0110: BCLK2 pin Output = INT2 Interrupt Output 0111-1000: Reserved. Do not use. 1001: BCLK2 pin Output = SAR ADC interrupt as defined in B0_P3 1010: BCLK2 pin Output = ADC_MOD_CLK Output for digital microphone 1011-1101: Reserved. Do not use. 1110: BCLK2 pin Output = L3, R3 Data Output for ASI1 (Multi-pin mode only) 1111: Reserved. Do not use.
D1	R	X	BCLK2 Input Pin State, used along with BCLK2 as general purpose input
D0	R/W	0	BCLK2 as General Purpose Output 0: BCLK2 General Purpose Output is '0' 1: BCLK2 General Purpose Output is '1'

Book 0 / Page 4 / Register 71: DOUT2 (Output) Pin Control - 0x00 / 0x04 / 0x47 (B0_P4_R71)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	1	DOUT2 Bus Keeper Control 0: DOUT2 Bus Keeper Enabled 1: DOUT2 Bus Keeper Disabled
D4-D1	R/W	0 001	DOUT2 Pin Control 0000: DOUT2 pin disabled 0001: DOUT2 pin Output = ASI2 Data Output 0010: DOUT2 pin Output = General Purpose Output 0011: Reserved. Do not use. 0100: DOUT2 pin Output = INT1 Interrupt 0101: DOUT2 pin Output = INT2 Interrupt 0110: DOUT2 pin is SAR ADC interrupt as defined in B0_P3 0111-1001: Reserved. Do not use. 1010: DOUT2 pin Output = ADC_MOD_CLK Output for digital microphone 1011-1100: Reserved. Do not use. 1101: DOUT2 pin Output = L2, R2 Data Output for ASI1 (Multi-pin mode only) 1110-1111: Reserved. Do not use
D0	R/W	0	DOUT2 as General Purpose Output 0: DOUT2 General Purpose Output is '0' 1: DOUT2 General Purpose Output is '1'

Book 0 / Page 4 / Register 72: DIN2 (Input) Pin Control - 0x00 / 0x04 / 0x48 (B0_P4_R72)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D5	R/W	01	DIN2 Pin Control 00: DIN2 Disabled with input buffer powered down. 01: DIN2 Enabled with auto-power-down of input buffer if not actively used by the device. Applicable for DIN2 used as Data Input of ASI1 and ASI2, Dig_Mic_In, Low-Frequency Clock Input (LFR_CLKIN) or ISR interrupt for miniDSP. 10: DIN2 Enabled with input buffer powered on. Required for DIN2 used as a General Purpose Input and applicable for DIN2 used as Data Input of ASI1 and ASI2, Dig_Mic_In, Low-Frequency Clock Input (LFR_CLKIN) or ISR interrupt for miniDSP. 11: Reserved. Do not use.
D4	R	X	DIN2 Input Pin State, used along with DIN2 as general purpose input
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 73-74: Reserved Register - 0x00 / 0x04 / 0x49-0x4A (B0_P4_R73-74)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0100	Reserved. Write only reset values

Book 0 / Page 4 / Register 75: Reserved Register - 0x00 / 0x04 / 0x4B (B0_P4_R75)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0010 0010	Reserved. Write only reset values.

Book 0 / Page 4 / Register 76: Reserved Register - 0x00 / 0x04 / 0x4C (B0_P4_R76)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0010 0000	Reserved. Write only reset values

Book 0 / Page 4 / Register 77-85: Reserved Registers - 0x00 / 0x04 / 0x4D-0x55 (B0_P4_R77-85)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

Book 0 / Page 4 / Register 86: GPIO1 (Input or Output) Pin Control - 0x00 / 0x04 / 0x56 (B0_P4_R86)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D2	R/W	000 00	GPIO1 Pin Control 00000: GPIO1 pin input or output disabled. 00001: GPIO1 pin = Input Mode, which can be used for Data Input for ASI1, digital microphone input, clock input, general purpose input or ISR interrupt to miniDSP 00010: Reserved. Do not use. 00011: GPIO1 pin = General Purpose Output 00100: GPIO1 pin = CLKOUT Output 00101: GPIO1 pin = INT1 Interrupt Output 00110: GPIO1 pin = INT2 Interrupt Output 00111-01000: Reserved. Do not use. 01001: GPIO1 pin = SAR ADC interrupt as defined in B0_P3 01010: GPIO1 pin = ADC_MOD_CLK Output for digital microphone 01011: GPIO1 pin = Bit-Banged General Purpose Output (Value set in B0_P4_R104_D0) 01100-01101: Reserved. Do not use. 01110: GPIO1 pin = L3, R3 Data Output for ASI1 (Multi-pin mode only) 01111: GPIO1 pin = L4, R4 Data Output for ASI1 (Multi-pin mode only) 10000-10100: Reserved. Do not use. 10101: GPIO1 pin = ASI3 Bit Clock Output 10101: Reserved. Do not use. 10110: GPIO1 pin = ASI1 ADC Word Clock Output 10111: GPIO1 pin = ASI1 ADC Bit Clock Output 11000: GPIO1 pin = ASI2 ADC Word Clock Output 11001: GPIO1 pin = ASI2 ADC Bit Clock Output 11010-11111: Reserved. Do not use.
D1	R	X	GPIO1 Input Pin state, used along with GPIO1 as general purpose input
D0	R/W	0	GPIO1 as General Purpose Output 0: GPIO1 pin is driven to '0' in general purpose output mode 1: GPIO1 pin is driven to '1' in general purpose output mode

Book 0 / Page 4 / Register 87: GPIO2 (Input or Output) Pin Control - 0x00 / 0x04 / 0x57 (B0_P4_R87)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values

Book 0 / Page 4 / Register 87: GPIO2 (Input or Output) Pin Control - 0x00 / 0x04 / 0x57 (B0_P4_R87) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D2	R/W	000 00	GPIO2 Pin Control 00000: GPIO2 pin input or output disabled. 00001: GPIO2 pin = Input Mode, which can be used for Data Input for ASI1, digital microphone input, general purpose input or ISR interrupt to miniDSP. 00010: Reserved. Do not use. 00011: GPIO2 pin = General Purpose Output 00100: GPIO2 pin = CLKOUT Output 00101: GPIO2 pin = INT1 Interrupt Output 00110: GPIO2 pin = INT2 Interrupt Output 00111-01000: Reserved. Do not use. 01001: GPIO2 pin = SAR ADC interrupt as defined in B0_P3 01010: GPIO2 pin = ADC_MOD_CLK Output for digital microphone 01011: GPIO2 pin = Bit-Banged General Purpose Output (Value set in B0_P4_R104_D1) 01100: Reserved. Do not use. 01101: GPIO2 pin = L2, R2 Data Output for ASI1 (Multi-pin mode only) 01110: GPIO2 pin = L3, R3 Data Output for ASI1 (Multi-pin mode only) 01111: GPIO2 pin = L4, R4 Data Output for ASI1 (Multi-pin mode only) 10000-10011: Reserved. Do not use. 10100: GPIO2 pin = ASI3 Word Clock Output 10101: Reserved. Do not use. 10110: GPIO2 pin = ASI1 ADC Word Clock Output 10111: GPIO2 pin = ASI1 ADC Bit Clock Output 11000: GPIO2 pin = ASI2 ADC Word Clock Output 11001: GPIO2 pin = ASI2 ADC Bit Clock Output 11010-11111: Reserved. Do not use.
D1	R	X	GPIO2 Input Pin state, used along with GPIO2 as general purpose input
D0	R/W	0	GPIO2 as General Purpose Output 0: GPIO2 pin is driven to '0' in general purpose output mode 1: GPIO2 pin is driven to '1' in general purpose output mode

Book 0 / Page 4 / Register 88: GPIO3 (Input or Output) Pin Control - 0x00 / 0x04 / 0x58 (B0_P4_R88)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D2	R/W	000 00	GPIO3 Pin Control 00000: GPIO3 pin input or output disabled. 00001: GPIO3 pin = Input Mode, which can be used for Data Input for ASI1, General Purpose Input, ADC Clock Inputs for any ASI, digital microphone input, or ISR interrupt to miniDSP. 00010-00100: Reserved. Do not use. 00101: GPIO3 pin = INT1 interrupt 00110: GPIO3 pin = INT2 interrupt 00111-01001: Reserved. Do not use. 01010: GPIO3 pin = ADC_MOD_CLK Output for digital microphone 01011: GPIO3 pin = Bit-Banged General Purpose Output (Value set in B0_P4_R104_D2) 01100-10101: Reserved. Do no use. 10110: GPIO3 pin = ASI1 ADC Word Clock Output 10111: GPIO3 pin = ASI1 ADC Bit Clock Output 11000: GPIO3 pin = ASI1 ADC Word Clock Output 11001: GPIO3 pin = ASI2 ADC Bit Clock Output 11010-11111: Reserved. Do not use.
D1	R	X	GPIO3 Input Pin state, used along with GPIO3 as general purpose input
D0	R	0	Reserved. Write only reset values

Book 0 / Page 4 / Register 89: GPIO4 (Input or Output) Pin Control - 0x00 / 0x04 / 0x59 (B0_P4_R89)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values

Book 0 / Page 4 / Register 89: GPIO4 (Input or Output) Pin Control - 0x00 / 0x04 / 0x59 (B0_P4_R89) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D2	R/W	000 00	GPIO4 Pin Control 00000: GPIO4 pin input or output disabled. 00001: GPIO4 pin = Input Mode, which can be used for ADC Clock Inputs for any ASI, digital microphone input, or general purpose input. 00010-00100: Reserved. Do not use. 00101: GPIO4 pin = INT1 interrupt 00110: GPIO4 pin = INT2 interrupt 00111-01001: Reserved. Do not use. 01010: GPIO4 pin = ADC_MOD_CLK Output for digital microphone 01011: GPIO4 pin = Bit-Banged General Purpose Output (Value set in B0_P4_R104_D3) 01100-10101: Reserved. Do not use. 10110: GPIO4 pin = ASI1 ADC Word Clock Output 10111: GPIO4 pin = ASI1 ADC Bit Clock Output 11000: GPIO4 pin = ASI1 ADC Word Clock Output 11001: GPIO4 pin = ASI2 ADC Bit Clock Output 11010-11100: Reserved. Do not use. 11101: GPIO4 pin = ASI3 Data Output 11110-11111: Reserved. Do not use.
D1	R	X	GPIO4 Input Pin state, used along with GPIO4 as general purpose input
D0	R	0	Reserved. Write only reset values.

Book 0 / Page 4 / Register 90: GPIO5 (Input or Output) Pin Control - 0x00 / 0x04 / 0x5A (B0_P4_R90)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D2	R/W	000 00	GPIO5 Pin Control 00000: GPIO5 pin input or output disabled. 00001: GPIO5 pin = Input Mode, which can be used for Data Input for ASI1, or digital microphone input. 00010-01001: Reserved. Do not use. 01010: GPIO5 pin = ADC_MOD_CLK Output for digital microphone 01011-11100: Reserved. Do not use. 11101: GPIO5 pin = ASI3 Data Output 11110-11111: Reserved. Do not use.
D1	R	X	GPIO5 Input Pin state, used along with GPIO5 as general purpose input
D0	R/W	0	GPIO5 as General Purpose Output 0: GPIO5 pin is driven to '0' in general purpose output mode 1: GPIO5 pin is driven to '1' in general purpose output mode

Book 0 / Page 4 / Register 91: Reserved Register - 0x00 / 0x04 / 0x5B (B0_P4_R91)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

Book 0 / Page 4 / Register 92-95: Reserved Registers - 0x00 / 0x04 / 0x5C-0x5F (B0_P4_R92-95)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

Book 0 / Page 4 / Register 96: MISO_GPO1 (Output) Pin Control - 0x00 / 0x04 / 0x60 (B0_P4_R96)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values

Book 0 / Page 4 / Register 96: MISO_GPO1 (Output) Pin Control - 0x00 / 0x04 / 0x60 (B0_P4_R96) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D1	R/W	0 001	MISO_GPO1 Pin Control 0000: MISO_GPO1 pin output disabled 0001: MISO_GPO1 pin is used for data output in SPI interface (MISO), is disabled for I2C interface 0010: MISO_GPO1 pin is General Purpose Output 0011: MISO_GPO1 pin is CLKOUT Output 0100: MISO_GPO1 pin is INT1 Interrupt Output 0101: MISO_GPO1 pin is INT2 Interrupt Output 0110: MISO_GPO1 pin is SAR ADC interrupt as defined in B0_P3 0111: MISO_GPO1 pin is ADC_MOD_CLK Output for Digital Microphone 1000-1100: Reserved. Do not use. 1101: MISO_GPO1 pin is L2, R2 Data Ouput for ASI1 (Multi-pin mode only) 1110: MISO_GPO1 pin is L3, R3 Data Ouput for ASI1 (Multi-pin mode only) 1111: Reserved. Do not use.
D0	R/W	0	MISO_GPO1 as General Purpose Output 0: MISO_GPO1 General Purpose Output Value = 0 1: MISO_GPO1 General Purpose Output Value = 1

Book 0 / Page 4 / Register 97-99: Reserved Registers - 0x00 / 0x04 / 0x61-0x63 (B0_P4_R97-99)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 100: Digital Microphone Clock Control - 0x00 / 0x04 / 0x64 (B0_P4_R100)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Digital Microphone 1 Left Channel Clock Edge 0: Digital Microphone 1 Left Channel is latched on Rising Edge of ADC_MOD_CLK 1: Digital Microphone 1 Left Channel is latched on Falling Edge of ADC_MOD_CLK
D6	R/W	1	Digital Microphone 1 Right Channel Clock Edge 0: Digital Microphone 1 Right Channel is latched on Rising Edge of ADC_MOD_CLK 1: Digital Microphone 1 Right Channel is latched on Falling Edge of ADC_MOD_CLK
D5-D4	R	00	Reserved. Write only reset values.
D3	R/W	0	Digital Microphone 2 Left Channel Clock Edge 0: Digital Microphone 2 Left Channel is latched on Rising Edge of ADC_MOD_CLK 1: Digital Microphone 2 Left Channel is latched on Falling Edge of ADC_MOD_CLK
D2	R/W	1	Digital Microphone 2 Right Channel Clock Edge 0: Digital Microphone 2 Right Channel is latched on Rising Edge of ADC_MOD_CLK 1: Digital Microphone 2 Right Channel is latched on Falling Edge of ADC_MOD_CLK
D1-D0	R	00	Reserved. Write only reset values.

Book 0 / Page 4 / Register 101: Digital Microphone 1 Input Pin Control - 0x00 / 0x04 / 0x65 (B0_P4_R101)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0011	Digital Microphone 1 Left Data Input Control 0000: Left Channel Input is on GPIO1 pin 0001: Left Channel Input is on GPIO2 pin 0010: Left Channel Input is on GPIO3 pin 0011: Left Channel Input is on GPIO4 pin 0100: Left Channel Input is on GPIO5 pin 0101-0111: Reserved. Do not use. 1000: Left Channel Input is on DIN1 pin 1001: Left Channel Input is on DIN2 pin 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 101: Digital Microphone 1 Input Pin Control - 0x00 / 0x04 / 0x65 (B0_P4_R101) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0011	Digital Microphone 1 Right Data Input Control 0000: Right Channel Input is on GPIO1 pin 0001: Right Channel Input is on GPIO2 pin 0010: Right Channel Input is on GPIO3 pin 0011: Right Channel Input is on GPIO4 pin 0100: Right Channel Input is on GPIO5 pin 0101-0111: Reserved. Do not use. 1000: Right Channel Input is on DIN1 pin 1001: Right Channel Input is on DIN2 pin 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 102: Digital Microphone 2 Input Pin Control - 0x00 / 0x04 / 0x66 (B0_P4_R102)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0100	Digital Microphone 2 Left Data Input Control 0000: Left Channel Input is on GPIO1 pin 0001: Left Channel Input is on GPIO2 pin 0010: Left Channel Input is on GPIO3 pin 0011: Left Channel Input is on GPIO4 pin 0100: Left Channel Input is on GPIO5 pin 0101-0111: Reserved. Do not use. 1000: Left Channel Input is on DIN1 pin 1001: Left Channel Input is on DIN2 pin 1010-1111: Reserved. Do not use.
D3-D0	R/W	0100	Digital Microphone 2 Right Data Input Control 0000: Right Channel Input is on GPIO1 pin 0001: Right Channel Input is on GPIO2 pin 0010: Right Channel Input is on GPIO3 pin 0011: Right Channel Input is on GPIO4 pin 0100: Right Channel Input is on GPIO5 pin 0101-0111: Reserved. Do not use. 1000: Right Channel Input is on DIN1 pin 1001: Right Channel Input is on DIN2 pin 1011-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 103: Reserved Register - 0x00 / 0x04 / 0x67 (B0_P4_R103)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 104: Bit-Bang Output - 0x00 / 0x04 / 0x68 (B0_P4_R104)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R/W	0	GPIO4 Bit Bang Data Output 0: GPIO4 Bit Bang Data Output = 0 1: GPIO4 Bit Bang Data Output = 1
D2	R/W	0	GPIO3 Bit Bang Data Output 0: GPIO3 Bit Bang Data Output = 0 1: GPIO3 Bit Bang Data Output = 1
D1	R/W	0	GPIO2 Bit Bang Data Output 0: GPIO2 Bit Bang Data Output = 0 1: GPIO2 Bit Bang Data Output = 1
D0	R/W	0	GPIO1 Bit Bang Data Output 0: GPIO1 Bit Bang Data Output = 0 1: GPIO1 Bit Bang Data Output = 1

Book 0 / Page 4 / Register 105-106: Reserved Registers - 0x00 / 0x04 / 0x69-0x6A (B0_P4_R105-106)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 107: Bit-Bang Input - 0x00 / 0x04 / 0x6B (B0_P4_R107)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	XXXX	Reserved. Write only reset values.
D3	R	X	GPIO4 Bit Bang Data Input (Input Buffer value also shown in B0_P4_R89_D1) 0: GPIO4 Bit Bang Data Input = 0 1: GPIO4 Bit Bang Data Input = 1
D2	R	X	GPIO3 Bit Bang Data Input (Input Buffer value also shown in B0_P4_R88_D1) 0: GPIO3 Bit Bang Data Input = 0 1: GPIO3 Bit Bang Data Input = 1
D1	R	X	GPIO2 Bit Bang Data Input (Input Buffer value also shown in B0_P4_R87_D1) 0: GPIO2 Bit Bang Data Input = 0 1: GPIO2 Bit Bang Data Input = 1
D0	R	X	GPIO1 Bit Bang Data Input (Input Buffer value also shown in B0_P4_R86_D1) 0: GPIO1 Bit Bang Data Input = 0 1: GPIO1 Bit Bang Data Input = 1

Book 0 / Page 4 / Register 108-112: Reserved Registers - 0x00 / 0x04 / 0x6C-0x70 (B0_P4_R108-112)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 113: Bit-Bang miniDSP Output Control - 0x00 / 0x04 / 0x71 (B0_P4_R113)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	0	0: Use B0_P4_R104 for bit-bang of outputs GPIO1, GPIO2, GPIO3, GPIO4 or GPIO6 1: Use miniDSP_D port for bit-bang of outputs GPIO1, GPIO2, GPIO3, GPIO4 or GPIO6
D5-D0	R	00 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 114: Reserved Register - 0x00 / 0x04 / 0x72 (B0_P4_R114)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 115: ASI1, ADC Bit Clock and ADC Word Clock Output - 0x00 / 0x04 / 0x73 (B0_P4_R115)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	ASI1_ADC_BCLK_OUT mux control used for 6-wire ASI1 mode with ADC Bit Clock as output: 0000: ASI1_ADC_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 0001: Reserved. Do not use. 0010: ASI1_ADC_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 0011: ASI1_ADC_BCLK_OUT = ASI2 Bit Clock Input (ASI2_BCLK) 0100: ASI1_ADC_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 0101: ASI1_ADC_BCLK_OUT = ASI3 Bit Clock Input (ASI3_BCLK) 0110: Reserved. Do not use. 0111: ASI1_ADC_BCLK_OUT = ASI2 ADC Bit Clock Output (ASI2_ADC_BCLK) 1000-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 115: ASI1, ADC Bit Clock and ADC Word Clock Output - 0x00 / 0x04 / 0x73 (B0_P4_R115) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	ASI1_ADC_WCLK_OUT mux control used for 6-wire ASI1 mode with ADC Word Clock as output: 0000: ASI1_ADC_WCLK_OUT = Generated DAC_FS 0001: ASI1_ADC_WCLK_OUT = Generated ADC_FS 0010: ASI1_ADC_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 0011: Reserved. Do not use. 0100: ASI1_ADC_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 0101: ASI1_ADC_WCLK_OUT = ASI2 Word Clock Input (ASI2_WCLK) 0110: ASI1_ADC_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 0111: ASI1_ADC_WCLK_OUT = ASI3 Word Clock Input (ASI3_WCLK) 1000: Reserved. Do not use. 1001: ASI1_ADC_WCLK_OUT = ASI2 ADC Word Clock 1010-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 116: ASI2, ADC Bit Clock and ADC Word Clock Output - 0x00 / 0x04 / 0x74 (B0_P4_R116)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	ASI2_ADC_BCLK_OUT mux control used for 6-wire ASI1 mode with ADC Bit Clock as output: 0000: ASI2_ADC_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 0001: ASI2_ADC_BCLK_OUT = ASI1 Bit Clock Input (ASI1_BCLK) 0010: ASI2_ADC_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 0011: Reserved. Do not use. 0100: ASI2_ADC_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 0101: ASI2_ADC_BCLK_OUT = ASI3 Bit Clock Input (ASI3_BCLK) 0110: ASI2_ADC_BCLK_OUT = ASI1 ADC Bit Clock Output (ASI1_ADC_BCLK) 0111-1111: Reserved. Do not use.
D3-D0	R/W	0000	ASI2_ADC_WCLK_OUT mux control used for 6-wire ASI1 mode with ADC Word Clock as output: 0000: ASI2_ADC_WCLK_OUT = Generated DAC_FS 0001: ASI2_ADC_WCLK_OUT = Generated ADC_FS 0010: ASI2_ADC_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 0011: ASI2_ADC_WCLK_OUT = ASI1 Word Clock Input (ASI1_WCLK) 0100: ASI2_ADC_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 0101: Reserved. Do not use. 0110: ASI2_ADC_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 0111: ASI2_ADC_WCLK_OUT = ASI3 Word Clock Input (ASI3_WCLK) 1000: ASI2_ADC_WCLK_OUT = ASI1 ADC Word Clock 1001-1111: Reserved. Do not use.

Book 0 / Page 4 / Register 117: ASI3, ADC Bit Clock and ADC Word Clock Output - 0x00 / 0x04 / 0x75 (B0_P4_R117)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	Reserved. Write only default values.
D3-D0	R/W	0000	Reserved. Write only default values

Book 0 / Page 4 / Register 118: miniDSP Data Port Control - 0x00 / 0x04 / 0x76 (B0_P4_R118)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	0	ADC miniDSP Data Output Configuration 0: Independent Left and Right Channels for ADC miniDSP output 1: Left Channel of ADC miniDSP output copied to Right Channel miniDSP output that is miniDSP_A_DataOutput[2] = miniDSP_A_DataOutput[1]
D5-D4	R/W	00	miniDSP_D_DataInput_1 Configuration 00: miniDSP_D_DataInput_1[1:8] receives data from ASI1_DataInput[1:8] 01: miniDSP_D_DataInput_1[1:2] receives data from ASI2_DataInput[1:2] 10: miniDSP_D_DataInput_1[1:2] receives data from ASI3_DataInput[1:2] 11: miniDSP_D_DataInput_1[1:8] receives data from miniDSP_A_DataOutput[1:8] (ADC-to-DAC Loopback)

Book 0 / Page 4 / Register 118: miniDSP Data Port Control - 0x00 / 0x04 / 0x76 (B0_P4_R118) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D2	R/W	01	miniDSP_D_DataInput_2 Configuration 00: miniDSP_D_DataInput_2[1:2] receives data from ASI1_DataInput[1:2] 01: miniDSP_D_DataInput_2[1:2] receives data from ASI2_DataInput[1:2] 10: miniDSP_D_DataInput_2[1:2] receives data from ASI3_DataInput[1:2] 11: Reserved. Do not use.
D1-D0	R/W	10	miniDSP_D_Data Input 3 Configuration 00: miniDSP_D_DataInput_3[1:2] receives data from ASI1_DataInput[1:2] 01: miniDSP_D_DataInput_3[1:2] receives data from ASI2_DataInput[1:2] 10: miniDSP_D_DataInput_3[1:2] receives data from ASI3_DataInput[1:2] 11: Reserved. Do not use.

Book 0 / Page 4 / Register 119: Digital Audio Engine Synchronization Control - 0x00 / 0x04 / 0x77 (B0_P4_R119)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	DAC Engine Synchronization: 00: Enable DAC engine syncing using ASI1 01: Enable DAC engine syncing using ASI2 10: Enable DAC engine syncing using ASI3 11: Disable DAC engine syncing with miniDSP_D_in data frame from ASI mux at power up. Recommended to disable sync when not using programmble mode for miniDSP_D (when B0_P0_R60_D[4:0] /= "0 0000")
D5-D4	R/W	00	ADC Engine Synchronization: 00: Enable ADC engine syncing using ASI1 01: Enable ADC engine syncing using ASI2 10: Enable ADC engine syncing using ASI3 11: Disable ADC engine syncing with miniDSP_A_in data frame from ASI mux at power up
D3-D0	R	0000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 120-127: Reserved Registers - 0x00 / 0x04 / 0x78-0x7F (B0_P4_R120-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	Reserved. Write only reset values.

8.6.6 Book 0 Page 252

Book 0 / Page 252 / Register 0: Page Select Register - 0x00 / 0xFC / 0x00 (B0_P252_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

Book 0 / Page 252 / Register 1: SAR Buffer Mode Data (MSB) and Buffer Flags - 0x00 / 0xFC / 0x01 (B0_P252_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Buffer-Full Flag 0: 64-sample Buffer is not filled 1: 64-sample Buffer has been filled
D6	R	1	Buffer-Empty Flag 0: Buffer still contains un-read data 1: Buffer is empty (contains no un-read data)
D5	R	X	Reserved. Write only reset values.

Book 0 / Page 252 / Register 1: SAR Buffer Mode Data (MSB) and Buffer Flags - 0x00 / 0xFC / 0x01 (B0_P252_R1) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R	X	Data Identification: 0: VBAT or IN1R/AUX2 data found in SAR Buffer Data (that is B0_P252_R1_D[3:0] and B0_P252_R2_D[7:0]. 1: IN1L/AUX1 or TEMP data found in SAR Buffer Data (that is B0_P252_R1_D[3:0] and B0_P252_R2_D[7:0].
D3-D0	R	XXXX	SAR ADC Buffer Mode Data (11:8) - Reading this register will return MSB 4 bits of SAR Buffer Mode data (based on Read Pointer).

Book 0 / Page 252 / Register 2: SAR Buffer Mode Data (LSB) - 0x00 / 0xFC / 0x02 (B0_P252_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	SAR ADC Buffer Mode Data (7:0) - Reading this register will return LSB 8 bits of SAR Buffer Mode data (based on Read Pointer).

Book 0 / Page 252 / Register 3-127: Reserved Registers - 0x00 / 0xFC / 0x03-0x7F (B0_P252_R3-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

8.6.7 Book 20 Page 0

Book 20 / Page 0 / Register 0: Page Select Register - 0x14 / 0x00 / 0x00 (B20_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 20 / Page 0 / Register 1-126: Reserved Registers - 0x14 / 0x00 / 0x01-0x7E (B20_P0_R1-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 20 / Page 0 / Register 127: Book Selection Register - 0x14 / 0x00 / 0x7F (B20_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.8 Book 20 Page 1-26

Book 20 / Page 1-26 / Register 0: Page Select Register - 0x14 / 0x01-0x1A / 0x00 (B20_P1-26_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 20 / Page 1-26 / Register 1-7: Reserved Registers - 0x14 / 0x01-0x1A / 0x01-0x07 (B20_P1-26_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 20 / Page 1-26 / Register 8-127: ADC Fixed Coefficients C(0:767) - 0x14 / 0x01-0x1A / 0x08-0x7F (B20_P1-26_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Fixed Coefficient. Refer to Table "ADC Fixed Coefficient Map" for details.

8.6.9 Book 40 Page 0

Book 40 / Page 0 / Register 0: Page Select Register - 0x28 / 0x00 / 0x00 (B40_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 40 / Page 0 / Register 1: ADC Adaptive CRAM Configuration Register - 0x28 / 0x00 / 0x01 (B40_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R	0	miniDSP_A Generated Flag for toggling MSB Bit of Coefficient Address
D2	R/W	0	ADC Adaptive Filtering Control 0: Adaptive Filtering disabled for ADC 1: Adaptive Filtering enabled for ADC
D1	R	0	ADC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, ADC miniDSP accesses ADC Coefficient Buffer-A, and control interface accesses ADC Coefficient Buffer-B 1: In adaptive filter mode, ADC miniDSP accesses ADC Coefficient Buffer-B, and control interface accesses ADC Coefficient Buffer-A
D0	R/W	0	ADC Adaptive Filter Buffer Switch control 0: ADC Coefficient Buffers will not be switched at next frame boundary 1: ADC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

Book 40 / Page 0 / Register 2-126: Reserved Registers - 0x28 / 0x00 / 0x02-0x7E (B40_P0_R2-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 40 / Page 0 / Register 127: Book Selection Register - 0x28 / 0x00 / 0x7F (B40_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.10 Book 40 Page 1-17

Book 40 / Page 1-17 / Register 0: Page Select Register - 0x28 / 0x01-0x11 / 0x00 (B40_P1-17_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 40 / Page 1-17 / Register 1-7: Reserved Registers - 0x28 / 0x01-0x11 / 0x01-0x07 (B40_P1-17_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 40 / Page 1-17 / Register 8-127: ADC Adaptive Coefficients C(0:509) - 0x28 / 0x01-0x11 / 0x08-0x7F (B40_P1-17_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficients. Refer to Tables "ADC Adaptive Coefficient Buffer-A Map" and "ADC Adaptive Coefficient Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, ADC Coefficients are one contiguous block.

8.6.11 Book 40 Page 18

Book 40 / Page 18 / Register 0: Page Select Register - 0x28 / 0x12 / 0x00 (B40_P18_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 40 / Page 18 / Register 1-7: Reserved Registers - 0x28 / 0x12 / 0x01-0x07 (B40_P18_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 40 / Page 18 / Register 8-15: ADC Adaptive Coefficients C(510:511) - 0x28 / 0x12 / 0x08-0x0F (B40_P18_R8-15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficients. Refer to Tables "ADC Adaptive Coefficient Buffer-A Map" and "ADC Adaptive Coefficient Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, ADC Coefficients are one contiguous block.

Book 40 / Page 18 / Register 16-127: Reserved Registers - 0x28 / 0x12 / 0x10-0x7F (B40_P18_R16-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

8.6.12 Book 60 Page 0

Book 60 / Page 0 / Register 0: Page Select Register - 0x3C / 0x00 / 0x00 (B60_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 60 / Page 0 / Register 1-126: Reserved Registers - 0x3C / 0x00 / 0x01-0x7E (B60_P0_R1-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 60 / Page 0 / Register 127: Book Selection Register - 0x3C / 0x00 / 0x7F (B60_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.13 Book 60 Page 1-35

Book 60 / Page 1-35 / Register 0: Page Select Register - 0x3C / 0x01-0x23 / 0x00 (B60_P1-35_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 60 / Page 1-35 / Register 1-7: Reserved Registers - 0x3C / 0x01-0x23 / 0x01-0x07 (B60_P1-35_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 60 / Page 1-35 / Register 8-127: DAC Fixed Coefficients C(0:1023) - 0x3C / 0x01-0x23 / 0x08-0x7F (B60_P1-35_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Fixed Coefficient. Refer to Table "DAC Fixed Coefficient Map" for details.

8.6.14 Book 80 Page 0

Book 80 / Page 0 / Register 0: Page Select Register - 0x50 / 0x00 / 0x00 (B80_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 80 / Page 0 / Register 1: DAC Adaptive Coefficient Bank 1 Configuration Register - 0x50 / 0x00 / 0x01 (B80_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R	0	miniDSP_D Generated Flag for toggling MSB Bit of Coefficient Address
D2	R/W	0	DAC Bank 1 Adaptive Filtering Control 0: Adaptive Filtering disabled for DAC Adaptive Coefficient Bank 1 1: Adaptive Filtering enabled for DAC Adaptive Coefficient Bank 1
D1	R	0	DAC Bank 1 Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC miniDSP accesses DAC Coefficient Bank 1 Buffer-A, and control interface accesses DAC Coefficient Bank 1 Buffer-B 1: In adaptive filter mode, DAC miniDSP accesses DAC Coefficient Bank 1 Buffer-B, and control interface accesses DAC Coefficient Bank 1 Buffer-A
D0	R/W	0	DAC Bank 1 Adaptive Filter Buffer Switch control 0: DAC Coefficient Bank 1 Buffers will not be switched at next frame boundary 1: DAC Coefficient Bank 1 Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

Book 80 / Page 0 / Register 2-126: Reserved Registers - 0x50 / 0x00 / 0x02-0x7E (B80_P0_R2-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 80 / Page 0 / Register 127: Book Selection Register - 0x50 / 0x00 / 0x7F (B80_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.15 Book 80 Page 1-17

Book 80 / Page 1-17 / Register 0: Page Select Register - 0x50 / 0x01-0x11 / 0x00 (B80_P1-17_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 80 / Page 1-17 / Register 1-7: Reserved Registers - 0x50 / 0x01-0x11 / 0x01-0x07 (B80_P1-17_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 80 / Page 1-17 / Register 8-127: DAC Adaptive Coefficient Bank 1 C(0:509) - 0x50 / 0x01-0x11 / 0x08-0x7F (B80_P1-17_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank 1. Refer to Tables "DAC Adaptive Coefficient Bank 1 Buffer-A Map" and "DAC Adaptive Coefficient Bank 1 Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

8.6.16 Book 80 Page 18

Book 80 / Page 18 / Register 0: Page Select Register - 0x50 / 0x12 / 0x00 (B80_P18_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 80 / Page 18 / Register 1-7: Reserved Registers - 0x50 / 0x12 / 0x01-0x07 (B80_P18_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 80 / Page 18 / Register 8-15: DAC Adaptive Coefficient Bank 1 C(510:511) - 0x50 / 0x12 / 0x08-0x0F (B80_P18_R8-15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank 1. Refer to Tables "DAC Adaptive Coefficient Bank 1 Buffer-A Map" and "DAC Adaptive Coefficient Bank 1 Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

Book 80 / Page 18 / Register 16-127: Reserved Registers - 0x50 / 0x12 / 0x10-0x7F (B80_P18_R16-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

8.6.17 Book 82 Page 0

Book 82 / Page 0 / Register 0: Page Select Register - 0x52 / 0x00 / 0x00 (B82_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 82 / Page 0 / Register 1: DAC Adaptive Coefficient Bank 2 Configuration Register - 0x52 / 0x00 / 0x01 (B82_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R	0	miniDSP_D Generated Flag for toggling MSB Bit of Coefficient Address
D2	R/W	0	DAC Coefficient Bank 2 Adaptive Filtering Control 0: Adaptive Filtering disabled for DAC Adaptive Coefficient Bank 2 1: Adaptive Filtering enabled for DAC Adaptive Coefficient Bank 2
D1	R	0	DAC Coefficient Bank 2 Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC miniDSP accesses DAC Coefficient Bank 2 Buffer-A, and control interface accesses DAC Coefficient Bank 2 Buffer-B 1: In adaptive filter mode, DAC miniDSP accesses DAC Coefficient Bank 2 Buffer-B, and control interface accesses DAC Coefficient Bank 2 Buffer-A
D0	R/W	0	DAC Coefficient Bank 2 Adaptive Filter Buffer Switch control 0: DAC Coefficient Bank 2 Buffers will not be switched at next frame boundary 1: DAC Coefficient Bank 2 Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

Book 82 / Page 0 / Register 2-126: Reserved Registers - 0x52 / 0x00 / 0x02-0x7E (B82_P0_R2-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

Book 82 / Page 0 / Register 127: Book Selection Register - 0x52 / 0x00 / 0x7F (B82_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.18 Book 82 Page 1-17

Book 82 / Page 1-17 / Register 0: Page Select Register - 0x52 / 0x01-0x11 / 0x00 (B82_P1-17_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 82 / Page 1-17 / Register 1-7: Reserved Registers - 0x52 / 0x01-0x11 / 0x01-0x07 (B82_P1-17_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 82 / Page 1-17 / Register 8-127: DAC Adaptive Coefficient Bank 2 C(0:509) - 0x52 / 0x01-0x11 / 0x08-0x7F (B82_P1-17_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank 2. Refer to Tables "DAC Adaptive Coefficient Bank 2 Buffer-A Map" and "DAC Adaptive Coefficient Bank 2 Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

8.6.19 Book 82 Page 18

Book 82 / Page 18 / Register 0: Page Select Register - 0x52 / 0x12 / 0x00 (B82_P18_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 82 / Page 18 / Register 1-7: Reserved Registers - 0x52 / 0x12 / 0x01-0x07 (B82_P18_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 82 / Page 18 / Register 8-15: DAC Adaptive Coefficient Bank 2 C(510:511) - 0x52 / 0x12 / 0x08-0x0F (B82_P18_R8-15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank 2. Refer to Tables "DAC Adaptive Coefficient Bank 2 Buffer-A Map" and "DAC Adaptive Coefficient Bank 2 Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

Book 82 / Page 18 / Register 16-127: Reserved Registers - 0x52 / 0x12 / 0x10-0x7F (B82_P18_R16-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

8.6.20 Book 100 Page 0

Book 100 / Page 0 / Register 0: Page Select Register - 0x64 / 0x00 / 0x00 (B100_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 100 / Page 0 / Register 1-46: Reserved Registers - 0x64 / 0x00 / 0x01-0x2E (B100_P0_R1-46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 100 / Page 0 / Register 47: Non-Programmable Override Options - 0x64 / 0x00 / 0x2F (B100_P0_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1	W	0	0: Use the hardwired IADC and DECIM value for the specific non-programmable mode 1: Use IADC value and DECIM value from register B100_P0_R48-50 for the non-programmable mode
D0	R	0	Reserved. Write only reset values.

Book 100 / Page 0 / Register 48: ADC miniDSP_A Instruction Control Register 1 - 0x64 / 0x00 / 0x30 (B100_P0_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0001	ADC miniDSP IADC (14:8) Control. (Use only when ADC miniDSP_A is in use for signal processing, that is B0_P0_R61_D[4:0]=00000.) ADC miniDSP IADC(14:0) 000 0000 0000 0000: ADC miniDSP IADC=32768 000 0000 0000 0001: ADC miniDSP IADC = 1 000 0000 0000 0010: ADC miniDSP IADC = 2 ... 111 1111 1111 1110: ADC miniDSP IADC = 32766 111 1111 1111 1111: ADC miniDSP IADC = 32767 Note: IADC should be a integral multiple of DECIM (B100_P0_R50_D[3:0]) Note: B100_P0_R48 takes effect after programming B100_P0_R49 in the immediate next control command.

Book 100 / Page 0 / Register 49: ADC miniDSP_A Instruction Control Register 2 - 0x64 / 0x00 / 0x31 (B100_P0_R49)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ADC miniDSP IADC (14:8) Control. (Use only when ADC miniDSP_A is in use for signal processing, that is B0_P0_R61_D[4:0]=00000.) ADC miniDSP IADC(14:0) 000 0000 0000 0000: ADC miniDSP IADC=32768 000 0000 0000 0001: ADC miniDSP IADC = 1 000 0000 0000 0010: ADC miniDSP IADC = 2 ... 111 1111 1111 1110: ADC miniDSP IADC = 32766 111 1111 1111 1111: ADC miniDSP IADC = 32767 Note: IADC should be a integral multiple of DECIM (B100_P0_R50_D[3:0]) Note: B100_P0_R48 takes effect after programming B100_P0_R49 in the immediate next control command.

Book 100 / Page 0 / Register 50: ADC miniDSP_A CIC Input and Decimation Ratio Control Register - 0x64 / 0x00 / 0x32 (B100_P0_R50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: FIFO at CIC output is bypassed. 1: FIFO at CIC output is not bypassed. THIS BIT SHOULD ALWAYS BE WRITTEN TO 1 AT INITIALIZATION
D6-D4	R/W	0	Reserved. Write only default values
D3-D0	R/W	0100	ADC miniDSP Decimation factor Control. (Use only when ADC miniDSP_A is in use for signal processing, that is B0_P0_R61_D[4:0]=00000.) (B0_P0_R61) 0000: Decimation factor in ADC miniDSP = 16 0001: Decimation factor in ADC miniDSP = 1 0010: Decimation factor in ADC miniDSP = 2 ... 1110: Decimation factor in ADC miniDSP = 14 1111: Decimation factor in ADC miniDSP = 15

Book 100 / Page 0 / Register 51-59: Reserved Registers - 0x64 / 0x00 / 0x33-0x3B (B100_P0_R51-59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 100 / Page 0 / Register 60: ADC miniDSP_A Secondary CIC Input Control - 0x64 / 0x00 / 0x3C (B100_P0_R60)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: FIFO at CIC2 output is bypassed. 1: FIFO at CIC2 output is not bypassed.
D6-D0	R/W	000 0000	Reserved. Write only reset values.

Book 100 / Page 0 / Register 61: miniDSP_A to Audio Serial Interface Handoff Control - 0x64 / 0x00 / 0x3D (B100_P0_R61)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: miniDSP_A to ASI1 handoff synchronizer logic is initiated based on instruction counter-3 1: miniDSP_A to ASI1 handoff synchronizer logic is initiated based on interrupt port. Use only if B0_P0_R61_D[4:0] = "0 0000".
D6	R/W	0	0: miniDSP_A to ASI2 handoff synchronizer logic is initiated based on instruction counter-3 1: miniDSP_A to ASI2 handoff synchronizer logic is initiated based on interrupt port. Use only if B0_P0_R61_D[4:0] = "0 0000".

Book 100 / Page 0 / Register 61: miniDSP_A to Audio Serial Interface Handoff Control - 0x64 / 0x00 / 0x3D (B100_P0_R61) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	0: miniDSP_A to ASI3 handoff synchronizer logic is initiated based on instruction counter-3 1: miniDSP_A to ASI3 handoff synchronizer logic is initiated based on interrupt port. Use only if B0_P0_R61_D[4:0] = "0 0000".
D4-D0	R/W	0 0000	Reserved. Write only reset values.

Book 100 / Page 0 / Register 62-126: Reserved Registers - 0x64 / 0x00 / 0x3E-0x7E (B100_P0_R62-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 100 / Page 0 / Register 127: Book Selection Register - 0x64 / 0x00 / 0x7F (B100_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.21 Book 100 Page 1-52

Book 100 / Page 1-52 / Register 0: Page Select Register - 0x64 / 0x01-0x34 / 0x00 (B100_P1-52_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 100 / Page 1-52 / Register 1-7: Reserved Registers - 0x64 / 0x01-0x34 / 0x01-0x07 (B100_P1-52_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

Book 100 / Page 1-52 / Register 8-127: miniDSP_A Instructions - 0x64 / 0x01-0x34 / 0x08-0x7F (B100_P1-52_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	32 bit instructions for ADC miniDSP engine. For details refer to Table "ADC miniDSP Instruction Map". These instructions control the operation of ADC miniDSP mode. When the fully programmable miniDSP mode is enabled and ADC channel is powered up, the read and write access to these registers is disabled.

8.6.22 Book 120 Page 0

Book 120 / Page 0 / Register 0: Page Select Register - 0x78 / 0x00 / 0x00 (B120_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 120 / Page 0 / Register 1-46: Reserved Registers - 0x78 / 0x00 / 0x01-0x2E (B120_P0_R1-46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

Book 120 / Page 0 / Register 47: Non-Programmable Override Options - 0x78 / 0x00 / 0x2F (B120_P0_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1	W	0	0: Use the hardwired IDAC and INTERP value for the specific non-programmable mode 1: Use IDAC value and INTERP value from register B120_P0_R48-50 for the non-programmable mode
D0	R	0	Reserved. Write only reset values.

Book 120 / Page 0 / Register 48: DAC miniDSP_D Instruction Control Register 1 - 0x78 / 0x00 / 0x30 (B120_P0_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0010	DAC miniDSP IDAC (14:8) Control. (Use only when DAC miniDSP_D is in use for signal processing, that is B0_P0_R60_D[4:0]=00000.) DAC miniDSP IDAC(14:0) 000 0000 0000 0000: DAC miniDSP IDAC = 32768 000 0000 0000 0001: DAC miniDSP IDAC = 1 000 0000 0000 0010: DAC miniDSP IDAC = 2 ... 111 1111 1111 1110: DAC miniDSP IDAC = 32766 111 1111 1111 1111: DAC miniDSP IDAC = 32767 Note: IDAC should be a integral multiple of INTERP (B120_P0_R50_D[3:0]) Note: B120_P0_R48 takes effect after programming B120_P0_R49 in the immediate next control command.

Book 120 / Page 0 / Register 49: DAC miniDSP_D Instruction Control Register 2 - 0x78 / 0x00 / 0x31 (B120_P0_R49)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	DAC miniDSP IDAC (7:0) Control. (Use only when DAC miniDSP_D is in use for signal processing, that is B0_P0_R60_D[4:0]=00000.) DAC miniDSP IDAC(14:0) 000 0000 0000 0000: DAC miniDSP IDAC = 32768 000 0000 0000 0001: DAC miniDSP IDAC = 1 000 0000 0000 0010: DAC miniDSP IDAC = 2 ... 111 1111 1111 1110: DAC miniDSP IDAC = 32766 111 1111 1111 1111: DAC miniDSP IDAC = 32767 Note: IDAC should be a integral multiple of INTERP (B120_P0_R50_D[3:0]) Note: B120_P0_R49 should be programmed immediately after B120_P0_R48.

Book 120 / Page 0 / Register 50: DAC miniDSP_D Interpolation Factor Control Register - 0x78 / 0x00 / 0x32 (B120_P0_R50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: FIFO at modulator input is bypassed 1: FIFO at modulator input is not bypassed. THIS BIT SHOULD ALWAYS BE WRITTEN TO 1 AT INITIALIZATION
D6-D4	R/W	000	Reserved. Write only default values.

Book 120 / Page 0 / Register 50: DAC miniDSP_D Interpolation Factor Control Register - 0x78 / 0x00 / 0x32 (B120_P0_R50) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	1000	miniDSP_D interpolation factor control. (Use only when DAC miniDSP is in use for signal processing, that is B0_P0_R60_D[4:0]=00000.) 0000: Interpolation Ratio in DAC MAC Engine = 16 0001: Interpolation Ratio in DAC MAC Engine = 1 0010: Interpolation Ratio in DAC MAC Engine = 2 ... 1110: Interpolation Ratio in DAC MAC Engine = 14 1111: Interpolation Ratio in DAC MAC Engine = 15

Book 120 / Page 0 / Register 51-126: Reserved Registers - 0x78 / 0x00 / 0x33-0x7E (B120_P0_R51-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only default values.

Book 120 / Page 0 / Register 127: Book Selection Register - 0x78 / 0x00 / 0x7F (B120_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

8.6.23 Book 120 Page 1-103

Book 120 / Page 1-103 / Register 0: Page Select Register - 0x78 / 0x01-0x67 / 0x00 (B120_P1-103_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

Book 120 / Page 1-103 / Register 1-7: Reserved Registers - 0x78 / 0x01-0x67 / 0x01-0x07 (B120_P1-103_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

Book 120 / Page 1-103 / Register 8-127: miniDSP_D Instructions - 0x78 / 0x01-0x67 / 0x08-0x7F (B120_P1-103_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	XXXX XXXX	32 bit instructions for DAC miniDSP engine. For details refer to Table "DAC miniDSP Instruction Map". These instructions control the operation of DAC miniDSP mode. When the fully programmable miniDSP mode is enabled and DAC channel is powered up, the read and write access to these registers is disabled.

8.6.24 ADC Coefficients

Table 53. ADC Fixed Coefficient Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	20	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	20	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 53. ADC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
		..	..	..	..	..	..
C29	20	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	20	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	20	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	20	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	20	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	20	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	20	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	20	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	20	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	20	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	20	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	20	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	20	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	20	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	20	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	20	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C269	20	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C270	20	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C299	20	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C300	20	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C329	20	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C330	20	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C359	20	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C360	20	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C389	20	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C390	20	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C419	20	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C420	20	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C449	20	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C450	20	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C479	20	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 53. ADC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C480	20	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C509	20	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C510	20	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C539	20	18	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C540	20	19	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C569	20	19	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C570	20	20	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C599	20	20	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C600	20	21	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C629	20	21	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C630	20	22	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C659	20	22	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C660	20	23	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C689	20	23	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C690	20	24	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C719	20	24	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C720	20	25	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C749	20	25	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C750	20	26	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C767	20	26	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 54. ADC Adaptive Coefficient Buffer-A Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	40	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	40	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	40	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	40	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	40	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	40	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	40	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	40	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	40	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 54. ADC Adaptive Coefficient Buffer-A Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C120	40	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	40	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	40	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	40	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	40	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	40	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	40	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	40	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	40	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C255	40	9	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 55. ADC Adaptive Coefficient Buffer-B Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	40	9	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	40	9	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C13	40	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C14	40	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C43	40	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C44	40	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C73	40	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C74	40	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C103	40	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C104	40	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C133	40	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C134	40	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C163	40	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C164	40	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C193	40	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C194	40	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C223	40	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C224	40	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C253	40	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 55. ADC Adaptive Coefficient Buffer-B Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C254	40	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C255	40	18	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

8.6.25 ADC Defaults

Table 56. Default values of ADC Coefficients in Buffers A and B

ADC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	01170000H
C2	01170000H
C3	7DD30000H
C4	7FFFFF00H
C5,C6	00000000H
C7	7FFFFF00H
C8,..,C11	00000000H
C12	7FFFFF00H
C13,..,C16	00000000H
C17	7FFFFF00H
C18,..,C21	00000000H
C22	7FFFFF00H
C23,..,C26	00000000H
C27	7FFFFF00H
C28,..,C35	00000000H
C36	7FFFFF00H
C37,C38	00000000H
C39	7FFFFF00H
C40,..,C43	00000000H
C44	7FFFFF00H
C45,..,C48	00000000H
C49	7FFFFF00H
C50,..,C53	00000000H
C54	7FFFFF00H
C55,..,C58	00000000H
C59	7FFFFF00H
C60,..,C253	00000000H
C254	04280000H
C255	01000000H

8.6.26 DAC Coefficients

Table 57. DAC Fixed Coefficient Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	60	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	60	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 57. DAC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
		..	..	..	..	..	..
C29	60	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	60	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	60	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	60	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	60	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	60	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	60	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	60	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	60	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	60	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	60	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	60	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	60	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	60	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	60	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	60	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C269	60	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C270	60	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C299	60	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C300	60	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C329	60	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C330	60	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C359	60	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C360	60	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C389	60	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C390	60	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C419	60	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C420	60	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C449	60	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C450	60	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C479	60	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 57. DAC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C480	60	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C509	60	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C510	60	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C539	60	18	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C540	60	19	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C569	60	19	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C570	60	20	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C599	60	20	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C600	60	21	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C629	60	21	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C630	60	22	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C659	60	22	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C660	60	23	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C689	60	23	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C690	60	24	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C719	60	24	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C720	60	25	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C749	60	25	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C750	60	26	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C779	60	26	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C780	60	27	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C809	60	27	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C810	60	28	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C839	60	28	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C840	60	29	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C869	60	29	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C870	60	30	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C899	60	30	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C900	60	31	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C929	60	31	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C930	60	32	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..

Table 57. DAC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C959	60	32	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C960	60	33	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C989	60	33	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C990	60	34	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C1019	60	34	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1020	60	35	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C1023	60	35	20	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 58. DAC Adaptive Coefficient Bank 1 Buffer-A Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	80	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	80	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	80	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	80	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	80	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	80	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	80	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	80	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	80	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	80	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	80	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	80	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	80	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	80	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	80	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	80	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	80	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	80	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C255	80	9	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 59. DAC Adaptive Coefficient Bank 1 Buffer-B Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	80	9	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 59. DAC Adaptive Coefficient Bank 1 Buffer-B Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C1	80	9	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C13	80	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C14	80	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C43	80	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C44	80	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C73	80	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C74	80	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C103	80	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C104	80	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C133	80	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C134	80	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C163	80	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C164	80	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C193	80	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C194	80	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C223	80	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C224	80	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C253	80	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C254	80	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C255	80	18	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 60. DAC Adaptive Coefficient Bank 2 Buffer-A Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	82	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	82	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	82	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	82	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	82	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	82	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	82	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	82	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	82	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	82	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 60. DAC Adaptive Coefficient Bank 2 Buffer-A Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
		..	..	..	..	..	..
C149	82	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	82	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	82	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	82	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	82	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	82	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	82	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	82	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C255	82	9	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 61. DAC Adaptive Coefficient Bank 2 Buffer-B Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	82	9	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	82	9	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C13	82	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C14	82	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C43	82	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C44	82	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C73	82	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C74	82	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C103	82	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C104	82	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C133	82	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C134	82	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C163	82	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C164	82	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C193	82	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C194	82	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C223	82	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C224	82	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C253	82	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C254	82	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 61. DAC Adaptive Coefficient Bank 2 Buffer-B Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C255	82	18	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

8.6.27 DAC Defaults

Table 62. Default values of DAC Coefficients Bank 1 and Bank 2 in Buffers A and B

DAC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	7FFFFF00H
C2,C3	00000000H
C4	7FFFFF00H
C5,..,C8	00000000H
C9	7FFFFF00H
C10,..,C13	00000000H
C14	7FFFFF00H
C15,..,C18	00000000H
C19	7FFFFF00H
C20,..,C23	00000000H
C24	7FFFFF00H
C25,..,C28	00000000H
C29	7FFFFF00H
C30,..,C35	00000000H
C36	7FFFFF00H
C37,C38	00000000H
C39	7FFFFF00H
C40,..,C43	00000000H
C44	7FFFFF00H
C45,..,C48	00000000H
C49	7FFFFF00H
C50,..,C53	00000000H
C54	7FFFFF00H
C55,..,C58	00000000H
C59	7FFFFF00H
C60,..,C63	00000000H
C64	7FFFFF00H
C65,..,C70	00000000H
C71	7FF70000H
C72	80090000H
C73	7FEF0000H
C74,C75	00110000H
C76	7FDE0000H
C77,..,C253	00000000H
C254	01180000H
C255	04400000H

9 Applications and Implementation

9.1 Application Information

The TLV320AIC3268 is a highly integrated stereo audio codec with integrated miniDSP, mono Speaker amplifier and mutiple digital audio interfaces. It enables many different types of audio platforms having a need for stereo audio record and playback and needing to interface with several other devices in the system over multiple digital audio interfaces.

9.2 Typical Applications

Figure 109 shows a typical circuit configuration for a system utilizing the TLV320AIC3268.

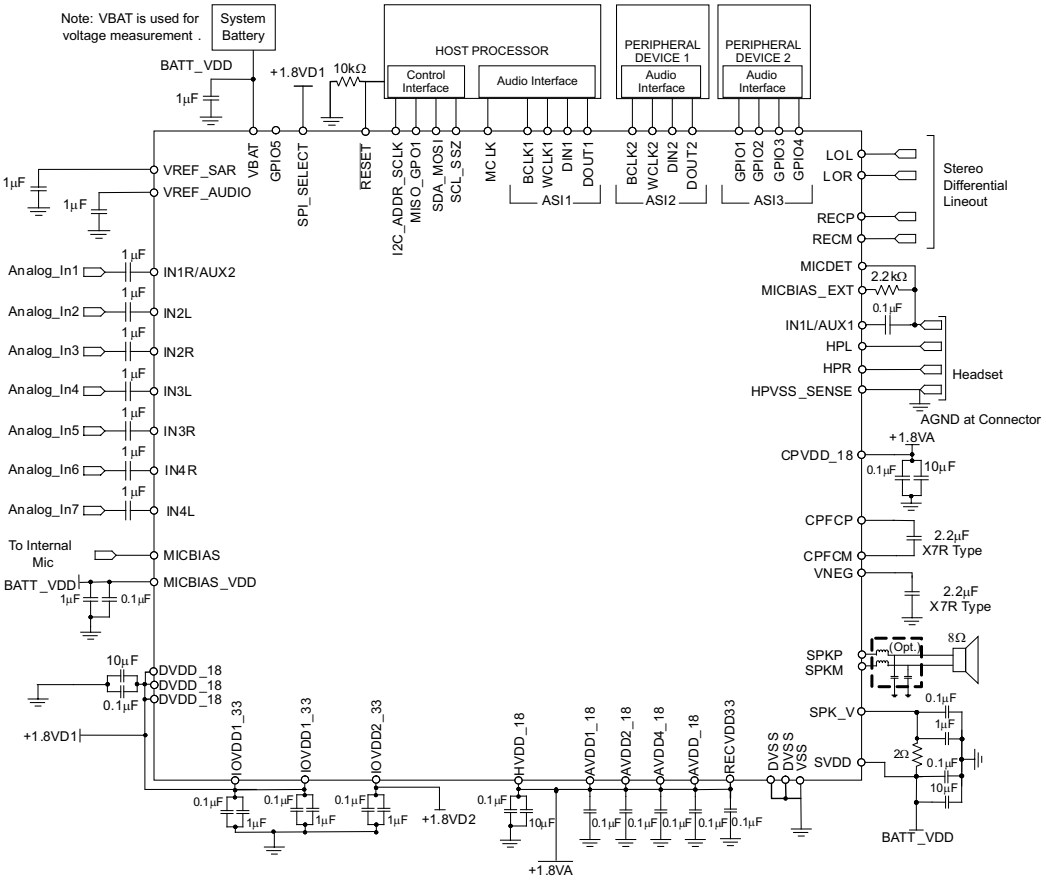


Figure 109. Typical Circuit Configuration

9.2.1 Design Requirements

9.2.1.1 Charge Pump Flying and Holding Capacitor

The TLV320AIC3268 features a built in charge-pump to generate a negative supply rail, VNEG from CPVDD_18. This negative voltage is used by the headphone amplifier to enable driving the output signal biased around ground potential. For proper operation of the charge pump and headphone amplifier, it is recommended that the flying capacitor connected between CPFCP and CPFCM terminals and the holding capacitor connected between VNEG and ground be of X7R type. It is recommended to use 2.2µF as capacitor values. Failure to use X7R type capacitor can result in degraded performance of charge pump and headphone amplifier.

9.2.1.2 Reference Fitlering Capacitor

The TLV320AIC3268 has a built-in bandgap used to generate reference voltages and currents for the device. To acheive high SNR, the reference voltage on VREF_AUDIO should be filtered using a 1µF capacitor from VREF_AUDIO terminal to ground.

Typical Applications (continued)

The built-in SAR ADC in TLV320AIC3268 can operate with either internally generated reference voltage or externally provided reference voltage. When used with internal reference, the reference voltage on VREF_SAR should be filtered with a 1µF capacitor for filtering noise as well as reference stability.

9.2.1.3 Micbias

The TLV320AIC3268 has a built-in bias voltage output for biasing of microphones. No intentional capacitors should be connected directly to either MICBIAS or MICBIAS_EXT outputs for filtering.

9.2.1.4 Power Supply

The TLV320AIC3268 needs several power supplies for it's operation.

The SVDD input is used to power the speaker amplifier. This includes the power required for internal circuits as well as the power delivered to the speaker load. It is recommended that this supply is directly connected to battery, for systems where battery rail is in the range of 2.7V to 5.5V.The peak switching current on this power can exceed 1A. MICBIAS_VDD can be tapped from same source that is used for SVDD.

The AVDDx_18, HVDD_18 and CPVDD_18 power inputs are used to power the analog circuits including analog to digital converters, digital to analog converters, programmable gain amplifiers, headphone amplifiers, charge pump etc. The analog blocks in TLV320AIC3268 have high power supply rejection ratio, however it is recommended that these supplies be powered by well regulated power supplies like low dropout regulators (LDO) for optimal performance. When these power terminals are driven from a common power source, the current drawn from the source will depend upon blocks enabled inside the device. However as an example when all the internal blocks powered are enabled the source should be able to deliver 150mA of current.

The RECVDD_33 powers the receiver amplifier of TLV320AIC3268. When the receiver amplifier is used in differential lineout mode, then the RECVDD_33 could be connected to the same supply as AVDDx_18 terminals. When the receiver amplifier is used to drive mono receiver speakers in BTL mode, the RECVDD_33 supply could consume approximately 150mA of peak current.

The DVDD_18 powers the digital core of TLV320AIC3268, including the miniDSP, audio serial interfaces (ASI), control interfaces (SPI or I2C), clock generation and PLL. The DVDD_18 power can be driven by high efficiency switching regulators or low drop out regulators. When the miniDSP_a and miniDSP_D are enabled in programmable mode and operated at peak frequencies, the supply source should be able to able to deliver approx 100mA of current. When the PRB modes are used instead of programmable miniDSP mode, then the peak current load on DVDD_18 supply source could be approximately 20mA.

The IOVDD1_33 and IOVDD2_33 power the digital input and digital output buffers of TLV320AIC3268. The current consumption of this power depends on configuration of digital terminals as inputs or outputs. When the digital terminals are configured as outputs, the current consumption would depend on switching frequency of the signal and the load on the output terminal, which depends on board design and input capacitance of other devices connected to the signal .

Refer to Figure 109 for recommendations on decoupling capacitors.

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input Connection

The analog inputs to TLV320AIC3268 should be ac-coupled to the device terminals to allow decoupling of signal source's common mode voltage with that of TLV320AIC3268's common mode voltage. The input coupling capacitor in combination with the selected input impedance of TLV320AIC3268 forms a high-pass filter.

$$F_c = 1/(2*\pi*R_{eq}C_c) \quad (22)$$

$$C_c = 1/(2*\pi*R_{eq}F_c) \quad (23)$$

For high fidelity audio recording application it is desirable to keep the cutoff frequency of the high pass filter as low as possible. For single-ended input mode, the equivalent input resistance R_{eq} can be calculated as

$$R_{eq} = R_{in}* (1 + 2g)/(1+g) \quad (24)$$

where g is the analog PGA gain calculated in linear terms.

$$g = 10000 * 2^{floor(G/6)}/R_{in} \quad (25)$$

Typical Applications (continued)

where G is the analog PGA gain programmed in B0_P1_R59-60 (in dB) and R_{in} is the value of the resistor programmed in B0_P1_R52-53 and B0_P1_R55-56 and assumes $R_{in} = R_{cm}$ (as defined in B0_P1_R54 and B0_P1_R57). For differential input mode, R_{eq} can be calculated as:

$$R_{eq} = R_{in} \quad (26)$$

where R_{in} is the value of the resistor programmed in B0_P1_R52-54 and B0_P1_R55-57, assuming symmetrical inputs.

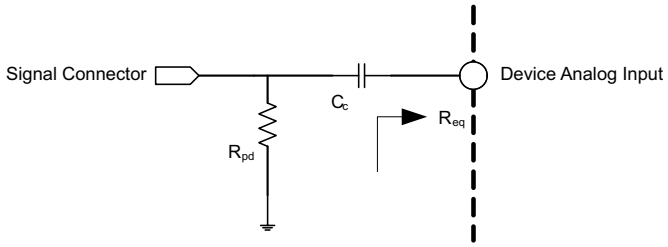


Figure 110. Analog Input Connection With Pull-down Resistor

When the analog signal is connected to the system through a connector such as audio jack, it is recommended to put a pull-down resistor on the signal as shown in Figure 111. The pulldown resistor helps keep the signal grounded and helps improve noise immunity when no source is connected to the connector. The pulldown resistor value should be chosen large enough to avoid loading of signal source.

Each analog input of the TLV320AIC3268 is capable of handling signal amplitude of 0.5Vrms. If the input signal source can drive signals higher than the maximum value, an external resistor divider network as shown in Figure 111 should be used to attenuate the signal to less than 0.5Vrms before connecting the signal to the device. The resistor values of the network should be chosen to provide desired attenuation as well as Equation 27.

$$R_1 || R_2 << R_{eq} \quad (27)$$

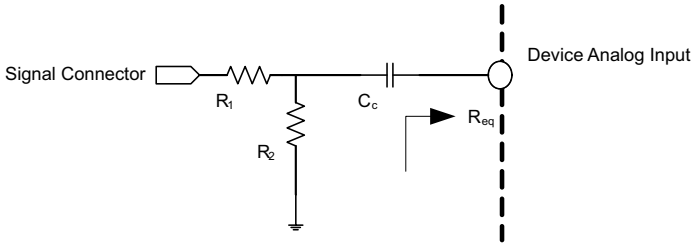


Figure 111. Analog Input Connection With Resistor Divider Network

Certain non audio applications require supporting of high impedance sources. The TLV320AIC3268 supports a high-input impedance mode on IN1L/AUX1 and IN1R/AUX2 terminals, for such use cases. See High Impedance Input Mode for more details. For such cases the input coupling capacitor can be eliminated from design.

Whenever any of the analog input terminals IN1L_AUX1, IN2L, IN3L, IN4L, IN1R_AUX2, IN2R, IN3R or IN4R are not used in an application, it is recommended to short the unused input terminals together and connect them to ground using a small capacitor (example 0.1µF). If VBAT is not used in an application, then it can be shorted to ground.

9.2.2.2 Analog Output Connection

The line outputs of the TLV320AIC3268 drive a signal biased around the device common mode voltage. To avoid loading the common mode with the load, it is recommended to connect the single-ended load through an ac-coupling capacitor. The ac-coupling capacitor in combination with the load impedance forms a high pass filter.

$$F_c = 1/(2*\pi*R_L C_c) \quad (28)$$

$$C_c = 1/(2*\pi*R_L F_c) \quad (29)$$

Typical Applications (continued)

For high fidelity playback, the cutoff frequency of the resultant high-pass filter should be kept low. For example with R_L of 10kΩ, using 1µF coupling capacitor results in a cut-off frequency of 8Hz.

For differential lineout configurations, the load should be directly connected between the differential outputs, with no coupling capacitor.

The TLV320AIC3268 supports headphone in single-ended configuration and drives the signal biased around ground. The headphone load can be directly connected between device terminals and ground.

The TLV320AIC3268 supports BTL load for receiver and speaker amplifier. The load can be directly connected between the differential output terminals of receiver and speaker amplifier.

Whenver any of the analog output terminals LOL, LOR, RECP, RECM, HPL, HPR, SPKP or SPKM are not used in an application, they should be left open or not connected.

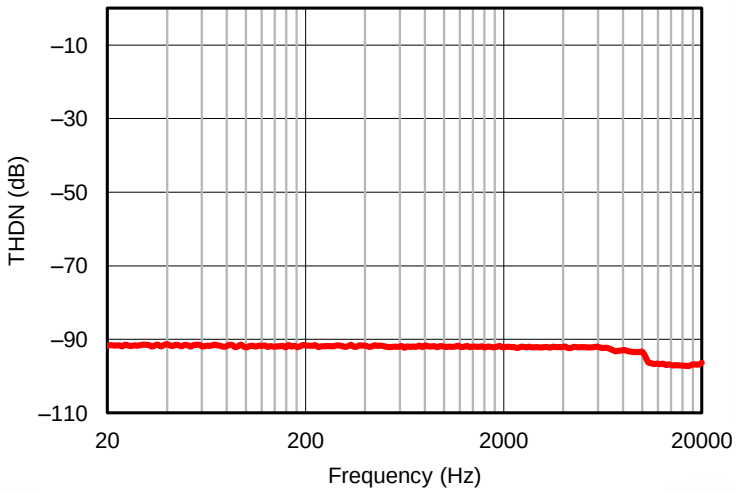
9.2.2.3 EMI Passive Devices

The TLV320AIC3268 does not need filters for the functioning of it's speaker amplifier.

However depending on the board layout and system level EMI requirements, an optional EMI filter consisting of ferrite beads and capacitors may be used as shown in and and labelled as optional. The ferrite beads if used should be capable of handing peak currents for desired power delivery into speakers. If EMI passives are not used, ferrite bead should be replaced with a short and the capacitor not installed.

9.2.3 Application Performance Plots

Figure 112 shows the excellent low-distortion performance of the TLV320AIC3268 in a system over the 20Hz to 20kHz audio spectrum.

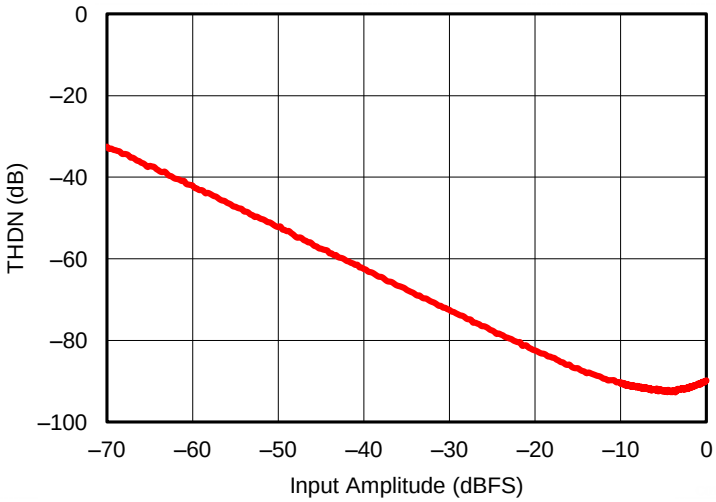


Conditions: Differential Lineout, R_{load}=10kΩ, CM=0.9V, Input Amplitude=-3dBFS

Figure 112. Total Harmonic Distortion + Noise versus Input Frequency

Figure 113 shows the distortion performance of the TLV320AIC3268 in a system over the input amplitude range.

Typical Applications (continued)



Conditions: Differential Lineout, R_{load}=10kΩ, CM=0.9V

Figure 113. Total Harmonic Distortion + Noise versus Input Amplitude

9.3 Initialization Setup

The TLV320AIC3268 has multiple power supply domains to support various functions. Before the device is fully functional, all the power supplies must be enabled. The section Power On Sequence describes the supported power supply sequencing for TLV320AIC3268.

9.3.1 Power On Sequence

There are two recommended power sequence possible for TLV320AIC3268:

1) Speaker/Microphone Supplies, then Digital Supplies, then Analog Supplies

2) Speaker/Microphone Supplies, then Digital and Analog Supplies

The first power on sequence is useful if the end system uses separate analog and digital supplies. This is useful to improve the efficiency of the digital rails by using a DC/DC converter, while keeping the analog supplies clean by using a low-dropout regulator (LDO). While it is recommended to separate analog and digital supplies, if all the 1.8V supplies (analog and digital) must be tied together, the second power sequence can be utilized.

9.3.1.1 Power On Sequence 1 - Separate Digital and Analog Supplies

Figure 114 shows a timing diagram for the case where all supplies are provided separately. In such case, the depicted sequence should be used. The dashed lines marked in blue color refer to an internally supplied voltage.

Initialization Setup (continued)

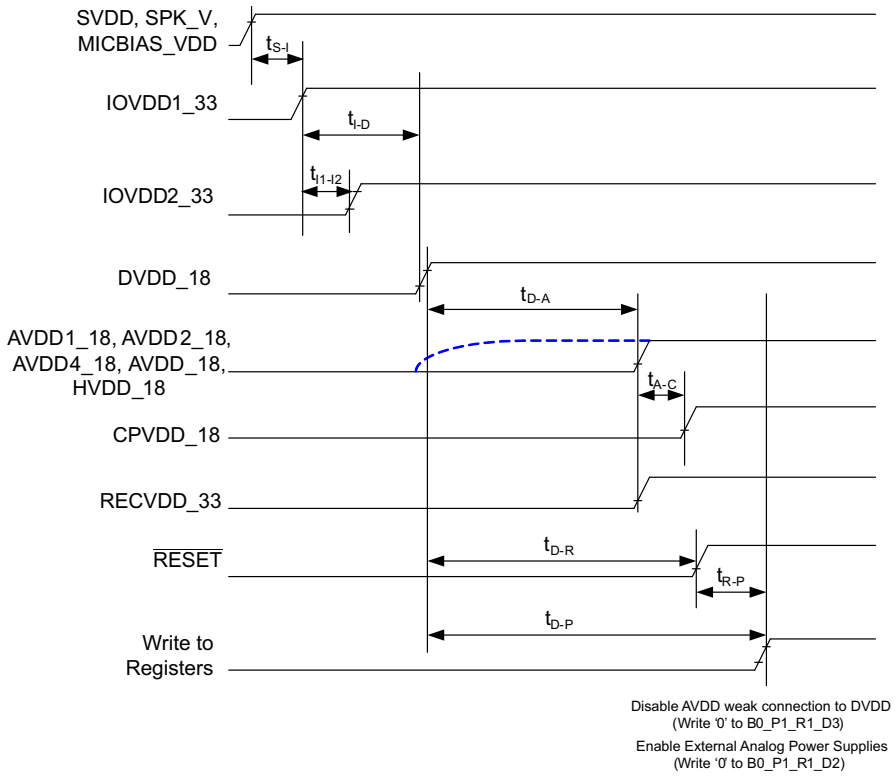


Figure 114. Analog Supplies provided after Digital Supplies

SVDD, SPK_V, and MICBIAS_VDD should be provided first. Next, IOVDD1_33 and IOVDD2_33 should be provided, and DVDD_18 can be provided at the same time as these IOVDDx_33 supplies. Since, by default, DVDD_18 is weakly connected to AVDD1_18 by a 10kΩ resistor, AVDDx_18 and HVDD_18 (it is recommended to connect these five supplies together) will ramp up to the DVDD_18 voltage once DVDD_18 is provided at approximately $5*10k*C_{AVDD}$ seconds, where C_{AVDD} are the sum of the decoupling capacitors on the AVDDx_18 and HVDD_18 terminals. For C_{AVDD} = 1uF, the charging time is approximately 50ms. Parameter t_{D-A} allows analog supplies to be stable before analog supplies are provided. To prevent high currents from DVDD_18 to the 1.8V and 3.3V analog supplies (that is AVDDx_18, HVDD_18, RECVDD_33), these analog supplies cannot be externally driven low by the external power source. This means that the external power source should be either high impedance or have a weak pull-down before being enabled.

Ensure that CPVDD_18 supply is provided either at same time as analog supplies or later. After $\overline{\text{RESET}}$ is released (or a software reset is performed), no register writes should be performed within 1ms.

Table 63. Power Supply Timing Parameters

Parameter	Minimum	Typical	Maximum	Comments
t_{S-I}	0	0		Time between SVDD/SPK_V/MICBIAS_VDD is provided and IOVDD1_33 is provided.
t_{I-D}	0	0		Time between IOVDD1_33 is provided and DVDD_18 is provided.
t_{I1-I2}	0	0	Before DVDD_18 provided	Time between IOVDD1_33 is provided and IOVDD2_33 is provided.
t_{D-A}	$5*10k*C_{AVDD}$	$5*10k*C_{AVDD}$		Time between DVDD_18 is provided and the 1.8V and 3.3V analog supplies (AVDDx_18, HVDD_18, AVDD3_33, RECVDD_33) are provided. AVDDx_18 must be internally present before changing to external 1.8V analog supplies to prevent pop at headphone outputs.
t_{A-C}	0	0		Time between AVDDx_18 supplies are provided and CPVDD_18 is provided.

Initialization Setup (continued)

Table 63. Power Supply Timing Parameters (continued)

Parameter	Minimum	Typical	Maximum	Comments
t_{D-R}	10ns	10ns		Time between DVDD_18 (and IOVDD1_33) is provided and reset can be released.
t_{D-P}	10ms	10ms		Time between DVDD_18 (and IOVDD1_33) is provided and when registers can be written to enable the external 1.8V analog supplies.
t_{R-P}	1ms	1ms		Time between release of the reset and when registers can be written (that is to enable the external 1.8V analog supplies).

9.3.1.2 Power On Sequence 2 - Shared 1.8V Analog Supplies

If desired, the analog supplies (AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 and HVDD_18) could also be externally supplied at the same time as DVDD_18. In this case, the weak pullup is not utilized. This is shown in Figure 115.

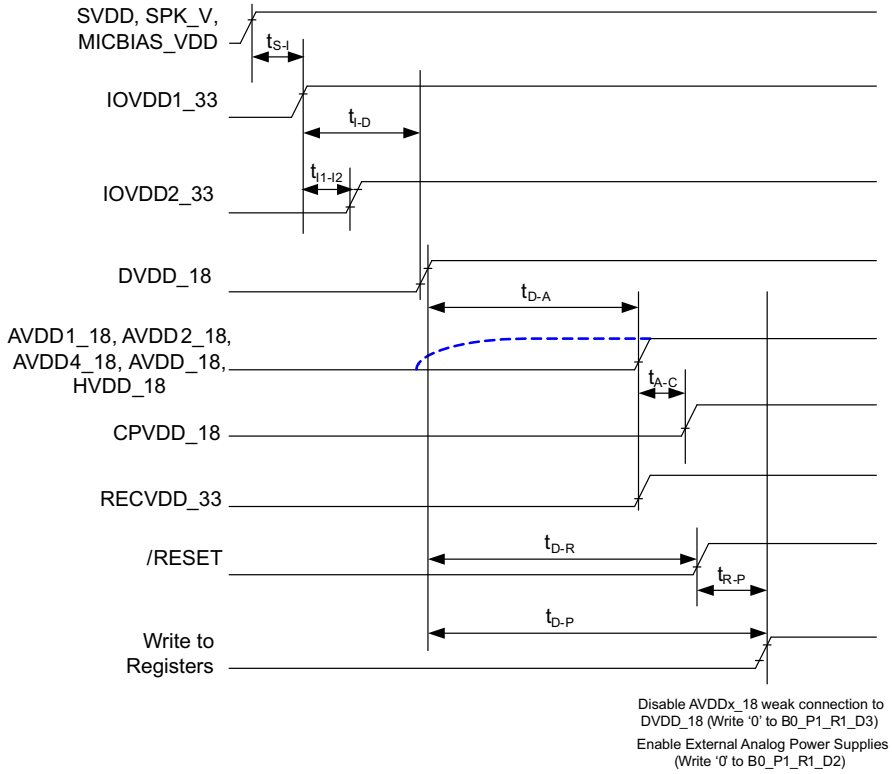


Figure 115. Simultaneous Powerup of Digital and Analog 1.8V Supplies

After $\overline{\text{RESET}}$ is released (or a software reset is performed), no register writes should be performed within 1ms.

Table 64. Power Supply Timing Parameters

Parameter	Minimum	Typical	Maximum	Comments
t_{S-I}	0	0		Time between SVDD/SPK_V/MICBIAS_VDD is provided and IOVDD1_33 is provided.
t_{I-D}	0	0		Time between IOVDD1_33 is provided and DVDD_18 is provided.
t_{I1-I2}	0	0	Before DVDD_18 provided	Time between IOVDD1_33 is provided and IOVDD2_33 is provided.
t_{A-C}	0	0		Time between AVDDx_18 supplies are provided and CPVDD_18 is provided.

Table 64. Power Supply Timing Parameters (continued)

Parameter	Minimum	Typical	Maximum	Comments
t_{D-R}	10ns	10ns		Time between DVDD_18 (and IOVDD1_33) is provided and reset can be released.
t_{D-P}	10ms	10ms		Time between DVDD_18 (and IOVDD1_33) is provided and when registers can be written to enable the external 1.8V analog supplies.
t_{R-P}	1ms	1ms		Time between release of the reset and when registers can be written (that is to enable the external 1.8V analog supplies).

When the TLV320AIC3268 is controlled over a shared I^2C bus, it is recommended that any I^2C communication be attempted only after the IOVDDx_33 and DVDD_18 rails have been powered up and the hardware reset signal applied. If I^2C communication is attempted before this requirement, even with other devices on the same I^2C bus, error conditions may occur.

9.3.2 Reset

The TLV320AIC3268 internal logic must be initialized to a known condition for proper device function. To initialize the device in its default operating condition, the hardware reset terminal (RESET) must be pulled low for at least 10ns. For this initialization to work, both the IOVDDx_33 and DVDD_18 supplies must be powered up. It is recommended that while the DVDD_18 supply is being powered up, the RESET terminal be pulled low.

The device can also be reset via software reset. Writing '1' into B0_P0_R1_D0 resets the device. After a device reset, all registers are initialized with default values as listed in the Register Map section.

After hardware or software reset, the TLV320AIC3268 is in a sleep mode, when all the blocks and functions are disabled. In this mode however the control interface, SPI or I^2C remains enabled, allowing an external host controller to configure the device. The blocks inside the TLV320AIC3268 must be configured for desired function by writing into the control registers.

Given below are some of the typical configurations that are needed to be done before enabling TLV320AIC3268. However the list of configurations is not unique or comprehensive and the requirements must be determined per the application requirements.

- Wait for Lockout time. See Device Startup Lockout Times for details.
- Configuration of FIFO's. See Setting Device FIFOs for details.
- Configure the device for PRB modes or programmable miniDSP modes for ADC and DAC.
  - For PRB modes, program the coefficients of user programmable filters, including setup adaptive coefficient updates if necessary.
  - For programmable miniDSP mode, configure the instruction and coefficient memory for miniDSP.
- Configure the oversampling rates, AOSR and DOSR, and power tune modes for ADCs and DACs.
- Configure the clock dividers and PLL, if required. See Clock Generation and PLL for details.
- Configure the Audio Serial Interfaces (ASI).
- Configure the device common mode voltages. See Setting Device Common Mode Voltage for details.
- Configure the analog signal routing to ADCs and from DACs, volume controls and power up the relevant blocks.

Some device configurations require wait times after register configuration, to take effect. See Analog and Reference Startup and PLL Startup for details. Table 42 describes internal flags which can be used to check device status in response to device configurations or input signals.

The details of control registers for device configurations are described in Register Maps.

9.3.3 Device Startup Lockout Times

After the TLV320AIC3268 is initialized through hardware reset at power-up or software reset, the internal registers are initialized to default values. This initialization takes place within 1ms after pulling the RESET signal high. During this initialization phase, no register-read or register-write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

9.3.4 Analog and Reference Startup

The TLV320AIC3268 uses an external VREF_AUDIO terminal for decoupling the reference voltage used for the data converters and other analog blocks. VREF_AUDIO terminal requires a minimum 1µF decoupling capacitor from VREF_AUDIO to VSS. In order for any analog block to be powered up, the Analog Reference block must be powered up. By default, the Analog Reference block will implicitly be powered up whenever any analog block is powered up, or it can be powered up independently. Detailed descriptions of Analog Reference including fast power-up options are provided in Reference Voltage. During the time that the reference block is not completely powered up, subsequent requests for powering up analog blocks (for example PLL) are queued, and executed after the reference power up is complete.

When analog inputs are routed to the ADC PGA, approximately 2ms of wait is required to enable charging up of input coupling capacitor before the routing is enabled.

9.3.5 PLL Startup

Whenever the PLL is powered up, a startup delay of approx 1ms is involved after the power up command of the PLL and before the clocks are available to the codec. This delay is to ensure stable operation of PLL and clock-divider logic.

9.3.6 Setting Device Common Mode Voltage

The TLV320AIC3268 allows the user to set the common mode voltage for analog inputs to 0.75V or 0.9V by programming B0_P1_R8_D2. The input common-mode voltage of 0.9V works best when the analog supply voltage is centered around 1.8V or above, and offers the highest possible performance. For analog supply voltages below 1.8V, a common mode voltage of 0.75V must be used.

Table 65. Input Common Mode voltage and Input Signal Swing

Input Common Mode Voltage (V)	AVdd (V)	Channel Gain (dB)	Single-Ended Input Swing for 0dBFS output signal (V_{RMS})	Differential Input Swing for 0dBFS output signal (V_{RMS})
0.75	>1.5	–2	0.375	0.75
0.90	1.8 … 1.95	0	0.5	1.0

NOTE

The input common mode setting is common for DAC playback and Analog Bypass path

9.3.7 Setting Device FIFOs

The TLV320AIC3268 features FIFO between CIC filters and miniDSP_A and miniDSP_D and DAC modulators. These FIFO's allow ease of programming of signal processing functions within the miniDSP by allowing easier interface with other blocks. However use of these FIFOs adds to group delay in the channel and should be bypassed for delay sensitive applications along with appropriate care taken in miniDSP programming. By default the FIFO between CIC filter and miniDSP_A is disabled and is recommended to be enabled by writing B64_P0_R32_D7 as '1'. Similarly by default the FIFO between miniDSP_D and DAC modulator is disabled and is recommended to be enabled by writing B120_P0_R50_D7 as '1'.

The TLV320AIC3268 has a feature which allows the miniDSP instruction frame to be synchronized with ASI's data frame. For miniDSP_D, the synchronization is done with ASI1's data frame by default. However when the TLV320AIC3268 is used with PRB modes for playback, it is recommended to disable miniDSP_D's synchronization with ASI data frame by programming B0_P4_R119_D[7:6] as "11".

9.3.8 Miscellaneous

When enabling headphone amplifiers, it is recommended to program B0_P1_R77_D0 as '1' before powering up headphone amplifier.

10 Power Supply Recommendations

See Power Supply for details about driving power supplies. See Power On Sequence for details on sequencing of power supplies.

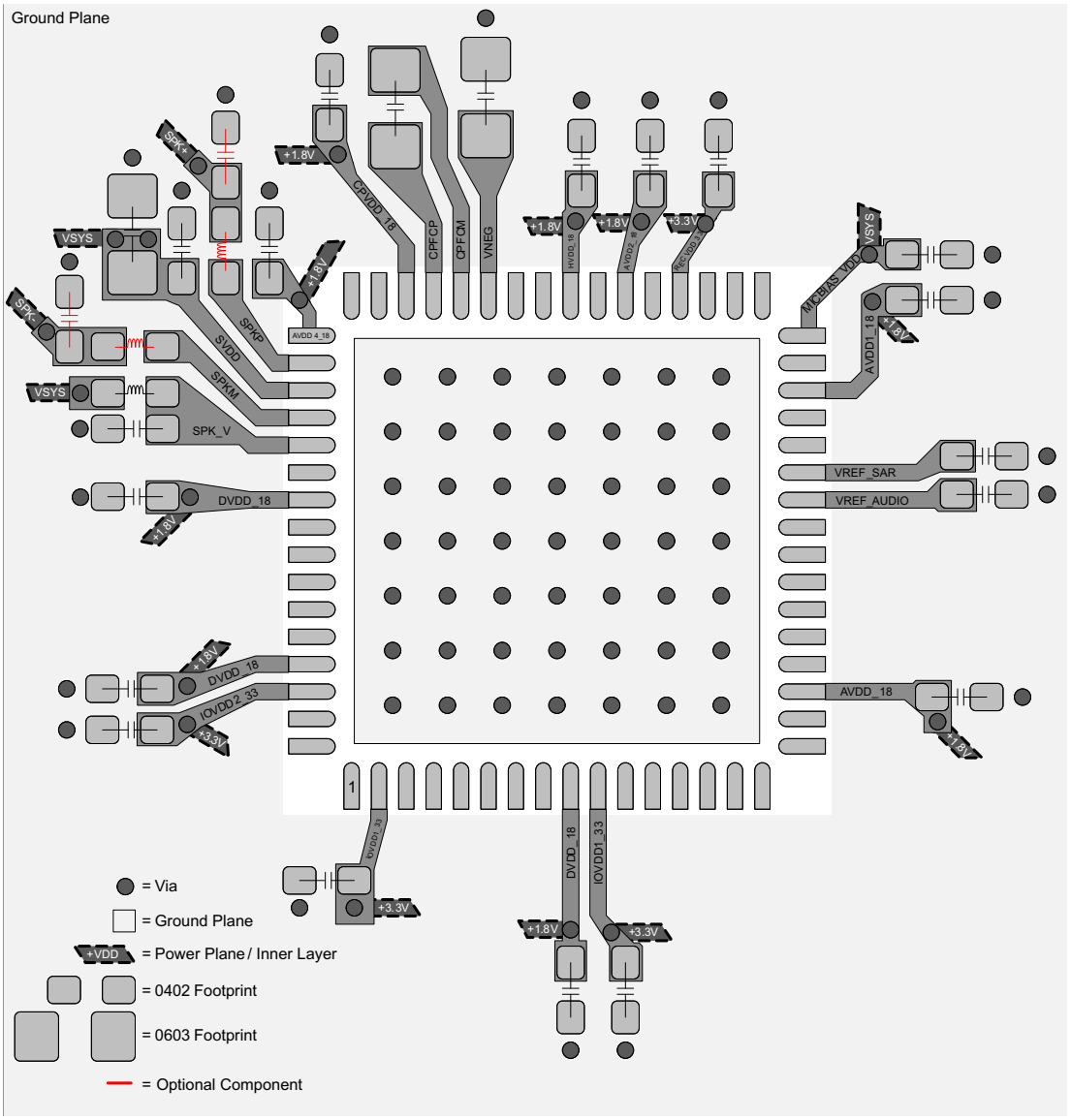
11 Layout

11.1 Layout Guidelines

Each system design and PCB layout is unique; layout should be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize TLV320AIC3268 performance:

- The TLV320AIC3268 thermal pad also serves as a device ground connection. Connect the thermal pad to the ground plane using multiple VIAS to minimize impedance between device ground and PCB ground. The TLV320AIC3268 has only one ground terminal. The digital ground and analog ground planes on the PCB should be shorted to each other close the TLV320AIC3268 thermal pad.
- The decoupling capacitors for the power supplies should be placed close to the device terminals. Figure 109 shows the recommended decoupling capacitors for the TLV320AIC3268. For SVDD, place the 10µF bulk decoupling capacitor near where battery supply enters the PCB, and place the smaller 0.1µF and 1µF decoupling capacitors closer to the device terminals.
- Place the flying capacitor between CPFCP and CPFCM near the device terminals, with no VIAS between the device terminals and the capacitor. Similarly, keep the decoupling capacitor on VNEG near the device terminal with minimal VIAS between the device terminals, capacitor and PCB ground.
- The TLV320AIC3268 internal voltage references must be filtered using external capacitors. Place the filter capacitors on VREF_AUDIO and VREF_SAR near the device terminals for optimal performance.
- The TLV320AIC3268 reduces crosstalk by a separate ground sense signal for the headphone jack. To optimize crosstalk performance, use a separate trace from the HPVSS_SENSE terminal to the headphone-jack ground terminal, with no other ground connections along the length.
- The parasitic capacitance to ground plane should be minimized for SPKP and SPKM signals. Keep the signal routing for SPKP and SPKM as short as possible for optimal performance of the speaker amplifier.
- For analog differential audio signals, the signals should be routed differentially on the PCB for better noise immunity. Avoid crossing of digital and analog signals to avoid undesirable crosstalk.

11.2 Layout Example



12 Device and Documentation Support

12.1 Community Resources

E2E™ Audio Converters Forum

TI E2E Community

12.2 Trademarks

E2E is a trademark of Texas Instruments, Inc..

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320AIC3268IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AIC3268	Samples
TLV320AIC3268IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AIC3268	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

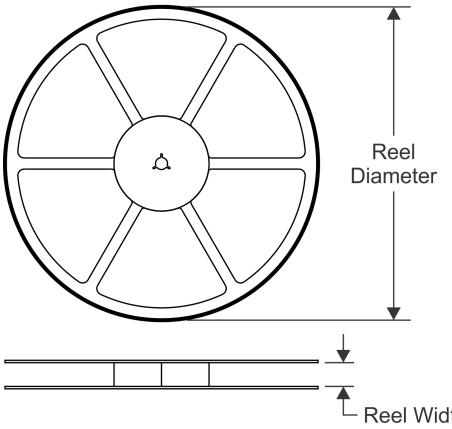
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

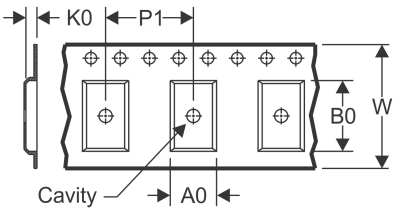
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

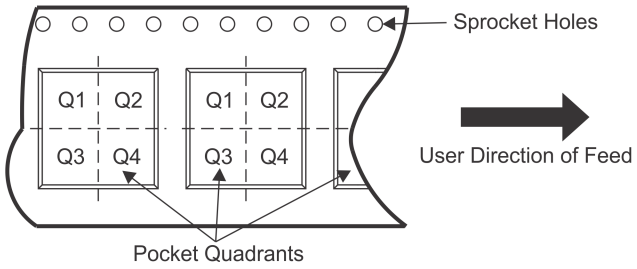


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

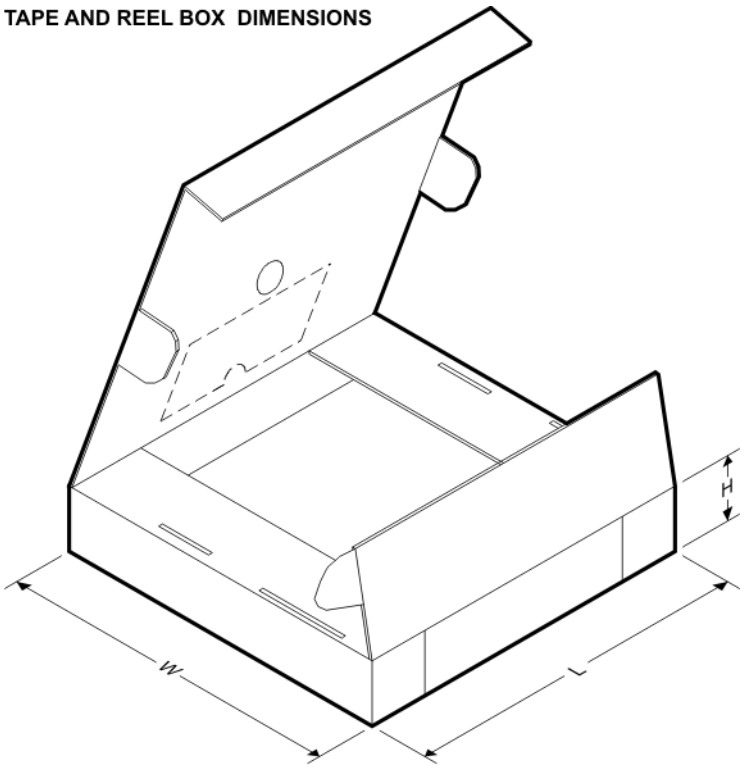
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3268IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TLV320AIC3268IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

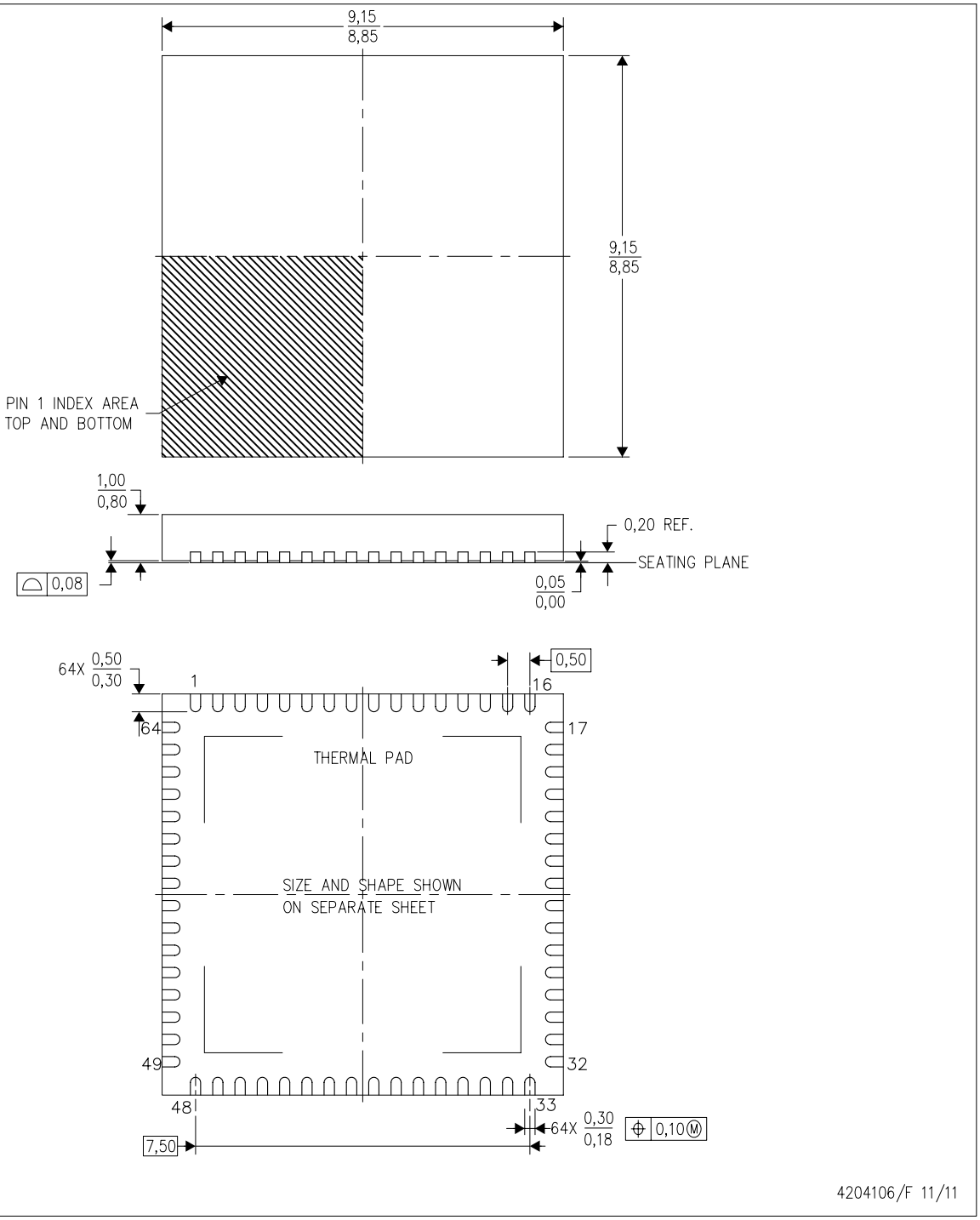
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3268IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
TLV320AIC3268IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

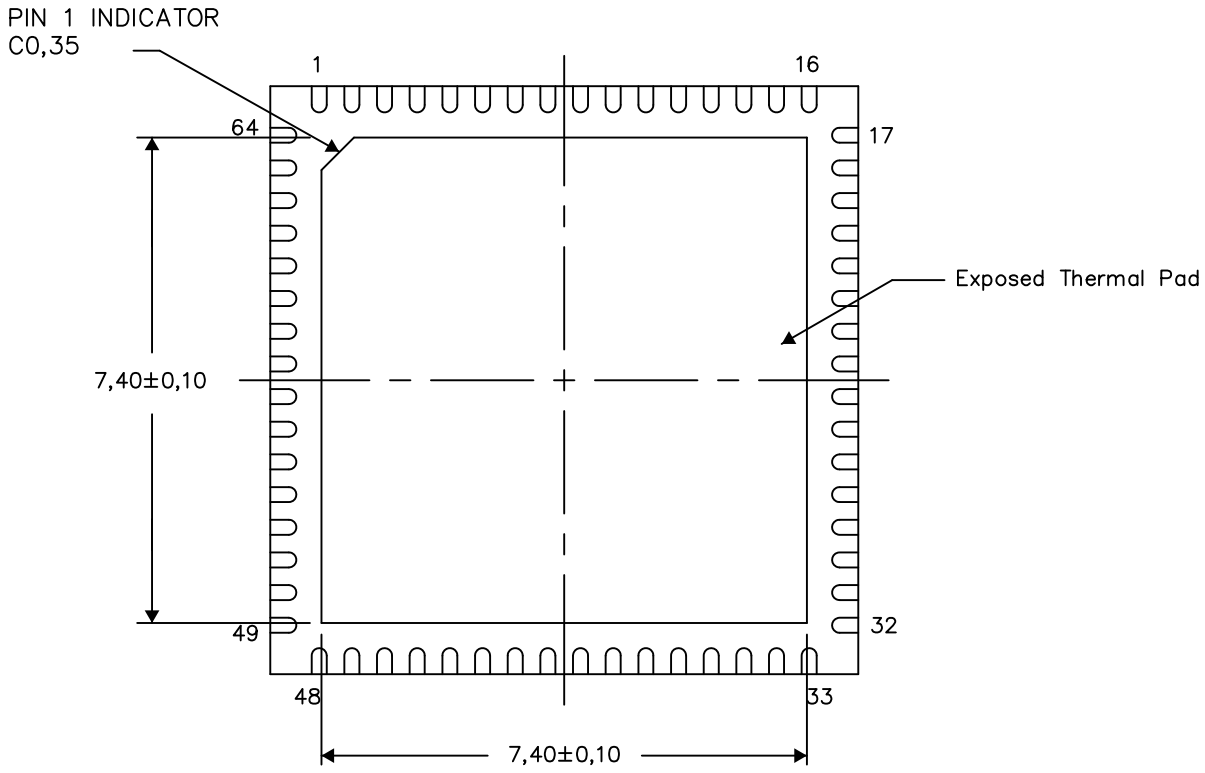
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



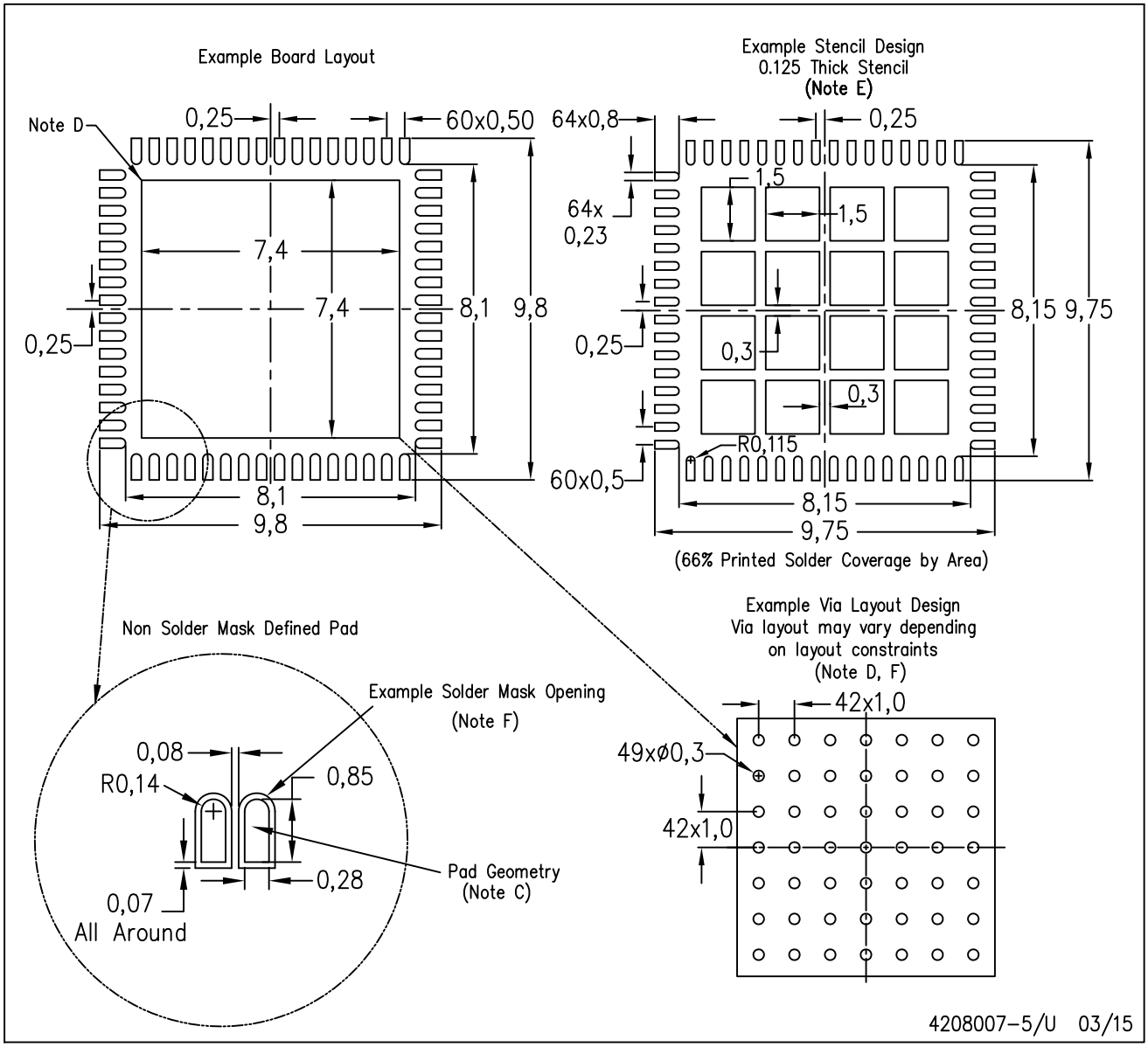
Bottom View

Exposed Thermal Pad Dimensions

4206192–4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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