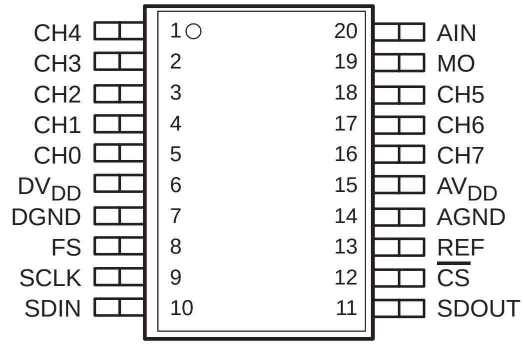
features

- Fast Throughput Rate: 1.25 MSPS at 5 V,
  625 KSPS at 3 V
- Wide Analog Channel Input: 0 V to AV_{DD}
- Eight Analog Input Channels
- Channel Auto-Scan
- Differential Nonlinearity Error: < ±1 LSB
- Integral Nonlinearity Error: < ±1 LSB
- Signal-to-Noise and Distortion Ratio: 57 dB
- Single 2.7-V to 5.5-V Supply Operation
- Very Low Power: 40 mW at 5.5 V,
  8 mW at 2.7 V
- Autopower-Down: 300 μA Max
- Software Power Down: 10 μA Max
- Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Microcontrollers
- Programmable Internal Reference Voltage:
  3.8-V Reference for 5-V Operation,
  2.3-V Reference for 3-V Operation

applications

- Mass Storage and Hard Disk Drive
- Automotive
- Digital Servos
- Process Control
- General-Purpose DSP
- Image Sensor Processing

DW OR PW PACKAGE
(TOP VIEW)



description

The TLV1570 is a 10-bit data acquisition system that combines an 8-channel input multiplexer (MUX), a high-speed 10-bit ADC, an on-chip reference, and a high-speed serial interface. The device contains an on-chip control register allowing control of channel selection, conversion start, reference voltage levels, and power down via the serial port. The MUX is independently accessible, which allows the user to insert a signal conditioning circuit such as an antialiasing filter or an amplifier, if required, between the MUX and the ADC. Therefore one signal conditioning circuit can be used for all eight channels.

The TLV1570 operates from a single 2.7-V to 5.5-V power supply. The device accepts an analog input range from 0 V to AV_{DD} and digitizes the input at a maximum 1.25 MSPS throughput rate. Power dissipation is only 8 mW with a 2.7-V supply or 40 mW with a 5.5-V supply. The device features an autopower-down mode that automatically powers down to 300 μA, 10 ns after a conversion is performed. With software power down enabled, the device is further powered down to only 10 μA.

The TLV1570 communicates with digital microprocessors via a simple 4- or 5-wire serial port that interfaces directly to Texas Instruments TMS320 DSPs, and SPI™ and QSPI™ compatible microcontrollers without using additional glue logic.

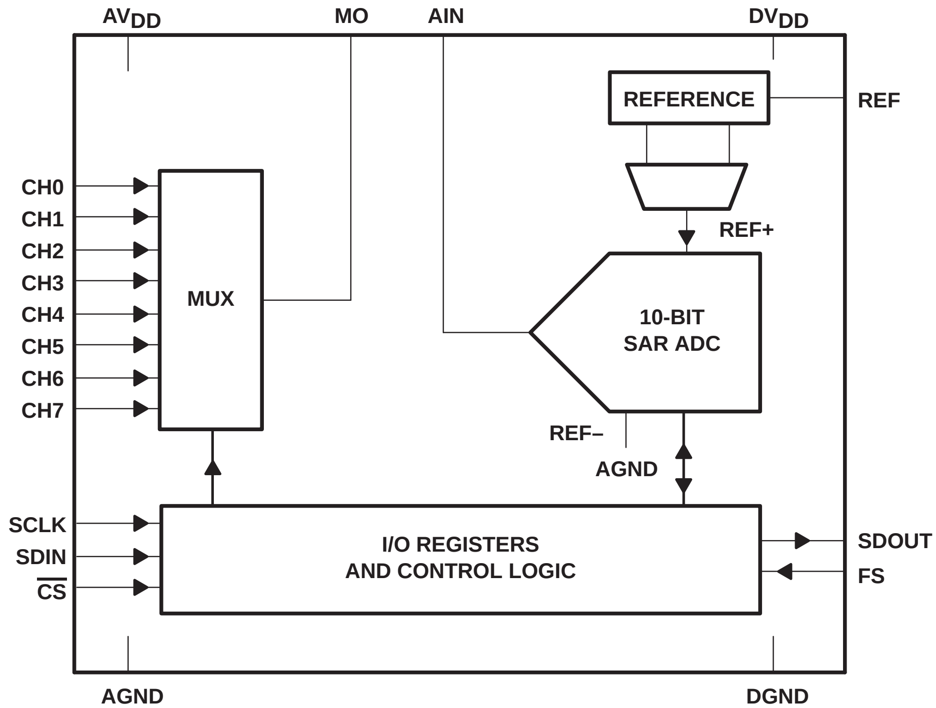
A very high throughput rate, a simple serial interface, and low power consumption make the TLV1570 an ideal choice for high-speed digital signal processing requiring multiple analog inputs.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (DW)	SMALL OUTLINE (PW)
0°C to 70°C	TLV1570CDW	TLV1570CPW
–40°C to 85°C	TLV1570IDW	TLV1570IPW

SPI and QSPI are trademarks of Motorola, Inc.

functional block diagram



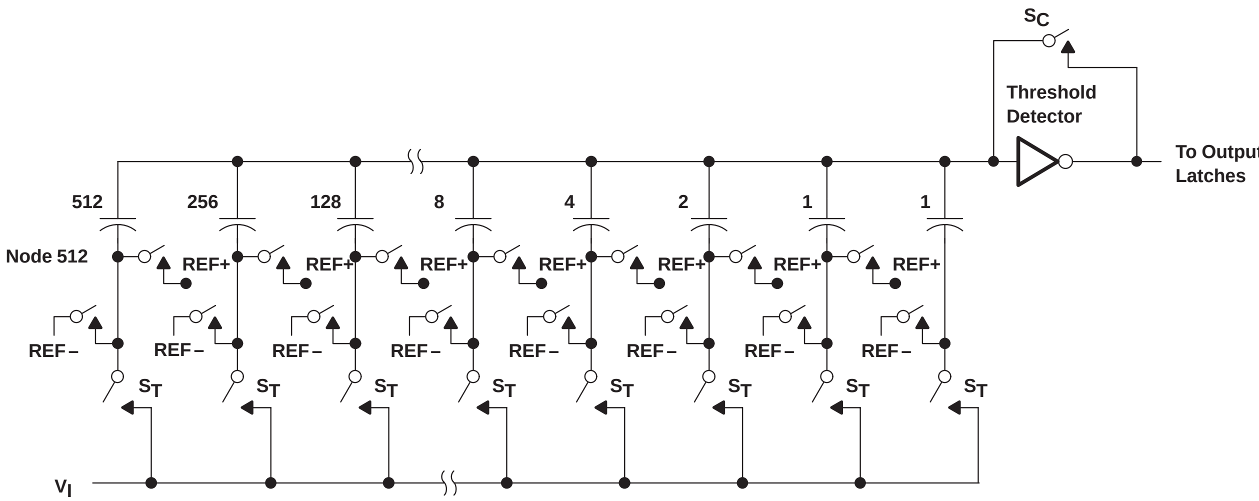
Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	14		Analog ground
AIN	20	I	ADC analog input
AV_{DD}	15		Analog supply voltage, 2.7 V to 5.5 V
CH0 – CH7	5,4,3,2,1, 18,17,16	I	Analog input channels 0 – 7
$\overline{CS}$	12	I	Chip select. A low level signal on $\overline{CS}$ enables the TLV1570. A high level signal on $\overline{CS}$ disables the device and disconnects power to the TLV1570.
DGND	7		Digital ground
DV_{DD}	6		Digital supply voltage, 2.7 V to 5.5 V
FS	8	I	Frame sync. The falling edge of the frame sync pulse from a DSP indicates the start of a serial data frame shifted out of the TLV1570. FS is pulled high when interfaced to a microcontroller.
MO	19	O	On-chip MUX analog output
REF	13	I	Reference voltage input. The voltage applied to REF defines the input span of the TLV1570. In external reference mode, a 0.1 μF decoupling capacitor must be placed between the reference and AGND. This is not required for internal reference mode.
SCLK	9	I	Serial clock input. SCLK synchronizes the serial data transfer and is also used for internal data conversion.
SDIN	10	I	Serial data input used to configure the internal control register.
SDOUT	11	O	Serial data output. A/D conversion results are output at SDOUT.

detailed description

analog-to-digital converter

The TLV1570 ADC uses the SAR architecture described in this section. The CMOS threshold detector in the successive-approximation conversion system determines the value of each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all of the capacitors to the input voltage.



NOTE: REF– is tied to AGND

Figure 1. Simplified Model of the Successive-Approximation System

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage (REF– is tied to AGND). In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

In the case of the TLV1570, REF– is tied to ground and REF+ is connected to the REF input.

The TLV1570 can be programmed to use the on-chip internal reference (DI6=1). The user can select between two values of internal reference, 2.3 V or 3.8 V, using the control bit DI5.

During internal reference mode, the reference voltage is not output on the REF pin. Therefore it cannot be decoupled to analog ground (AGND), which acts as the negative reference for the ADC, using an external capacitor. Hence this mode requires the ground noise to be very low. The REF pin can be left open in this mode.

sampling frequency, f_S

The TLV1570 requires 16 SCLKs for each sampling and conversion, therefore the equivalent maximum sampling frequency achievable with a given SCLK frequency is:

$$f_{S(MAX)} = (1/16)f_{SCLK}$$

power down

The TLV1570 offers two different power-down options. With autopower-down mode enabled, (DI4=0) the ADC proceeds to power down if FS is not detected on the 17th falling SCLK edge of a cycle (a cycle starts with FS being detected on a falling edge of SCLK) in DSP mode and after 16 SCLKs in µC mode. The TLV1570 will recover from auto power down when FS goes high in DSP mode or when the next SCLK comes in µC mode. In the case of software power down, the ADC goes to the software power-down state one cycle after CR.DI15 is set to 1. Unlike autopower down which recovers in 1 SCLK, software power down takes 16 SCLKs to recover.

DESCRIPTION		AUTOPOWER DOWN	SOFTWARE POWERDOWN $\overline{CS} = DV_{DD}$
Maximum power down dissipation current		300 µA	10 µA
Comparator		Power down	Powerdown
Clock buffer†		Power down	Powerdown
Reference		Active	Powerdown
Register		Not saved	Not saved
Minimum power down time		1 SCLK	1 µs
Minimum resume time		1 SCLK	800 ns
Power down	DSP mode	No FS present one SCLK after previous conversion completed	CR.DI15 set to 1
	Microprocessor mode (FS = 1)	SCLK stopped after previous conversion completed	CR.DI15 set to 1
Power up	DSP mode	FS present	CR.DI15 set to 1
	Microprocessor mode (FS = 1)	SCLK present	CR.DI15 set to 1

† Only in DSP mode is input buffer of clock in power-down mode.
‡ The software power down enable/disable bit is not acted until the start of the next cycle (see section *configuring the TLV1570 for more information*.

configuring the TLV1570

The TLV1570 is to be configured by writing the control bits to SDIN. The configuration will not take affect until the next cycle. A new configuration is needed for each conversion. Once the channel input and other options are selected, the conversion takes place in the next cycle. Conversion results are shifted out as conversion progresses (see Figure 2).

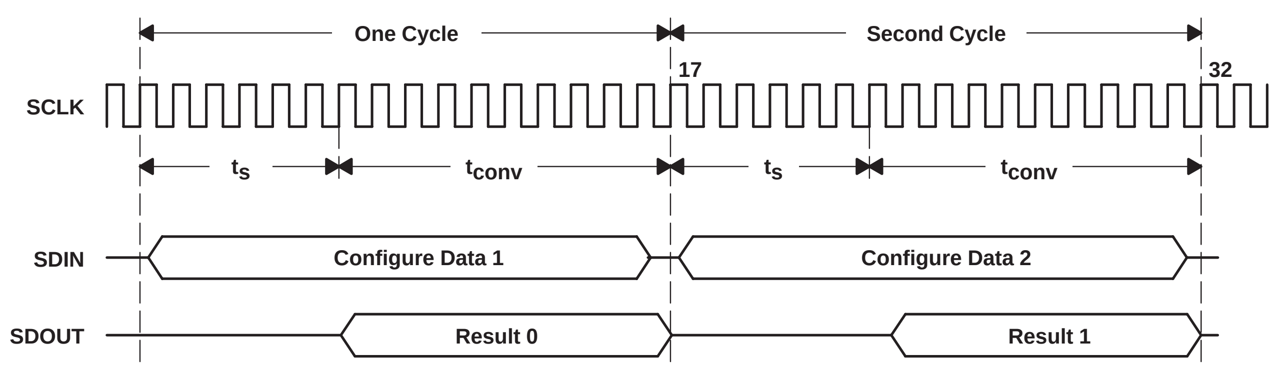


Figure 2. TLV1570 Configuration Cycle Timing

configuration register (CR) definition

<table>
<tr><th>BIT</th><th colspan="2">DESCRIPTION</th><th>5 V</th><th>3 V</th></tr>
<tr><td>DI15</td><td colspan="2">Software power down:
0: Normal
1: Power down enabled</td><td>X
X</td><td>X
X</td></tr>
<tr><td>DI14</td><td colspan="2">Reads out values of the internal register, 1 – read. Only DI15 – DI1 are read out.</td><td>X</td><td>X</td></tr>
<tr><td>DI13, DI12</td><td colspan="2">These two bits select the self-test voltage to be applied to the ADC input during next clock cycle:
00: Allow AIN to come in normally
01: Apply AGND to AIN
10: Apply VREF/2 to AIN
11: N/A</td><td>X</td><td>X</td></tr>
<tr><td>DI11</td><td colspan="2">Choose speed application
0: High speed (higher power consumption)
1: Low speed (lower power consumption)</td><td>X</td><td>X</td></tr>
<tr><td>DI10</td><td colspan="2">This bit enables channel auto-scan function.
0: Autoscan disabled
1: Autoscan enabled</td><td>X</td><td>X</td></tr>
<tr><td rowspan="4">DI9, DI8, DI7</td><td>DI9 – DI7 These three bits select which of the eight channels is to be used (if DI10 = 0).</td><td>DI9, DI8 These two bits select the channel swept sequence used by auto scan mode (if DI10 = 1)</td><td rowspan="4">X</td><td rowspan="4">X</td></tr>
<tr><td rowspan="3">000: Channel 0 selected as input
001: Channel 1 selected as input
010: Channel 2 selected as input
011: Channel 3 selected as input
100: Channel 4 selected as input
101: Channel 5 selected as input
110: Channel 6 selected as input
111: Channel 7 selected as input</td><td>00: Analog inputs CH0, CH1, CH2, ….., CH7 sequentially selected
01: Analog inputs CH1, CH3, CH5, CH7 sequentially selected
10: Analog inputs CH0, CH2, CH4, CH6 sequentially selected
11: Analog inputs CH7, CH6, CH5, ….., CH0 sequentially selected</td></tr>
<tr><td>DI7 Auto-scan reset</td></tr>
<tr><td>0: No reset
1: Reset autoscan sequence</td></tr>
<tr><td>DI6</td><td colspan="2">Selects Internal or external reference voltage:
0: External
1: Internal</td><td>X</td><td>X</td></tr>
<tr><td>DI5</td><td colspan="2">Selects internal reference voltage value to be applied to the ADC during next conversion cycle.
0: 2.3 V
1: 3.8 V</td><td>

X</td><td>
X
</td></tr>
<tr><td>DI4</td><td colspan="2">Enables/disables autopower-down function:
1: Enable
0: Disable</td><td>X</td><td>X</td></tr>
<tr><td>DI3</td><td colspan="2">Performance optimizer – linearity
0: AV_{DD} = 5.5 V to 3.6 V
1: AV_{DD} = 3.5 V to 2.7 V</td><td>X</td><td>X</td></tr>
<tr><td>DI2</td><td colspan="2">Always write 0 (reserved bit)</td><td>X</td><td>X</td></tr>
<tr><td>DI1</td><td colspan="2">Always write 0 (reserved bit)</td><td>X</td><td>X</td></tr>
<tr><td>DI0</td><td colspan="2">Always write 0 (reserved bit)</td><td>X</td><td>X</td></tr>
</table>

initialization-software sequence

This sequence shows the default settings, unless otherwise specified. The ADC requires that the user write to it every cycle. There is a cycle delay before control bits are implemented.

Example 1. Normal Sample Mode With Internal Reference

CYCLE	WRITE TO SDIN	CHANNEL SAMPLED	OUTPUT FROM SDOUT	COMMENT
1st	0040h	N/A	Invalid	No analog input channel sampled
2nd	01C0h	N/A	Invalid	No analog input channel sampled
3rd	0040h	3	From Channel 3	
4th	8040h	0	From Channel 0	Software power down enabled
5th	0040h	N/A	Invalid	Software power-down mode, no analog input channel sampled
Wait 800 ns				Recovery time, no analog input channel sampled (16 SCLKs if AV_{DD} = 5 V and f_{CLK} = 20 MHz)
6th	0140h	N/A	Invalid	Recovery time, no analog input channel sampled
7th	0040h	2	From Channel 2	

Example 2. Auto Scan Mode

CYCLE	WRITE TO SDIN	CHANNEL SAMPLED	OUTPUT FROM SDOUT	COMMENT
1st	0480h	N/A	Invalid	Autoscan reset enabled, no analog input channel sampled
2nd	0480h	N/A	Invalid	No analog input channel sampled
3rd	0400h	0	From Channel 0	
4th	0400h	1	From Channel 1	
5th	0400h	2	From Channel 2	
6th	0400h	3	From Channel 3	
7th	0400h	4	From Channel 4	
8th	0400h	5	From Channel 5	
9th	0400h	6	From Channel 6	
10th	0400h	7	From Channel 7	
11th	0400h	0	From Channel 0	

NOTE: If software power down is enabled during auto-scan mode, the next channel in the sequence is skipped.

initialization-software sequence (continued)

Example 3. Auto-Scan Mode

This example shows a change in sequence in the middle of the current sequence. The following shows that after the initial autoscan reset, a reset is not necessary again when switching channel sequences.

CYCLE	WRITE TO SDIN	CHANNEL SAMPLED	OUTPUT FROM SDOUT	COMMENT
1st	0480h	N/A	N/A	No analog input channel sampled
2nd	0480h	N/A	N/A	Autoscan reset enabled, no analog input channel sampled
3rd	0400h	0	From Channel 0	Start of sequence 0
4th	0700h	1	From Channel 1	Enable channel sequence 3 (no auto-scan reset required)
5th	0700h	7	From Channel 7	Start of sequence 3
6th	0700h	6	From Channel 6	
7th	0700h	5	From Channel 5	
8th	0700h	4	From Channel 4	
9th	0700h	3	From Channel 3	
10th	0700h	2	From Channel 2	
11th	0700h	1	From Channel 1	
12th	0700h	0	From Channel 0	

Example 4. Auto-Scan Mode

This example shows a switch in sequence in the course of a sequence. The following shows that a particular sequence does not have to be continued if remaining channels do not need to be sampled (i.e., only channel 1 through channel 5 sampled, not channels 6, 7, 8)

CYCLE	WRITE TO SDIN	CHANNEL SAMPLED	OUTPUT FROM SDOUT	COMMENT
1st	0480h	N/A	N/A	No analog input channel sampled
2nd	0480h	N/A	N/A	Autoscan reset enabled, no analog input channel sampled
3rd	0400h	0	From Channel 0	
4th	0400h	1	From Channel 1	
5th	0400h	2	From Channel 2	
6th	0400h	3	From Channel 3	
7th	0400h	4	From Channel 4	
8th	0480h	5	From Channel 5	Autoscan reset enabled
9th	0400h	0	From Channel 0	Sequence is reset to channel 0
10th	0400h	1	From Channel 1	
11th	0400h	2	From Channel 2	

The TLV1570 is a 800-ns 10-bit 8-analog input channel analog-to-digital converter with a throughput of up to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V respectively. To run at its fastest conversion rate, it must be clocked at 20 MHz at 5-V or 10 MHz at 3-V. The TLV1570 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. The TLV1570 serial interface is designed to be fully compatible with serial peripheral interface (SPI) and TMS320 DSP serial ports. No additional hardware is required to interface between the TLV1570 and a microcontroller (µCs) with a SPI serial port or a TMS320 DSP. However, the speed is limited by the SCLK rate of the µC or the DSP.

initialization-software sequence (continued)

The TLV1570 interfaces to a DSP over five lines: $\overline{CS}$, SCLK, SDOUT, SDIN, and FS, and interfaces to a µC over four lines: $\overline{CS}$, SCLK, SDOUT, and SDIN. The FS input should be pulled high in µC mode. The device is in 3-state and power-down mode when $\overline{CS}$ is high. After $\overline{CS}$ falls, the TLV1570 checks the FS input at the $\overline{CS}$ falling edge to determine the operation mode. If FS is low, DSP mode is set, otherwise µC mode is set.

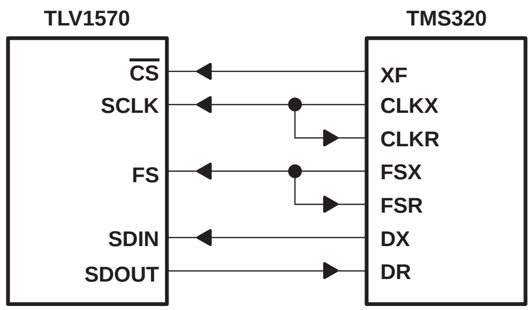


Figure 3. DSP to TLV1570 Interface

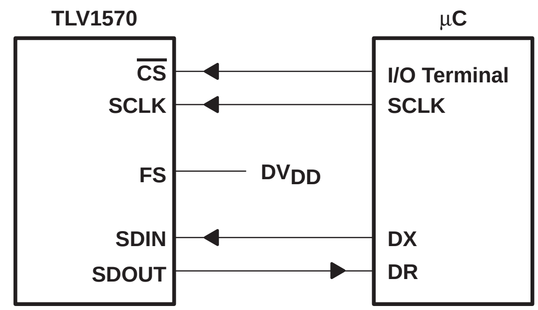


Figure 4. µC to TLV1570 Interface

grounding and decoupling considerations

General practices should apply to the PCB design to limit high frequency transients and noise that are fed back into the supply and reference lines (see Figure 5). This requires that the supply and reference pins be sufficiently bypassed. In most cases 0.1 µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Since their effectiveness depends largely on the proximity to the individual supply pin. They should be placed as close to the supply pins as possible.

To reduce high frequency and noise coupling, it is highly recommended that digital and analog ground be shorted immediately outside the package. This can be accomplished by running a low impedance line between DGND and AGND, under the package.

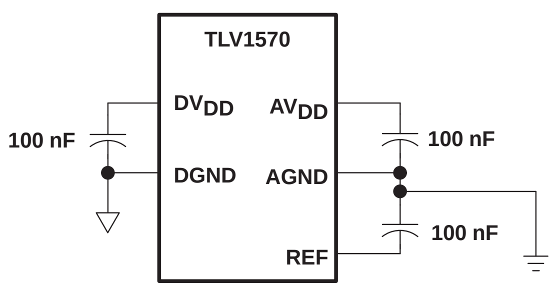


Figure 5. Placement of Decoupling Capacitors

power supply ground layout

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the ADC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.

simplified analog input analysis

Using the equivalent circuit in Figure 6, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB, t_{ch}(1/2 LSB), can be derived as follows:

The capacitance charging voltage is given by:

$$V_{C(t)} = V_S\left(1 - e^{-t_{ch}/R_tC_i}\right) \qquad (1)$$

Where:

$R_t = R_s + R_i$

$R_i = R_{i(ADC)} + R_{i(MUX)}$

t_{ch} = Charge time

The input impedance R_i is 718 Ω at 5 V, and is higher (~1.25 kΩ) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/2048) \qquad (2)$$

Equating equation 1 to equation 2 and solving for cycle time t_c gives:

$$V_S - \left(V_S/2048\right) = V_S\left(1 - e^{-t_{ch}/R_tC_i}\right) \qquad (3)$$

and time to change to 1/2 LSB (minimum sampling time) is:

$$t_{ch}\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048)$$

Where:

$\ln(2048) = 7.625$

Therefore, with the values given, the time for the analog input signal to settle is:

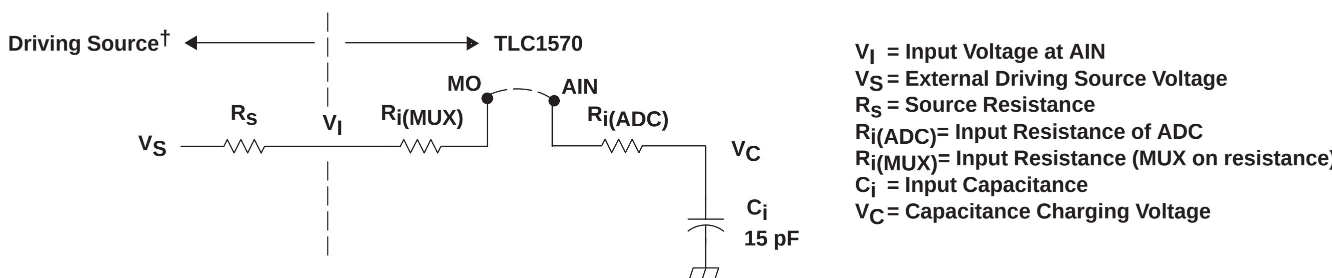
$$t_{ch}\ (1/2\ \text{LSB}) = (R_S + 718\ \Omega) \times 15\ \text{pF} \times \ln(2048) \qquad (4)$$

This time must be less than the converter sample time shown in the timing diagrams. Which is 6x SCLK.

$$t_{ch}\ (1/2\ \text{LSB}) \le 6\text{x}\ 1/f_{(SCLK)} \qquad (5)$$

Therefore the maximum SCLK frequency is:

$$\text{Max}(f_{(SCLK)}) = 6/t_{ch}\ (1/2\ \text{LSB}) = 6/(\ln(2048) \times R_t \times C_i) \qquad (6)$$



† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 6. Equivalent Input Circuit Including the Driving Source

definitions of specifications and terminology

integral nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

It is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, AGND to AV_{DD}, DGND to DV_{DD}		–0.3 V to 6.5 V
Analog input voltage range		–0.3 V to AV_{DD}+0.3 V
Reference input voltage		AV_{DD}+0.3 V
Digital input voltage range		–0.3 V to DV_{DD}+0.3 V
Operating virtual junction temperature range, T_J		–40°C to 150°C
Operating free-air temperature range, T_A:	TLV1570C	0°C to 70°C
	TLV1570I	–40°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	TYP	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 1)	2.7		5.5	V
Digital supply voltage, DV_{DD} (see Note 1)	2.7		5.5	V

NOTE 1: Abs (AV_{DD} – DV_{DD}) < 0.5 V

analog inputs

		MIN	TYP	MAX	UNIT
Analog input voltage, AIN		AGND		V_{REF}	V
Reference input voltage, REF	DV_{DD} = 3.3 V to 2.7 V	55% AV_{DD}		AV_{DD}	V
	DV_{DD} = 5.5 V to 4.5 V	60% AV_{DD}		AV_{DD}	

digital inputs

		MIN	TYP	MAX	UNIT
High-level input voltage, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2.1			V
Low-level input voltage, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Input SCLK frequency	DV_{DD} = 5.5 V to 4.5 V			20	MHz
	DV_{DD} = 3.6 V to 2.7 V	1		10	
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	DV_{DD} = 5.5 V to 4.5 V	23			ns
	DV_{DD} = 3.6 V to 2.7 V	46			
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	DV_{DD} = 5.5 V to 4.5 V	23			ns
	DV_{DD} = 3.6 V to 2.7 V	46			

electrical characteristics,over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

digital specifications (SDOUT at 25 pF)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Logic inputs							
I_{IH}	High-level input current	DV_{DD} = 5 V,	V_I = 5 V			1	µA
I_{IL}	Low-level input current	DV_{DD} = 5 V,	V_I = 0 V			–1	µA
C_I	Input capacitance	Control inputs			5	15	pF
Logic outputs							

V_{OH}	High-level output voltage	I_{OH} = 50 µA – 0.5 mA	DV_{DD}–0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA – 0.5 mA	0.4	V
I_{OZH}	High-impedance-state output current		1	µA
I_{OZL}	Low-impedance-state output current		–1	µA
C_O	Output capacitance		5	pF

electrical characteristics, over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted) (continued)

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
Accuracy						
	Integral nonlinearity, INL	Best fit		±0.6	±1	LSB
	Differential nonlinearity, DNL			±0.65	±1	LSB
E_O	Offset error			±0.1	±0.15	%FSR
E_G	Gain error			±0.1	±0.2	%FSR
Analog input						
C_i	Input capacitance			15	20	pF
I_{lkg}	Input leakage current	V_{AIN} = 0 V to AV_{DD}			±1	µA
$R_{i(MUX)}$	Input MUX ON resistance	DV_{DD} = 3 V, AV_{DD} = 3 V		265	780	Ω
		DV_{DD} = 5 V, AV_{DD} = 5 V		235	450	Ω
$R_{i(ADC)}$	Input MUX ON resistance	DV_{DD} = 3 V, AV_{DD} = 3 V		158	465	Ω
		DV_{DD} = 5 V, AV_{DD} = 5 V		140	268	Ω
Voltage reference						
REF	Internal reference voltage	Internal reference mode, V_{DD} = 3 V	2.08	2.26	2.48	V
		Internal reference mode, V_{DD} = 5 V	3.48	3.82	4.15	V
	Temperature coefficient			100		ppm/°C
r_i	Input resistance	External reference mode	3			kΩ
$C_{i(VR)}$	Input capacitance	External reference mode		300		pF
Power supply						
$I_{DD} + I_{REF}$	Operating supply current	AV_{DD} = 2.7 V, DV_{DD} = 2.7 V, f_{SCLK} = 10 MHz†		3	5	mA
		AV_{DD} = 5.5 V, DV_{DD} = 5.5 V, f_{SCLK} = 20 MHz‡		7.2	8.5	mA
P_D	Power dissipation	AV_{DD} = 2.7 V, DV_{DD} = 2.7 V		8	13	mW
		AV_{DD} = 5.5 V, DV_{DD} = 5.5 V		40	47	mW
	Supply current in power down, Software, $I_{DD} + I_{REF}$	AVDD = 2.7 V, $\overline{CS}$ = AV_{DD}		3	10	µA
		AVDD = 2.7 V, $\overline{CS}$ = AGND		500		µA
		AVDD = 5.5 V, $\overline{CS}$ = AV_{DD}		3	10	µA
		AVDD = 5.5 V, $\overline{CS}$ = AGND		2000		µA
	Supply current in power down, Auto, $I_{DD} + I_{REF}$	AVDD = 2.7V		175	275	µA
		AVDD = 5.5V		200	300	µA

† I_{REF} = 0.7 mA typ.
‡ I_{REF} = 1.5 mA typ.

electrical characteristics, over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_i = 100 kHz, 70% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference	58	61		dB
				Internal reference	53	56		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference	56	61		
				Internal reference	53	55		
		f_i = 50 kHz, 90% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		61		
				Internal reference		56		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		61		
				Internal reference		55		
SINAD	Signal-to-noise ratio + distortion	f_i = 100 kHz, 70% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference	55	58		dB
				Internal reference	53	55		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference	53	58		
				Internal reference	52	54		
		f_i = 50 kHz, 90% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		59		
				Internal reference		55		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		60		
				Internal reference		55		
THD	Total harmonic distortion	f_i = 100 kHz, 70% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		–60	–55	dB
				Internal reference		–70	–58	
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		–60	–55	
				Internal reference		–66	–58	
		f_i = 50 kHz 90% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		–64		
				Internal reference		–72		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		–63		
				Internal reference		–68		
SFDR	Spurious-free dynamic range	f_i = 100 kHz, 70% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		–63	–57	dB
				Internal reference		–73	–59	
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		–61	–57	
				Internal reference		–68	–60	
		f_i = 50 kHz, 90% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		–66		
				Internal reference		–75		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		–65		
				Internal reference		–70		
ENOB	Effective number of bits	f_i = 100 kHz, 70% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference	8.8	9.3		dB
				Internal reference	8.6	8.9		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference	8.6	9.3		
				Internal reference	8.4	8.8		
		f_i = 50 kHz, 90% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	External reference		9.5		
				Internal reference		8.9		
			f_S = 625 KSPS, AV_{DD} = 3 V	External reference		9.5		
				Internal reference		8.9		

ac specifications (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
	Channel-to-channel crosstalk			–75		dB
BW	Full-power bandwidth	–1 dB full-scale input sine wave	12	15		MHz
		–3 dB full-scale input sine wave		25		MHz
BW	Small-signal bandwidth	–1 dB	15	20		MHz
		–3 dB		35		MHz
f_S	Sampling rate	AV_{DD} = 5 V	0.0625		1.25	MSPS
		AV_{DD} = 3 V	0.0625		0.625	

timing requirements†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(SCLK)}$	SCLK cycle time	DV_{DD} = 5.5 V to 4.5 V	50			ns
		DV_{DD} = 3.6 V to 2.7 V	100			
$t_{w(1)}$	Pulse duration, chip select		100			ns
$t_{(s)}$	Sampling period			6		SLCK cycles
$t_{(conv)}$	Conversion period			10		SLCK cycles
$t_{su(1)}$	Setup time, FS to SCLK falling edge in DSP mode		5			ns
$t_{h(1)}$	Hold time, FS to SCLK falling edge in DSP mode		2			ns
$t_{su(2)}$	Setup time, FS to $\overline{CS}$ falling edge in DSP mode		5.5			ns
$t_{h(2)}$	Hold time, FS to $\overline{CS}$ falling edge in DSP mode		9			ns
$t_{d(1)}$	Delay time, FS falling edge to next SCLK falling edge in DSP mode		6			ns
$t_{d(2)}$	Delay time, SCLK rising edge after $\overline{CS}$ falling edge in µC mode		4			ns
$t_{d(3)}$	Delay time, output after SCLK rising edge in µC mode and DSP mode			10	20	ns
$t_{su(3)}$	Setup time, serial input data to SCLK falling edge		10			ns
$t_{h(3)}$	Hold time, serial input data to SCLK falling edge		4			ns
t_r	Rise time		3		200	ns

† Specifications subject to change without notice.

PARAMETER MEASUREMENT INFORMATION

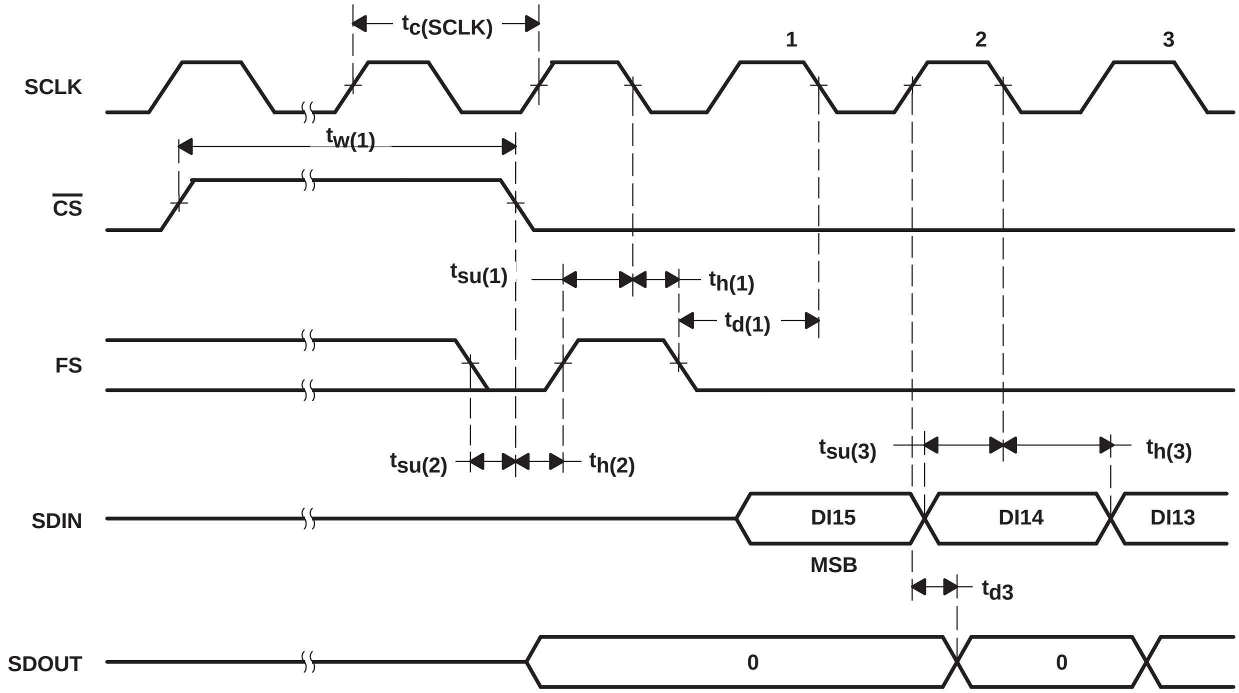


Figure 7. DSP Mode Timing Diagrams

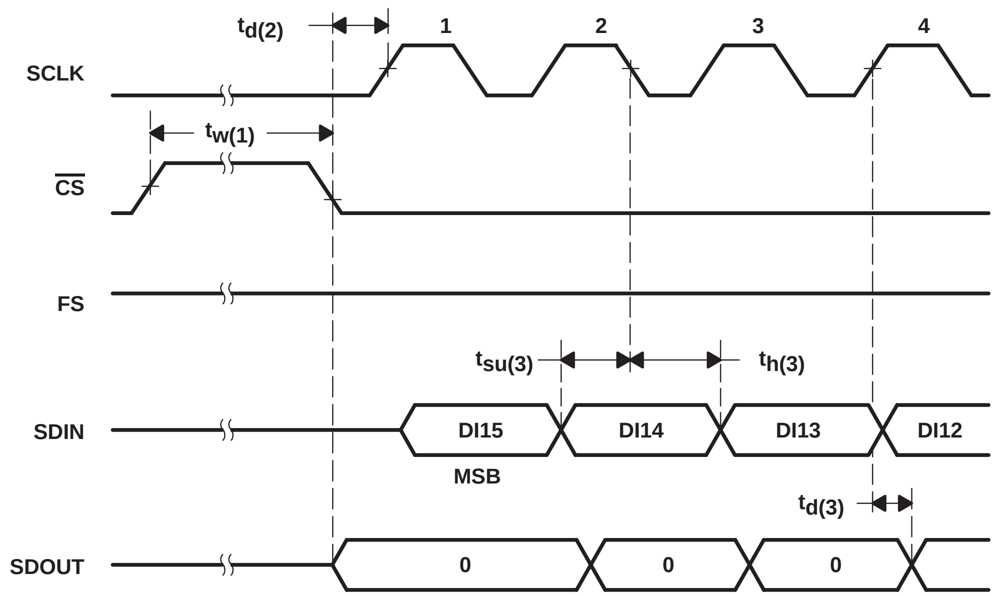


Figure 8. μC Mode Timing Diagrams

TYPICAL CHARACTERISTICS

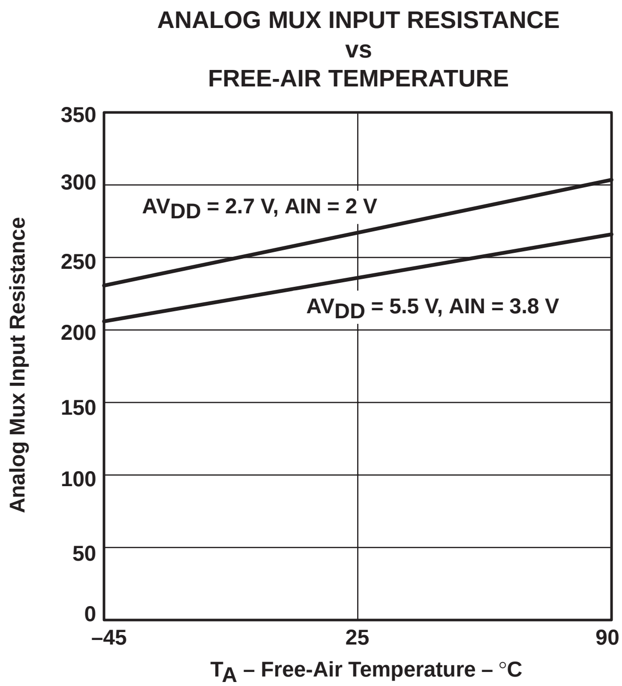


Figure 9

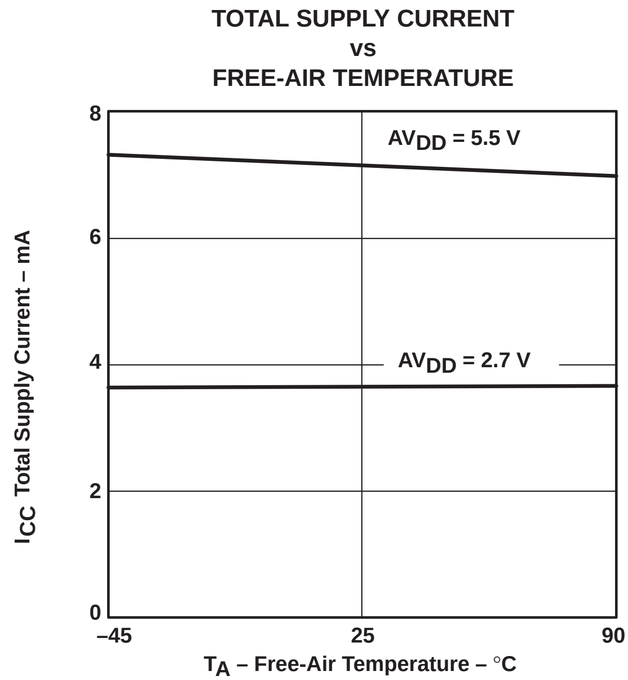


Figure 10

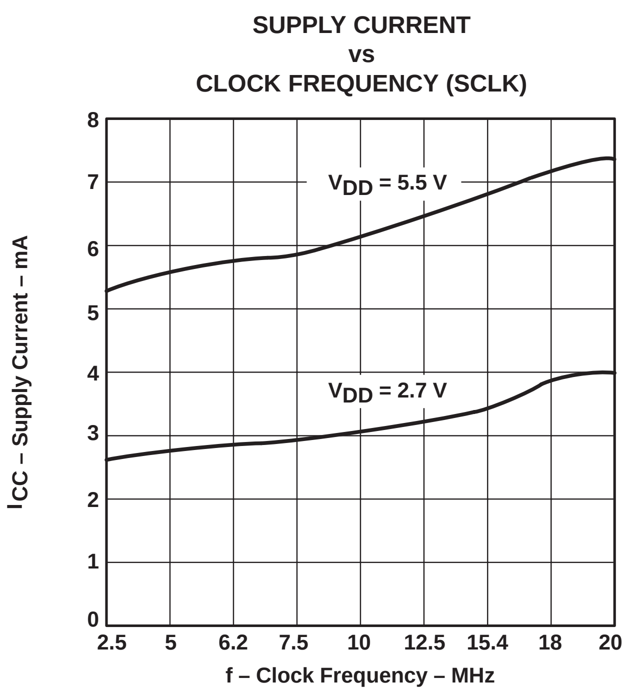


Figure 11

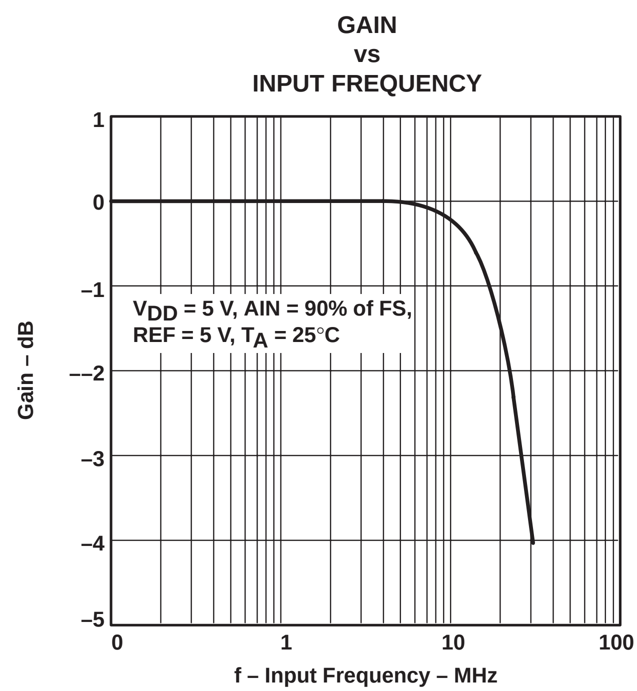


Figure 12

TYPICAL CHARACTERISTICS

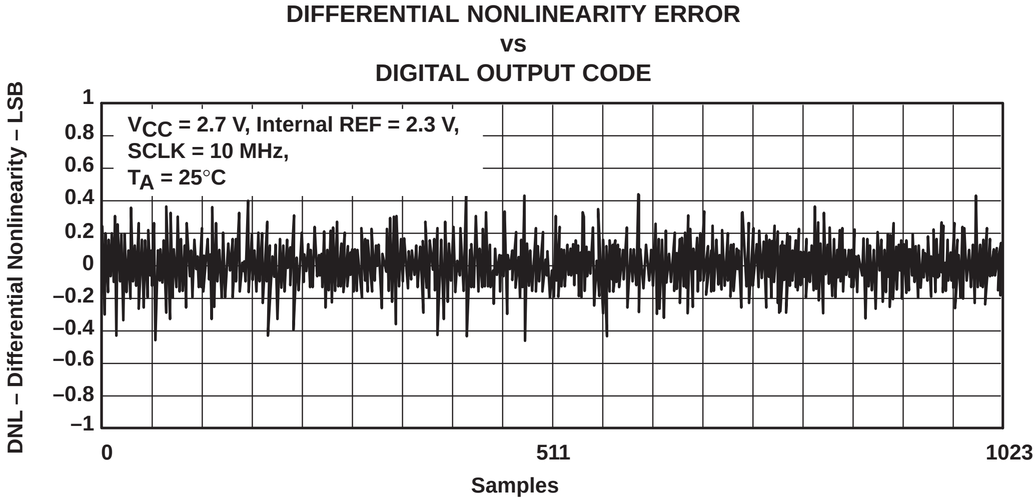


Figure 13

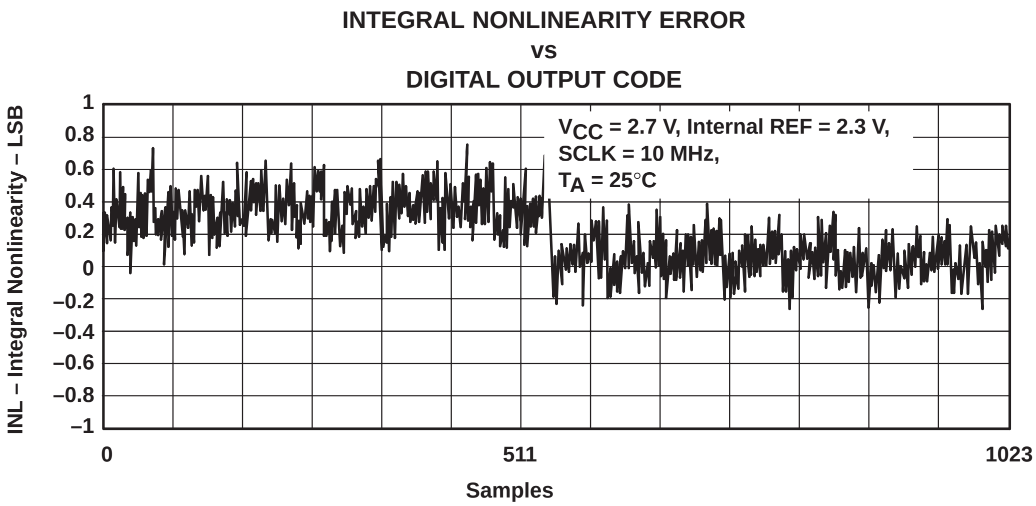


Figure 14

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

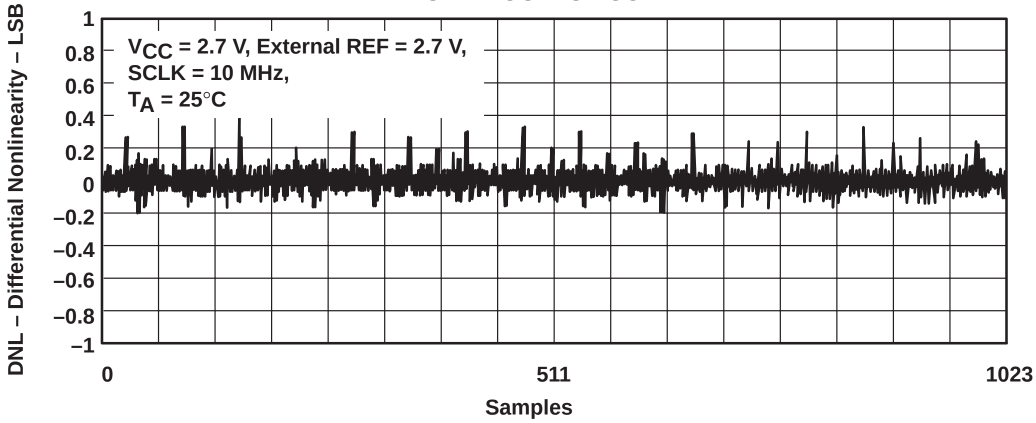


Figure 15

INTEGRAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

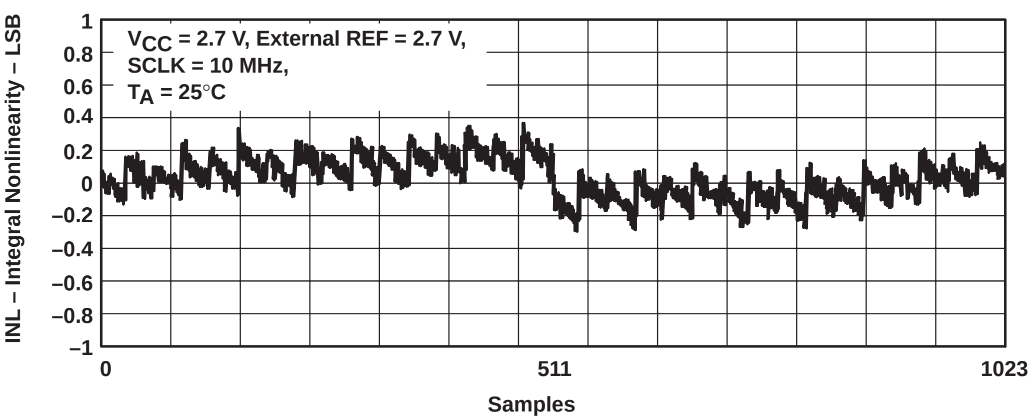


Figure 16

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

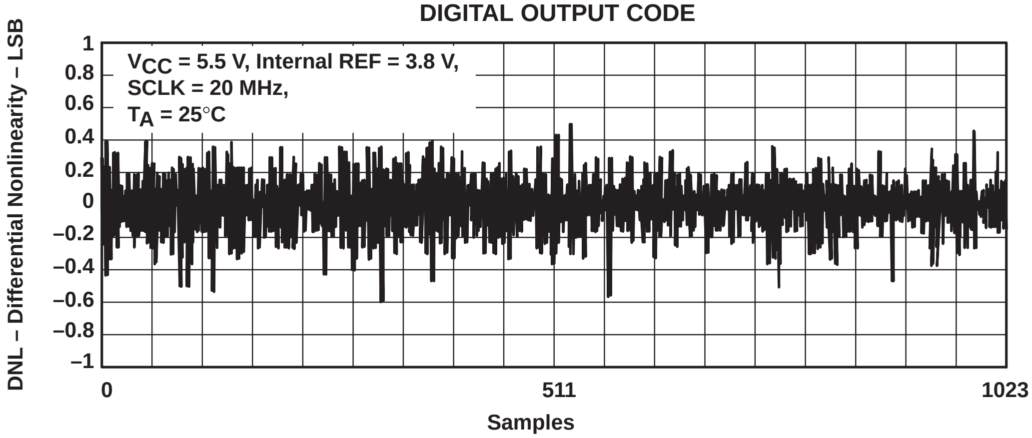


Figure 17

INTEGRAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

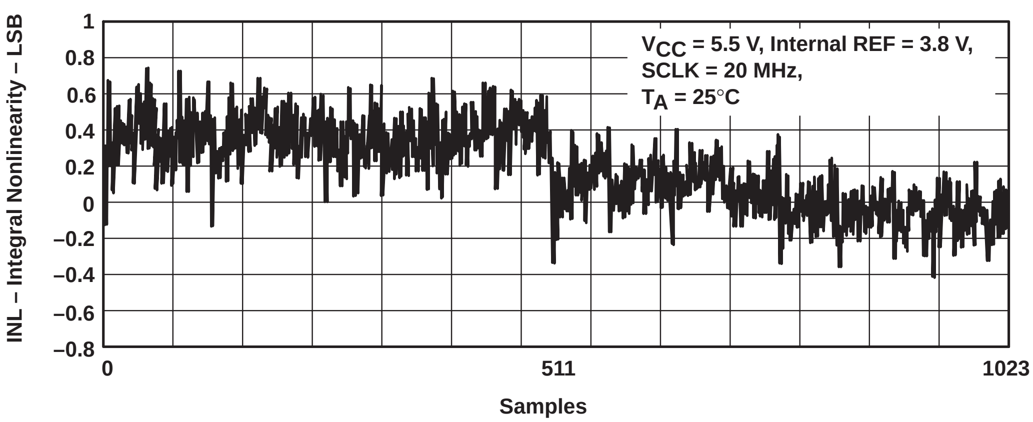


Figure 18

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

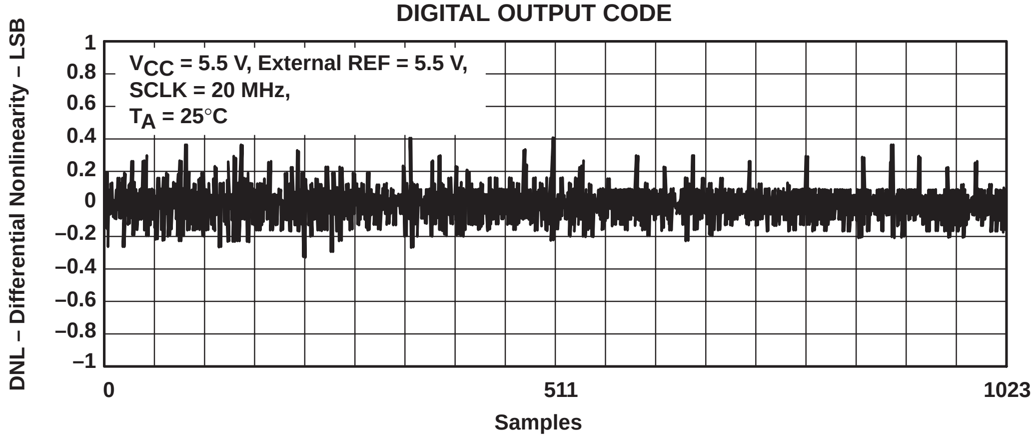


Figure 19

INTEGRAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE

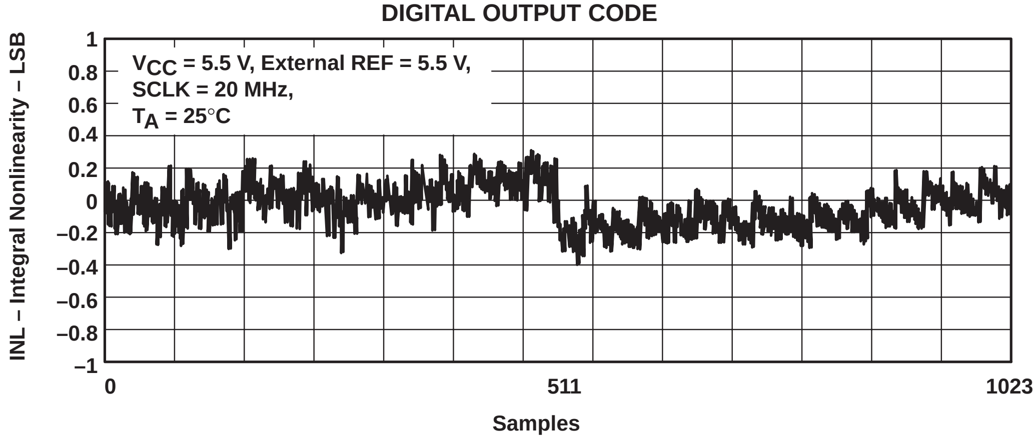


Figure 20

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODE

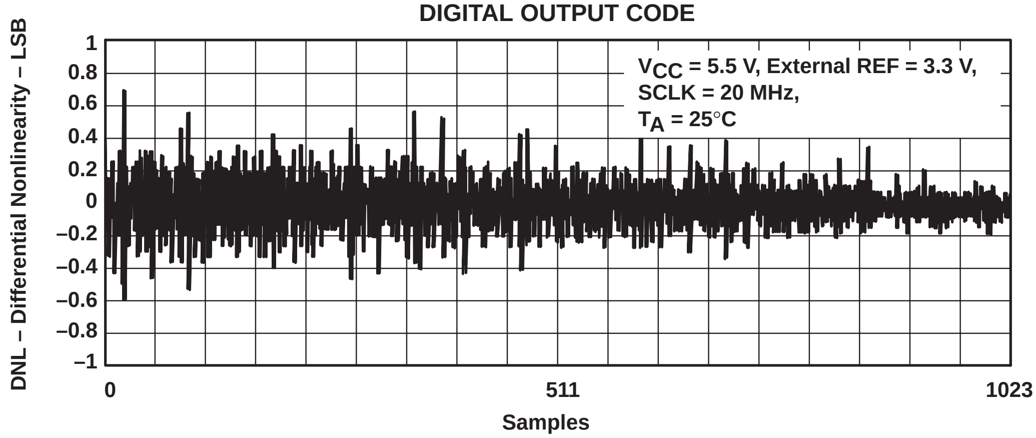


Figure 21

INTEGRAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODE

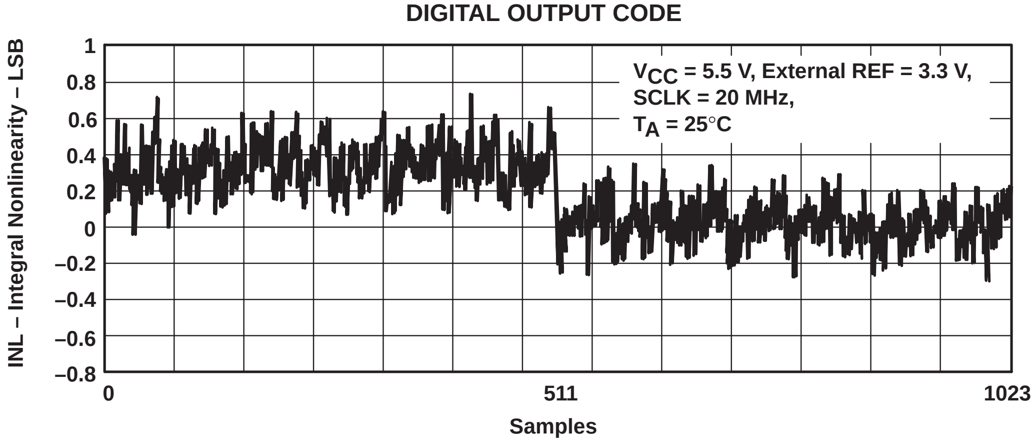


Figure 22

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

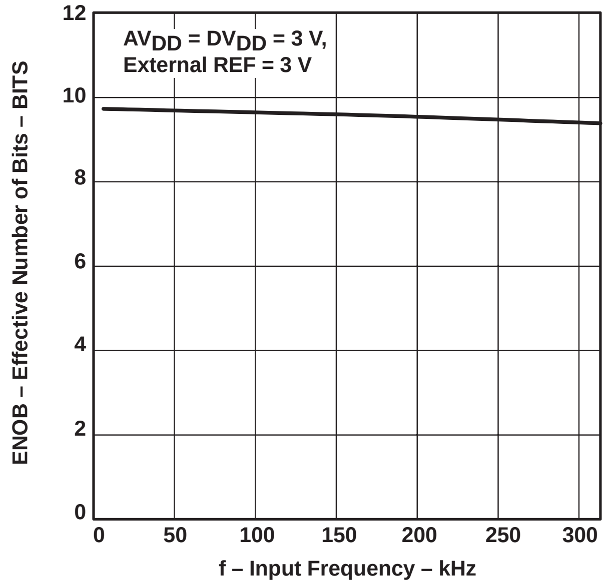


Figure 23

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

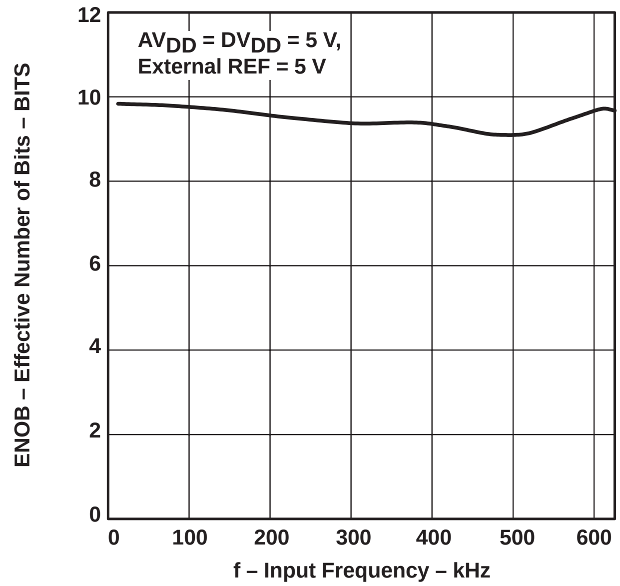


Figure 24

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

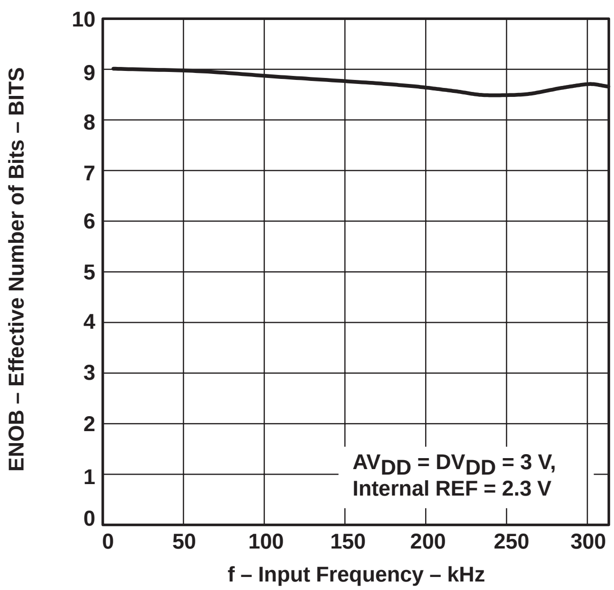


Figure 25

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

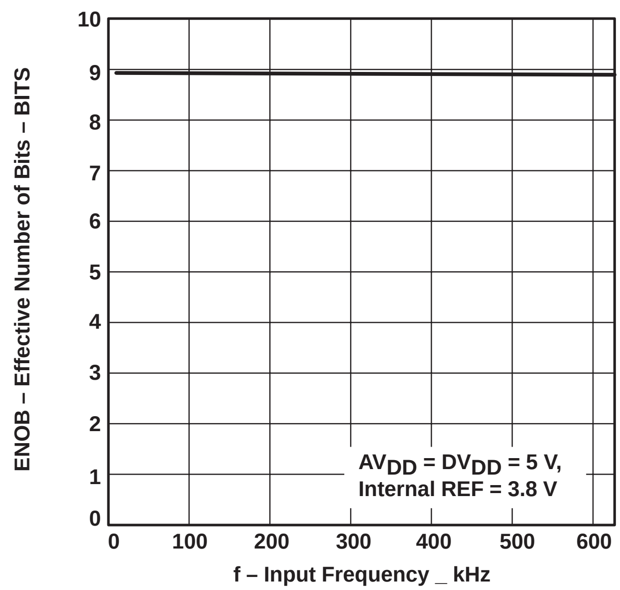


Figure 26

TYPICAL CHARACTERISTICS

**FAST FOURIER TRANSFORM
vs
FREQUENCY**

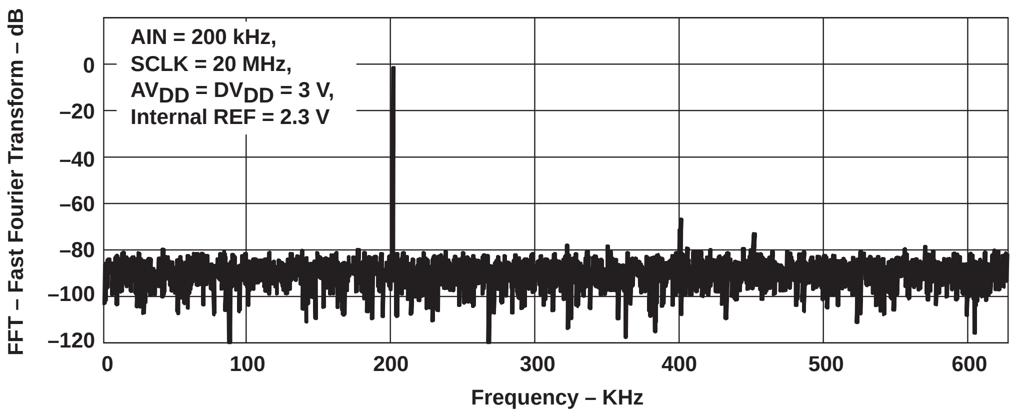


Figure 27

**FAST FOURIER TRANSFORM
vs
FREQUENCY**

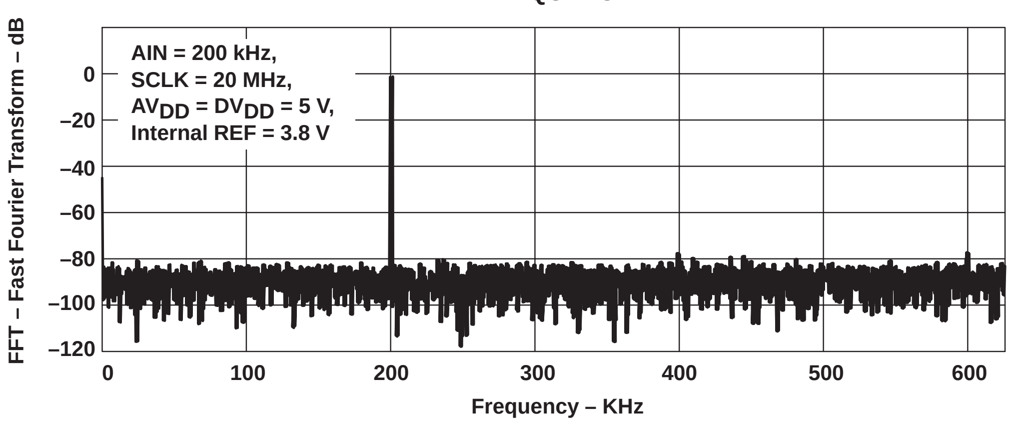


Figure 28

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM
vs
FREQUENCY

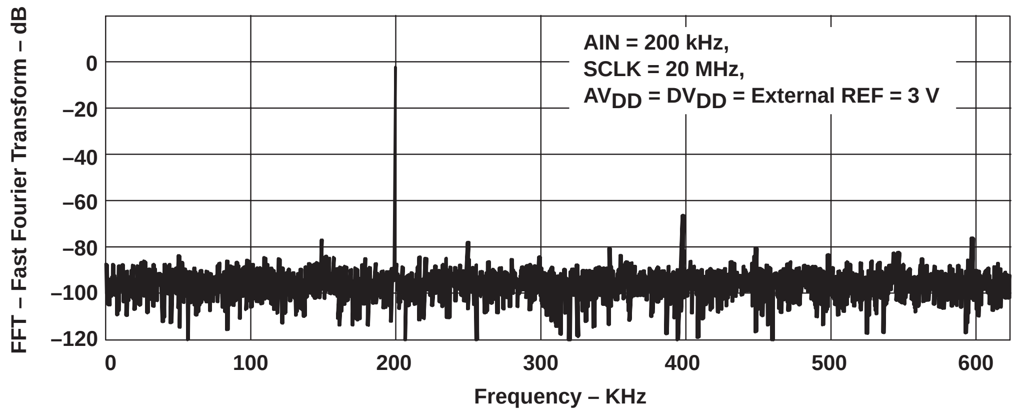


Figure 29

FAST FOURIER TRANSFORM
vs
FREQUENCY

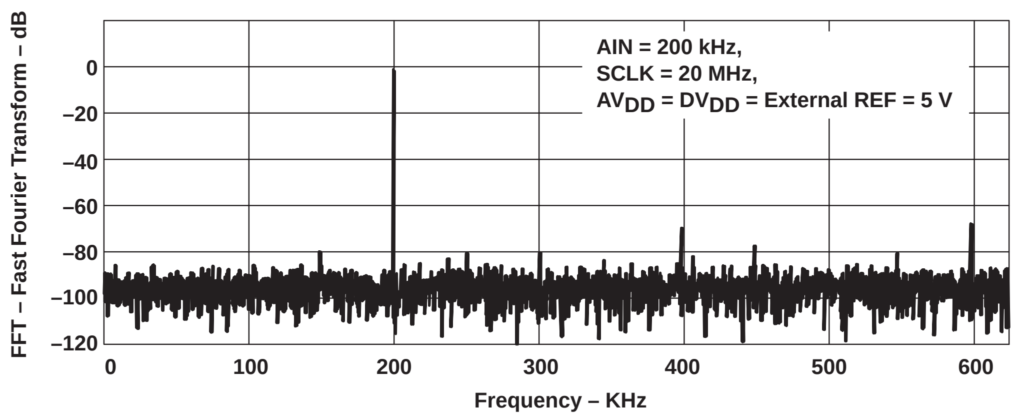


Figure 30

TYPICAL CHARACTERISTICS

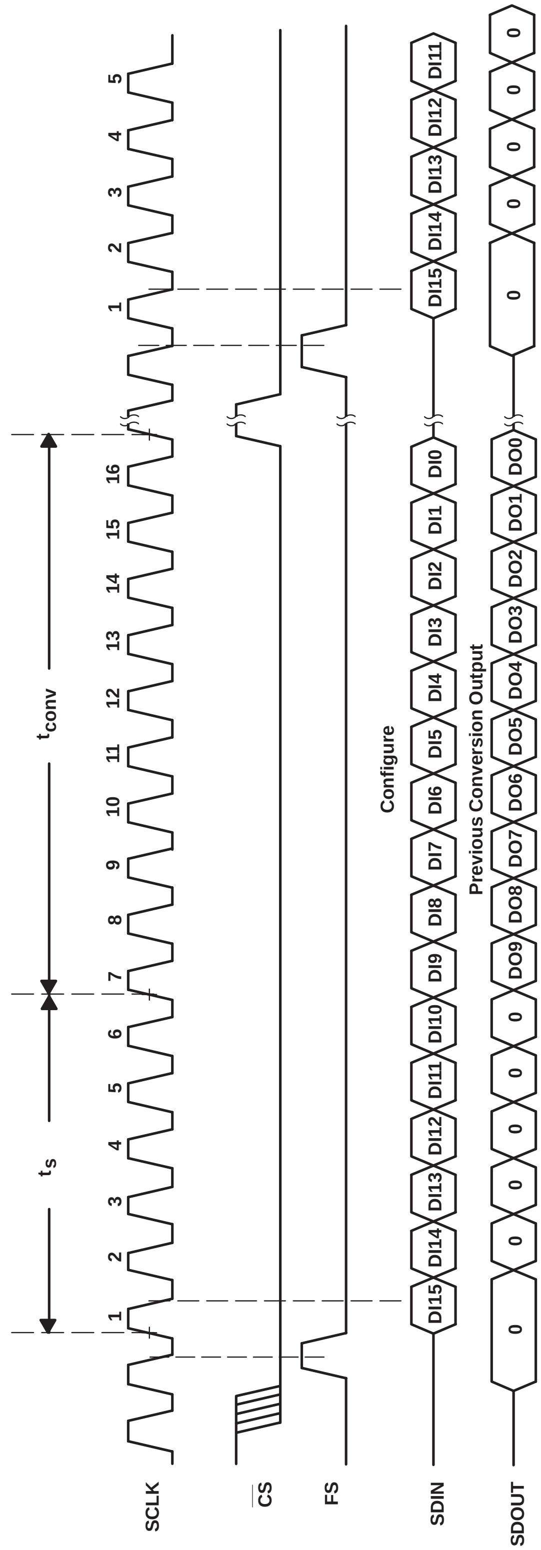


Figure 31. Typical Timing Diagram for DSP Application

TYPICAL CHARACTERISTICS

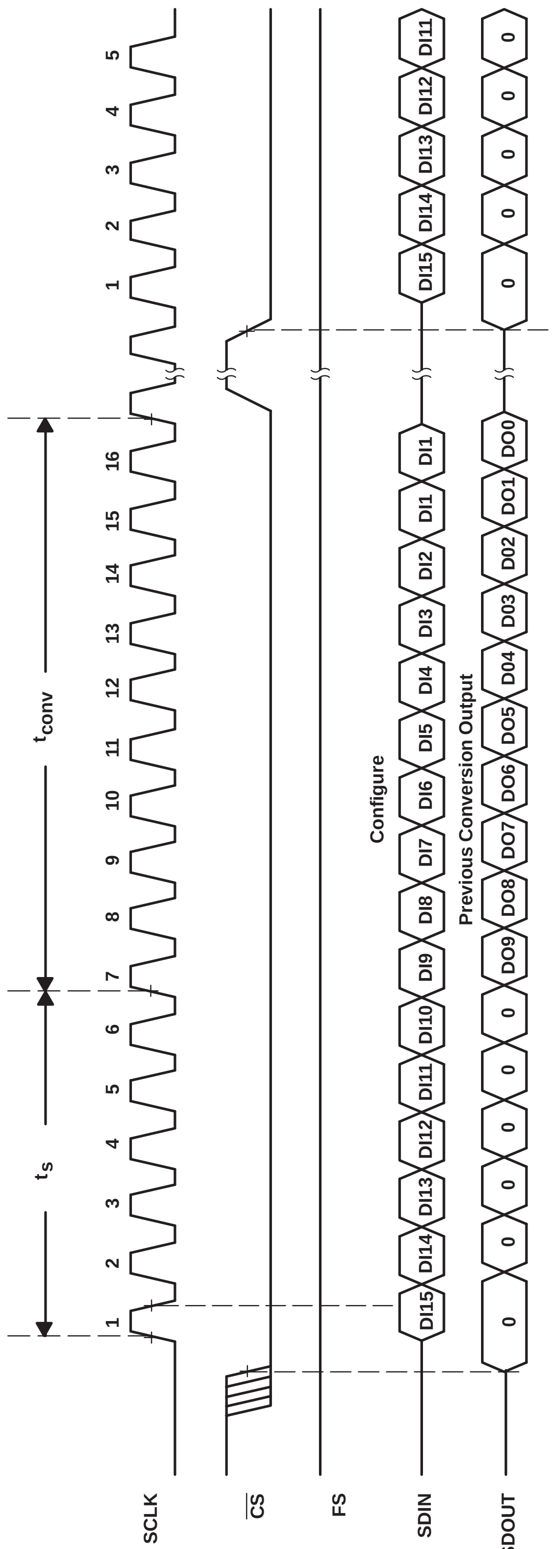


Figure 32. Typical Timing Diagram for µC Application

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLV1570CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570CPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1570IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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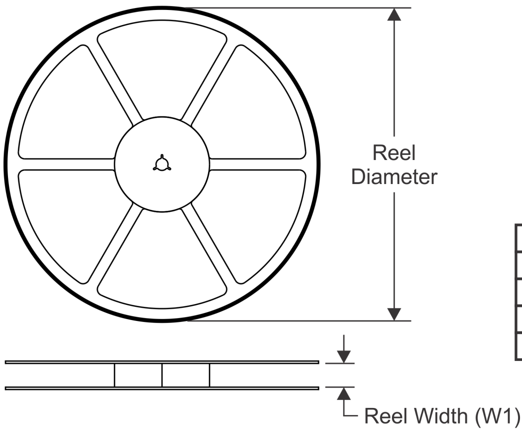
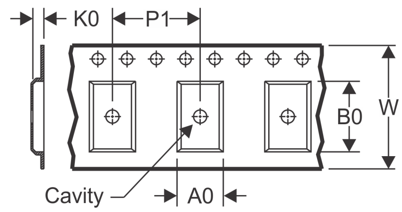
TAPE AND REEL INFORMATION

REEL DIMENSIONS

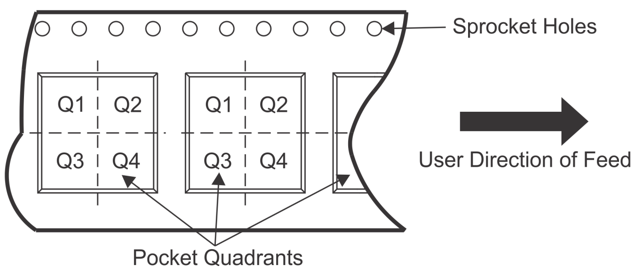


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

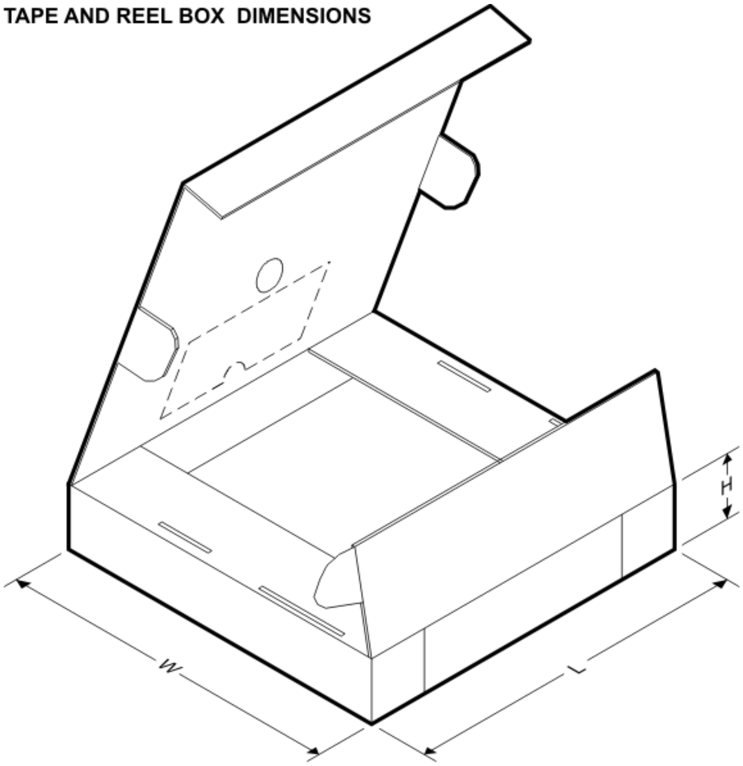
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1570CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV1570CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV1570IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1570CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV1570CPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLV1570IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

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