

TLP700

Industrial inverters
 Inverter for air conditioners
 IGBT/Power MOSFET gate drive

TLP700 consists of a GaAlAs light-emitting diode and an integrated photodetector.

This unit is 6-lead SDIP package. The TLP700 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The TLP700 is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP700 is capable of "direct" gate driving of low-power IGBTs.

- Peak output current: ± 2.0 A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: 2 mA (max)
- Power supply voltage: 15 to 30 V
- Threshold input current: $I_{FLH} = 5$ mA (max)
- Switching time (t_{PLH} / t_{PHL}): 500 ns (max)
- Common mode transient immunity: ± 15 kV/ μs (min)
- Isolation voltage: 5000 Vrms (min)
- Construction mechanical rating

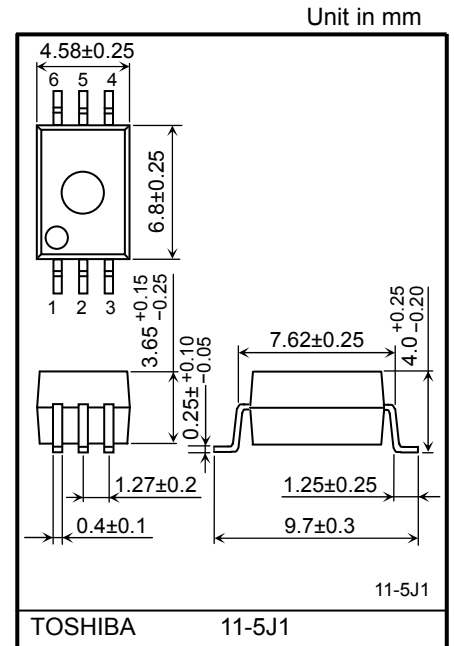
	7.62-mm pitch standard type	10.16-mm pitch TLPXXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

- UL recognized: UL1577, File No. E67349
 - Option (D4) type TÜV approved: EN60747-5-2
- Maximum operating insulation voltage: 890 Vpk
 Highest permissible over voltage: 8000 Vpk

(Note) When a EN60747-5-2 approved type is needed, please designate the "Option(D4)"

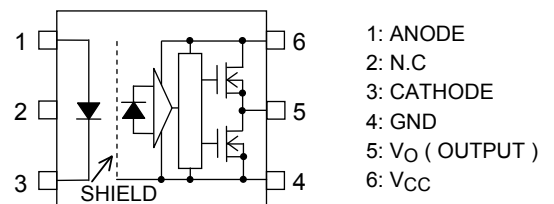
Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

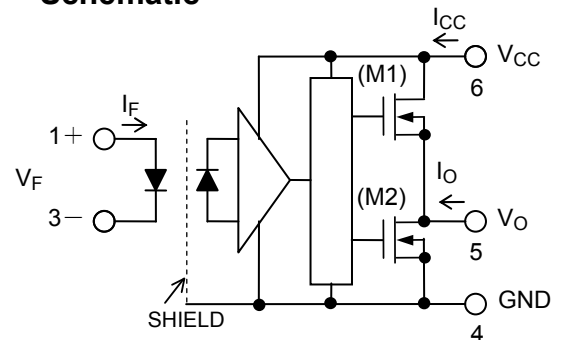


Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



A 0.1- μF bypass capacitor must be connected between pins 6 and 4. (See Note 6.)

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta ≥ 85°C)	ΔI _F /ΔTa	-0.54	mA/°C
	Peak transient forward current (Note 1)	I _{FP}	1	A
	Reverse voltage	V _R	5	V
	Junction temperature	T _j	125	°C
Detector	"H" peak output current	I _{OPH}	-2.0	A
	"L" peak output current			
	Output voltage	V _O	35	V
	Supply voltage	V _{CC}	35	V
	Junction temperature	T _j	125	°C
Operating frequency (Note 3)	f	50	kHz	
Operating temperature range	T _{opr}	-40 to 100	°C	
Storage temperature range	T _{stg}	-55 to 125	°C	
Lead soldering temperature (10 s) (Note 4)	T _{sol}	260	°C	
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)	BV _S	5000	V _{rms}	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 0.3 μs, f ≤ 15 kHz

Note 3: Exponential waveform I_{OPH} ≥ -1.5 A (≤ 0.3 μs), I_{OPL} ≤ +1.5 A (≤ 0.3 μs), Ta=100°C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Note 6: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	I _F (ON)	7.5	—	10	mA
Input voltage, OFF	V _F (OFF)	0	—	0.8	V
Supply voltage *	V _{CC}	15	—	30	V
Peak output current	I _{OPH} / I _{OPL}	—	—	± 1.5	A
Operating temperature	T _{opr}	-40	—	100	°C

* This item denotes operating ranges, not meaning of recommended operating conditions.

Note : Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) ≤ 0.5 μs.

Note 8: If the V_{cc} rise slope is sharp, an internal circuit might not operate with stability. Please design the V_{cc} rise slope under 3.0 V/μs.

Electrical Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Forward voltage		V _F	—	I _F = 10 mA, Ta = 25 °C	—	1.57	1.75	V	
Temperature coefficient of forward voltage		ΔV _F /ΔTa	—	I _F = 10 mA	—	-1.8	—	mV/°C	
Input reverse current		I _R	—	V _R = 5 V, Ta = 25 °C	—	—	10	μA	
Input capacitance		C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	100	—	pF	
Output current (Note 9)	"H" Level	I _{OPH1}	1	V _{CC} = 15 V I _F = 5 mA	V ₆₋₅ = 3.5 V	—	-1.4	-1.0	A
		I _{OPH2}			V ₆₋₅ = 7 V	—	—	-1.5	
	"L" Level	I _{OPL1}	2	V _{CC} = 15 V I _F = 0 mA	V ₅₋₄ = 2.5 V	1.0	1.4	—	
		I _{OPL2}			V ₅₋₄ = 7 V	1.5	—	—	
Output voltage	"H" Level	V _{OH}	3	V _{CC1} = +15V, V _{EE1} = -15V R _L = 200Ω, I _F = 5 mA	11	13.7	—	V	
	"L" Level	V _{OL}	4	V _{CC1} = +15V, V _{EE1} = -15V R _L = 200Ω, V _F = 0.8 V	—	-14.9	-12.5		
Supply current	"H" Level	I _{CCH}	5	V _{CC} = 30 V V _O = Open	I _F = 10 mA	—	1.3	2.0	mA
	"L" Level	I _{CCL}	6			I _F = 0 mA	—	1.3	
Threshold input current	L → H	I _{FLH}	—	V _{CC} = 15 V, V _O > 1 V	—	1.8	5	mA	
Threshold input voltage	H → L	V _{FHL}	—	V _{CC} = 15 V, V _O < 1 V	0.8	—	—	V	
Supply voltage		V _{CC}	—	—	15	—	30	V	
UVLO thresh hold		V _{UVLO+}	—	V _O > 2.5V, I _F = 5 mA	11.0	12.5	13.5	V	
		V _{UVLO-}	—	V _O < 2.5V, I _F = 5 mA	9.5	11.0	12.0	V	
UVLO hysteresis		V _{UVLOHYS}	—	—	—	1.5	—	V	

(*): All typical values are at Ta = 25°C

Note 9: Duration of I_O time ≤ 50 μs, 1 pulse

Note 10: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.

It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Isolation Characteristics (Ta = 25 °C)

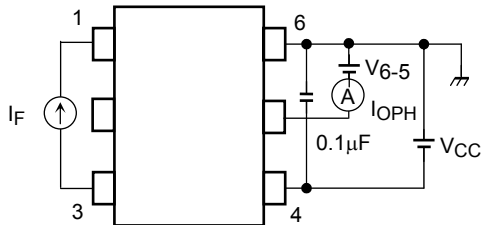
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C _S	V _s = 0 V, f = 1MHz (Note 5)	—	1.0	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V (Note 5)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 1 minute	5000	—	—	V _{rms}
		AC, 1 second, in oil	—	10000	—	V _{rms}
		DC, 1 minute, in oil	—	10000	—	V _{dc}

Switching Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

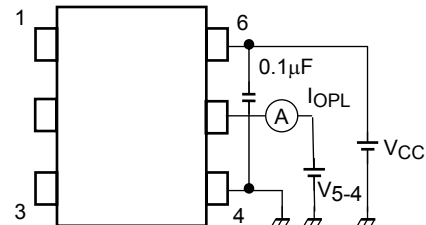
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	V _{CC} = 30 V R _g = 20 Ω C _g = 10 nF	I _F = 0 → 5 mA	50	—	500	ns
	H → L			t _{pHL}	I _F = 5 → 0 mA	50	—	
Output rise time (10–90 %)	t _r	7	V _{CC} = 30 V R _g = 20 Ω C _g = 10 nF	I _F = 0 → 5 mA	—	50	—	
Output fall time (90–10 %)	t _f			I _F = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF	t _{pHL} - t _{pLH}			I _F = 0 ↔ 5 mA	—	—	250	
Common mode transient immunity at HIGH level output	CM _H	8	V _{CM} = 1000 Vp-p Ta = 25 °C V _{CC} = 30 V	I _F = 5 mA V _O (min) = 26 V	-15	—	—	kV/μs
Common mode transient immunity at LOW level output	CM _L			I _F = 0 mA V _O (max) = 1 V	15	—	—	

(*): All typical values are at Ta = 25 °C.

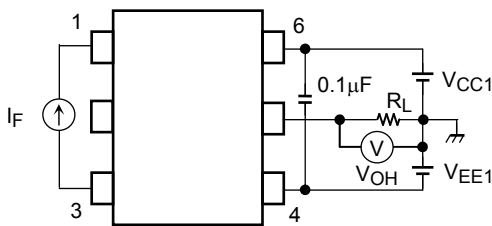
Test Circuit 1: I_{OPH}



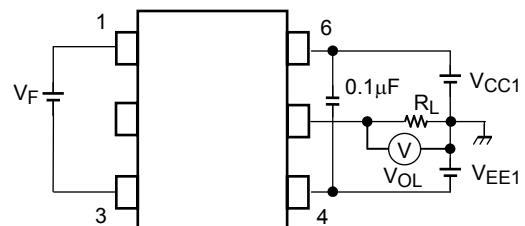
Test Circuit 2: I_{OPL}



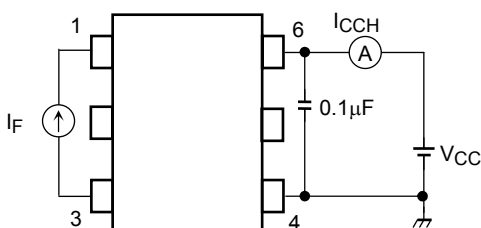
Test Circuit 3: V_{OH}



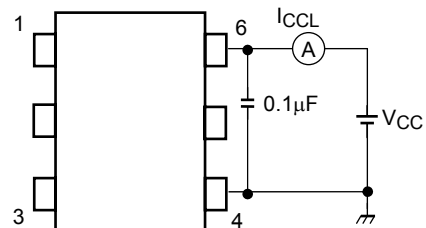
Test Circuit 4: V_{OL}



Test Circuit 5: I_{CCH}

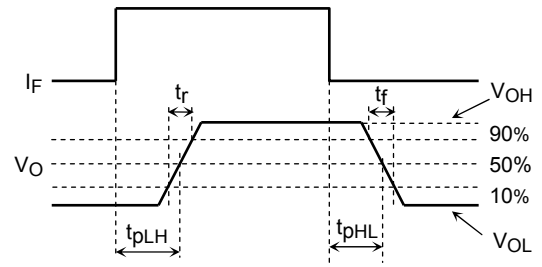
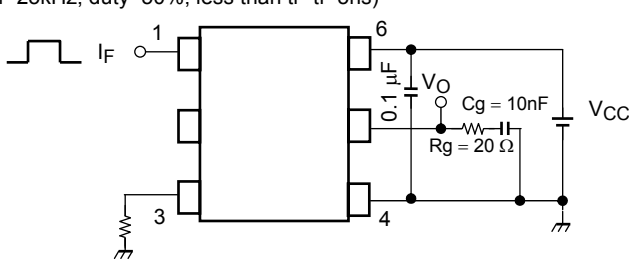


Test Circuit 6: I_{CCL}

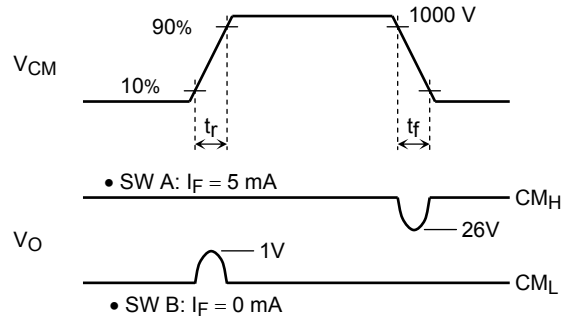
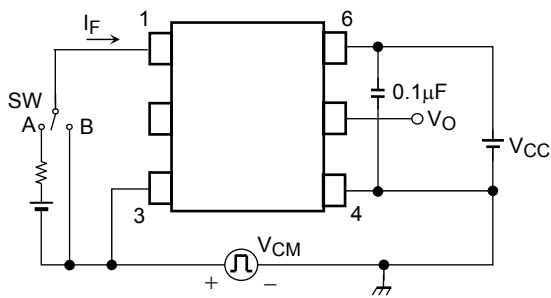


Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , $|t_{pHL}-t_{pLH}|$

($f=25\text{kHz}$, $\text{duty}=50\%$, less than $t_r=t_f=5\text{ns}$)



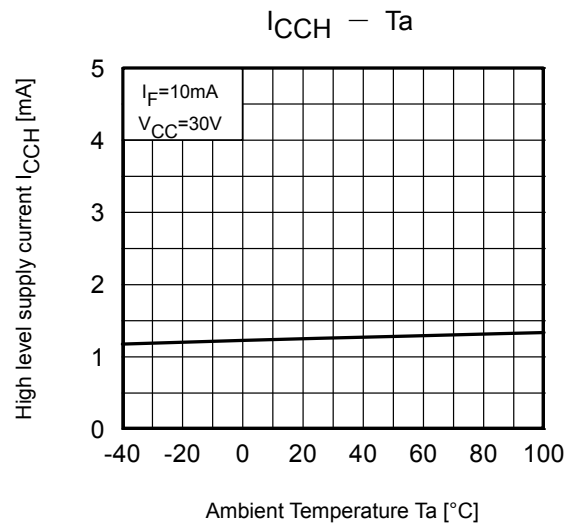
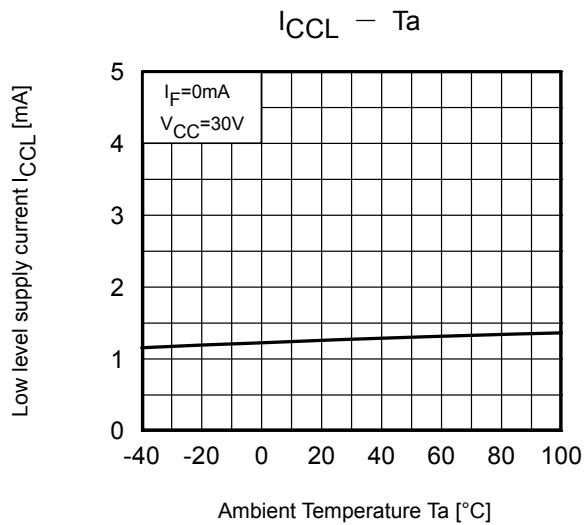
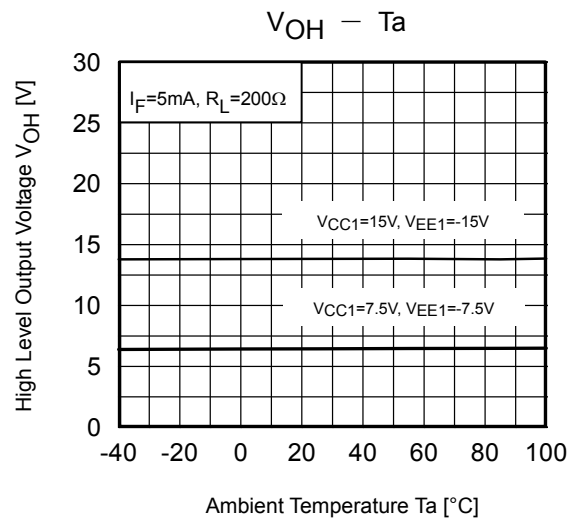
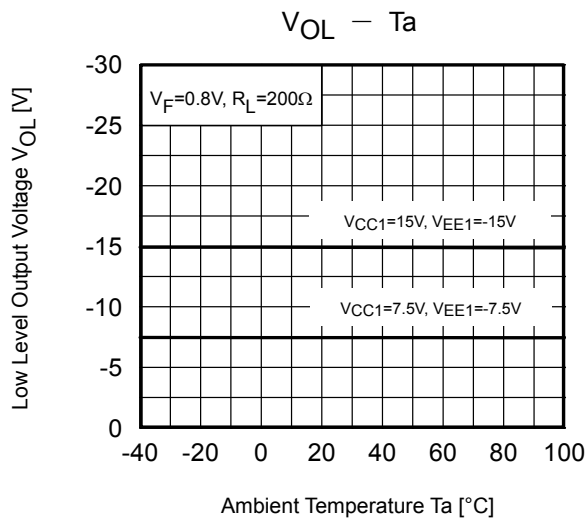
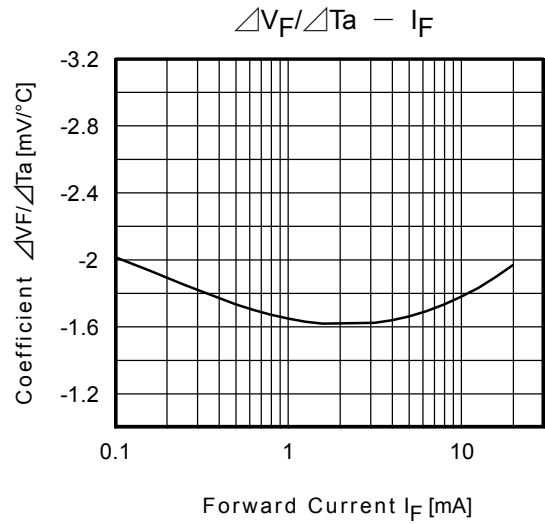
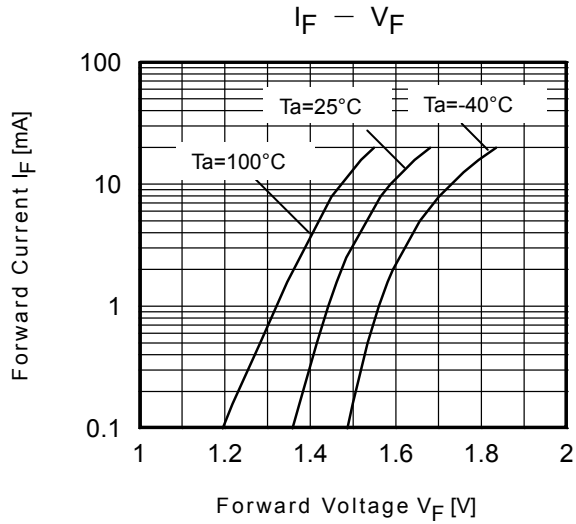
Test Circuit 8: CM_H , CM_L



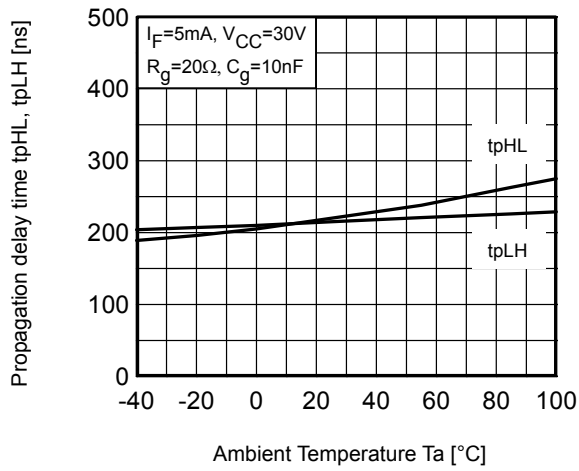
$$CM_H = - \frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$$CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

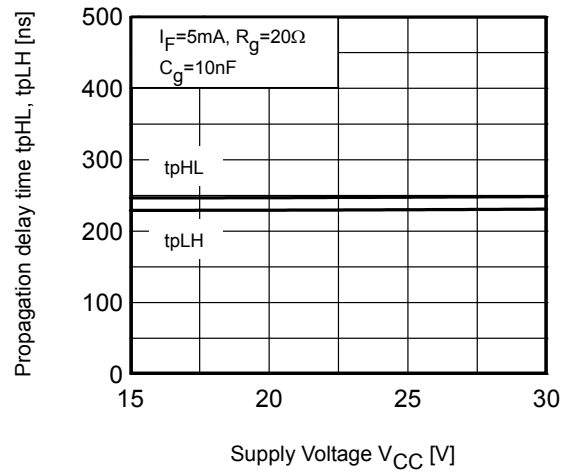
CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.



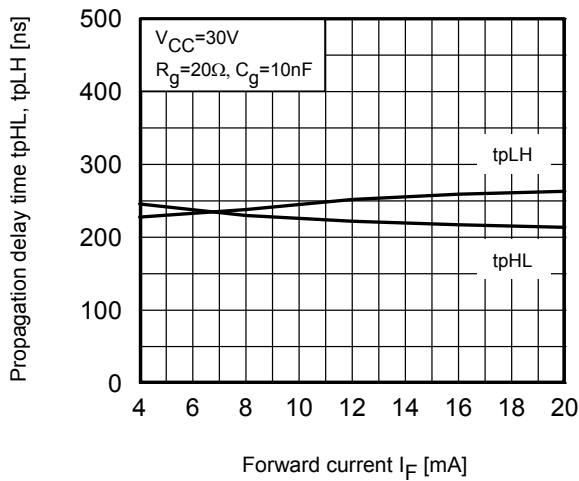
$t_{PLH}, t_{PHL} - T_a$



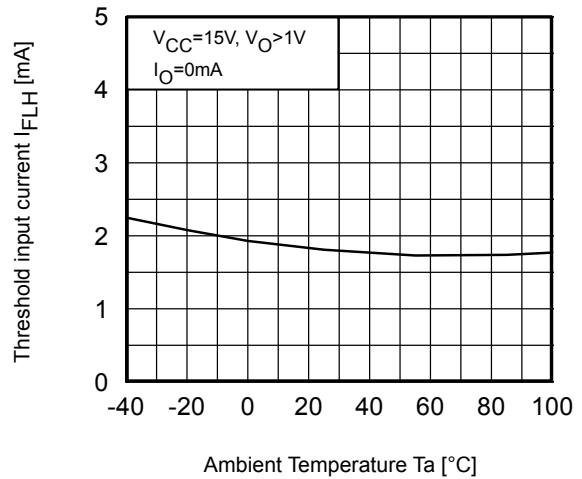
$t_{PLH}, t_{PHL} - V_{CC}$



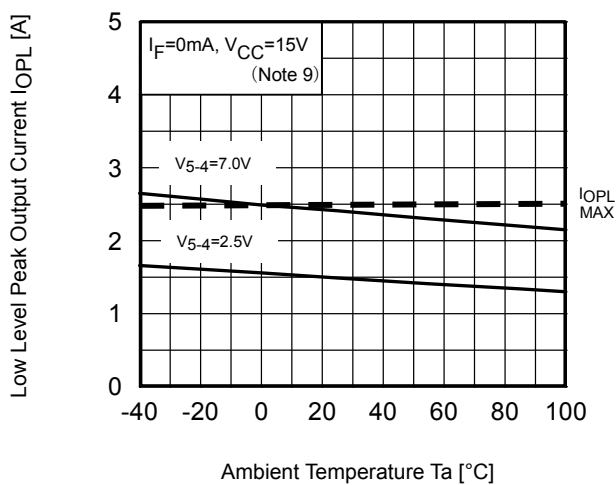
$t_{PLH}, t_{PHL} - I_F$



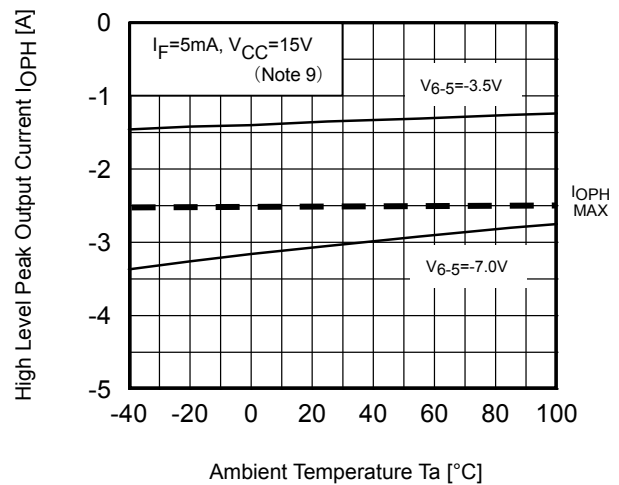
$I_{FLH} - T_a$



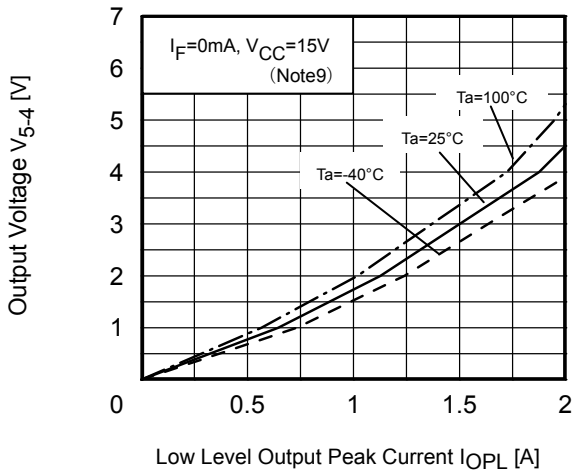
$I_{OPL} - T_a$



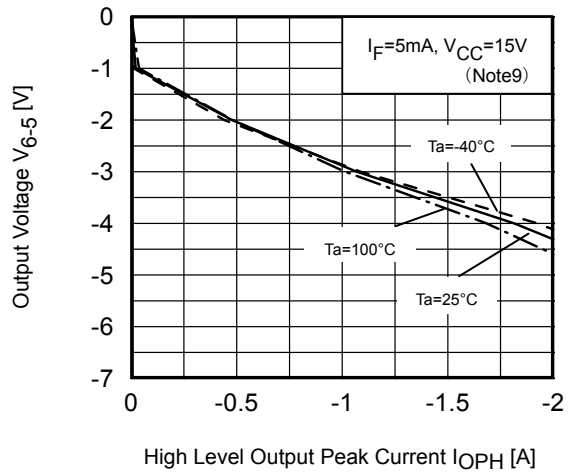
$I_{OPH} - T_a$



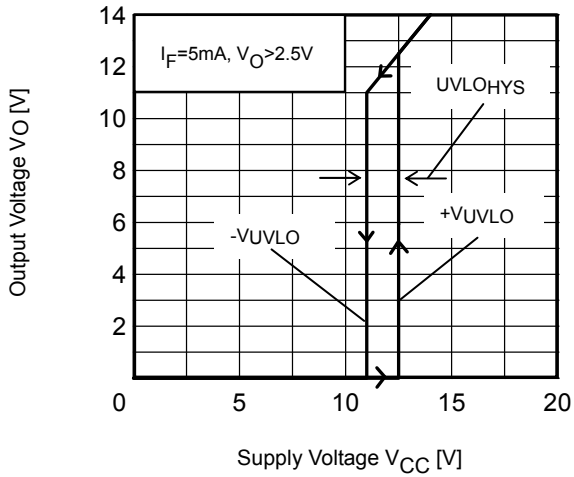
V₅₋₄ - I_{OPL}



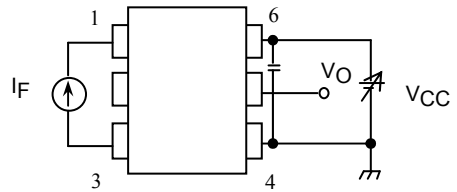
V₆₋₅ - I_{OPH}



V_O(VUVLO)** - V_{CC}



**Test Circuit : V_O(VUVLO) - V_{CC}



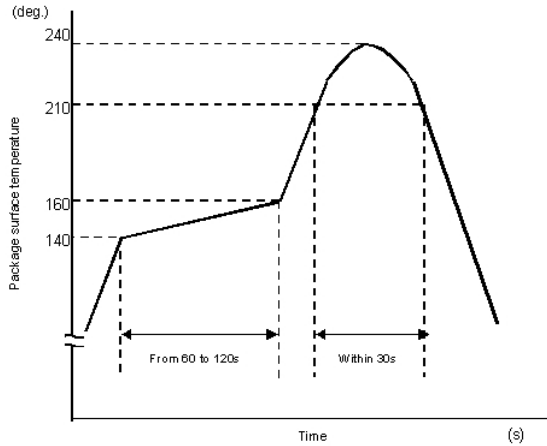
*: The above graphs show typical characteristics.

Soldering and Storage

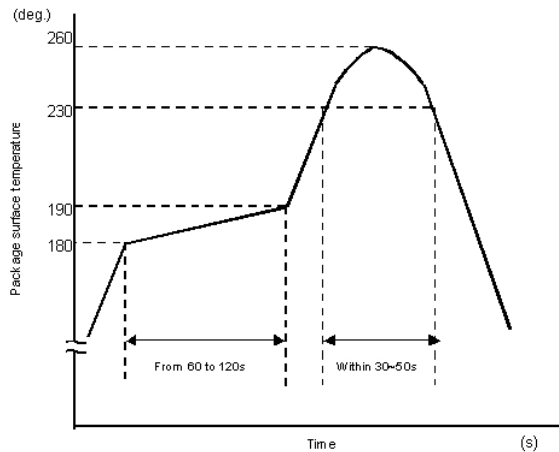
(1) Precautions for Soldering

1) When Using Soldering Reflow

- An example of a temperature profile when Sn-Pb eutectic solder is used:



- An example of a temperature profile when lead(Pb)-free solder is used:



- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

2) When using soldering Flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Apply preheating of 150 deg.C for 60 to 120 seconds.
- Mounting condition of 260 deg.C or less within 10 seconds is recommended.
- Flow soldering must be performed once

3) When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Complete soldering within 10 seconds for lead temperature not exceeding 260 deg.C or within 3 seconds not exceeding 350 deg.C.
- Heating by soldering iron must be only once per 1 lead

(2) Precautions for General Storage

- 1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.
- 2) When transportation or storage of devices, follow the cautions indicated on the carton box.
- 3) The storage area temperature should be kept within a temperature range of 5 degree C to 35 degree C, and relative humidity should be maintained at between 45% and 75%.
- 4) Do not store devices in the presence of harmful (especially corrosive)gases, or in dusty conditions.
- 5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.
- 6) When repacking devices, use anti-static containers.
- 7) Do not apply any external force or load directly to devices while they are in storage.
- 8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.

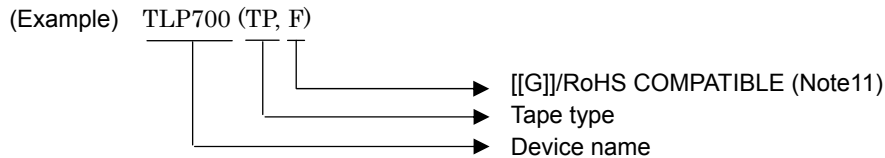
Specifications for Embossed-Tape Packing (TP) for SDIP6 Type Photocoupler

1. Applicable Package

Package Name	Product Type
SDIP6	Photocouplers

2. Product Naming System

Type of package used for shipment is denoted by a symbol suffix after a product number. The method of classification is as below.



3. Tape Dimensions

3.1 Orientation of Devices in Relation to Direction of Tape Movement

Device orientation in the recesses is as shown in Figure 1.

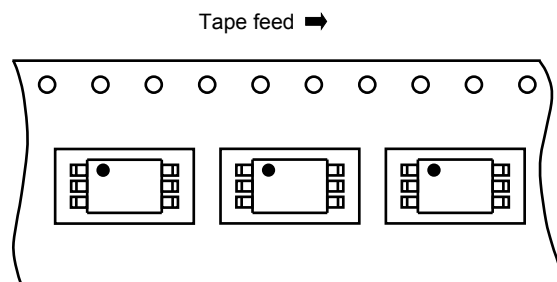


Figure 1 Device Orientation

3.2 Tape Packing Quantity: 1500 devices per reel

3.3 Empty Device Recesses Are as Shown in Table 1.

Table 1 Empty Device Recesses

	Standard	Remarks
Occurrences of 2 or more successive empty device recesses	0	Within any given 40-mm section of tape, not including leader and trailer
Single empty device recesses	6 devices (max) per reel	Not including leader and trailer

3.4 Start and End of Tape:

The start of the tape has 30 or more empty holes. The end of the tape has 30 or more empty holes and two empty turns only for a cover tape.

3.5 Tape Specification

- (1) Tape material: Plastic (protection against electrostatics)
- (2) Dimensions: The tape dimensions are as shown in Figure 2 and Table 2.

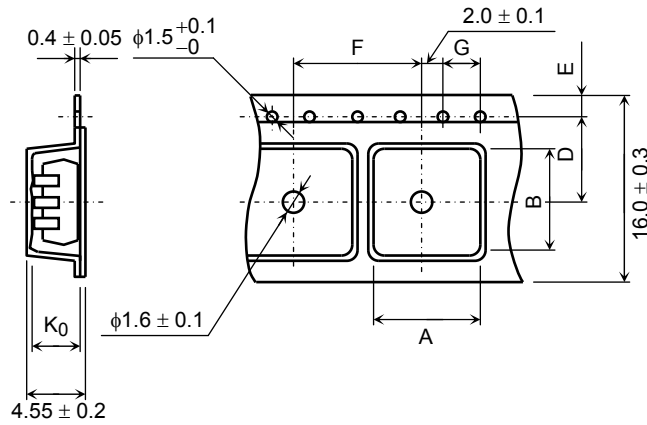


Figure 2 Tape Forms

Table 2 Tape Dimension

Unit: mm
Unless otherwise specified: ±0.1

Symbol	Dimension	Remark
A	10.4	—
B	5.1	—
D	7.5	Center line of indented square hole and sprocket hole
E	1.75	Distance between tape edge and hole center
F	12.0	Cumulative error $\begin{matrix} +0.1 \\ -0.3 \end{matrix}$ (max) per 10 feed holes
G	4.0	Cumulative error $\begin{matrix} +0.1 \\ -0.3 \end{matrix}$ (max) per 10 feed holes
K ₀	4.1	Internal space

3.6 Reel

- (1) Material: Plastic
- (2) Dimensions: The reel dimensions are as shown in Figure 3 and Table 3.

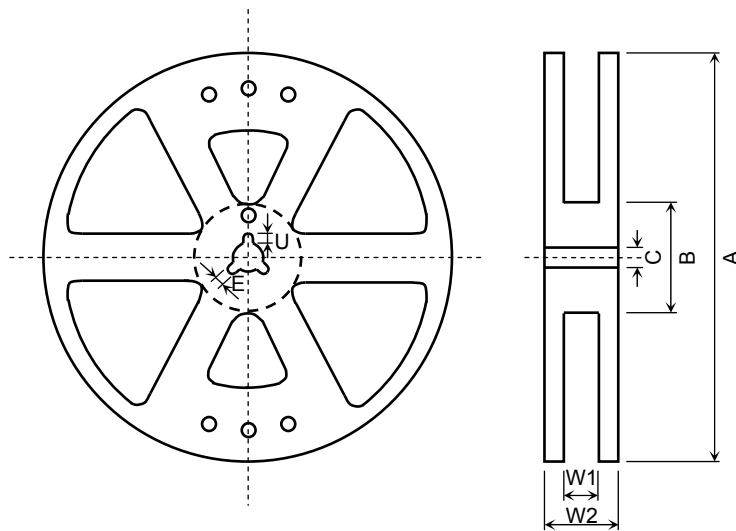


Table 3 Reel Dimension

Unit: mm

記号	寸法
A	$\phi 380 \pm 2$
B	$\phi 80 \pm 1$
C	$\phi 13 \pm 0.5$
E	2.0 ± 0.5
U	4.0 ± 0.5
W1	17.5 ± 0.5
W2	21.5 ± 1.0

Figure 3 Reel Forms

4. Packing

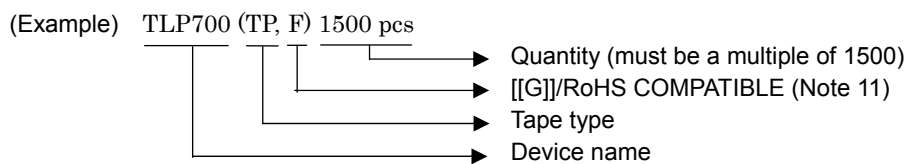
Either one reel or five reels of photocouplers are packed in a shipping carton.

5. Label Indication

The carton bears a label indicating the product number, the symbol representing classification of standard, the quantity, the lot number and the Toshiba company name.

6. Ordering Method


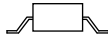
When placing an order, please specify the product number, the CTR rank, the tape type and the quantity as shown in the following example.



Note 11 :Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

Insulation Related Specifications

		 7.62mm pitch TLPxxx type	 10.16mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0mm	8.0mm
Minimum clearance	Cl	7.0mm	8.0mm
Minimum insulation thickness	ti	0.4mm	
Comperative tracking index	CTI	175	

1. If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g.at a standard distance between soldering eye centres of 7.5mm). If this is not permissible, the user shall take suitable measures.
2. This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN60747 : **4**

Marking Example :

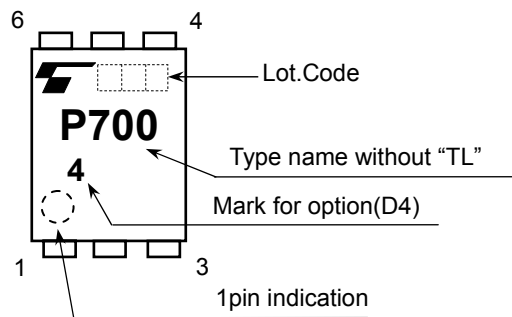


Figure 1 Partial discharge measurement procedure according to EN60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests,
destructive tests)

- t_1, t_2 = 1 to 10 s
- t_3, t_4 = 1 s
- t_p (Measuring time for partial discharge) = 10 s
- t_b = 12 s
- t_{ini} = 60 s

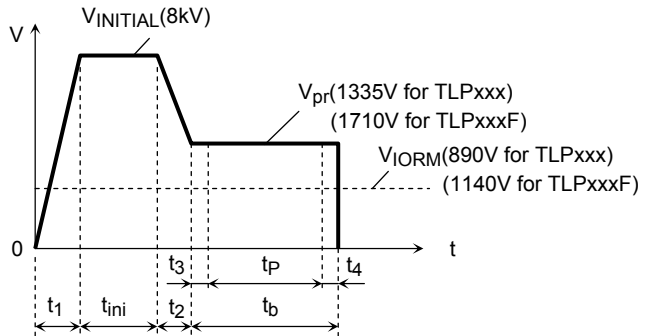


Figure 2 Partial discharge measurement procedure according to EN60747
Non-destructive test for 100% inspection.

Method B

(for sample test, non-destructive test)

- t_3, t_4 = 0.1 s
- t_p (Measuring time for partial discharge) = 1 s
- t_b = 1.2 s

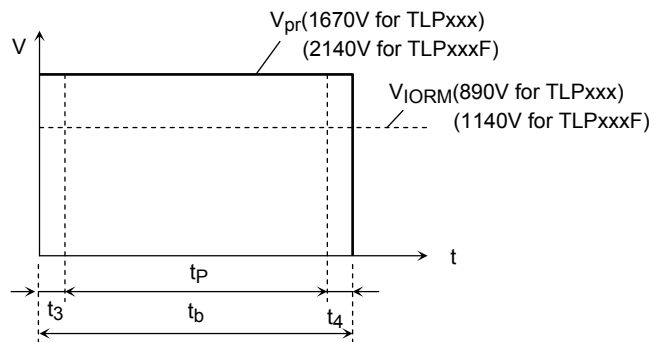
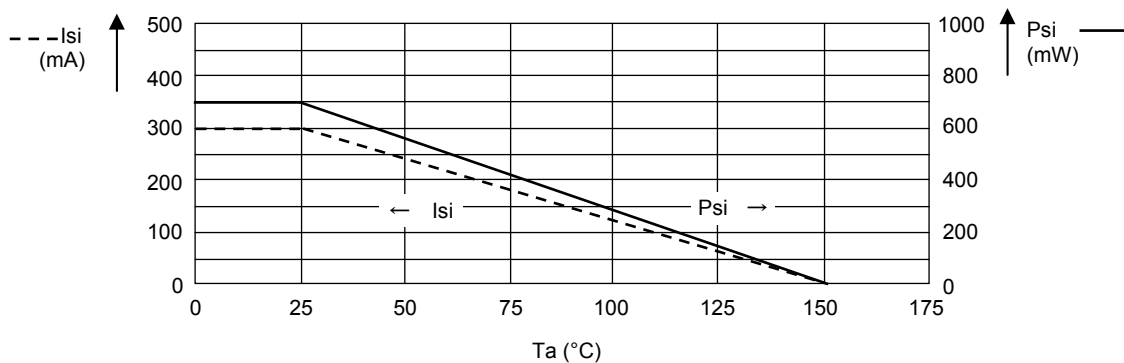


Figure 3 Dependency of maximum safety ratings on ambient temperature



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