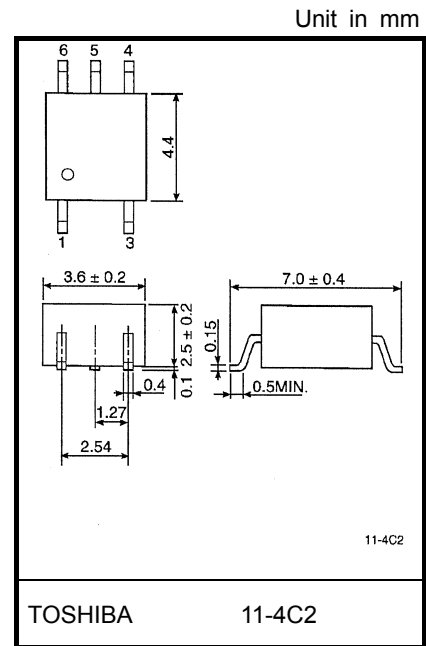


# TLP116

PDP(Plasma Display Panel)  
 High Speed Interface  
 FA(Factory Automation)

The Toshiba TLP116 consists of a GaAlAs light-emitting diode and an integrated high-gain, high-speed photodetector.

- Inverter logic (totempole output)
- Package type : MFSOP6
- Guaranteed performance over temperature : -40~100°C
- Power supply voltage : 4.5~5.5V
- Input thresholds current :  $I_{FHL}=5\text{mA(Max.)}$
- Propagation delay time (tpHL/tpLH) : 60ns(Max.)
- Switching speed : 20MBd(TYP.)
- Common mode transient immunity : 10kV/us
- Isolation voltage : 3750Vrms
- UL Recognized : UL1577,File No.E67349

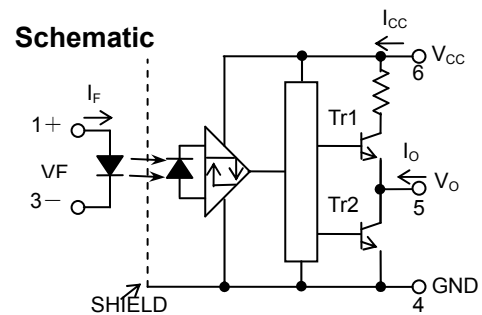
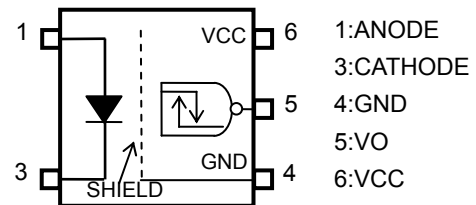


Weight: 0.09 g(Typ.)

**Truth Table**

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

**Pin Configuration (Top View)**



0.1uF bypass capacitor must be connected between pins 6 and 4

**Absolute Maximum Ratings (Ta=25°C)**

Characteristic		Symbol	Rating	Unit
LED	Forward current	$I_F$	20	mA
	Forward current derating (Ta≥85°C)	$\Delta I_F/\Delta T_a$	-0.5	mA/°C
	Peak transient forward current (Note1)	$I_{FPT}$	1	A
	Reverse voltage	$V_R$	5	V
DETECTOR	Output current	$I_O$	10	mA
	Output voltage	$V_O$	6	V
	Supply voltage	$V_{CC}$	6	V
	Output power dissipation	$P_O$	40	mW
Operating temperature range		$T_{opr}$	-40~100	°C
Storage temperature range		$T_{stg}$	-55~125	°C
Lead solder temperature(10s)		$T_{sol}$	260	°C
Isolation voltage (AC, 1min., R.H.≤60%, Ta=25°C) (Note2)		$BVs$	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Recommended Operating Conditions**

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current , ON	$I_{F(ON)}$	8	—	18	mA
Input voltage , OFF	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage (Note3)	$V_{CC}$	4.5	5.0	5.5	V
Operating temperature	$T_{opr}$	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

**Correlation between Input current , switching speed and drive circuit (reference information).**

Input current (IF)	test Circuit	Typical switching speed
12mA	1 (Page 4)	21 – 23 MBd
8mA	1 (Page 4)	18 – 20 MBd
8mA	2 (Page 4, With Speed up capacitor)	23 – 27 MBd

Note1 : Pulse width  $PW \leq 1\mu s, 300pps$ .

Note2 : This device is regarded as a two terminal device : pins 1 and 3 are shorted together, as are pins 4,5 and 6.

Note3 : The detector of this product requires a power supply voltage (VCC) of 4.5 V or higher for stable operation. If the VCC is lower than this value, an ICC may increase, or an output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

## Electrical Characteristics

(Unless otherwise specified, Ta=-40 to 100°C, VCC=4.5~5.5V)

Characteristic	Symbol	Test Circuit	Conditions	Min.	Typ.	Max.	Unit
Input forward voltage	V <sub>F</sub>	—	I <sub>F</sub> =10mA, Ta=25°C	—	1.3	1.5	V
Temperature coefficient of forward voltage	ΔV <sub>F</sub> /ΔTa	—	I <sub>F</sub> =10mA	—	-2.0	—	mV/°C
Input reverse current	I <sub>R</sub>	—	V <sub>R</sub> =5V, Ta=25°C	—	—	10	μA
Input capacitance	C <sub>T</sub>	—	V=0, f=1MHz, Ta=25°C	—	70	—	pF
Logic low output voltage	V <sub>OL</sub>	1	I <sub>OL</sub> =1.6mA, I <sub>F</sub> =12mA, V <sub>CC</sub> =5V	—	—	0.4	V
Logic high output voltage	V <sub>OH</sub>	2	I <sub>OH</sub> =-0.02mA, V <sub>F</sub> =1.05V, V <sub>CC</sub> =5V	4.0	—	—	V
Logic low supply current	I <sub>CCL</sub>	3	I <sub>F</sub> =12mA	—	—	5.0	mA
Logic high supply current	I <sub>CCH</sub>	4	V <sub>F</sub> =0V	—	—	5.0	mA
Input current logic low output	I <sub>FHL</sub>	—	I <sub>O</sub> =1.6mA, V <sub>O</sub> <0.4V	—	—	5	mA
Input voltage logic high output	V <sub>FLH</sub>	—	I <sub>O</sub> =-0.02mA, V <sub>O</sub> >4.0V	0.8	—	—	V

\*All typical values are at Ta=25°C, V<sub>CC</sub>=5V, I<sub>F</sub>(ON)=12mA unless otherwise specified

## Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Capacitance input to output	C <sub>S</sub>	V = 0, f = 1MHz (Note 2)	—	0.8	—	pF
Isolation resistance	R <sub>S</sub>	R.H. ≤ 60%, V <sub>S</sub> = 500V (Note 2)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	BV <sub>S</sub>	AC, 1 minute	3750	—	—	V <sub>rms</sub>
		AC, 1 second, in oil	—	10000	—	V <sub>dc</sub>
		DC, 1 minute, in oil	—	10000	—	

Note 4: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.  
The total lead length between capacitor and coupler should not exceed 1 cm.

## Switching Characteristics

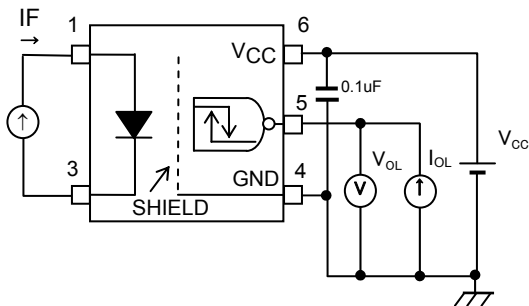
(Unless otherwise specified,  $T_a = -40$  to  $100^\circ\text{C}$ ,  $V_{CC} = 4.5 \sim 5.5\text{V}$ )

Characteristic	Symbol	Test Circuit	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time to logic high output	$t_{pHL}$	5	$I_F = 0 \rightarrow 12\text{mA}$	—	—	60	ns
Propagation delay time to logic low output	$t_{pLH}$		$I_F = 12 \rightarrow 0\text{mA}$				
Propagation delay time to logic high output	$t_{pHL}$	6	$V_{IN} = 0 \rightarrow 5\text{V}$ ( $I_F = 0 \rightarrow 8\text{mA}$ )	—	—	60	ns
Propagation delay time to logic low output	$t_{pLH}$		$V_{IN} = 5 \rightarrow 0\text{V}$ ( $I_F = 8 \rightarrow 0\text{mA}$ )				
Switching time dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $	5	$I_F = 12\text{mA}$ , $R_{IN} = 100\Omega$ , $C_L = 15\text{pF}$ (Note 5)	—	—	30	ns
Output fall time(90-10%)	$t_f$		$I_F = 0 \rightarrow 12\text{mA}$	—	15	—	ns
Output rise time(10-90%)	$t_r$		$I_F = 12 \rightarrow 0\text{mA}$	—	15	—	ns
Common mode transient immunity at high Level output	$CM_H$	7	$V_{CM} = 1000\text{Vp-p}$ , $I_F = 0\text{mA}$ , $V_o(\text{Min}) = 4\text{V}$ , $T_a = 25^\circ\text{C}$	10000	—	—	V/us
Common mode transient immunity at low level output	$CM_L$		$V_{CM} = 1000\text{Vp-p}$ , $I_F = 12\text{mA}$ , $V_o(\text{Max}) = 0.4\text{V}$ , $T_a = 25^\circ\text{C}$	-10000	—	—	V/us

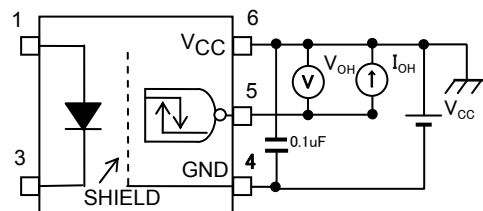
\*All typical values are at  $T_a = 25^\circ\text{C}$

Note 5 :  $C_L$  is approximately 15pF which includes probe and Jig/stray wiring capacitance.

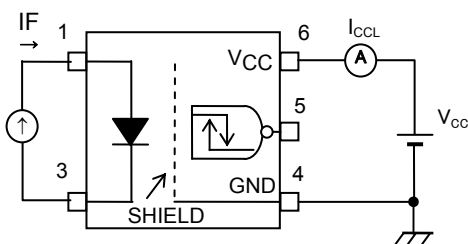
TEST CIRCUIT 1 :  $V_{OL}$



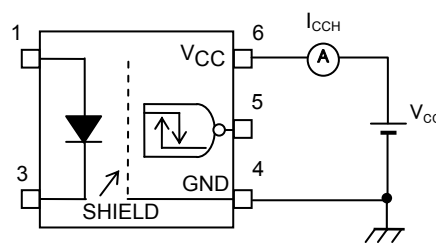
TEST CIRCUIT 2 :  $V_{OH}$



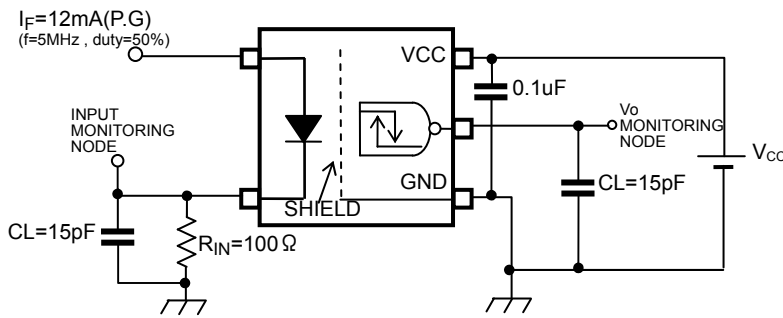
TEST CIRCUIT 3 :  $I_{CCL}$



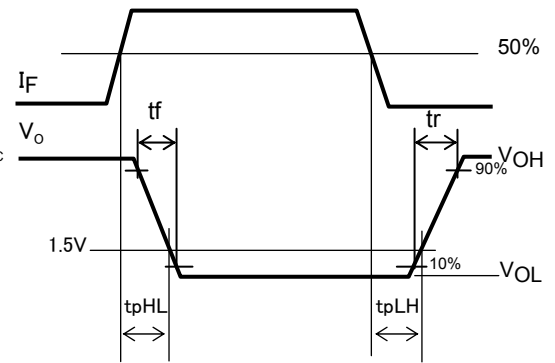
TEST CIRCUIT 4 :  $I_{CCH}$



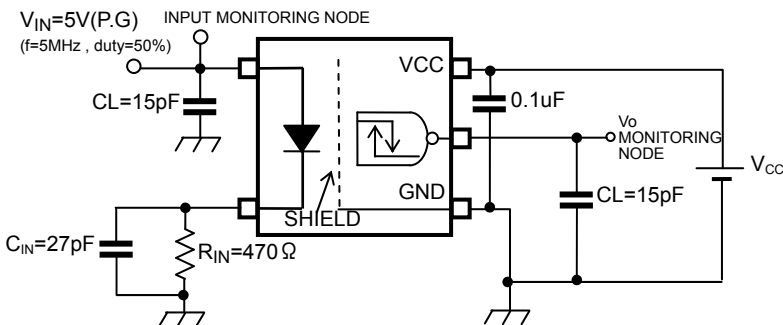
### TEST CIRCUIT 5 : tpHL , tpLH



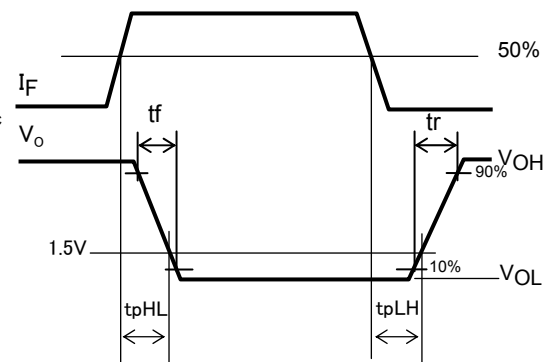
CL is capacitance of the probe and JIG.  
(P.G) : Pulse Generator



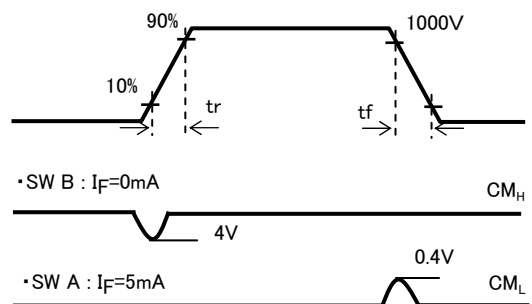
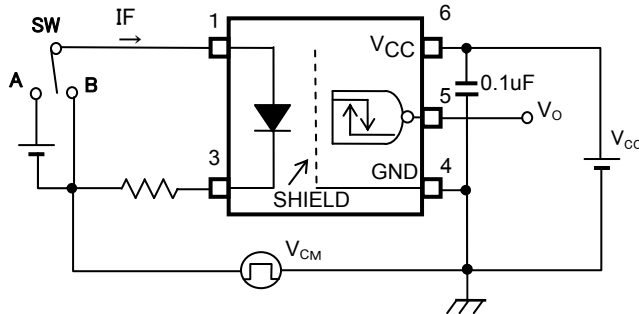
### TEST CIRCUIT 6 : tpHL , tpLH



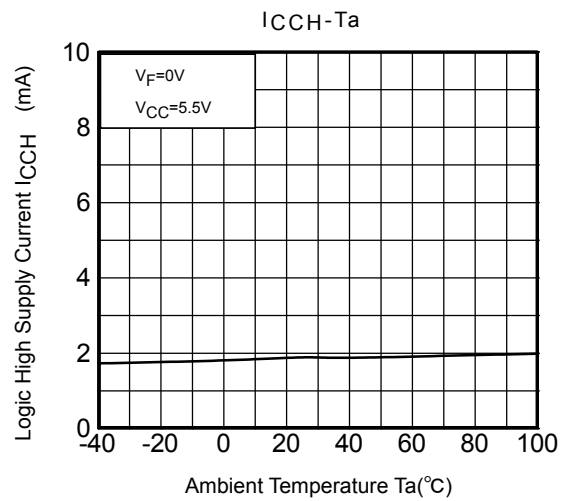
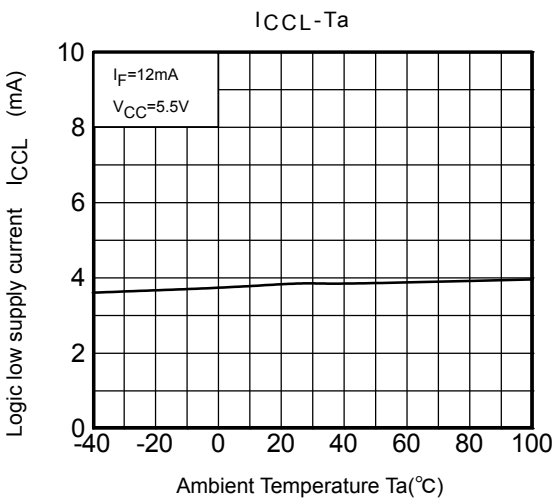
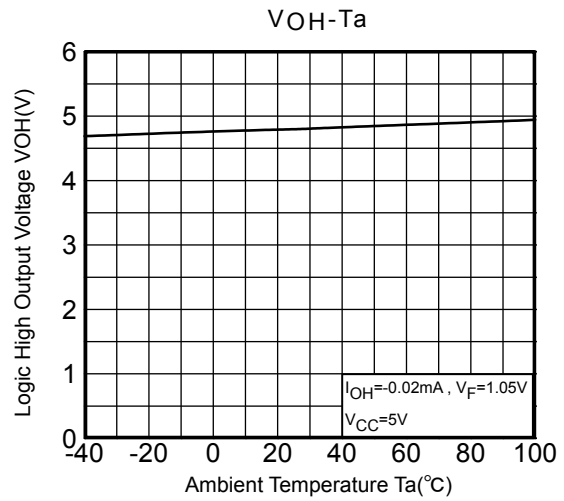
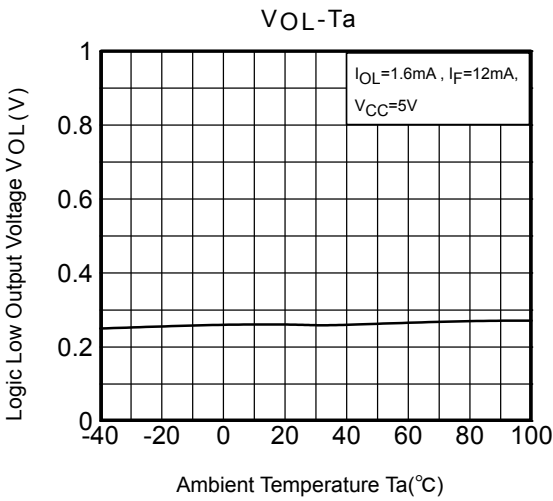
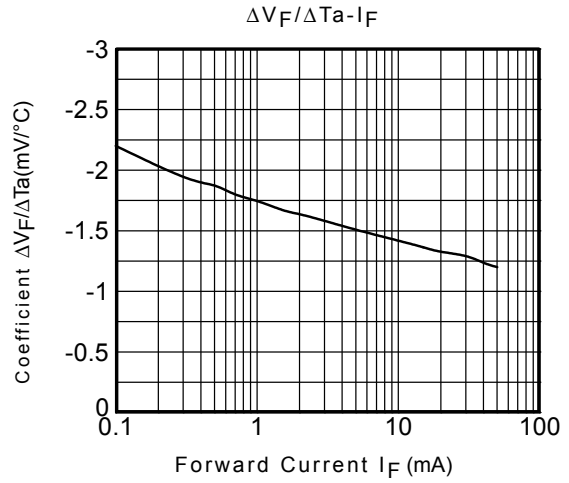
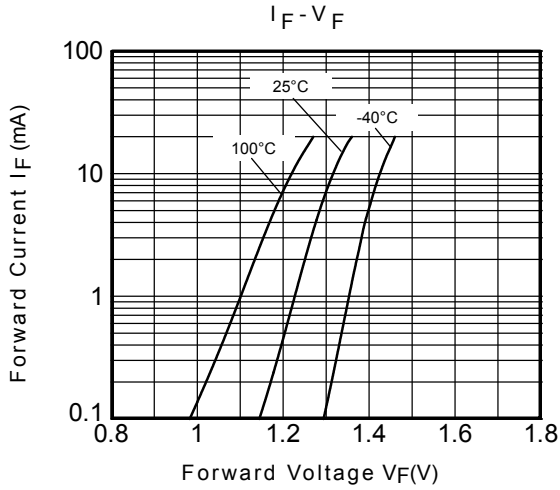
CL is capacitance of the probe and JIG.  
(P.G) : Pulse Generator



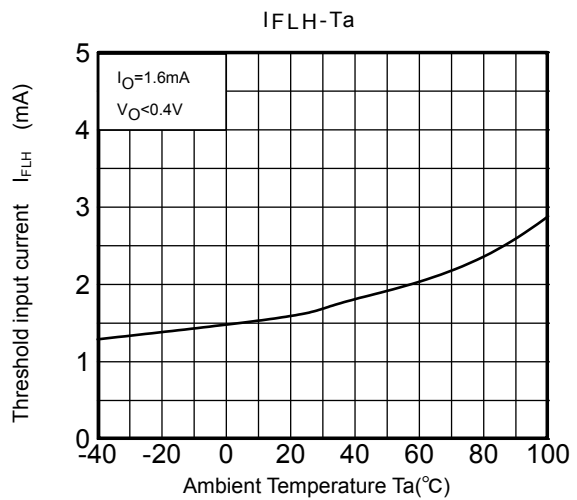
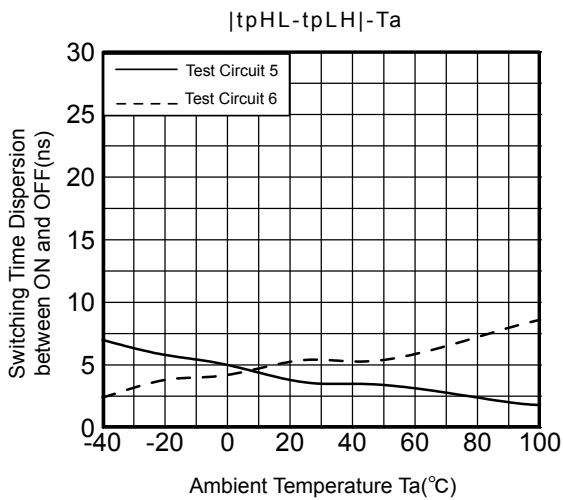
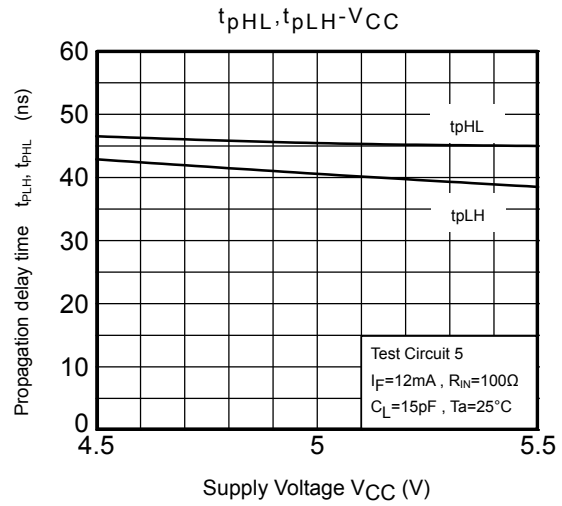
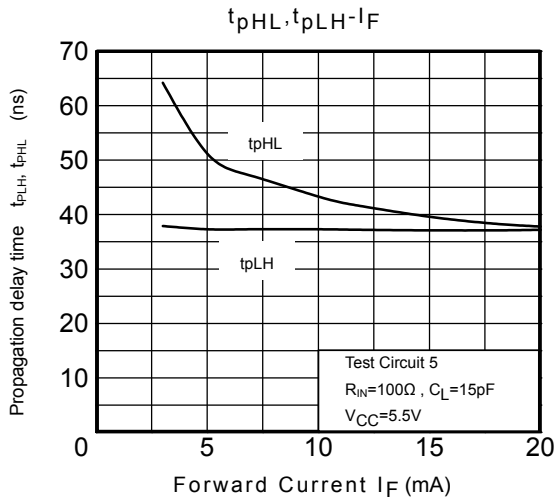
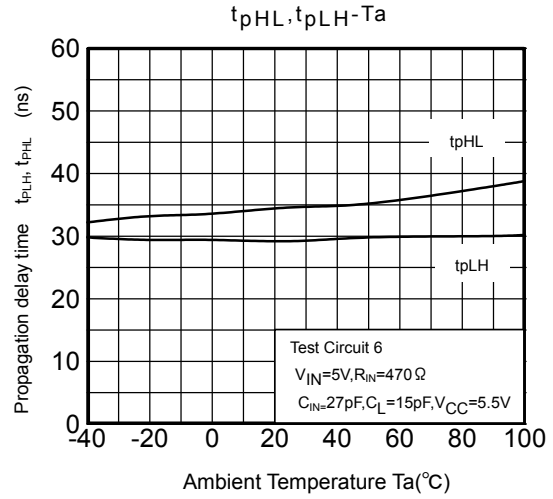
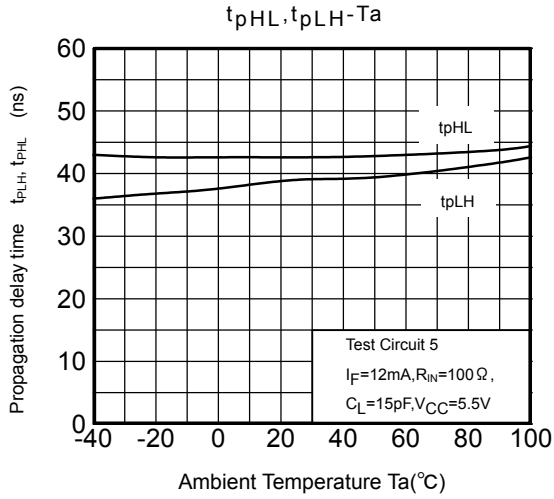
### TEST CIRCUIT 7 : Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r(\mu s)} \quad CM_L = \frac{800(V)}{t_f(\mu s)}$$



\*: The above graphs show typical characteristics.



\*: The above graphs show typical characteristics.

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20070701-EN

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