TLIN1021-Q1 Local Interconnect Network (LIN) Transceiver with Local Wake and Inhibit

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C T_A
  - HBM ESD classification level 3A
  - CDM ESD classification level C4A
- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2
- Conforms to SAEJ2602 recommended practice for LIN
- Supports 12 V applications
- LIN transmit data rate up to 20 kbps
- Wide operating ranges
  - Extended operation with supply from 4.5 V to 36 V DC
  - ±45 V LIN bus fault protection
- Sleep mode: ultra-low current consumption allows wake up events from:
  - LIN bus
  - Wake up input (external switch)
  - Local wake up through EN
- Power up and down glitch free operation
- Control of external voltage regulator using INH Pin
- Protection features
  - Undervoltage protection on V_{SUP}
  - TXD Dominant state time-out protection
  - Thermal shutdown
  - Unpowered node or ground disconnection fail-safe at system level
- Available in the SOIC (8) package and VSON (8) package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Infotainment and cluster
- Hybrid electric vehicles and power train systems
- Passive safety
- Appliances

3 Description

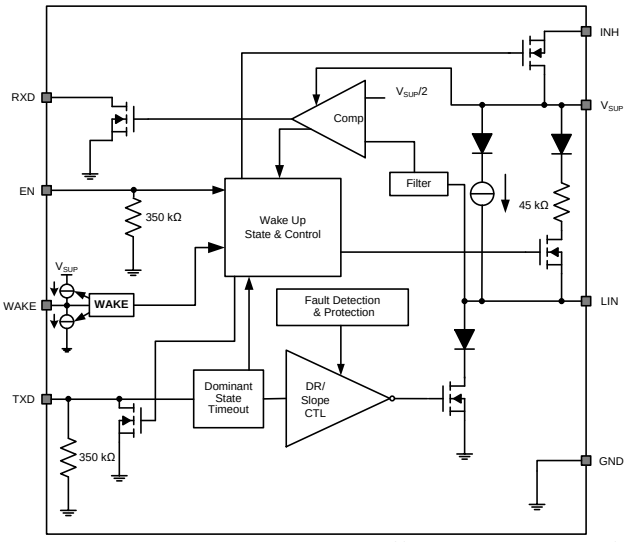
The TLIN1021-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.2A and ISO/DIS 17987-4.2 standards. LIN is a single-wire bidirectional bus typically used for in-vehicle networks using data rates up to 20 kbps. The receiver supports data rates up to 100 kbps for end-of-line programming. The TLIN1021-Q1 controls the state of the LIN bus via the TXD pin and reports the state of the bus on the open-drain RXD pin. The TLIN1021-Q1 is designed to support 12 V applications across a wide operating voltage and protect against DC faults with integrated protection. Ultra-low current consumption is possible by putting the device in sleep mode and can be put in normal mode via messages on the LIN bus, the WAKE pin, or the EN pin. The TLIN1021-Q1 allows for system-level reductions in battery current consumption by selectively enabling, via the INH output pin, the various power supplies that may be present on a node. The TLIN1021-Q1 has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLIN1021-Q1	SOIC (D) (8)	4.90 mm x 6.00 mm
	VSON (DRB) (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

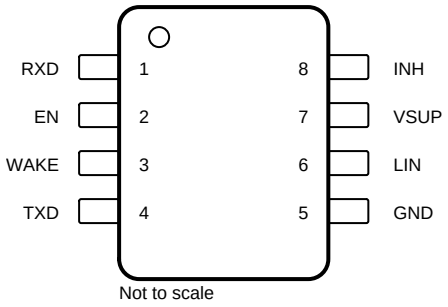
DATE	REVISION	NOTES
June, 2019	*	Advanced Information

5 Description (continued)

The integrated resistor, electrostatic discharge (ESD) protection, and fault protection allow designers to save board in their applications. The TLIN1021-Q1 has been designed for operation in the harsh automotive environment. The device prevents back-feed current through LIN to the supply input in case of a ground shift or supply voltage disconnection. Other features include undervoltage, overtemperature, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

6 Pin Configuration and Functions

D Package
8-Pin (SOIC)
Top View



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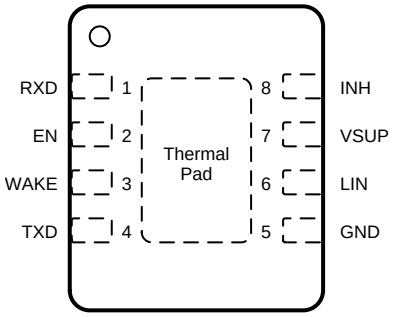
DRB Package
8-Pin (VSON)
Top View



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Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
RXD	1	D O	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	D I	Enable input - High put the device in normal operation mode and low put the device in sleep mode
WAKE	3	HV I	High Voltage Local wake up pin
TXD	4	D I/O	TXD input interface to control state of LIN output - Internal pulled to ground; active low output afer a local wake-up event
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	Supply	Device supply voltage (connected to battery in series with external reverse blocking diode
INH	8	HV O	High voltage output pin for node regulator enable
GND	Thermal Pad	GND	Ground and should be soldered

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7 Specifications

7.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987)	–0.3	45	V
V_{LIN}	LIN Bus input voltage (ISO/DIS 17987)	–45	45	V
V_{WAKE}	WAKE pin input voltage	–0.3	45	V
V_{INH}	INH pin output voltage	–0.3	45 and $V_O \le V_{SUP}$+0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
$I_{O(INH)}$	Inhibit output current		4	mA
$I_{O(WAKE)}$	WAKE output current due to ground shift ($V_{WAKE} \le V_{GND}$) – 0.3 V thus current out of the WAKE pin must be limited		3	mA
T_A	Ambient temperature range	–40	125	°C
T_J	Junction Temp	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD RATINGS

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002	Pins TXD, RXD, EN, INH(1)	±4000	V
			Pins LIN bus, V_{SUP}, WAKE(2)	±8000	
		Charged-device model (CDM), per AEC-Q100-002	All pins	±750	

(1) Tested in accordance to AEC-Q100-002
(2) Test method based upon AEC-Q100-002, LIN bus a stressed with respect to GND.

7.3 ESD RATINGS, IEC SPECIFICATION

			VALUE	UNIT
IEC 61000-4-2 according to IBEE EMC test spec(1)	LIN , WAKE, Vsup terminal to GND(2)		±8000	kV
ISO7637-2 & IEC 62215-3 Transients according to IBEE LIN EMC test spec(3)	LIN , Vsup, WAKE	Pulse 1	-100	V
ISO7637-2 & IEC 62215-3 Transients according to IBEE LIN EMC test spec(3)	LIN , Vsup, WAKE	Pulse 2	75	V
ISO7637-2 & IEC 62215-3 Transients according to IBEE LIN EMC test spec(3)	LIN , Vsup, WAKE	Pulse 3a	-150	V
ISO7637-2 & IEC 62215-3 Transients according to IBEE LIN EMC test spec(3)	LIN , Vsup, WAKE	Pulse 3b	150	V
Powered ESD Performance SAEJ2962-1	SAEJ2962-1(4)	Contact	±8000	V
		Air Discharge	±15000	V
ISO7637 Slow Transients Pulse	SAEJ2962-1 test spec(5) and IBEE Zwickau		TBD	V

(1) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system level configurations may lead to different results
(2) Testing performed at 3rd party IBEE Zwickau test house, test report available upon request.
(3) ISO7637 is a system level transient test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system level configurations may lead to different results.
(4) SAEJ2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.
(5) ISO7637 is a system level transient test. Results given here are specific to the SAEJ2962-1 Test specification conditions. Different system level configurations may lead to different results

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7.4 Thermal Information

THERMAL METRIC(1)		TLIN1021-Q1		UNIT
		D (SOIC)	DRB (VSON)	
		PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.8	71.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	68.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	41.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.1	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	41.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	31.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 RECOMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	4.5		36	V
V_{LIN}	LIN Bus input voltage	0		36	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

7.6 POWER SUPPLY CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range See Figure 8 and Figure 9	4.5		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10)	Normal and standby modes: ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50 % duty cycle and 18V swing. See Figure 8 and Figure 9	4.5		36	V
		Sleep Mode	4.5		36	V
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp Up		4.15	4.45	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp Down	3.6	4		V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.2		V
I_{SUP}	Supply current dominant only	Normal mode: EN = VCC, bus dominant: total bus load where $R_{LIN} \geq 500\ \Omega$ and $C_{LIN} \leq 10$ nF, INH = WAKE = V_{SUP}		1.2	6.5	mA
		Standby mode: EN = 0 V, bus dominant: total bus load where $R_{LIN} \geq 500\ \Omega$ and $C_{LIN} \leq 10$ nF, INH = WAKE = V_{SUP}		1	1.7	mA
I_{SUP}	Supply current recessive only	Normal mode: EN = high, bus recessive: LIN = INH = WAKE = V_{SUP}		300	650	µA
		Standby mode: EN = low, LIN = recessive, INH = WAKE = V_{SUP}		15	30	µA
I_{SUP}	Supply current sleep mode	4.5 V < $V_{SUP} \leq$ 14 V, LIN = WAKE = V_{SUP}, EN = low, TXD and RXD floating		6	12	µA
		14 V < $V_{SUP} \leq$ 36 V, LIN = WAKE = V_{SUP}, EN = low, TXD and RXD floating			20	µA

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7.7 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD OUTPUT TERMINAL (OPEN DRAIN)						
V_{OL}	Output low voltage	Based upon external pull-up to V_{CC} (1)			0.2 * V_{CC}	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5	0	5	µA
TXD INPUT TERMINAL						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{LKG}	Low level input leakage current	TXD = low	–5	0	5	µA
I_{TXD_Wake}	Local wake up source recognition TXD (2)	Standby mode after a local wake up event, V_{LIN} = V_{SUP}, WAKE = 0 V or V_{SUP}, TXD = high	1.3		8	mA
R_{TXD}	Interal pull-down resistor value		125	350	800	kΩ
EN INPUT TERMINAL						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low level input current	EN = low	–5	0	5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIN TERMINAL (REFERENCED TO V_{SUP})						
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 7 V to 36 V	0.85			V_{SUP}
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 4.5 V ≤ V_{SUP} ≤ 7 V	3			V
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 7 V to 36 V			0.2	V_{SUP}
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 4.5 V ≤ V_{SUP} ≤ 7 V			1.2	V
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open LIN = 4.5 V to 45 V	–0.3		42	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 18 V, R_{MEAS} = 440 Ω, V_{SUP} = 18 V, V_{BUSdom} < 4.518 V Figure 13	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	LIN = 0 V, V_{SUP} = 12 V Driver off/recessive Figure 14	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN ≥ V_{SUP}, 4.5 V ≤ V_{SUP} ≤ 36 V Driver off; Figure 15			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN = V_{SUP}, Driver off; Figure 15	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 18 V, 0 V ≤ V_{LIN} ≤ 18 V; Figure 16	–1		1	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 18 V, V_{SUP} = GND; Figure 17			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up) Figure 10, Figure 11			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	Lin recessive Figure 10, Figure 11	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2 Figure 10, Figure 11	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)	V_{HYS} = (V_{IL} - V_{IH}) Figure 10, Figure 11			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path	By design and characterization	0.4	0.7	1.0	V
R_{SLAVE}	Pull-up resistor to V_{SUP}	Normal and Standby modes	20	30	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 14 V, LIN = GND	–20		–2	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin				45	pF
INH OUTPUT TERMINAL (HIGH VOLTAGE OPEN DRAIN OUTPUT)						

(1) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(2) Open drain drive

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = - 0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current	INH = 0 V, Sleep Mode	–0.5		0.5	µA
WAKE INPUT TERMINAL						
V_{IH}	High-level input voltage	Selective Wake-up or Standby Mode, WAKE pin enabled	V_{SUP} – 2			V
V_{IL}	Low-level input voltage	Selective Wake-up or Standby Mode, WAKE pin enabled			V_{SUP} – 3	V
I_{IH}	High-level input leakage current	WAKE = V_{SUP} - 1 V	–25	–15		µA
I_{IL}	Ligh-level input leakage current	WAKE = 1 V		15	25	µA
t_{WAKE}	WAKE hold time	Wake up time from a wake edge on WAKE; Standby or Sleep mode	5		50	µs
DUTY CYCLE CHARACTERISTICS						
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(3)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)	0.396			
$D1_{12V}$	Duty Cycle 1	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.5 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)(4)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)	0.417			
$D3_{12V}$	Duty Cycle 3	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 18, Figure 19)			0.59	

(3) Duty cycle LIN driver bus load conditions (C_{LINBUS}, R_{LINBUS}): Load1 = 1 nF; 1 kΩ / Load2 = 6.8 nF; 660 Ω / Load3 = 10 nF; 500 Ω.
(4) Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TLIN1029 meets these lower data rate requirements while it is also capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAE J2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAE J2602 specification.

7.8 AC SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 20, Figure 21 and Figure 25)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (Figure 20, Figure 21 and Figure 25)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 24, Figure 27 and Figure 28	25	100	150	µs

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AC SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 28	8	17	50	µs
t_{DST}	Dominant state time out		20	34	80	ms
t_{MODE_CHANGE}	Mode change delay time(1)	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin: See Figure 22	2		15	µs
t_{NOMINT}	Normal mode initialization time(1)	Time for normal mode to initialize and data on RXD pin to be valid See Figure 22			30	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

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7.9 Typical Characteristics

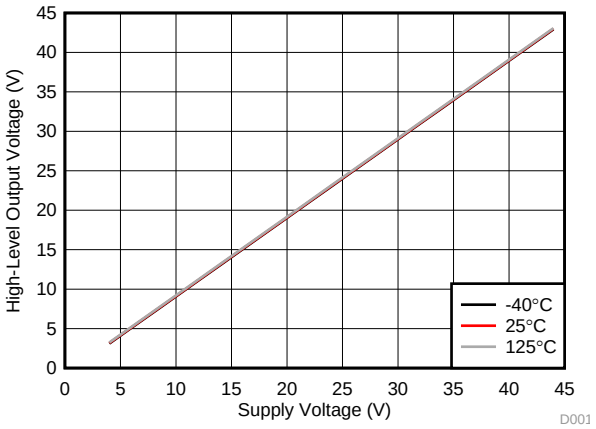


Figure 1. V_{OH} vs V_{SUP} and Temperature

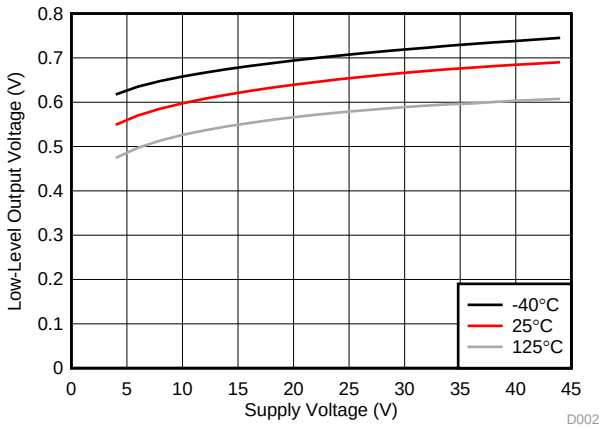


Figure 2. V_{OL} vs V_{SUP} and Temperature

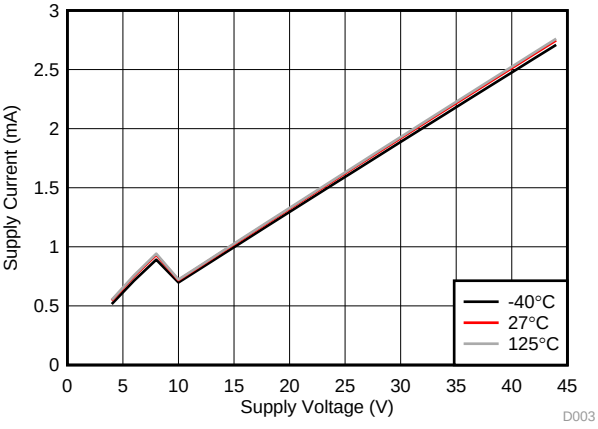


Figure 3. Dominant I_{SUP} vs V_{SUP} and Temperature

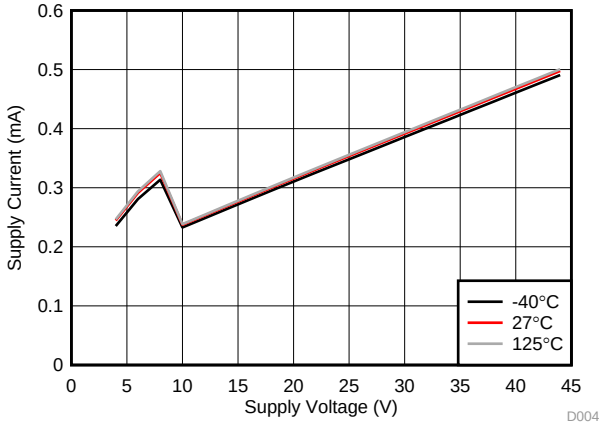


Figure 4. Recessive I_{SUP} vs V_{SUP} and Temperature

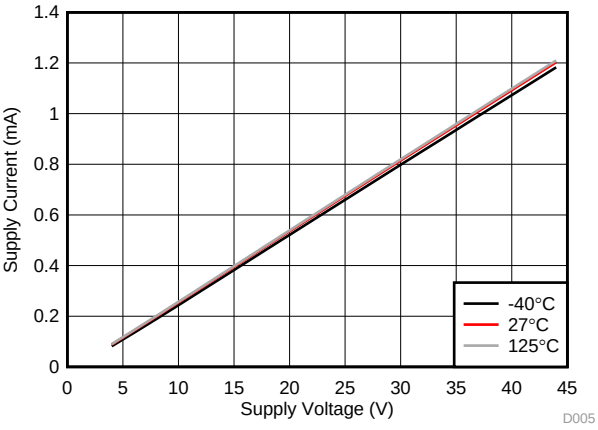


Figure 5. Standby Dominant I_{SUP} vs V_{SUP} and Temperature

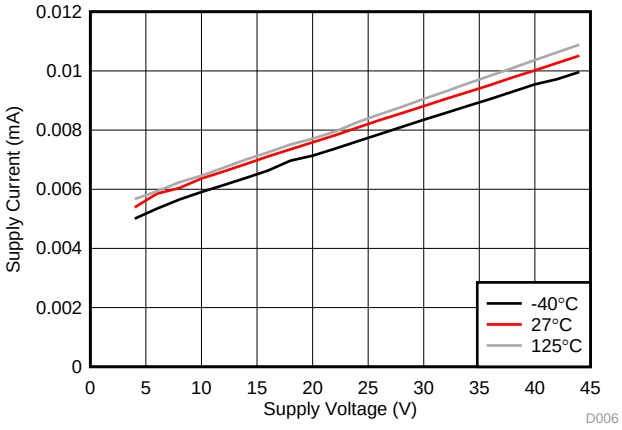


Figure 6. Standby Recessive I_{SUP} vs V_{SUP} and Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

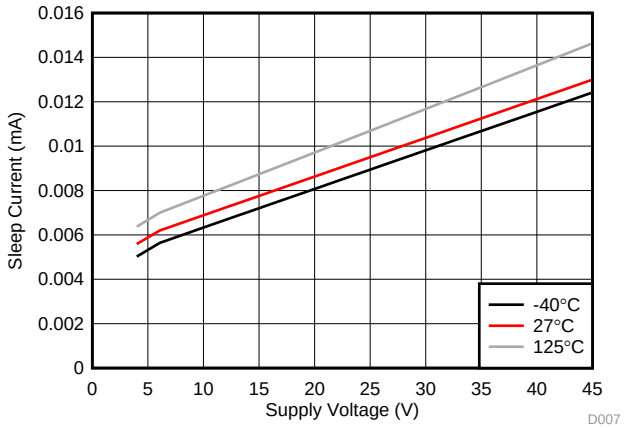


Figure 7. Sleep Current vs V_{SUP} and Temperature

8 Parameter Measurement Information

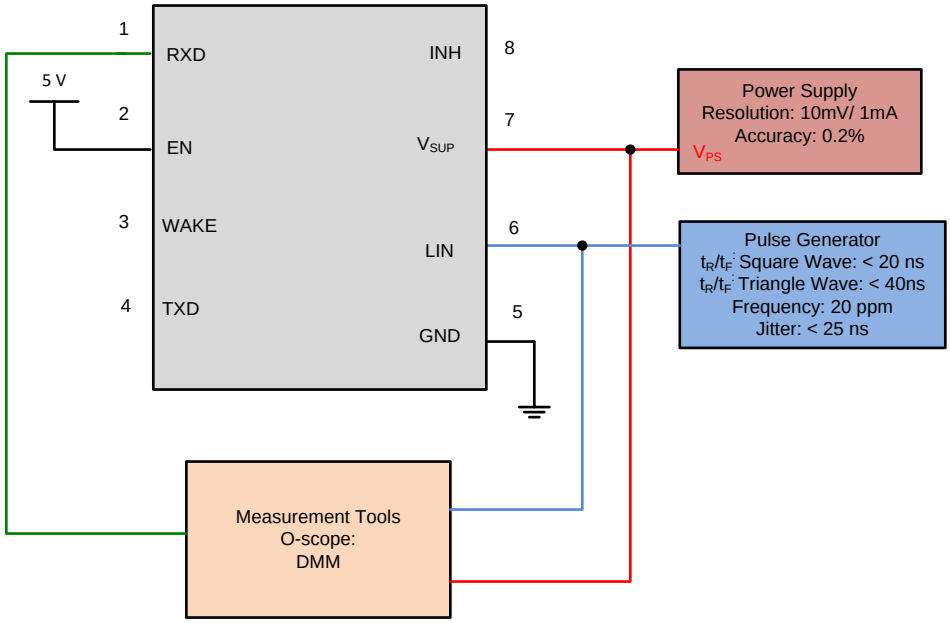


Figure 8. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

ADVANCE INFORMATION

Parameter Measurement Information (continued)

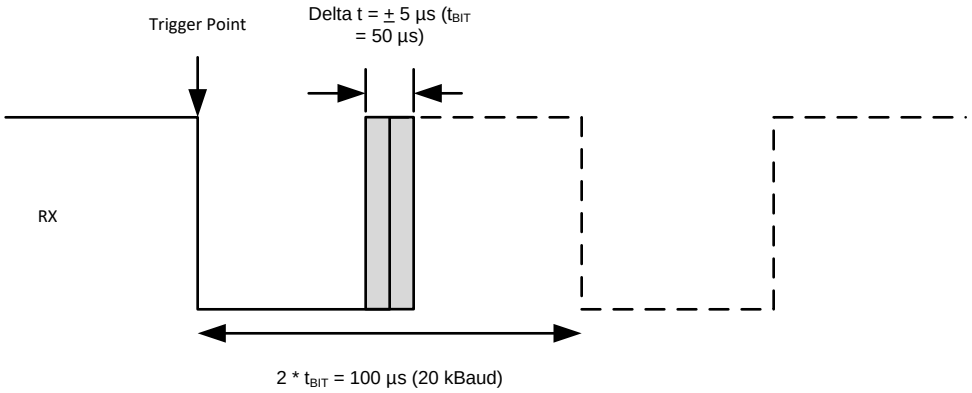


Figure 9. RX Response: Operating Voltage Range

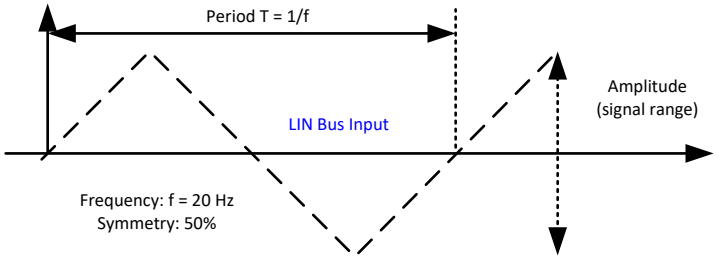


Figure 10. LIN Bus Input Signal

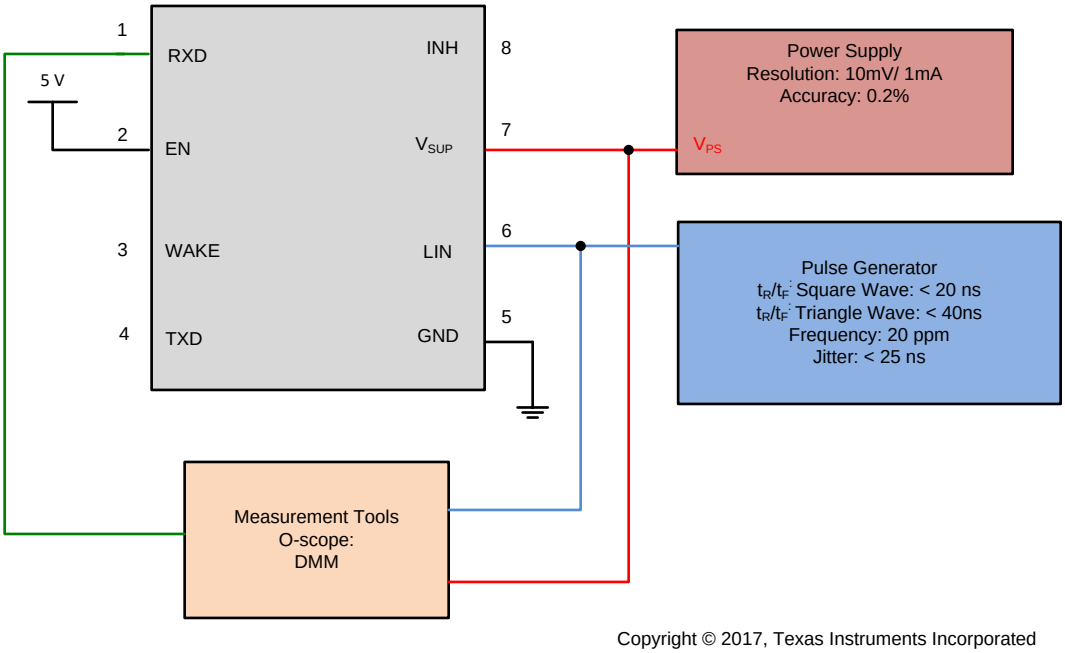


Figure 11. LIN Receiver Test with RX access Param 17, 18, 19, 20

ADVANCE INFORMATION

Parameter Measurement Information (continued)

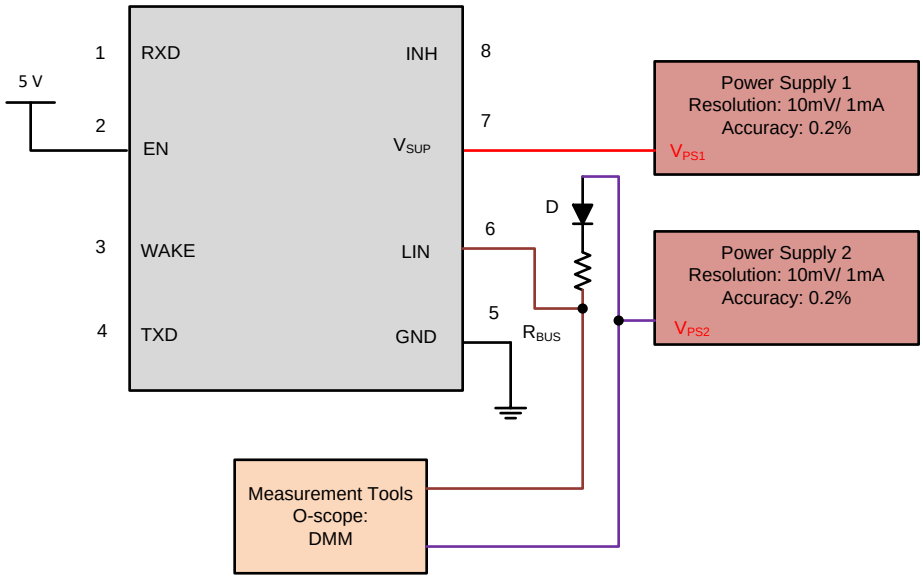


Figure 12. $V_{SUP\_NON\_OP}$ Param 11

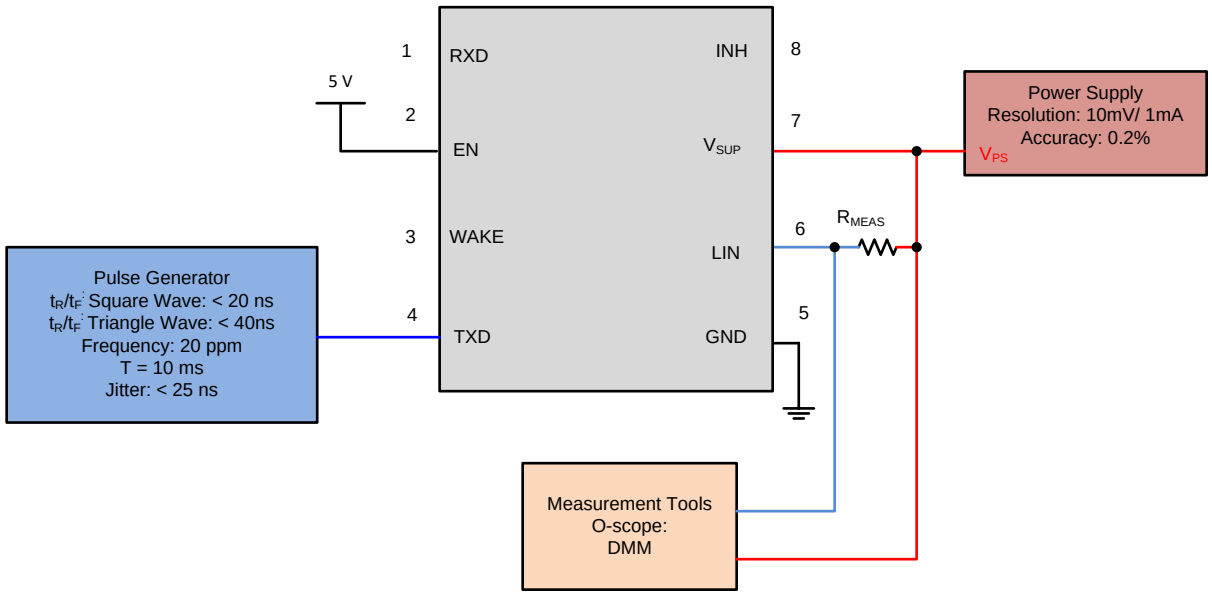


Figure 13. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on) Param 12

Parameter Measurement Information (continued)

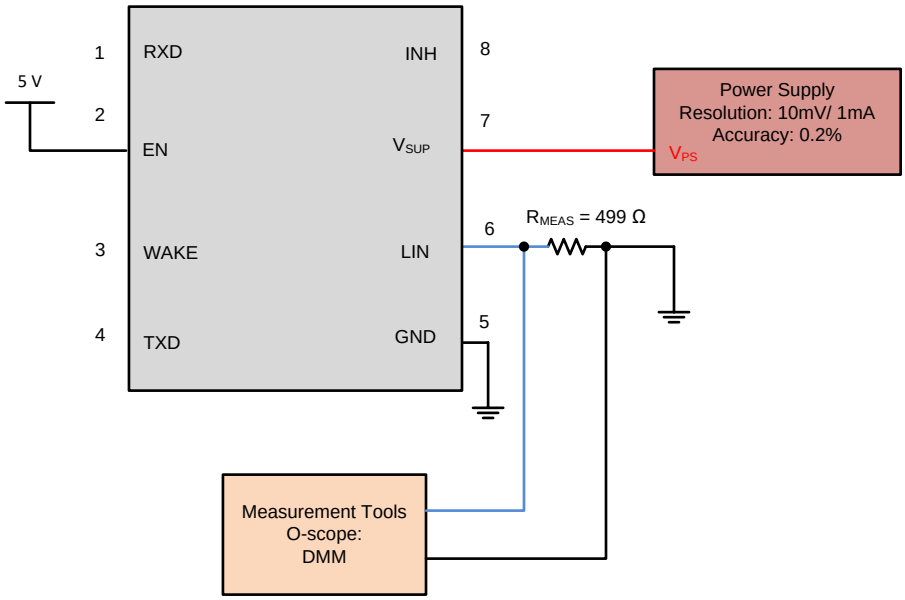


Figure 14. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13

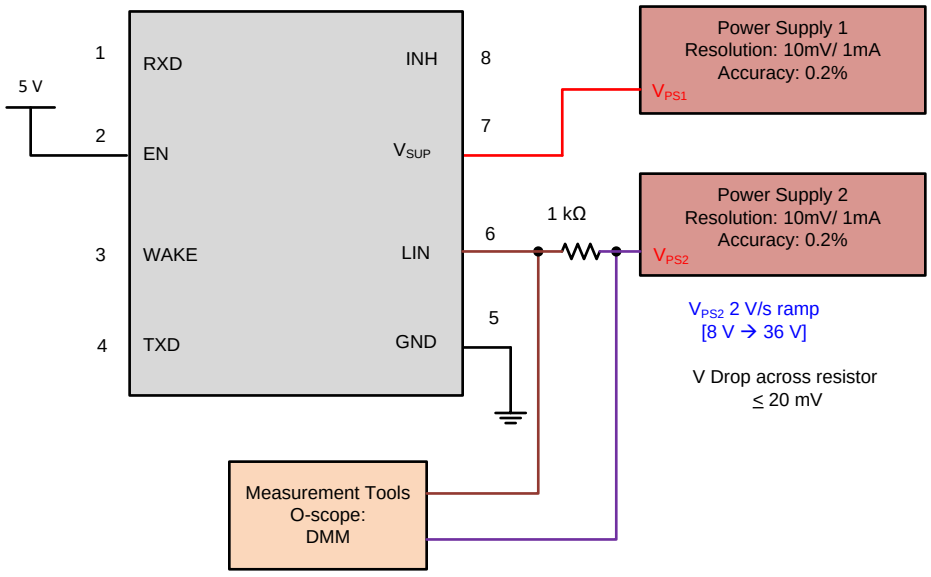


Figure 15. Test Circuit for $I_{BUS\_PAS\_rec}$ Param 14

ADVANCE INFORMATION

Parameter Measurement Information (continued)

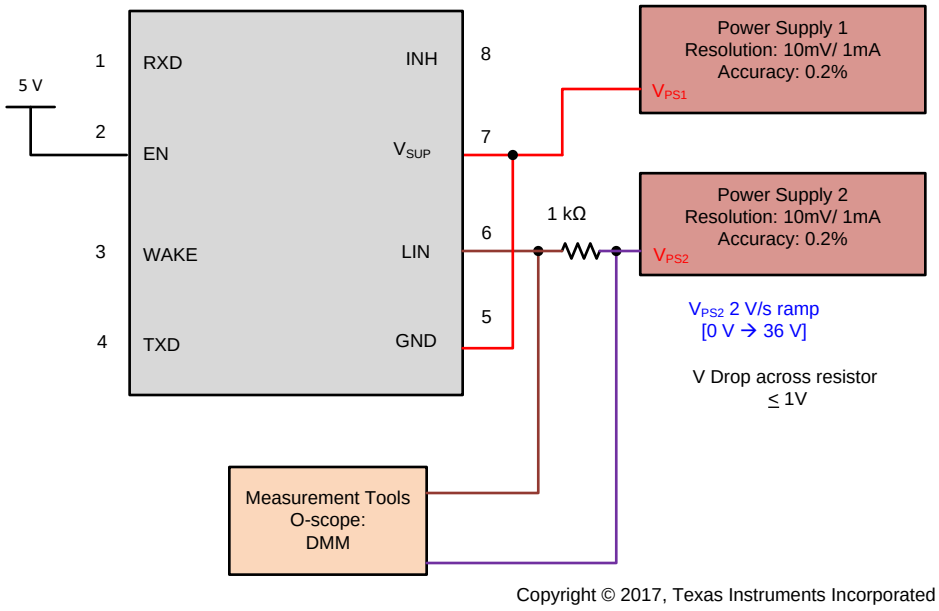


Figure 16. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND

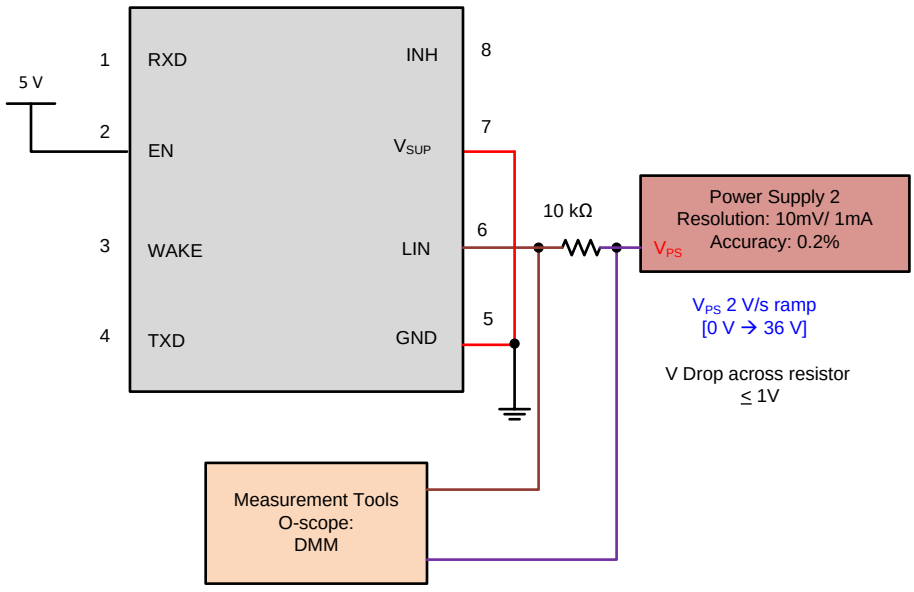


Figure 17. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery

ADVANCE INFORMATION

Parameter Measurement Information (continued)

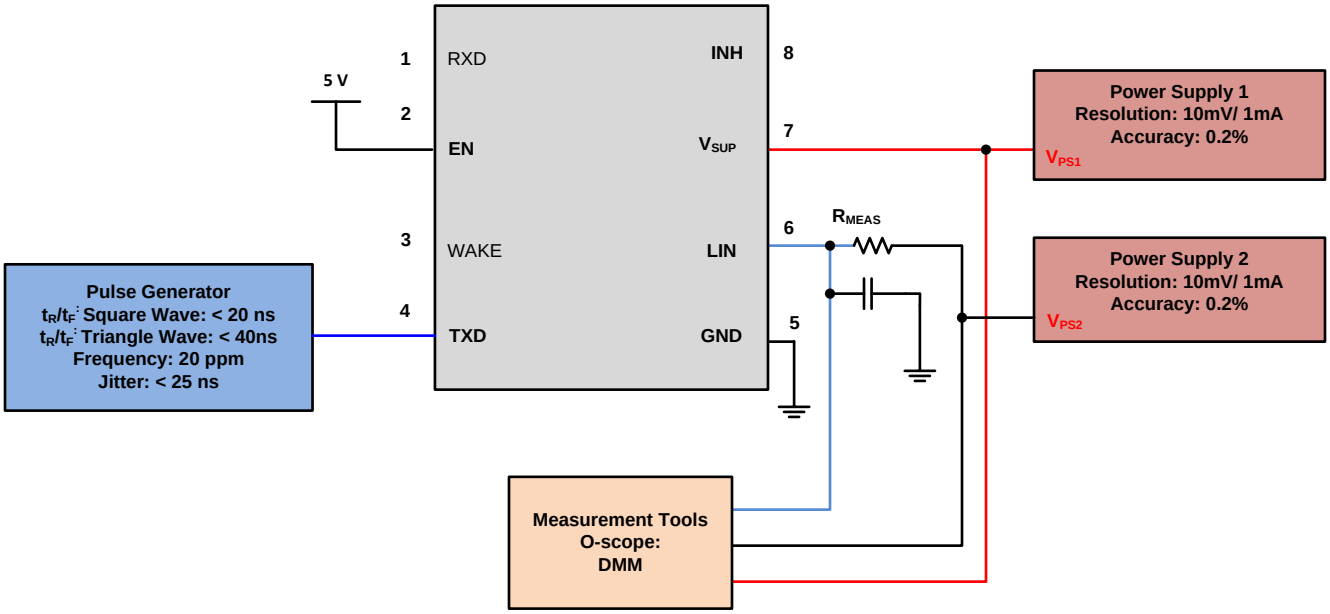


Figure 18. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

ADVANCE INFORMATION

Parameter Measurement Information (continued)

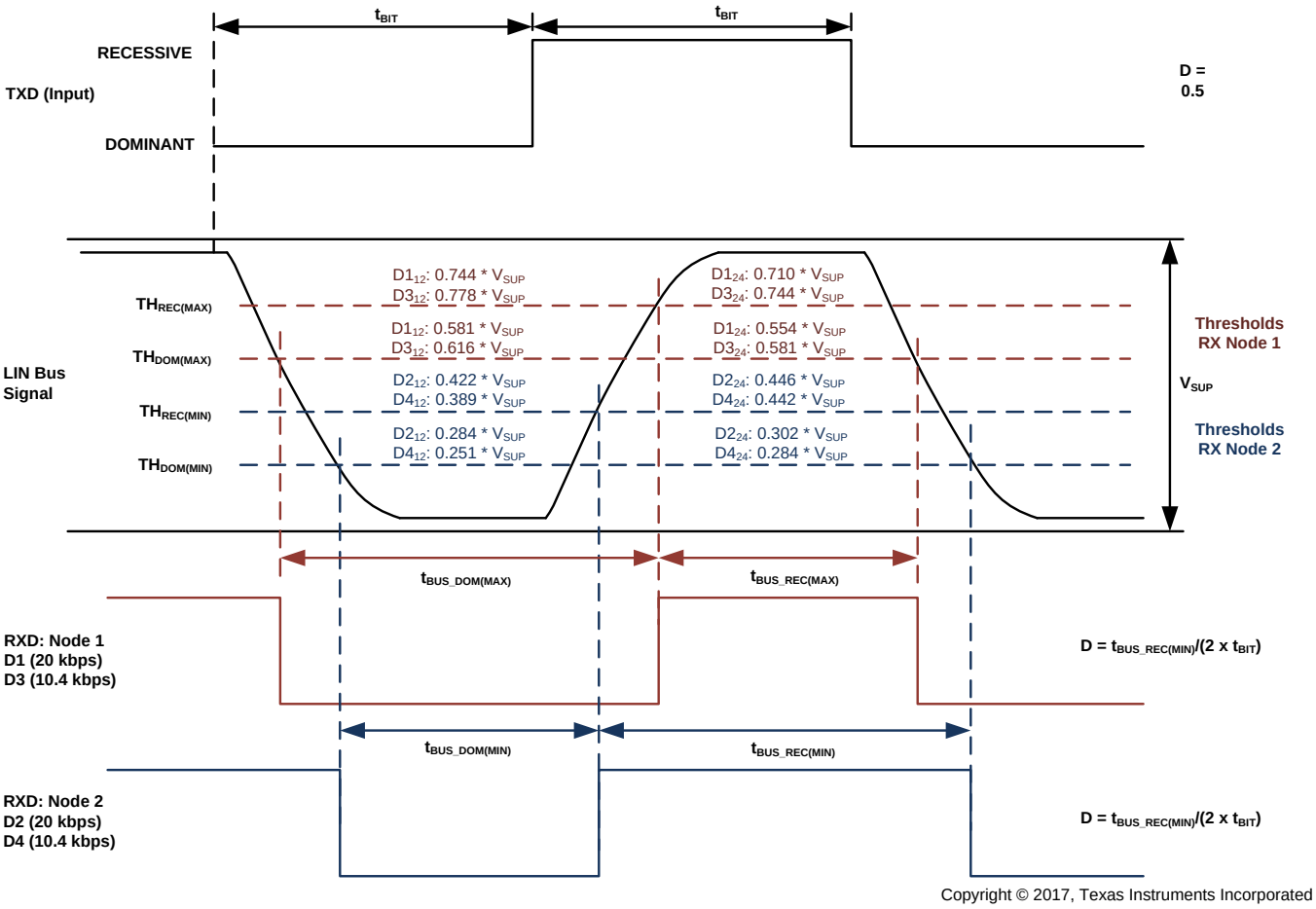


Figure 19. Definition of Bus Timing Parameters

ADVANCE INFORMATION

Parameter Measurement Information (continued)

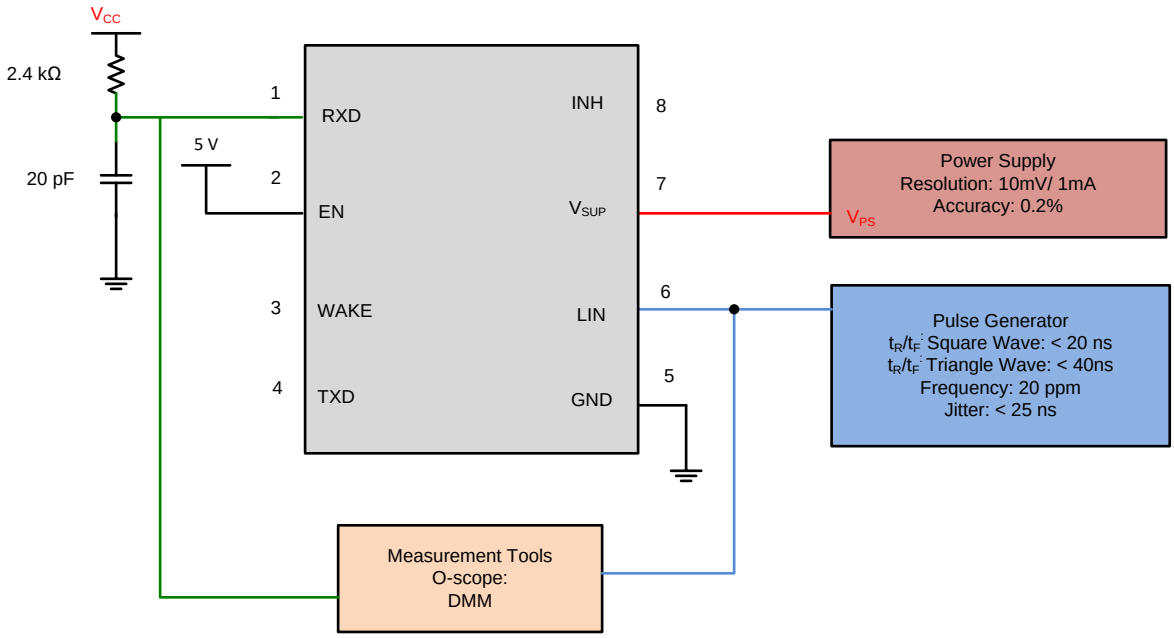


Figure 20. Propagation Delay Test Circuit; Param 31, 32

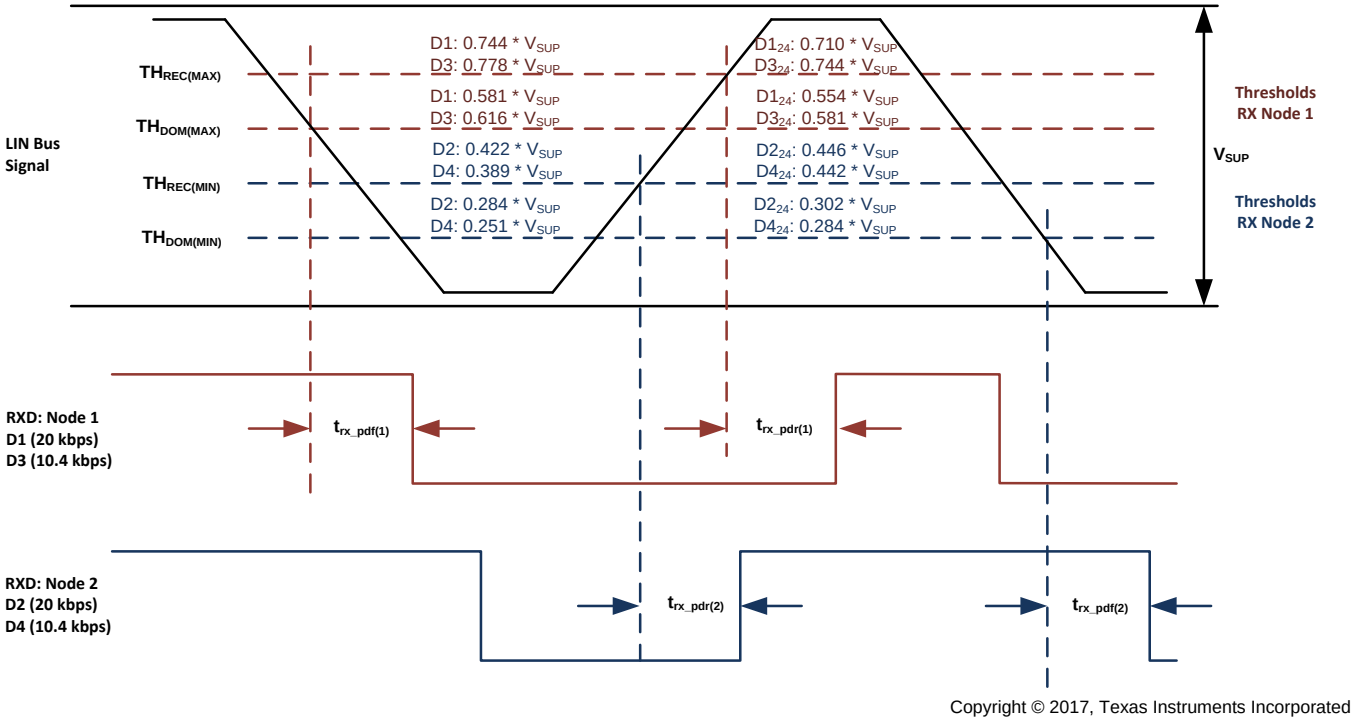


Figure 21. Propagation Delay

Parameter Measurement Information (continued)

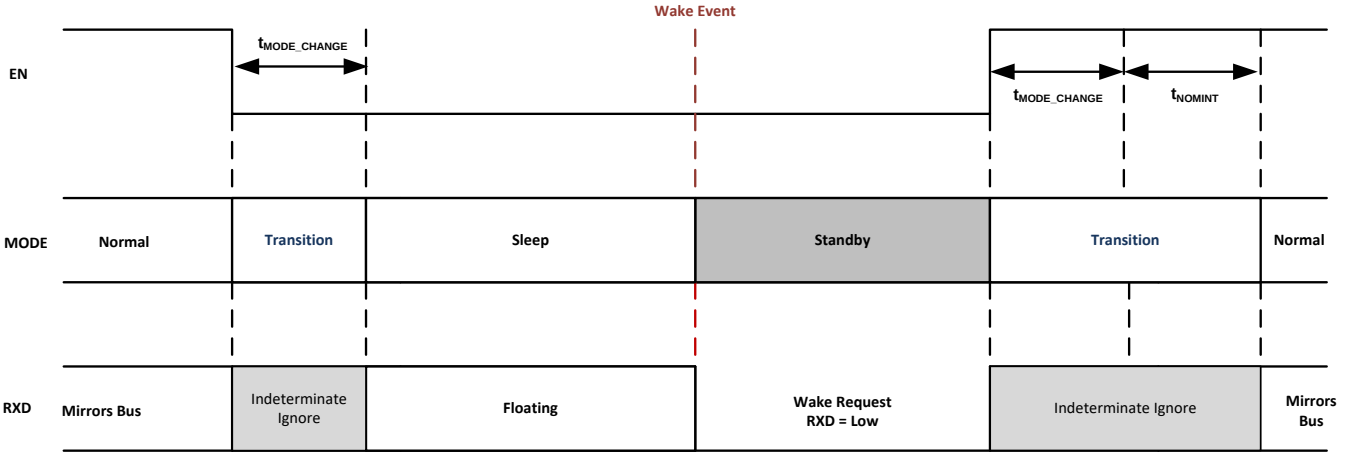


Figure 22. Mode Transitions

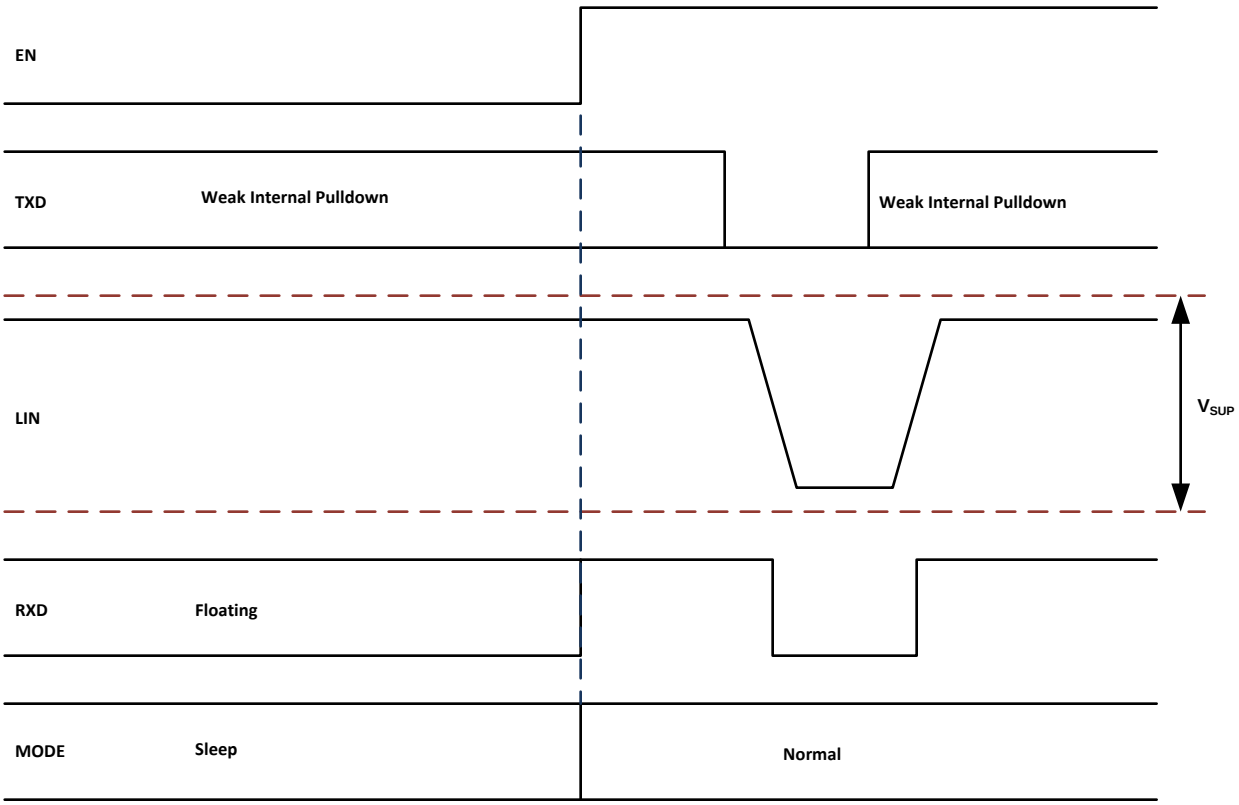


Figure 23. Wakeup Through EN

ADVANCE INFORMATION

Parameter Measurement Information (continued)

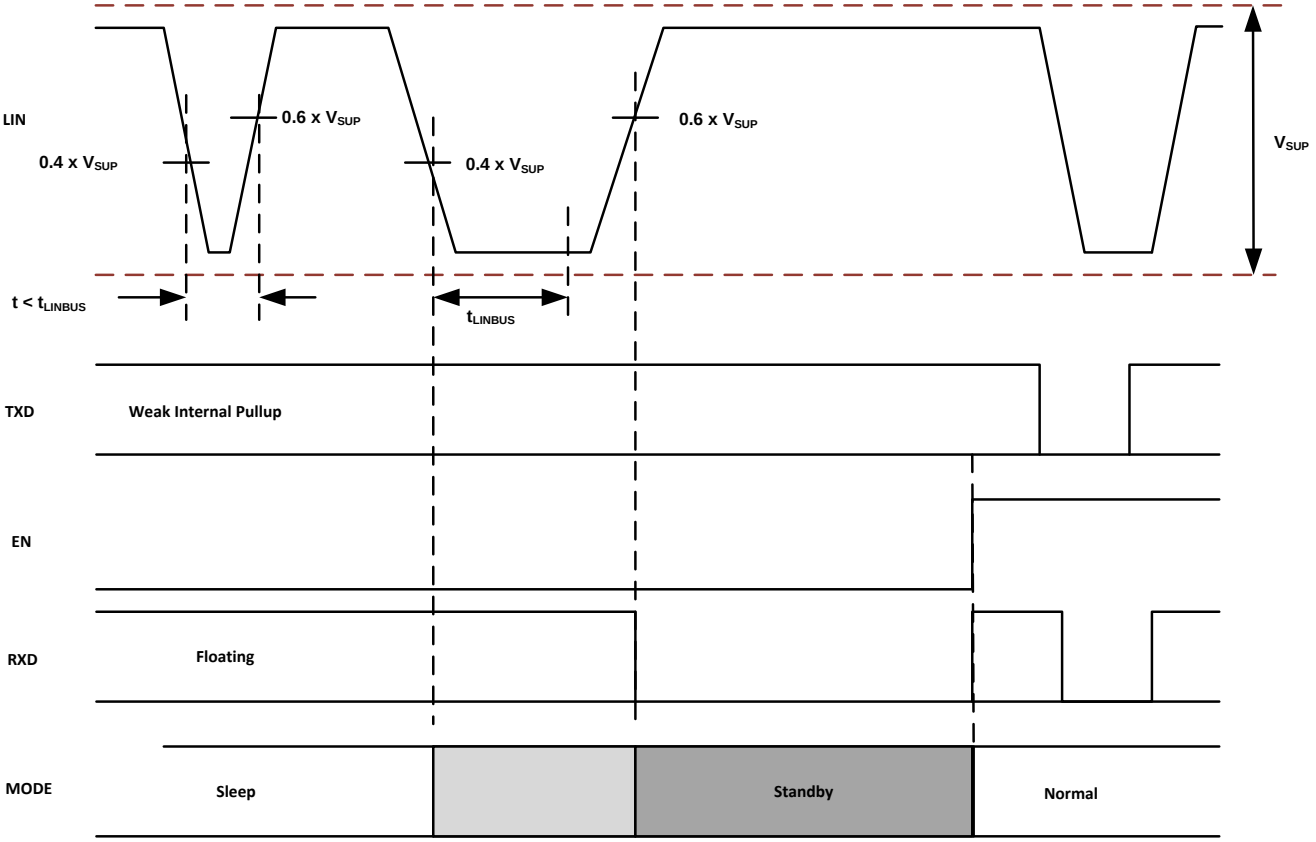


Figure 24. Wakeup through LIN

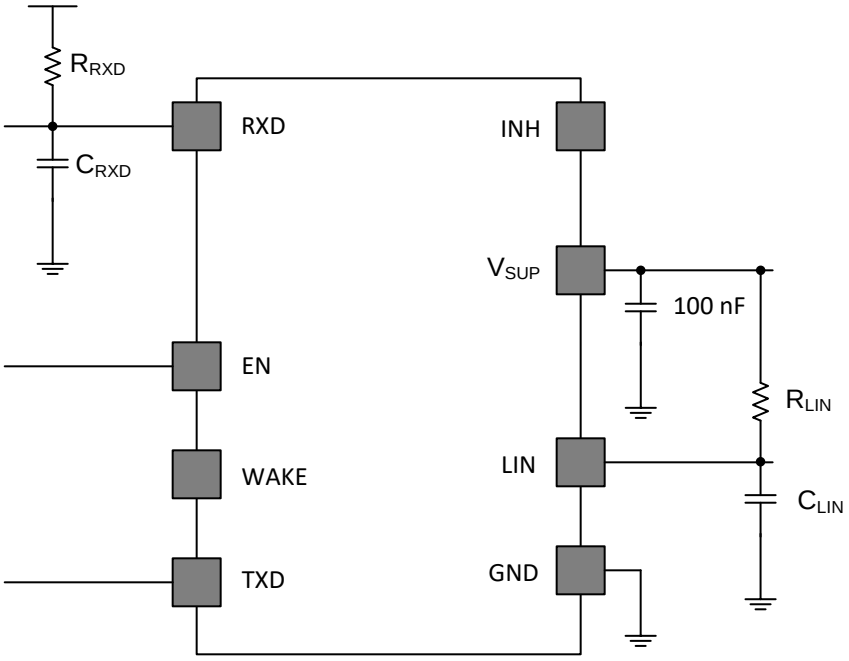


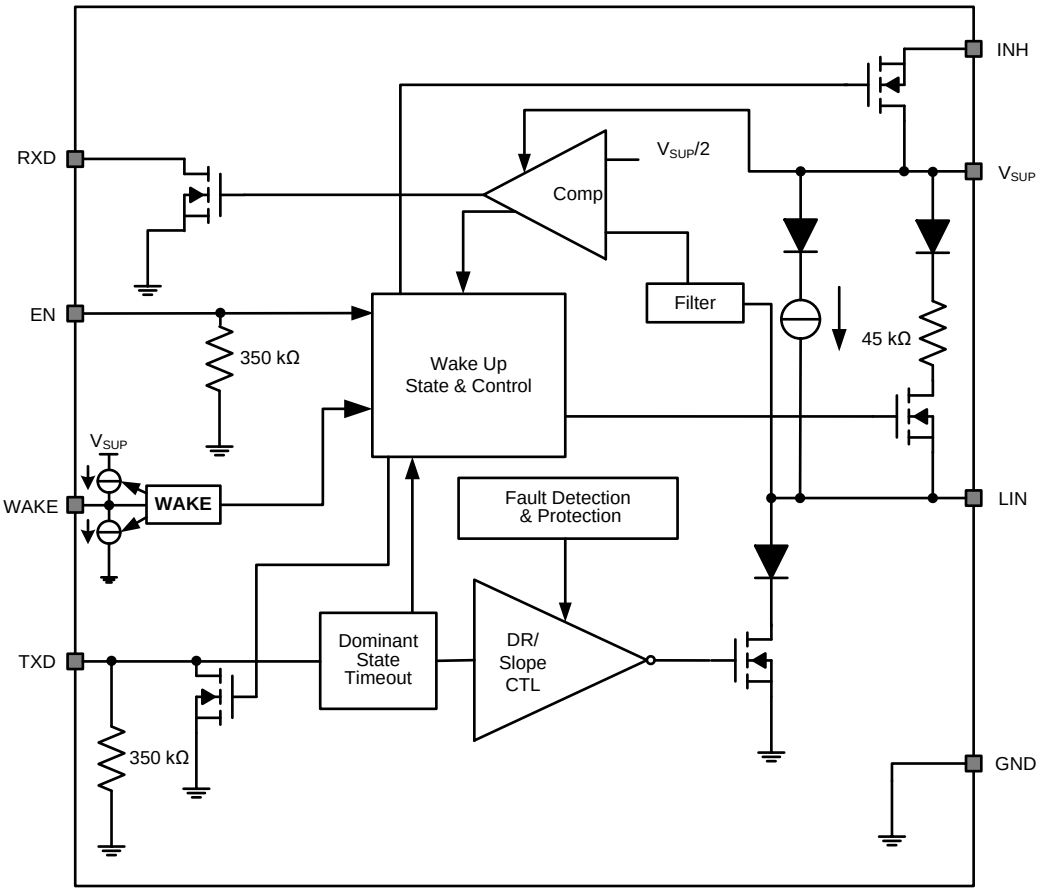
Figure 25. Test Circuit for AC Characteristics

9 Detailed Description

9.1 Overview

The TLIN1021-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, complaint to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 standards, with integrated wake-up and protection features. The LIN bus is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates from 2.4 kbps to 20 kbps. The TLIN1021-Q1 LIN receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN1021-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification. The TLIN1021-Q1 provides many protection features such as immunity to ESD and high bus standoff voltage. The device also provides two methods to wake up: EN pin and from the LIN bus.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 42 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

ADVANCE INFORMATION

Feature Description (continued)

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a master node application.

9.3.1.2 LIN Receiver Characteristics

The receiver's characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1021-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for master node applications as per the LIN specification.

Figure 26 shows a Master Node configuration and how the voltage levels are defined

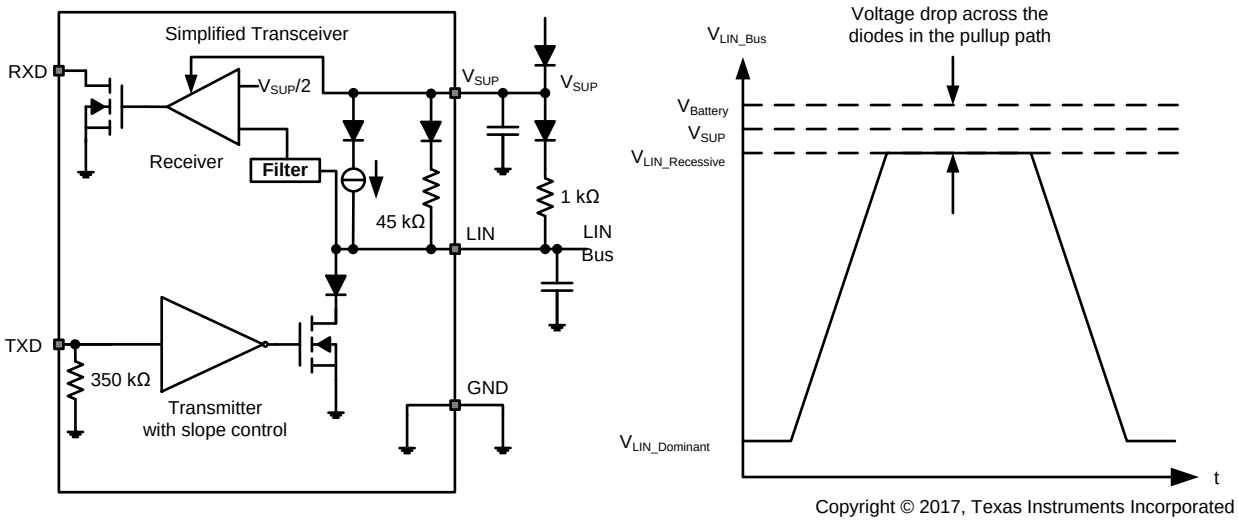


Figure 26. Master Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCU's LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See Figure 26. The TXD input structure is compatible with microprocessors with 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer. When a change of state on the WAKE pin initiating a local wake-up event this pin is pulled hard to ground. The hard pull to ground is released upon the rising edge on the EN pin.

Feature Description (continued)

9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microprocessors. If the microprocessor's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microprocessor I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from the LIN bus.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (Figure 26). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

9.3.7 WAKE (Local Wake Up Input)

WAKE pin is used for a high voltage device local wake up (LWU). This function is explained further in Local Wake Up (LWU) via WAKE Input Terminal section. The pin is bi-directional edge trigger, meaning it will recognize a LWU on either a rising or falling edge of WAKE pin transition.

9.3.8 INH (Inhibit Output)

The INH pin is a high voltage output pin provideing voltage from the V_{SUP} minus a diode drop to enable an external high voltage regulator. These regulators are usually used to support the microprocessor. The INH function is on in all modes but sleep mode. In sleep mode the INH pin is turned off, going into a high Z state. This allows the node to be placed into the lowest power state while in sleep mode.

NOTE

This terminal should be considered a "high voltage logic" terminal, not a power output thus should be used to drive the EN terminal of the system's power management device and not used as a switch for power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside of the system module.

9.3.9 Protection Features

The TLIN1021-Q1 has several protection features that will now be described.

ADVANCE INFORMATION

Feature Description (continued)

9.3.10 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

NOTE

If EN pin is high at power up the device will enter normal mode. With the internal TXD connected low it will start the DTO timer. To avoid a DTO timeout put a recessive signal onto the TXD pin or placing the device into sleep mode by connecting EN pin low.

9.3.11 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN1021-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 27 and Figure 28 show the behavior of this protection.

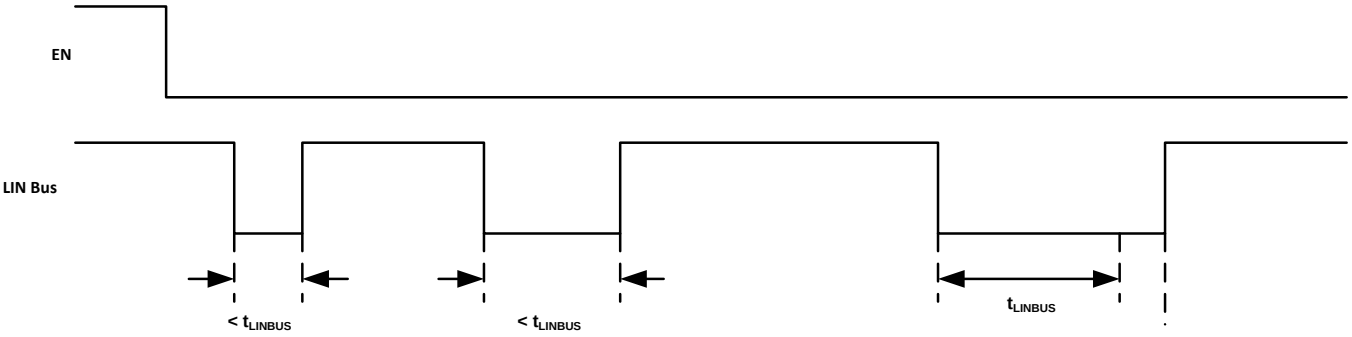


Figure 27. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

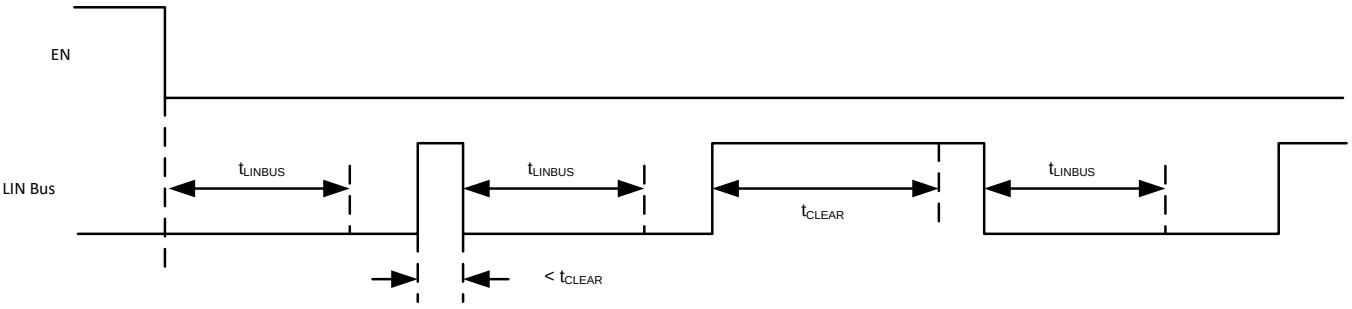


Figure 28. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

ADVANCE INFORMATION

Feature Description (continued)

9.3.12 Thermal Shutdown

The LIN transmitter is protected by limiting the current; however if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

9.3.13 Under Voltage on V_{SUP}

The TLIN1021-Q1 contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.14 Unpowered Device and LIN Bus

In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN1021-Q1 has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN1021-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. Figure 29 graphically shows the relationship while Table 1 shows the state of pins.

Table 1. Operating Modes

MODE	EN	TXD	RXD	INH	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Weak pull-down	Floating	Floating	Weak Current pull-up	Off	No wake up request
Standby	Low	weak pull-down if LIN bus wake-up; Strong pull-down if a local wake-up event (WAKE pin)	Low	High	45 kΩ (typical)	Off	Wake up event detected, waiting on MCU to set EN
Normal	High	High: recessive state Low: dominant state	LIN Bus Data	High	45 kΩ (typical)	On	LIN transmission up to 20 kbps

ADVANCE INFORMATION

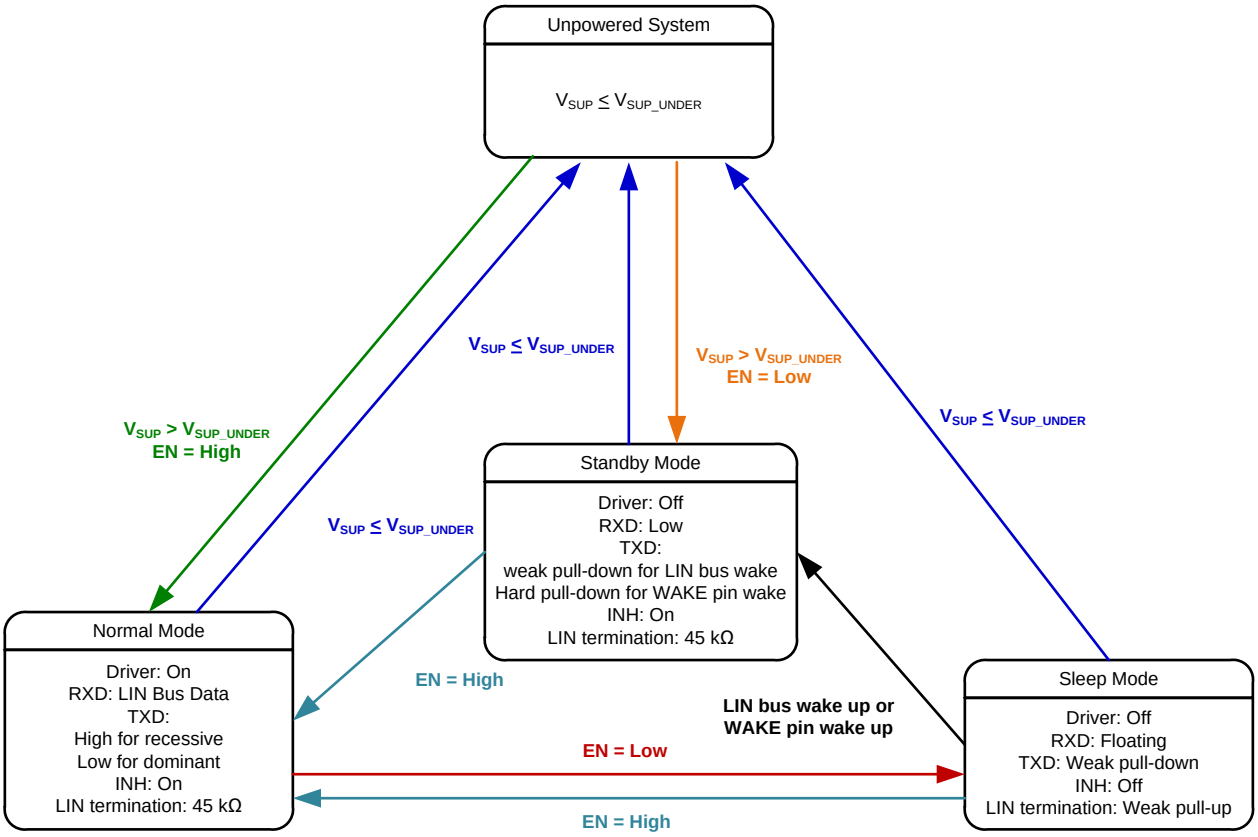


Figure 29. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high at power up the device will power up in normal mode and if low will power up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN1021-Q1 is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1021-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN1021-Q1 can still wake up from LIN bus through a wake up signal, local wake event from the WAKE pin or if EN is set high for > t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake up events. The wake up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input, WAKE pin and LIN wake up receiver are active.

9.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus slave termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *Standby Mode Application Note* for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake Up Events

There are three ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Wake up through EN being set high for longer than t_{MODE_CHANGE}.
- Change in voltage level on the WAKE pin ≥ t_{WAKE}

9.4.4.1 Wake Up Request (RXD)

When the TLIN1021-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin is releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a high voltage input terminal which can be used for local wake up (LWU) request via a voltage transition. The terminal triggers a LWU event on either a low to high or high to low transition as it has bidirectional input thresholds. This terminal may be used with a switch to V_{SUP} or ground. If the terminal is not used it should be pulled to ground or V_{SUP} to avoid unwanted parasitic wake up events. When a LWU event takes place the TXD pin is pulled hard to GND letting the microprocessor know that the wake event was due to the WAKE pin and not a wake through the LIN bus.

The LWU circuitry is active in sleep mode and standby mode. If a valid LWU event occurs the device will transition to standby mode. The LWU circuitry is not active in normal mode. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(MIN)}$. A constant high level on WAKE will have an internal pull-up to V_{SUP} and a constant low level on WAKE will have an internal pull-down to GND.

ADVANCE INFORMATION

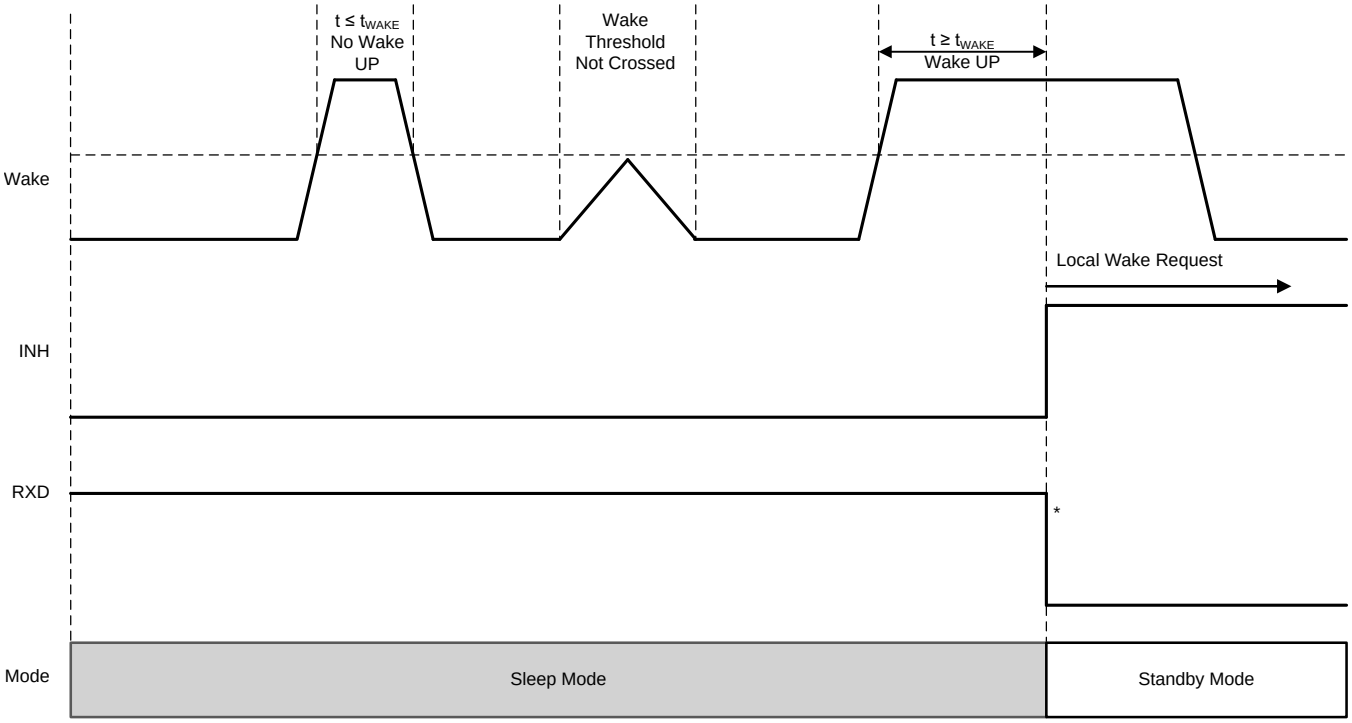


Figure 30. Local Wake Up – Rising Edge

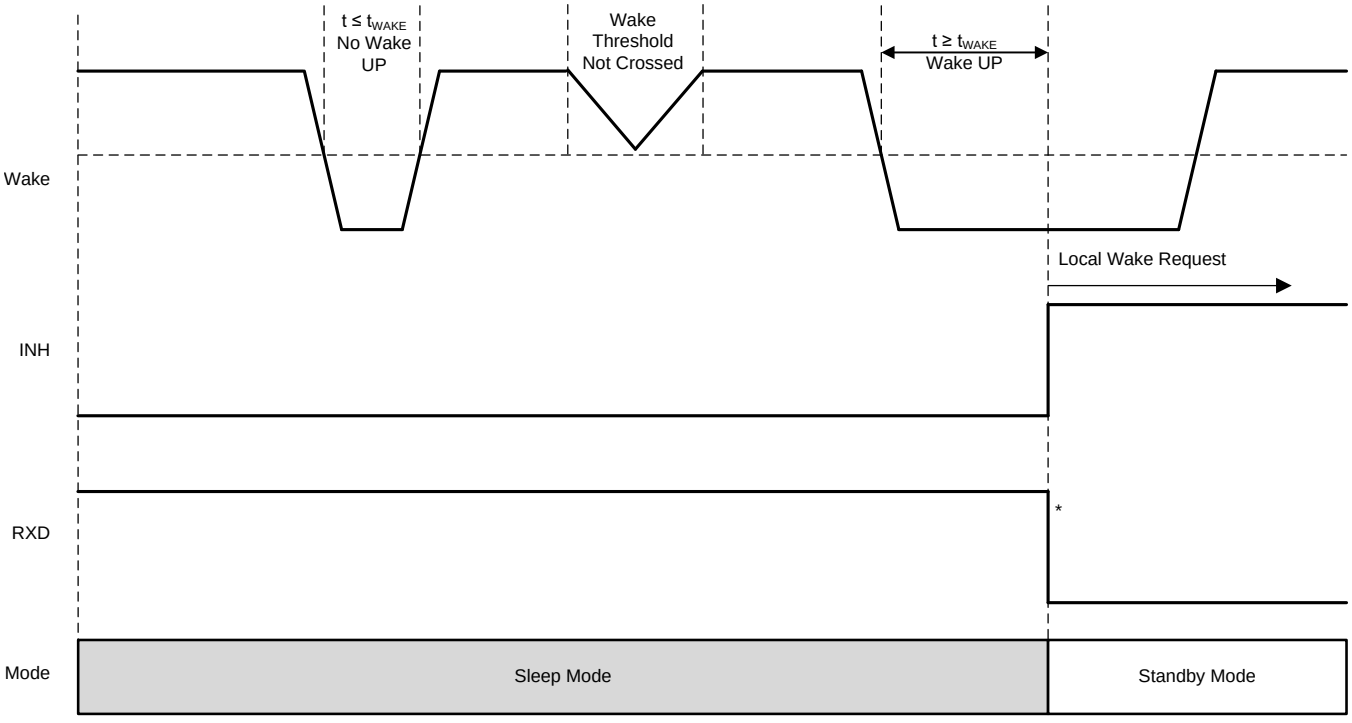


Figure 31. Local Wake Up – Falling Edge

9.4.4.3 Mode Transitions

When the TLIN1021-Q1 is transitioning from normal to sleep or standby modes the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{MODE_CHANGE} plus t_{NOMINT}.

ADVANCE INFORMATION

10 Application and Implementation

NOTE

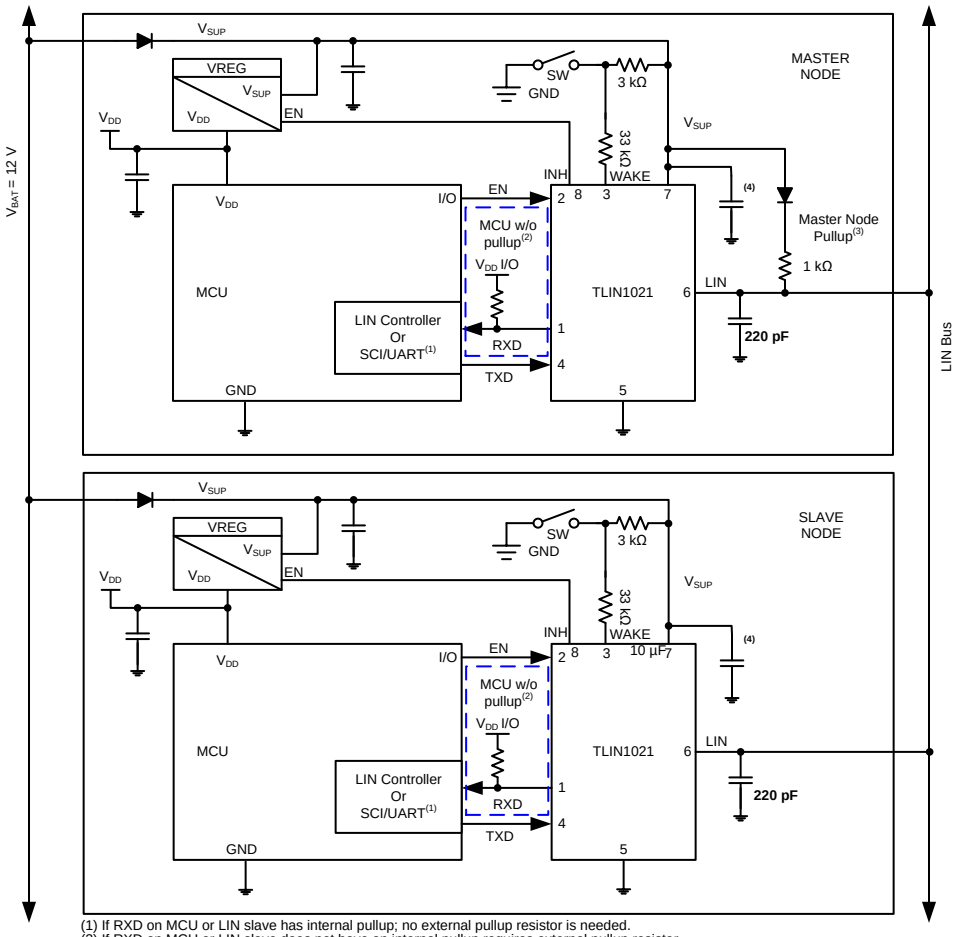
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1021-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

10.2 Typical Application

The device integrates a 45 kΩ pull-up resistor and series diode for slave applications. For master applications an external 1 kΩ pull-up resistor with series blocking diode can be used. Figure 32 shows the device being used in both master and slave applications.



(1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.
(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

Figure 32. Typical LIN Bus

Typical Application (continued)

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN1021-Q1 to be used with 3.3- V and 5-V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor's I/O supply voltage is required. The select external pull-up resistor value should be between 1 kΩ to 10 kΩ. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible. The system should include 1 µF and ≥ 10 µF decoupling capacitors on V_{SUP} as per each application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN1021-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in Figure 22

10.2.2.2 Standby Mode Application Note

If the TLIN1021-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low and would signal to the software that the TLIN1021-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.2.2.1 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.3 Application Curves

Figure 33 and Figure 34 show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant stated under lightly loaded conditions.

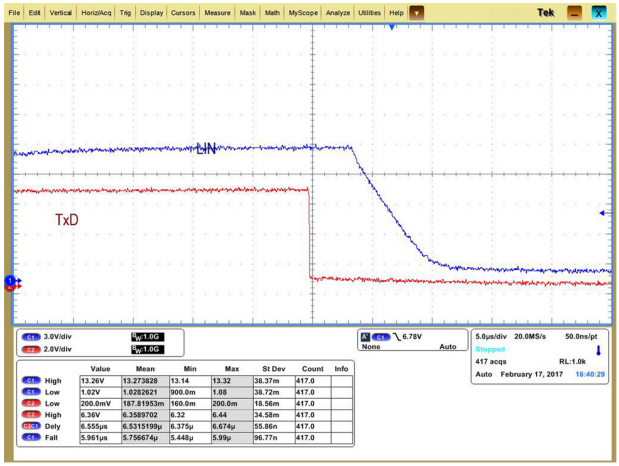


Figure 33. Recessive to Dominant Propagation

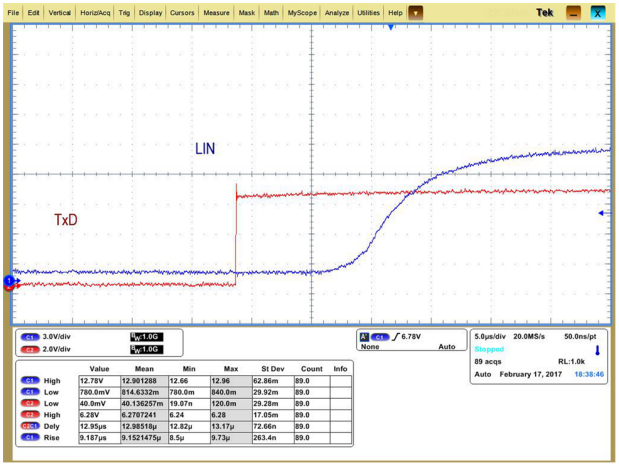


Figure 34. Dominant to Recessive Propagation

11 Power Supply Recommendations

The TLIN1021-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 36 V. A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

ADVANCE INFORMATION

12 Layout

In order for your PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1(RXD):** The pin is an open drain output and requires and external pull-up resistor in the range of 1 kΩ and 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (WAKE):** SW1 is oriented in a low-side configuration which is used to implement a local WAKE event. The series resistor R5 is needed for protection against over current conditions as it limits the current into the WAKE pin when the ECU has lost its ground connection. The pull-up resistor R4 is required to provide sufficient current during stimulation of a WAKE event. In this layout example R4 is set to 3 kΩ and R5 is set to 33 kΩ.
- **Pin 4 (TXD):** The TXD pin is the transmit input signal to the device from the microprocessor. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For slave applications a 220 pF capacitor to ground is implemented. For maser applications and additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See Figure 32.
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (INH):** can have a 100 kΩ resistor to ground as shown by R8.

NOTE

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

ADVANCE INFORMATION

12.2 Layout Example

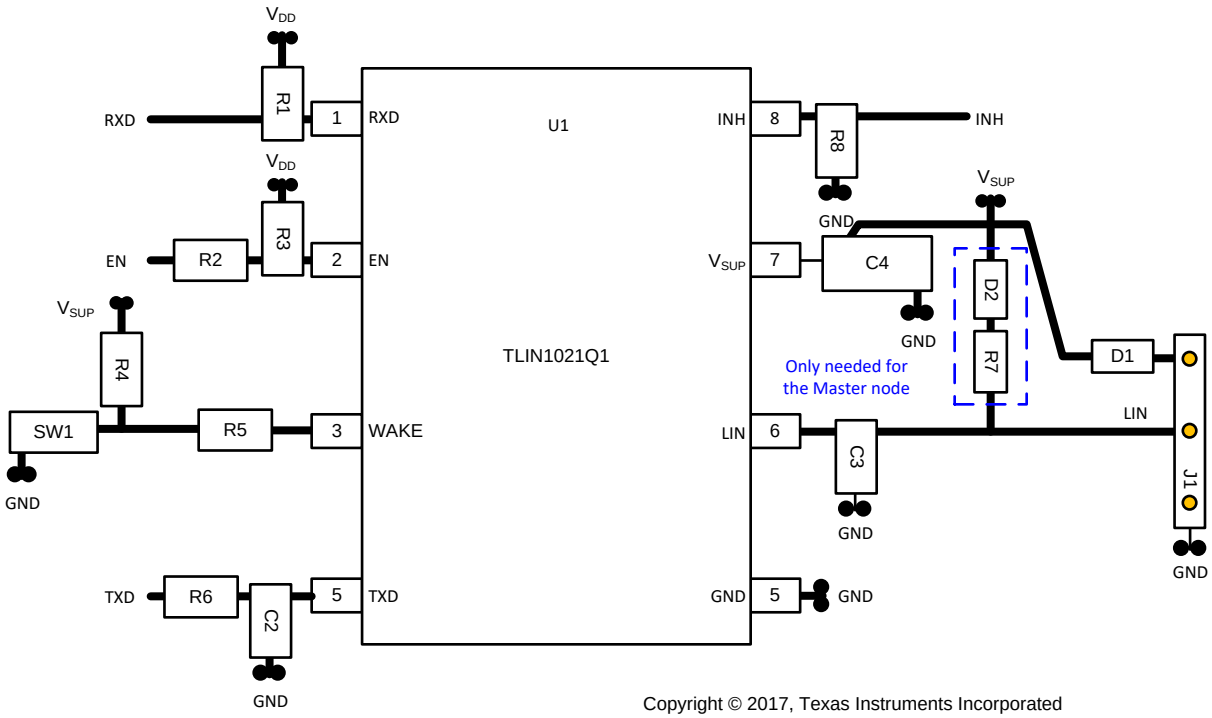


Figure 35. Layout Example

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLIN1021DRBRQ1	ACTIVE	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLIN1021DRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TLIN1021DRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TLIN1021DRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

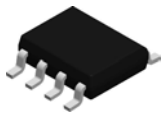
DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

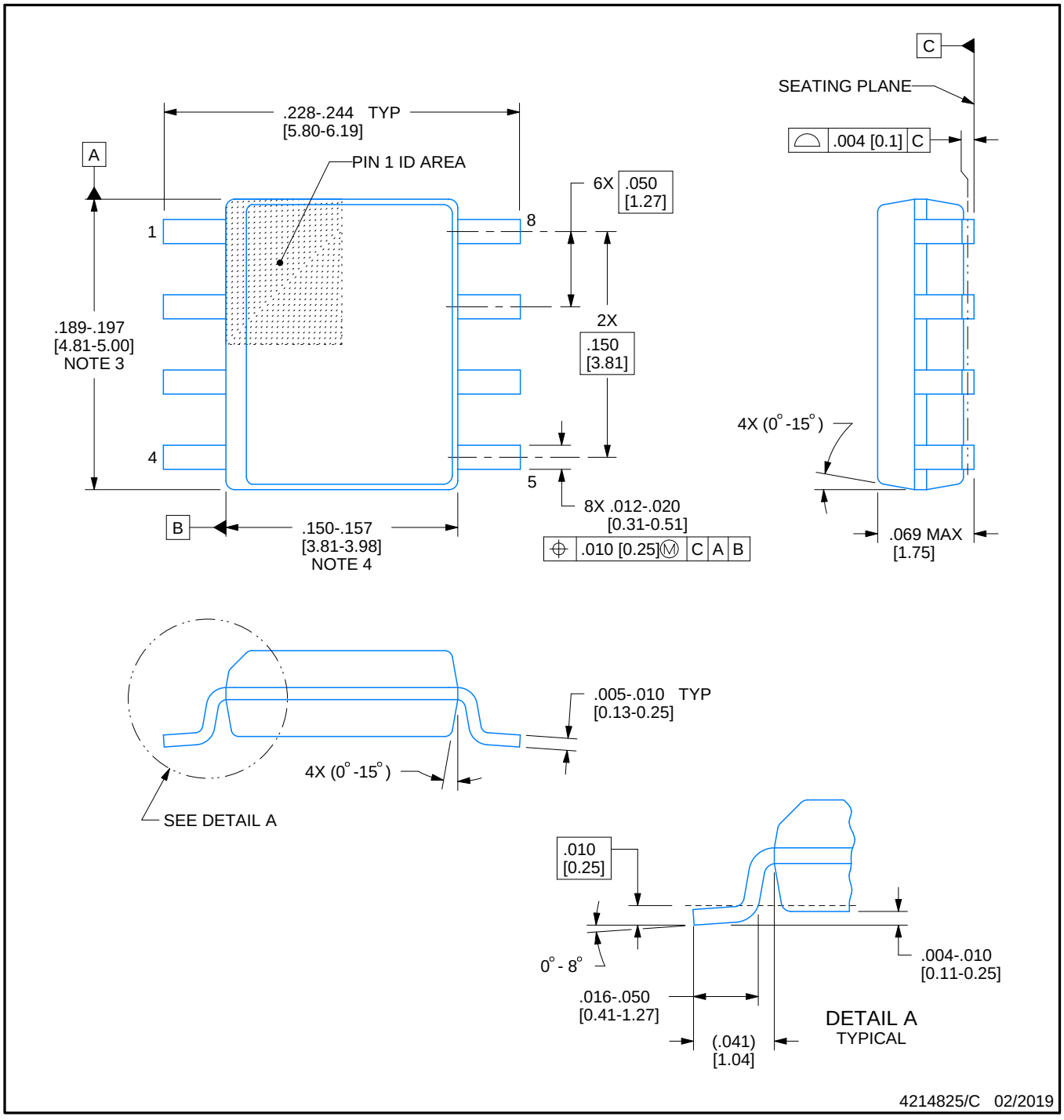


PACKAGE OUTLINE

D0008A

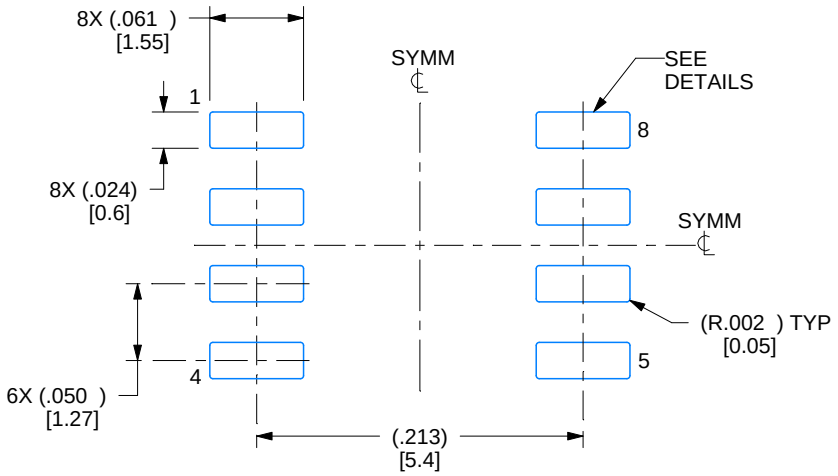
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

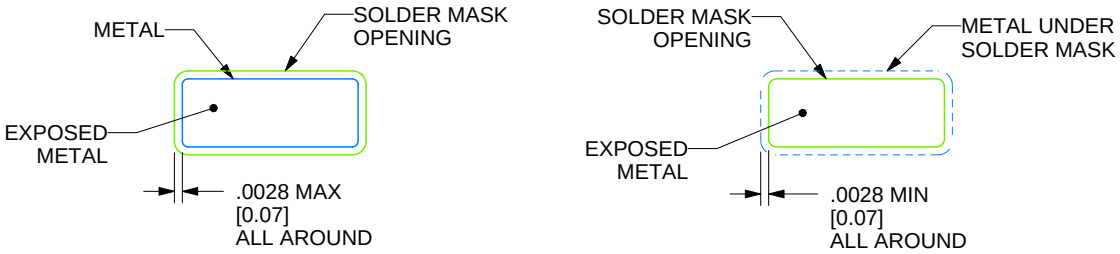


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

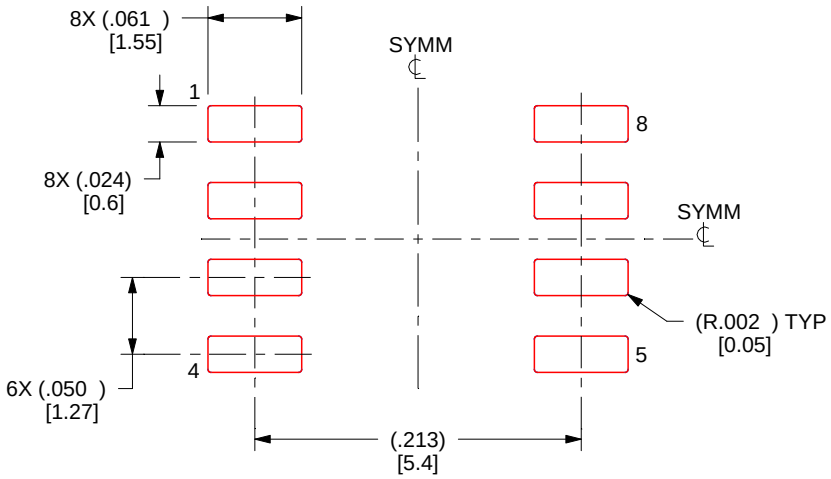
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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