

TLE9104SH

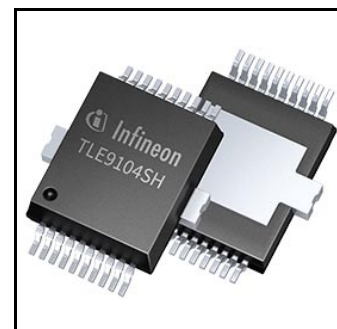
Smart Quad Channel Powertrain Switch



1 Overview

Features

- Configurable overcurrent protection
- Overtemperature protection
- Open load detection
- Short circuit to GND detection
- Electrostatic Discharge (ESD) protection
- 16-Bit SPI (for diagnostic and control)
- Soldering: Automated Optical Inspection capability (AOI)
- Green product (completely lead free)
- AEC qualified



Potential applications

The TLE9104SH is best suited for Automotive Powertrain applications. It can be used as driver IC for inductive and ohmic actuators such as injectors, solenoids and relays.

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

Description

Quad Low-Side Switch in Smart Power Technology (SPT) with four open drain DMOS output stages. The TLE9104SH is protected by embedded protection functions and designed for automotive powertrain applications. The output stages can be controlled directly by parallel inputs for PWM applications (for example gasoline multiport injection) or by SPI.

| Type | Package | Marking |
|-----------|--------------|-----------|
| TLE9104SH | PG-DSO-20-88 | TLE9104SH |

Overview

Table 1 Product summary

| Parameter | Symbol | Value, Unit |
|--|---------------|--------------------|
| Signal supply voltage | V_{IO} | 3.0...5.5 V |
| Analog supply voltage | V_{DD} | 4.5...5.5 V |
| Output clamping voltage | $V_{DS(AZ)}$ | 50...60 V |
| Typical On-state resistance CH 1-4 at $T_j = 25^\circ\text{C}$ | $R_{DS(ON)}$ | 150 m Ω |
| Typical On-state resistance CH 1-4 at $T_j = 150^\circ\text{C}$ | $R_{DS(ON)}$ | 300 m Ω |
| Nominal load current CH 1-4 (continuous) | I_D | 3 A |
| Short circuit to battery detection threshold CH 1-4 | I_{SCB} | 5 A |

Table of contents

| | | |
|----------|--|-----------|
| 1 | Overview | 1 |
| 2 | Block diagram | 4 |
| 3 | Pin configuration | 5 |
| 3.1 | Pin assignment | 5 |
| 3.2 | Pin definitions and functions | 5 |
| 4 | General product characteristics | 7 |
| 4.1 | Absolute maximum ratings | 7 |
| 4.2 | Operating conditions | 8 |
| 5 | Electrical and functional description of blocks | 9 |
| 5.1 | Power supply | 9 |
| 5.2 | Parallel inputs | 10 |
| 5.3 | Power stages | 10 |
| 5.4 | Protection functions | 12 |
| 5.4.1 | Overtemperature protection | 12 |
| 5.4.2 | Short circuit to battery protection | 12 |
| 5.4.3 | Overcurrent protections | 12 |
| 5.5 | Diagnostic functions | 12 |
| 5.5.1 | Output stage status | 15 |
| 5.6 | Communication watchdog | 16 |
| 6 | 16 bit SPI interface | 17 |
| 6.1 | Electrical characteristics 16 bit SPI interface | 17 |
| 6.2 | SPI registers | 19 |
| 6.2.1 | Registers | 22 |
| 7 | Package outlines | 32 |
| 8 | Application information | 33 |
| 9 | Revision history | 34 |

Block diagram

2 Block diagram

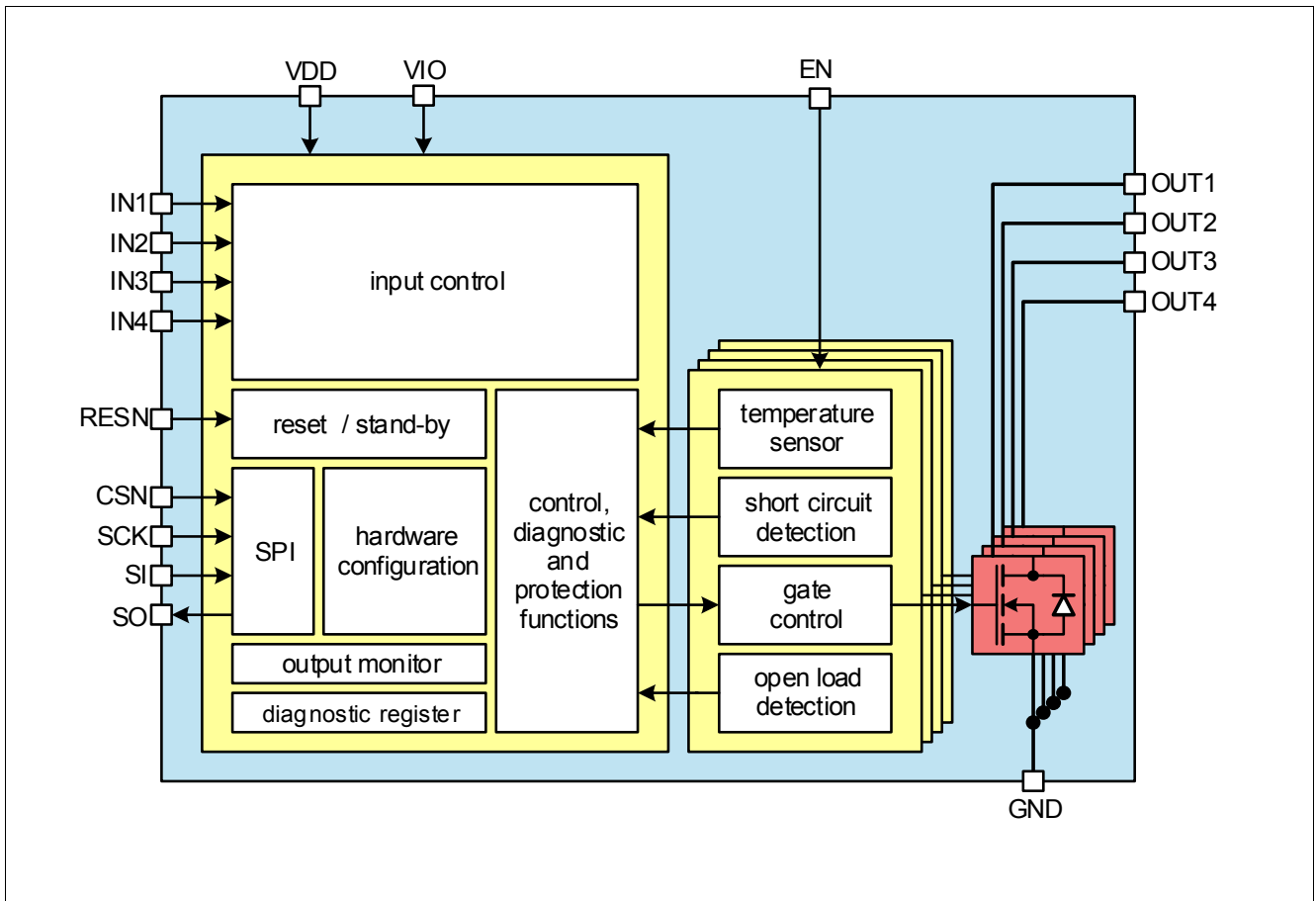


Figure 2-1 Block diagram

Pin configuration

3 Pin configuration

3.1 Pin assignment

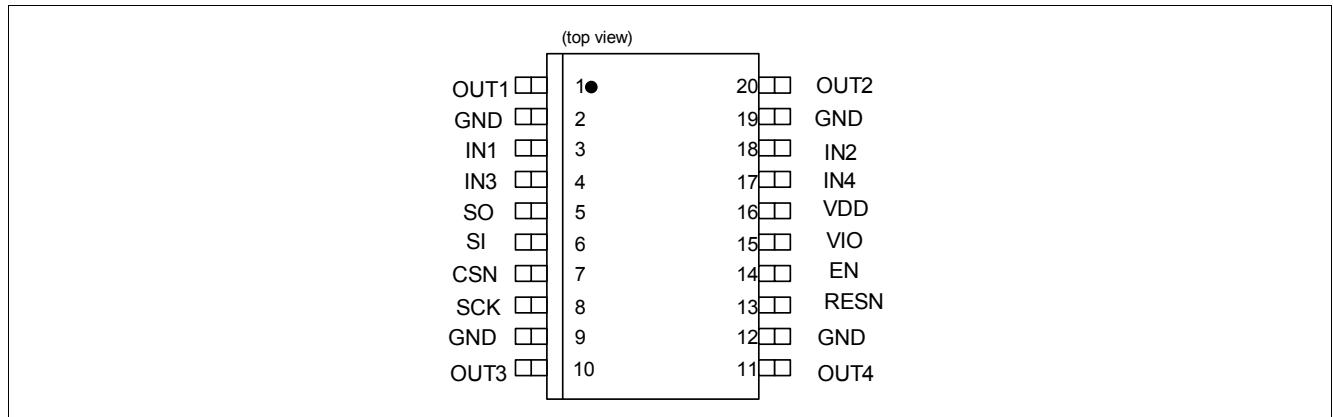


Figure 3-1 Pin configuration (top view)

3.2 Pin definitions and functions

Table 3-1 Pin configuration

| # | Pin Name | Function |
|----|----------|---------------------------------|
| 1 | OUT1 | Power Output 1 |
| 2 | GND | Ground |
| 3 | IN1 | Input 1 |
| 4 | IN3 | Input 3 |
| 5 | SO | Serial Data Output |
| 6 | SI | Serial Data Input |
| 7 | CSN | Serial Chip Select (active low) |
| 8 | SCK | Serial Clock |
| 9 | GND | Ground |
| 10 | OUT3 | Power Output 3 |
| 11 | OUT4 | Power Output 4 |
| 12 | GND | Ground |
| 13 | RESN | Reset (active low) |
| 14 | EN | Output Enable |
| 15 | VIO | Signal Supply Voltage |
| 16 | VDD | Analog Supply Voltage |
| 17 | IN4 | Input 4 |
| 18 | IN2 | Input 2 |
| 19 | GND | Ground |
| 20 | OUT2 | Power Output 2 |

Pin configuration

Notes

1. *The exposed pad of TLE9104SH is not connected to ground internally. It is highly recommended to connect the exposed pad to GND pins externally.*
2. *Pins 2 and 19 are the ground pins of outputs 1 and 2 and pins 9 and 12 are the ground pins of outputs 3 and 4. It is highly recommended to connect all GND pins externally.*

General product characteristics

4 General product characteristics

4.1 Absolute maximum ratings

Table 4-1 Absolute maximum ratings

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------------------|--------|------|----------------|------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Signal supply voltage | V_{IO} | -0.3 | – | 5.5 | V | – | P_4.1.1 |
| Analog supply voltage | V_{DD} | -0.3 | – | 5.5 | V | – | P_4.1.2 |
| Continuous drain source voltage (OUT1 to OUT4) | V_{DS} | -0.3 | – | 50 | V | – | P_4.1.3 |
| Input voltage, all inputs and data outputs, sense lines | V_{IN} | -0.3 | – | $V_{IO} + 0.3$ | V | – | P_4.1.4 |
| Output current per channel ¹⁾ | I_D | 0 | – | 5.5 | A | Output ON | P_4.1.5 |
| Maximum voltage for short circuit protection (single event) ²⁾ | $V_{SC, \text{single}}$ | – | – | 30 | V | – | P_4.1.6 |
| Electrostatic Discharge voltage - HBM (human body model) ³⁾ | V_{ESD1} | -2000 | – | 2000 | V | – | P_4.1.7 |
| Electrostatic Discharge voltage - CDM (charge device model) ⁴⁾ | V_{ESD2} | -500 | – | 500 | V | – | P_4.1.8 |

- 1) Output current rating as long as maximum junction temperature is not exceeded. The maximum output current in the application must be calculated using R_{thJA} depending on mounting conditions.
- 2) Short circuit is designed to be short circuit robust according to AEC-Q100-012.
- 3) According to ANSI/ESDA/JEDEC JS-001.
- 4) According to JESD22-C101.

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

General product characteristics

4.2 Operating conditions

Table 4-2 Operating conditions

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|------------|---------------------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Maximum output clamping energy, linearly decreasing current ^{1) 2)} | E_{AR} | 14 | – | – | mJ | $I_{D(0)} = 1.4 \text{ A}$, $T_{J(0)} = 110^\circ\text{C}$, Cycles: 1 billion | P_4.2.6 |
| Maximum output clamping energy, linearly decreasing current ³⁾ | E_{AS} | 35 | – | – | mJ | $T_J = 85^\circ\text{C}$, Cycles: 10 | P_4.2.13 |
| Maximum output clamping energy, linearly decreasing current | E_{AS} | 25 | – | – | mJ | $T_J = 145^\circ\text{C}$, Cycles: 10 | P_4.2.14 |
| Maximum output clamping energy in parallel mode | $E_{AR,p}$ | $1.7 \times E_{AR}$ | – | – | mJ | OUT1&2 or OUT3&4, $I_{D(0),P} = 1.8 \times I_{D(0)}$ | P_4.2.2 |

Thermal resistance

| | | | | | | | |
|------------------|------------|---|---|------|-----|---|---------|
| Junction to case | R_{thJC} | – | 1 | 1.25 | K/W | PV = 3 W, homogenously distributed between all output stages | P_4.2.3 |
|------------------|------------|---|---|------|-----|---|---------|

Temperature range

| | | | | | | | |
|-----------------------------|-----------|-----|---|-----|----|---|---------|
| Operating temperature range | T_j | -40 | – | 150 | °C | – | P_4.2.4 |
| Storage temperature range | T_{stg} | -55 | – | 150 | °C | – | P_4.2.5 |

1) Pulse shape represents inductive switch off: $I_D(t) = I_D(0) \times (1 - t/t_{pulse})$; $0 < t < t_{pulse}$

2) The given energy values are based on a cumulative scenario as specified in the Notes column.

3) The given energy values are based on a cumulative scenario as specified in the Notes column.

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given by the related electrical characteristics table.

5 Electrical and functional description of blocks

5.1 Power supply

The TLE9104SH is supplied by analog power supply line V_{DD} and signal power supply V_{IO} . A capacitor between pins V_{DD} to GND and V_{IO} to GND is recommended. After start-up of the power supply, the RESN pin should be kept low until the Reset Duration Time has expired. This will reset all SPI registers to their default values. In order to enable the output stages the EN pin has to be kept high and OUT_EN register has to be set.

Table 5-1 Electrical characteristics: power supply

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------|--------|------|----------------|---------------|--------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Signal supply voltage | V_{IO} | 3 | – | 5.5 | V | – | P_5.1.1 |
| Analog supply voltage | V_{DD} | 4.5 | – | 5.5 | V | – | P_5.1.2 |
| Supply current | $I_{DD(on)}$ | – | – | 10 | mA | – | P_5.1.3 |
| Input low voltage of pin RESN | $V_{RESN(L)}$ | -0.3 | – | 1 | V | – | P_5.1.4 |
| Input high voltage of pin RESN | $V_{RESN(H)}$ | 2 | – | $V_{IO} + 0.3$ | V | – | P_5.1.5 |
| Hysteresis voltage of pin RESN | $V_{RESN(Hys)}$ | 100 | 300 | 500 | mV | – | P_5.1.6 |
| Input pull-up current through pin RESN | I_{RESN} | -100 | -65 | -30 | μA | $V_{RESET} = 0\text{ V}$ | P_5.1.7 |
| Reset duration time ¹⁾ | $t_{RESN(L)}$ | 10 | – | – | μs | – | P_5.1.8 |
| Input low voltage of pin EN | $V_{EN(L)}$ | -0.3 | – | 1 | V | – | P_5.1.9 |
| Input high voltage of pin EN | $V_{EN(H)}$ | 2 | – | $V_{IO} + 0.3$ | V | – | P_5.1.10 |
| Hysteresis voltage of pin EN | $V_{EN(Hys)}$ | 100 | 300 | 500 | mV | – | P_5.1.11 |
| Input pull-down current through pin EN | I_{EN} | 30 | 65 | 100 | μA | $V_{EN} = 2\text{ V}$ | P_5.1.12 |

1) For proper startup, after the supply V_{DD} has reached its final voltage, the RESN pin should be held low until the reset duration time has expired.

Electrical and functional description of blocks

5.2 Parallel inputs

Each input signal controls the output stage of its related channel. For example, IN1 controls OUT1, IN2 controls OUT2 etc. Input signals are active low. Hence, applying a voltage less than $V_{IN(L)}$ to INx turns OUTx on. It is possible to connect OUT1-2 and OUT3-4 in parallel. For this purpose the right configuration has to be selected in the CFG register. In this case IN1 controls OUT1-2 and IN3 controls OUT3-4.

Table 5-2 Electrical characteristics: parallel inputs

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin SO)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------------------------|---------------|--------|------|----------------|---------------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Input low voltage of pin INx | $V_{IN(L)}$ | -0.3 | - | 1 | V | - | P_5.2.1 |
| Input high voltage of pin INx | $V_{IN(H)}$ | 2 | - | $V_{IO} + 0.3$ | V | - | P_5.2.2 |
| Input voltage hysteresis | $V_{IN(Hys)}$ | 100 | 300 | 500 | mV | - | P_5.2.3 |
| Input pull-up current through pin INx | $I_{IN(L)}$ | -100 | -65 | -30 | μA | $V_{IN} = 0\text{ V}$ | P_5.2.4 |

5.3 Power stages

Table 5-3 Electrical characteristics: power outputs

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin SO)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------------|-----------------|--------|------|------|---------------|--|---------|
| | | Min. | Typ. | Max. | | | |
| ON resistance | $R_{DS(ON)}$ | - | 150 | | m Ω | $T_j = 25^\circ\text{C}$, | P_5.3.1 |
| ON resistance | $R_{DS(ON)}$ | - | 300 | 350 | m Ω | $T_j = 150^\circ\text{C}$, | P_5.3.2 |
| ON resistance in parallel mode | $R_{DS(ON)}$ | - | 75 | - | m Ω | $T_j = 25^\circ\text{C}$, outputs 1&2 or 3&4 in parallel | P_5.3.3 |
| ON resistance in parallel mode | $R_{DS(ON)}$ | - | 150 | 175 | m Ω | $T_j = 150^\circ\text{C}$, outputs 1&2 or 3&4 in parallel | P_5.3.4 |
| Output clamping voltage | $V_{DS(AZ)}$ | 50 | - | 60 | V | output OFF | P_5.3.5 |
| Output leakage current | $I_{D(lkg)}$ | - | - | 10 | μA | RESN=0 | P_5.3.6 |
| Output off-state current | I_{OUTx_OFF} | - | - | 30 | μA | RESN=1, OUTx_DIAG_EN =0, $V_{OUTx} = 35\text{ V}$ | P_5.3.6 |
| Turn-on time | t_{ON} | - | 15 | - | μs | from 50% of INx to 20% of Vbat | P_5.3.7 |

Electrical and functional description of blocks

Table 5-3 Electrical characteristics: power outputs (cont'd)

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin S0)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------------|-------------|--------|------|------|------------------|--------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Turn-off time | t_{OFF} | – | 15 | – | μs | from 50% of INx to 80% of Vbat | P_5.3.8 |
| Overtemperature shutdown threshold | $T_{j(OT)}$ | 165 | – | 200 | $^\circ\text{C}$ | – | P_5.3.9 |

Electrical and functional description of blocks

5.4 Protection functions

The TLE9104SH provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered “outside” the normal operating range. Protection functions are not designed for continuous repetitive operation. Following protection functions are implemented for TLE9104SH:

- Overtemperature protection (OT).
- Short circuit to battery protection (SCB).
- Overcurrent protection (OC).

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5.4.1 Overtemperature protection

A dedicated temperature sensor for each channel detects if the temperature of its channel exceeds the overtemperature shutdown threshold. If the channel temperature exceeds the overtemperature shutdown threshold, the overheated channel is switched off immediately to prevent destruction. The channel can be turned on again after clearing the overtemperature error; however, if the sensed temperature is still higher than the overtemperature shutdown threshold the channel will switch off after the filter time t_{OT} .

5.4.2 Short circuit to battery protection

The TLE9104SH is protected in case of short circuit to battery. If the current of an output channel exceeds I_{SCB} , the respective channel is switched off immediately. The channel can be turned on again after the fault condition has been removed and the error has been cleared.

5.4.3 Overcurrent protections

The TLE9104SH is protected with configurable overcurrent protection. If the current of an output channel exceeds I_{OC} , the respective channel is switched off after the filter time $t_{d(OC)}$. The channel can be turned on again after the fault condition has been removed and the error has been cleared. Both current limit threshold I_{OC} and its filter time $t_{d(OC)}$ are configurable via SPI. The filter time, $t_{d(OC)}$, and the current limit threshold, I_{OC} , can only be configured while the output bit, OUT_EN, is low in the SPI register.

5.5 Diagnostic functions

Following diagnosis functions are implemented for all output stages of TLE9104SH:

- Short to battery detection (SCB) can be detected if stages are turned on.
- Overtemperature detection (OT) can be detected if stages are turned on.
- Time based overcurrent detection (OCF) can be detected if stages are turned on.
- Temperature based overcurrent detection (OCT) can be detected if stages are turned on.
- Short to GND detection (SCG) can be detected if stages are turned off.
- Open load detection (OL) can be detected if stages are turned off.

The diagnosis information of TLE9104SH can be accessed via SPI interface. OL and SCG diagnosis are recognized using two thresholds ($V_{OUTn-SCG}$ and $V_{OUTn-OL}$). It is also possible to turn off the internal diagnostic pull-down and pull-up current sources. In this case diagnosis of OL and SCG are deactivated.

Electrical and functional description of blocks

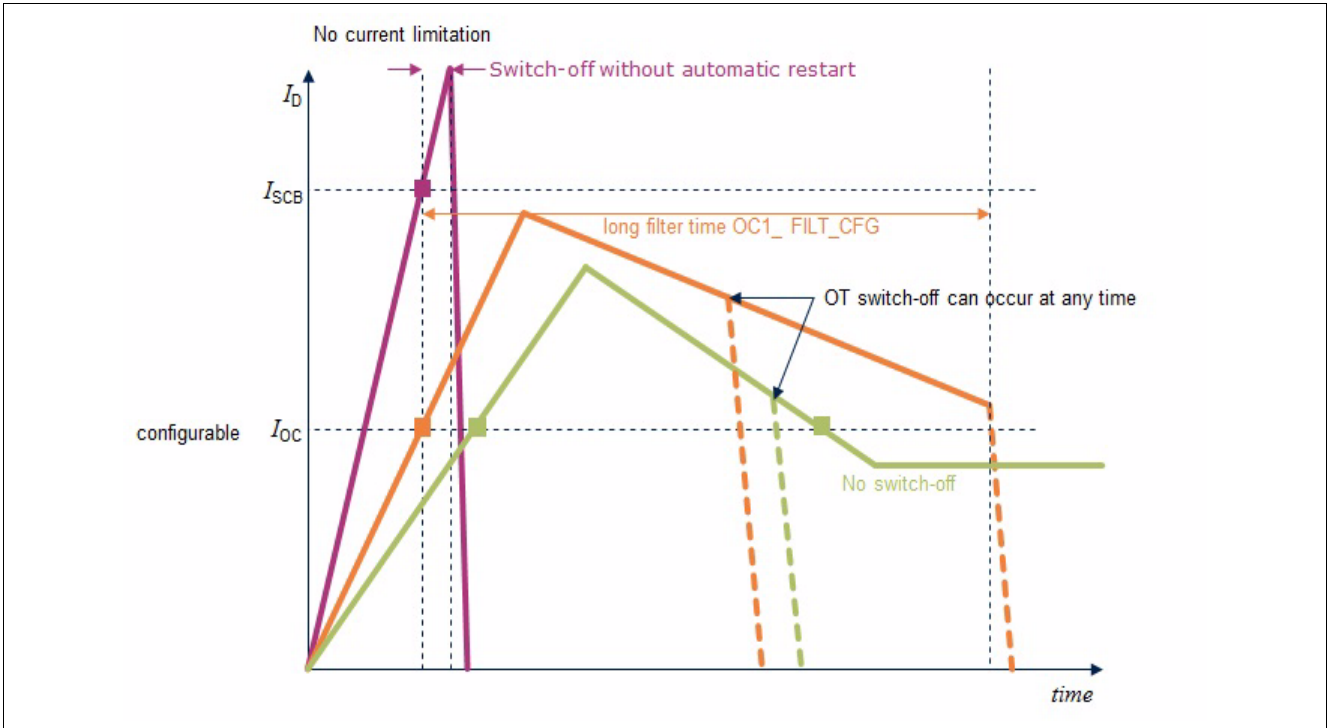


Figure 5-1 Overcurrent and short circuit to battery protection

The fault conditions SCG and OL will not be stored until an integrated filtering time, $t_{d(fault)}$, has expired. An additional blanking time, $t_{b(fault)}$, can be configured in addition to the filter time. The blanking time, $t_{b(fault)}$, can only be configured while output enable bit, OUT_EN, is low in the SPI register.

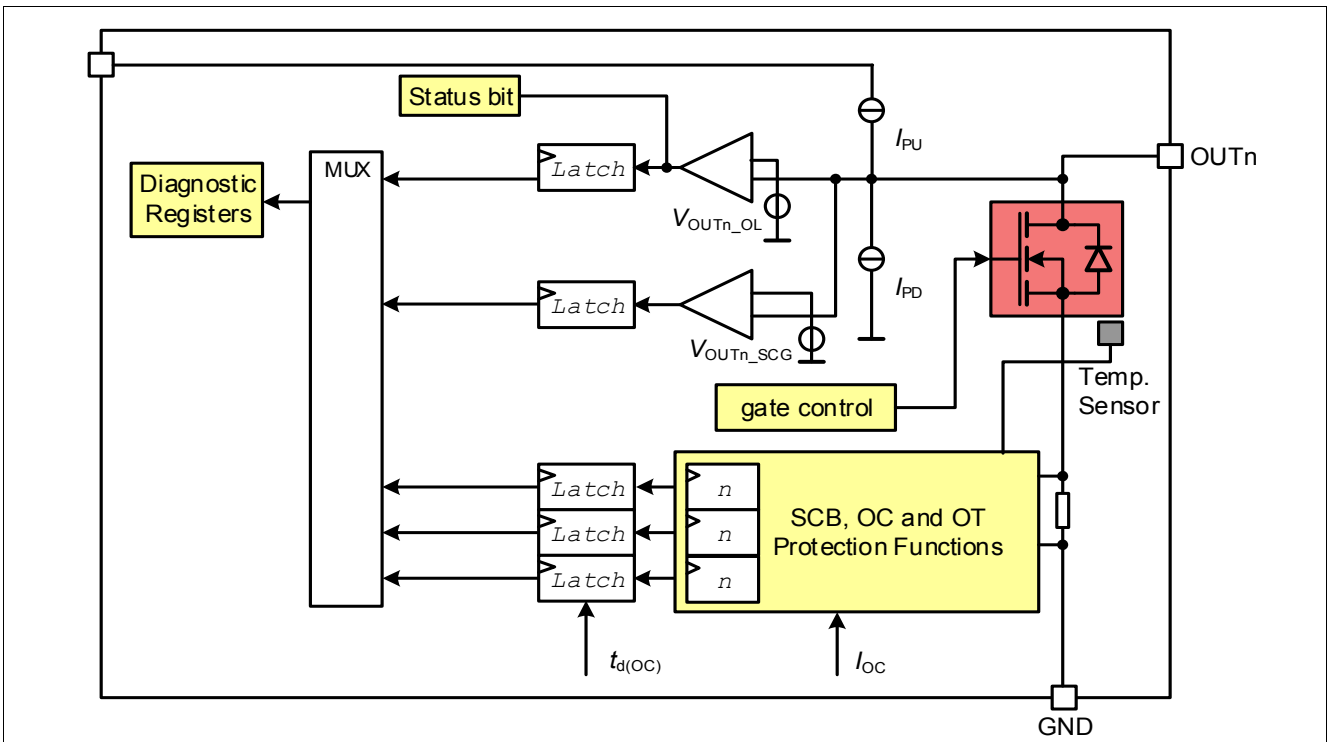


Figure 5-2 Diagnostic functions (overview only)

Electrical and functional description of blocks

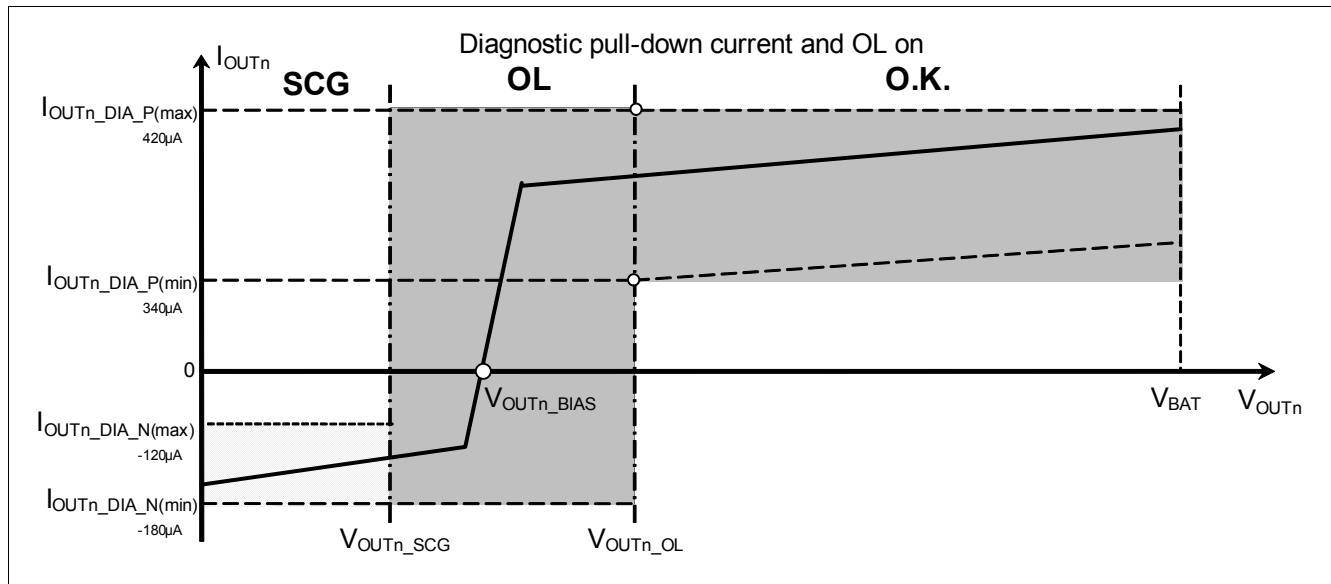


Figure 5-3 SCG and OL diagnostic function (overview only)

Table 5-4 Electrical characteristics: diagnostic functions

$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$, $V_{IO} = 3\text{ V to } 5.5\text{ V}$, $T_j = -40^\circ\text{C to } +150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin SO)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|----------------|--------------------|------|--------------------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Open load detection voltage | $V_{OUTn-OL}$ | $0.6 V_{DD} - 0.2$ | – | $0.6 V_{DD} + 0.2$ | V | – | P_5.5.1 |
| Diagnostic pull-down current | I_{PD} | 300 | 380 | 450 | µA | $V_{OUTn} = 0.6 V_{DD}$ | P_5.5.2 |
| Diagnostic pull-up current | I_{PU} | -180 | -150 | -120 | µA | $V_{OUTn} = 0.4 V_{DD}$ | P_5.5.3 |
| Short circuit to ground detection voltage | $V_{OUTn-SCG}$ | $0.4 V_{DD} - 0.2$ | – | $0.4 V_{DD} + 0.2$ | V | – | P_5.5.4 |
| Short circuit to battery detection current | I_{SCB} | 4.5 | 5 | 5.5 | A | – | P_5.5.5 |
| Short circuit to battery detection current in parallel mode | I_{SCB} | 9 | 10 | 11 | A | Outputs 1&2 or outputs 3&4 connected in parallel | P_5.5.6 |
| Fault filtering time ¹⁾ | $t_{d(fault)}$ | 0.015 | 0.02 | 0.025 | ms | | P_5.5.7 |
| Fault blanking time ²⁾ | $t_{b(fault)}$ | 0.16 | 0.2 | 0.24 | ms | configurable via SPI | P_5.5.8 |
| Fault blanking time | $t_{b(fault)}$ | 0.4 | 0.5 | 0.60 | ms | default value | P_5.5.9 |
| Fault blanking time | $t_{b(fault)}$ | 0.8 | 1 | 1.2 | ms | configurable via SPI | P_5.5.10 |
| Fault blanking time | $t_{b(fault)}$ | 1.6 | 2 | 2.4 | ms | configurable via SPI | P_5.5.11 |
| Overcurrent filtering time | $t_{d(OC)}$ | 0.04 | 0.06 | 0.08 | ms | default value | P_5.5.12 |
| Overcurrent filtering time | $t_{d(OC)}$ | 0.1 | 0.12 | 0.14 | ms | configurable via SPI | P_5.5.13 |
| Overcurrent filtering time | $t_{d(OC)}$ | 0.4 | 0.5 | 0.6 | ms | configurable via SPI | P_5.5.14 |

Electrical and functional description of blocks

Table 5-4 Electrical characteristics: diagnostic functions (cont'd)

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin S0)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Overcurrent filtering time | $t_{d(OC)}$ | 0.8 | 1 | 1.2 | ms | configurable via SPI | P_5.5.15 |
| Overcurrent filtering time | $t_{d(OC)}$ | 4 | 5 | 6 | ms | configurable via SPI | P_5.5.16 |
| Overcurrent filtering time | $t_{d(OC)}$ | 8 | 10 | 12 | ms | configurable via SPI | P_5.5.17 |
| Overcurrent filtering time | $t_{d(OC)}$ | 16 | 20 | 24 | ms | configurable via SPI | P_5.5.18 |
| Overcurrent filtering time | $t_{d(OC)}$ | 24 | 30 | 36 | ms | configurable via SPI | P_5.5.19 |
| Overcurrent threshold | I_{OC} | 0.75 | 1 | 1.25 | A | configurable via SPI | P_5.5.20 |
| Overcurrent threshold | I_{OC} | 1.75 | 2 | 2.25 | A | default value | P_5.5.21 |
| Overcurrent threshold | I_{OC} | 2.5 | 3 | 3.5 | A | configurable via SPI | P_5.5.22 |
| Overcurrent threshold | I_{OC} | 3.5 | 4 | 4.5 | A | configurable via SPI | P_5.5.23 |
| Overcurrent threshold in parallel mode | I_{OC} | 1.35 | 2 | 2.5 | A | configurable via SPI, outputs 1&2 or outputs 3&4 connected in parallel | P_5.5.24 |
| Overcurrent threshold in parallel mode | I_{OC} | 3.15 | 4 | 4.5 | A | default value, outputs 1&2 or outputs 3&4 connected in parallel | P_5.5.25 |
| Overcurrent threshold in parallel mode | I_{OC} | 4.5 | 6 | 7 | A | configurable via SPI, outputs 1&2 or outputs 3&4 connected in parallel | P_5.5.26 |
| Overcurrent threshold in parallel mode | I_{OC} | 6.3 | 8 | 9 | A | configurable via SPI, outputs 1&2 or outputs 3&4 connected in parallel | P_5.5.27 |
| Overtemperature filter time | t_{OT} | 2 | 3 | 4 | μs | – | P_5.5.28 |
| Short circuit to battery filter time | t_{SCB} | 1.2 | – | 2 | μs | – | P_5.5.28 |

- 1) $t_{d(\text{fault})}$ is the filter time for open load and short to ground diagnostic functions.
- 2) $t_{d(\text{fault})}$ is the blanking time for open load and short to ground diagnostic functions.

5.5.1 Output stage status

The output of open-load comparator of each channel is directly available via OUTx_STAT bit. This bit can be used to detect a failure condition in which the channel is turned on by INx or SPI but the power stage remains switched off. The delay between a turn on via INx or SPI and a change in status bit depends on the output voltage slew rates and hence on the load itself.

Electrical and functional description of blocks

5.6 Communication watchdog

The TLE9104SH is using the watchdog principle to monitor the SPI communication. In case of no communication or continuous communication failures all outputs are disabled. In case of a faulty SPI frame the CWD timer does not retrigger and after the filter time the register CWD-TO is set and can be read as soon as the SPI is back to normal operation. The watchdog is active by default; however, it can be deactivated via a SPI command.

The watchdog starts to work as soon as the device has finished start-up and all blocks are released from reset. If these conditions are met, the watchdog timer t_{CWD} is started. Each correct SPI communication restarts the t_{CWD} timer. If no valid communication is received within timeout, the t_{CWD} timer will expire and disable all outputs. For re-enabling, one needs to clear the error and enable outputs via SPI. Outputs will not be enabled automatically by clearing the error.

The watchdog timer t_{CWD} is configurable via SPI. The watchdog timer t_{CWD} can only be configured while the output enable bit, OUT_EN, is low in the SPI register.

Following SPI communication issues are detected as failure by the watchdog:

- No communication
- Wrong commands
- Frames not equal to 16 clocks

Table 5-5 Communication watchdog timeout configuration

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, (unless otherwise specified)
 all voltages with respect to ground, positive current flowing into pin (unless for pin SO)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------------|------------|--------|------|------|------|------------------------|-------------------------|
| | | Min. | Typ. | Max. | | | |
| Communication watchdog timeout | t_{CWD0} | 20 | 25 | 30 | ms | configurable via SPI | P_5.6.1 |
| Communication watchdog timeout | t_{CWD1} | 40 | 50 | 60 | ms | default value | P_5.6.2 |
| Communication watchdog timeout | t_{CWD2} | 60 | 75 | 90 | ms | configurable via SPI | P_5.6.3 |

16 bit SPI interface

6 16 bit SPI interface

The diagnostic and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCK, CSN. Data is transferred by the lines SI and SO at the data rate given by SCK. The falling edge of CSN indicated the beginning of a data access. Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK. Each access shall be terminated by a rising edge of CSN. A modulo 16 counter ensures that data is taken only, when a multiple of 16 bits has been transferred.

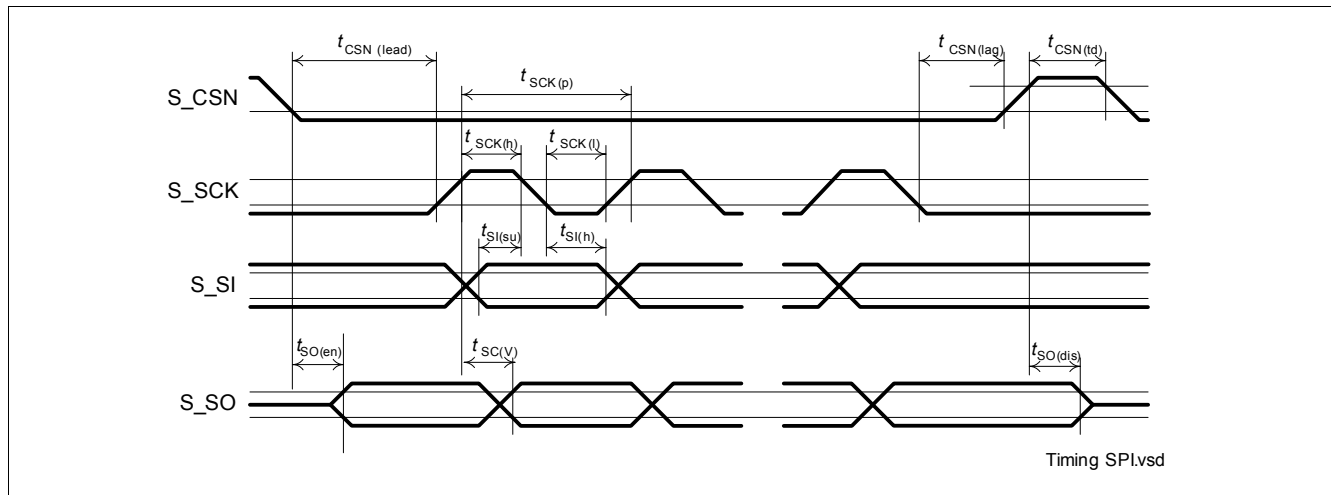


Figure 6-1 SPI timing

6.1 Electrical characteristics 16 bit SPI interface

Table 6-1 Electrical characteristics: 16 bit SPI interface

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|--|----------------|------|----------------|---------------|-----------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Input characteristics (CSN, SCK, SI) | | | | | | | |
| L level of pin CSN, SCK, SI | V_{IO_CSNL} V_{IO_SCKL} V_{IO_SIL} | -0.3 | - | 1 | V | - | P_6.1.1 |
| H level of pin CSN, SCK, SI | V_{IO_CSNH} V_{IO_SCKH} V_{IO_SIH} | 2 | - | $V_{IO} + 0.3$ | V | - | P_6.1.2 |
| Hysteresis input pins | V_{IO_CSNHy} V_{IO_SCKHy} V_{IO_SIHy} | 100 | 300 | 500 | mV | - | P_6.1.3 |
| Output characteristics (SO) | | | | | | | |
| L level output voltage | V_{IO_SOL} | 0 | - | 1 | V | $I_{IO_SO} = -2\text{ mA}$ | P_6.1.4 |
| H level output voltage | V_{IO_SOH} | $V_{IO} - 0.5$ | - | $V_{IO} + 0.3$ | - | - | P_6.1.5 |
| Output tristate leakage current | I_{IO_SOoff} | -10 | - | 10 | μA | - | P_6.1.6 |

16 bit SPI interface

Table 6-1 Electrical characteristics: 16 bit SPI interface

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $V_{IO} = 3\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------|--------|------|------|---------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Input capacitance | | | | | | | |
| For CSN, SCK, SI and SO | C_{in} | – | 6 | 8 | pF | – | P_6.1.13 |
| Timings | | | | | | | |
| Serial clock frequency ¹⁾ | f_{SCK} | 0 | – | 8 | MHz | $C_L = 25\text{ pF}$ | P_6.1.7 |
| Serial clock period | $t_{SCK(P)}$ | 125 | – | – | ns | – | P_6.1.8 |
| Serial clock high time | $t_{SCK(h)}$ | 50 | – | – | ns | – | P_6.1.9 |
| Serial clock low time | $t_{SCK(l)}$ | 50 | – | – | ns | – | P_6.1.10 |
| Enable lead time (falling CSN to rising SCK) | $t_{CSN(lead)}$ | 250 | – | – | ns | – | P_6.1.11 |
| Enable lag time (falling SCK to rising CSN) | $t_{CSN(lag)}$ | 250 | – | – | ns | – | P_6.1.12 |
| Data setup time (required time SI to falling SCK) | $t_{SI(su)}$ | 20 | – | – | ns | – | P_6.1.14 |
| Data hold time (falling SCK to SI) | $t_{SI(h)}$ | 20 | – | – | ns | – | P_6.1.15 |
| Output enable time (falling CSN to SO valid) | $t_{SO(en)}$ | – | – | 200 | ns | $C_L = 25\text{ pF}$ | P_6.1.16 |
| Output disable time (rising CSN to SO tri-state) | $t_{SO(dis)}$ | – | – | 200 | ns | $C_L = 25\text{ pF}$ | P_6.1.17 |
| Output data valid time with capacitive load | $t_{SO(v)}$ | – | – | 100 | ns | $C_L = 25\text{ pF}$ | P_6.1.18 |
| Transfer delay time (rising CSN to falling CSN) | $t_{CSN(td)}$ | 1 | – | 100 | μs | $C_L = 25\text{ pF}$ | P_6.1.19 |

1) Maximum SPI clock frequency in the application may be less depending on the load at the SO pin and the microcontroller SPI peripheral timing requirements.

16 bit SPI interface

6.2 SPI registers

The general SPI frame length is fixed at 16 bits. Bits 0 to 7 of each frame are used as data frame, bits 8 to 10 are used for address, bit 14 is the parity bit and bit 15 is used to specify a command as read or write. The parity bit is defined as:

$$b_{14} = (1 + b_{15} + \sum_{i=0}^{13} b_i) \bmod 2 \tag{6.1}$$

MOSI

| | | | | | | | | | | | | | | | |
|------------|---------------|----------|----------|----------------|----|---|---|-------------|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W | Parity | 0 | 0 | Address | | | | Data | | | | | | | |

MISO

| | | | | | | | | | | | | | | | |
|------------|---------------|----------------------------|---------------------|----------------|----|---|---|-------------|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W | Parity | Fault Communication | Fault Global | Address | | | | Data | | | | | | | |

IN MOSI and MISO a read is defined with a ‘0’ and a write is defined with a ‘1’. Each MISO SPI frame reports the important system faults as Global or Communication faults in bit 12 and 13 as following:

- Global fault is asserted (not latching) when the general fault bit in Global_Status register is set.
- Communication fault is asserted (not latching) when one of the following faults are present:
 - Communication error (the same as COM_ERR in Global_Status register)
 - Communication watchdog timeout
 - Parity error

Besides, global status register stores the faults as following:

- General fault if at least one of the following faults are present:
 - Over-current
 - Over-temperature
 - Over-temperature during overcurrent
 - Short circuit to battery
 - Open load
 - Short circuit to ground
- Communication error:
 - No communication
 - Wrong command
 - Frames not equal to 16 bits
- Parity error
- Communication watchdog

16 bit SPI interface

Apart from the faults, global register also restores the enable latch signal (EN_Latch) and power on reset latch (POR_Latch) as following:

- EN_Latch: This bit has a reset value of '0'. After setting the OUT_EN bit this bit changes to '1'. This bit shows whether the output has been enabled (via SPI) at least once since the last clear.
- POR_Latch: This bit has a reset value of '1'. It can be changed to '0' via SPI. Any power on reset will set the bit back to 1. This can be used to check whether a power on reset has happened since the bit value was changed to '0'.

16 bit SPI interface

Table 6-2 Register Address Space

| Module | Base Address | End Address | Note |
|--------|----------------|-----------------|------|
| apb | 0 _H | 1F _H | – |

Table 6-3 Register Overview

| Register Short Name | Register Long Name | Offset Address | Page Number |
|------------------------|---|-----------------|-------------|
| CTRL | Output control register | 00 _H | 22 |
| CFG | Configuration register | 01 _H | 24 |
| OFF_DIAG_CFG | Off-state diagnostic configuration register | 02 _H | 25 |
| ON_DIAG_CFG | On-state diagnostic configuration register | 03 _H | 26 |
| DIAG_OUT_1_2_ON | On-state diagnostic result register OUT1 & OUT2 | 04 _H | 27 |
| DIAG_OUT_3_4_ON | On-state diagnostic result register OUT3 & OUT4 | 05 _H | 28 |
| DIAG_OFF | Off-state diagnostic result register | 06 _H | 29 |
| GLOBAL_STATUS | Global device status register | 07 _H | 30 |
| ICVID | IC Version ID | 08 _H | 31 |

The registers are addressed wordwise.

Table 6-4 Register Overview

| Bit type short name | Bit type description | Note |
|---------------------|-------------------------|------------------|
| r | read | – |
| rw | read/write | – |
| rwc | read and clear on write | clear on write 0 |

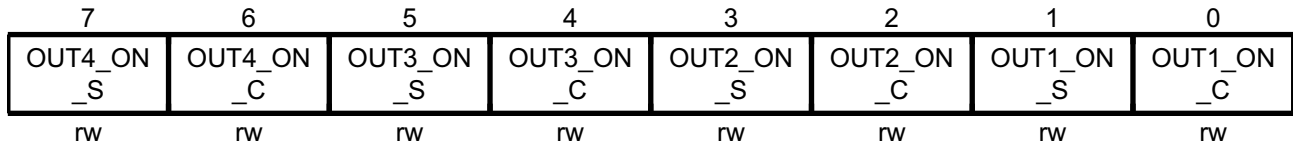
Note: All configurations can only be changed while the OUT_EN bit is cleared.

16 bit SPI interface

6.2.1 Registers

Output control register

| CTRL | Offset | Reset Value |
|-------------------------|-----------------|-----------------|
| Output control register | 00 _H | 00 _H |



| Field | Bits | Type | Description |
|-----------|------|------|--|
| OUT4_ON_S | 7 | rw | OUT4 SPI control bit (used if CFG.OUT4_DD = 0) 1 _D SET , Output 4 set 0 _D NO_ACTION , Output 4 no action Reset: 0 _B |
| OUT4_ON_C | 6 | rw | OUT4 SPI control bit (used if CFG.OUT4_DD = 0) 1 _D CLEAR , Output 4 clear 0 _D NO_ACTION , Output 4 no action Reset: 0 _B |
| OUT3_ON_S | 5 | rw | OUT3 SPI control bit (used if CFG.OUT3_DD = 0) 1 _D SET , Output 3 set 0 _D NO_ACTION , Output 3 no action Reset: 0 _B |
| OUT3_ON_C | 4 | rw | OUT3 SPI control bit (used if CFG.OUT3_DD = 0) 1 _D CLEAR , Output 3 clear 0 _D NO_ACTION , Output 3 no action Reset: 0 _B |
| OUT2_ON_S | 3 | rw | OUT2 SPI control bit (used if CFG.OUT2_DD = 0) 1 _D SET , Output 2 set 0 _D NO_ACTION , Output 2 no action Reset: 0 _B |
| OUT2_ON_C | 2 | rw | OUT2 SPI control bit (used if CFG.OUT2_DD = 0) 1 _D CLEAR , Output 2 clear 0 _D NO_ACTION , Output 2 no action Reset: 0 _B |
| OUT1_ON_S | 1 | rw | OUT1 SPI control bit (used if CFG.OUT1_DD = 0) 1 _D SET , Output 1 set 0 _D NO_ACTION , Output 1 no action Reset: 0 _B |

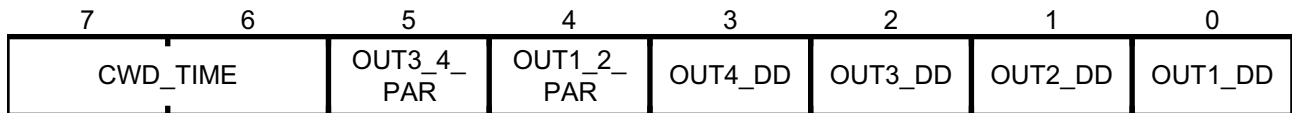
16 bit SPI interface

| Field | Bits | Type | Description |
|------------------|-------------|-------------|--|
| OUT1_ON_C | 0 | rw | OUT1 SPI control bit (used if CFG.OUT1_DD = 0) 1 _D CLEAR , Output 1 clear 0 _D NO_ACTION , Output 1 no action Reset: 0 _B |

16 bit SPI interface

Configuration register

CFG **Offset** **Reset Value**
Configuration register **01_H** **8F_H**

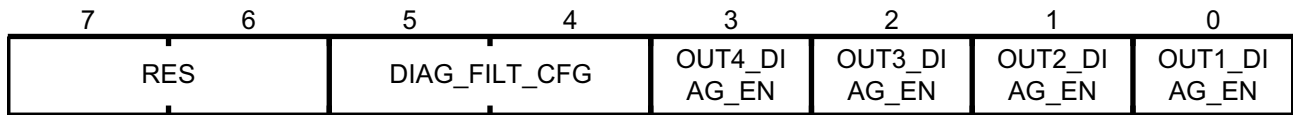


| Field | Bits | Type | Description |
|-------------------|------|------|--|
| CWD_TIME | 7:6 | rw | Communication watchdog timeout configuration 3 _D LONG , 75 ms 2 _D MEDIUM , 50 ms (default) 1 _D SHORT , 25 ms 0 _D DISABLED , Communication watchdog disabled Reset: 10 _B |
| OUT3_4_PAR | 5 | rw | OUT3-4 parallel mode 1 _D ENABLED , OUT3-4 parallel mode (controlled by IN3 or CTRL.OUT3_ON) 0 _D DISABLED , OUT3, OUT4 controlled separately (default) Reset: 0 _B |
| OUT1_2_PAR | 4 | rw | OUT1-2 parallel mode 1 _D ENABLED , OUT1-2 parallel mode (controlled by IN1 or CTRL.OUT1_ON) 0 _D DISABLED , OUT1, OUT2 controlled separately (default) Reset: 0 _B |
| OUT4_DD | 3 | rw | OUT4 direct drive mode 1 _D ENABLED , OUT4 controlled by IN4 (default) 0 _D DISABLED , OUT4 controlled by SPI (CTRL.OUT4_ON) Reset: 1 _B |
| OUT3_DD | 2 | rw | OUT3 direct drive mode 1 _D ENABLED , OUT3 controlled by IN3 (default) 0 _D DISABLED , OUT3 controlled by SPI (CTRL.OUT3_ON) Reset: 1 _B |
| OUT2_DD | 1 | rw | OUT2 direct drive mode 1 _D ENABLED , OUT2 controlled by IN2 (default) 0 _D DISABLED , OUT2 controlled by SPI (CTRL.OUT2_ON) Reset: 1 _B |
| OUT1_DD | 0 | rw | OUT1 direct drive mode 1 _D ENABLED , OUT1 controlled by IN1 (default) 0 _D DISABLED , OUT1 controlled by SPI (CTRL.OUT1_ON) Reset: 1 _B |

16 bit SPI interface

Off-state diagnostic configuration register

| OFF_DIAG_CFG | Offset | Reset Value |
|---|-----------------|-----------------|
| Off-state diagnostic configuration register | 02 _H | 1F _H |

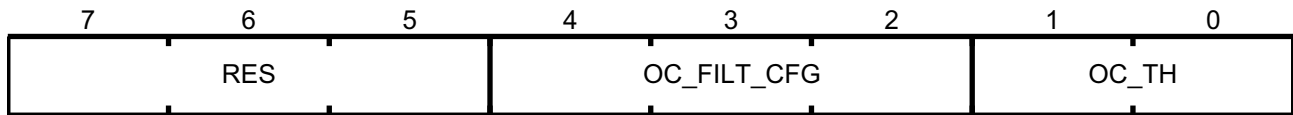


| Field | Bits | Type | Description |
|------------------------|------|------|---|
| DIAG_FILTER_CFG | 5:4 | rw | Diagnostic filter time configuration 3 _D 2000_us , 2000 us 2 _D 1000_us , 1000 us 1 _D 500_us , 500 us (default) 0 _D 200_us , 200 us Reset: 01 _B |
| OUT4_DIAG_EN | 3 | rw | Enable diagnostic current OUT4 1 _D ON , Diagnostic current ON (default) 0 _D OFF , Diagnostic current OFF Reset: 1 _B |
| OUT3_DIAG_EN | 2 | rw | Enable diagnostic current OUT3 1 _D ON , Diagnostic current ON (default) 0 _D OFF , Diagnostic current OFF Reset: 1 _B |
| OUT2_DIAG_EN | 1 | rw | Enable diagnostic current OUT2 1 _D ON , Diagnostic current ON (default) 0 _D OFF , Diagnostic current OFF Reset: 1 _B |
| OUT1_DIAG_EN | 0 | rw | Enable diagnostic current OUT1 1 _D ON , Diagnostic current ON (default) 0 _D OFF , Diagnostic current OFF Reset: 1 _B |

16 bit SPI interface

On-state diagnostic configuration register

| ON_DIAG_CFG | Offset | Reset Value |
|--|-----------------|-----------------|
| On-state diagnostic configuration register | 03 _H | 01 _H |

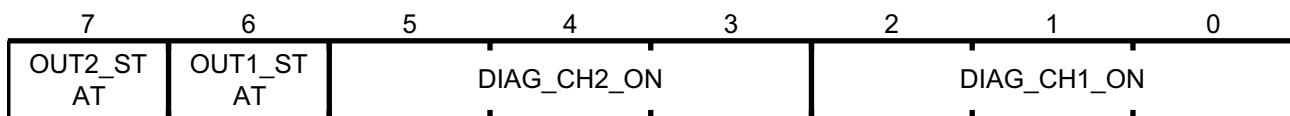


| Field | Bits | Type | Description |
|--------------------|------|------|---|
| OC_FILT_CFG | 4:2 | rw | Overcurrent shut-down delay time (for all channels) 7 _D 30_ms , 30 ms 6 _D 20_ms , 20 ms 5 _D 10_ms , 10 ms 4 _D 5_ms , 5 ms 3 _D 1_ms , 1 ms 2 _D 500_us , 500 us 1 _D 120_us , 120 us 0 _D 60_us , 60 us (default) Reset: 000 _B |
| OC_TH | 1:0 | rw | Overcurrent shut-down threshold (for all channels) (d_oc_th) 3 _D 4000_mA , 4 A 2 _D 3000_mA , 3 A 1 _D 2000_mA , 2 A (default) 0 _D 1000_mA , 1 A Reset: 01 _B |

16 bit SPI interface

On-state diagnostic result register OUT1 & OUT2

| DIAG_OUT_1_2_ON | Offset | Reset Value |
|---|-----------------|-----------------|
| On-state diagnostic result register OUT1 & OUT2 | 04 _H | 00 _H |

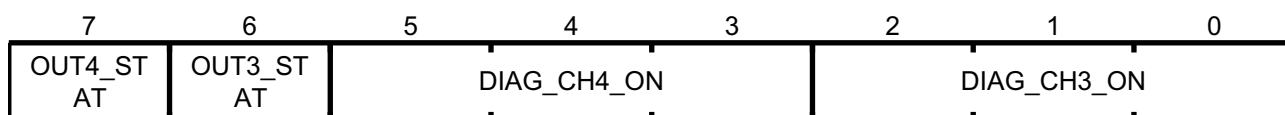


| Field | Bits | Type | Description |
|-------------|------|------|--|
| OUT2_STAT | 7 | r | Channel 2 output status 1 _D ON , Channel is ON 0 _D OFF , Channel is OFF Reset: 0 _B |
| OUT1_STAT | 6 | r | Channel 1 output status 1 _D ON , Channel is ON 0 _D OFF , Channel is OFF Reset: 0 _B |
| DIAG_CH2_ON | 5:3 | rwc | On-state diagnostic result register - Channel 2 7 _D UNUSED , unused combination 6 _D UNUSED , unused combination 5 _D OT , Overtemperature 4 _D OC_TIME , Overcurrent timeout 3 _D OC_OT , Overtemperature during overcurrent 2 _D SCB , Short to battery 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 000 _B |
| DIAG_CH1_ON | 2:0 | rwc | On-state diagnostic result register - Channel 1 7 _D UNUSED , unused combination 6 _D UNUSED , unused combination 5 _D OT , Overtemperature 4 _D OC_TIME , Overcurrent timeout 3 _D OC_OT , Overtemperature during overcurrent 2 _D SCB , Short to battery 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 000 _B |

16 bit SPI interface

On-state diagnostic result register OUT3 & OUT4

| DIAG_OUT_3_4_ON | Offset | Reset Value |
|---|-----------------|-----------------|
| On-state diagnostic result register OUT3 & OUT4 | 05 _H | 00 _H |

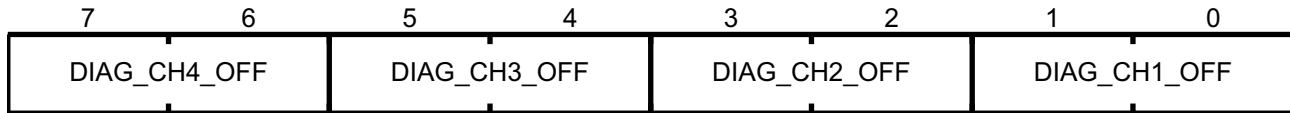


| Field | Bits | Type | Description |
|--------------------|------|------|--|
| OUT4_STAT | 7 | r | Channel 4 output status 1 _D ON , Channel is ON 0 _D OFF , Channel is OFF Reset: 0 _B |
| OUT3_STAT | 6 | r | Channel 3 output status 1 _D ON , Channel is ON 0 _D OFF , Channel is OFF Reset: 0 _B |
| DIAG_CH4_ON | 5:3 | rwc | On-state diagnostic result register - Channel 4 7 _D UNUSED , unused combination 6 _D UNUSED , unused combination 5 _D OT , Overtemperature 4 _D OC_TIME , Overcurrent timeout 3 _D OC_OT , Overtemperature during overcurrent 2 _D SCB , Short to battery 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 000 _B |
| DIAG_CH3_ON | 2:0 | rwc | On-state diagnostic result register - Channel 3 7 _D UNUSED , unused combination 6 _D UNUSED , unused combination 5 _D OT , Overtemperature 4 _D OC_TIME , Overcurrent timeout 3 _D OC_OT , Overtemperature during overcurrent 2 _D SCB , Short to battery 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 000 _B |

16 bit SPI interface

Off-state diagnostic result register

| DIAG_OFF | Offset | Reset Value |
|--------------------------------------|-----------------|-----------------|
| Off-state diagnostic result register | 06 _H | 00 _H |

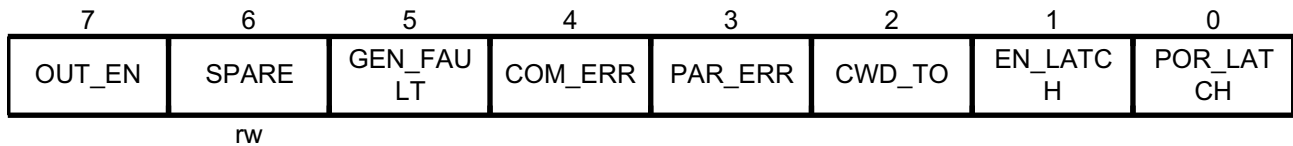


| Field | Bits | Type | Description |
|--------------|------|------|--|
| DIAG_CH4_OFF | 7:6 | rwc | Off-state diagnostic result register Channel 4 3 _D SCG , Short to ground 2 _D OL , Open load 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 00 _B |
| DIAG_CH3_OFF | 5:4 | rwc | Off-state diagnostic result register Channel 3 3 _D SCG , Short to ground 2 _D OL , Open load 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 00 _B |
| DIAG_CH2_OFF | 3:2 | rwc | Off-state diagnostic result register Channel 2 3 _D SCG , Short to ground 2 _D OL , Open load 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 00 _B |
| DIAG_CH1_OFF | 1:0 | rwc | Off-state diagnostic result register Channel 1 3 _D SCG , Short to ground 2 _D OL , Open load 1 _D NO_FAIL , no failure detected 0 _D UNKNOWN , no diagnosis done Reset: 00 _B |

16 bit SPI interface

Global device status register

| GLOBAL_STATUS | Offset | Reset Value |
|-------------------------------|-----------------|--------------------|
| Global device status register | 07 _H | 01 _H |

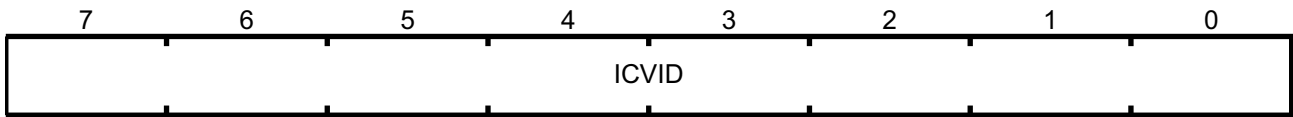


| Field | Bits | Type | Description |
|------------------|-------------|-------------|---|
| OUT_EN | 7 | rw | OUTx enable bit 1 _D ENABLED , Output switching enabled 0 _D DISABLED , Outputs disabled (default) Reset: 0 _B |
| SPARE | 6 | rw | Spare register for future use 1 _D GLOBAL_STATUS_SPARE_EN , 0 _D GLOBAL_STATUS_SPARE_DIS , (default) Reset: 0 _B |
| GEN_FAULT | 5 | rwc | General fault flag 1 _D ERR , At least one fault was detected 0 _D NO_ERR , No fault was detected Reset: 0 _B |
| COM_ERR | 4 | rwc | Communication Error Flag 1 _D ERR , At least one communication failure was detected 0 _D NO_ERR , No communication failure was detected Reset: 0 _B |
| PAR_ERR | 3 | rwc | Parity Error Flag 1 _D ERR , At least one parity error was detected 0 _D NO_ERR , No parity error was detected Reset: 0 _B |
| CWD_TO | 2 | rwc | Communication watchdog timeout 1 _D ERR , Communication watchdog timeout occurred 0 _D NO_ERR , No communication watchdog timeout (default) Reset: 0 _B |
| EN_LATCH | 1 | rwc | EN Latch 1 _D EN , Device was enabled since last read-out 0 _D NO_EN , Device was not enabled since last cleared Reset: 0 _B |
| POR_LATCH | 0 | rwc | Power-on reset latch 1 _D POR , Device was reset since last cleared 0 _D NO_POR , Device was not reset since last cleared Reset: 1 _B |

16 bit SPI interface

IC Version ID

| | | |
|---------------|-----------------|--------------------|
| ICVID | Offset | Reset Value |
| IC Version ID | 08 _H | B1 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| ICVID | 7:0 | r | IC Version ID 177 _D ICVID, Reset: B1 _H |

Package outlines

7 Package outlines

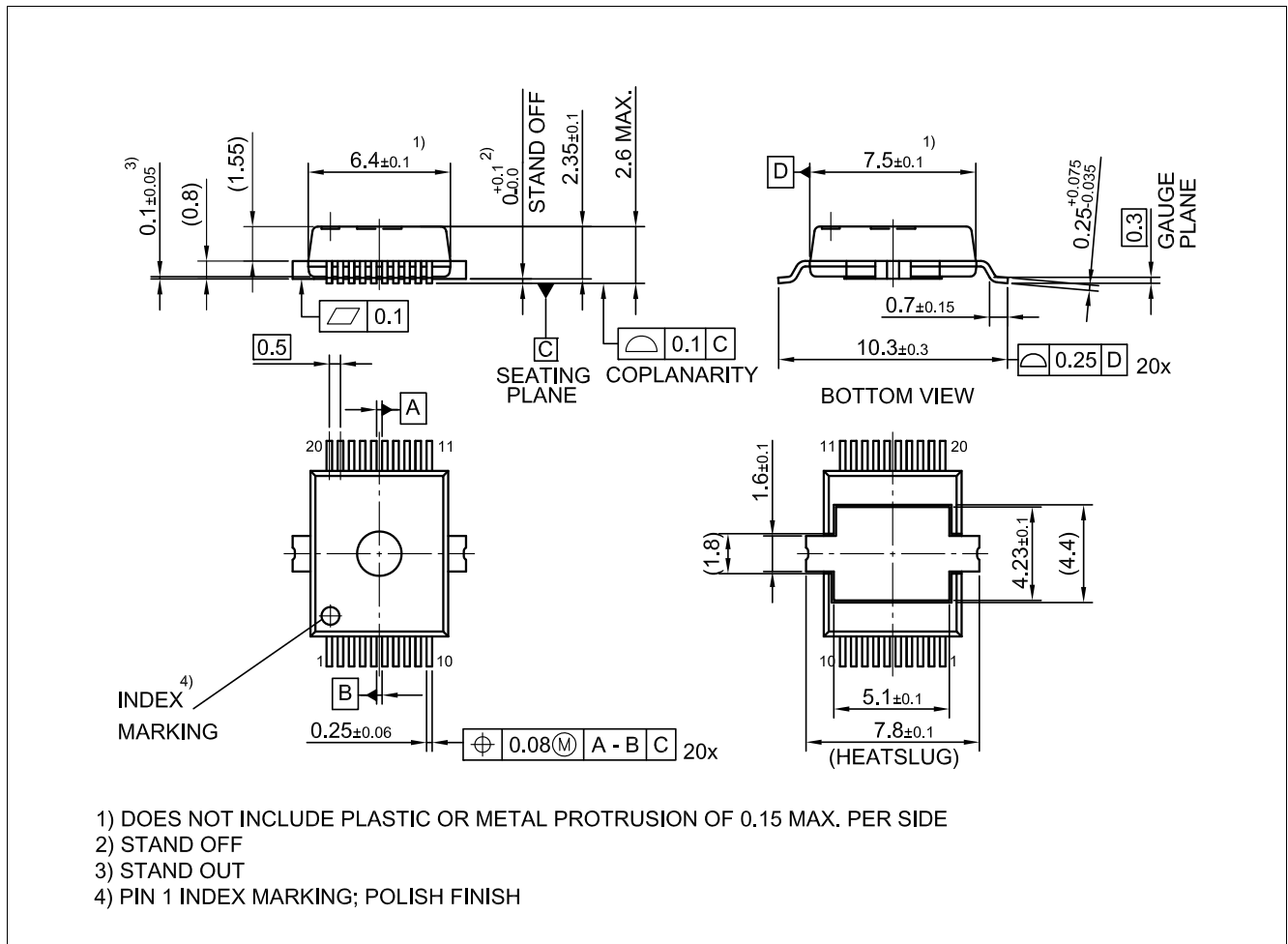


Figure 7-1 PG-DSO-20-88 (Plastic Dual Small Outline Package) Green Product - Package dimensions are preliminary and may be updated

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Floating exposed pad

The exposed pad of TLE9104SH is not connected to the ground internally. It is highly recommended to connect the exposed pad to GND pins externally.

For further information on alternative packages, please visit our website:
<http://www.infineon.com/packages>.

Dimensions in mm

Application information

8 Application information

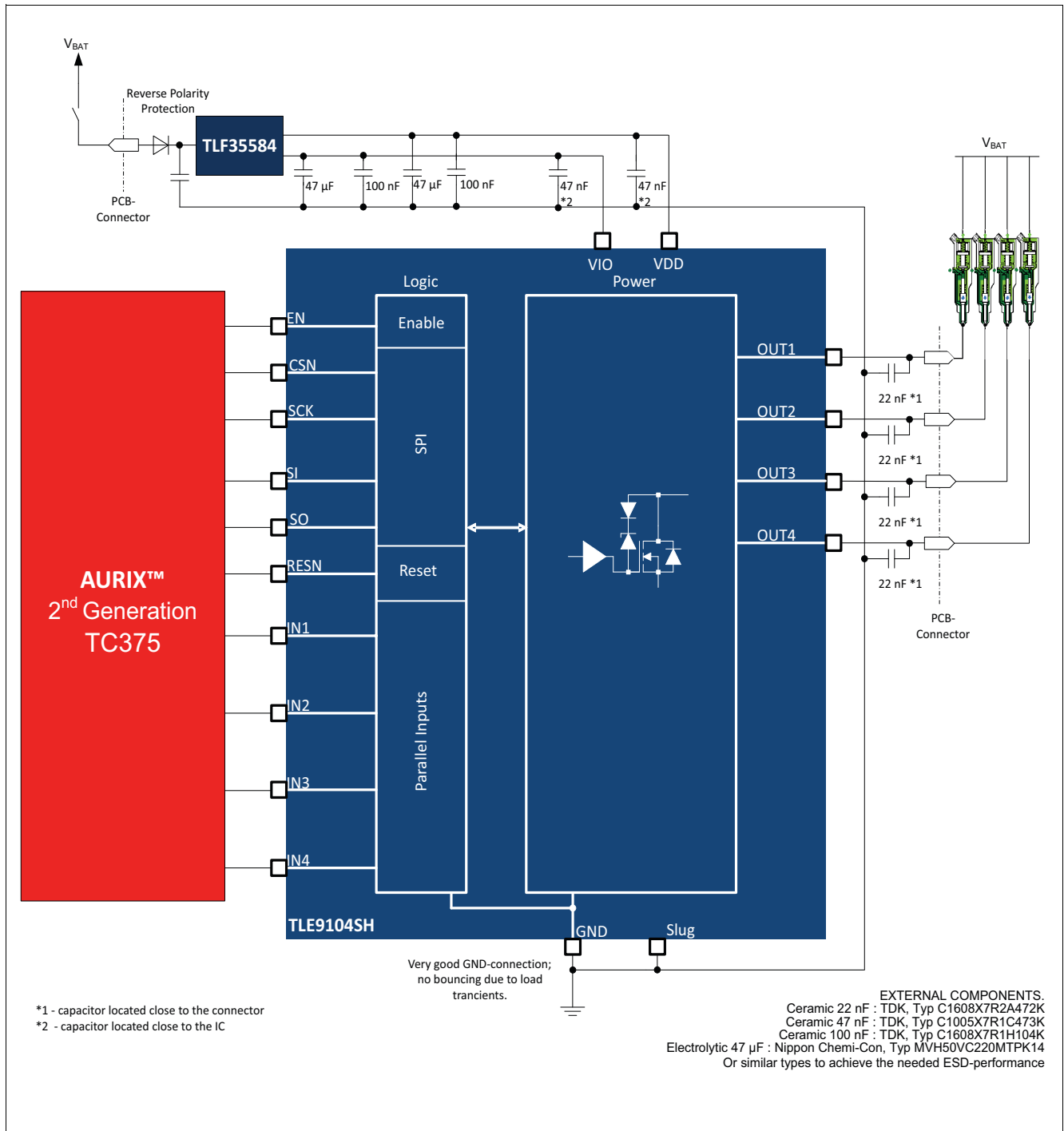


Figure 8-1 Multi port injection application diagram

Revision history

9 Revision history

Table 9-1 Revision history

| Version | Date | Changes |
|----------------|-------------|---|
| Rev. 1.2 | 2018-10-26 | Changed H level output voltage of SO Pin symbol and minimum value changed |
| Rev. 1.1 | 2018-02-15 | OC filter times updates in SPI table |
| Rev. 1.0 | 2018-02-01 | First datasheet release |

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-10-26

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2018 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

Z8F56123922

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.