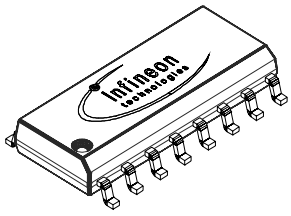
LIN-Transceiver LDO TLE 6286

Target Data Sheet



P-DSO-16-4

1 Overview

1.1 Features

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification
- Compatible to ISO 9141 functions
- Very low current consumption in sleep mode
- Control output for voltage regulator
- Short circuit proof to ground and battery
- Overtemperature protection
- Output voltage tolerance $\leq \pm 2$ %
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics

Type	Ordering Code	Package
TLE 6286 G	on request	P-DSO-16-4

1.2 Description

The TLE 6286 is a single-wire transceiver with a LDO. It is chip by chip integrated circuit in a P-DSO-16-4 package. It works as an interface between the protocol controller and the physical bus. The TLE 6286 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

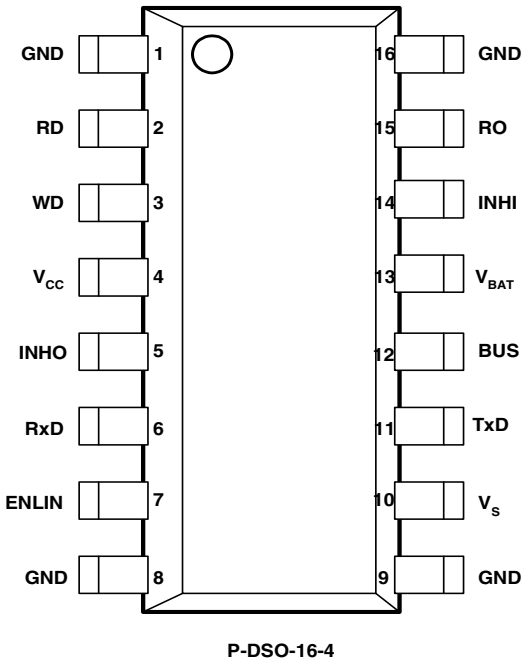
In order to reduce the current consumption the TLE 6286 offers a sleep operation mode. In this mode a voltage regulator can be controlled in order to minimize the current consumption of the whole application. The on-chip voltage regulator is designed for this

application but it is also possible to use an external voltage regulator. A wake-up caused by a message on the bus enables the voltage regulator and sets the RxD output low until the device is switched to normal operation mode.

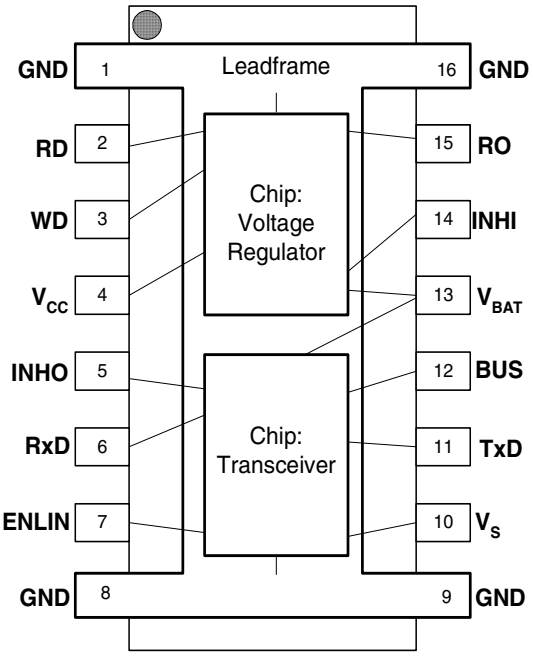
The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE 6286 is designed to withstand the severe conditions of automotive applications.

1.3 Pin Configuration (top view)



P-DSO-16-4



P-DSO-16-4

Figure 1 Pinout

1.4 Pin Definitions and Functions:

Pin No.	Symbol	Function
1,8,9,16	GND	**Ground;** place to cooling tabs to improve thermal behavior
2	RD	**Reset delay;** connected to ground with capacitor
3	WD	**Window Watchdog;** rising-edge triggered, for monitoring a microcontroller
4	V_{CC}	**5V Output;** connected to GND with 22µF capacitor, ESC<3Ω
5	INHO	**Inhibit LIN Output;** to control a voltage regulator
6	RxD	**Receive Data Output;** internal 30kΩ pull up to Vs, LOW in dominat state
7	ENLIN	**Enable LIN Input;** integrated 30kΩ pull down, transceiver in normal operation mode when HIGH
10	V_S	**5V Supply Input;** V_{CC} input to supply the LIN transceiver
11	TxD	**Transmit Data Input;** internal 30kΩ pull up to Vs, LOW in dominant state
12	BUS	**LIN BUS Output/Input;** internal 30kΩ pull up to Vs, LOW in dominant state
13	V_{BAT}	**Battery Supply Input;** a reverse current protection diode is required, block GND with 100nF ceramic capacitor and 22µF capacitor
14	INHI	**Inhibit Voltage Regulator Input;** TTL compatible, low active input
15	RO	**Reset Output;** open collector output connected to the output via a resistor of 30kΩ

1.5 Functional Block Diagram

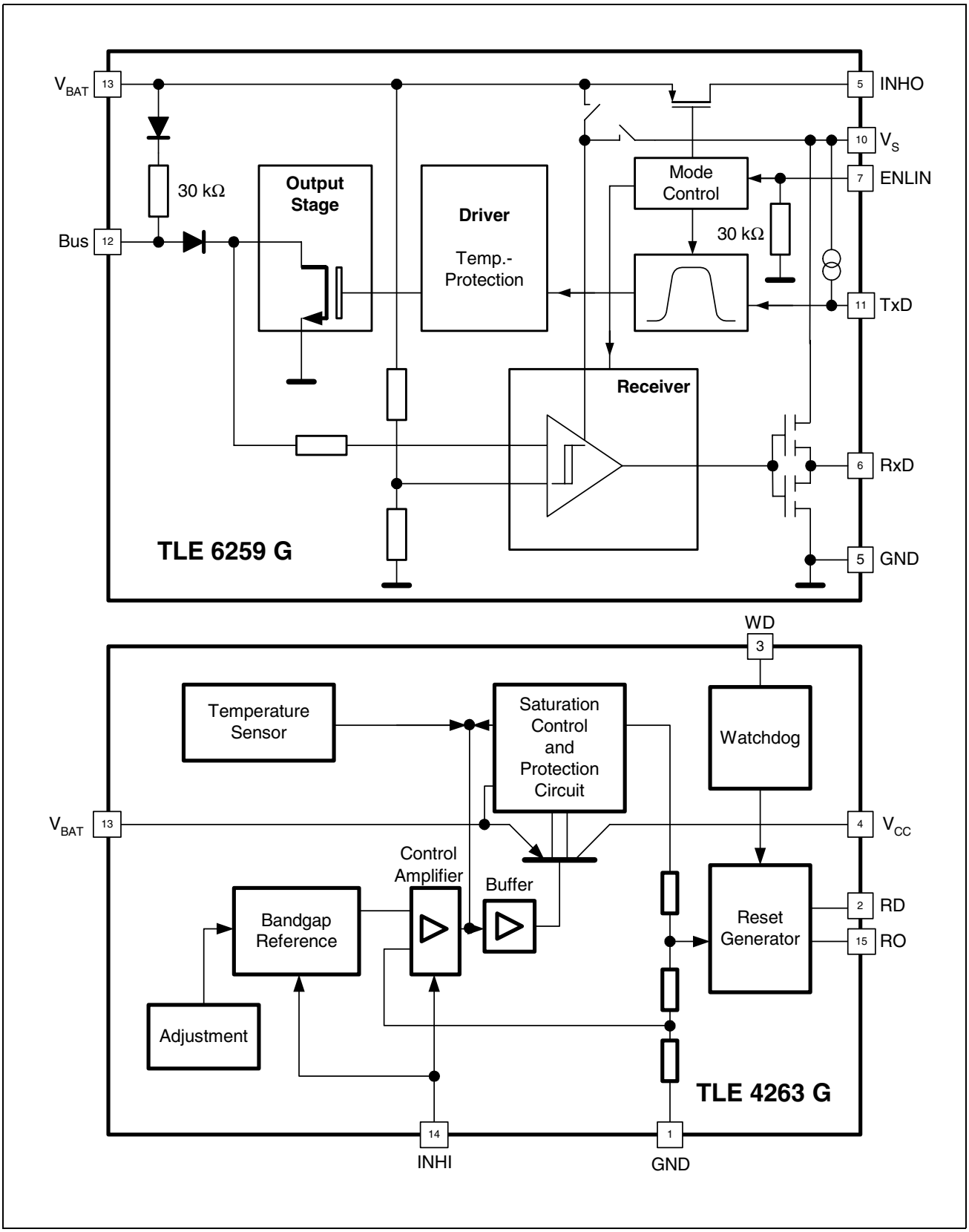


Figure 2 Block Diagram

2 Circuit Description

The TLE 6286 is a single-wire transceiver combined with a LDO. It is a chip by chip integrated circuit in a P-DSO-16-4 package. It works as an interface between the protocol controller and the physical bus. The TLE 6286 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems. The on-chip voltage regulator with watchdog is designed for sleep mode applications but it is also possible to use an external voltage regulator.

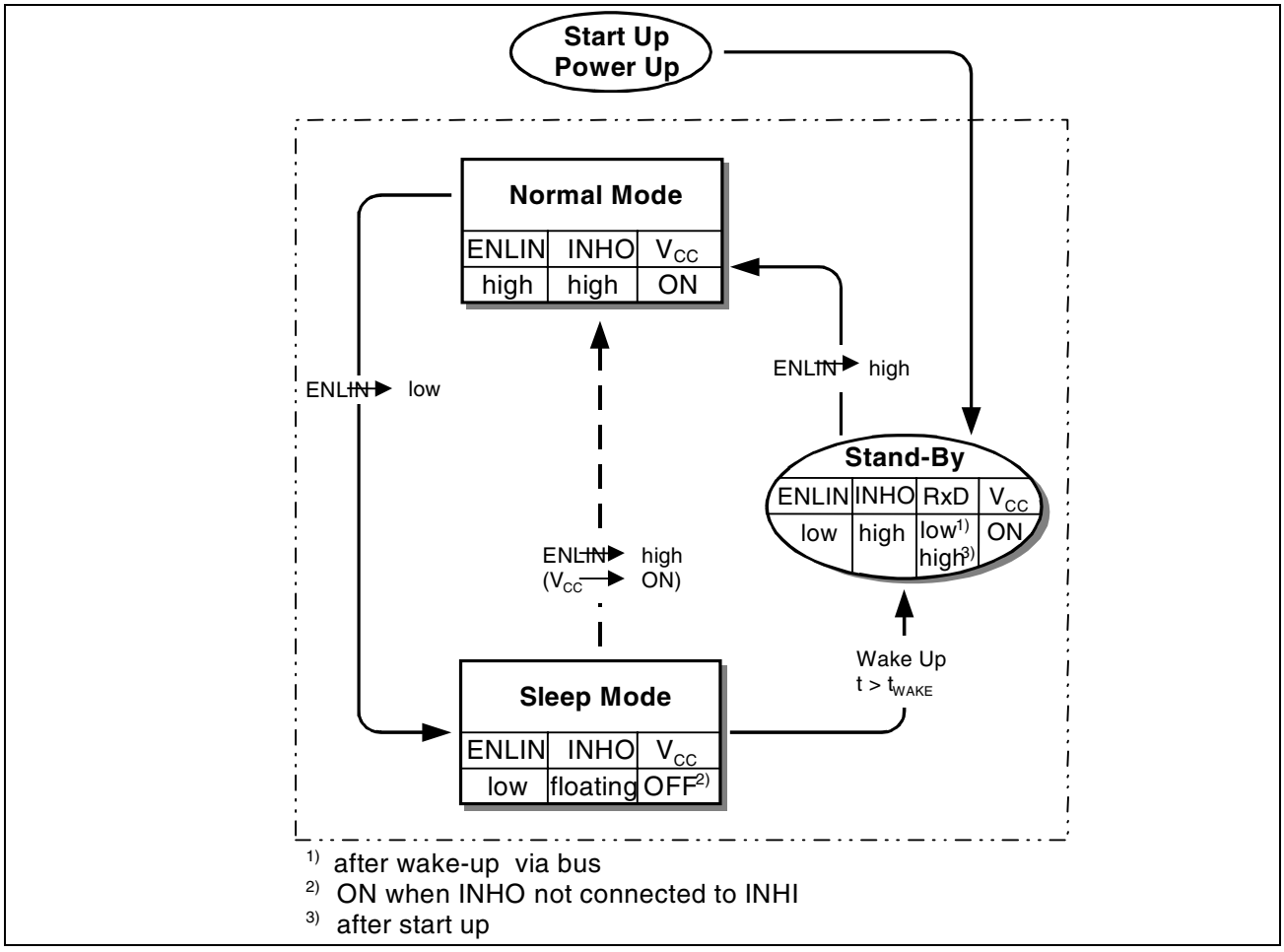


Figure 3 Operation Mode State Diagram

2.1 Operation Modes

In order to reduce the current consumption the TLE 6286 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see **figure 3**, state diagram). In the sleep mode a voltage regulator can be controlled via the INH output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INH output high. In parallel the wake-up is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE6286 can be set in normal operation mode without a wake-up via the communication bus.

2.2 LIN Transceiver

The LIN Transceiver has already a pull up resistor of 30kΩ as termination implemented. There is also a diode in this path, to protect the circuit from feedback of voltages from the bus line to the power supply. To configure the TLE 6286 as a master node, an additional external termination resistor of 1kΩ is required. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is also recommended to place a diode in series to the external pull up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1nF in the master node (see figure 6, application circuit).

An capacitor of 10µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

2.3 Voltage Regulator

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold V_{DRL}, a reset signal occurs at the reset output and is held until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typ. 4.65 V. A connected microcontroller will be monitored through the watchdog logic. In case of missing pulses at pin W, the reset output is set to low. The pulse sequence time can be set in a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against overload, overtemperature, reverse polarity

2.4 Input Capacitor

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

2.5 Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$C_D = (t_{rd} \times I_{D,ch})/\Delta V$

Definitions:C_D = delay capacitor

t_{rd} = reset delay time

$I_{D,ch}$ = charge current, typical 60 µA

$\Delta V = V_{DU}$, typical 1.70 V

V_{DU} = upper delay switching threshold at C_D for reset delay time

2.6 Watchdog Timing

The frequency of the watchdog pulses has to be higher than the minimum pulse sequence which is set by the external reset delay capacitor C_D. Calculation can be done according to the formulas given in **Figure 5**.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	
Battery supply voltage	V_S	-0.3	40	V	
Bus input voltage	V_{bus}	-20	32	V	
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INH	V_{INH}	-0.3	V_S + 0.3	V	
Output current at INH	I_{INH}		1	mA	
Reset output voltage	V_R	– 0.3	42	V	–
Reset delay voltage	V_D	– 0.3	42	V	
Output voltage Vcc	V_Q	– 0.3	7	V	–
INHIBIT voltage	V_{INH}	– 42	45	V	–
Watchdog voltage	V_W	– 0.3	6	V	–
Electrostatic discharge voltage at Vs, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	5.5	V	
Battery Supply Voltage	V_S	6	20	V	
Junction temperature	T_j	– 40	150	°C	–

Thermal Shutdown (junction temperature)

Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K

Thermal Resistances

Junction ambient	$R_{thj\text{-}a}$	–	115	K/W	–

3.3 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Current Consumption						
Current consumption	I_{CC}		0.5	1.5	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_S		0.5	1.0	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_{CC}		0.7	2.0	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		0.7	1.5	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		20	30	µA	sleep mode; T_j = 25 °C
Current consumption	I_S		20	40	µA	sleep mode
Receiver Output R×D						
HIGH level output current	$I_{RD,H}$		-0.7	-0.4	mA	V_{RD} = 0.8 x V_{CC},
LOW level output current	$I_{RD,L}$	0.4	0.7		mA	V_{RD} = 0.2 x V_{CC},
Bus receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 x V_S	0.48 x V_S		V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$		0.52 x V_S	0.56 x V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 x V_S	0.04 x V_S	0.06 x V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
wake-up threshold voltage	V_{wake}	0.40 x V_S	0.55 x V_S	0.70 x V_S	V	
Transmission Input T×D						
HIGH level input voltage threshold	$V_{TD,H}$		2.9	0.7 x V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	600		mV	

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
LOW level input voltage threshold	$V_{TD,L}$	0.3 x V_{CC}	2.1		V	dominant state
TxD pull up current	I_{TD}	-150	-110	-80	µA	V_{TxD} < 0.3 Vcc
Bus transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 x V_S		V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0		1.5	V	V_{TxD} = 0 V;
Bus short circuit current	$I_{bus,sc}$	40	85	125	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-350	-100		µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V, T_j < 85 °C
			5	20	µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = 20 V, T_j < 85 °C
Bus pull up resistance	R_{bus}	20	30	47	kΩ	
Enable input (pin ENLIN)						
HIGH level input voltage threshold	$V_{EN,on}$		2.8	0.7 x V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 x V_{CC}	2.2		V	low power mode
EN input hysteresis	$V_{EN,hys}$	300	600		mV	
EN pull down resistance	R_{EN}	15	30	60	kΩ	
Inhibit output (pin INHO)						
HIGH level drop voltage $\Delta V_{INH} = V_S - V_{INH}$	ΔV_{INH}		0.5	1.0	V	I_{INH} = - 0.15 mA
Leakage current	$I_{INH,lk}$	- 5.0		5.0	µA	sleep mode; V_{INHO} = 0 V

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Vcc Output (pin Vcc)						
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
Output voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100 °C
Output current	I_Q	200	250	–	mA	1)
Current consumption; $I_q = I_I - I_Q$	I_q	–	0	50	µA	V_{INH} = 0
	I_q	–	900	1300	µA	I_Q = 0 mA
	I_q	–	10	18	mA	I_Q = 150 mA
	I_q	–	15	23	mA	I_Q = 150 mA; V_I = 4.5 V
Drop voltage	V_{dr}	–	0.35	0.50	V	I_Q = 150 mA[1)]
Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	I_Q = 5 mA to 150 mA
Line regulation	$\Delta V_{Q.li}$	–	3	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
Power Supply Ripple Rejection	PSRR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{PP}
Reset Genarator (pin RD)						
Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	
Reset adjust threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	V_Q > 3.5 V
Reset low voltage	$V_{RO,l}$	–	0.10	0.40	V	I_{RO} = 1 mA
Saturation voltage	$V_{D,sat}$	–	50	100	mV	V_Q < $V_{R,th}$
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.55	V	–
Charge current	$I_{D,ch}$	40	60	85	µA	–
Reset delay time	t_{rd}	1.3	2.8	4.1	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	4	µs	C_D = 100 nF

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Watchdog (pin WD)						
Discharge current	$I_{D,wd}$	4.40	6.25	9.10	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower timing threshold	V_{DWL}	0.20	0.35	0.55	V	–
Watchdog trigger time	$T_{WI,tr}$	16	22.5	27	ms	C_D = 100 nF
Inhibit Input (INHI)						
Switching voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on
Turn-OFF voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off
Input current	I_{INH}	5	10	25	µA	V_{INH} = 5 V

Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$

[1)]Drop voltage = V_i – V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input)

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Dynamic Transceiver Characteristics						
falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	80% > V_{bus} > 20% C_{bus}= 3.3 nF; $T_{ambient}$ < 85 °C; V_{CC} = 5 V; V_S = 13.5 V
rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	20% < V_{bus} < 80% C_{bus}= 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	2	5	10	µs	C_{bus} = 3.3nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 pF
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	2	5	10	µs	C_{bus} = 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 nF
Propagation delay TxD LOW to bus	$t_{d(L),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$		1	4	µs	V_{CC} = 5V; C_{RxD} = 20pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$		1	4	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2		2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2		2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
Wake-up delay time	t_{wake}	30	100	200	µs	

4 Diagrams

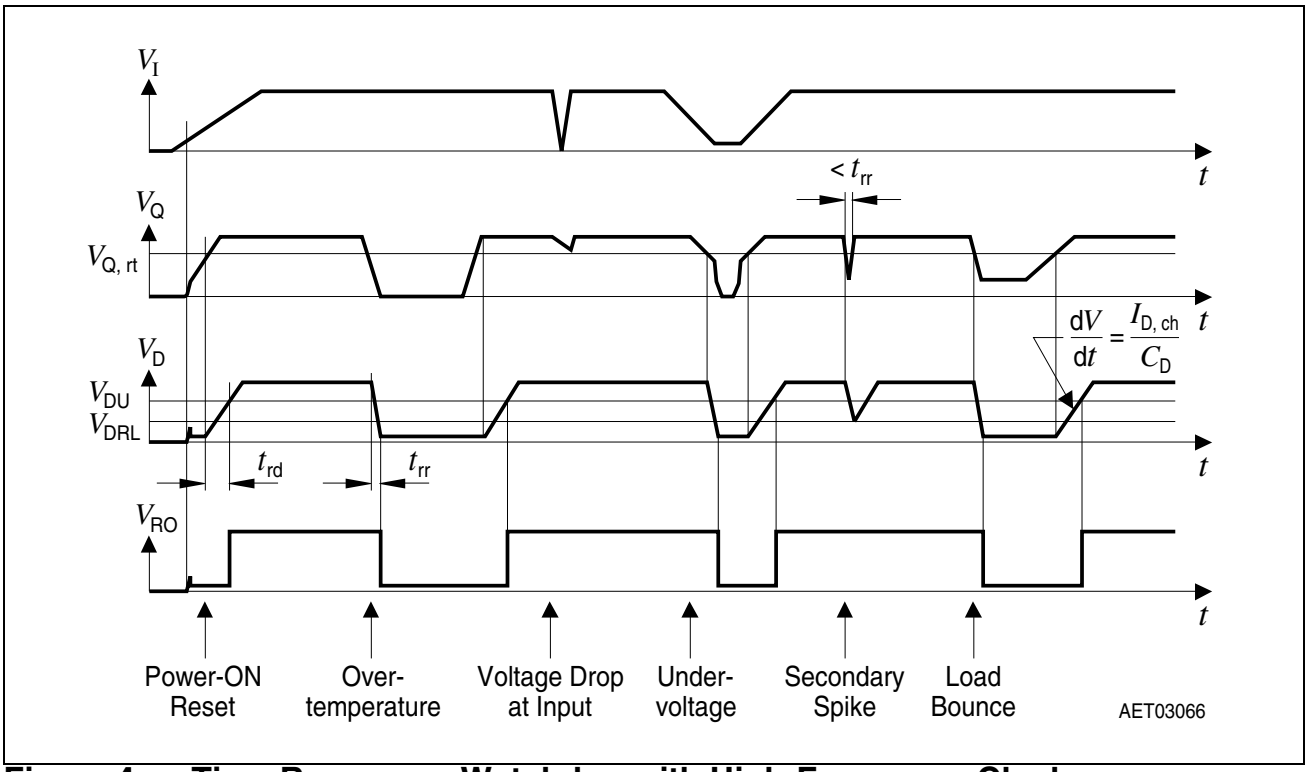


Figure 4 Time Response, Watchdog with High-Frequency Clock

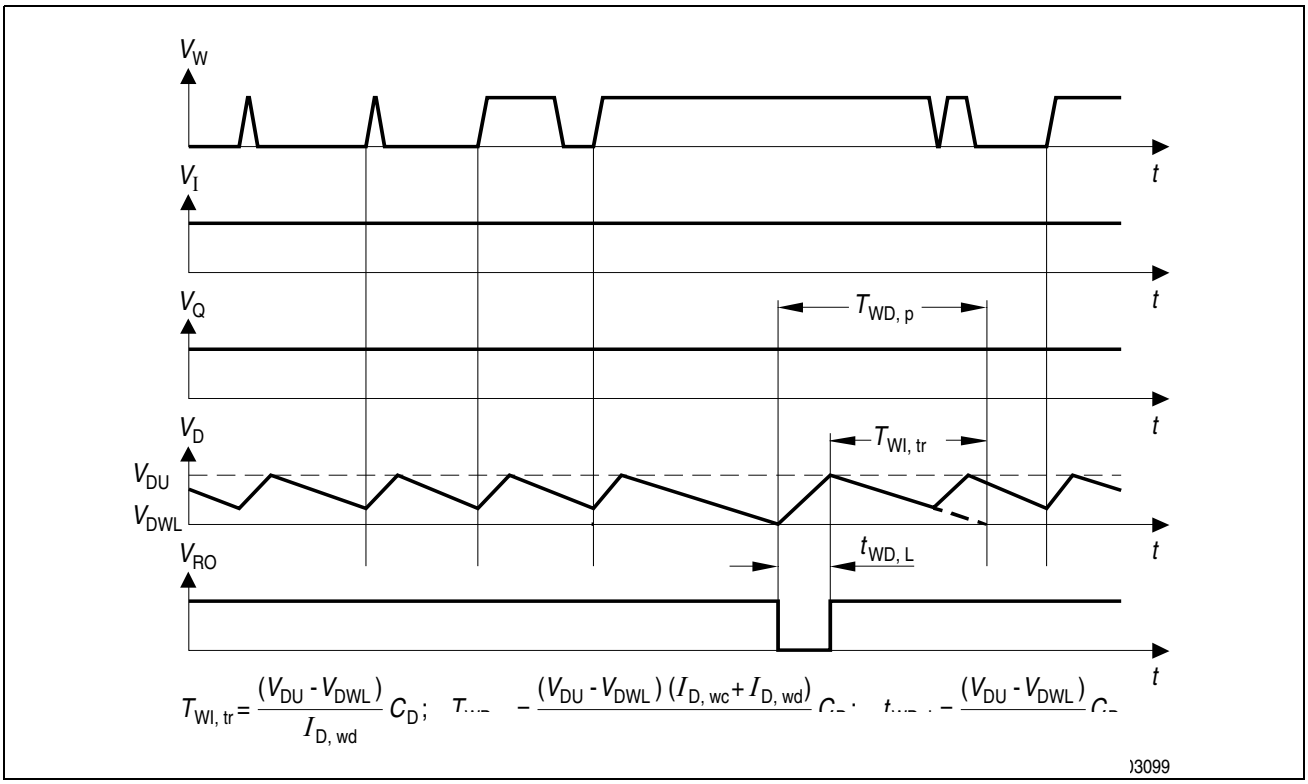


Figure 5 Timing of the Watchdog FunctionReset

5 Application

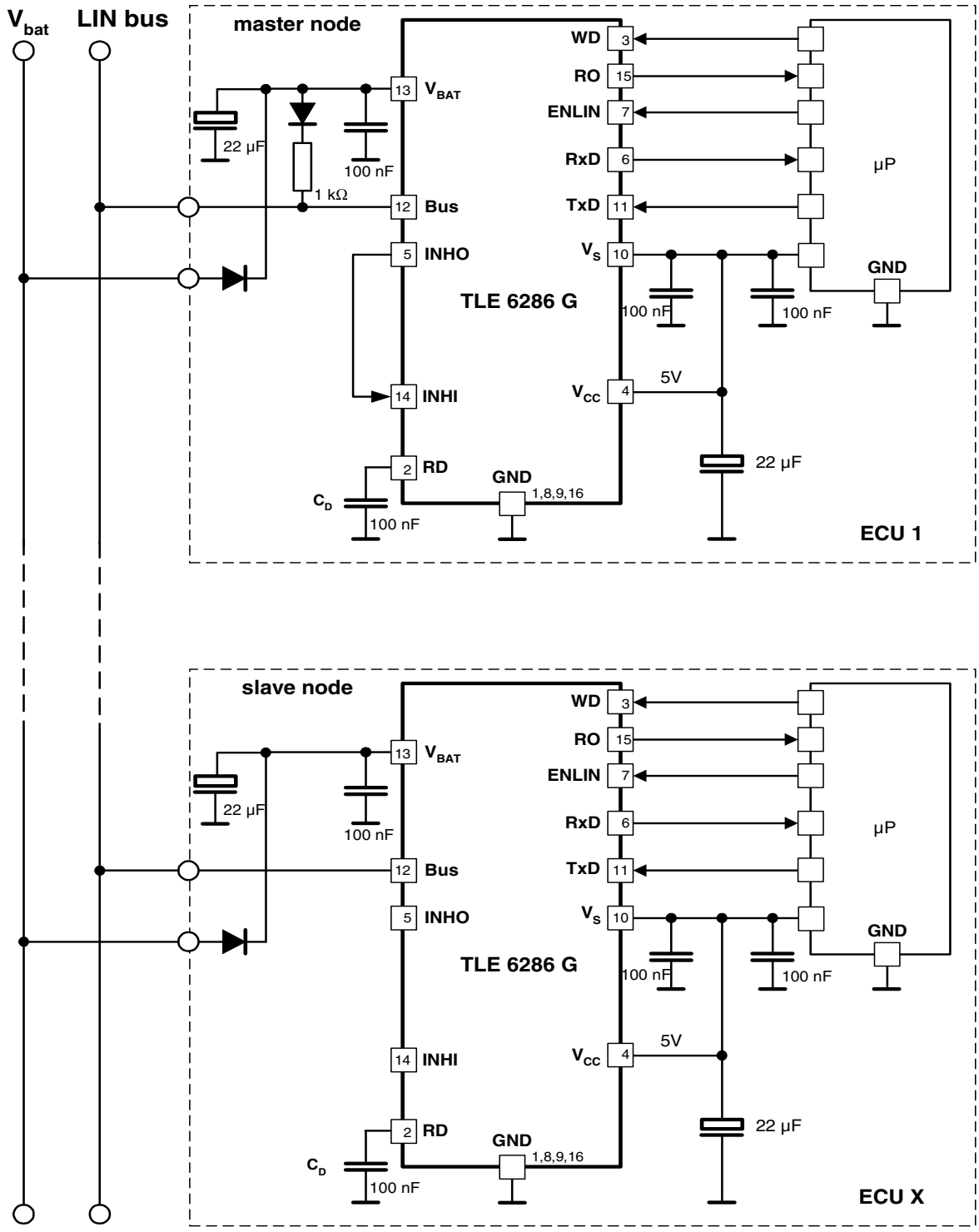


Figure 6 Application Circuit

6 Package Outlines

P-DSO-16-4
(Plastic Dual Small Outline Package)

Pictures of the housing will be added in near future!

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 1999-10-12

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D-81541 München

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