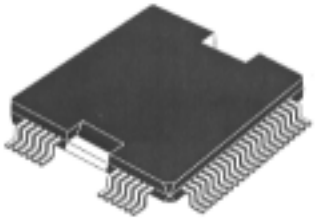
# 18 Channel Smart Lowside Switch

**ASSP for Powertrain**

**Final Data Sheet**

## Features

- **Short Circuit Protection**
- **Overtemperature Protection**
- **Overvoltage Protection**
- **16 bit Serial Data Input and Diagnostic Output (2 bit/chan. acc. SPI Protocol)**
- **Direct Parallel Control of 16 channels for PWM Applications**
- **Low Quiescent Current**
- **Compatible with 3.3V Microcontrollers**
- **Electrostatic discharge (ESD) Protection**

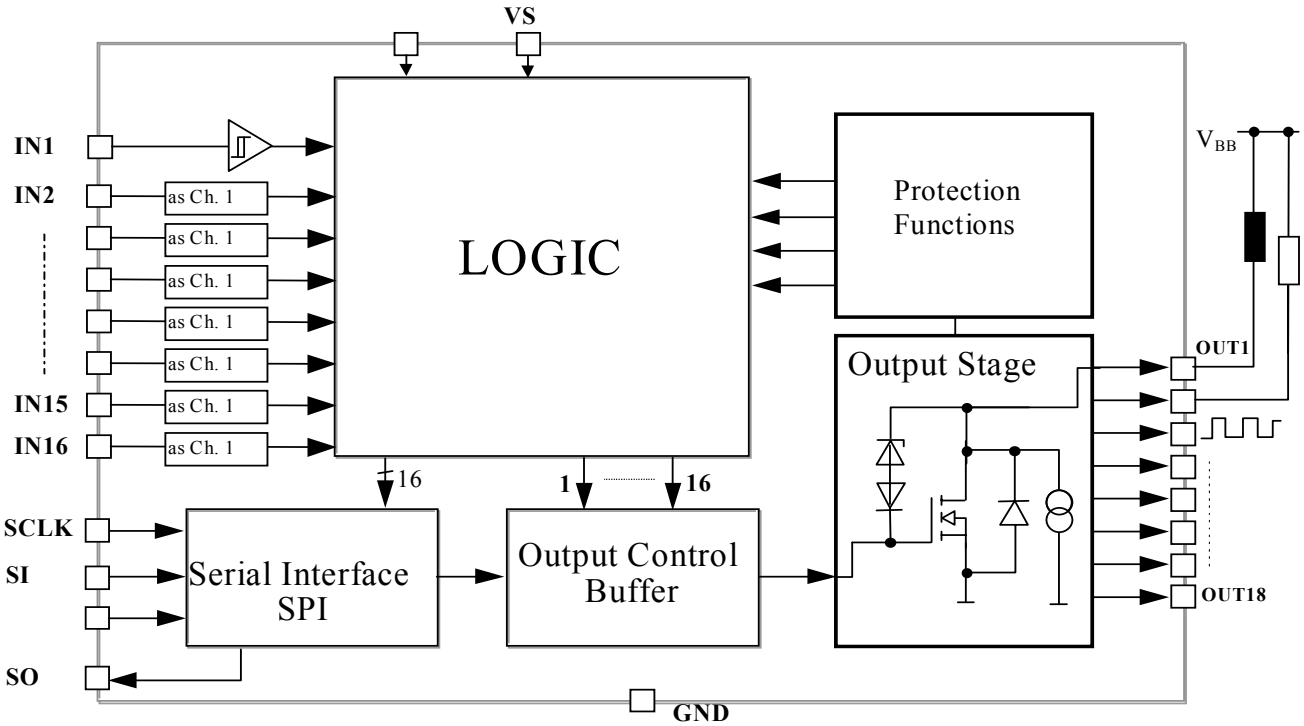


**P-MQFM 64-10**

Ordering Code: Q67007-A9613

## General description

18-fold Low-Side Switch (0.35 Ω to 1 Ω) in Smart Power Technology (SPT) with a Serial Peripheral Interface (SPI) and 18 open drain DMOS output stages. The TLE6244X is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via SPI Interface. Additionally 16 of the 18 channels can be controlled direct in parallel for PWM applications. Therefore the TLE6244X is particularly suitable for engine management and powertrain systems.



# 1. Description

## 1.1 Short Description

This circuit is available in MQFP64 package or as chip.

### 1.1.1 Features of the Power Stages

| | Nominal Current | $R_{on,max}$ at $T_J$ = 25°C | static current limitation enabled by SPI | Clamping |
|---|---|---|---|---|
| **OUT1, 2, 5, 6** | 2.2A | 400mΩ | - | 70V |
| **OUT3, OUT4** | 2.2A | 380mΩ | - | 70V |
| **OUT7, OUT8** | 1.1A | 780mΩ | - | 45V |
| **OUT9, OUT10** | 2.2A | 380mΩ | X | 45V |
| **OUT11...OUT14** | 2.2A | 380mΩ | - | 45V |
| **OUT15, OUT16** | 3.0A | 280mΩ | X | 45V |
| **OUT17, OUT18 *)** | 1.1A | 780mΩ | X | 45V |

*) only serial control possible (via SPI)

Parallel connection of power stages is possible (see 1.13)
Internal short-circuit protection
Phase relation: non-inverting (exception: IN8->OUT8 is inverting)

### 1.1.2 Diagnostic Features

The following types of error can be detected:
- Short-circuit to $U_{Batt}$ (SCB)
- Short-circuit to ground (SCG)
- Open load (OL)
- Overtemperature (OT)

Individual detection for each output.
Serial transmission of the error code via SPI.

### 1.1.3 VDD-Monitoring

Low signal at pin $\overline{\text{ABE}}$ and shut-off of the power stages if VDD is out of the permitted range.
Exception: If OUT8 is controlled by IN8, OUT8 will only be switched off by the overvoltage detection and not by undervoltage detection.
The state of VDD can be read out via SPI.

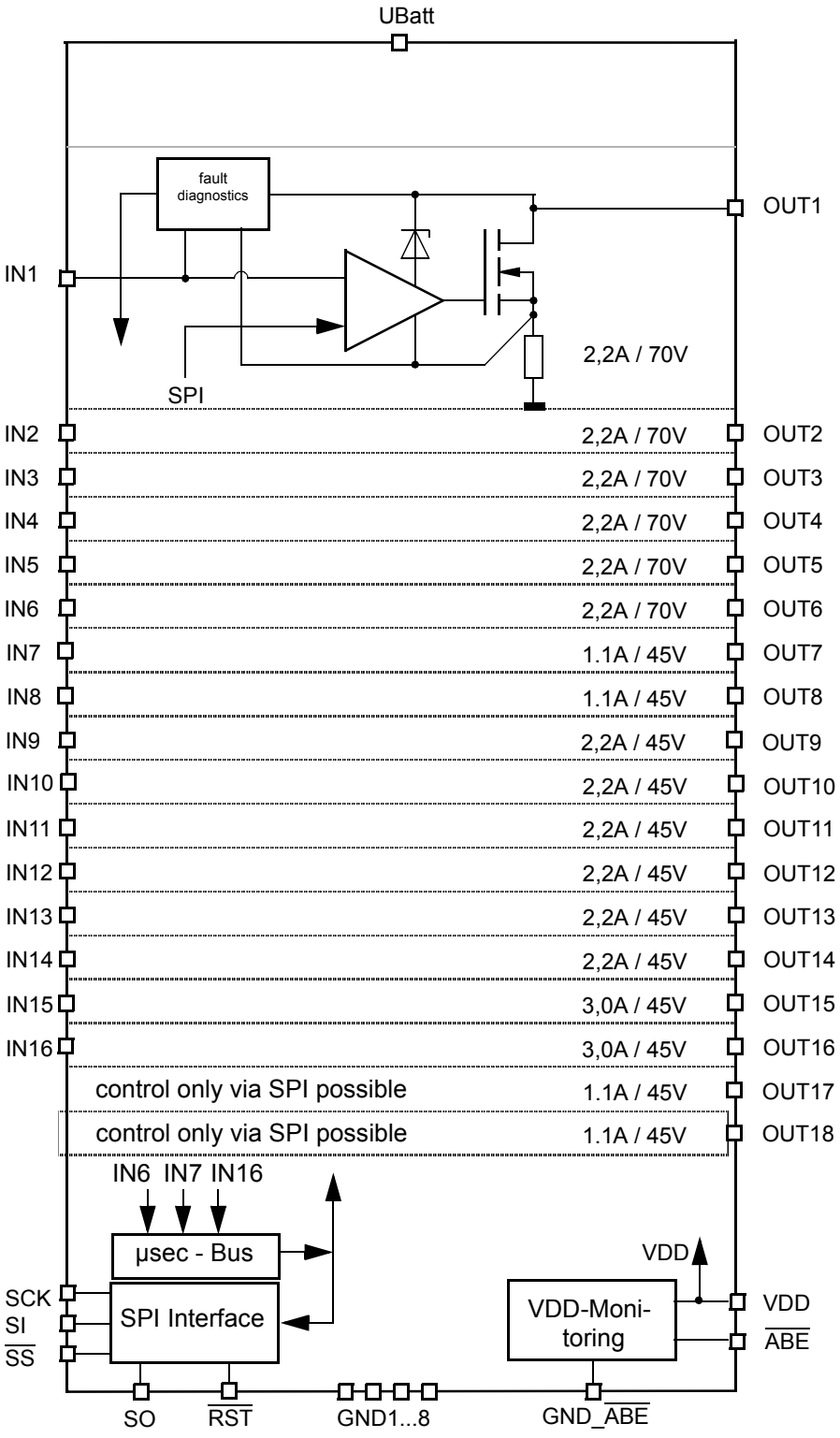
### 1.1.4 µsec-bus

Alternatively to the parallel and SPI control of the power stages, a high speed serial bus interface can be configured as control of the power stages OUT1...OUT7 and OUT9...OUT16.

### 1.1.5 Power Stage OUT8

OUT8 can be controlled by SPI or by the pin IN8 only. When controlled by IN8 this power stage is functional if the voltage at the pin VDD is above 3,5V. OUT8 will not be reset by RST. In SPI mode the power stage is fully supervised by the VDD-monitor.

## 1.2 Block Diagram



## 1.3 Description of the Power Stages

### OUT1... OUT6

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the µsec-bus or via SPI. For $T_J$ = 25°C the on-resistance of the power switches is below 400mΩ.
An integrated zener diode limits the output voltage to 70V typically.

A protection for inverse current is implemented for OUT1... OUT4 for use as stepper-motor control.

### OUT9... OUT14

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the µsec-bus or via SPI. For $T_J$ = 25°C the on-resistance of the power switches is below 380mΩ.
An integrated zener diode limits the output voltage to 45V typically.

### OUT15, OUT16

2 non-inverting low side power switches for nominal currents up to 3.0A. Control is possible by input pins, by the µsec-bus or via SPI. For $T_J$ = 25°C the on-resistance of the power switches is below 280mΩ.
An integrated zener diode limits the output voltage to 45V typically.

### OUT7, OUT8, OUT17, OUT18

4 low side power switches for nominal currents up to 1100mA. Stage 7 is non-inverting, Stage 8 is inverting (IN8 = '1' => OUT8 is active). For the output OUT7 control is possible by the input pin, by the µsec-bus or via SPI, OUT8 is controlled by the input pin IN8 or via SPI, for the outputs OUT17 and OUT18 control is only possible via SPI. For $T_J$ = 25°C the on-resistance of the power switches is below 780mΩ.
An integrated zener diode limits the output voltage to 45V typically.

In order to increase the switching current or to reduce the power dissipation parallel connection of power stages is possible (for additional information see 1.13).
The power stages are short-circuit proof:
Power stages **OUT1...OUT8, OUT11.14**: In case of overload (SCB) they will be turned off after a given delay time. During this delay time the output current is limited by an internal current control loop.
Power stages **OUT9, OUT10, OUT15...OUT18**:
In case of SCB these power stages can be configured for a shut-down mode or for static current limitation. In the shut down mode while SCB they will behave like OUT1..8 or OUT11..14.
In case of static current limitation and SCB the current is limited and the corresponding bit combination is set (early warning) after a given delay time. They will not be turned off. If this condition leads to an overtemperature condition, the output will be set into a low duty cycle PWM (selective thermal shut- down with restart) to prevent critical chip temperature.

There are 3 possibilities to turn the power stages on again:
- turn the power stage off and on, either via serial control (SPI) or via parallel control (input pin, except outputs OUT17 and OUT18) or by the µsec-bus (except OUT8, OUT17,OUT18)
- applying a reset signal.
- sending the instruction "del_dia" by the SPI-interface

The VDD-monitoring locks all power stages, except OUT8 for access by the IN8 input. OUT8 is locked by an internal threshold of 3,5V maximum when controlled by IN8. Otherwise OUT8 is locked by the VDD-monitor.

All low side switches are equipped with fault diagnostic functions:

- short-circuit to $U_{Batt}$: (SCB) can be detected if switches are turned on
- short-circuit to ground: (SCG) can be detected if switches are turned off
- open load: (OL) can be detected if switches are turned off
- overtemperature: (OT) will only be detected if switches are turned on

The fault conditions SCB, SCG, OL and OT will not be stored until an integrated filtering time is expired (please note for PWM application). If, at one output, several errors occur in a sequence, always the last detected error will be stored (with filtering time). All fault conditions are encoded in two bits per switch and are stored in the corresponding SPI registers. Additionally there are two central diagnostic bits: one specially for OT and one for fault occurrence at any output.

The registers can be read out via SPI. After each read out cycle the registers have to be cleared by the DEL_DIA command.

### 1.3.1 Power Stage OUT8 (Condensed Description)

1.3.1.1 Control of OUT8 and VDD-Monitoring

OUT8 can be controlled by SPI or by the pin IN8 only, control by µs-bus is not possible. When controlled by IN8 this power stage is functional if the voltage at the pin VDD is above 3,5V. In SPI mode the power stage is fully supervised by the VDD-monitor.
If OUT8 is controlled by IN8, OUT8 will only be switched off by the overvoltage detection and not by undervoltage detection.

1.3.1.2 Phase Relation IN8 - OUT8

The phase relation IN8 -> OUT8 is inverting.
OUT8 is active if IN8 is set to logic '1' (high level, see 3.4.2 ) in case of parallel access.
On executing the read instruction on RD_INP1/2 the inverted status of IN8 is read back.

1.3.1.3 Reset / Power Stage Diagnostics

If OUT8 is controlled by IN8, OUT8 will not be reseted by RST.
After reset parallel control (by IN8) is active for OUT8.
If UVDD < 4.5V errors are not stored because of the active RST of the external Regulator. Nevertheless
OUT8 is protected against overload.

1.3.1.4 Input Current

The control input IN8 has an internal pull-down current source. Thus the input currents I IN8 are positive (flow into the pin).

1.3.1.5 On Resistance

For OUT8 and 3.5V < UVDD < 4.5V R on increases (see 3.8.5).

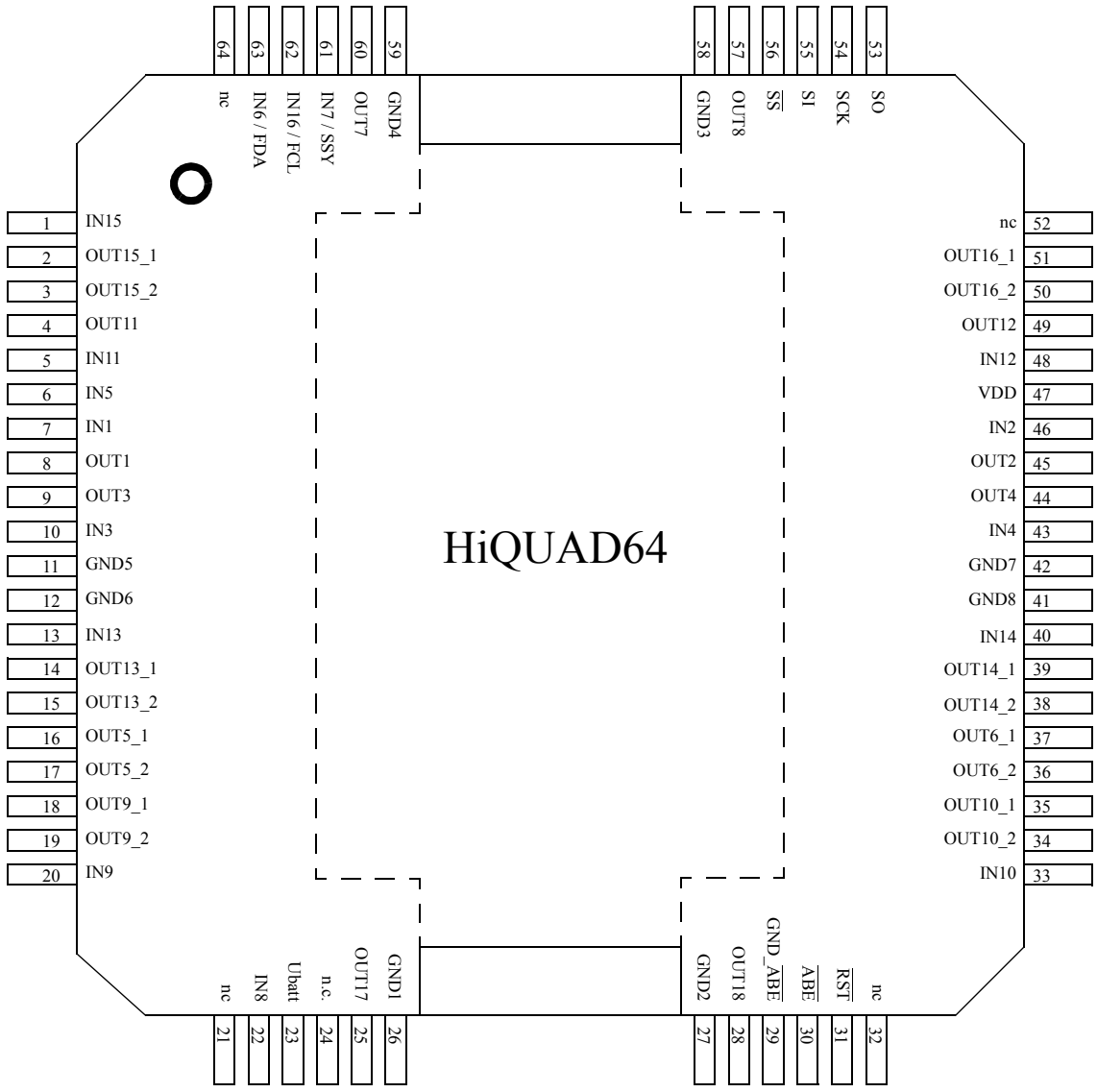
1.3.1.6 Parallel Connection of Power Stages

Parallel connection of power stages with OUT8 and parallel control is prohibited (inverting input IN8). Control via SPI is possible. See 1.13.

## 1.4 Pinout

| Function | Pin | Pin Number |
|---|---|---|
| Input 1 | IN1 | 7 |
| Input 2 | IN2 | 46 |
| Input 3 | IN3 | 10 |
| Input 4 | IN4 | 43 |
| Input 5 | IN5 | 6 |
| Input 6 or FDA | IN6 | 63 |
| Input 7 or SSY | IN7 | 61 |
| Input 8 | IN8 | 22 |
| Input 9 | IN9 | 20 |
| Input 10 | IN10 | 33 |
| Input 11 | IN11 | 5 |
| Input 12 | IN12 | 48 |
| Input 13 | IN13 | 13 |
| Input 14 | IN14 | 40 |
| Input 15 | IN15 | 1 |
| Input 16 or FCL | IN16 | 62 |
| | | |
| Output 1 | OUT1 | 8 |
| Output 2 | OUT2 | 45 |
| Output 3 | OUT3 | 9 |
| Output 4 | OUT4 | 44 |
| Output 5_1 | OUT5_1 | 16 |
| Output 5_2 | OUT5_2 | 17 |
| Output 6_1 | OUT6_1 | 37 |
| Output 6_2 | OUT6_2 | 36 |
| Output 7 | OUT7 | 60 |
| Output 8 | OUT8 | 57 |
| Output 9_1 | OUT9_1 | 18 |
| Output 9_2 | OUT9_2 | 19 |
| Output 10_1 | OUT10_1 | 35 |
| Output 10_2 | OUT10_2 | 34 |
| Output 11 | OUT11 | 4 |
| Output 12 | OUT12 | 49 |
| Output 13_1 | OUT13_1 | 14 |
| Output 13_2 | OUT13_2 | 15 |
| Output 14_1 | OUT14_1 | 39 |
| Output 14_2 | OUT14_2 | 38 |
| Output 15_1 | OUT15_1 | 2 |
| Output 15_2 | OUT15_2 | 3 |
| Output 16_1 | OUT16_1 | 51 |
| Output 16_2 | OUT16_2 | 50 |
| Output 17 | OUT17 | 25 |
| Output 18 | OUT18 | 28 |
| **(Note: OUTxy_1 and OUTxy_2 have to be connected externally!)** | | |
| | | |
| Slave Select | $\overline{SS}$ | 56 |
| Serial Output | SO | 53 |
| Serial Input | SI | 55 |
| SPI Clock | SCK | 54 |

| | | |
|---|---|---|
| Supply Voltage VDD | VDD | 47 |
| Supply Voltage $U_{Batt}$ | Ubatt | 23 |
| | | |
| GND1 | GND1 | 26 |
| GND2 | GND2 | 27 |
| GND3 | GND3 | 58 |
| GND4 | GND4 | 59 |
| GND5 | GND5 | 11 |
| GND6 | GND6 | 12 |
| GND7 | GND7 | 42 |
| GND8 | GND8 | 41 |
| | | |
| Sense Ground VDD-Monitoring | $\overline{GND\_ABE}$ | 29 |
| In-/Output VDD-Monitoring | $\overline{ABE}$ | 30 |
| Reset (low active) | $\overline{RST}$ | 31 |
| | | |
| not connected | nc | 21, 24, 32, 52, 64 |



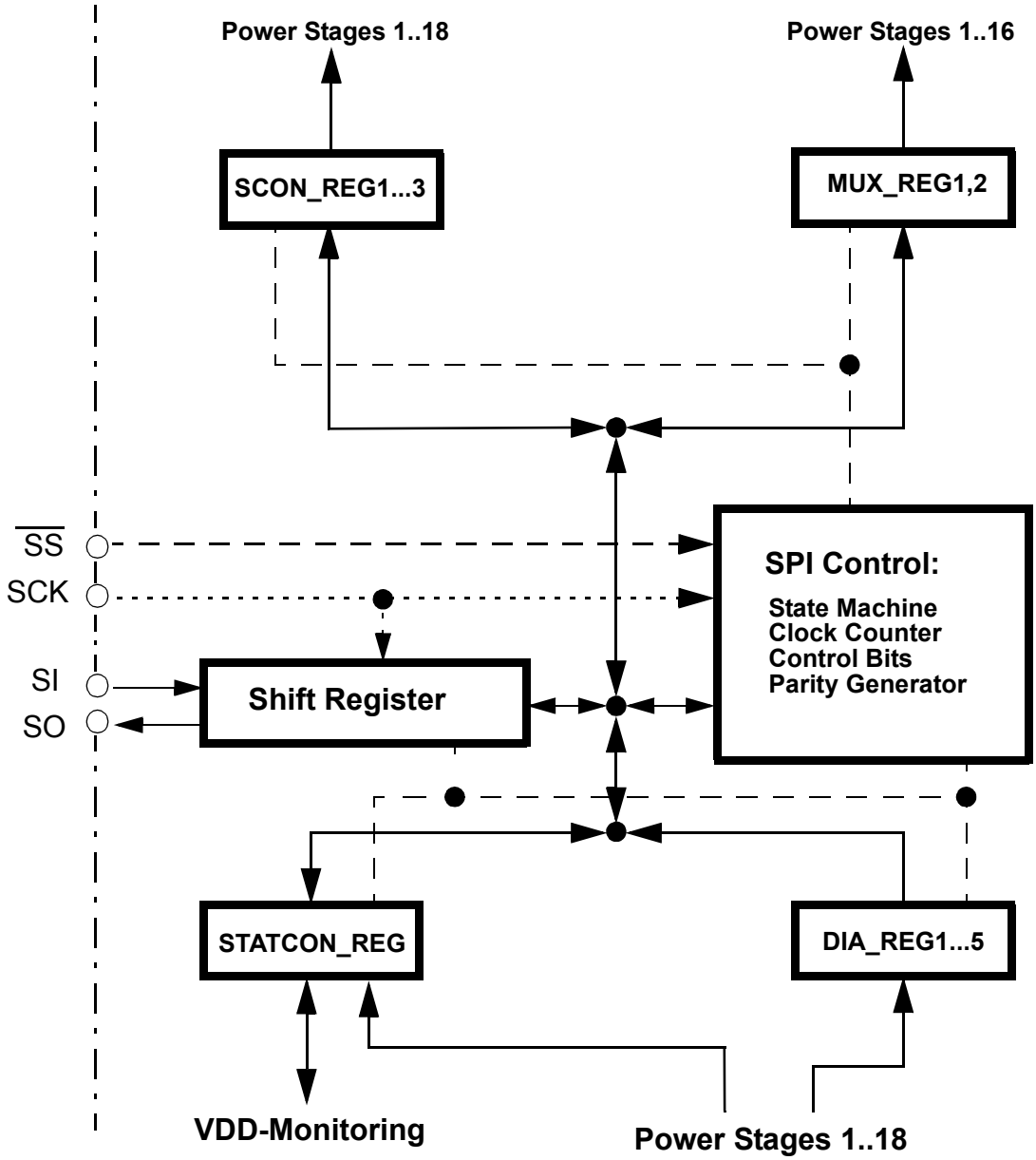
## 1.5 Function of Pins

| | |
|---|---|
| IN1 to IN16 | Control inputs of the power stages<br><br>Internal pull-up current sources (exception: IN8 with pull-down current source) |
| FCL<br>FDA<br>SSY | Clock for the µsec-bus (pin shared with IN16)<br>Data for the µsec-bus (pin shared with IN6)<br>Strobe and Synchronisation for the µsec-bus (pin shared with IN7) |
| OUT1 to OUT18 | Outputs of the power switches<br><br>Short-circuit proof<br>Low side switches<br>Limitation of the output voltage by zener diodes |
| VDD | Supply voltage 5V |
| UBatt | Supply voltage $U_{Batt}$<br><br>Pin must not be left open but has to be connected either to $U_{Batt}$ or to $V_{DD}$ (e.g. in commercial vehicles) |
| GND1 to GND8 | Ground pins<br><br>Ground pins for the power stages (see 2.4)<br>Ground reference of all logic signals is GND1/2 |
| $\overline{RST}$ | Reset<br><br>Active low<br>Locks all power switches regardless of their input signals (except OUT8)<br>Clears the fault registers<br>Resets the µsec-bus interface registers |
| $\overline{ABE}$ | In-/Output VDD-Monitoring<br><br>Active low<br>Output pin for the VDD-Monitoring<br>Input pin for the shut-off signal coming from the supervisor |
| GND_$\overline{ABE}$ | Sense ground VDD-Monitoring |
| SI, SO, SCK, $\overline{SS}$ | SPI Interface |

## 1.6 SPI Interface

The serial SPI interface establishes a communication link between TLE6244X and the systems microcontroller. TLE6244X always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 5 MBaud.
The TLE6244X is selected by the SPI master by an active slave select signal at $\overline{SS}$ and by the first two bits of the SPI instruction.SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.
In case of inactive slave select signal (High) the data output SO goes into tristate.

**Block Diagram:**



A SPI communication always starts with a SPI instruction sent from the controller to TLE6244X. During a write cycle the controller sends the data after the SPI instruction, beginning with the MSB. During a reading cycle, after having received the SPI instruction, TLE6244X sends the corresponding data to the controller, also starting with the MSB.

**SPI Command/Format:**

| **MSB** | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | INSTR4 | INSTR3 | INSTR2 | INSTR1 | INSTR0 | INSW |

| **Bit** | **Name** | **Description** |
|---|---|---|
| 7,6 | CPAD1,0 | Chip Address (has to be ‘0’, ‘0’) |
| 5-1 | INSTR (4-0) | SPI instruction (encoding) |
| 0 | INSW | Parity of the instruction |

**Characteristics of the SPI Interface:**

1) If the slave select signal at $\overline{SS}$ is High, the SPI-logic is set on default condition, i.e. it expects an instruction.

2) If the 5V-reset ($\overline{RST}$) is active, the SPI output SO is switched into tristate.
The VDD monitoring ($\overline{ABE}$) has no influence on the SPI interface.

3) Verification byte:
Simultaneously to the receipt of an SPI instruction TLE6244X transmits a verification byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial bit pattern and a flag indicating an invalid instruction of the previous access.

4) On a read access the databits at the SPI input SI are rejected. On a writing access or after the DEL_DIA instruction the TLE6244XTLE6244X sets the SPI output SO to low after sending the verification byte. If more than 16 bits are received the rest of the frame is rejected.

5) Invalid instruction/access:
An instruction is invalid, if one of the following conditions is fulfilled:
- an unused instruction code is detected (see tables with SPI instructions)
- in case the previous transmission is not completed in terms of internal data processing
- number of SPI clock pulses counted during active $\overline{SS}$ differs from exactly 16 clock pulses.
A write access and the instruction DEL_DIA is internally suppressed (i.e internal registers will not be affected) in all cases where at the rising (inactive) edge of $\overline{SS}$ the number of falling edges applied to the SPI input SCK during the access is not equal to 16. A write access is also internally suppressed (i.e internal registers will not be affected) if at the rising (inactive) edge of $\overline{SS}$ a 17th bit is submitted (SCK=‘1’).

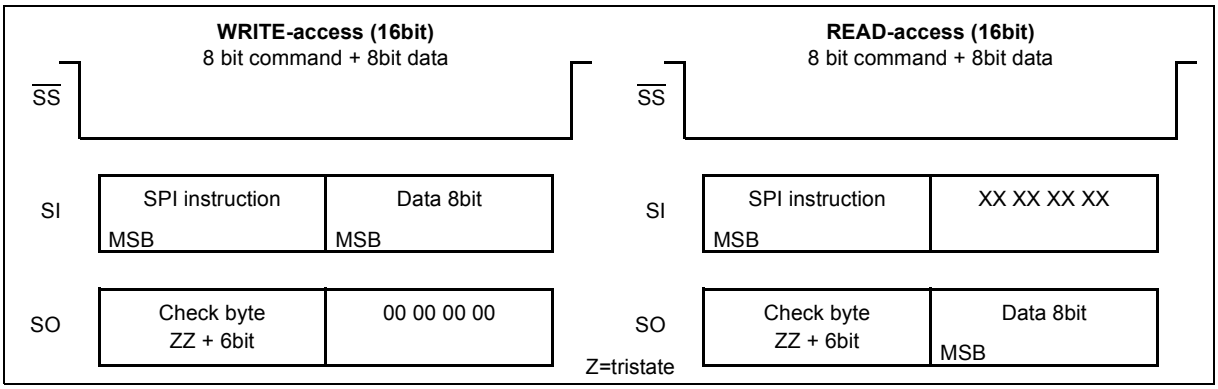
After the bits CPAD1,0 and INSTR (4-0) have been sent from the microcontroller TLE6244X is able to check if the instruction code is valid. If an invalid instruction is detected, any modification on a register of TLE6244X is not allowed and the data byte ‘FFh’ is transmitted after having sent the verification byte. If a valid read instruction is detected the content of the corresponding register is transmitted to the controller after having sent the verification byte (even if bit INSW afterwards is wrong). If a valid write instruction is

detected the data byte ’00h’ is transmitted to the controller after having sent the verification byte (even if bit INSW afterwards is wrong) but modifications on any register of TLE6244 are not allowed until bit INSW is valid, too.

If an invalid instruction is detected bit TRANS_F in the following verification byte is set to ’High’. This bit must not be cleared before it has been sent to the microcontroller.

6) If TLE6244X and additional IC’s are connected to one common slave select, they are distinguished by the chip address (CPAD1, CPAD0). If an IC with 32bit-transmission-format is selected, TLE6232 must not be activated, even if slave select is set to ’low’ and the first two bits of the third byte of the 32bit-transmission are identical to the chip address of TLE6244X.
During the transmission of CPAD1 and CPAD0 the data output SO remains in tristate (see timing diagram of the SPI in chapter 3.9. ).

**SPI access format:**




**Verification byte:**

| **MSB** | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Z | Z | 1 | 0 | 1 | 0 | 1 | TRANS_F |

| **Bit** | **Name** | **Description** |
|---|---|---|
| 0 | TRANS_F | Bit = 1: error detected during previous transfer<br>Bit = 0: previous transfer was recognised as valid<br>State after reset: 0 |
| 1 | | Fixed to High |
| 2 | | Fixed to Low |
| 3 | | Fixed to High |
| 4 | | Fixed to Low |
| 5 | | Fixed to High |
| 6 | | send as high impedance |
| 7 | | send as high impedance |

**SPI Instructions**

| SPI Instruction | Encoding | | | Description |
|---|---|---|---|---|
| | bit 7,6 CPAD1,0 | bit 5,4,3,2,1 INSTR(4...0) | Parity | |
| RD_IDENT1 | 00 | 00000 | 0 | read identifier 1 |
| RD_IDENT2 | 00 | 00001 | 1 | read identifier2 |
| | | | | |
| WR_STATCON | 00 | 10001 | 0 | write into STATCON_REG |
| WR_MUX1 | 00 | 10010 | 0 | write into MUX_REG1 |
| WR_MUX2 | 00 | 10011 | 1 | write into MUX_REG2 |
| WR_SCON1 | 00 | 10100 | 0 | write into SCON_REG1 |
| WR_SCON2 | 00 | 10101 | 1 | write into SCON_REG2 |
| WR_SCON3 | 00 | 10110 | 1 | write into SCON_REG3 |
| WR_CONFIG | 00 | 10111 | 0 | write into CONFIG |
| | | | | |
| RD_MUX1 | 00 | 00010 | 1 | read MUX_REG1 |
| RD_MUX2 | 00 | 00011 | 0 | read MUX_REG2 |
| RD_SCON1 | 00 | 00100 | 1 | read SCON_REG1 |
| RD_SCON2 | 00 | 00101 | 0 | read SCON_REG2 |
| RD_SCON3 | 00 | 00110 | 0 | read SCON_REG3 |
| RD_STATCON | 00 | 00111 | 1 | read STATCON_REG |
| DEL_DIA | 00 | 11000 | 0 | resets the 5 diagnostic registers DIA_REG |
| RD_DIA1 | 00 | 01000 | 1 | read DIA_REG1 |
| RD_DIA2 | 00 | 01001 | 0 | read DIA_REG2 |
| RD_DIA3 | 00 | 01010 | 0 | read DIA_REG3 |
| RD_DIA4 | 00 | 01011 | 1 | read DIA_REG4 |
| RD_DIA5 | 00 | 01100 | 0 | read DIA_REG5 |
| RD_CONFIG | 00 | 01101 | 1 | read CONFIG |
| RD_INP1 | 00 | 01110 | 1 | read INP_REG1 |
| RD_INP2 | 00 | 01111 | 0 | read INP_REG2 |
| | | all others | | no function |

### 1.6.1 Serial/Parallel Control

Serial/Parallel Control of the Power Stages 1...16 and Serial Control (SPI) of the Power Stages 17 and 18:
The registers MUX_REG1/2 and the bmux-bit prescribe parallel control or serial control (SPI or µsec-bus) of the power stages.

**(SPI-Instructions: WR_MUX1...2, RD_MUX1...2, WR_SCON1...3, RD_SCON1...3)**

The following table shows the truth table for the control of the power stages 1...18. The registers MUX_REG1, 2 prescribe parallel-control or serial control of the power stages. The registers SCON_REG1...3 prescribe the state of the power stage in case of SPI-serial control. BMUX determines parallel control or control by µsec-bus.
For the power stages 17 and 18 control is exclusively possible via SCON17/18. IN17/18 and MUX17/18 do **not** exist. BMUX has no function for OUT17/18.

| $\overline{\text{ABE}}$ | $\overline{\text{RST}}$ | INx | BMUX | MUXx | SCONx | µsec-REGx | Output OUTx of Power Stage x, x = 1..18 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | X | X | X | OUTx off |
| 0 | 1 | X | X | X | X | X | OUTx off |
| 1 | 0 | X | X | X | X | X | OUTx off |
| 1 | 1 | X | X | 0 | 0 | X | SPI Control: OUTx on |
| 1 | 1 | X | X | 0 | 1 | X | SPI Control: OUTx off |
| 1 | 1 | 0 | 1 | 1 | X | X | Parallel Control: OUTx on |
| 1 | 1 | 1 | 1 | 1 | X | X | Parallel Control: OUTx off |
| 1 | 1 | X | 0 | 1 | X | 0 | µsec-bus Control: OUTx on |
| 1 | 1 | X | 0 | 1 | X | 1 | µsec-bus Control: OUTx off |

Exception: OUT8 is on (active) if IN8 is set to logic ‘1’ (and off if IN8 is set to logic ‘0’) in case of parallel access.

Note: OUT8 cannot be controlled by the µsec-Bus. Refer to section 1.7.

### Description of the SPI Registers

| Register: MUX_REG1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MUX7 | MUX6 | MUX5 | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 |

**State of Reset: 80H**

**Access by Controller:** Read/Write

| Bit | Name | Description |
|---|---|---|
| 0 | MUX0 | Serial or parallel control of power stage 1 |
| 1 | MUX1 | Serial or parallel control of power stage 2 |
| 2 | MUX2 | Serial or parallel control of power stage 3 |
| 3 | MUX3 | Serial or parallel control of power stage 4 |
| 4 | MUX4 | Serial or parallel control of power stage 5 |
| 5 | MUX5 | Serial or parallel control of power stage 6 |
| 6 | MUX6 | Serial or parallel control of power stage 7 |
| 7 | MUX7 | Serial or parallel control of power stage 8 |

| Register: MUX_REG2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MUX15 | MUX14 | MUX13 | MUX12 | MUX11 | MUX10 | MUX9 | MUX8 |

**State of Reset: 00H**

**Access by Controller:** Read/Write

| Bit | Name | Description |
|---|---|---|
| 0 | MUX8 | Serial or parallel control of power stage 9 |
| 1 | MUX9 | Serial or parallel control of power stage 10 |
| 2 | MUX10 | Serial or parallel control of power stage 11 |
| 3 | MUX11 | Serial or parallel control of power stage 12 |
| 4 | MUX12 | Serial or parallel control of power stage 13 |
| 5 | MUX13 | Serial or parallel control of power stage 14 |
| 6 | MUX14 | Serial or parallel control of power stage 15 |
| 7 | MUX15 | Serial or parallel control of power stage 16 |

| Register: SCON_REG1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCON7 | SCON6 | SCON5 | SCON4 | SCON3 | SCON2 | SCON1 | SCON0 |

| State of Reset: FFH | | |
|---|---|---|
| Access by Controller: Read/Write | | |
| **Bit** | **Name** | **Description** |
| 0 | SCON0 | State of serial control of power stage 1 |
| 1 | SCON1 | State of serial control of power stage 2 |
| 2 | SCON2 | State of serial control of power stage 3 |
| 3 | SCON3 | State of serial control of power stage 4 |
| 4 | SCON4 | State of serial control of power stage 5 |
| 5 | SCON5 | State of serial control of power stage 6 |
| 6 | SCON6 | State of serial control of power stage 7 |
| 7 | SCON7 | State of serial control of power stage 8 |

| Register: SCON_REG2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCON15 | SCON14 | SCON13 | SCON12 | SCON11 | SCON10 | SCON9 | SCON8 |

| State of Reset: FFH | | |
|---|---|---|
| Access by Controller: Read/Write | | |
| **Bit** | **Name** | **Description** |
| 0 | SCON8 | State of serial control of power stage 9 |
| 1 | SCON9 | State of serial control of power stage 10 |
| 2 | SCON10 | State of serial control of power stage 11 |
| 3 | SCON11 | State of serial control of power stage 12 |
| 4 | SCON12 | State of serial control of power stage 13 |
| 5 | SCON13 | State of serial control of power stage 14 |
| 6 | SCON14 | State of serial control of power stage 15 |
| 7 | SCON15 | State of serial control of power stage 16 |

| Register: SCON_REG3 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | SCON17 | SCON16 |

| State of Reset: FFH | | |
|---|---|---|
| Access by Controller: Read/Write | | |
| **Bit** | **Name** | **Description** |
| 0 | SCON16 | State of serial control of power stage 17 |
| 1 | SCON17 | State of serial control of power stage 18 |
| 7-2 | | No function: HIGH on reading |

### 1.6.2 Diagnostics/Encoding of Failures

**Description of the SPI Registers**

**(SPI Instructions: RD_DIA1...5)**

| **Register: DIA_REG1** | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIA7 | DIA6 | DIA5 | DIA4 | DIA3 | DIA2 | DIA1 | DIA0 |

| **State of Reset: FFH** | | |
|---|---|---|
| **Access by Controller:** Read only | | |
| **Bit** | **Name** | **Description** |
| 1-0 | DIA (1-0) | Diagnostic Bits of power stage 1 |
| 3-2 | DIA (3-2) | Diagnostic Bits of power stage 2 |
| 5-4 | DIA (5-4) | Diagnostic Bits of power stage 3 |
| 7-6 | DIA (7-6) | Diagnostic Bits of power stage 4 |

| **Register: DIA_REG2** | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIA15 | DIA14 | DIA13 | DIA12 | DIA11 | DIA10 | DIA9 | DIA8 |

| **State of Reset: FFH** | | |
|---|---|---|
| **Access by Controller:** Read only | | |
| **Bit** | **Name** | **Description** |
| 1-0 | DIA (9-8) | Diagnostic Bits of power stage 5 |
| 3-2 | DIA (11-10) | Diagnostic Bits of power stage 6 |
| 5-4 | DIA (13-12) | Diagnostic Bits of power stage 7 |
| 7-6 | DIA (15-14) | Diagnostic Bits of power stage 8 |

| Register: DIA_REG3 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIA23 | DIA22 | DIA21 | DIA20 | DIA19 | DIA18 | DIA17 | DIA16 |

**State of Reset: FFH**

**Access by Controller:** Read only

| Bit | Name | Description |
|---|---|---|
| 1-0 | DIA (17-16) | Diagnostic Bits of power stage 9 |
| 3-2 | DIA (19-18) | Diagnostic Bits of power stage 10 |
| 5-4 | DIA (21-20) | Diagnostic Bits of power stage 11 |
| 7-6 | DIA (23-22) | Diagnostic Bits of power stage 12 |

| Register: DIA_REG4 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIA31 | DIA30 | DIA29 | DIA28 | DIA27 | DIA26 | DIA25 | DIA24 |

**State of Reset: FFH**

**Access by Controller:** Read only

| Bit | Name | Description |
|---|---|---|
| 1-0 | DIA (25-24) | Diagnostic Bits of power stage 13 |
| 3-2 | DIA (27-26) | Diagnostic Bits of power stage 14 |
| 5-4 | DIA (29-28) | Diagnostic Bits of power stage 15 |
| 7-6 | DIA (31-30) | Diagnostic Bits of power stage 16 |

| Register: DIA_REG5 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | 1 | UBatt | DIA35 | DIA34 | DIA33 | DIA32 |

| State of Reset: FFH | | |
|---|---|---|
| **Access by Controller:** Read only | | |
| **Bit** | **Name** | **Description** |
| 1-0 | DIA (33-32) | Diagnostic Bits of power stage 17 |
| 3-2 | DIA (35-34) | Diagnostic Bits of power stage 18 |
| 4 | UBatt | 0: Voltage Level at Pin UBatt is below 2V (typically)<br>1: Voltage Level at Pin UBatt is above 2V (typically)<br>Diagnosis of UBatt is only possible if $U_{VDD}$ > 4.5V<br>Status of UBatt is not latched. |
| 7-5 | | No function: High on reading |

| Encoding of the Diagnostic Bits of the Power Stages | | |
|---|---|---|
| DIA(2*x-1) | DIA(2*x-2) | State of power stage x x = 1..18 |
| 1 | 1 | Power stage o.k. |
| 1 | 0 | Short-circuit to $U_{Batt}$ (SCB) / OT |
| 0 | 1 | Open load (OL) |
| 0 | 0 | Short-circuit to ground (SCG) |

### 1.6.3 Configuration

The µsec-bus is enabled by this register. In addition the shut off at SCB can be configured for the power-stages OUT9, OUT10 and OUT15... OUT18.

| CONFIG (Read and write) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O16-SCB | O15-SCB | O10-SCB | O9-SCB | O18-SCB | O17-SCB | BMUX | 1 |

| State of Reset: FFh | | |
|---|---|---|
| **Bit** | **Name** | **Description** |
| 0 | | No function: HIGH on reading |
| 1 | BMUX | 1: parallel inputs INx enabled<br>0: µsec-Bus Interface enabled |
| 2 | O17-SCB | 1: The output OUT17 is switched off in case of SCB<br>0: The output is not switched off in case of SCB |
| 3 | O18-SCB | 1: The output OUT18 is switched off in case of SCB<br>0: The output is not switched off in case of SCB |
| 4 | O9-SCB | 1: The output OUT9 is switched off in case of SCB<br>0: The output is not switched off in case of SCB |
| 5 | O10-SCB | 1: The output OUT10 is switched off in case of SCB<br>0: The output is not switched off in case of SCB |
| 6 | O15-SCB | 1: The output OUT15 is switched off in case of SCB<br>0: The output is not switched off in case of SCB |
| 7 | O16-SCB | 1: The output OUT16 s switched off in case of SCB<br>0: The output is not switched off in case of SCB |

Description of the µsec-bus see chapter 1.7

### 1.6.4 Other

**Reading the IC Identifier (SPI Instruction: RD_IDENT1):**

| IC Identifier1 (Device ID) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

| Bit | Name | Description |
|---|---|---|
| 7...0 | ID(7...0) | ID-No.: 10101000 |

**Reading the IC revision number (SPI Instruction: RD_IDENT2):**

| IC revision number | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SWR3 | SWR2 | SWR1 | SWR0 | MSR3 | MSR2 | MSR1 | MSR0 |
| | | | | | | | |

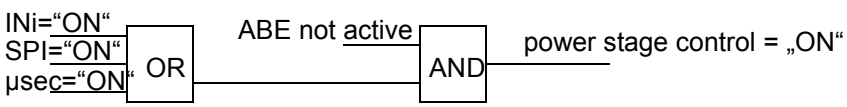
| Bit | Name | Description |
|---|---|---|
| 7...4 | SWR(3...0) | Revision corresponding to Software release: $0_{Hex}$ |
| 3...0 | MSR(3...0) | Revision corresponding to Maskset: $0_{Hex}$ |

**Reset of the Diagnostic Information (SPI Instruction: DEL_DIA):**

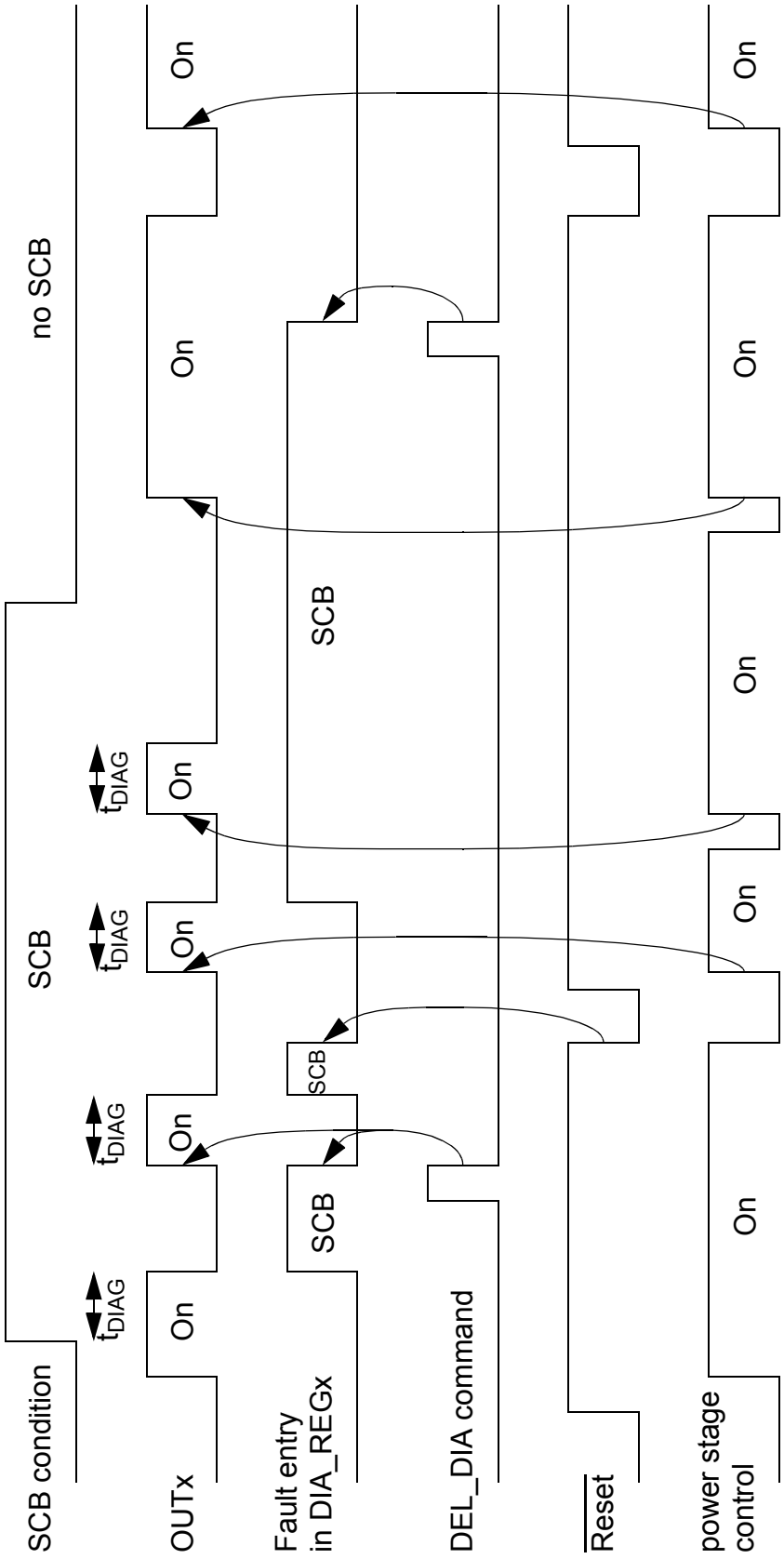
Resets the 5 diagnostic registers DIA_REG1...5 to FFH and the common overtemperature flag in register STATCON_REG (Bit4) to High. These bits are only cleared by the DEL_DIA instruction when there is no failure entry at the input of the registers.
Access is performed like a writing access with any data byte.

In the case a power stage is shut off because of SCB, the output is activated again by the DEL_DIA instruction and the filtering-time is enabled. Therefore in case of SCB the output is activated and shut off after the shutoff delay.
For a power stage in the current limitation mode, the current limitation mode is left, if a DEL_DIA instruction has been received. If there is still the condition for SCB the current limitation mode is entered again.

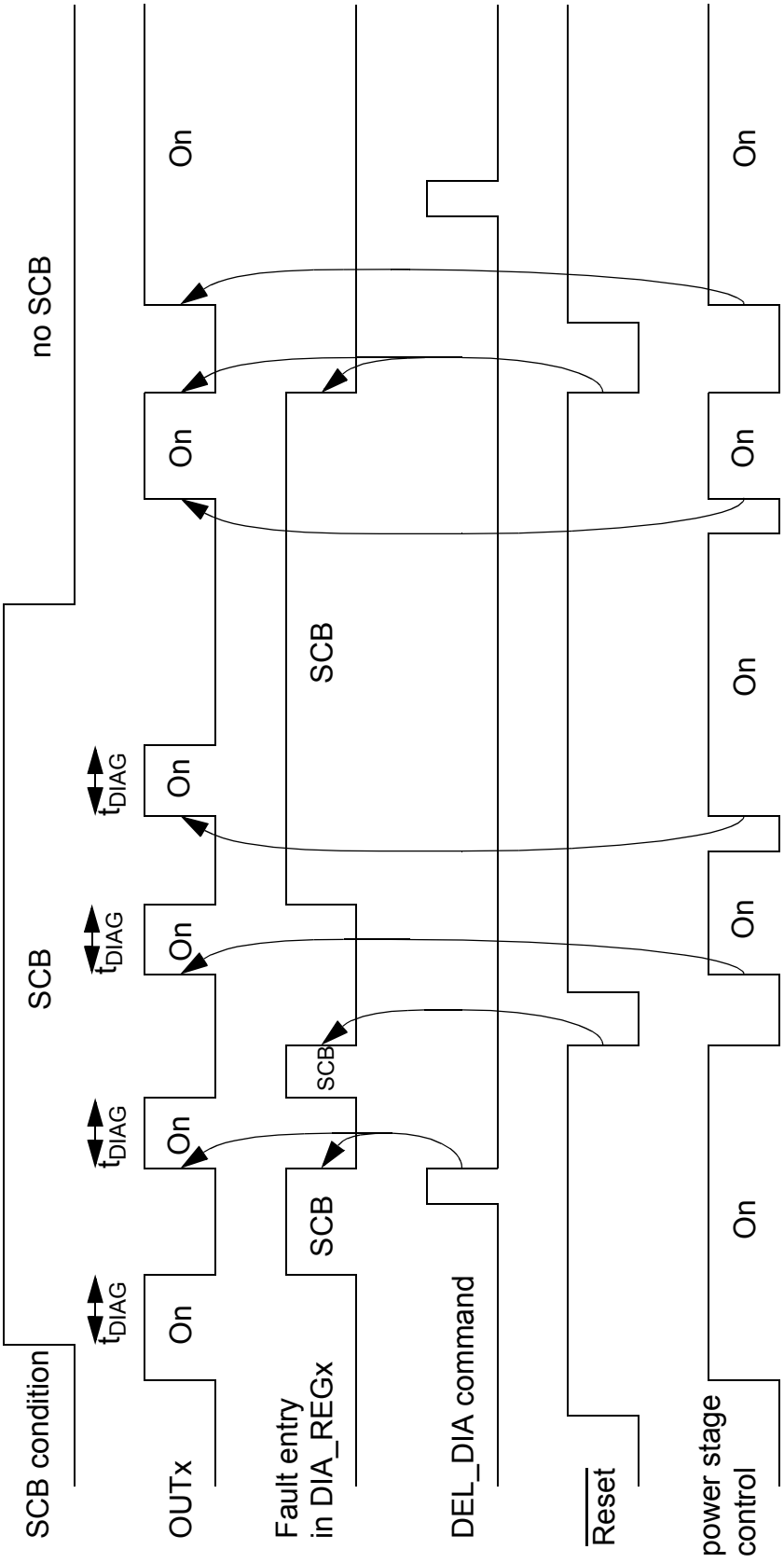
On the following pages the conditions for set and reset of the SCB report in DIA_REGx is shown in several schematics. The signal „power stage control“ is generated as follows:



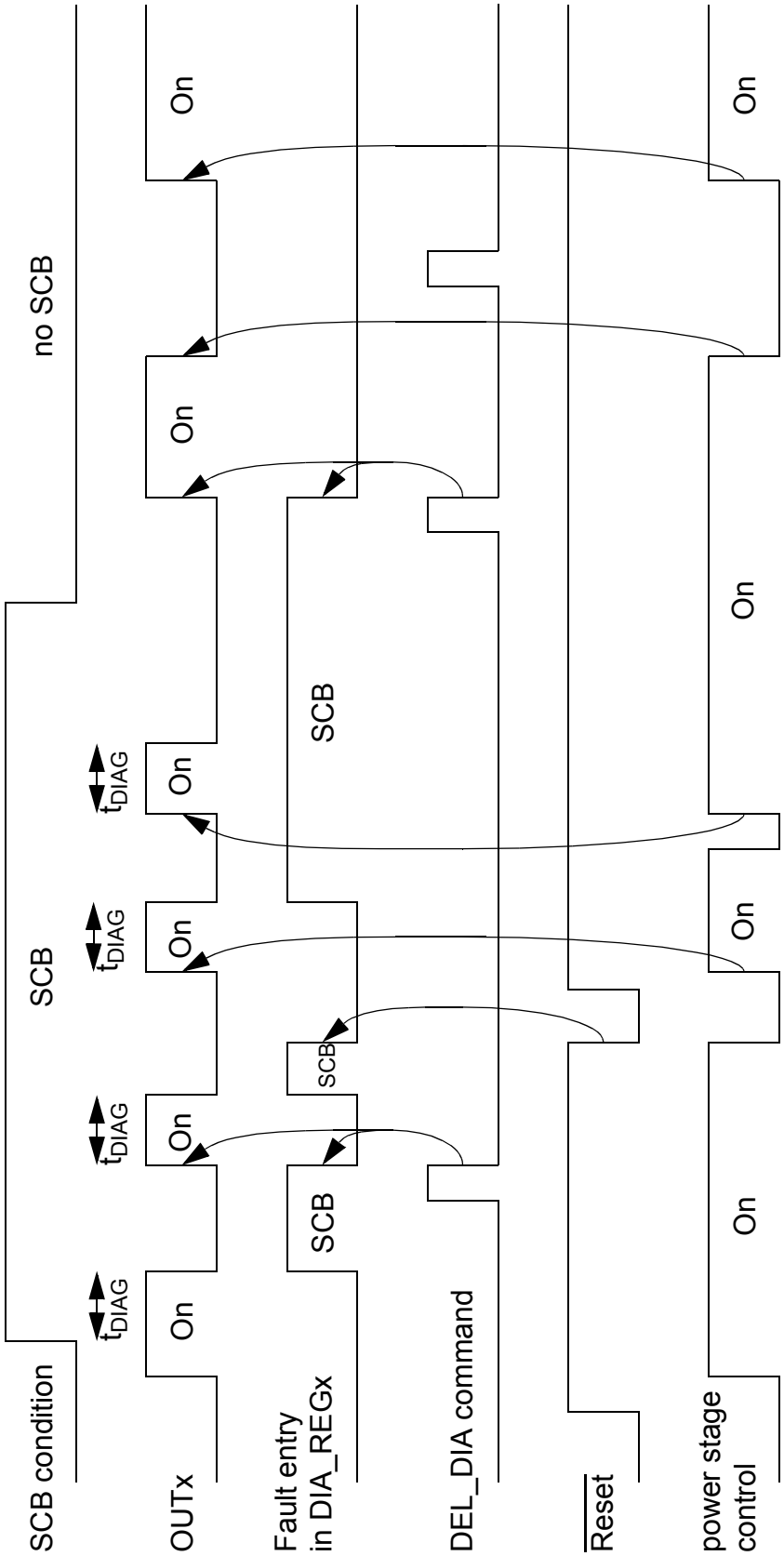
**Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by DEL_DIA after SCB condition disappeared and power stage control was toggled**



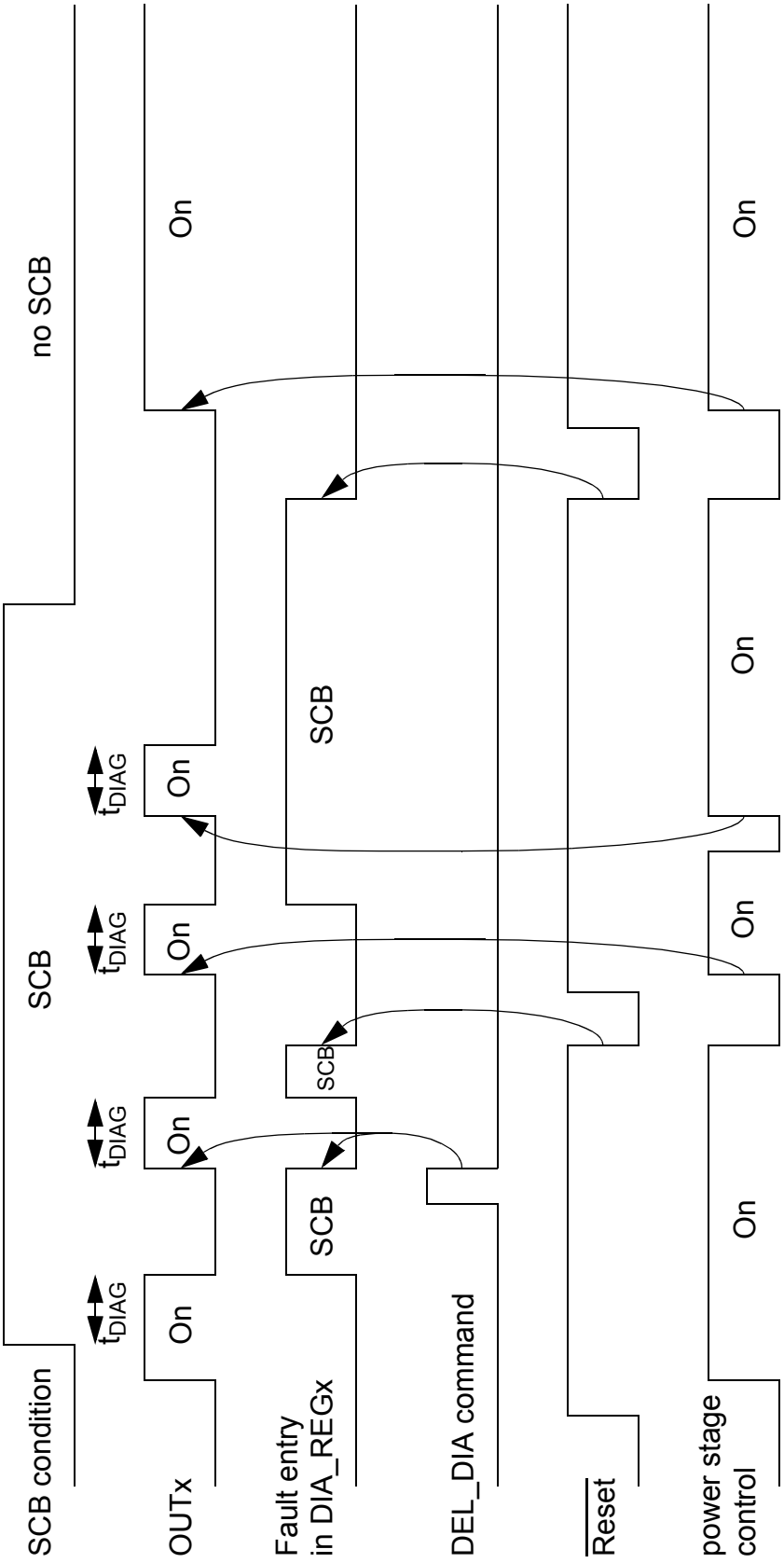
**Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by Reset after SCB condition disappeared and power stage control was toggled**



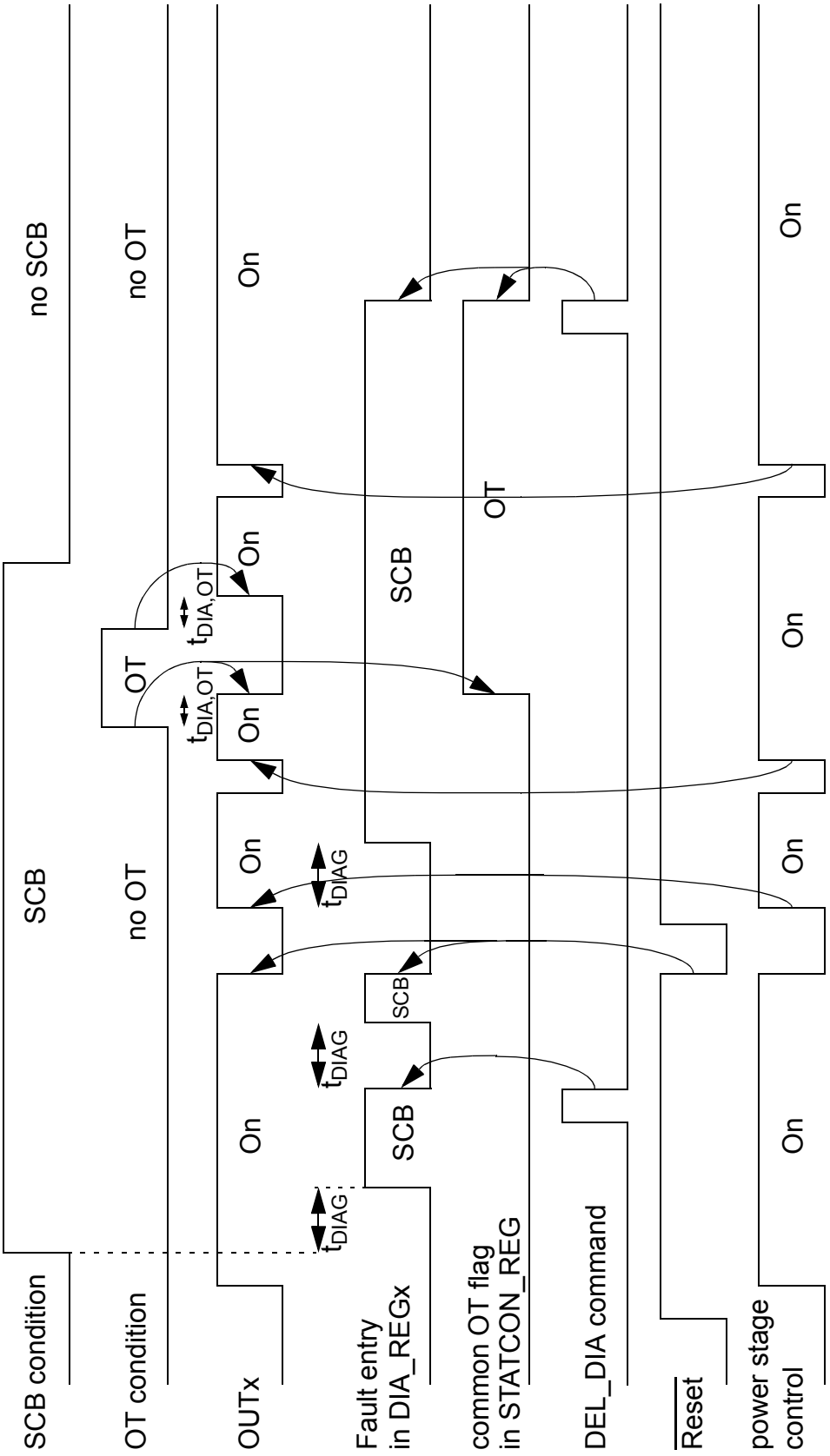
**Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by DEL_DIA after SCB condition disappeared but power stage control was not toggled**



**Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by Reset after SCB condition disappeared but power stage control was not toggled**



**Schematic of SCB report of power stages OUT9,10,15...18 (power stage programmed for current limitation in case of SCB), SCB resp. OT flag entry deleted exemplary by DEL_DIA after SCB resp. OT condition disappeared and power stage control was toggled**



**Reading Input1 (SPI Instruction: RD_INP1)**
**:**

| Register INP_REG1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN8 | Test | 0 | IN5 | IN4 | IN3 | IN2 | IN1 |

| Bit | Name | Description |
|---|---|---|
| 0..4 | IN(1...5) | Status of the input pins IN1... IN5 |
| 5 | | No function: LOW on reading |
| 6 | Test | µsec-test-bit, the bit D8 of the µsec-bus is read |
| 7 | IN8 | Inverted status of the input pin IN8:<br>Low level at pin IN8: Bit 7 = 1<br>High level at pin IN8: Bit 7 = 0 |

**Reading Input2 (SPI Instruction: RD_INP2):**

| Register INP_REG2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | IN15 | IN14 | IN13 | IN12 | IN11 | IN10 | IN9 |

| Bit | Name | Description |
|---|---|---|
| 0..6 | IN9...IN15 | Status of the input pins IN9...IN15 |
| 7 | | No function: LOW on reading |

The input pins IN1..IN5 and IN8...IN15 can be used as input port expander by reading the status of the input pins using the SPI-commands RD_INP1/2. If the µsec-bus-interface is enabled (BMUX=0) the pull-up current sources at the input IN1..5 and IN9..15 are disabled. If BMUX=1 the pullup current sources at these pins are enabled. The pull-up/pull-down current sources of the other input pins are not effected by the bit BMUX.

On executing the read instruction on RD_INP1/2, the present status (not latched) of the input pins INx is read back (exception: bit IN8 represents the **inverted** status of input pin IN8).

**Reading the State resp. the Configuration:**
**(SPI Instructions: WR_STATCON, RD_STATCON)**

| **Register: STATCON_REG** | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CONFIG2 | CONFIG1 | CONFIG0 | STATUS4 | STATUS3 | STATUS2 | STATUS1 | STATUS0 |

| Bit | Name | Description |
|---|---|---|
| 0 | STATUS0 | Bit = 1: No overvoltage at VDD<br>Bit = 0: Overvoltage at VDD resp. state of overvoltage still stored (reset by CONFIG0 = 0)<br>**Access by Controller:** Read only<br>Overvoltage information (bit STATUS0 = 0) will not be reset by an external reset signal (pin RST=low). Overvoltage will be detected and stored (CONFIG0 = 1) during RST=low. The information will be deleted when an internal (undervoltage) reset occurs or when CONFIG0 is set to 0. |
| 1 | STATUS1 | Bit = 1: No undervoltage at VDD<br>Bit = 0: Undervoltage at VDD<br>**Access by Controller:** Read only |
| 2 | STATUS2 | Reading the voltage level at $\overline{ABE}$<br>**Access by Controller:** Read only |
| 3 | STATUS3 | Common error flag<br>Bit =1: At present no error is entered in one of the 5 diagnostic registers DIA_REG1..5.<br>Bit = 0: For at least at one power stage an error has been detected and entered in the corresponding diagnostic register.<br>**Access by Controller:** Read only |
| 4 | STATUS4 | Common overtemperature flag<br>Bit = 1: No overtemperature detected since the last reset of diagnostic information (by del_dia instruction, $\overline{RST}$ = Low or undervoltage at VDD (see 3.2. ))<br>Bit = 0: Overtemperature for at least one power stage has been detected since the last reset of the diagnostic information (by del_dia instruction, $\overline{RST}$ = Low or undervoltage at VDD (see 3.2. ))<br>**State of Reset: 1**<br>**Access by Controller:** Read only |
| 5 | CONFIG0 | Bit = 1: Latch function for overvoltage at VDD is switched on<br>Bit = 0: Latch function for overvoltage at VDD is switched off<br>**State of Reset: 1**<br>**Access by Controller:** Read/Write |

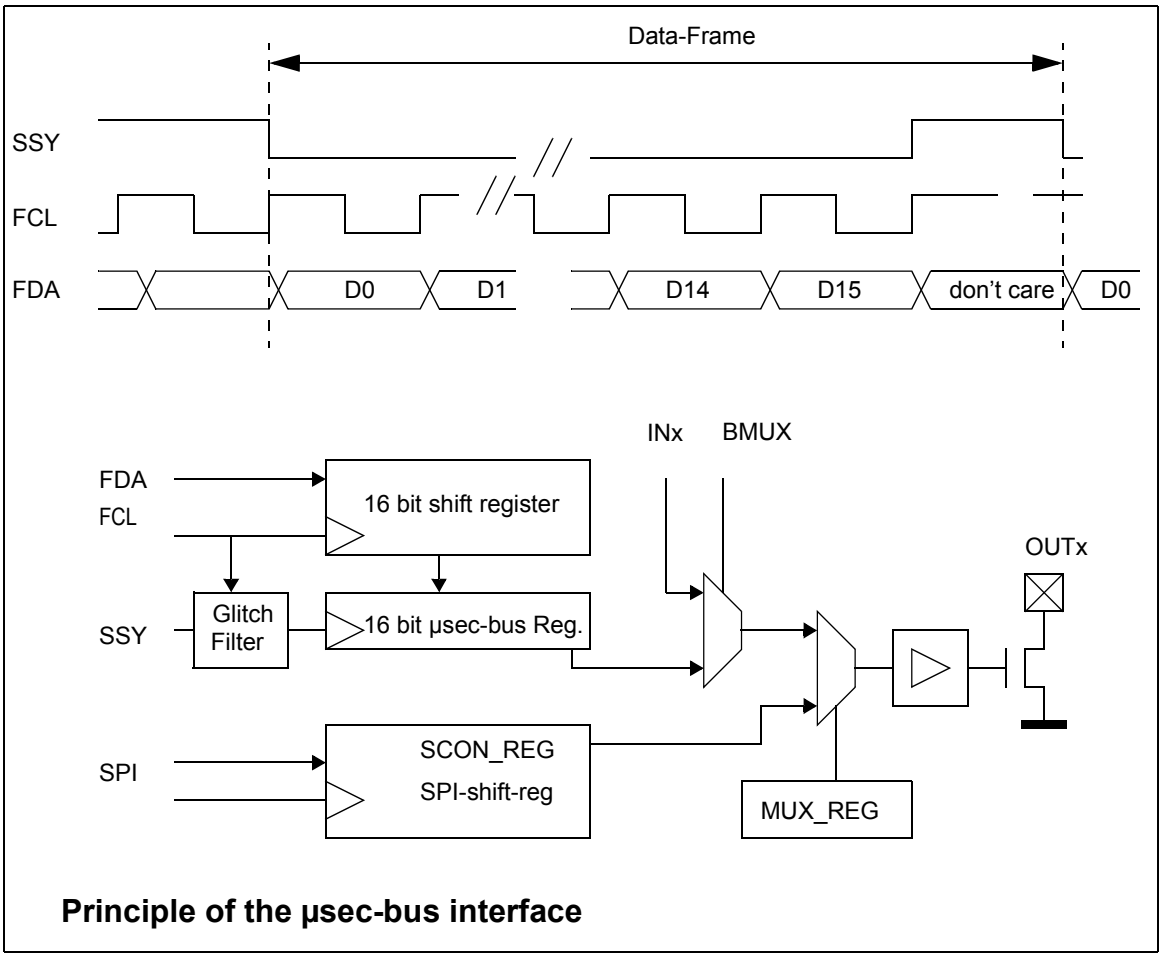
| | | |
|---|---|---|
| 6 | CONFIG1 | Bit = 1: Lower threshold of VDD-monitoring is lifted<br>if bit CONFIG2 = 0 (test of switch-off path)<br>Bit = 0: Upper threshold of VDD-monitoring is reduced<br>if bit CONFIG2 = 0 (test of switch-off path)<br>**State of Reset: 1**<br>**Access by Controller:** Read/Write |
| 7 | CONFIG2 | Bit = 1: Test of VDD threshold is switched off<br>Bit = 0: Test of VDD threshold is switched on<br>**State of Reset: 1**<br>**Access by Controller:** Read/Write |

## 1.7 µsec - Bus Interface

The µsec-bus-interface is one of three possibilities to control the power stages. OUT1...OUT7 and OUT9...OUT16 are influenced by the reset input RST. If RST is set to Low, these power stages are switched off. After reset they are controlled by the SPI (default initialization of TLE6244X). Power stage 8 however is not influenced by the reset input if it's controlled by IN8 and $U_{VDD} \geq 3{,}5V$. Alternatively these outputs can be controlled either by the pins IN1...IN16 or by the µsec-bus interface. Exception: OUT8 can be controlled by IN8 or by the SPI-interface only. The bit 'Bus-Multiplex' (BMUX) in the SPI register CONFIG prescribes parallel access (IN1...IN7, IN9...IN16) or µsec-bus control (see figure below). Exception: If BMUX is set to '0' only the power-stages OUT1...OUT7 and OUT9...OUT16 are controlled by the µsec-bus.

**Main features:**

- 16 data bits for each data-frame (at the pin FDA)
- 16 clock-pulses for each data-frame (at the pin FCL)
- clock frequency TLE6244: 0...16 MHz
- one sync -input (pin SSY) to latch the input data stream
- input level interface same as for IN6, IN7, IN16
- no error correction




**Principle of the µsec-bus interface**

When the bit BMUX in CONFIG is set to Low, the power stages 1...7 and 9...16 are controlled by the µsec-bus-interface on condition that registers MUX_REG1/2 are configured for serial access. The received µsec-bus bit stream (D0... D15) is latched into a 16-bit register by the rising edge at SSY. Power stages 1...7 and 9...16 are switched according to bits D0...D7 and D9...D15:

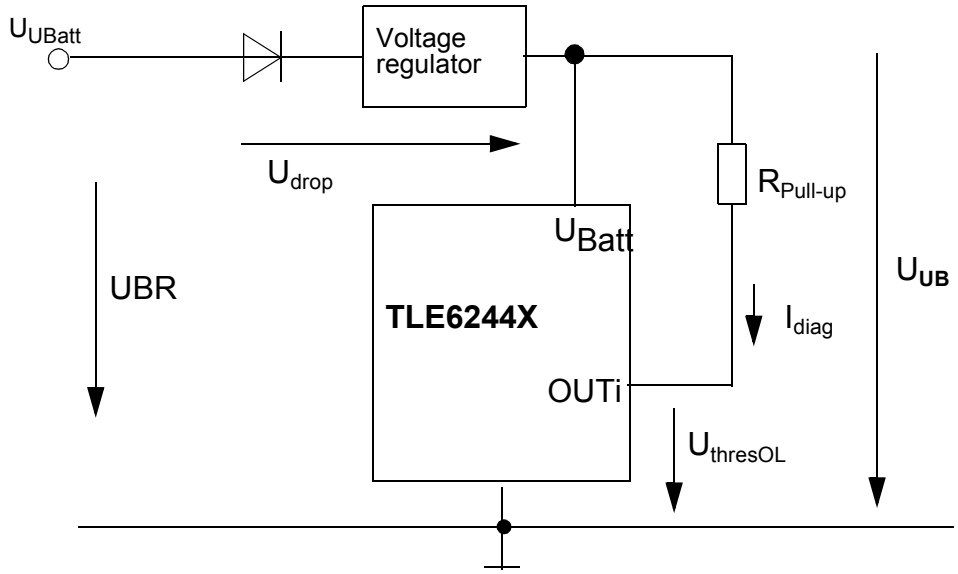
| µsec-bus | control of power stage | µsec-bus | control of power stage |
|---|---|---|---|
| D0 | OUT14 | D8 | µsec-bus Test Bit |
| D1 | OUT1 | D9 | OUT11 |
| D2 | OUT2 | D10 | OUT10 |
| D3 | OUT3 | D11 | OUT9 |
| D4 | OUT4 | D12 | OUT12 |
| D5 | OUT5 | D13 | OUT13 |
| D6 | OUT6 | D14 | OUT16 |
| D7 | OUT7 | D15 | OUT15 |

Bit Dx = 0: Power stage OUTx is switched on
Bit Dx = 1: Power stage OUTx is switched off
State of reset: $FFFF_H$

Because the power stage 8 is not controlled by the µsec-bus-interface, the corresponding bit D8 can be used as test bit, that can be read back by the SPI-interface (see register RD_INP1).
If the µsec-bus-interface is used to control the power stages, the input pins IN1..IN5 and IN8...IN15 can be used as input port expander by reading the status of the input pins by the SPI-commands RD_INP1/2.

### 1.8 Unused Power Stages

To avoid an „open load“ fault indication an unused power switch has to be connected to an external pull up resistor connected to $U_{UB}$ or has to be switched on by the input pin or via SPI or the µsec-bus-interface.



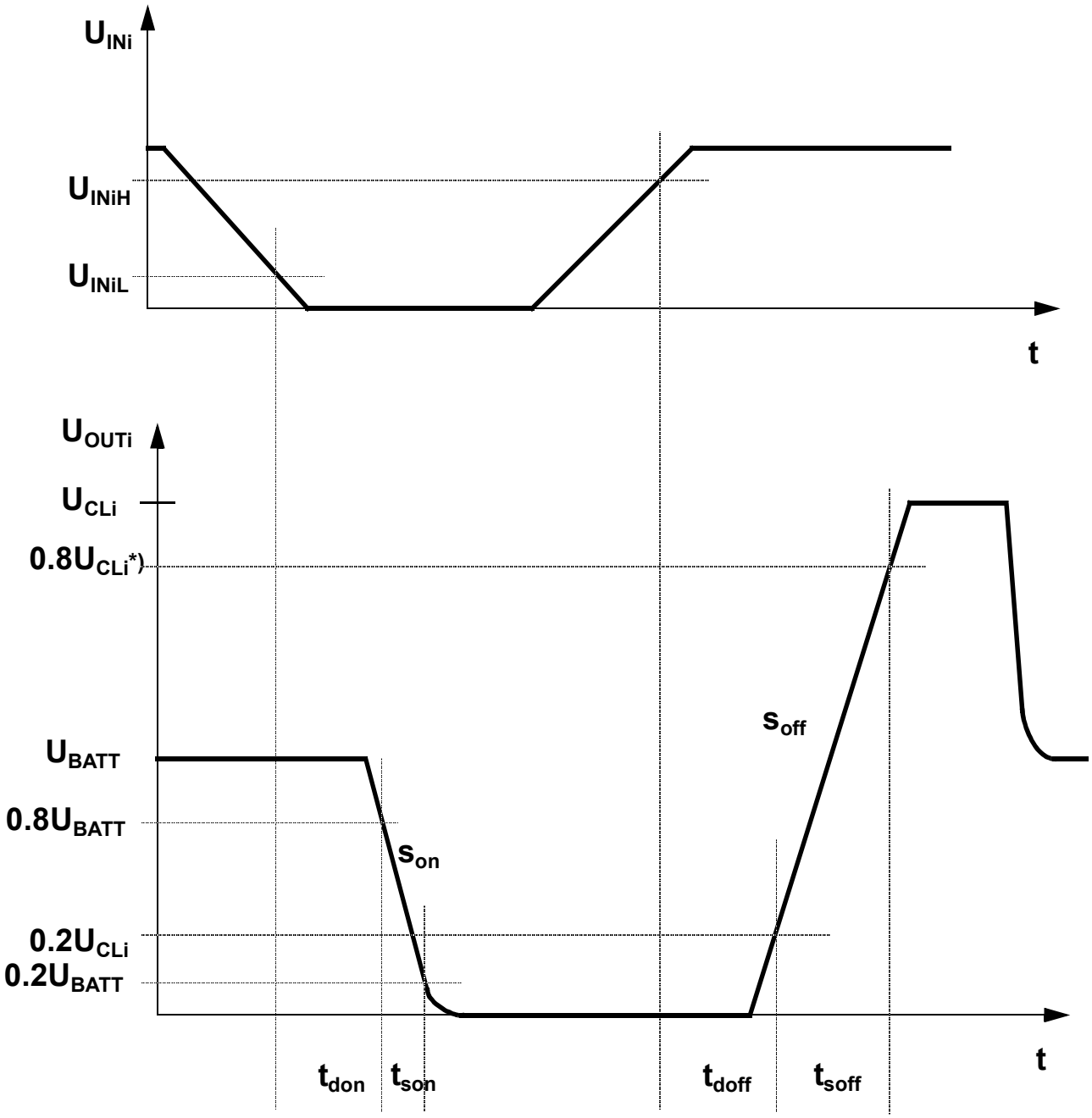

$$R_{Pull\text{-}up,max} = (UBR_{min} - U_{drop,max} - U_{thresOL,max}) / I_{diag,max}$$

$UBR_{min}$ is the required minimum battery voltage for diagnostic function of the ECU. The drop voltage is composed of the drop voltage of the regulator and the drop voltage of the reverse protection circuit of the regulator resp. the forward voltage of a reverse protection diode.

**Attention:**
This equation also applies to power switches that are used as signal drivers (pull up resistor inside ECU or outside ECU): the permissible pull up resistance without a wrong diagnostic information is calculated by the same equation. On dimensioning the pull up resistance in combination with the diagnostic current, in applications as signal drivers attention must be paid especially to the required high level (also for low battery voltage).

## 1.9 Timing Diagram of the Power Outputs

### 1.9.1 Power Stages




If the output is controlled via SPI the timing starts with the positive slope at SS
If the output is controlled by the µsec-bus, the timing starts with the pos. slope of SSY
*) With ohmic load, UCLi = UBatt

## 1.10 VDD-Monitoring

**Overview:**

The VDD-monitoring generates a „low“ signal at the bidirectional pin $\overline{ABE}$ if the 5V supply voltage at pin VDD is out of the permissible range of 4.5V...5.5V. On $\overline{ABE}$ = low the power stages of TLE6244X are switched off. Exception: OUT8 is not switched off in case of parallel control via IN8 by the VDD monitoring undervoltage threshold, but by a threshold of 3.5V at VDD.
On shorting pin $\overline{ABE}$ to $V_{DD}$ or UBATT (≤ 36V), the power stages will be switched off in case of undervoltage or overvoltage at pin VDD in spite of $\overline{ABE}$ = high.
The behavior of the $\overline{ABE}$ level on the return of VDD out of the undervoltage range into the correct range is not configurable. At the transition from undervoltage to normal voltage the signal at pin $\overline{ABE}$ goes high after a filtering time is expired. The behavior of the $\overline{ABE}$ level on the return of VDD out of the overvoltage range into the correct range is configurable in STATCON_REG, Bit5. At the transition from overvoltage to normal voltage the signal at pin $\overline{ABE}$ goes high either after a filtering time (OV not latched) or after a SPI writing instruction (OV latched, state after reset).
On undervoltage condition the signal at pin $\overline{ABE}$ goes high after a filtering time is expired. On overvoltage condition pin $\overline{ABE}$ goes high either after a filtering time or after a SPI writing instruction. Before this SPI instruction is sent to TLE6244X appropriate tests can be carried out by the controller.
If the voltage at pin VDD is below the lower limit or is resp. was above the upper limit, this can be read out by the SPI instruction RD_STATCON.
VDD-monitoring has **no** influence on SCON_REGx, MUX_REGx, DIA_REGx, CONFIG and INP_REGx.
If output stages are switched off by the internal over-/undervoltage detection or by externally applying a low signal at the $\overline{ABE}$ pin, no failure storage (DIAREG1...5) may occur.

**Description in Detail:**

Description of the Register:
STATCON_REG

Bit 7 1: Normal operation
0: Test of VDD threshold
Access by controller: read/write
State of reset: 1

Bit 6 1: Testing the lower threshold (if bit 7 = 0)
0: Testing the upper threshold (if bit 7 = 0)
Access by controller: read/write
State of reset: 1

Bit 5 1: $\overline{ABE}$ latched after overvoltage
0: $\overline{ABE}$ deactivated immediately after the disappearance of the overvoltage
Access by controller: read/write
State of reset: 1

Bit 2 Reading out the level at pin $\overline{ABE}$
Access by controller: read only

Bit 1 1: no undervoltage at pin VDD
0: undervoltage at pin VDD
Access by controller: read only

Bit 0 1: no overvoltage at pin VDD
0: overvoltage at pin VDD resp. state of overvoltage still stored
Access by controller: read only

Testing the VDD-Monitoring:

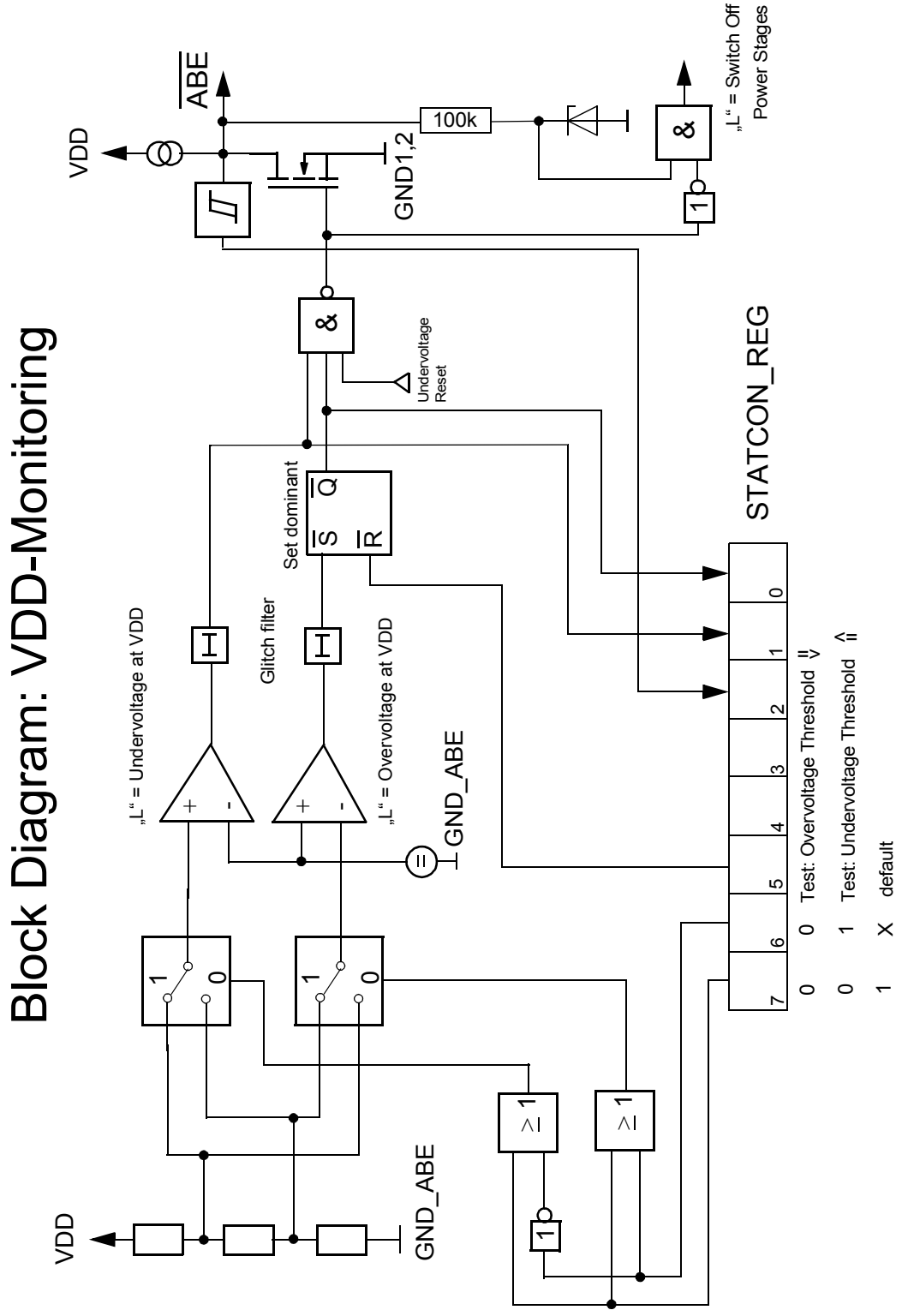
Upper threshold:
By writing $000xxxxx_b$ in the register STATCON_REG the overvoltage threshold is reduced by 0.8V. In STATCON_REG Bit 0 has to be LOW then.
After writing $110xxxxx_b$ in the register STATCON_REG Bit 0 in STATCON_REG must be HIGH again.

Lower threshold:
By writing $010xxxxx_b$ in the register STATCON_REG the overvoltage threshold is increased by 0.8V. In STATCON_REG Bit 1 has to be LOW then.
After writing $110xxxxx_b$ in the register STATCON_REG Bit 1 in STATCON_REG must be HIGH again.

Example of configuration:

Requirement: After overvoltage $\overline{ABE}$ is to be LOW;
After overvoltage a self-test is carried out by the ECU, afterwards $\overline{ABE}$ is deactivated.

Register STATCON_REG is set to $111xxxxx_b$ during driving cycle.
When $\overline{ABE}$ becomes active, overvoltage can be detected by reading out STATCON_REG.
After the ECU's self-test a reset condition is achieved by writing $110xxxxx_b$ into the register STATCON_REG. This reset is only possible after disappearance of the overvoltage condition because the set input is dominant. The reset signal is withdrawn by writing $111xxxxx_b$.


Block Diagram: VDD-Monitoring
VDD
ABE
100k
GND1,2
„L“ = Switch Off
Power Stages
Undervoltage
Reset
Set dominant
Glitch filter
„L“ = Undervoltage at VDD
„L“ = Overvoltage at VDD
GND_ABE
STATCON_REG
0 0 Test: Overvoltage Threshold
0 1 Test: Undervoltage Threshold
1 X default
VDD
GND_ABE

## 1.11 Notes for the Application in Commercial Vehicles

**For electric systems with 24V battery voltage, that can even increase to ≥ 37V in case of load dump, some peculiarities have to be observed!**

The static voltage at pin UBatt without destruction is limited to 37V, therefore this pin must either be connected to the 5V supply voltage VDD or else the voltage at pin UBatt has to be limited by adequate external circuitry. By connecting pin UBatt to VDD the values of $R_{ds,\ on}$ of the power switches will increase up to 20%.

The power stages 7...18 are equipped with a 40V active clamping. Therefore this power stages must only drive loads with an accordingly high resistance that can be switched on in case of overvoltage (e.g. a maximum load dump voltage of 60V and a load resistor of 1kΩ result in a power dissipation of 0.8W for each power stage. For all of the 12 power stages together there is a power dissipation of 9.6W for the typical duration of a load dump of 500ms.).

**The restrictions listed above are no longer relevant in case of a „overvoltage-protected battery voltage“within the 24V electric system that limits the voltage to e.g. a maximum of 37V.**

The thresholds of the currents, on which the power stages are switched off in case of overload, are increased by approximately 25% if there is a voltage at pin UBatt higher than19V (reason: jump start requirements in 12V electric systems). Exception: OUT9 and OUT10 and OUT15... OUT18. See characteristics in chapters 3.5.3, 3.6.3, 3.7.3 and 3.8.3.
The restrictions concerning overload of power stages (see 3.5.2, 3.6.2, 3.7.2 and 3.8.2) and permissible clamping energy (see 3.5.8, 3.6.8, 3.7.8 and 3.8.8) are relevant further on.

### 1.11.1 Notes for short circuit limitation

The power stages are short circuit protected for the following conditions:
The max. voltage at the output pins are limited to 36V and the TLE6244 is not operating in the booster mode.
The power stages will be switched on/off with a max. frequency of 1 kHz.
Only a 40 msec burst with the 1 kHz on/off-frequency is allowed, with a minimum burst repetition time of 1 sec. The maximum number of burst repetition cycles is 25. The number of driving cycles under these conditions is limited to 100 in lifetime. The temperature of the slug of the MQFP64 package must not exceed 130°C.
These limitations are valid for UBatt > 24 V.
For Ubatt ≤ 24 V the number of driving cycles under these conditions is extended to 1000 in lifetime.

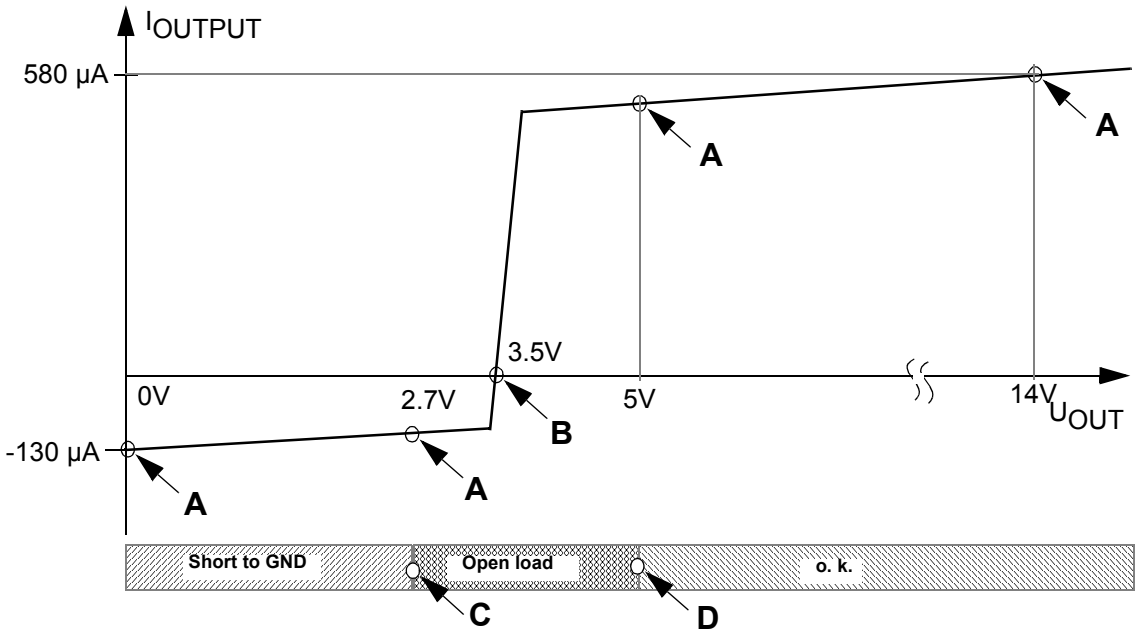
## 1.12 Notes for the Diagnostics

- SCB entry in DIA_REGx see diagrams in chapter 1.6.4.

- In case of overvoltage at pin VDD (VDD > 5,5V) the diagnostic information can be wrong. In that case, the diagnostic information has to be cleared with the DEL_DIA instruction.

- The filtering time restarts when the output voltage passes the diagnostic threshold for short to ground (SCG).

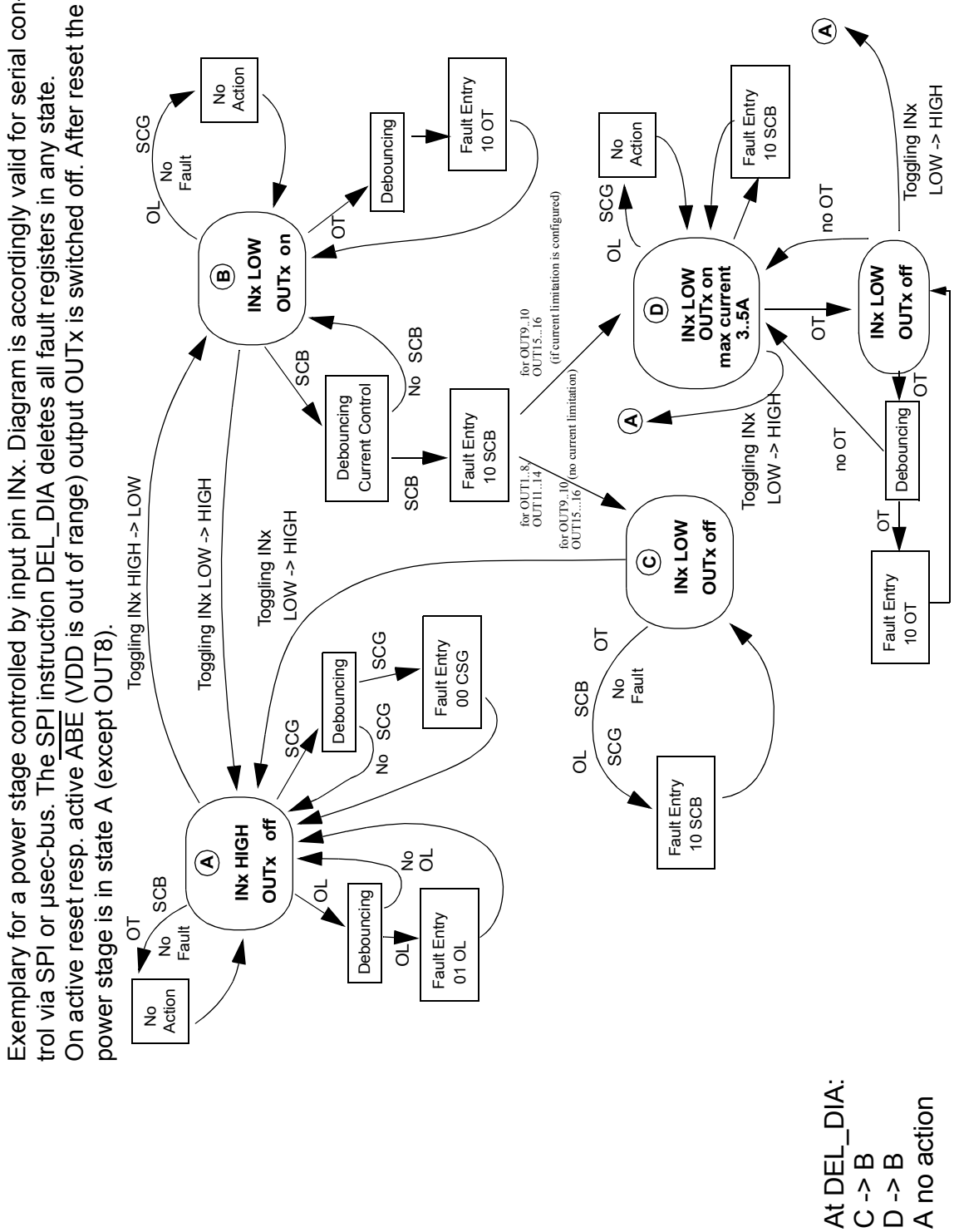
- Diagram of the typical diagnostic current:




A: Diagnostic current (see 3.11.3)
B: Bias Voltage Open Load (see3.11.2)
C: Short to GND Threshold (see 3.11.1.2)
D: Open load Threshold (see 3.11.1.1)

## State Diagram of the Power Stages Diagnostics

Exemplary for a power stage controlled by input pin INx. Diagram is accordingly valid for serial control via SPI or µsec-bus. The SPI instruction DEL_DIA deletes all fault registers in any state. On active reset resp. active $\overline{ABE}$ (VDD is out of range) output OUTx is switched off. After reset the power stage is in state A (except OUT8).



## 1.13 Parallel Connection of Power Stages

The power stages (PS) which are connected in parallel have to be switched on and off simultaneously. The corresponding SPI-Bits SCONx have to be in the same register (see page 15), when the PS are serial controlled via SPI.
In case of overload the ground current and the power dissipation are increasing. The application has to take into account that all maximum ratings are observed (e.g. operating temperature $T_J$ and total ground current $I_{GND}$, see page 36, 37).
Max. number of parallel connections: 3

**The following statements apply to PS within the same TLE6244X**

The max. short circuit shutdown threshold of the parallel connected PS is the summation of the corresponding max. values of the PS ($I_{SC,OUTx} + I_{SC,OUTy} + ....$).

| | Max. Nominal Current | Max. Clamping Energy | On Resistance |
|---|---|---|---|
| 2 symmetrical PS (see note 1) | $0.9 \times (I_{max,OUTx} + I_{max,OUTy})$ | $0.75 \times (E_{Cl,OUTx} + E_{Cl,OUTy})$ | $0.5 \times R_{on,OUTx,y}$ |
| 2 PS of the same type (see note 2) | $0.85 \times (I_{max,OUTx} + I_{max,OUTy})$ | $0.75 \times (E_{Cl,OUTx} + E_{Cl,OUTy})$ | $0.5 \times R_{on,OUTx,y}$ |
| 3 PS of the same type (see note 2) | $0,8 \times (I_{max,OUTx} + I_{max,OUTy} + I_{max,OUTz})$ | $0,58 \times (E_{Cl,OUTx} + E_{Cl,OUTy} + E_{Cl,OUTz})$ | $0.34 \times R_{on,OUTx,y,z}$ |
| 2 PS with the same nominal current, but different clamping voltage (application without free-wheeling-diode) (see note 3) | $0.7 \times (I_{max,OUTx} + I_{max,OUTy})$ | Clamping energy of the PS with the lower clamping voltage | $\frac{R_{on,OUTx} \times R_{on,OUTy}}{R_{on,OUTx} + R_{on,OUTy}}$ |
| 2 PS with the same nominal current, but different clamping voltage (application with free-wheeling-diode) (see note 3) | $0.7 \times (I_{max,OUTx} + I_{max,OUTy})$ | no clamping required | $\frac{R_{on,OUTx} \times R_{on,OUTy}}{R_{on,Ax} + R_{on,OUTy}}$ |
| 2 PS with the same clamping voltage, but different nominal current (see note 4) | $\text{Max}\left[\begin{array}{l} I_{max,OUTx} \\ I_{max,OUTy} \\ 0.75 \times (I_{max,OUTx} + I_{max,OUTy}) \end{array}\right]$ | $\text{Min}\left[\begin{array}{l} E_{Cl,OUTx} \\ E_{Cl,OUTy} \end{array}\right]$ | $\frac{R_{on,OUTx} \times R_{on,OUTy}}{R_{on,OUTx} + R_{on,OUTy}}$ |
| 2 PS with different nominal current and different clamping voltage (see note 5) | $\text{Max}\left[\begin{array}{l} I_{max,OUTx} \\ I_{max,OUTy} \end{array}\right]$ | Clamping energy of the PS with the lower clamping voltage | $\frac{R_{on,OUTx} \times R_{on,OUTy}}{R_{on,OUTx} + R_{on,OUTy}}$ |

note 1: For every PS there exists only one symmetrical PS
OUT1 and OUT2 are symmetrical PS.
OUT3 and OUT4 are symmetrical PS.
...
OUT17 and OUT18 are symmetrical PS.

note 2: PS of the same type have the same nominal current and the same clamping voltage

note 3: Parallel connection of PS-type 2,2A/45V with type 2,2A/70V

note 4: Parallel connection of PS-type 2,2A/45V with type 3.0A/45V or
Parallel connection of PS-type 1.1A/45V with type 2,2A/45V

note 5: Parallel connection of PS-type 2,2A/70V with type 1.1A/45V or
Parallel connection of PS-type 2,2A/70V with type 3.0A/45V

If the power stages are configured for static current limitation the max. current limitation of the parallel connected PS is the summation of the corresponding max. values of the PS ($I_{SC,OUTx}$ + $I_{SC,OUTy}$ +....).

**The following statements apply to Power Stages within different TLE6244X**

The application has to take into account that all maximum ratings of each TLE6244X are observed.

# 2. Maximum Ratings

## 2.1 Definition of Test Conditions

The integrated circuit must not be destroyed if maximum ratings are reached. Every maximum rating is allowed to reach, as far as no other maximum rating is exceeded.

Unless otherwise indicated all voltages are referred to GND (GND pins 1...8 connected to each other)

Positive current flows into the pin.

## 2.2 Test Coverage (TC) in Series Production

In the standard production flow not all parameters can be covered due to technical or economic reasons. Therefore the following test coverage was defined:

**A**) Parameter test
**B**) Go/NoGo test (in the course of release qualification/characterization: parameter test)
**C**) Guaranteed by design (covered by lab tests, not considered within the standard production flow)

## 2.3 Thermal Limits

**Operating temperature TLE6244**

| | |
|---|---|
| continuous | $-40°C \le T_J \le 150°C$ |
| additionally only for the power switches (for 100h accumulated) | $150°C \le T_J \le 200°C$ |
| **Storage temperature** | $-55°C \le T_C \le 125°C$ |
| **Thermal resistance** | $R_{thJC} \le 2{,}5$ K/W |

## 2.4 Electrical Limits

Limits must absolutely not be exceeded. By exceeding only one limit the integrated circuit might be destroyed.

**Power Supplies $U_{VDD}$ and $U_{UBatt}$**

| | |
|---|---|
| Static (without destruction) *) | $-0.3V \le U_{VDD} \le 36V$<br>$-0.3V \le U_{UBatt} \le 37V$ |
| Dynamic <10µsec (without destruction) | $-0.5V \le U_{VDD} \le 36V$<br>$-0.5V \le U_{UBatt} \le 40V$ |

Dynamic (500 ms, 10 x in lifetime, without destruction) $-0.5V \le U_{UBatt} \le 40V$

*) $U_{VDD} \ge 5.5V$ is allowed only in case of error conditions! Not suitable for continuous operation.

**SPI Output**

| | |
|---|---|
| Output voltage | $-0.3V \le U_{SO} \le 36V$ |

| | |
|---|---|
| Output current | $I_{SO} \leq 5mA$ |

**Outputs Low Side Switches**

| | | |
|---|---|---|
| Static voltage (without destruction) | OUT1...6 | ≤ 64V |
| | OUT7..18 | ≤ 40V |

Dynamic voltage without destruction after ISO/DIS7637-1, pulses 1 to 4

| | |
|---|---|
| OUT1 to 6, OUT9 to16: via external load (e.g. 2W lamp) | ≤ 2ms |
| OUT7, OUT8, OUT17 and OUT18: via external load | ≤ 2ms |

**Ground Current**

| | |
|---|---|
| Total current GND1+2 (pins 26/27)<br>(total ground current of OUT5,6,9,10,17,18) | $I_{GND1+2} \leq 18$ A |
| Total current GND3+4 (pins 58/59)<br>(total ground current of OUT1,2,7,8,11,12,15,16) | $I_{GND3+4} \leq 20$ A |
| Total current GND5+6 (pins 11/12)<br>(total ground current of OUT3,13) | $I_{GND5+6} \leq 6$ A |
| Total current GND7+8 (pins 41/42)<br>(total ground current of OUT4,14) | $I_{GND7+8} \leq 6$ A |

**Attention:** Even if all ground pins are connected with each other on the PCB the total ground currents $I_{GND1+2}$ and $I_{GND3+4}$ and $I_{GND5+6}$ and $I_{GND7+8}$ must not be exceeded.

The 4 ground pins GND1...4 are internally connected to the heat sink via an unspecified rivet joint. Therefore it is advisable to short-circuit the 4 ground pins on the PCB and to connect them with the heat sink. In addition the 4 ground pins GND5..8 must be connected to the other ground pins on the PCB

**Inputs of the Power Switches, SPI Inputs, Reset and Shut-off of the Power Stages**

| | |
|---|---|
| Input voltage | $-0.3V \leq U_{INi,\overline{RST},\overline{SS},SI,SCK,\overline{ABE}} \leq 36V$ |
| Input currents | see 3.4.4 , 3.9.1 , 3.9.2 , 3.9.3 , 3.13.2 |

**Pin $\overline{\text{RST}}$**

| | |
|---|---|
| Minimum reset duration (Power-On) | 15 ms |
| Input currents | see 3.4.4 |

## 3. Electrical Characteristics

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.1 Operating Range** (see also 3.13 VDD-monitoring $\overline{ABE}$) | Out of this range the power stages can be shut off by the VDD-monitoring except OUT8 | | | | | | |
| | Voltage referred to GND_$\overline{ABE}$ | | $U_{VDD}$ | 4.7 | | 5.3 | V |
| | Minimum reset duration (Power-On) | | $t_{\overline{RST},min}$ | 15 | | | ms |
| | Minimum reset duration in operation mode $4.5V \le U_{VDD} \le 5.5V$ | | $t_{\overline{RST},min}$ | 1 | | | µs |
| **3.2 Validity of Parameters** | Parameters are valid for $4.5V \le U_{VDD} \le 5.5V$, $4.5V \le U_{UBatt} \le 37V$ TLE6244: $-40°C \le T_J \le 150°C$ and 2 power stages in current limitation unless otherwise noted. If VDD-monitoring is active the power stages are switched off except OUT8 (see page 28). Positive current flows into the pin, negative current flows out of the pin. Unless otherwise noted all voltages are referred to GND (GND1...8 connected with each other). | | | | | | |
| | If the $U_{VDD}$ falls below this trashed the power stages (except OUT8) are switched off. If $U_{VDD}$ rises above this threshold the power stages work regularly after a delay time of 250 µsec. | | $U_{VDD}$ | 3.5 | 4.2 | 4.5 | V |
| | Threshold for shut off of OUT8: If $U_{VDD}$ rises above this threshold the power stages work regularly after a delay time of 250 µsec. | | $U_{VDD}$ | | | 3.5 | V |
| | Supply voltage | | $U_{VDD}$ | 4.5 | | 5.5 | V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.3 Power Consumption** | $U_{VDD} \leq 5.5V$ | A | $I_{VDD}$ | | | 20 | mA |
| | 5,5 V < UVDD < 36 V (IC is not destroyed) | C | $I_{VDD}$ | | | 50 | mA |
| | $U_{UBatt}$ = 14V | A | $I_{UBatt}$ | | | 3 | mA |
| | $U_{UBatt}$ = 28V | A | $I_{UBatt}$ | | | 4 | mA |
| | $U_{UBatt} \leq U_{VDD}$ | A | $I_{UBatt}$ | | | 1 | mA |
| | Power consumption in standby mode in case of missing $U_{VDD}$, $U_{UBatt} \leq 14V$ | A | $I_{UBatt}$ | | | 200 | µA |
| **3.4 Inputs of the Power Stages and Reset** IN1...IN16, $\overline{RST}$ | Outputs are switched off if inputs are open (parallel control). | | | | | | |
| **3.4.1 Low Level** | Reset not active, Power stage on for | B | $U_{\overline{RSTL}}$ | | | 1.0 | V |
| | i = 1...5, 9...15 | B | $U_{INiL}$ | | | 1.0 | V |
| | i = 6, 7, 16 | B | $U_{INiL}$ | | | 1.0 | V |
| | Power stage off for i = 8 | B | $U_{INiL}$ | | | 1.0 | V |
| **3.4.2 High Level** | Power stage off for | B | $U_{\overline{RSTH}}$ | 1.7 | | | V |
| | i = 1...7, 9...16 | B | $U_{INiH}$ | 2.0 | | | V |
| | | | | | | | V |
| | Power stage on for i = 8 | B | $U_{INiH}$ | 2.0 | | | V |
| **3.4.3 Hysteresis** | | C | $\Delta U_{INi}$, $\Delta U_{\overline{RST}}$ | 0.1 | | 0.6 | V |
| **3.4.4 Input Currents In, RST** | $-0.3V \leq U_{INi,\overline{RST}} \leq U_{VDD}$ (i = 1...7, 9...16) | A/B | $I_{INi,\overline{RST}}$ | -100 | | 5 | µA |
| | $U_{VDD} \leq U_{INi} \leq 36$ V (i = 1...7, 9...16) | C | $\|I_{INi}\|$ | | | 5 | µA |
| | $-0.3V \leq U_{IN8} \leq U_{VDD}$ | A/B | $I_{IN8}$ | -100 | | 100 | µA |
| | $0.8V \leq U_{IN8} \leq U_{VDD}$, pull down | A | $I_{IN8}$ | 20 | 40 | 100 | µA |
| | $U_{VDD} \leq U_{IN8} \leq 36$ V, pull down | C | $I_{IN8}$ | 20 | 40 | 100 | µA |
| | $0V \leq U_{\overline{RST}} \leq U_{VDD}$ - 1.7V, pull up | A | $-I_{\overline{RST}}$ | 20 | 40 | 100 | µA |
| | $0V \leq U_{INi} \leq U_{VDD}$ - 1.7V, pull up (i = 6,7,16) | A | $-I_{INi}$ | 5 | 10 | 20 | µA |
| | Bit BMUX = 1 (CONFIG_REG): $0V \leq U_{INi} \leq U_{VDD}$ - 1.7V, pull up (i = 1..5, 9..15) | A | $-I_{INi}$ | 20 | 40 | 100 | µA |
| | Bit BMUX = 0 (CONFIG_REG): $0V \leq U_{INi} \leq U_{VDD}$, high-impedance (i = 1..5, 9..15) | A | $\|I_{INi}\|$ | | | 1 | µA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.4.5 Input Protection INi** | Input clamping at INi (i = 1...16): No malfunction during clamping. | | | | | | |
| | Max. clamping current (externally limited) | | | | | | |
| | static | C | $\|I_{INi}\|$ | | | 2 | mA |
| | dynamic (t < 2ms) | C | $\|I_{INi}\|$ | | | 5 | mA |
| | Max. clamping voltage | | | | | | |
| | $I_{INi}$ = -5mA | C | $U_{INi}$ | -3 | | | V |
| | $I_{INi}$ = +2mA (t < 2ms) | C | $U_{INi}$ | 40 | | 70 | V |
| | External current limitation at INi is only provided if µsec-bus control is used. In that case INi are used as digital inputs. If µsec-bus is not used, there is no external resistor for current limitation. See 2.4 “Inputs of the Power Switches, SPI Inputs...” | | | | | | |
| **3.5 Power Outputs 2.2A/70V** OUT1...6 | In case of open input (parallel control) or missing power supply the power stage is switched off. Parallel connection of power stages is possible. | | | | | | |
| **3.5.1 Nominal Current** | | C | $I_{OUT1..6}$ | | | 2.2 | A |
| **3.5.2 Extended Current Range** | $I_{OUT1...6}$ > 2.2A | | | | | | |
| | Accumulated operating time | C | | | | 100 | h |
| **3.5.3 Maximum Current (Short Circuit Shut- down Threshold)** | 4.5V ≤ $U_{UBatt}$ ≤ 17V | | | | | | |
| | $T_J$ = -40°C | B | $I_{OUT1..6}$ | 2.4 | | 4.0 | A |
| | $T_J$ = 150°C | A | $I_{OUT1..6}$ | 2.2 | | 3.7 | A |
| | $U_{UBatt}$ ≥ 21V | | | | | | |
| | $T_J$ = -40°C | B | $I_{OUT1..6}$ | 3 | | 5.0 | A |
| | $T_J$ = 150°C | A | $I_{OUT1..6}$ | 2.7 | | 4.6 | A |
| | Above this limit short circuit to UBatt is detected. For the duration of the shutoff delay time $t_{Voff}$ (see 3.5.4) the output current is limited to approximately this value. If the short circuit condition is still present after $t_{Voff}$, the output is switched off. An error is stored after $t_{Diag}$ (see 3.11.4). | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Between -40°C and 150°C an approximately linear characteristic line can be assumed for the short circuit shutdown threshold.<br><br>Between 17V ≤ $U_{UBatt}$ ≤ 21V, the short circuit shutdown threshold is switched.<br><br>A power stage that is switched off in case of SCB can be switched on again by an off/on cycle at the corresponding input pin resp. by the change of the state of the corresponding SPI bit SCONx (see page 16), by the µsec-Bus, by a DEL_DIA instruction or can be released again by reset. If the fault register is cleared before this release (by a DEL_DIA instruction), a new fault entry of SCB is immediately carried out, even if SCB condition is no longer present. | | | | | | |
| 3.5.3.1 Maximum Battery Voltage at Short Circuit to Battery | See Note 1.11.1 | C | $U_{OUT}$ 1..6 | 36 | | | V |
| **3.5.4 Shutoff Delay** | Shutoff delay of the power stages after detection of SCB | B | $t_{Voff}$ | 60 | | 215 | µs |
| **3.5.5 On Resistance** | OUT1,2,5,6: $T_J$ = 25°C | A | $R_{on1,2,5,6}$ | 220 | 320 | 400 | mΩ |
| | OUT1,2,5,6: $T_J$ = 150°C | A | $R_{on1,2,5,6}$ | 420 | 600 | 750 | mΩ |
| | OUT1,2,5,6: $T_J$ = -40°C | A | $R_{on1,2,5,6}$ | 180 | 250 | 310 | mΩ |
| | OUT3,4: $T_J$ = 25°C | A | $R_{on3,4}$ | 210 | 300 | 380 | mΩ |
| | OUT3,4: $T_J$ = 150°C | A | $R_{on3,4}$ | 410 | 580 | 720 | mΩ |
| | OUT3,4: $T_J$ = -40°C | A | $R_{on3,4}$ | 170 | 240 | 300 | mΩ |
| | For $U_{UBatt}$ ≤ 10V $R_{on}$ is increased up to 20%. | | | | | | |
| **3.5.6 On/off Delay Times** | „On“ | B | $t_{don1...6}$ | | | 10 | µs |
| | | B | $t_{son1...6}$ | | | 5 | µs |
| | „Off“ | B | $t_{doff1...6}$ | | | 10 | µs |
| | (Measurement with ohmic load) | C | $t_{soff1...6}$ | | | 10 | µs |
| | $\|t_{don} - t_{doff}\|$ | C | $\Delta t_d$ | | | 5 | µs |
| | switch-on slew rate | C | $s_{on1...6}$ | | | 15 | V/µs |
| | switch-off slew rate | C | $s_{off1...6}$ | | | 21 | V/µs |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.5.7 Leakage Current** | $U_{VDD}$ = 0V, $U_{OUT1...6}$ = 14V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUT1..6}$ | | | 50 | µA |
| | $U_{VDD}$ = 0V, $U_{OUT1...6}$ = 24V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUT1..6}$ | | | 200 | µA |
| **3.5.8 Clamping** | | | | | | | |
| 3.5.8.1 Clamping Voltage | $I_{OUT1...6}$ = 0.2A | A | $U_{OUT1..6}$ | 64 | | 76 | V |
| 3.5.8.2 Matching of the Clamping Voltage | Between different outputs with identical inductive loads | A | ΔU | | | 3 | V |
| 3.5.8.3 Maximum Clamping Energy $T_C \leq 110°C$ | Linear decreasing current, $f_{max}$ = 50Hz (see diagrams E = f(I) on page 66) | | | | | | |
| | $I_{OUT1...6} \leq 2.2A$ | C | E | | | 8.5 | mJ |
| | $I_{OUT1...6} \leq 1.0A$ | C | E | | | 19 | mJ |
| | $I_{OUT1...6} \leq 0.5A$ | C | E | | | 30 | mJ |
| 3.5.8.4 Maximum Clamping Energy $T_C \leq 60°C$ | Linear decreasing current, $f_{max}$ = 50Hz | | | | | | |
| | $I_{OUT1...6} \leq 2.2A$ | C | E | | | 10.8 | mJ |
| | $I_{OUT1...6} \leq 1.0A$ | C | E | | | 22 | mJ |
| | $I_{OUT1...6} \leq 0.5A$ | C | E | | | 36 | mJ |
| 3.5.8.5 Maximum Clamping Energy with two Outputs connected in parallel | Each output 75% of the values of 3.5.8.3 resp. 3.5.8.4 | C | | | | | |
| 3.5.8.6 Maximum Clamping Energy at Load Dump | For a maximum of 10 times during ECU life (load dump with 400ms and $R_i$ = 2Ω over the load, e.g. 2W lamp) | C | E | | | 50 | mJ |
| 3.5.8.7 Jump Start | Each output 150% of the values of 3.5.8.4. For a maximum of 10 jump starts of 2 minutes each during ECU life. | C | | | | | |
| 3.5.8.8 Singlepulse $T_C \leq 60°C$ | $I_{OUT1...6} \leq 0.6A$, max 10 000 pulse | C | E | | | 50 | mJ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.6 Power outputs 2.2A/45V**<br>OUT9...OUT14 | In case of open input (parallel control) or missing power supply the power stage is switched off. Parallel connection of power stages is possible. | | | | | | |
| **3.6.1 Nominal Current** | | C | $I_{OUT9...14}$ | | | 2.2 | A |
| **3.6.2 Extended Current Range** | $I_{OUTi}$ > 2.2A | | | | | | |
| | Accumulated operating time | C | | | | 100 | h |
| **3.6.3 Maximum Current (Short Circuit Shut down Threshold)** | 4.5V ≤ $U_{UBatt}$ ≤ 17V for OUT11..14<br>4.5V ≤ $U_{UBatt}$ for OUT9/10 | | | | | | |
| | $T_J$ = -40°C | B | $I_{OUTi}$ | 2.4 | | 3.8 | A |
| | $T_J$ = 150°C | A | $I_{OUTi}$ | 2.2 | | 3.7 | A |
| | $U_{UBatt}$ > 21V for OUT11...14 | | | | | | |
| | $T_J$ = -40°C | B | $I_{OUTi}$ | 3 | | 5 | A |
| | $T_J$ = 150°C | A | $I_{OUTi}$ | 2.7 | | 4.6 | A |
| | **For OUT11... OUT14**<br>Above this limit short circuit to UBatt is detected. For the duration of the shutoff delay time $t_{Voff}$ (see 3.6.4) the output current is limited to approximately this value. If the short circuit condition is still present after $t_{Voff}$, the outputs OUT11...OUT14 are switched off. An error is stored after $t_{Diag}$ (see 3.11.4).<br>The same is true for OUT9, OUT10 if the static current limitation is not enabled. | | | | | | |
| | Between -40°C and 150°C an approximately linear characteristic line can be assumed. | | | | | | |
| | Between 17V ≤ $U_{UBatt}$ ≤ 21V, the short circuit shutdown threshold is switched for OUT11..14 | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | A power stage that is switched off in case of SCB can be switched on again by an off/on cycle at the corresponding input pin resp. by the change of the state of the corresponding bit for SPI or µsec-bus by a DEL_DIA instruction or can be released again by reset. If the fault register is cleared before this release (by a DEL_DIA instruction), a new fault entry of SCB is immediately carried out, even if SCB condition is no longer present.<br>**For OUT9, OUT10**<br>Above this limit short circuit to UBatt is detected. The output current is limited to approximately this value if the static current limitation is configured. An error is stored after $t_{Diag}$ (see 3.11.4). If the operation leads to an overtemperature condition, a second protection level (about 170°C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures<br>Between -40°C and 150°C an approximately linear characteristic line can be assumed. | | | | | | |
| 3.6.3.1 Maximum Battery Voltage at Short Circuit to Battery | See Note 1.11.1 | C | $U_{OUT}$ 9..14 | 36 | | | V |
| **3.6.4 Shutoff Delay** | Shutoff delay of the power stages after detection of KSUB. For the duration of $t_{Voff}$ current is limited to maximum current. | B | $t_{Voff}$ | 60 | | 215 | µs |
| **3.6.5 On Resistance** | $T_J$ = 25°C<br>$T_J$ = 150°C<br>$T_J$ = -40°C<br>For $U_{UBatt} \leq$ 10V $R_{on}$ is increased up to 20%. | A<br>A<br>A | $R_{on9-14}$<br>$R_{on9-14}$<br>$R_{on9-14}$ | 200<br>380<br>150 | 300<br>550<br>220 | 380<br>680<br>280 | mΩ<br>mΩ<br>mΩ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.6.6 On /off Delay Times** | „On“ | B | $t_{don}$ | | | 10 | µs |
| | | B | $t_{son}$ | | | 5 | µs |
| | „Off“ | B | $t_{doff}$ | | | 10 | µs |
| | (Measurement with ohmic load) | C | $t_{soff}$ | | | 10 | µs |
| | $\|t_{don} - t_{doff}\|$ | C | $\Delta t_d$ | | | 5 | µs |
| | switch-on slew rate | C | $s_{on}$ | | | 20 | V/µs |
| | switch-off slew rate | C | $s_{off}$ | | | 25 | V/µs |
| **3.6.7 Leakage Current** | $U_{VDD}$ = 0V, $U_{OUT9...14}$ = 14V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUTi}$ | | | 50 | µA |
| | $U_{VDD}$ = 0V, $U_{OUT9...14}$ = 24V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUTi}$ | | | 200 | µA |
| **3.6.8 Clamping** | | | | | | | |
| 3.6.8.1 Clamping Voltage | $I_{OUTi}$ = 0.2A | A | $U_{9...14}$ | 40 | 45 | 50 | V |
| 3.6.8.2 Maximum Clamping Energy $T_C \leq 110°C$ | Linear decreasing current, $f_{max}$ = 30Hz (see diagrams E = f(I) on page 66) | | | | | | |
| | $I_{OUT9...14} \leq 2.2A$ | C | E | | | 14 | mJ |
| | $I_{OUT9...14} \leq 1.0A$ | C | E | | | 30 | mJ |
| 3.6.8.3 Maximum Clamping Energy $T_C \leq 60°C$ | Linear decreasing current, $f_{max}$ = 30Hz | | | | | | |
| | $I_{OUT9...14} \leq 2.2A$ | C | E | | | 17 | mJ |
| | $I_{OUT9...14} \leq 1.0A$ | C | E | | | 36 | mJ |
| 3.6.8.4 Maximum Clamping Energy with two Outputs connected in parallel | Each output 75% of the values of 3.6.8.2 resp. 3.6.8.3. | C | | | | | |
| 3.6.8.5 Maximum Clamping Energy at Load Dump | For a maximum of 10 times during ECU life (load dump with 400ms and $R_i$ = 2Ω over the load, e.g. 2W lamp) | C | E | | | 50 | mJ |
| 3.6.8.6 Jump Start | Each output 150% of the values of 3.6.8.3. For a maximum of 10 jump starts of 2 minutes each during ECU life. | C | | | | | |
| 3.6.8.7 Single pulse $T_C \leq 60°C$ | $I_{OUT9...14} \leq 0.6A$, max 10 000 pulse | C | E | | | 50 | mJ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.7 Power outputs 3.0A/45V**<br>OUT15...OUT16 | In case of open input (parallel control) or missing power supply the power stage is switched off. Parallel connection of power stages is possible. | | | | | | |
| **3.7.1 Nominal Current** | | C | $I_{OUT15}$<br>$I_{OUT16}$ | | | 3.0 | A |
| **3.7.2 Extended Current Range** | $I_{OUT15,16}$ > 3.0A | | | | | | |
| | Accumulated operating time | C | | | | 100 | h |
| **3.7.3 Maximum Current (Short Circuit Shut down threshold)** | $U_{UBatt} \geq 4.5V$<br>$T_J$ = -40°C<br>$T_J$ = 150°C | B<br>A | $I_{OUT15}$<br>$I_{OUT16}$ | 3.3<br>3 | | 6<br>5.5 | A<br>A |
| | Above this limit short circuit to UBatt is detected. For the duration of the shutoff delay time $t_{Voff}$ (see 3.6.4) the output current is limited to approximately this value. If the short circuit condition is still present after $t_{Voff}$, the outputs OUT15/16 are switched off if the static current limitation is not enabled. An error is stored after $t_{Diag}$ (see 3.11.4). | | | | | | |
| | Above this limit short circuit to UBatt is detected. The output current is limited to approximately this value if the static current limitation is configured. An error is stored after $t_{Diag}$ (see 3.11.4). If the operation leads to an overtemperature condition, a second protection level (about 170°C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures. | | | | | | |
| | Between -40°C and 150°C an approximately linear characteristic line can be assumed. | | | | | | |
| 3.7.3.1 Maximum Battery Voltage at Short Circuit to Battery | See Note 1.11.1 | C | $U_{OUT}$ 15,16 | 36 | | | V |
| **3.7.4 Shuttoff Delay** | Shutoff delay of the power stages after detection of SCB. For the duration of $t_{Voff}$ current is limited to maximum current. | B | $t_{Voff}$ | 60 | | 215 | µs |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.7.5 On Resistance** | $T_J$ = 25°C: | A | $R_{on15,16}$ | 150 | 220 | 280 | mΩ |
| | $T_J$ = 150°C: | A | $R_{on15,16}$ | 270 | 390 | 480 | mΩ |
| | $T_J$ = -40°C: | A | $R_{on15,16}$ | 120 | 170 | 210 | mΩ |
| | For $U_{UBatt} \leq$ 10V $R_{on}$ is increased up to 20%. | | | | | | |
| **3.7.6 On /off Delay Times** | „On“ | B | $t_{don}$ | | | 10 | µs |
| | | B | $t_{son}$ | | | 5 | µs |
| | „Off“ | B | $t_{doff}$ | | | 10 | µs |
| | (Measurement with ohmic load) | C | $t_{soff}$ | | | 10 | µs |
| | $\|t_{don} - t_{doff}\|$ | C | $\Delta t_d$ | | | 5 | µs |
| | switch-on slew rate | C | $s_{on}$ | | | 20 | V/µs |
| | switch-off slew rate | C | $s_{off}$ | | | 25 | V/µs |
| **3.7.7 Leakage Current** | $U_{VDD}$ = 0V, $U_{OUT15,16}$ = 14V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUT15,16}$ | | | 50 | µA |
| | $U_{VDD}$ = 0V, $U_{OUT15,16}$ = 24V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUT15,16}$ | | | 200 | µA |
| **3.7.8 Clamping** | | | | | | | |
| 3.7.8.1 Clamping Voltage | $I_{OUT15,16}$ = 0.2A | | $U_{OUT15,16}$ | 40 | 45 | 50 | V |
| 3.7.8.2 Maximum Clamping Energy $T_C \leq$ 110°C | Linear decreasing current, $f_{max}$ = 30Hz (see diagrams E = f(I) on page 67) | | | | | | |
| | $I_{OUT15,16} \leq$ 3.0A | C | E | | | 18 | mJ |
| | $I_{OUT15,16} \leq$ 2.2A | C | E | | | 20 | mJ |
| | $I_{OUT15,16} \leq$ 1.5A | C | E | | | 24 | mJ |
| | $I_{OUT15,16} \leq$ 1.0A | C | E | | | 40 | mJ |
| 3.7.8.3 Maximum Clamping Energy $T_C \leq$ 60°C | Linear decreasing current, $f_{max}$ = 30Hz | | | | | | |
| | $I_{OUT15,16} \leq$ 3.0A | C | E | | | 20 | mJ |
| | $I_{OUT15,16} \leq$ 1.0A | C | E | | | 46 | mJ |
| 3.7.8.4 Maximum Clamping Energy with two Outputs connected in parallel | Each output 75% of the values of 3.7.8.2 resp. 3.7.8.3. | C | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3.7.8.5 Maximum Clamping Energy at Load Dump | For a maximum of 10 times during ECU life (load dump with 400ms and $R_i$ = 2Ω over the load, e.g. 2W lamp) | C | E | | | 50 | mJ |
| 3.7.8.6 Jump Start | Each output 150% of the values of 3.7.8.3.<br>For a maximum of 10 jump starts of 2 minutes each during ECU life. | C | | | | | |
| 3.7.8.7 Single pulse $T_C \leq 60°C$ | $I_{OUT15,\ 16} \leq 0.6A$, max 10 000 pulses | C | E | | | 50 | mJ |
| **3.8 Power Outputs 1.1A/45V** OUT7,8, OUT17,18 | In case of open input (parallel control) or missing power supply the power stage is switched off. Parallel connection of power stages is possible. | | | | | | |
| **3.8.1 Nominal Current** | for OUT7, 8, 17, 18 | C | $I_{OUTi}$ | | | 1.1 | A |
| **3.8.2 Extended Current Range** | $I_{OUT7,8,17,18}$ > 1.1A | | | | | | |
| | Accumulated operating time | C | | | | 100 | h |
| **3.8.3 Maximum Current (Short Circuit Shut down Threshold and static current limitation)** | 4.5V ≤ $U_{UBatt}$ ≤ 17V for OUT7, 8<br>4.5V ≤ $U_{UBatt}$ for OUT17,18 | | | | | | |
| | $T_J$ = -40°C<br>$T_J$ = 150°C | B<br>A | $I_{OUTi}$<br>$I_{OUTi}$ | 1.2<br>1.1 | | 2.2<br>2.0 | A<br>A |
| | $U_{UBatt}$ > 21V only for OUT7,8<br>$T_J$ = -40°C<br>$T_J$ = 150°C | B<br>A | $I_{OUTi}$<br>$I_{OUTi}$ | 1.5<br>1.3 | | 2.5<br>2.3 | A<br>A |
| | **For OUT7, OUT8**<br>Above this limit short circuit to UBatt is detected. For the duration of the shutoff delay time $t_{Voff}$ (see 3.8.4) the output current is limited to approximately this value. If the short circuit condition is still present after $t_{Voff}$, the outputs OUT7/8 are switched off. An error is stored after $t_{Diag}$ (see 3.11.4). The same is true for OUT17 OUT18 if the static current limitation is not enabled. | | | | | | |

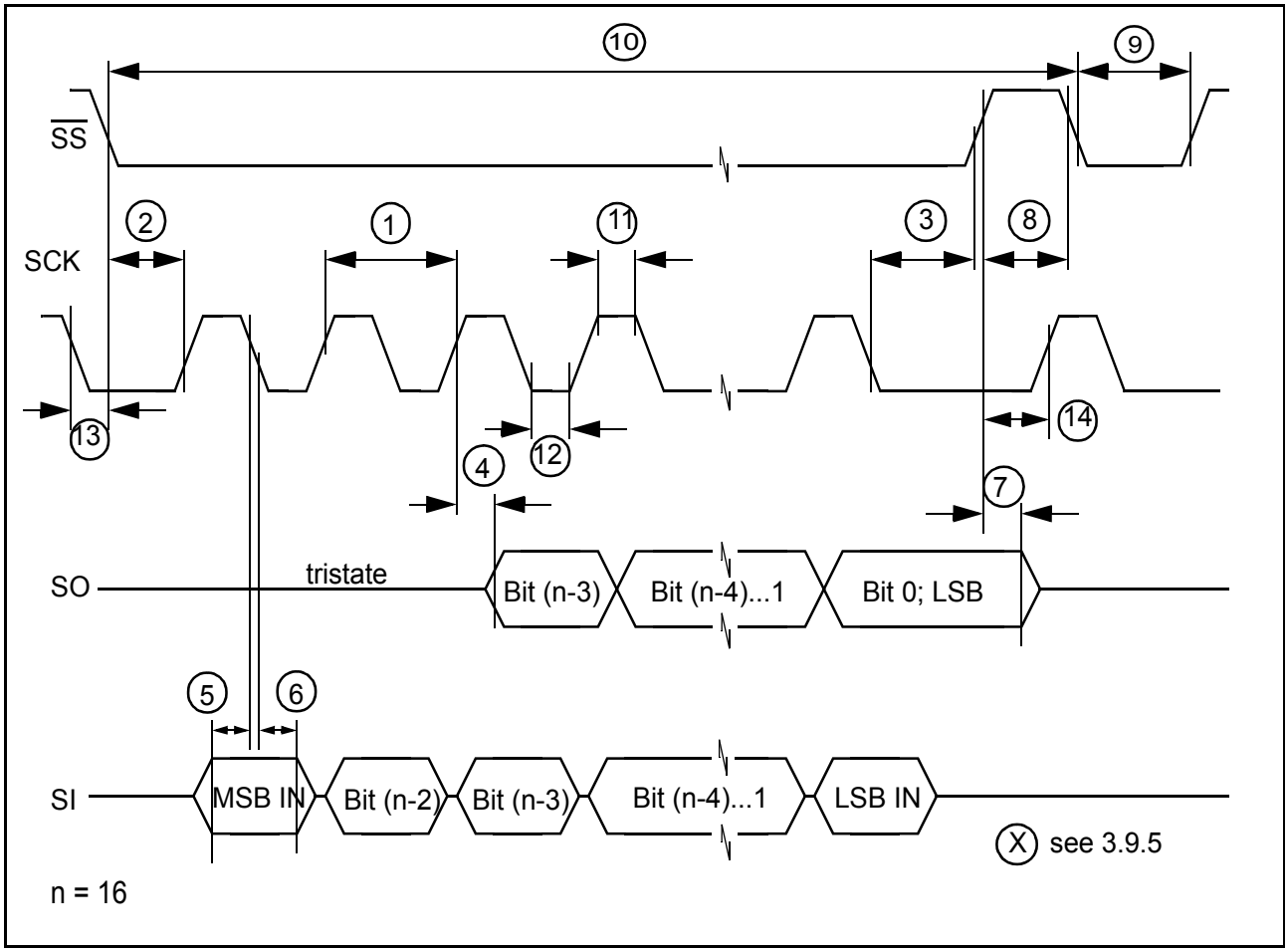
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Between -40°C and 150°C an approximately linear characteristic line can be assumed.<br><br>Between 17V ≤ $U_{UBatt}$ ≤ 21V, the short circuit shutdown threshold is switched for OUT7/8<br><br>A power stage that is switched off in case of SCB can be switched on again by an off/on cycle at the corresponding input pin resp. by the change of the state of the corresponding bit for SPI or µsec-bus by a DEL_DIA instruction or can be released again by reset. If the fault register is cleared before this release (by a DEL_DIA instruction), a new fault entry of SCB is immediately carried out, even if SCB condition is no longer present.<br><br>**For OUT17, OUT18**<br>Above this limit short circuit to UBatt is detected. The output current is limited to approximately this value if the static current limitation is configured. An error is stored after $t_{Diag}$ (see 3.11.4). If the operation leads to an overtemperature condition, a second protection level (about 170°C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures<br><br>Between -40°C and 150°C an approximately linear characteristic line can be assumed. | | | | | | |
| 3.8.3.1 Maximum Battery Voltage at Short Circuit to Battery | See Note 1.11.1 | C | $U_{OUT}$ 17,18 | 36 | | | V |
| **3.8.4 Shutoff Delay** | Shutoff delay of the power stages after detection of SCB. For the duration of $t_{Voff}$ current is limited to maximum current. | B | $t_{Voff}$ | 60 | | 215 | µs |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.8.5 On Resistance** | $T_J$ = 25°C | A | $R_{on7,8,17,18}$ | 400 | 620 | 780 | mΩ |
| | $T_J$ = 150°C | A | $R_{on7,8,17,18}$ | 780 | 1200 | 1500 | mΩ |
| | $T_J$ = -40°C | A | $R_{on7,8,17,18}$ | 290 | 450 | 560 | mΩ |
| | For $U_{UBatt} \leq$ 10V $R_{on}$ is increased up to 20%; condition: $U_{VDD}$ > 4.5 V | | | | | | |
| | For OUT8 only: 3.5V<($U_{VDD}$, $U_{UBatt}$)<4.5V | | | | | | |
| | $T_J$ = 25°C | A | $R_{on}$ | | | 1300 | mΩ |
| | $T_J$ = 150°C | A | $R_{on}$ | | | 2200 | mΩ |
| | $T_J$ = -40°C | A | $R_{on}$ | | | 1050 | mΩ |
| **3.8.6 On/off Delay Times** | „On“ | B | $t_{don}$ | | | 10 | µs |
| | | B | $t_{son}$ | | | 5 | µs |
| | „Off“ | B | $t_{doff}$ | | | 10 | µs |
| | (Measurementwithohmicload) | C | $t_{soff}$ | | | 10 | µs |
| | $\|t_{don} - t_{doff}\|$ | C | $\Delta t_d$ | | | 5 | µs |
| | Switch-on slew rate | C | $s_{on}$ | | | 25 | V/µs |
| | Switch-off slew rate | C | $s_{off}$ | | | 40 | V/µs |
| **3.8.7 Leakage Current** | For OUT7,8, OUT1718: | | | | | | |
| | $U_{VDD}$ = 0V, $U_{OUTi}$ = 14V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUTi}$ | | | 50 | µA |
| | $U_{VDD}$ = 0V, $U_{OUTi}$ = 24V (leakage current of the DMOS, diagnostic current = 0) | A | $I_{OUTi}$ | | | 200 | µA |
| **3.8.8 Clamping** | For OUT7,8, OUT17,18: | | | | | | |
| 3.8.8.1 Clamping Voltage | $I_{OUTi}$ = 0.2A | A | $U_{OUTi}$ | 40 | 45 | 50 | V |
| 3.8.8.2 Maximum Clamping Energy $T_C \leq$ 110°C | Linear decreasing current, $f_{max}$ = 10Hz (see diagrams E = f(I) on page 67) | | | | | | |
| | $I_{OUTi} \leq$ 0.6A | C | E | | | 10 | mJ |
| | $I_{OUTi} \leq$ 1.1A | C | E | | | 7 | mJ |
| 3.8.8.3 Maximum Clamping Energy $T_C \leq$ 60°C | Linear decreasing current, $f_{max}$ = 10Hz | | | | | | |
| | $I_{OUTi} \leq$ 0.6 | C | E | | | 12 | mJ |
| | $I_{OUTi} \leq$ 1.1A | C | E | | | 8.5 | mJ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3.8.8.4 Maximum Clamping Energy with two Outputs connected in parallel | Each output 75% of the values of 3.8.8.2 resp. 3.8.8.3. | C | | | | | |
| 3.8.8.5 Maximum Clamping Energy at Load Dump | For a maximum of 10 times during ECU life (load dump with 400ms and $R_i$ = 2Ω over the load) | C | E | | | 15 | mJ |
| 3.8.8.6 Jump Start | Each output 150% of the values of 3.8.8.3.<br>For a maximum of 10 jump starts of 2 minutes each during ECU life | C | | | | | |

### 3.9 SPI Interface

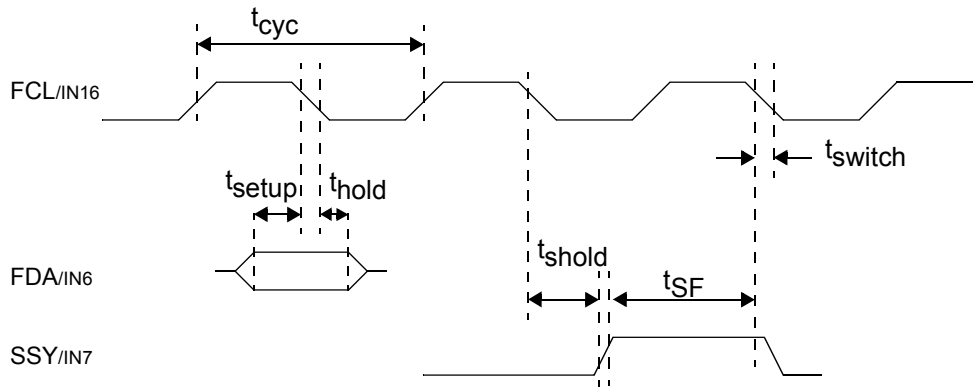
The timing of TLE6244X is defined as follows:
- The change at output (SO) is forced by the rising edge of the SCK signal.
- The input signal (SI) is sampled on the falling edge of the SCK signal.
- The data received during a writing access is taken over into the internal registers on the rising edge of the $\overline{SS}$ signal, if exactly 16 SPI clocks have been counted during $\overline{SS}$ = active.
(**Also:** Only if exactly 16 SPI clocks have been counted the instruction DEL_DIA resets the diagnostic registers.)



| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.9.1 Input SCK** | SPI clock input | | | | | | |
| 3.9.1.1 Low Level | | B | $U_{SCKL}$ | | | 1.0 | V |
| 3.9.1.2 High Level | | B | $U_{SCKH}$ | 2.0 | | | V |
| 3.9.1.3 Hysteresis | | C | $\Delta U_{SCK}$ | 0.1 | | 0.6 | V |
| 3.9.1.4 Input Capacity | | C | $C_{SCK}$ | | | 10 | pF |
| 3.9.1.5 Input Current | Pull up current source connected to VDD | A | $-I_{SCK}$ | 10 | 20 | 50 | µA |
| **3.9.2 Input $\overline{SS}$** | Slave select signal | | | | | | |
| 3.9.2.1 Low Level | TLE6244X is selected | B | $U_{SSL}$ | | | 1.0 | V |
| 3.9.2.2 High Level | | B | $U_{SSH}$ | 2.0 | | | V |
| 3.9.2.3 Hysteresis | | C | $\Delta U_{SS}$ | 0.1 | | 0.6 | V |
| 3.9.2.4 Input Capacity | | C | $C_{SS}$ | | | 10 | pF |
| 3.9.2.5 Input Current | Pull up current source connected to VDD | A | $-I_{SS}$ | 10 | 20 | 50 | µA |
| **3.9.3 Input SI** | SPI data input | | | | | | |
| 3.9.3.1 Low Level | | B | $U_{SIL}$ | | | 1.0 | V |
| 3.9.3.2 High Level | | B | $U_{SIH}$ | 2.0 | | | V |
| 3.9.3.3 Hysteresis | | C | $\Delta U_{SI}$ | 0.1 | | 0.6 | V |
| 3.9.3.4 Input Capacity | | C | $C_{SI}$ | | | 10 | pF |
| 3.9.3.5 Input Current | Pull up current source connected to VDD | A | $-I_{SI}$ | 10 | 20 | 50 | µA |
| **3.9.4 Output SO** | Tristate output of the TLE6244X (SPI output); On active reset ($\overline{RST}$) output SO is in tristate. | | | | | | |
| 3.9.4.1 Low Level | $I_{SO}$ = 2mA | A | $U_{SOL}$ | | | 0.4 | V |
| 3.9.4.2 High Level | $I_{SO}$ = -2mA | A | $U_{SOH}$ | $U_{VDD}$ - 1.0 | | | V |
| 3.9.4.3 Capacity | Capacity of the pin in tristate | C | $C_{SO}$ | | | 10 | pF |
| 3.9.4.4 Leakage Current | In tristate | A | $I_{SO}$ | -10 | | 10 | µA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.9.5 Timing** | 1. Cycle-Time (referred to master) | B | $t_{cyc}$ | 200 | | | ns |
| | 2. Enable Lead Time (referred to master) | C | $t_{lead}$ | 100 | | | ns |
| | 3. Enable Lag Time (referred to master) | C | $t_{lag}$ | 150 | | | ns |
| | 4. Data Valid CL = 50pF (5 MHz)<br>Data Valid CL = 200pF (2MHz) (referred to TLE6244X) | C<br>C | $t_v$<br>$t_v$ | | | 100<br>150 | ns<br>ns |
| | 5. Data Setup Time (referred to master) | C | $t_{su}$ | 50 | | | ns |
| | 6. Data Hold Time (referred to master) | C | $t_h$ | 20 | | | ns |
| | 7. Disable Time (referred to TLE6244X) | C | $t_{dis}$ | | | 100 | ns |
| | 8. Transfer Delay (referred to master) | C | $t_{dt}$ | 150 | | | ns |
| | 9. Select time (referred to master) | C | $t_{sel}$ | 50 | | | nsec |
| | 10. Access time (referred to master) | C | $t_{acc}$ | 8.35 | | | µsec |
| | 11. Serial clock high time (referred to master) | C | $t_{SCKH}$ | 50 | | | ns |
| | 12. Serial clock low time | C | $t_{SCKL}$ | 120 | | | ns |
| | 13. Disable Lead Time | C | $t_{dld}$ | 250 | | | ns |
| | 14. Disable Lag Time | C | $t_{dlg}$ | 250 | | | ns |

## 3.10 µsec-bus



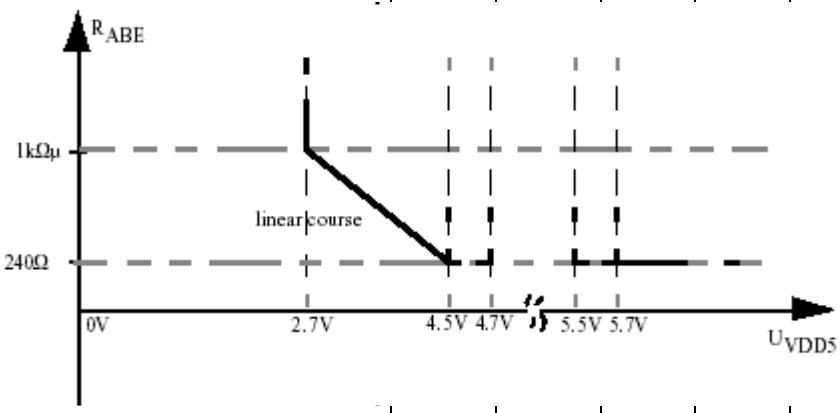

**Timing µsec-bus**

Notes for the timing:
Timing definitions are starting or ending at a voltage level of 1V (Low Level) resp. 2V (High Level).
During SSY = high the clock at FCL may be interrupted, i.e. there is no need for a clock during SSY = high.
The clock signal may remain on high or low statically during SSY = high.
A rising edge at SSY and a falling edge at FCL must not occur simultaneously!
On the rising edge of SSY the 16 bits clocked in TLE6244X by the last 16 falling edges at FCL are latched.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.10.1 Input FCL, FDA, SSY** | µsec-bus interface pins | | | | | | |
| 3.10.1.1 Low Level | | B | $U_{FCLl}$ $U_{FDAl}$ $U_{SSYl}$ | | | 1.0 | V |
| 3.10.1.2 High Level | | B | $U_{FCLh}$ $U_{FDAh}$ $U_{SSYh}$ | 2.0 | | | V |
| 3.10.1.3 Hysteresis | | C | $\Delta U_{FCL}$ $\Delta U_{FDA}$ $\Delta U_{SSY}$ | 0.1 | | 0.6 | V |
| 3.10.1.4 Input Capacity | | C | $C_{FCL}$ $C_{FDA}$ $C_{SSY}$ | | | 10 | pF |
| 3.10.1.5 Input Current | Pull up current source connected to VDD | A | $I_{FCL}$ $I_{FDA}$ $I_{SSY}$ | 5 | 10 | 20 | µA |
| **3.10.2 Timing** | Cycle Time | C | $t_{CYC}$ | 62 | | | nsec |
| | Data setup time | C | $t_{setup}$ | 10 | | | nsec |
| | Data hold time | C | $t_{hold}$ | 10 | | | nsec |
| | Switching time on FCL $f_{FCL}$ < 10MHz | C | $t_{switch}$ | | | 30 | nsec |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Switching time on FCL<br>$f_{FCL}$ > 10MHz | C | $t_{switch}$ | | | 8 | nsec |
| | Select hold time | C | $t_{shold}$ | 25 | | 10 | nsec |
| | FCL Low time<br>FCL High time | C<br>C | tFCLL<br>tFCLH | 25<br>25 | | | nsec |
| | SSY Low time<br>SSY High time | C<br>C | tSSYL<br>tSSYH | 25<br>25 | | | nsec |
| | Time between rising edge of SSY and next falling edge of FCL | C | tSF | 8 | | | nsec |
| **3.11 Diagnostics** | | | | | | | |
| **3.11.1 Diagnostic Thresholds Power Stages** | | | | | | | |
| 3.11.1.1 Open Load (OL) | Output turned off | B | $U_{OUT1..18}$ | $U_{VDD}$ - 0.5V | $U_{VDD}$ | $U_{VDD}$ + 0.5V | V |
| 3.11.1.2 Short to Ground (SCG) | Output turned off | B | $U_{OUT1...18}$ | 0.54 * $U_{VDD}$ - 0.5V | 0.54 * $U_{VDD}$ | 0.54 * $U_{VDD}$ + 0.5V | V |
| 3.11.1.3 Short to Battery (SCB) | See 3.5.3, 3.6.3, 3.7.3, 3.8.3 | | | | | | |
| 3.11.1.4 Overtemperature | Output turned on<br>Individually for each stage | B | $T_J$ | 150 | | | °C |
| **3.11.2 Bias Voltage Open Load Power Stages** | Output turned off, $I_{OUT1...18}$ = 0 | A | $U_{OUT1...18}$ | 0.6 * $U_{VDD}$ | 0.7 * $U_{VDD}$ | 0.76* $U_{VDD}$ | V |
| **3.11.3 Diagnostic Currents Power Stages** | 4.5V ≤ $U_{VDD}$ ≤ 5.5V, output turned off | | | | | | |
| | $U_{OUT1...18}$ = 14V (diagnostic current incl. leakage current) | A | $I_{OUT}$ | 270 | 580 | 980 | µA |
| | $U_{OUT1...18}$ = 0V | A | $-I_{OUT}$ | 50 | 130 | 250 | µA |
| | $U_{OUT1...18}$ = OL-Threshold | C | $I_{OUT}$ | 220 | | 980 | µA |
| | $U_{OUT1...18}$ = SCG-Threshold | C | $-I_{OUT}$ | 40 | | 250 | µA |

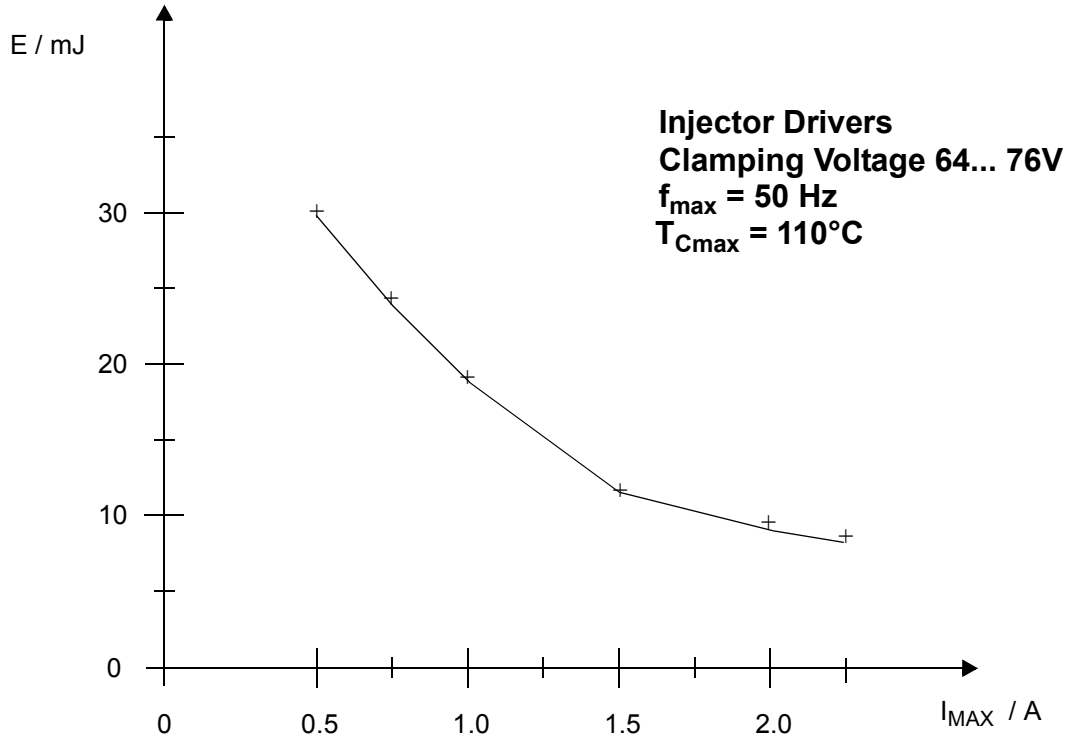
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.11.4 Filtering Time Power Switches** | Time from occurrence of one of the errors 'short to ground', 'open load' or 'short to battery' until the fault is entered into the corresponding diagnostic register. | B | $t_{Diag}$ | 60 | | 240 | µs |
| | Time from occurrence of OT until the information is entered into the corresponding diagnostic register. | C | $t_{DiatOT}$ | 3 | | 30 | µs |
| **3.11.5 Diagnostic Threshold UBatt** | Bit Ubatt in DIA_REG5 | | $U_{th,UB}$ | 1 | | 9 | V |
| **3.12 Reverse Currents** | $U_{VDD} \leq 1V$ | | | | | | |
| **3.12.1 Reverse Current at OUT1...18 without Supply Voltage** | Static | C | $-I_{O1...6}$ | 3 | | | A |
| | | C | $-I_{O9...16}$ | 3 | | | A |
| | | C | $-I_{O7,8}$ | 0.8 | | | A |
| | | C | $-I_{O17,18}$ | 0.8 | | | A |
| | Dynamic (Test pulse 1 according to ISO: 100V, $R_i$ = 10W, 2ms) | C | $-I_{O1...6}$ | 10 | | | A |
| | | C | $-I_{O9...16}$ | 10 | | | A |
| | | C | $-I_{O7,8}$ | 1.5 | | | A |
| | | C | $-I_{O17,18}$ | 1.5 | | | A |
| **3.12.2 Reverse Current at OUT1...OUT18 in Operation Mode** | $4.5V \leq U_{VDD} \leq 5.5V$ Pulsed power stage. Neighboring stages, reset, input signals of the power stages, VDD-monitoring, SPI interface (incl. registers) and µsec-bus must not be disturbed. Diagnostics of fault conditions at neighboring stages is still possible. Control bits in the SPI registers (serial control of power stages are not disturbed). | | | | | | |
| | Open load failure at neighboring stages may be detected as short to ground | C | $-I_{O1...16}$ | 1 | | | A |
| | | C | $-I_{O7,8}$ | 0.3 | | | A |
| | | C | $-I_{O17,18}$ | 0.3 | | | A |
| | Open load failure at neighboring stages **are not** detected as short to ground | C | $-I_{O1...4}$ | 0.5 | | | A |
| | | C | $-I_{O5...16}$ | 0.25 | | | A |
| | | C | $-I_{O7,8}$ | 0.3 | | | A |
| | | C | $-I_{O17,18}$ | 0.3 | | | A |
| | Destruction limit | C | $-I_{O1...6}$ | 3 | | | A |
| | | C | $-I_{O9...16}$ | 3 | | | A |
| | | C | $-I_{O7,8}$ | 0.8 | | | A |
| | | C | $-I_{O17,18}$ | 0.8 | | | A |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.13 VDD-Monitoring ABE** | Bidirectional: open drain output / input with pull up current source An external current limitation must guarantee $I_{\overline{ABE}}$ < 5 mA for any $U_{\overline{ABE}}$ | | | | | | |
| **3.13.1 Output** | $U_{\overline{ABE}}$ = Low (after $t_{glitch}$)for: 2.7V < $U_{VDD}$ < 4.5V... 4.7V or 5.3V... 5.5V < $U_{VDD}$ < 36V or Testmode (see 3.13.5 or 3.13.6) or Pin GND_ABE is open | | | | | | |
| 3.13.1.1 Low Level | $U_{VDD}$ > 4.5V, $I_{\overline{ABE}}$<5mA<br>$U_{VDD}$ = 2.7V, $I_{\overline{ABE}}$<1mA,<br>in case of less current, ohmic behavior can be assumed | A<br>A | $U_{\overline{ABE}}$<br>$U_{\overline{ABE}}$ | | | 1.2<br>1.0 | V<br>V |
| |  | | | | | | |
| 3.13.1.2 Maximum Voltage | No current recovery on VDD, UBatt and the logical pins ($\overline{SS}$,SCK,SI,SO,INx,$\overline{RST}$) in case of short to battery at $\overline{ABE}$ (up to 36V) | C | $U_{\overline{ABE}}$ | | | 36 | V |
| **3.13.2 Input** | | | | | | | |
| 3.13.2.1 Low Level | | B | $U_{\overline{ABEL}}$ | | | 0.3 * $U_{VDD}$ | V |
| 3.13.2.2 High Level | | B | $U_{\overline{ABEH}}$ | 0.7 * $U_{VDD}$ | | | V |
| 3.13.2.3 Hysteresis | | C | $\Delta U_{\overline{ABE}}$ | 0.2 | | 1.0 | V |
| 3.13.2.4 Input Current | Pull up current source connected to VDD | | | | | | |
| | -0.25V ≤ $U_{\overline{ABE}}$ ≤ $U_{VDD}$-1.7 V<br>-0.25V ≤ $U_{\overline{ABE}}$ ≤ $U_{VDD}$-1.5 V<br>-0.3V ≤ $U_{\overline{ABE}}$ < -0,25V | A<br>C<br>C | $-I_{\overline{ABE}}$<br>$-I_{\overline{ABE}}$<br>$-I_{\overline{ABE}}$ | 20<br>15 | 40<br>40 | 100<br>100<br>300 | μA<br>μA<br>μA |
| **3.13.3 Overvoltage Threshold** | Voltage referred to GND_$\overline{ABE}$ | B | $V_{DDth\_h}$ | 5.3 | | 5.5 | V |

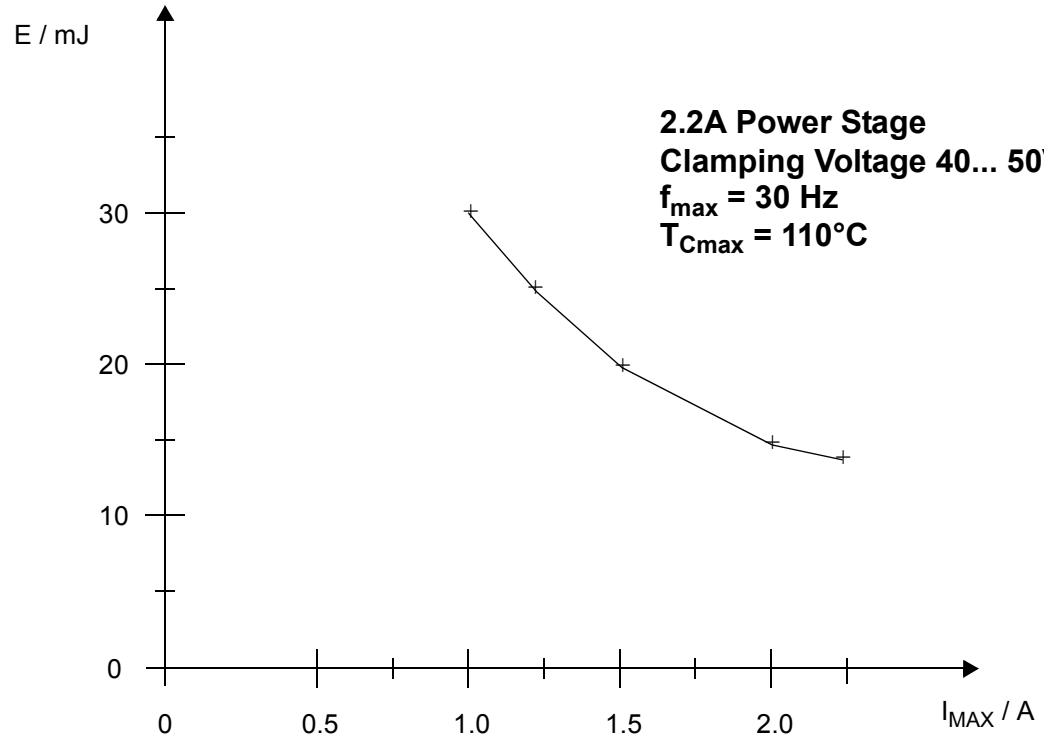
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **3.13.4 Undervoltage Threshold** | Voltage referred to GND_$\overline{ABE}$ | B | $V_{DDth\_l}$ | 4.5 | | 4.7 | V |
| **3.13.5 Test Mode: Reducing the Overvoltage Threshold** | Voltage referred to GND_$\overline{ABE}$ | B | $V_{DDth\_h}$ | 4.5 | | 4.7 | V |
| **3.13.6 Test Mode: Lifting the Undervoltage Threshold** | Voltage referred to GND_$\overline{ABE}$ | B | $V_{DDth\_l}$ | 5.3 | | 5.5 | V |
| **3.13.7 Suppression of Glitches** | Periodical alternating between overvoltage and normal operating voltage with T< 50µs and overvoltage duration > 5µs leads to overvoltage detection.<br>If the transition from undervoltage to overvoltage is faster than the filtering time $t_{glitch}$, the filtering time $t_{glitch}$ for overvoltage detection is not started again. The same is valid for reverse order. | A | $t_{glitch}$ | 50 | | 215 | µs |
| **3.13.8 GND_$\overline{ABE}$** | | | | | | | |
| 3.13.8.1 Permissible Offset between GND_$\overline{ABE}$ and GND | | C | $\Delta U_{GND}$ | | | 0.3 | V |
| 3.13.8.2 Bond Lift / Solder Crack on GND_ABE | Pin $\overline{ABE}$ goes LOW (see 3.13.1.1).<br>The power stages are switched off.<br>The over- and undervoltage thresholds are increased by typically 700mV for $T_A$ = 25°C. | | | | | | |

### 3.14 Clamping Energy

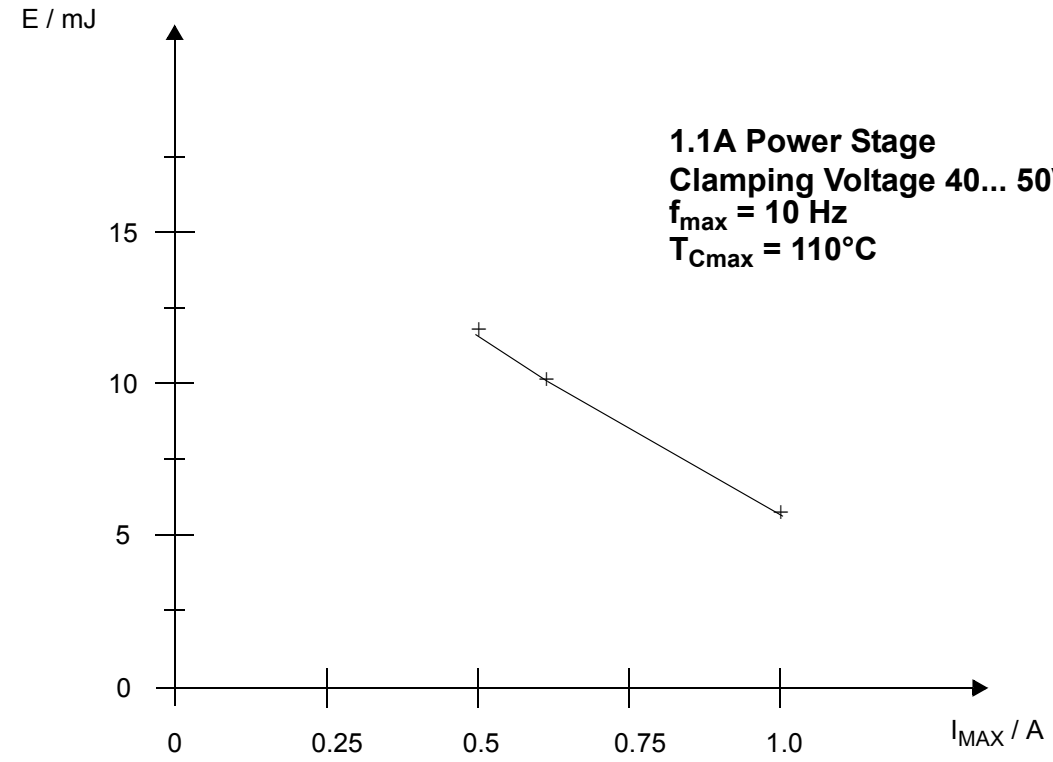
#### 3.14.1 E = f($I_{OUT1...6}$), 2.2A Power Stages with 70V Clamping



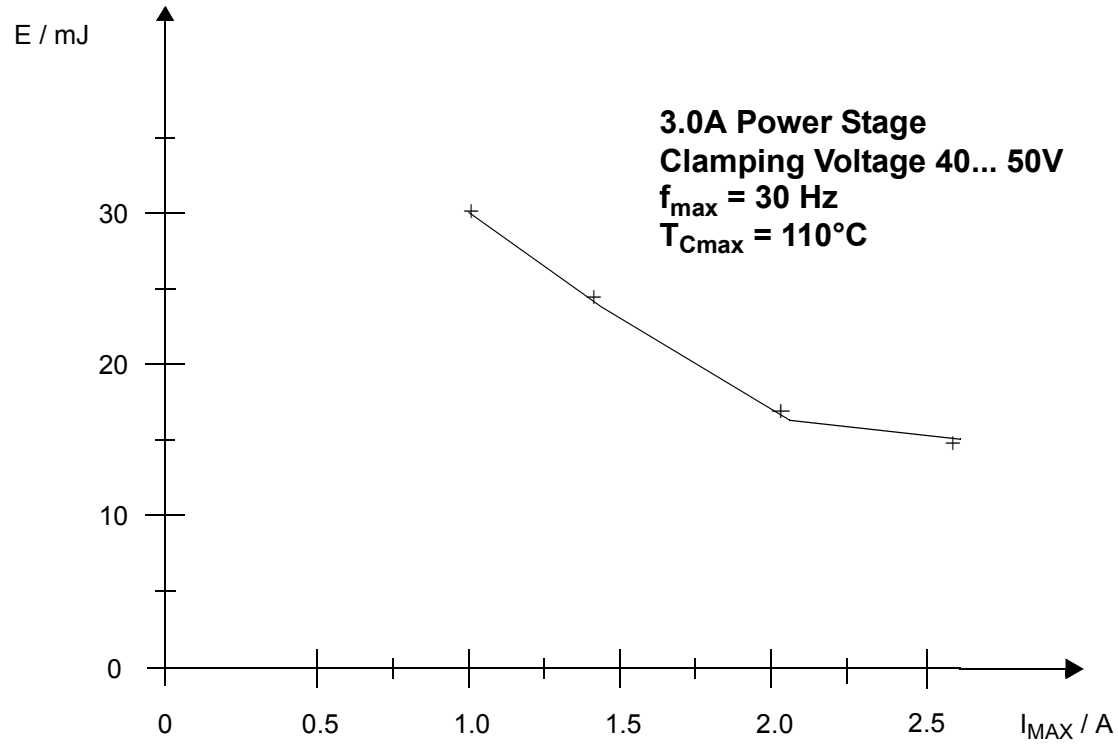

#### 3.14.2 E = f ($I_{OUT9...A14}$), 2.2A Power Stages with 45V Clamping



### 3.14.3 E = f($I_{OUT7,8,17,18}$), 1100mA Power Stages with 45V Clamping




### 3.14.4 E = f($I_{OUT15, OUT16}$), 3.0A Power Stages with 45V Clamping



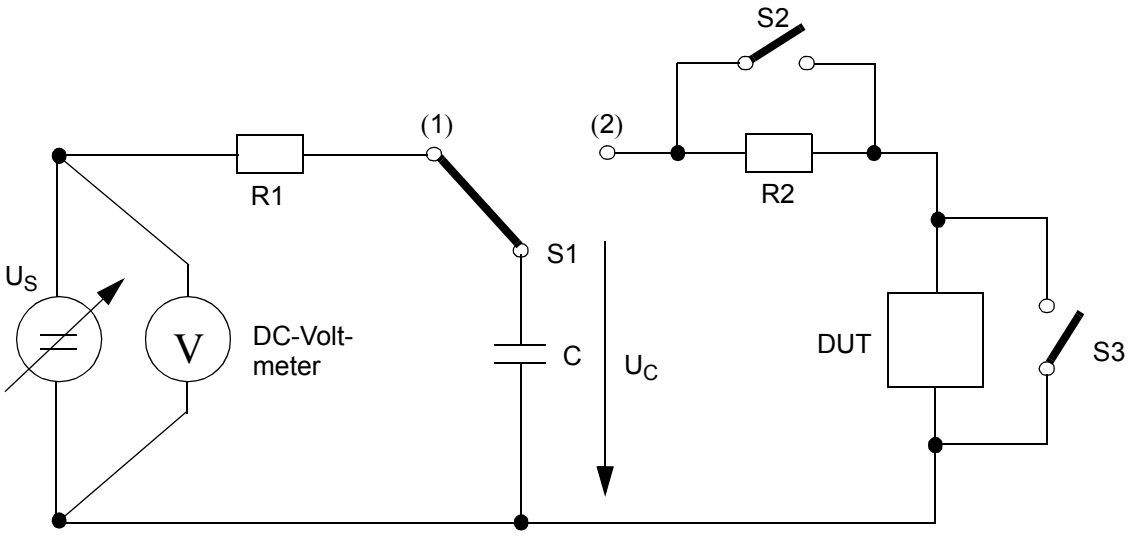
## 4. ESD

All pins of the IC have to be protected against electrostatic discharge (ESD) by appropriate protection
components.

The integrated circuit has to meet the requirements of the „Human Body Model“ with $U_C$ = 2kV, C = 100pF and R2 = 1,5kΩ without any defect or destruction of the IC.

Appropriate measures to reach the required ESD capability have to be coordinated.

The ESD capability of the IC has to be verified by the following test circuit.




$U_C$ = ± 2kV

$R_1$ = 100kΩ

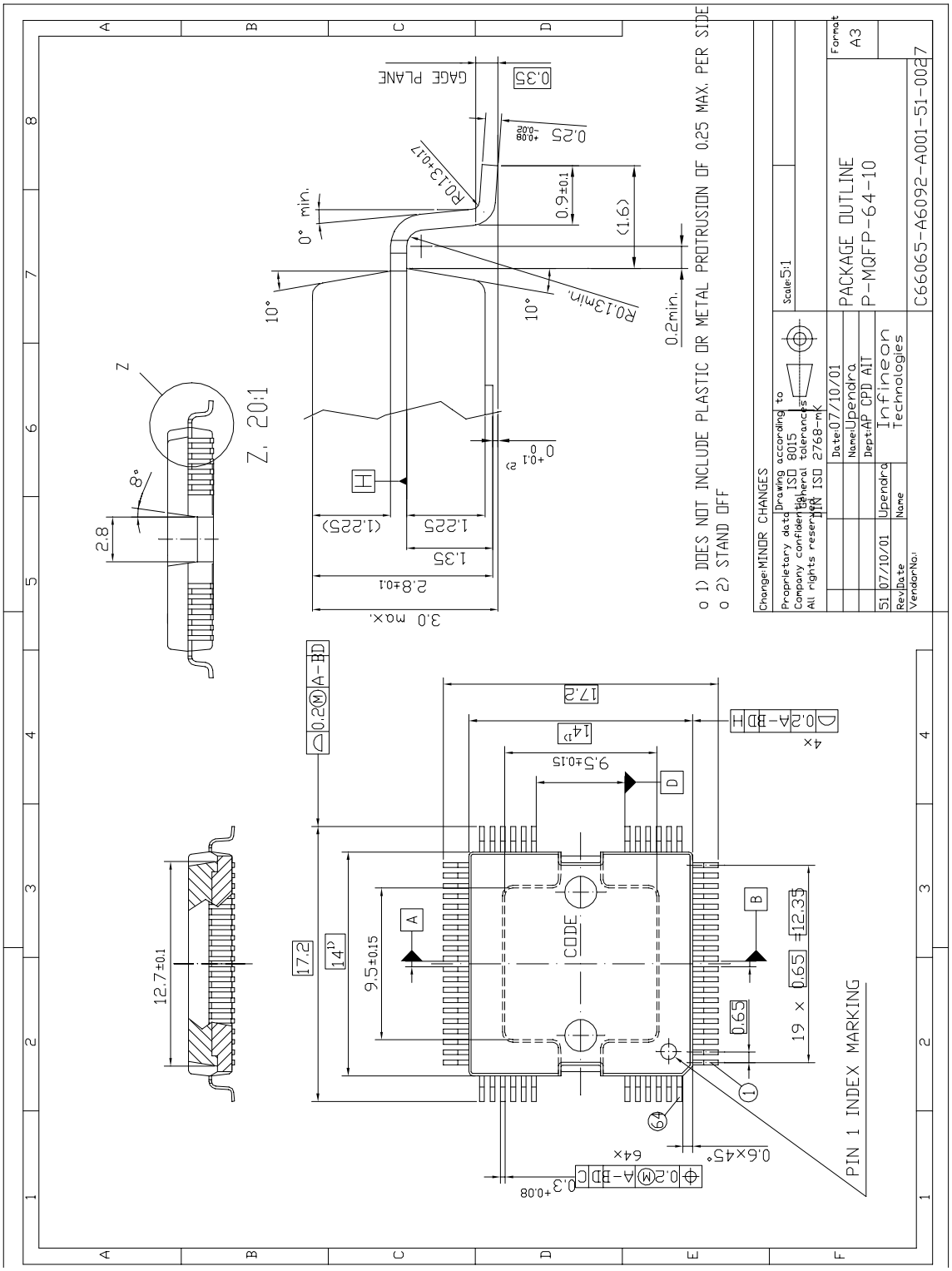
$R_2$ = 1,5kΩ

C = 100pF

Number of pulses each pin: 18 in all
Frequency: 1Hz

Arrangement and performance:
The requirements of MIL883D Method 3015 (latest revision) have to be fulfilled.

## 5. Package Outline



**Edition 2003-08-29**

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**



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