

TLC6C598 8-Bit Shift-Register LED Driver

1 Features

- Wide V_{CC} From 3 V to 5.5 V
- Output Maximum Rating of 40 V
- Eight Power DMOS Transistor Outputs of 50-mA Continuous Current With $V_{CC} = 5$ V or 200-mA PWM Current With Single-Pulse Duration Less Than 1 ms and Average Current Less Than 50 mA
- Thermal Shutdown Protection
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption
- Slow Switching Time (t_r and t_f), Which Helps Significantly With Reducing EMI
- 16-Pin TSSOP-PW Package

2 Applications

- Appliance Display Panel
- Elevator Display Panel
- PLC Function Indicator
- Seven-Segment Display

3 Description

The TLC6C598 device is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks are provided for both the shift and storage register. Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50 mA continuous sink-current OR 200-mA PWM current with single-pulse duration less than 1 ms and average current less than 50 mA capabilities when $V_{CC} = 5$ V. The device contains built-in thermal shutdown protection and provides up to 2000 V of ESD protection when tested using the human-body model and the 200 V machine model.

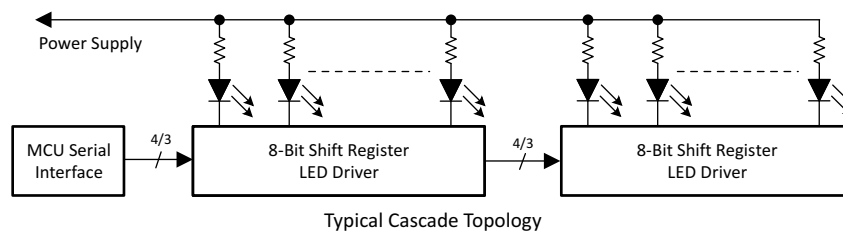
The TLC6C598 characterization is for operation over the operating ambient temperature range of -40°C to 105°C .

Device Information⁽¹⁾

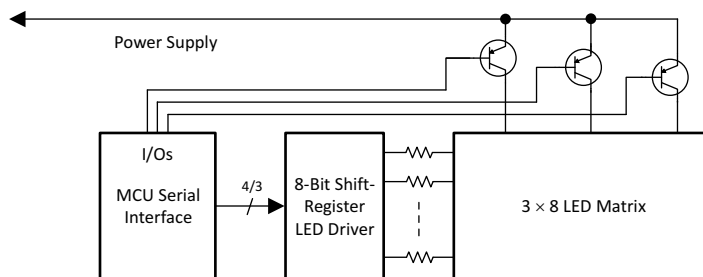
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| TLC6C598 | TSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Typical Cascade Topology



Typical Scan Topology

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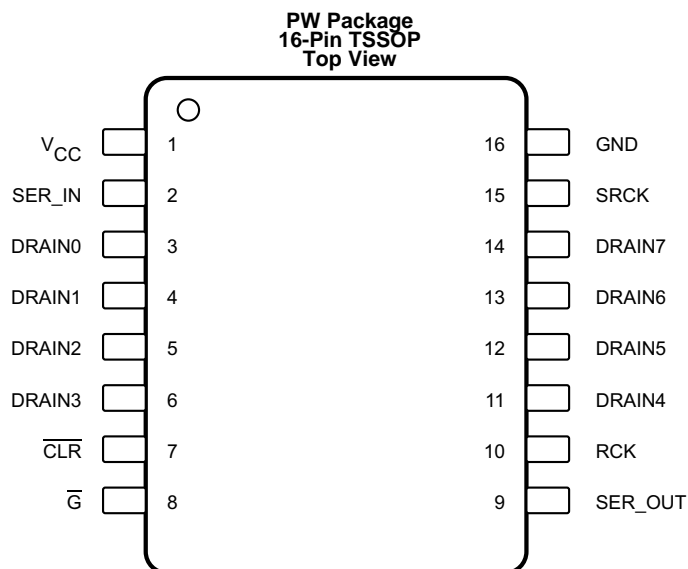
Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 8.1 Overview | 11 |
| 2 Applications | 1 | 8.2 Functional Block Diagram | 11 |
| 3 Description | 1 | 8.3 Feature Description | 12 |
| 4 Revision History | 2 | 8.4 Device Functional Modes | 12 |
| 5 Pin Configuration and Functions | 3 | 9 Application and Implementation | 13 |
| 6 Specifications | 4 | 9.1 Application Information | 13 |
| 6.1 Absolute Maximum Ratings | 4 | 9.2 Typical Application | 13 |
| 6.2 ESD Ratings | 4 | 10 Power Supply Recommendations | 16 |
| 6.3 Recommended Operating Conditions | 4 | 11 Layout | 16 |
| 6.4 Thermal Information | 4 | 11.1 Layout Guidelines | 16 |
| 6.5 Electrical Characteristics | 5 | 11.2 Layout Example | 16 |
| 6.6 Timing Requirements | 5 | 12 Device and Documentation Support | 17 |
| 6.7 Switching Characteristics | 6 | 12.1 Community Resources | 17 |
| 6.8 Timing Waveforms | 7 | 12.2 Trademarks | 17 |
| 6.9 Typical Characteristics | 8 | 12.3 Electrostatic Discharge Caution | 17 |
| 7 Parameter Measurement Information | 9 | 12.4 Glossary | 17 |
| 8 Detailed Description | 11 | 13 Mechanical, Packaging, and Orderable Information | 17 |

4 Revision History

| DATE | REVISION | NOTE |
|----------|----------|-----------------|
| May 2016 | * | Initial release |

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------------------|-----|-----|---|
| NAME | NO. | | |
| $\overline{\text{CLR}}$ | 7 | I | Shift register clear, active-low. The storage register transfers data to the output buffer when CLR is high. Driving CLR low clears all the registers in the device. |
| DRAIN0 | 3 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN1 | 4 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN2 | 5 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN3 | 6 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN4 | 11 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN5 | 12 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN6 | 13 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| DRAIN7 | 14 | O | Open-drain output, LED current-sink channel, connect to LED cathode |
| $\overline{\text{G}}$ | 8 | I | Output enable, active-low. LED-channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off. |
| GND | 16 | — | Power ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB. |
| RCK | 10 | I | Register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. |
| SER IN | 2 | I | Serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK. |
| SER OUT | 9 | O | Serial data output of the 8-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. |
| SRCK | 15 | I | Serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers. |
| V _{CC} | 1 | I | Power supply pin for the device. TI recommends adding a 0.1- μF ceramic capacitor close to the pin. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|--------------------------------------|---|-----|------|
| V _{CC} | Logic supply voltage | -0.3 | 8 | V |
| V _I | Logic input-voltage range | -0.3 | 8 | V |
| V _{DS} | Power DMOS drain-to-source voltage | -0.3 | 42 | V |
| | Continuous total dissipation | See Thermal Information | | |
| T _J | Operating junction temperature range | -40 | 125 | °C |
| T _{stg} | Storage temperature range | -55 | 165 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT | |
|--------------------|-------------------------|---|-------------------------------|------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V | |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | | ±750 |
| | | | Corner pins (1, 8, 9, and 16) | | ±750 |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-----------------|-------------------------------|-----|-----|------|
| V _{CC} | Supply voltage | 3 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.4 | | V |
| V _{IL} | Low-level input voltage | | 0.7 | V |
| T _A | Operating ambient temperature | -40 | 105 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TLC6C598 | UNIT |
|-------------------------------|--|------------|------|
| | | PW (TSSOP) | |
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 129.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 55.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 65.8 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 9.9 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 65.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

6.5 Electrical Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|--|-----------------------|------|-------|------|------------------|
| DRAIN0 to DRAIN7. Drain-to-source voltage | | | | | | 40 | V |
| V_{OH} | High-level output voltage, SER OUT | $I_{OH} = -20\ \mu\text{A}$ | $V_{CC} = 5\text{ V}$ | 4.9 | 4.99 | | V |
| | | $I_{OH} = -4\ \text{mA}$ | | 4.5 | 4.69 | | V |
| V_{OL} | Low-level output voltage, SER OUT | $I_{OH} = 20\ \mu\text{A}$ | $V_{CC} = 5\text{ V}$ | | 0.001 | 0.01 | V |
| | | $I_{OH} = 4\ \text{mA}$ | | | 0.25 | 0.4 | V |
| I_{IH} | High-level input current | $V_{CC} = 5\text{ V}$, $V_I = V_{CC}$ | | | 0.2 | | μA |
| I_{IL} | Low-level input current | $V_{CC} = 5\text{ V}$, $V_I = 0$ | | | -0.2 | | μA |
| I_{CC} | Logic supply current | $V_{CC} = 5\text{ V}$, no clock signal | All outputs off | | 0.1 | 1 | μA |
| | | | All outputs on | | 88 | 160 | |
| $I_{CC}(\text{FRQ})$ | Logic supply current at frequency | $f_{SRCK} = 5\text{ MHz}$, $C_L = 30\text{ pF}$ | All outputs on | | 200 | | μA |
| I_{DSx} | Off-state drain current | $V_{DS} = 30\text{ V}$ | $V_{CC} = 5\text{ V}$ | | | 0.1 | μA |
| | | $V_{DS} = 30\text{ V}$, $T_C = 105^\circ\text{C}$ | $V_{CC} = 5\text{ V}$ | | 0.15 | 0.3 | |
| $r_{DS(\text{on})}$ | Static drain-source on-state resistance | $I_D = 20\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Single channel ON | | 6 | 7.41 | 8.6 | Ω |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, All channels ON | | 6.7 | 8.3 | 9.6 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, Single channel ON | | 7.9 | 9.34 | 11.2 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, All channels ON | | 8.7 | 10.25 | 12.3 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 105^\circ\text{C}$, Single channel ON | | 9.1 | 11.13 | 12.9 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 105^\circ\text{C}$, All channels ON | | 10.3 | 12.28 | 14.5 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $T_A = 105^\circ\text{C}$, Single channel ON | | 11.6 | 13.69 | 16.4 | |
| | | $I_D = 20\text{ mA}$, $V_{CC} = 3.3\text{ V}$, $T_A = 105^\circ\text{C}$, All channels ON | | 12.8 | 14.89 | 18.2 | |
| T_{SHUTDOWN} | Thermal shutdown trip point | | | 150 | 175 | 200 | $^\circ\text{C}$ |
| T_{hys} | Hysteresis | | | | 15 | | $^\circ\text{C}$ |

6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|----------|--|-----|-----|-----|------|
| t_{su} | Setup time, SER IN high before SRCK \uparrow | 15 | | | ns |
| t_h | Hold time, SER IN high after SRCK \uparrow | 15 | | | ns |
| t_w | SER IN pulse duration | 40 | | | ns |

6.7 Switching Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|---|-----|------|-----|------|
| t_{PLH} | Propagation delay time from \overline{G} to output, low-to-high level | $C_L = 30\text{ pF}$, $I_D = 48\text{ mA}$ | | 220 | | ns |
| t_{PHL} | Propagation delay time from \overline{G} to output, high-to-low level | | | 75 | | ns |
| t_r | Rise time, drain output | | | 210 | | ns |
| t_f | Fall time, drain output | | | 128 | | ns |
| t_{pd} | Propagation delay time, SRCK \downarrow to SER OUT | $C_L = 30\text{ pF}$, $I_D = 48\text{ mA}$ | | 49.4 | | ns |
| t_{or} | SER OUT rise time (10% to 90%) | $C_L = 30\text{ pF}$ | | 20 | | ns |
| t_{of} | SER OUT fall time (90% to 10%) | $C_L = 30\text{ pF}$ | | 20 | | ns |
| $f_{(SRCK)}$ | Serial clock frequency | $C_L = 30\text{ pF}$, $I_D = 20\text{ mA}$ | | | 10 | MHz |
| t_{SRCK_WH} | SRCK pulse duration, high | | 30 | | | ns |
| t_{SRCK_WL} | SRCK pulse duration, low | | 30 | | | ns |

6.8 Timing Waveforms

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 13). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

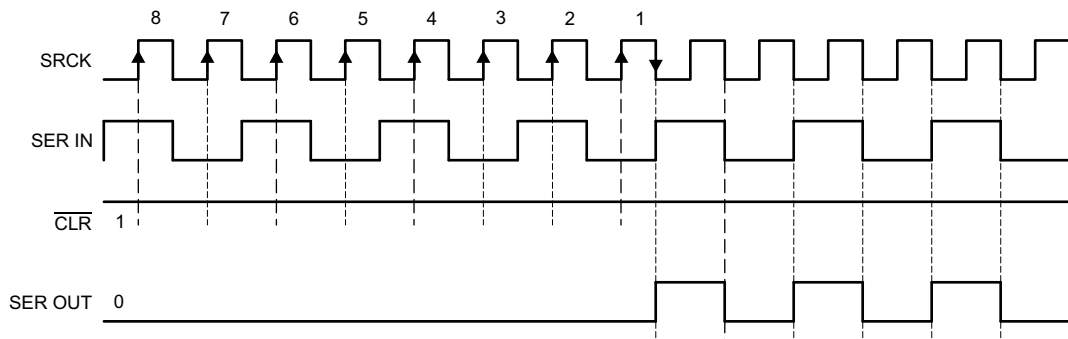


Figure 1. SER IN to SER OUT Waveform

Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 11.

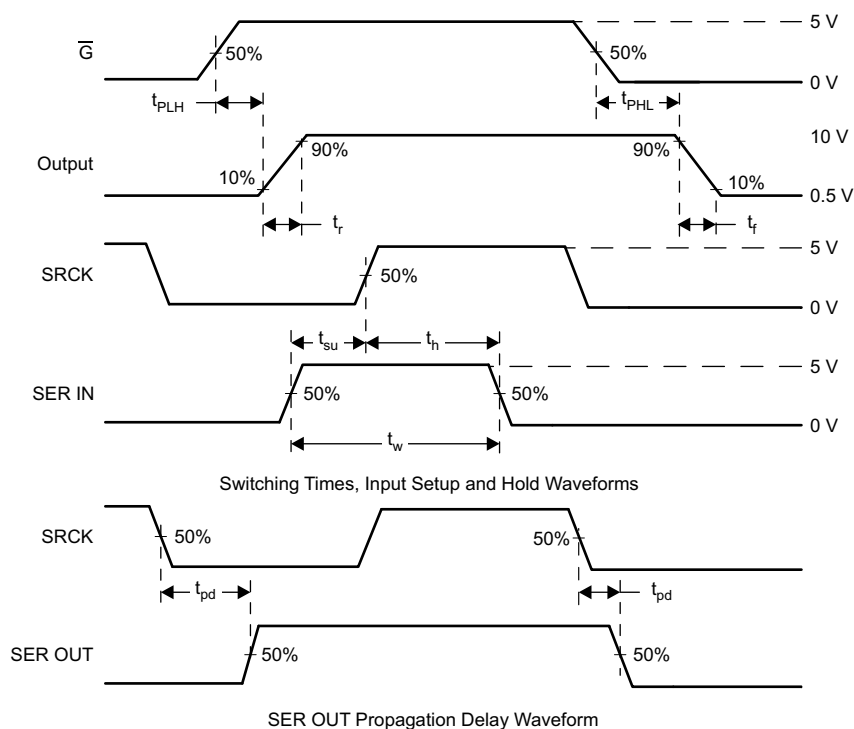
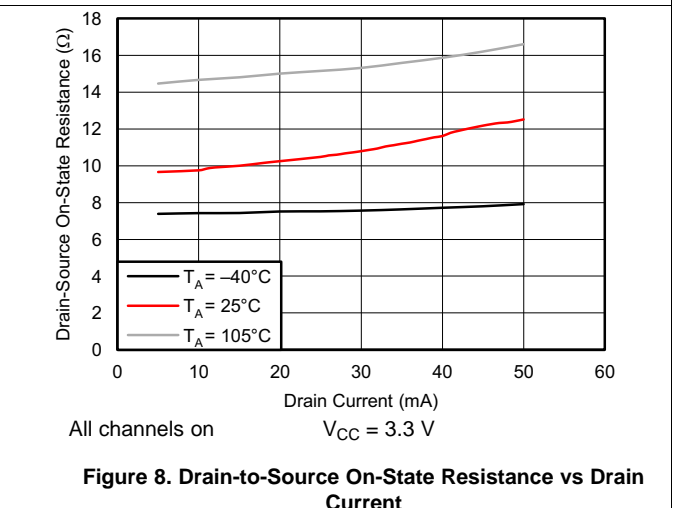
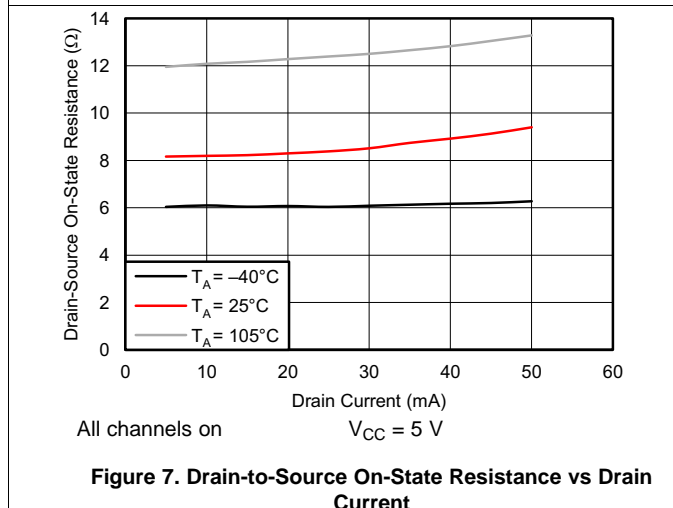
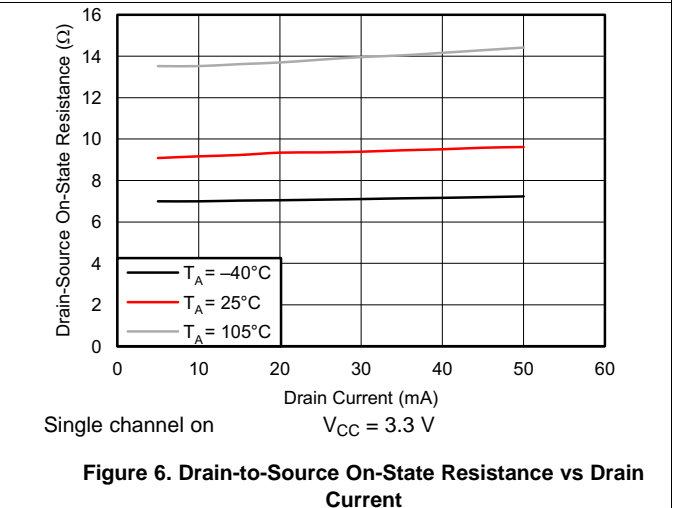
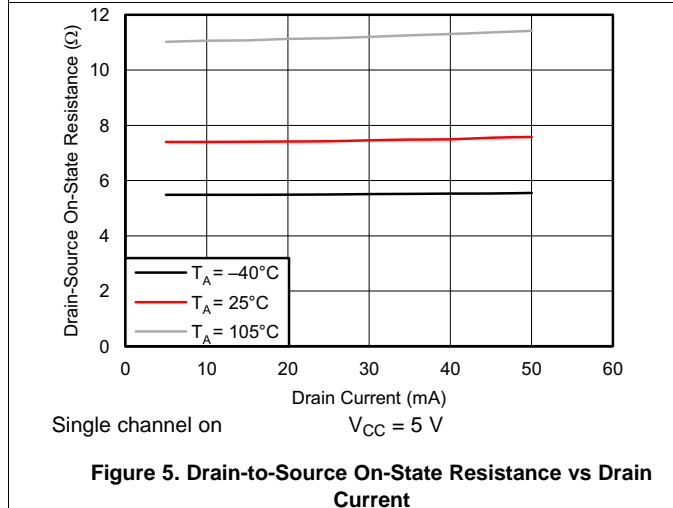
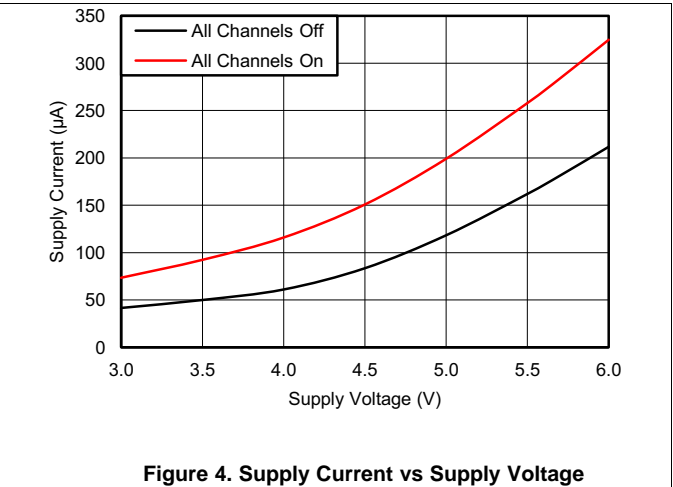
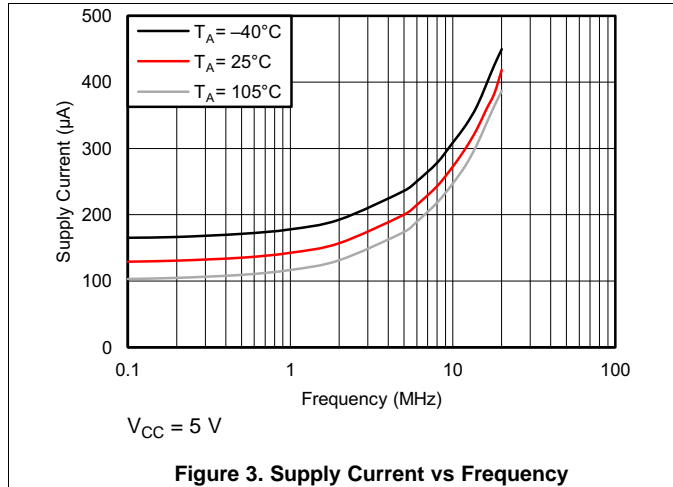
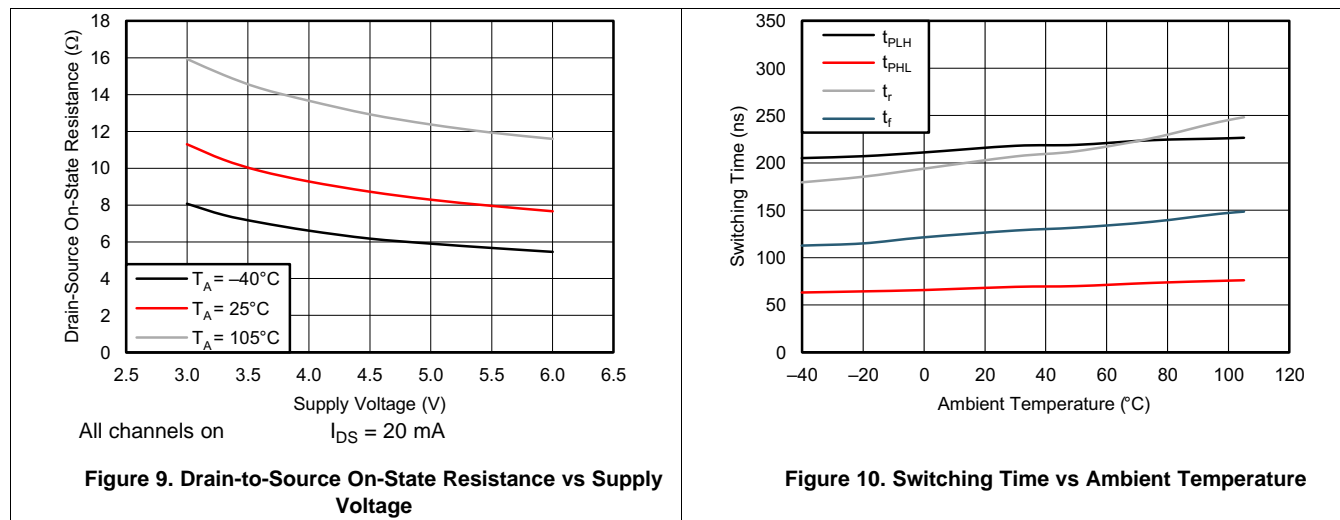


Figure 2. Switching Times and Voltage Waveforms

6.9 Typical Characteristics

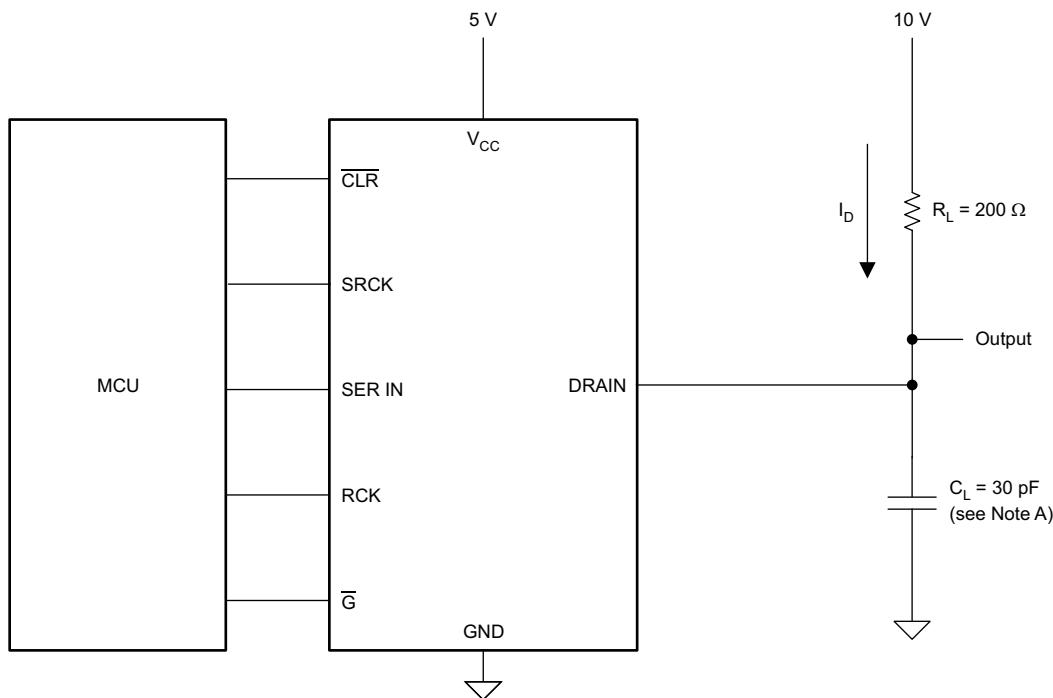


Typical Characteristics (continued)



7 Parameter Measurement Information

Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with \overline{G} held low and \overline{CLR} held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.



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A. C_L includes probe and jig capacitance.

Figure 11. Resistive-Load Test Circuit

Parameter Measurement Information (continued)

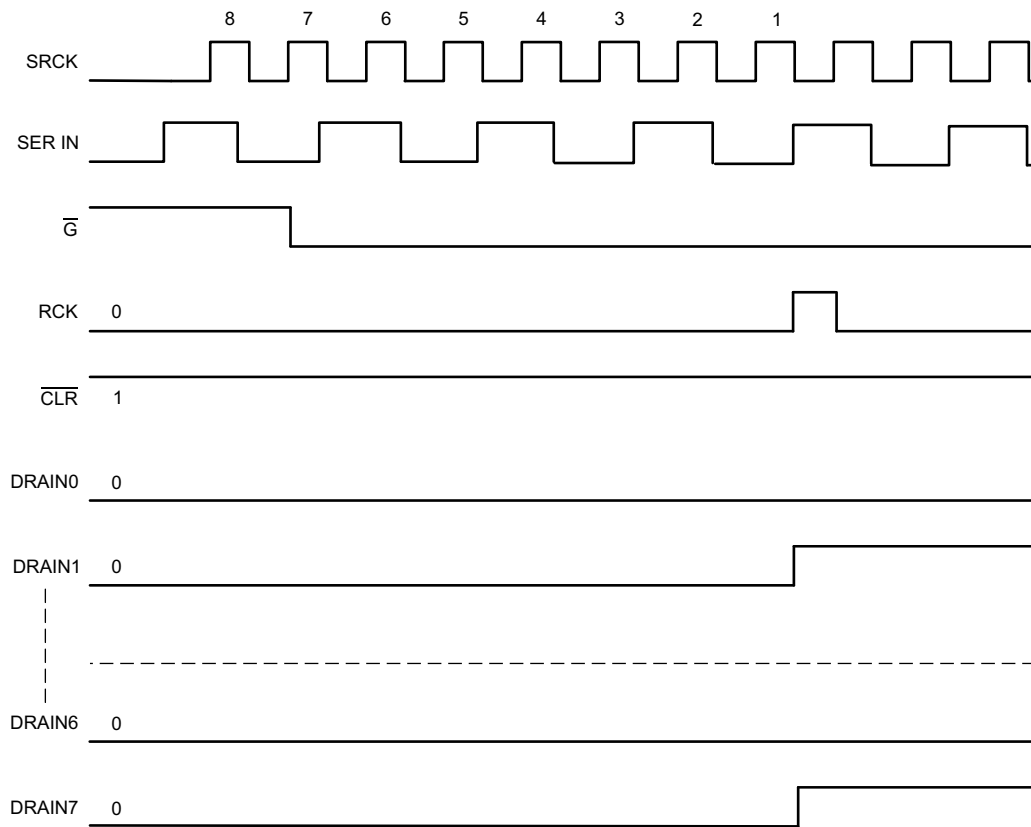


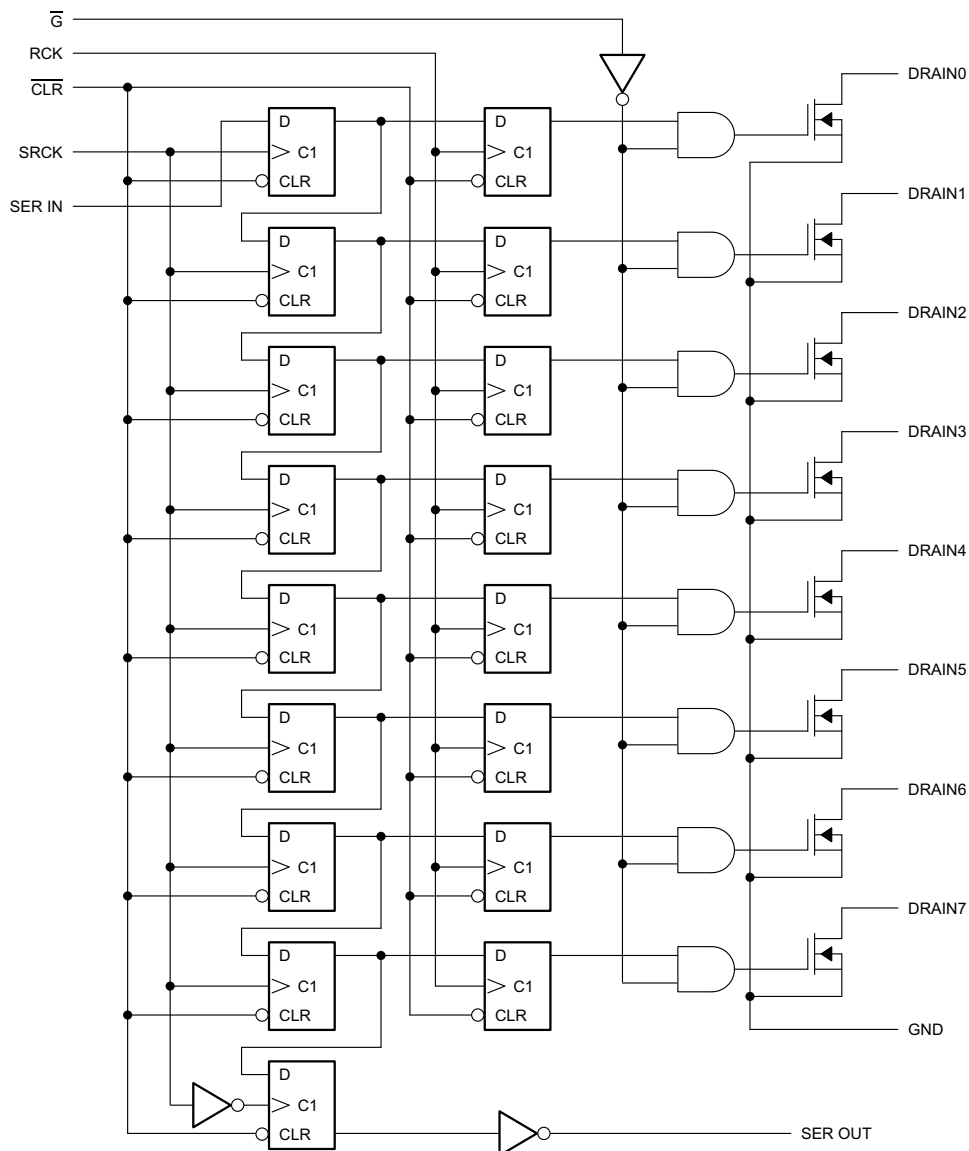
Figure 12. Voltage Waveforms

8 Detailed Description

8.1 Overview

The TLC6C598 device is a monolithic, medium-voltage, low-current 8-bit shift register designed to drive relatively moderate load power such LEDs. The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Thermal shutdown protection is also built-into the device.

8.2 Functional Block Diagram



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Figure 13. Logic Diagram (Positive) of TLC6C598

8.3 Feature Description

8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfer through the shift and storage registers is on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{CLR}}$) is high.

8.3.3 Clear Registers

A logic low on the $\overline{\text{CLR}}$ pin clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.4 Output Channels

DRAIN0–DRAIN7. These pins can survive up to 40-V LED supply voltage.

8.3.5 Register Clock

RCK is the storage-register clock. Data in the storage register appears at the output whenever the output enable ($\overline{\text{G}}$) input signal is high.

8.3.6 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus in cascade, the data transfers to the next device on the falling edge of SRCK. This connection can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input on the same rising edge of SRCK.

8.3.7 Output Control

Holding the output enable (pin $\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{\text{G}}$ low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sinking current. This pin also can be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With $V_{\text{CC}} < 3 \text{ V}$

This device works normally within the range $3 \text{ V} \leq V_{\text{CC}} \leq 5.5 \text{ V}$. When the operating voltage is lower than 3 V, correct behavior of the device, including communication interface and current capability, is not assured.

8.4.2 Operation With $5.5 \text{ V} \leq V_{\text{CC}} \leq 8 \text{ V}$

The device works normally in this voltage range, but reliability issues may occur if the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

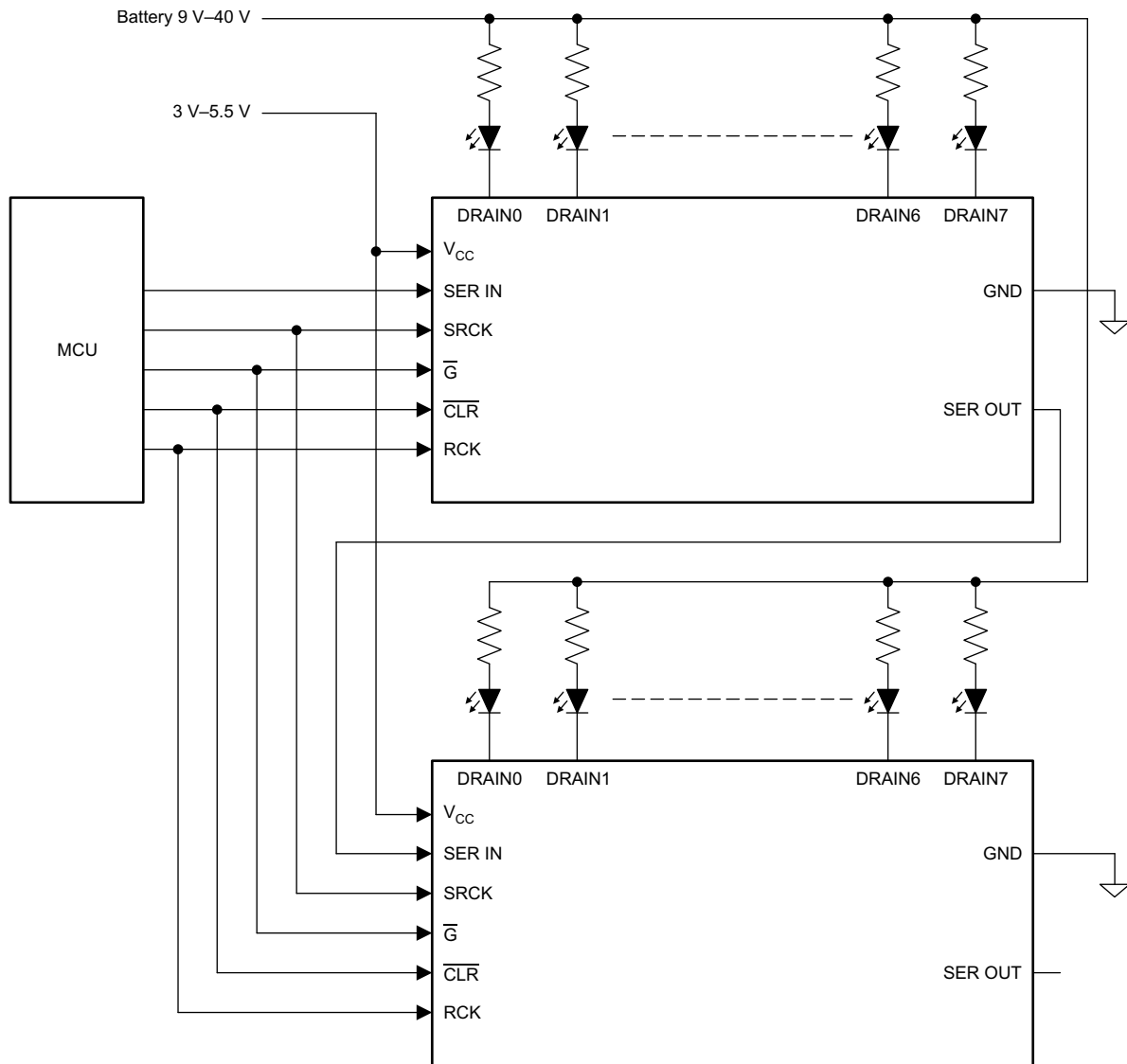
9.1 Application Information

The TLC6C598 device is a serial-in, parallel-out, power and logic, 8-bit shift register with low-side open-drain DMOS output ratings of 40-V and 50-mA continuous sink-current capabilities when $V_{CC} = 5\text{ V}$. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

9.2 Typical Application

[Figure 14](#) shows a typical cascade application circuit with two TLC6C598 chips configured in cascade topology. The MCU generates all the input signals.

Typical Application (continued)



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Figure 14. Typical Application Circuit

9.2.1 Design Requirements

| DESIGN PARAMETER | EXAMPLE VALUE |
|--|---------------|
| V _{Battery} | 9 V to 40 V |
| V _{CC_1} | 3.3 V |
| I(D0), I(D1), I(D2), I(D3), I(D4), I(D5), I(D6), I(D7) | 30 mA |
| V _{CC_2} | 5 V |
| I(D8), I(D9), I(D10), I(D11), I(D12), I(D13), I(D14), I(D15) | 50 mA |

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- V_{supply} : LED supply voltage
- V_{Dx} : LED forward voltage
- I : LED current

With these parameters determined, the resistor in series with the LED can be calculated by using the following equation:

$$R_X = (V_{\text{Supply}} - V_{\text{Dx}}) / I \quad (1)$$

9.2.3 Application Curve

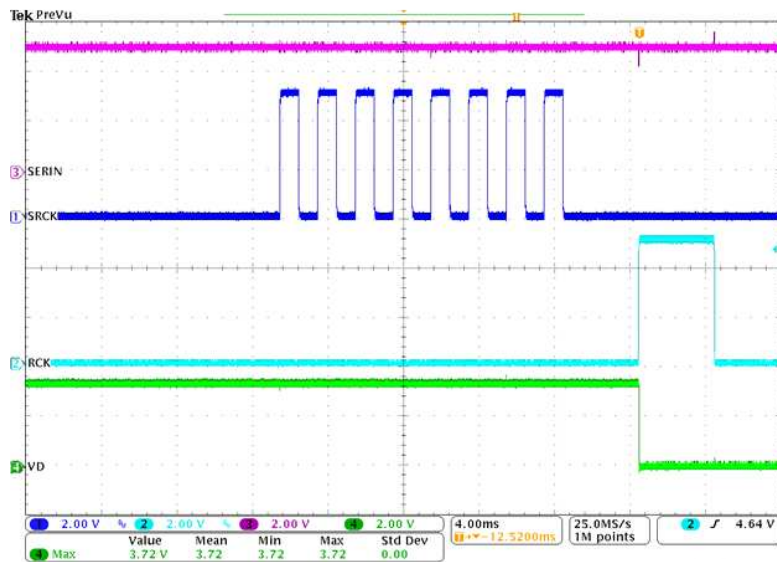


Figure 15. TLC6C598 Application Waveform

10 Power Supply Recommendations

The TLC6C598 device is designed to operate with an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirements for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pins.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.

All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

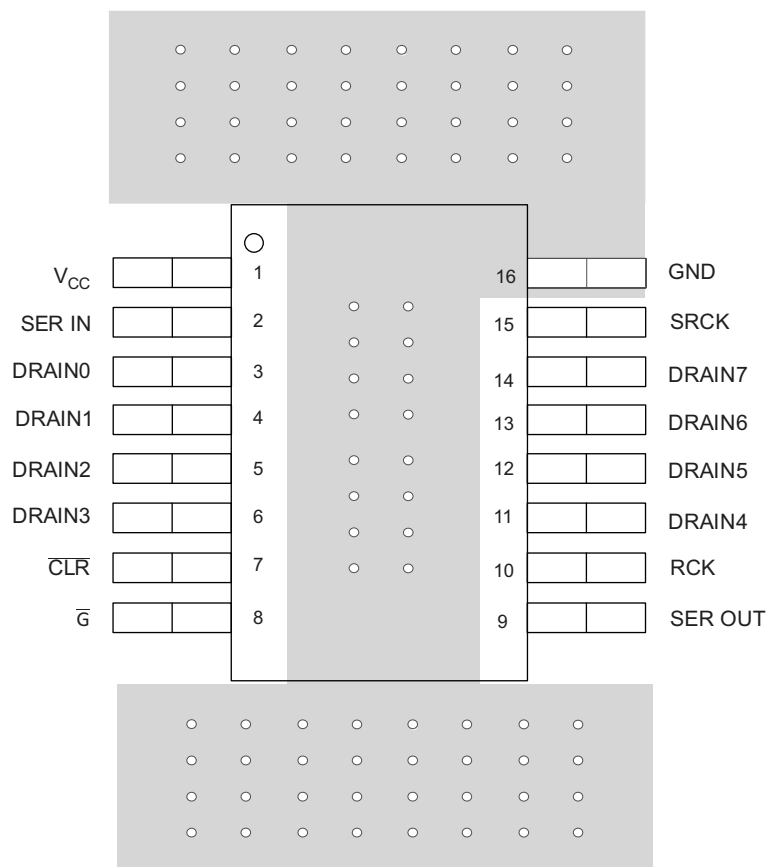


Figure 16. TLC6C598 Example Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TLC6C598PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | 6C598I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC6C598 :

- Automotive: [TLC6C598-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC6C598PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

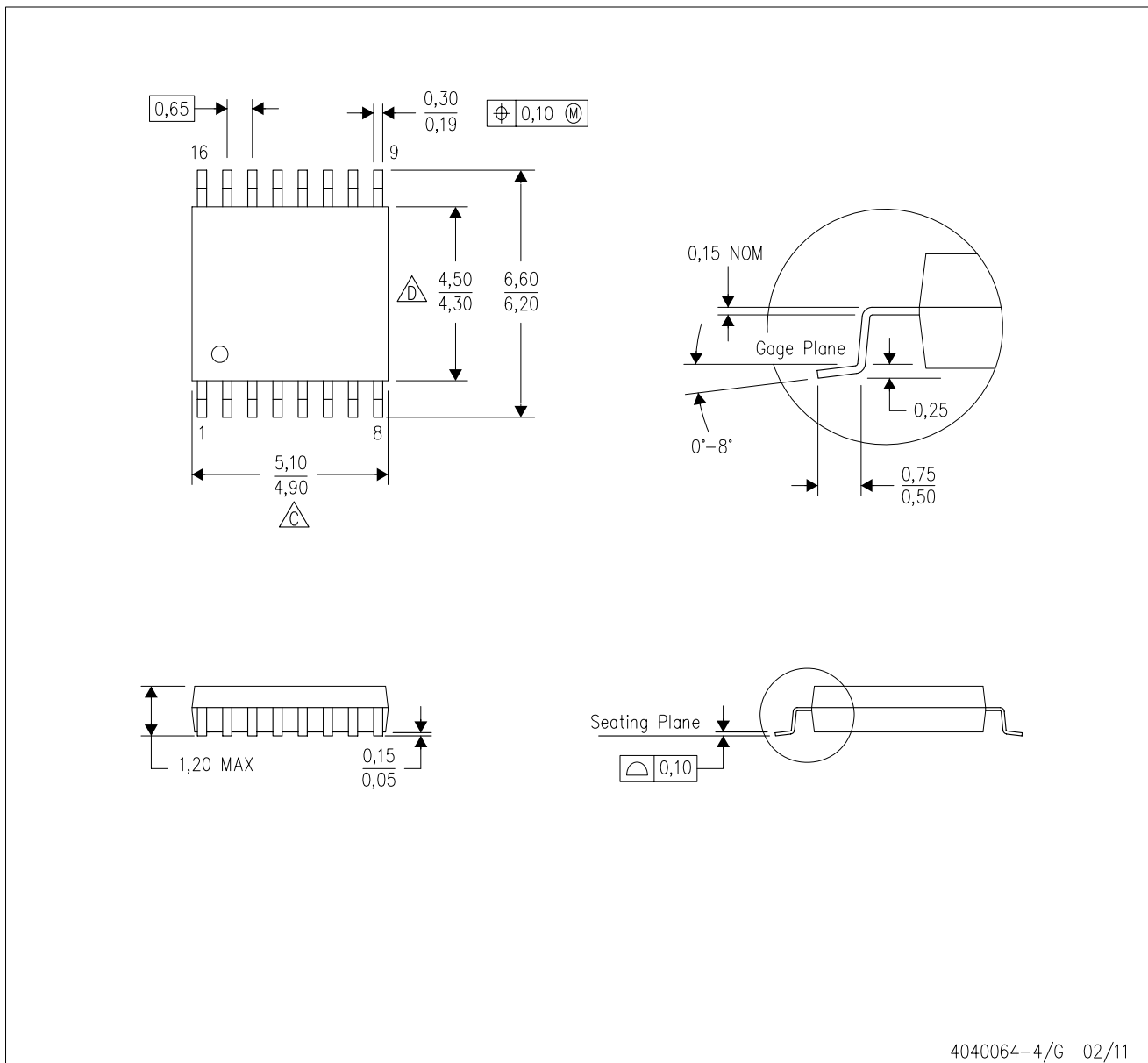
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC6C598PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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