TLC59213x 8-Bit Parallel In and Out Darlington Source Driver With Latch

1 Features

- Output Current on Each Channel (I_{OUT} Max = –500 mA)
- $V_{CE(sus)}$ = 13.2 V
- Input Compatible With TTL/5-V CMOS
- Clear ($\overline{CLR}$) and Clock (CLK) TTL/CMOS Control Inputs
- CLR Control Input to Off the Output
- Darlington Source Driver
- Clock Input Up to 1 MHz
- Enhanced Hold Time (t_h) on TLC59213A
- Temperature Range: –40°C to 85°C

2 Applications

- Lamp and Display (LED)
- Hammer
- Relay

3 Description

The TLC59213 and TLC59213A are 8-bit source drivers with input latch with CLK input and $\overline{CLR}$ to set the output OFF. The TLC59213 and TLC59213A have large output source currents up to 500 mA with Darlington transistor and collectors tied to V_{CC}. These feature make the device optimum level of driving the matrix of ink jet printer head, LEDs, and the scan-side of resistor's matrix. The TLC59213 and TLC59213A differ only in the Data Hold Time Specification (t_h).

The clamp diode is between output and ground for switching inductive load.

All inputs are TTL/CMOS, which enable to any logic-level inputs such as MCU, CPU or SN74LV594 (serial to parallel) and the output enable LED matrix display. It can also be used with another device sink driver such as TLC59210, TLC59211 and TLC59212.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59213 TLC59213A	PDIP (20)	24.33 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram÷

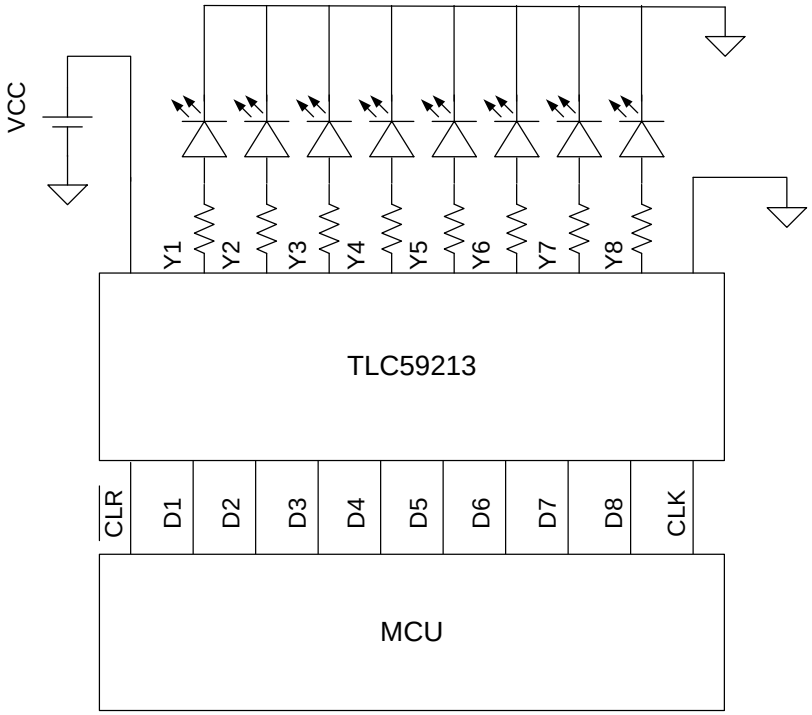


Table of Contents

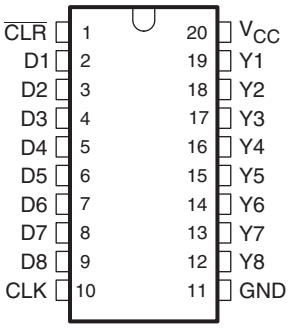
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2010) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

N or PW Package
20-Pin PDIP or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	1	I	Direct clear of output
D1	2	I	Input control to the current source driver
D2	3	I	Input control to the current source driver
D3	4	I	Input control to the current source driver
D4	5	I	Input control to the current source driver
D5	6	I	Input control to the current source driver
D6	7	I	Input control to the current source driver
D7	8	I	Input control to the current source driver
D8	9	I	Input control to the current source driver
CLK	10	I	Clock to positive edge triggered D flipflops
GND	11	—	Ground
Y8	12	O	Output to load
Y7	13	O	Output to load
Y6	14	O	Output to load
Y5	15	O	Output to load
Y4	16	O	Output to load
Y3	17	O	Output to load
Y2	18	O	Output to load
Y1	19	O	Output to load
V_{cc}	20	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	15	V
V_I	Input voltage		–0.5	V_{CC} + 0.5	V
	Collector-emitter voltage		–0.5	15	V
I_O	Peak output current			–500	mA
I_{IK}	Input clamp current	V_I < 0 V		–20	mA
I_{OK}	Output clamp current	V_O < 0 V		–500	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			4.5	13.2	V
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.8	V
I_O	Output current (8 channel)	N package	Duty cycle < 10%		400	mA
			Duty cycle < 50%		200	
		PW package	Duty cycle < 10%		350	
			Duty cycle < 50%		170	
T_A	Operating free-air temperature			–40	85	°C

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CEX}	Output leakage current	V_{CC} = 13.2 V, Outputs off				2	µA
$V_{CE(sus)}$	Output saturation voltage	I_{OUT} = –350 mA				2.35	V
		I_{OUT} = –225 mA				2.15	
		I_{OUT} = –100 mA				1.96	
I_I	Input current	V_{CC} = 13.2 V, V_I = 0 or 13.2 V				1	µA
V_f	Clamp forward voltage	I_f = –350 mA		–2			V
I_{CC}	Supply current	V_{CC} = 13.2 V, V_I = 0 or 13.2 V	All outputs OFF		4.6	13	mA
			All outputs ON		4.8	13	
C_I	Input capacitance					10	pF

6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted), see Figure 3

					MIN	MAX	UNIT
t_{su}	Setup time	D before CLK ↑			50		ns
		$\overline{CLR}$ high before CLK ↑			50		ns
t_h	Hold time	D after CLK ↑	TLC59213, TLC59213A	T_A = -40°C to 85°C	50		ns
			TLC59213	T_A = 0°C to 70°C	25		
			TLC59213A	T_A = 0°C to 70°C, V_{CC} = 4.5 V to 5.5 V	15		
				T_A = 0°C to 70°C, V_{CC} = 10.8 V to 13.2 V	19		
t_w	Pulse width	CLK, $\overline{CLR}$			100		ns

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), see Figure 3

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	CLK	Y	RL = 25 Ω, C_L = 15 pF		107	200		250	ns
t_{PHL}	Propagation delay time, high-to-low level output	CLK	Y	RL = 25 Ω, C_L = 15 pF		111	200		250	ns
t_{PHLR}	Propagation delay time, high-to-low level output	$\overline{CLR}$	Y	RL = 25 Ω, C_L = 15 pF		104	200		250	ns

6.7 Typical Characteristics

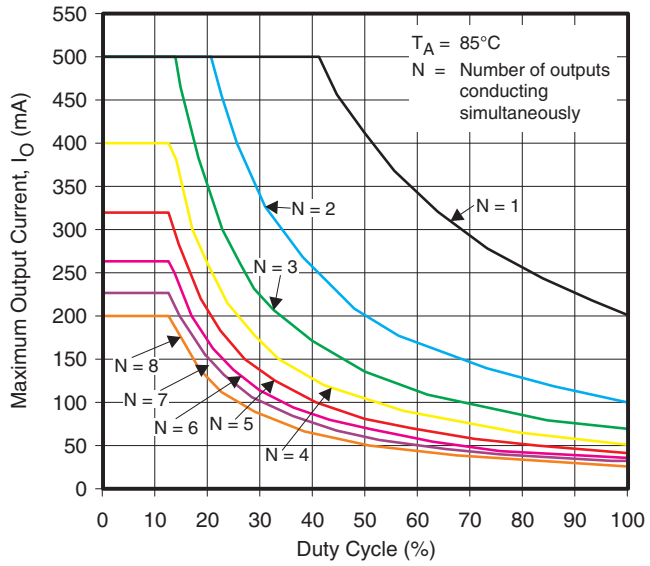


Figure 1. Maximum Output Current vs Duty Cycle (TSSOP (PW) Package)

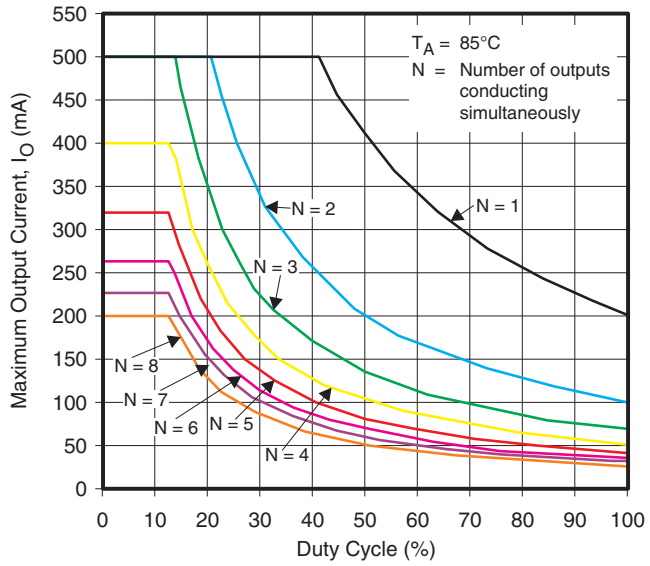
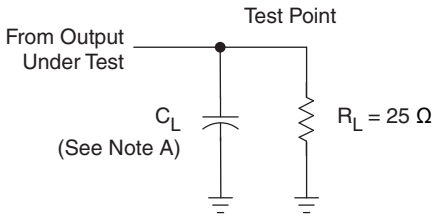
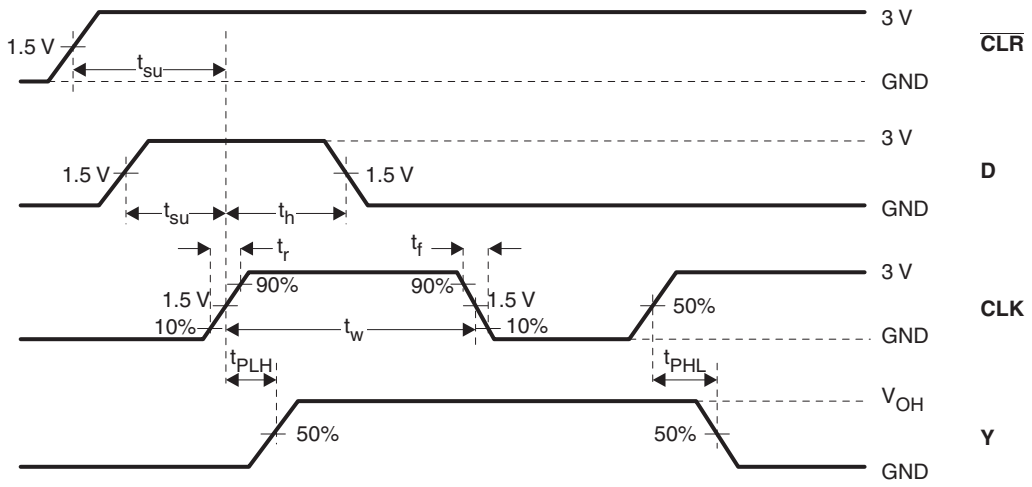


Figure 2. Maximum Output Current vs Duty Cycle (DIP (N) Package)

7 Parameter Measurement Information



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.

C. The outputs are measured one at a time with one transition per measurement.

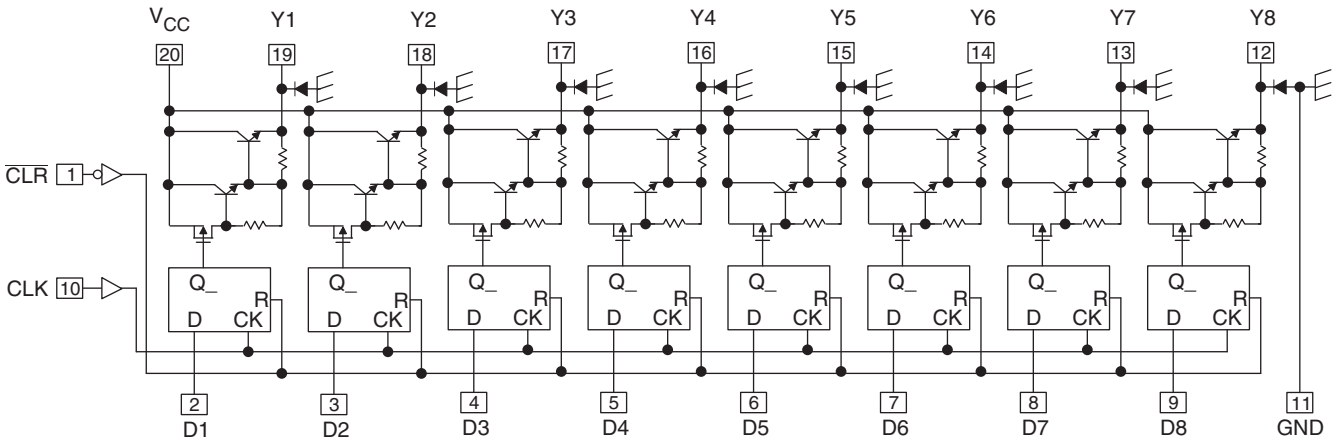
Figure 3. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TLC59213 device is an 8-bit Darlington source driver with latch for large-output source currents up to 500 mA.

8.2 Functional Block Diagram



(1) This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

8.3 Feature Description

Each of the 8 channels is controlled by its input (Dn), a direct clear ($\overline{CLR}$), and clock (CLK) through a positive-edge-triggered D-type flip-flops. Information at the data (D) input meeting the setup time requirements is transferred to the output (Y) on the positive-going edge of the clock (CLK) pulse. When CLK is at either the high or low level, the D-input has no effect at the output. When $\overline{CLR}$ is at low level, the D-input has no effect at the output.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TLC59213.

Table 1. Function Table (Each Latch)(1)

INPUTS			OUTPUT Y
$\overline{CLR}$	CLK	D	
L	X	X	Z (OFF)
H	↑	L	Z (OFF)
H	↑	H	H (ON)
H	L	X	Y_0
H	↓	X	Y_0

(1) L: Low-level
H: High-level
X: Irrelevant
↑: Rising edge
↓: Falling edge
Z : High-impedance (OFF)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In LED display application, TLC59213 is used to drive the current source for 8 LEDs in parallel. LED display pattern can be created by providing different bit pattern. At every positive clock edge, new bit pattern will be transferred to LED display.

9.2 Typical Application

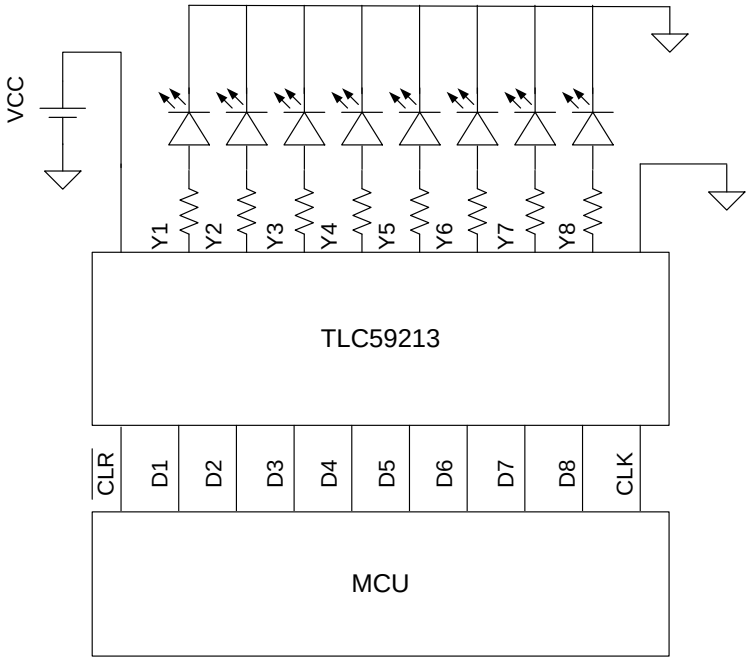


Figure 4. Typical Application Diagram

9.2.1 Design Requirements

For LED display application, LED is selected based on the application. The current level is determined by the required brightness. Given the available supply, the resistor value could be determined. The maximum output current is constrained by the duty cycle. See Figure 1 and Figure 2.

9.2.2 Detailed Design Procedure

The selection of supply voltage (VCC), LED, and resistor sets the current of the LED.

$$VR + VL + VCE = VCC \quad (1)$$

$$I = (VCC - VL - VCE) / R \quad (2)$$

VR is the voltage drop across the resistor, VL is the voltage drop across the LED when LED is on, VCE is the collector-to-emitter voltage of the Darlington current source driver, when the driver is enabled. For example, when VCC = 12 V, VL = 2.9 V, and VCE = 1.6 V, a 75-Ω resistor is used to obtain output current 100 mA.

Typical Application (continued)

9.2.3 Application Curve

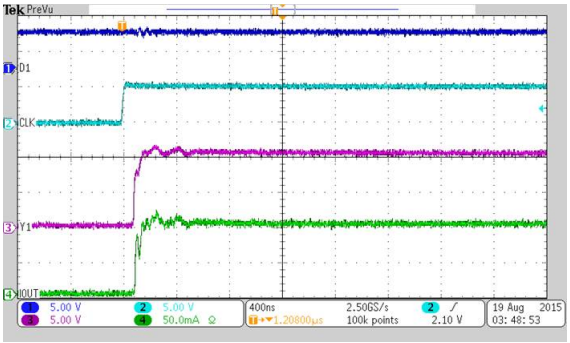


Figure 5. Output Voltage and Current Response

10 Power Supply Recommendations

The supply voltage to TLC59213 is from 4.5 V to 13.2 V.

11 Layout

11.1 Layout Guidelines

The traces that carry current from the output pins must be wide enough to support the current.

11.2 Layout Example

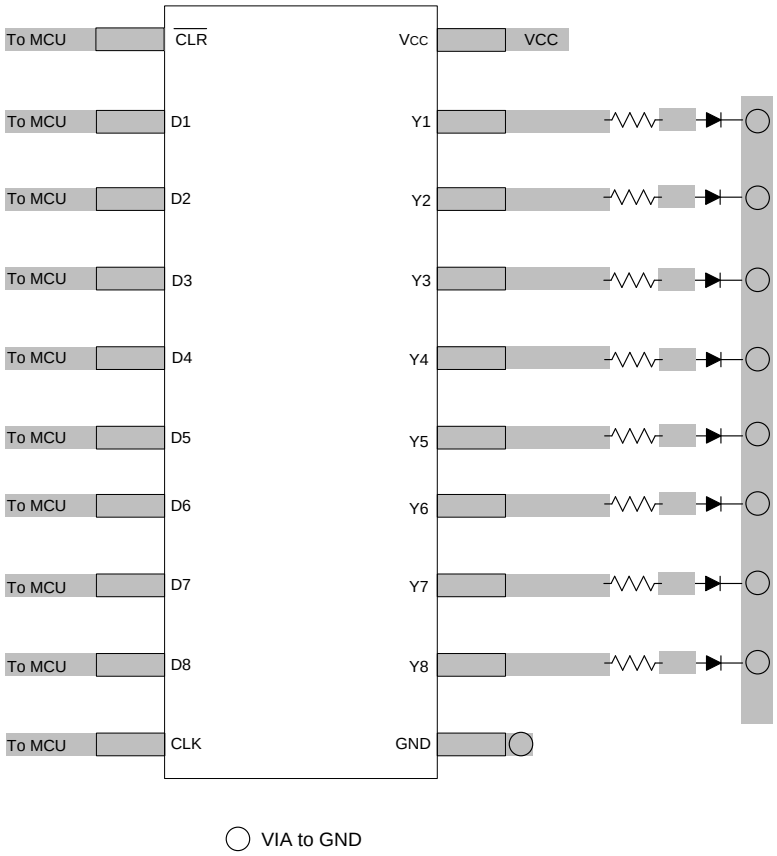


Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59213AIN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC59213AIN	Samples
TLC59213AIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y59213A	Samples
TLC59213AIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213A	Samples
TLC59213AIPWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213A	Samples
TLC59213IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC59213IN	Samples
TLC59213IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

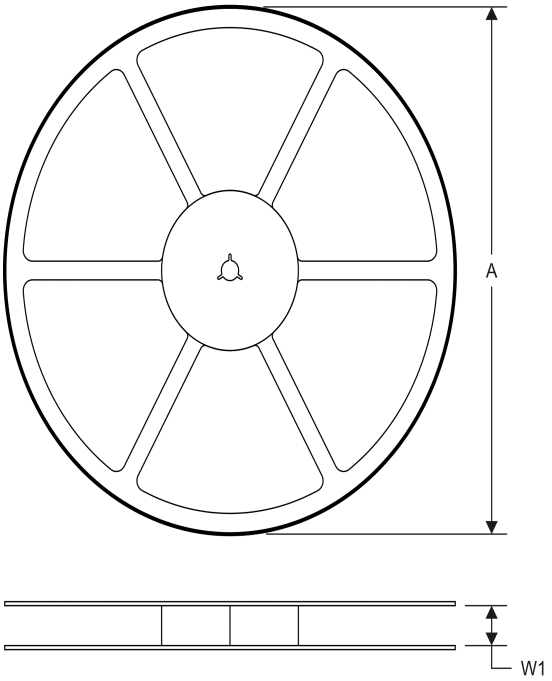
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

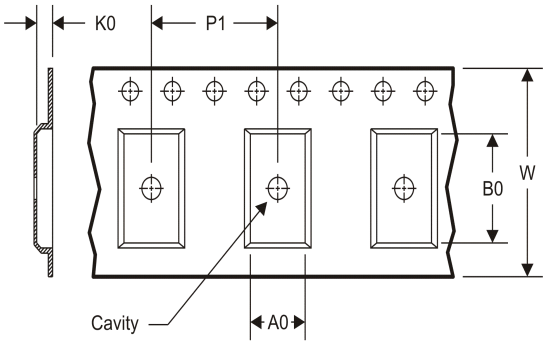
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



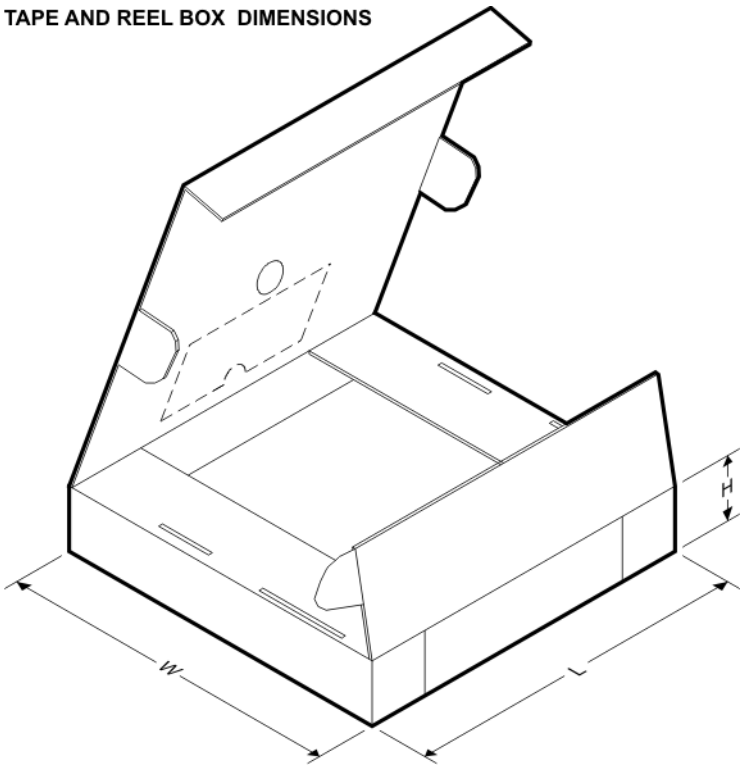
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59213AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59213AIPWT	TSSOP	PW	20	250	180.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59213IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



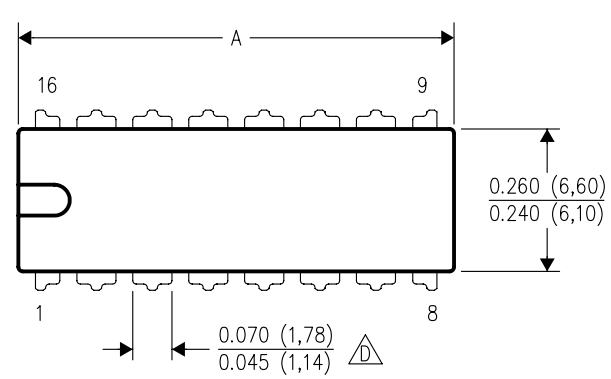
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59213AIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLC59213AIPWT	TSSOP	PW	20	250	210.0	185.0	35.0
TLC59213IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

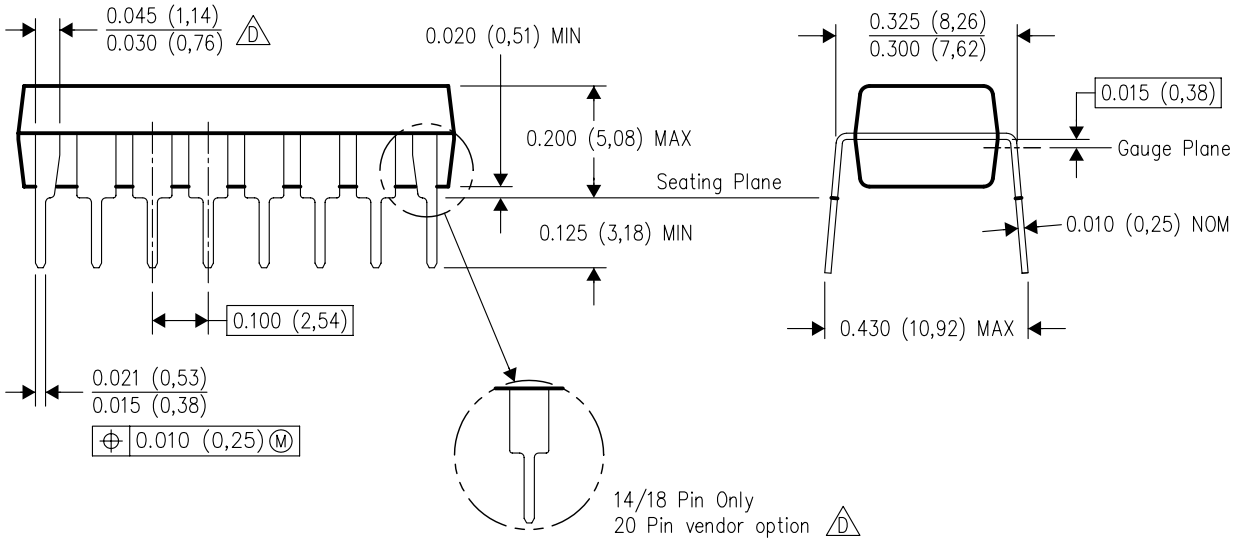
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



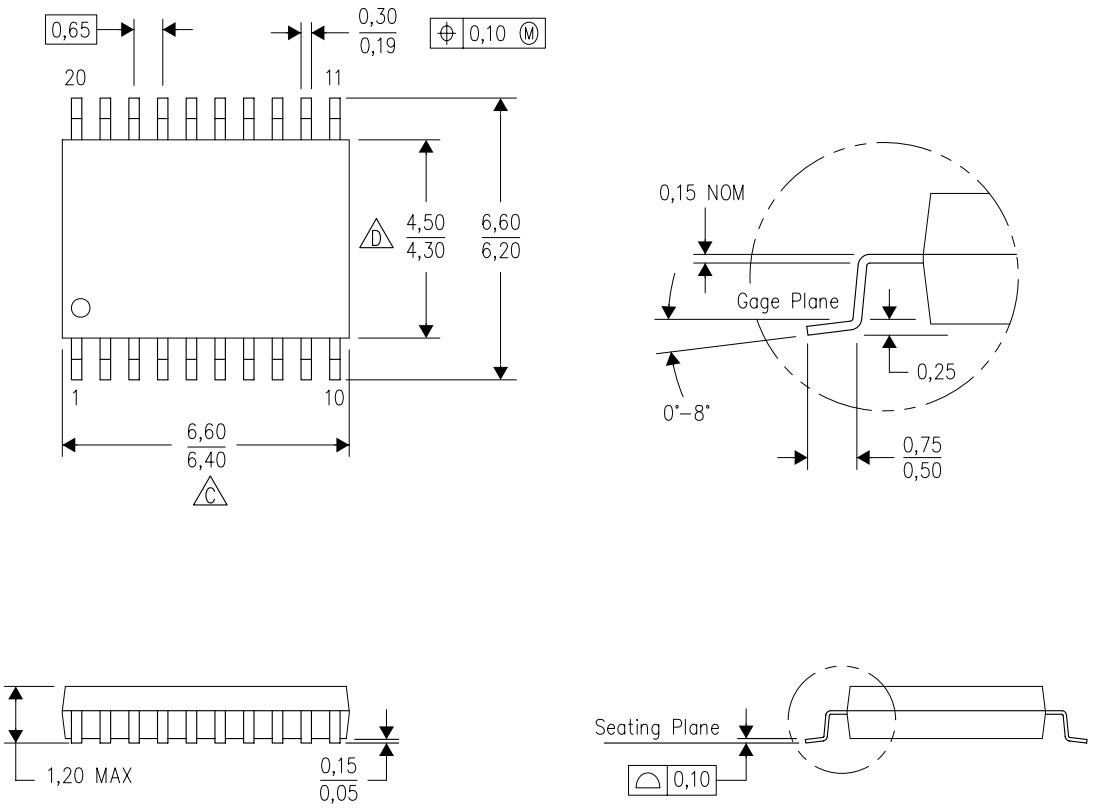
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

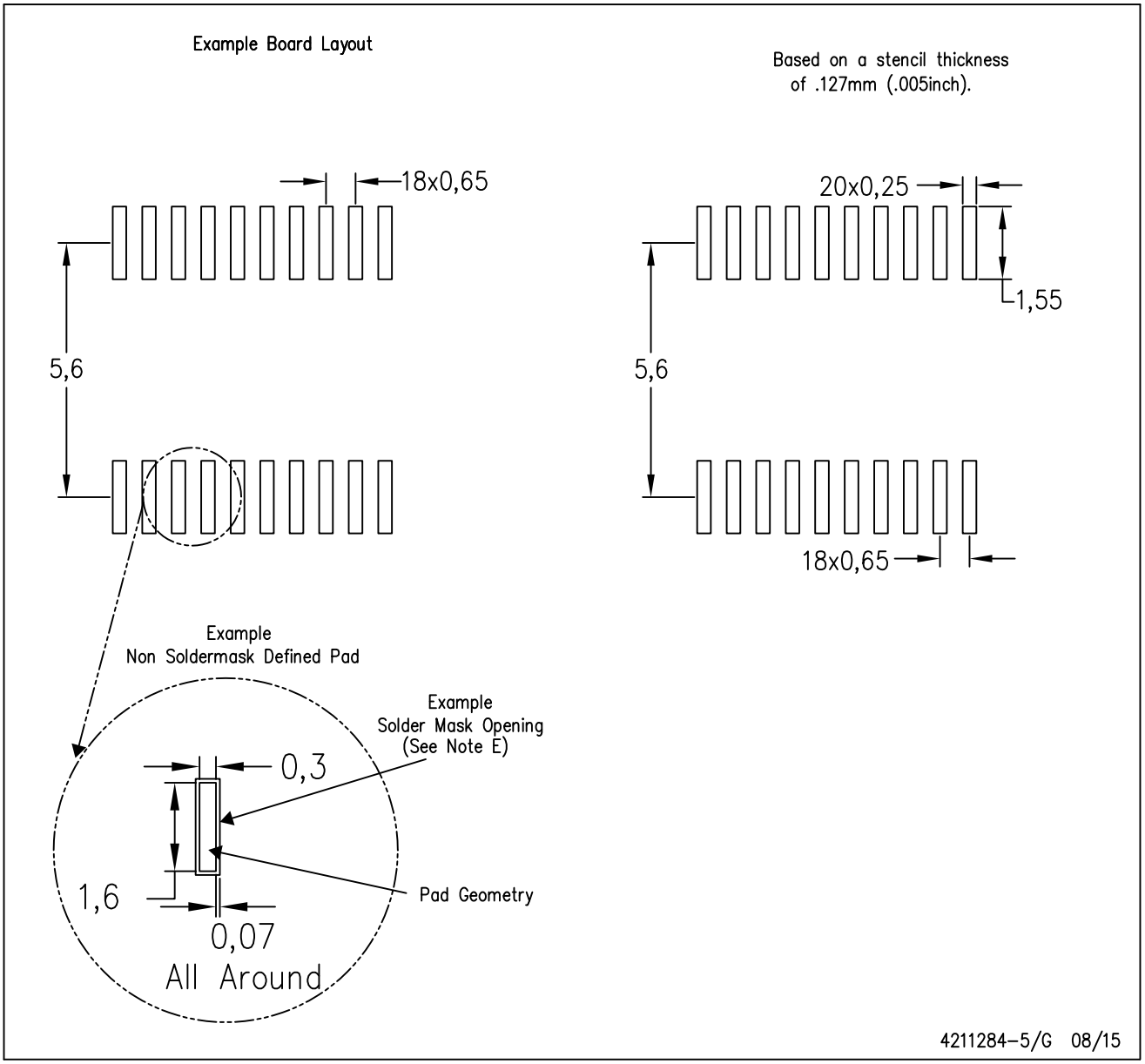
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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