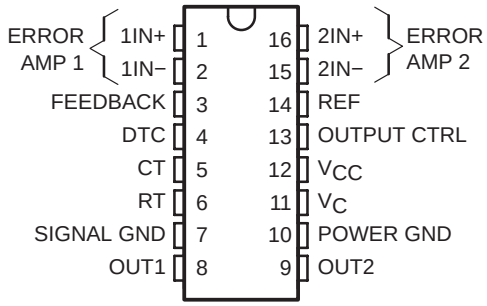
SLVS053D − FEBRUARY 1988 − REVISED NOVEMBER 2003

- **Complete PWM Power-Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Undervoltage Lockout for Low-V_{CC} Conditions**
- **Separate Power and Signal Grounds**

D OR N PACKAGE
(TOP VIEW)



description/ordering information

The TL598 incorporates all the functions required in the construction of pulse-width-modulated (PWM) controlled systems on a single chip. Designed primarily for power-supply control, the TL598 provides the systems engineer with the flexibility to tailor the power-supply control circuits to a specific application.

The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control (DTC) comparator, a pulse-steering flip-flop, a 5-V precision reference, undervoltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise- and fall-time performance for power FET control. The outputs share a common source supply and common power ground terminals, which allow system designers to eliminate errors caused by high current-induced voltage drops and common-mode noise.

The error amplifier has a common-mode voltage range of 0 V to V_{CC} − 2 V. The DTC comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. A synchronous multiple supply operation can be achieved by connecting RT to the reference output and providing a sawtooth input to CT.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation. The output frequency for push-pull applications is one-half the oscillator frequency $\left(f_O = \frac{1}{2\ RT\ CT}\right)$. For single-ended applications: $f_O = \frac{1}{RT\ CT}$.

ORDERING INFORMATION

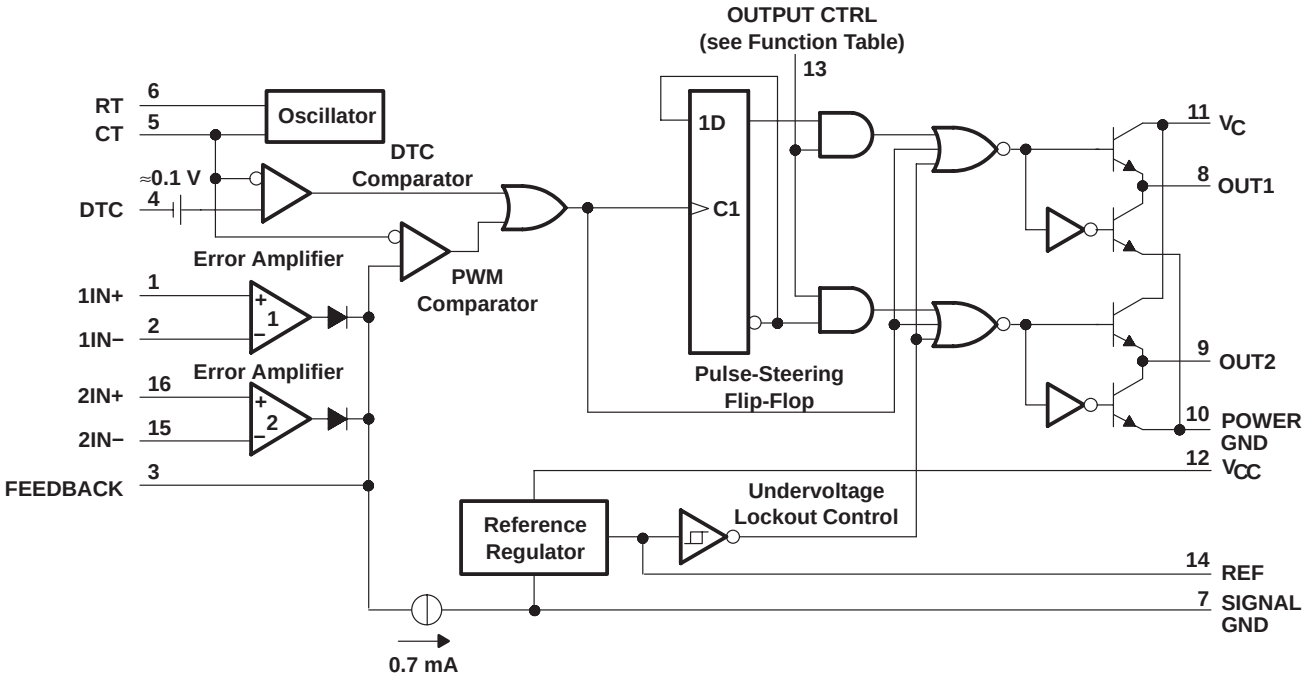
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	TL598CN	TL598CN
	SOIC (D)	Tube of 40	TL598CD	TL598C
		Reel of 2500	TL598CDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT/OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = REF	Normal push-pull operation

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 41 V
Amplifier input voltage, V_I . . . . . V_{CC} + 0.3 V
Collector voltage . . . . . 41 V
Output current (each output), sink or source, I_O . . . . . 250 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the signal ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	7	40	V
V_I	Amplifier input voltage	0	$V_{CC}-2$	V
I_O	Collector voltage		40	V
I_{IL}	Output current (each output), sink or source		200	mA
	Current into feedback terminal		0.3	mA
C_T	Timing capacitor	0.00047	10	μF
R_T	Timing resistor	1.8	500	kΩ
f_{osc}	Oscillator frequency	1	300	kHz
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

reference section (see Note 4)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	V
		T_A = full range	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	25	mV
Output regulation	I_O = 1 mA to 10 mA	T_A = 25°C		1	15	mV
		T_A = full range			50	
Output voltage change with temperature	ΔT_A = MIN to MAX			2	10	mV/V
Short-circuit output current§	REF = 0 V		−10	−48		mA

† Full range is 0°C to 70°C.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 4: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

oscillator section, C_T = 0.001 μF, R_T = 12 kΩ (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1	10	Hz/kHz
Frequency change with temperature#	ΔT_A = full range		70	120	Hz/kHz
	ΔT_A = full range, C_T = 0.01 μF		50	80	

† Full range is 0°C to 70°C.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

Effects of temperature on external R_T and C_T are not taken into account.
NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted) (continued)

error amplifier section (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	FEEDBACK = 2.5 V		2	10	mV
Input offset current	FEEDBACK = 2.5 V		25	250	nA
Input bias current	FEEDBACK = 2.5 V		0.2	1	µA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	FEEDBACK = 0.5 V	0.3	0.7		mA
Output source current (FEEDBACK)	FEEDBACK = 3.5 V	−2			mA
Phase margin at unity gain	FEEDBACK = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply-voltage rejection ratio	FEEDBACK = 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

undervoltage lockout section (see Note 4)

PARAMETER	TEST CONDITIONS‡	MIN	MAX	UNIT
Threshold voltage	T_A = 25°C	4	6	V
	ΔT_A = full range	3.5	6.9	
Hysteresis§	T_A = 25°C	100		mV
	T_A = full range	50		

‡ Full range is 0°C to 70°C.
§ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

output section (see Note 4)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
High-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = −200 mA	12		V
		I_O = −20 mA	13		
Low-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = 200 mA		2	V
		I_O = 20 mA		0.4	
Output-control input current	V_I = V_{ref}			3.5	mA
	V_I = 0.4 V			100	µA

NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted) (continued)

dead-time control section (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (DTC)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	DTC = 0 V	0.45			
Input threshold voltage (DTC)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

pwm comparator section (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75	4.5	V
Input sink current (FEEDBACK)	$V_{(FEEDBACK)}$ = 0.5 V	0.3	0.7		mA

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
NOTE Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

total device (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15	21	mA
		V_{CC} = 40 V		20	26	
Average supply current	DTC = 2 V			15		mA

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

switching characteristics, T_A = 25°C (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output-voltage rise time	CL = 1500 pF, VC = 15 V, VCC = 15 V, See Figure 2		60	150	ns
Output-voltage fall time			35	75	

NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

PARAMETER MEASUREMENT INFORMATION

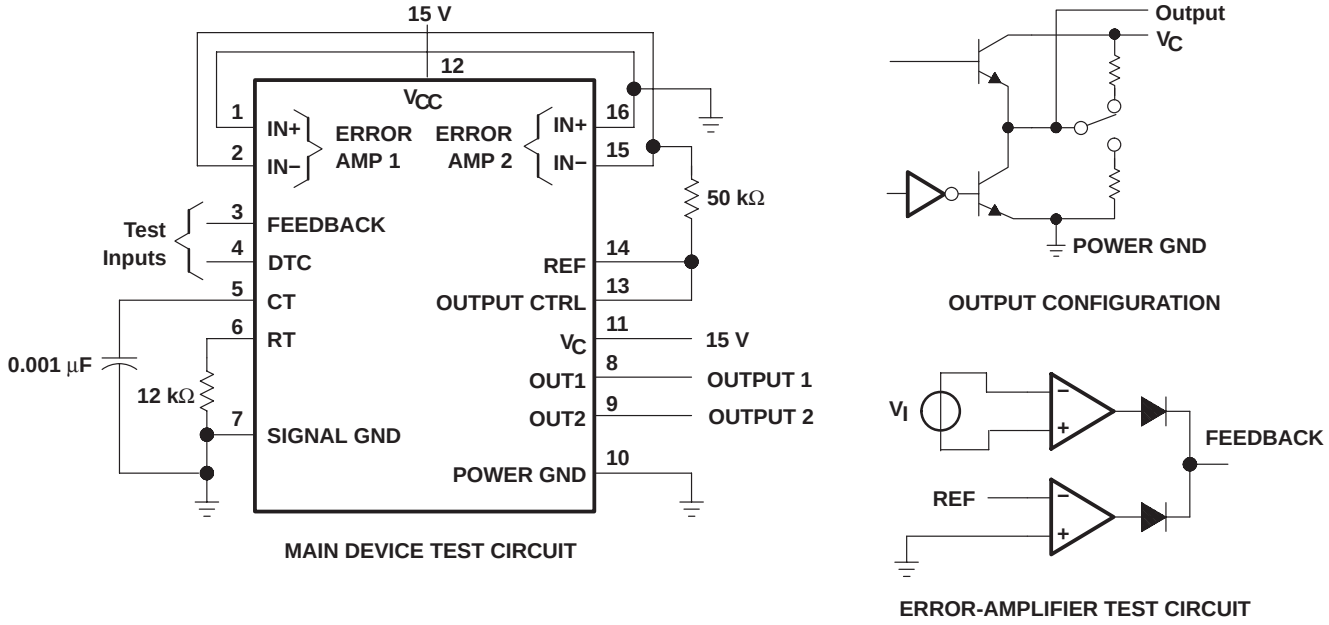


Figure 1. Test Circuits

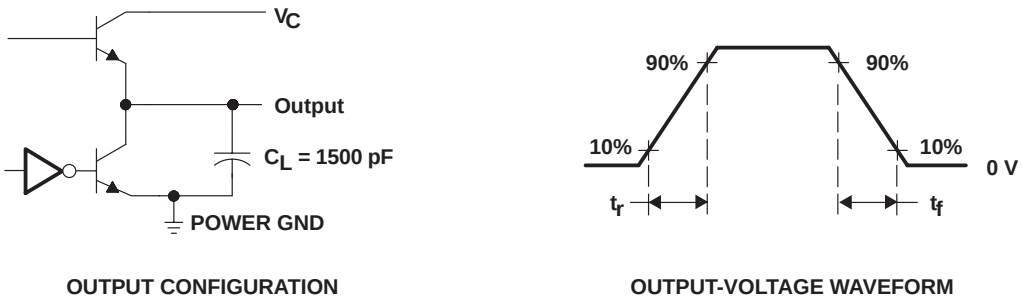
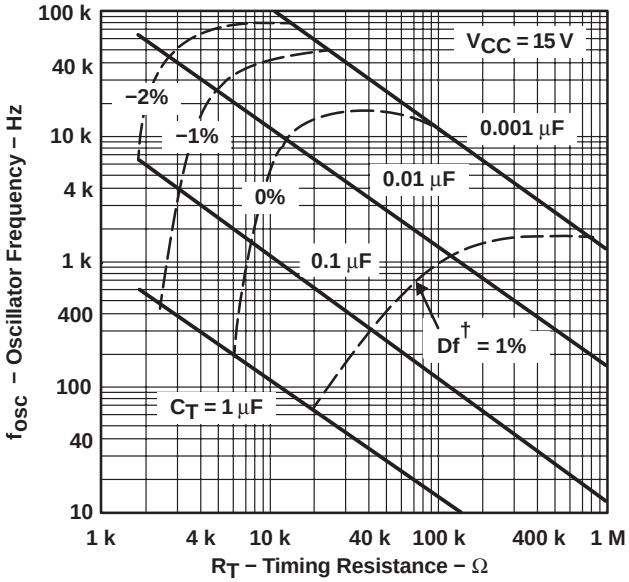


Figure 2. Switching Output Configuration and Voltage Waveform

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE



† Frequency variation (Δf) is the change in predicted oscillator frequency that occurs over the full temperature range.

Figure 3

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

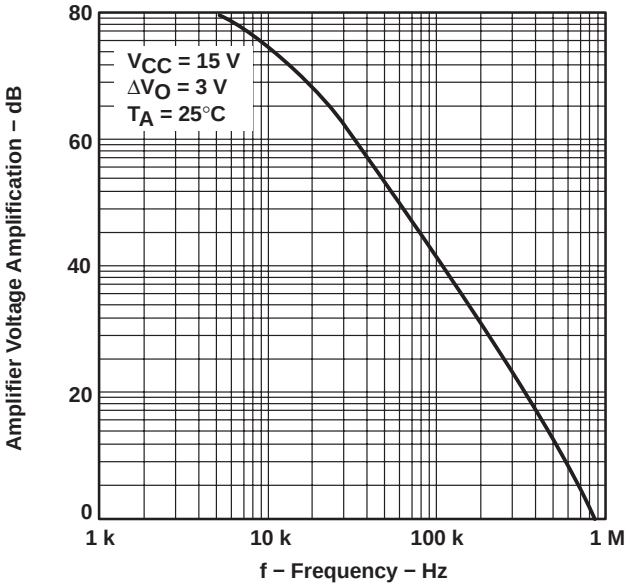


Figure 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9166801QEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL598CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL598C	Samples
TL598CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL598C	Samples
TL598CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL598C	Samples
TL598CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL598C	Samples
TL598CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL598CN	Samples
TL598CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL598CN	Samples
TL598MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL598MJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL598QD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125		
TL598QDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125		
TL598QN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

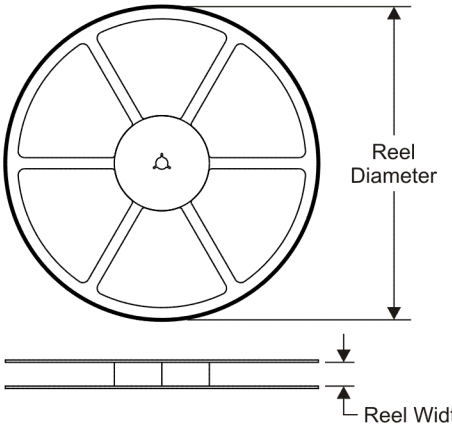
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

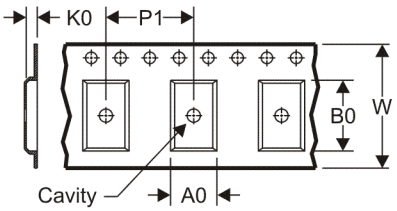
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

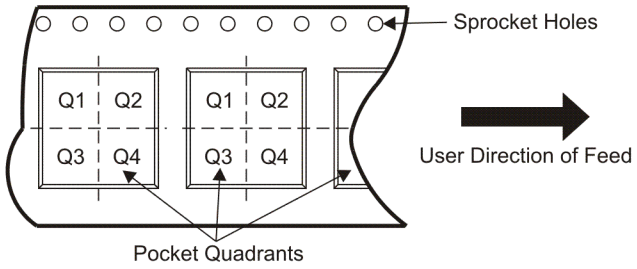


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

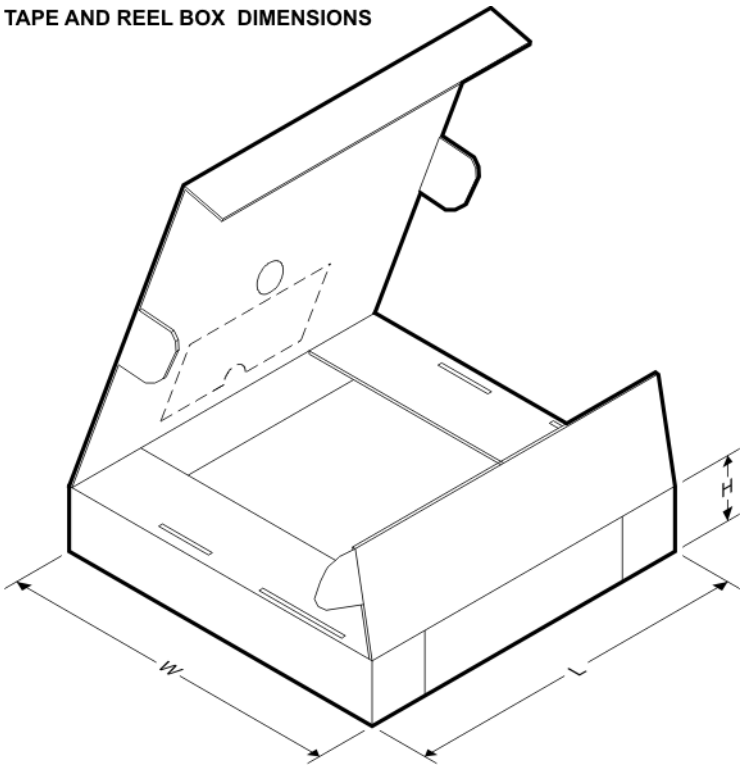
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL598CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



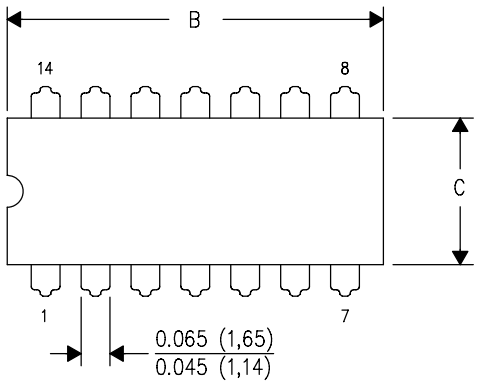
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL598CDR	SOIC	D	16	2500	333.2	345.9	28.6

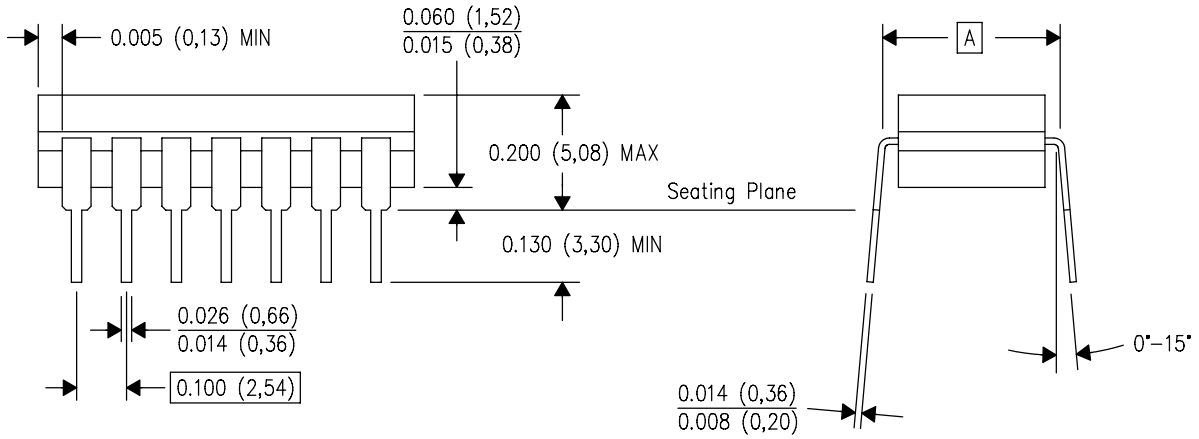
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

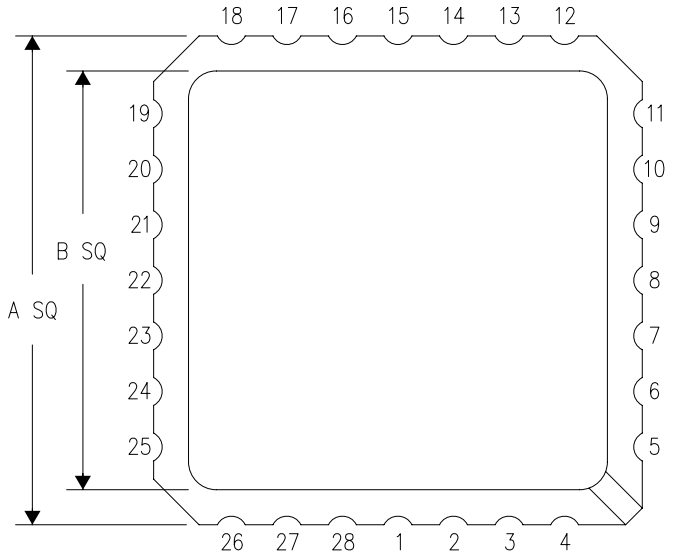


4040083/F 03/03

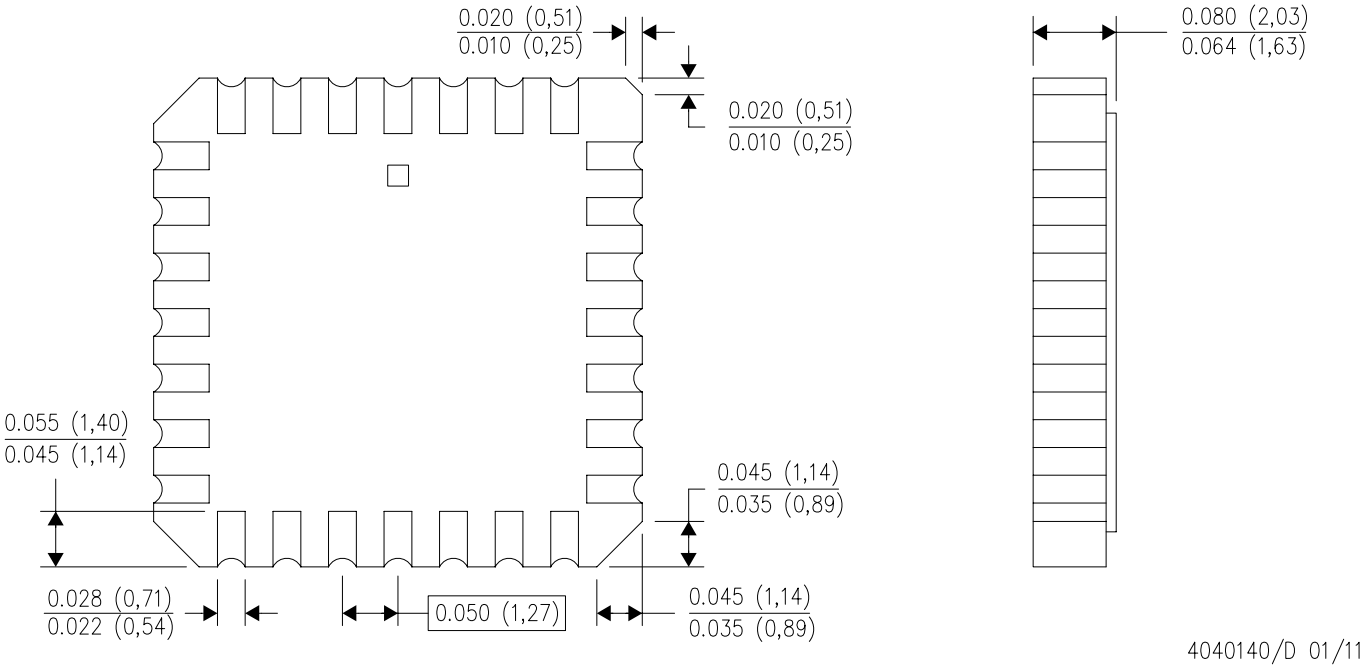
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



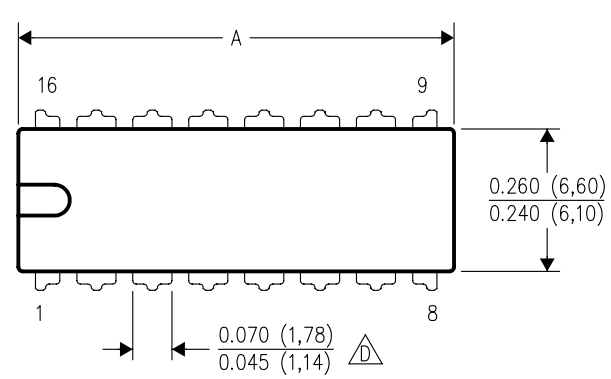
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

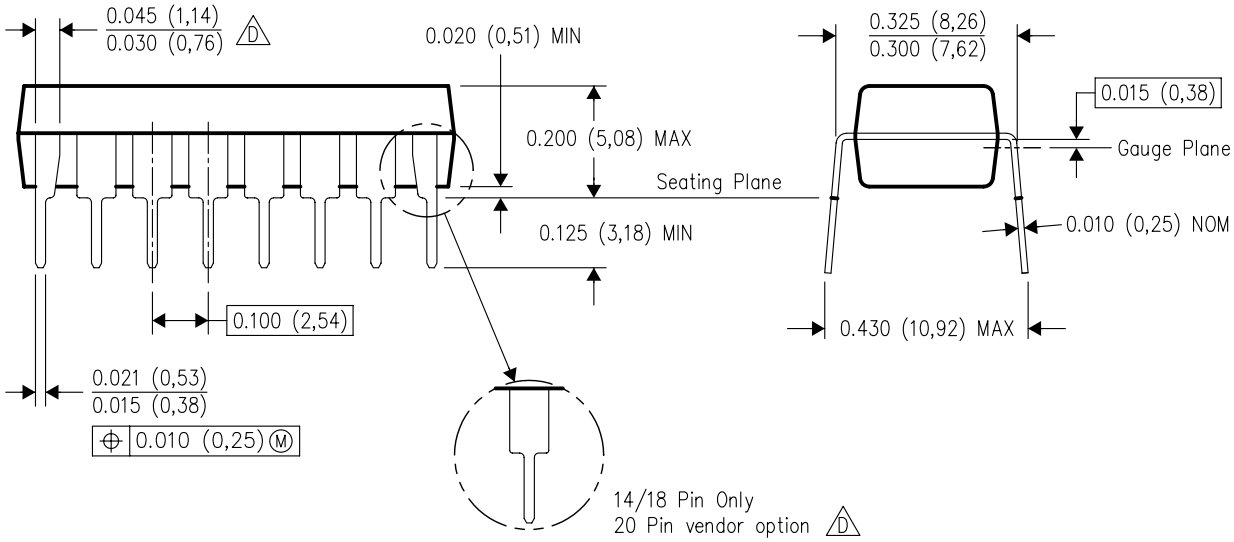
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



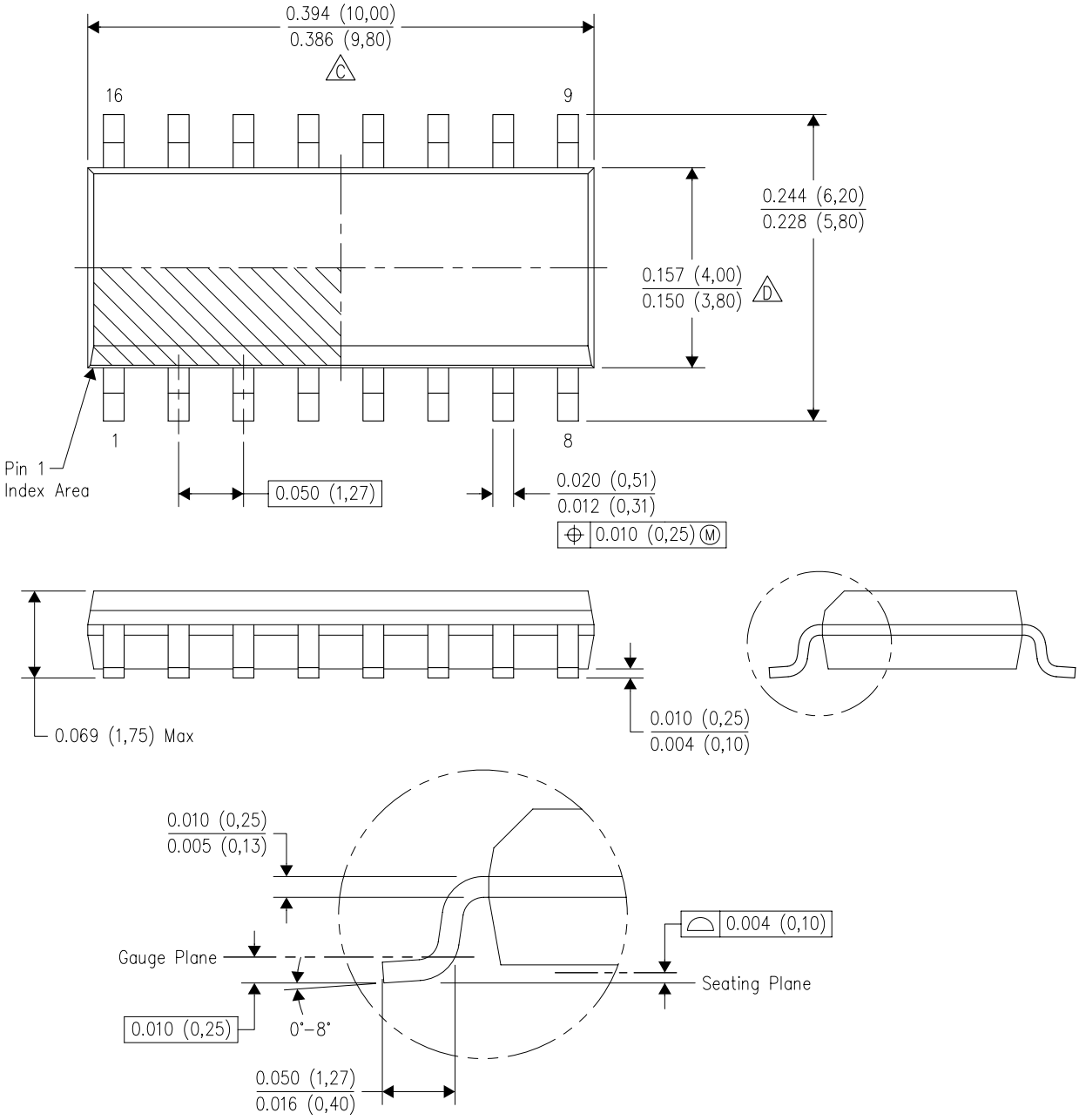
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

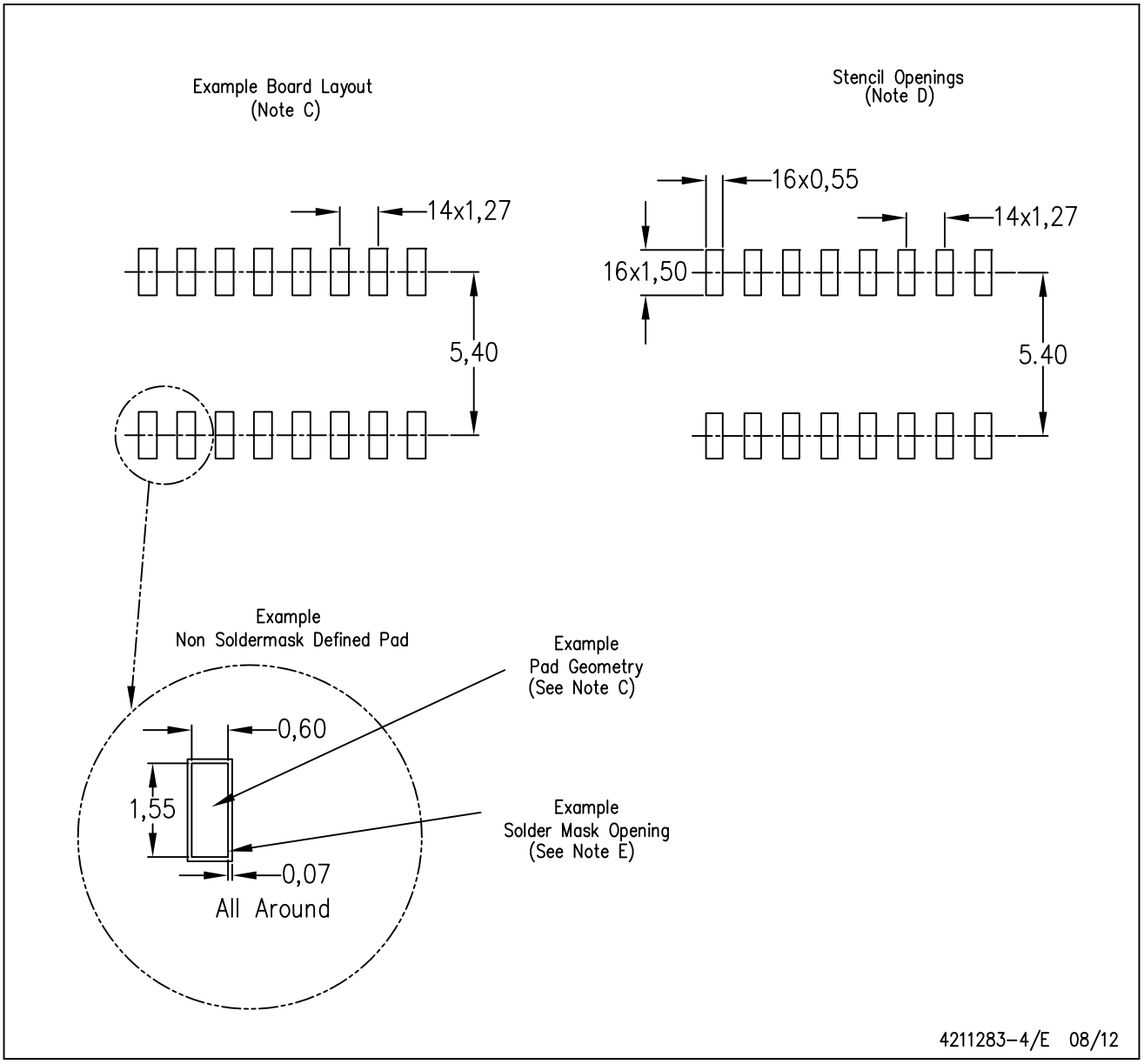
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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