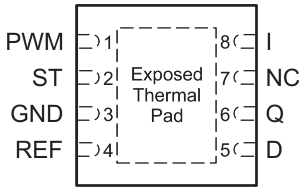
ADJUSTABLE LED DRIVER

Check for Samples: TL4242-Q1

FEATURES

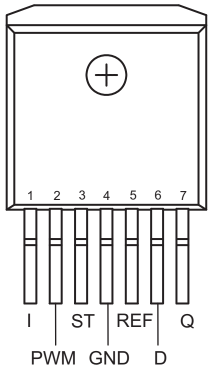
- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range for QFN package**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range for SFM package**
  - **Device HBM ESD Classification Level H1C**
  - **Device CDM ESD Classification Level C3B**
- **Adjustable Constant Current up to 500 mA (±5%)**
- **Wide Input-Voltage Range up to 42 V**
- **Low Dropout Voltage**
- **Open-Load Detection**
- **Overtemperature Protection**
- **Short-Circuit Proof**
- **Reverse-Polarity Proof**

DRJ (QFN) PACKAGE
(TOP VIEW)



NC – No internal connection

KTT (SFM) PACKAGE
(TOP VIEW)



DESCRIPTION

The TL4242-Q1 is an integrated adjustable constant-current source, driving loads up to 500 mA. One can adjust the output current level through an external resistor. The device design is for supplying high-power LEDs (for example, OSRAM Dragon LA W57B) under the severe conditions of automotive applications, resulting in constant brightness and extended LED lifetime. The device comes in the DRJ (QFN) package. Protection circuits prevent damage to the device in case of overload, short circuit, reverse polarity, and overheat. The device provides the connected LEDs protection against reverse polarity as well as excess voltages up to 45 V.

The integrated PWM input of the TL4242-Q1 permits LED brightness regulation by pulse-width modulation (PWM). The high input impedance of the PWM input, allows operating the LED driver as a protected high-side switch.

An external shunt resistor in the ground path of the connected LEDs senses the LED current. A regulation loop holds the voltage drop at the shunt resistor at a constant level of 177 mV (typical). The selection of the shunt resistance, R_{REF}, sets the constant-current level. Calculate the typical output current using the equation:

$$I_{Q,typ} = \frac{V_{REF}}{R_{REF}}$$

where V_{REF} is the reference voltage (typically 177 mV) (see *Reference Electrical Characteristics*). The equation applies for R_{REF} = 0.39 Ω to 10 Ω.

The output current is shown as a function of the reference resistance in . With the PWM input, One can regulate the LED brightness through the duty cycle. Also, PWM = L sets the TL4242-Q1 in sleep mode, resulting in a very low current consumption of < 1 μA (typical). The high impedance of the PWM input (see) permits the use of the PWM pin as an enable input.

ORDERING INFORMATION[1]

T_A	ORDERABLE PART NUMBER[2]	TOP-SIDE MARKING
–40°C to 105°C	TL4242TDRJRQ1	4242T
–40°C to 125°C	TL4242QKTTRQ1	TL4242Q

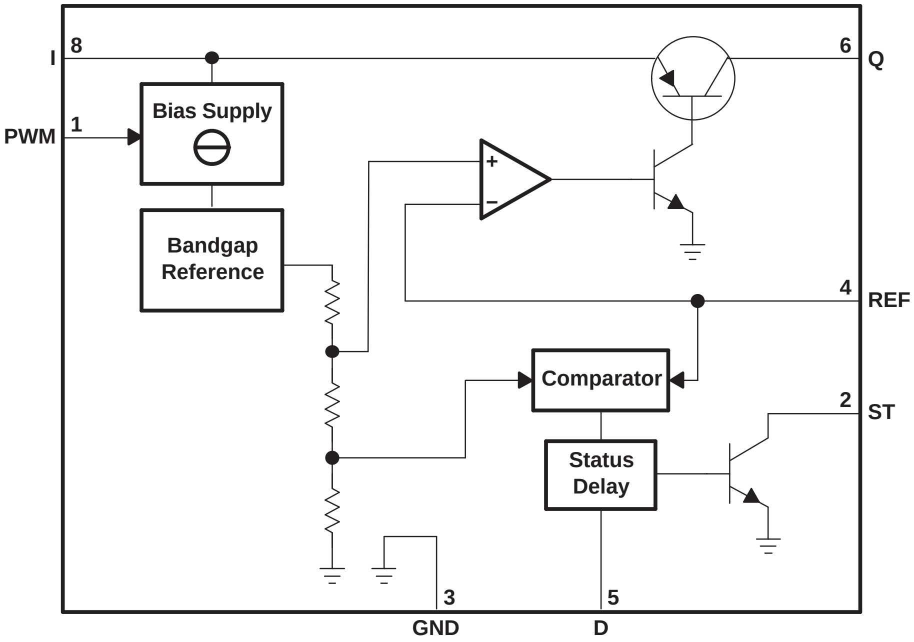
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN FUNCTIONS

NAME	NO.		DESCRIPTION
	DRJ	KTT	
D	5	6	Status delay. To set status reaction delay, connect to GND with a capacitor. For no delay, leave open.
GND	3	4	Ground
NC	7	N/A	No internal connection
PWM	1	2	Pulse-width modulation input. If not used, connect to I.
Q	6	7	Output
REF	4	5	Reference input. Connect to a shunt resistor.
ST	2	3	Status output. Open-collector output. Connect to an external pullup resistor (R_{PULLUP} ≥ 4.7 kΩ).
I	8	1	Input. Connect directly to GND as close as possible to the device with a 100-nF ceramic capacitor.
Thermal pad	–	–	Solder the thermal pad directly to the PCB. Connect to ground or leave floating

Figure 1. FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–42	45	V
V_I	Input voltage range	D	–0.3	7	V
		PWM	–40	40	V
		REF	–1	16	V
V_O	Output voltage range	Q	–1	41	V
		ST	–0.3	40	V
I_O	Output current range	PWM		±1	mA
		REF		±2	mA
		ST		±5	mA
T_J	Virtual-junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–55	150	°C
ESD	Electrostatic discharge rating	Human-body model (HBM) AEC-Q100 Classification Level H1C		1500	V
		Machine model (MM) AEC-Q100 Classification Level M3		200	
		Charged-device model (CDM) AEC-Q100 Classification Level C3B		1000	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

THERMAL INFORMATION

THERMAL METRIC[1]		TL4242-Q1		UNIT
		DRJ (8 PINS)	KTT (7 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	39	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	31.5	34.7	
θ_{JB}	Junction-to-board thermal resistance	15.5	8.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.7	
ψ_{JB}	Junction-to-board characterization parameter	15.6	8.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.8	0.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	42	V
V_{ST}	Status (ST) output voltage		16	V
V_{PWM}	PWM voltage	0	40	V
C_D	Status delay (D) capacitance	0	2.2	µF
R_{REF}	Reference (REF) resistor	0	10	Ω
T_A	Operating free-air temperature, QFN	–40	105	°C
T_A	Operating free-air temperature, SFM	–40	125	°C

OVERALL DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = –40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{qL}	Supply current	V_Q = 6.6 V		12	22	mA
I_{qOFF}	Supply current, off mode	PWM = L, T_J < 85°C		0.1	2	µA

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = –40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Output current	$V_Q – V_{REF}$ [1] = 6.6 V	357	376	395	mA
		$V_Q – V_{REF}$ = 6.6 V, R_{REF} = 1 Ω	168	177	185	
		$V_Q – V_{REF}$ = 6.6 V, R_{REF} = 0.39 Ω	431	454	476	
		$V_Q – V_{REF}$ = 5.4 V to 7.8 V, V_I = 9 V to 16 V	357	376	395	
I_{Qmax}	Output current limit	R_{REF} = 0 Ω		600		mA
V_{dr}	Drop voltage	I_Q = 300 mA		0.35	0.7	V

(1) $V_Q – V_{REF}$ equals the forward voltage sum of the connected LEDs (see).

PWM INPUT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = -40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PWM,H}$	High-level PWM voltage		2.6			V
$V_{PWM,L}$	Low-level PWM voltage				0.7	V
$I_{PWM,H}$	High-level PWM input current	V_{PWM} = 5 V		220	500	µA
$I_{PWM,L}$	Low-level PWM input current	V_{PWM} = 0 V	–1		1	µA
$t_{PWM,ON}$	Delay time, turnon	70% of I_{Qnom}, see Figure 8	0	15	40	µs
$t_{PWM,OFF}$	Delay time, turnoff	30% of I_{Qnom}, see Figure 8	0	15	40	µs

REFERENCE (REF) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = –40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	R_{REF} = 0.39 Ω to 1 Ω	168	177	185	mV
I_{REF}	Reference input current	V_{REF} = 180 mV	–1	0.1	1	µA

STATUS OUTPUT (ST) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = –40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IQL}	Lower status-switching threshold	ST = L	15	25		mV
V_{IQH}	Upper status-switching threshold	ST = H		30	40	mV
V_{STL}	Low-level status voltage	I_{ST} = 1.5 mA			0.4	V
I_{STLK}	Leakage current	V_{ST} = 5 V			5	µA

STATUS DELAY (D) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_A = –40°C to 105°C (QFN), T_A = –40°C to 125°C (SFM), all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STHL}	Delay time, status reaction	C_D = 47 nF, ST H→L	6	10	14	ms
t_{STLH}	Delay time, status release	C_D = 47 nF, ST L→H		10	20	µs

TYPICAL CHARACTERISTICS

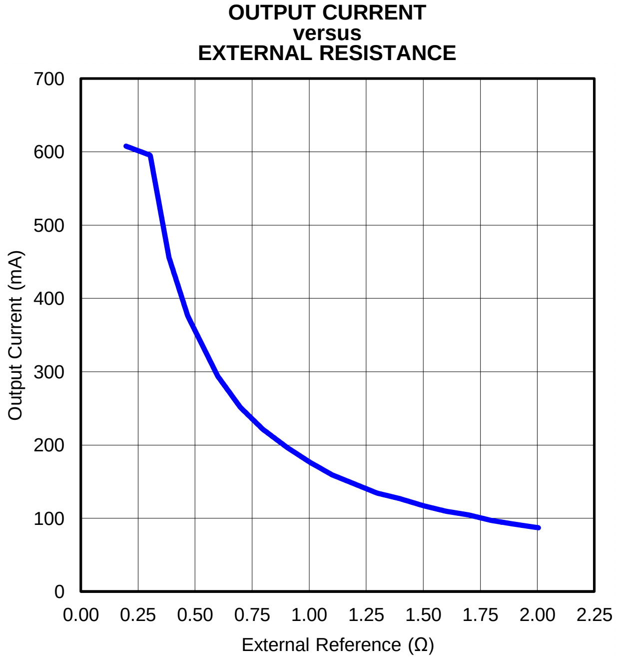


Figure 2.

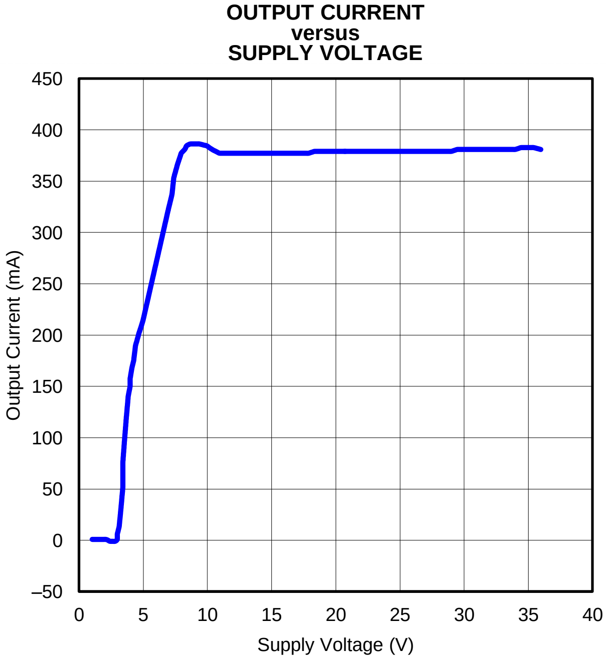


Figure 3.

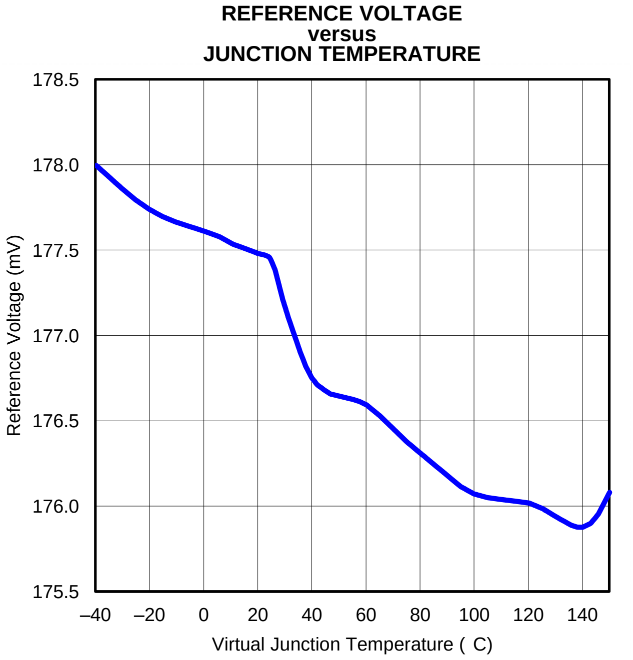


Figure 4.

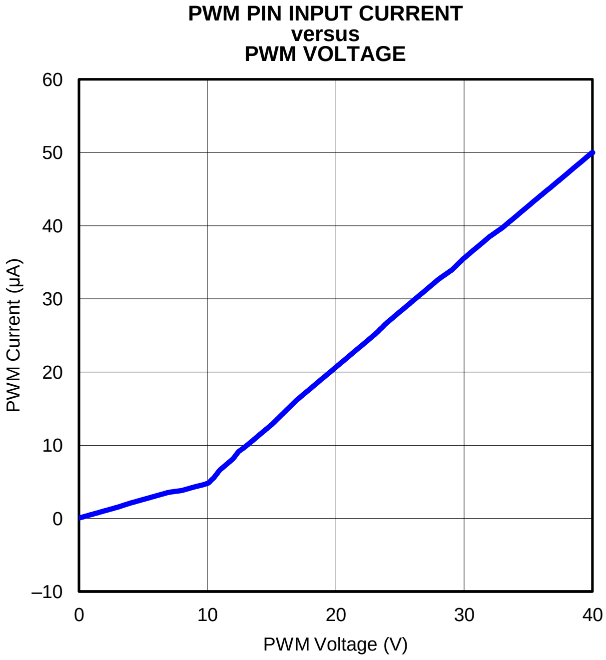


Figure 5.

TYPICAL CHARACTERISTICS (continued)

ST PIN VOLTAGE
versus
ST PIN PULLDOWN CURENT

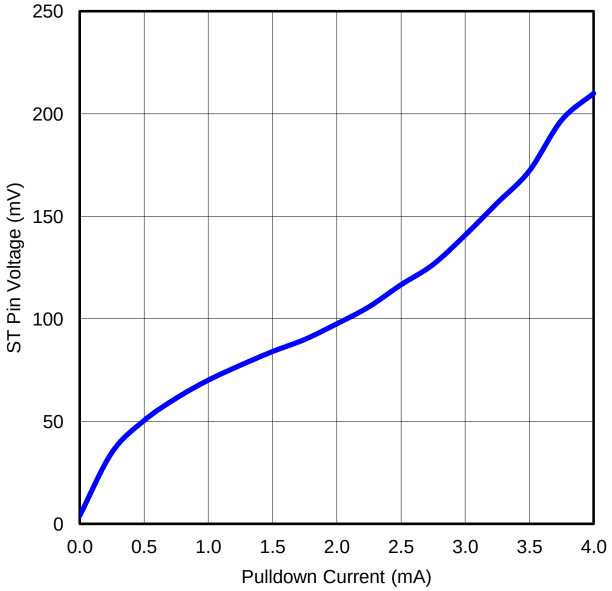


Figure 6.

APPLICATION INFORMATION

Figure 7 shows a typical application with the TL4242-Q1 LED driver. A supply current adjusted by the R_{REF} resistor drives the three LEDs, preventing brightness variations due to forward voltage spread of the LEDs. An appropriate duty cycle applied to the PWM pin can compensate through software for the luminosity spread arising from the LED production process. Therefore, it is not necessary to select LEDs for forward voltage or luminosity classes. The minimum supply voltage calculates as the sum of the LED forward voltages, the TL4242-Q1 drop voltage (maximum 0.7 V at an LED current of 300 mA), and the maximum voltage drop at the shunt resistor R_{REF} of 185 mV.

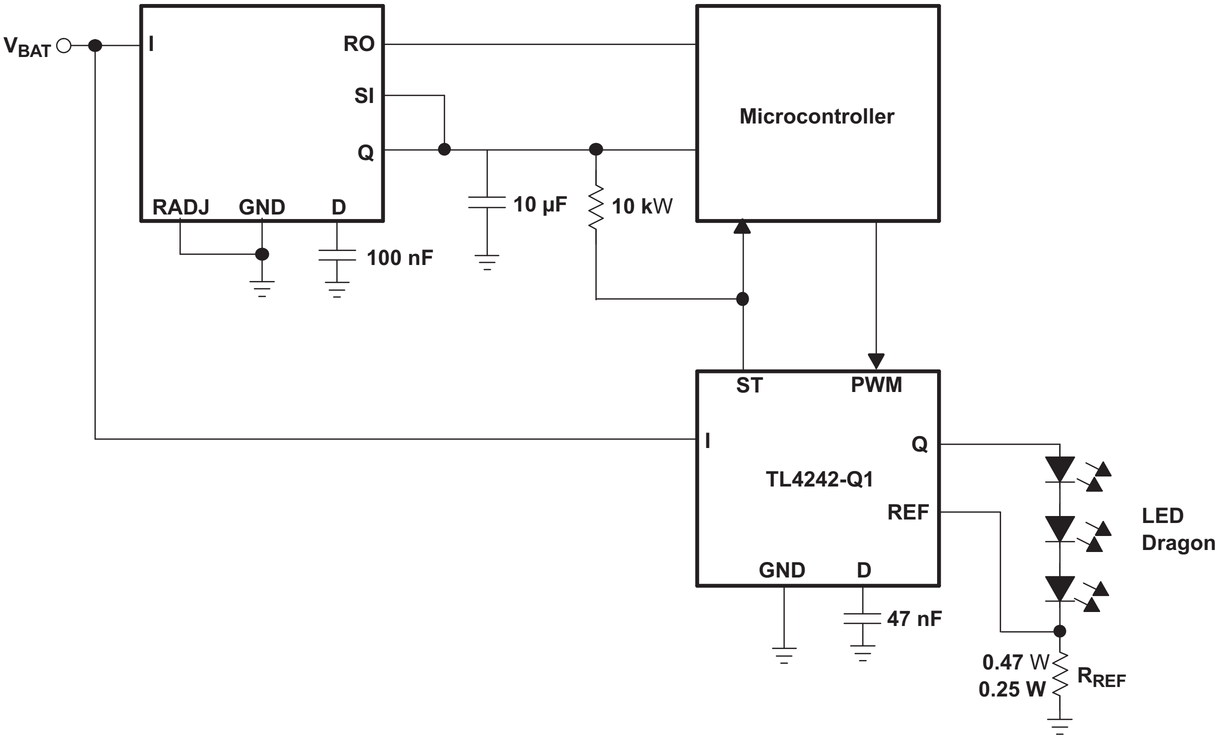


Figure 7. Application Circuit

The status output of the LED driver (ST) detects an open-load condition, enabling supervision of correct LED operation. A voltage drop at the shunt resistor (R_{REF}) below 25 mV (typical) detects an LED failure. In this case, the status output pin (ST) goes low after a delay time adjustable by an optional capacitor connected to pin D.

Figure 8 shows the functionality and timing of ST and PWM. One can adjust the status delay through the capacitor connected to pin D. Delay time scales linearly with the capacitance, C_D:

$$t_{STHL,typ} = \frac{C_D}{47\text{ nF}} \times 10\text{ ms}$$

$$t_{STLH,typ} = \frac{C_D}{47\text{ nF}} \times 10\ \mu\text{s}$$

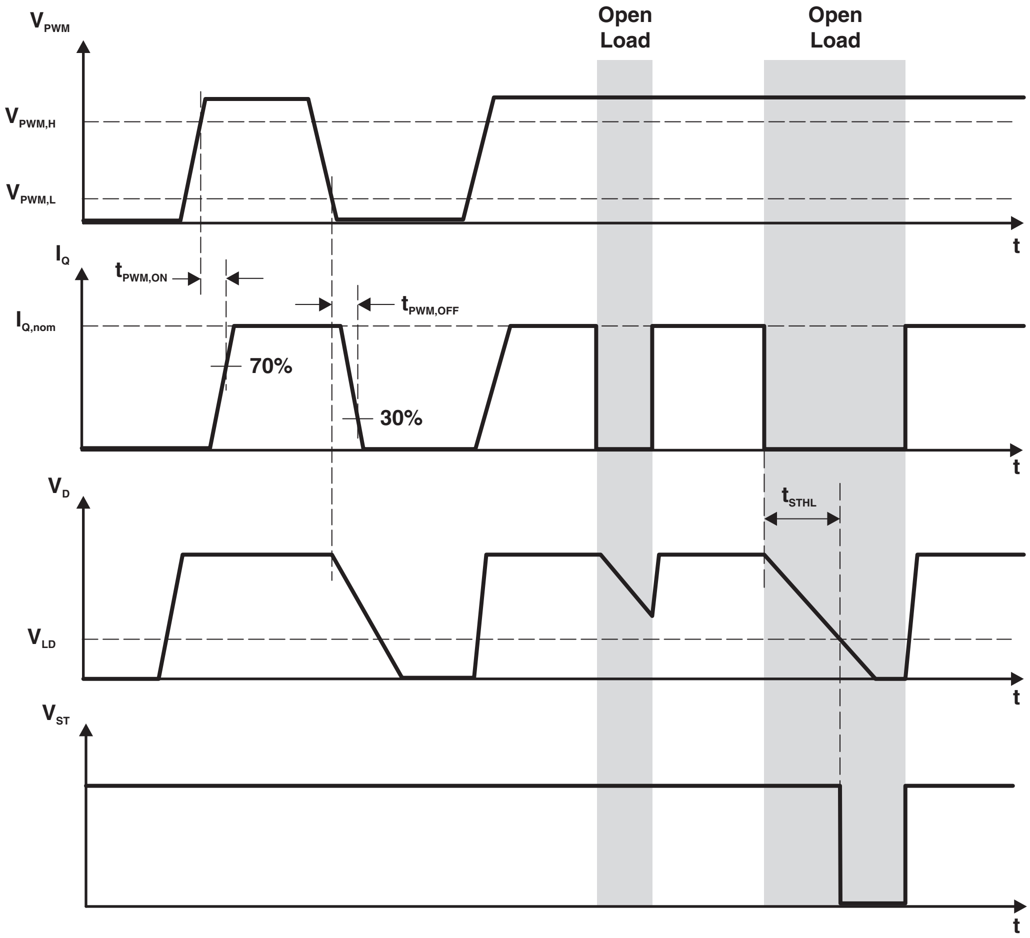


Figure 8. Function and Timing Diagram

Stoplight and Taillight Application

For many automobiles, the same set of LEDs illuminates both taillights and stoplights. Thus, the LEDs must operate at two different brightness levels, full brightness for the stoplight and 10% to 25% brightness for the taillight. The easiest way to achieve the different brightness is dimming by pulse-width modulation (PWM), which holds the color spectrum of the LED over its whole brightness range. The maximum current that passes through the LED is programmable by sense resistor R_{REF}.

Obtain the maximum current, I_{Qmax}, that passes through the LEDs by the following expression:

$$I_{Q\max} = \frac{V_{REF}}{R_{REF}}$$

For example, if R_{REF} equals 1 Ω, as V_{REF} is a fixed value range from 168 mV to 185 mV, I_{Qmax} should be 168 mA to 185 mA.

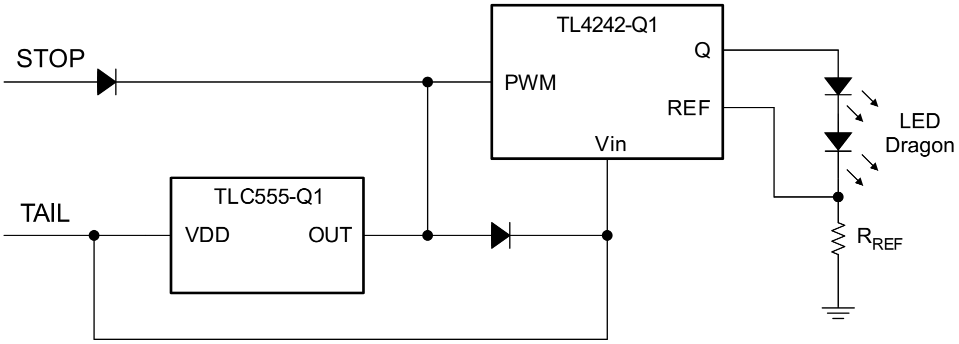


Figure 9. Stoplight and Taillight Application Circuit

Figure 9 shows the application circuit of the stoplight and taillight including an automotive-qualified timer, TLC555-Q1, the duty cycle of which is programmable by two external resistors. One can see that driving the STOP signal high pulls the PWM pin constantly high, creating 100% duty cycle. Thus the LEDs operate at full brightness. When the TAIL signal is high, the LEDs operate at 25% brightness because the TLC555-Q1 timer is programmed at a fixed duty cycle of 25%.

Thermal Information

This device operates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to the following formula:

$$P = (V_I - V_O) \times I_O + V_I \times I_Q$$

In the formula, V_I represents the input voltage of the device, V_O stands for the output voltage, and I_O means the output current of LED and I_Q is the quiescent current dissipated by the device. The very small value of I_Q sometimes allows one to neglect it.

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + \theta_{JA} \times P$$

PCB Design Guideline

In order to prevent thermal shutdown, T_J must be less than 150ºC. If the input voltage is very high, the power dissipation might be large. Currently there is the KTT (DDPAK) package which has good thermal impedance, but at the same time, the PCB layout is also very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximjum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85 percent.

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Added new graph to Typical Characteristics	6

Changes from Revision C (October 2012) to Revision D	Page
• Changed minimum storage temperature to –55ºC	3

Changes from Revision B (September 2012) to Revision C	Page
• Added Stoplight and Taillight Application section	9
• Added Thermal Information section	10
• Added PCB Desogm Guideling section	10

Changes from Revision A (August, 2012) to Revision B	Page
• Removed package column in ordering information table.	2
• Manually appended mechanical data, thermal pad data, and package option addendum	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL4242QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL4242Q	Samples
TL4242TDRJRQ1	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	4242T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL4242-Q1 :

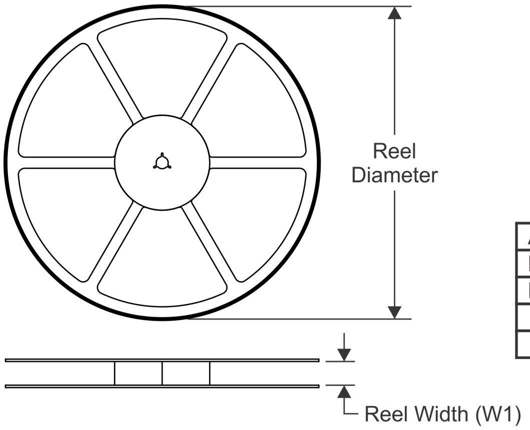
- Catalog: TL4242

NOTE: Qualified Version Definitions:

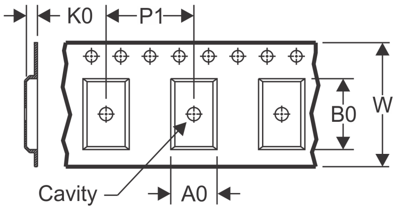
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

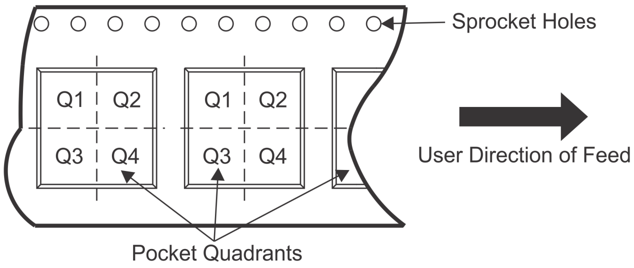


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

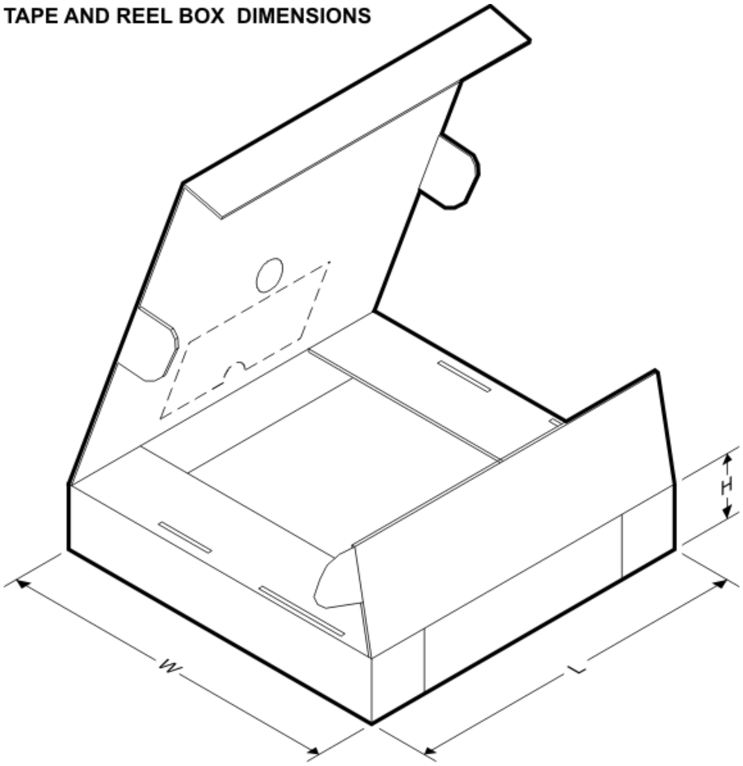
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4242QKTTRQ1	DDPAK/ TO-263	KTT	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL4242TDRJRQ1	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

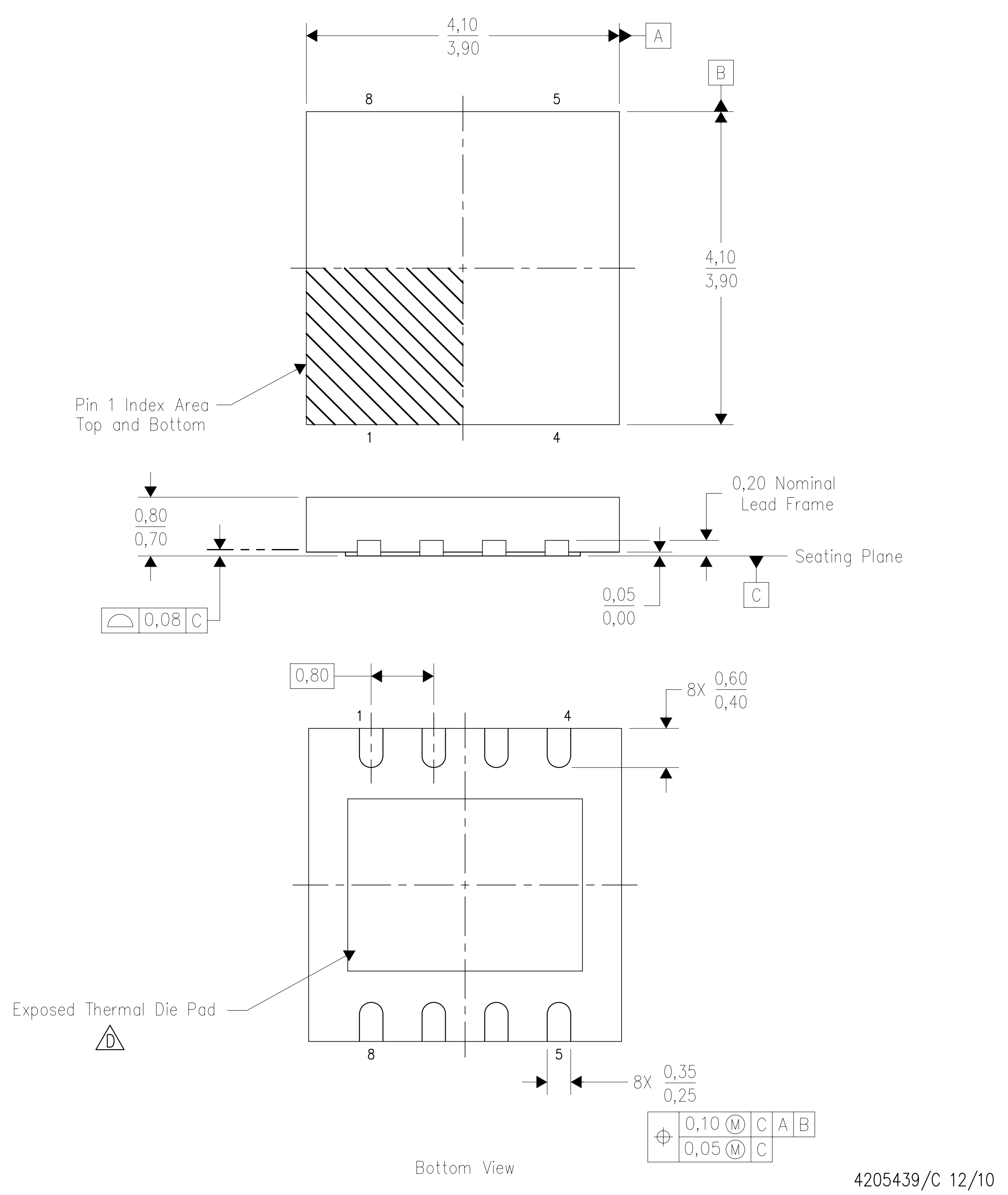
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4242QKTTRQ1	DDPAK/TO-263	KTT	7	500	340.0	340.0	38.0
TL4242TDRJRQ1	SON	DRJ	8	1000	210.0	185.0	35.0

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- △D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO–229 variation WGGB.

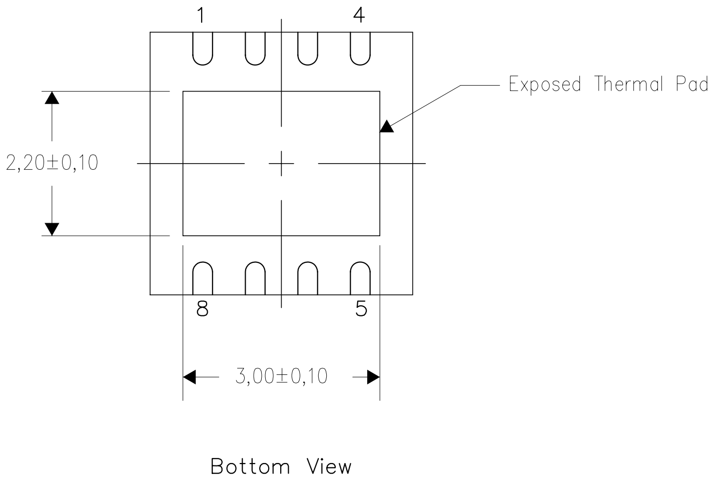
DRJ (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

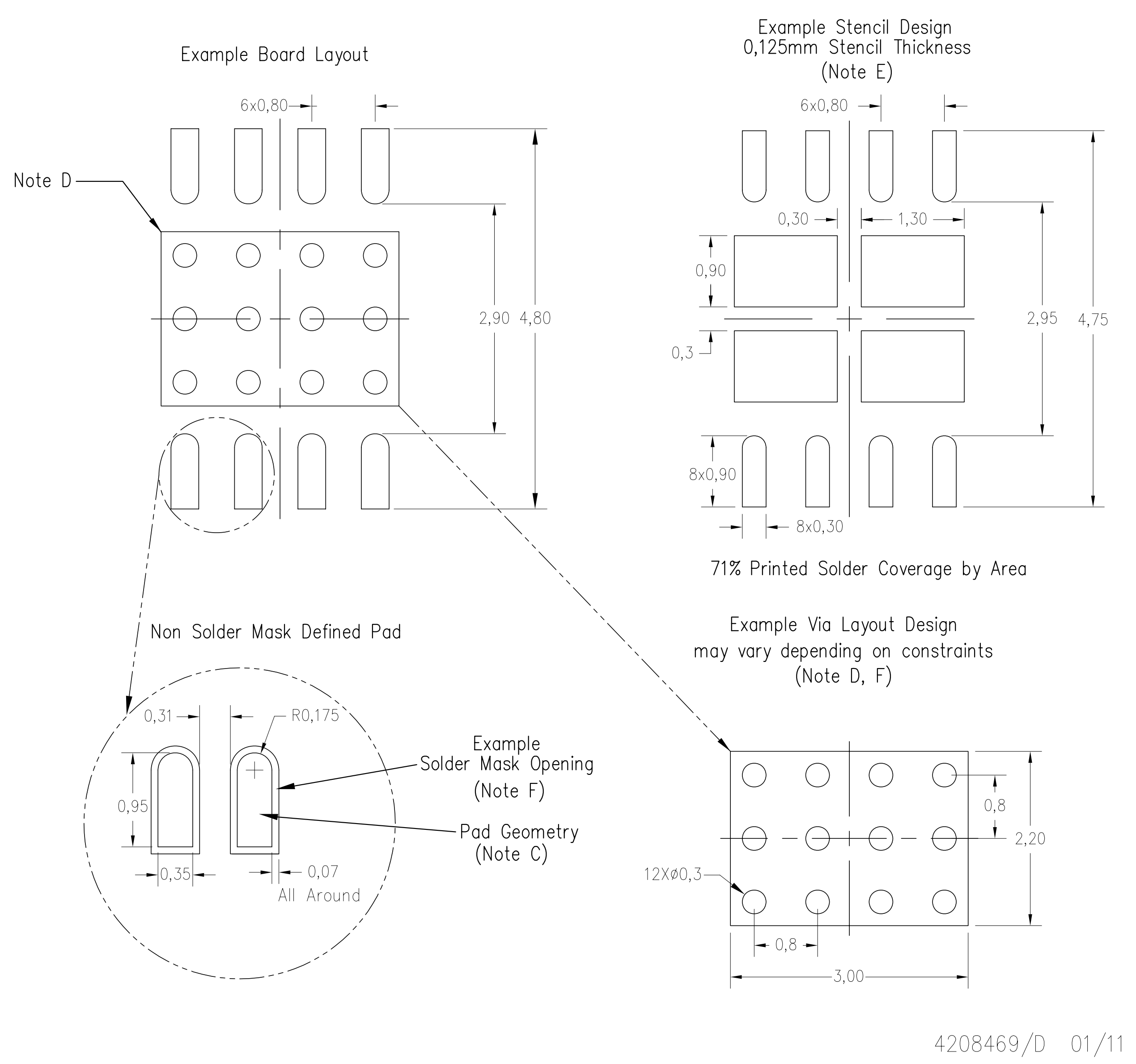


Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S-PWSON-N8) SMALL PACKAGE OUTLINE NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

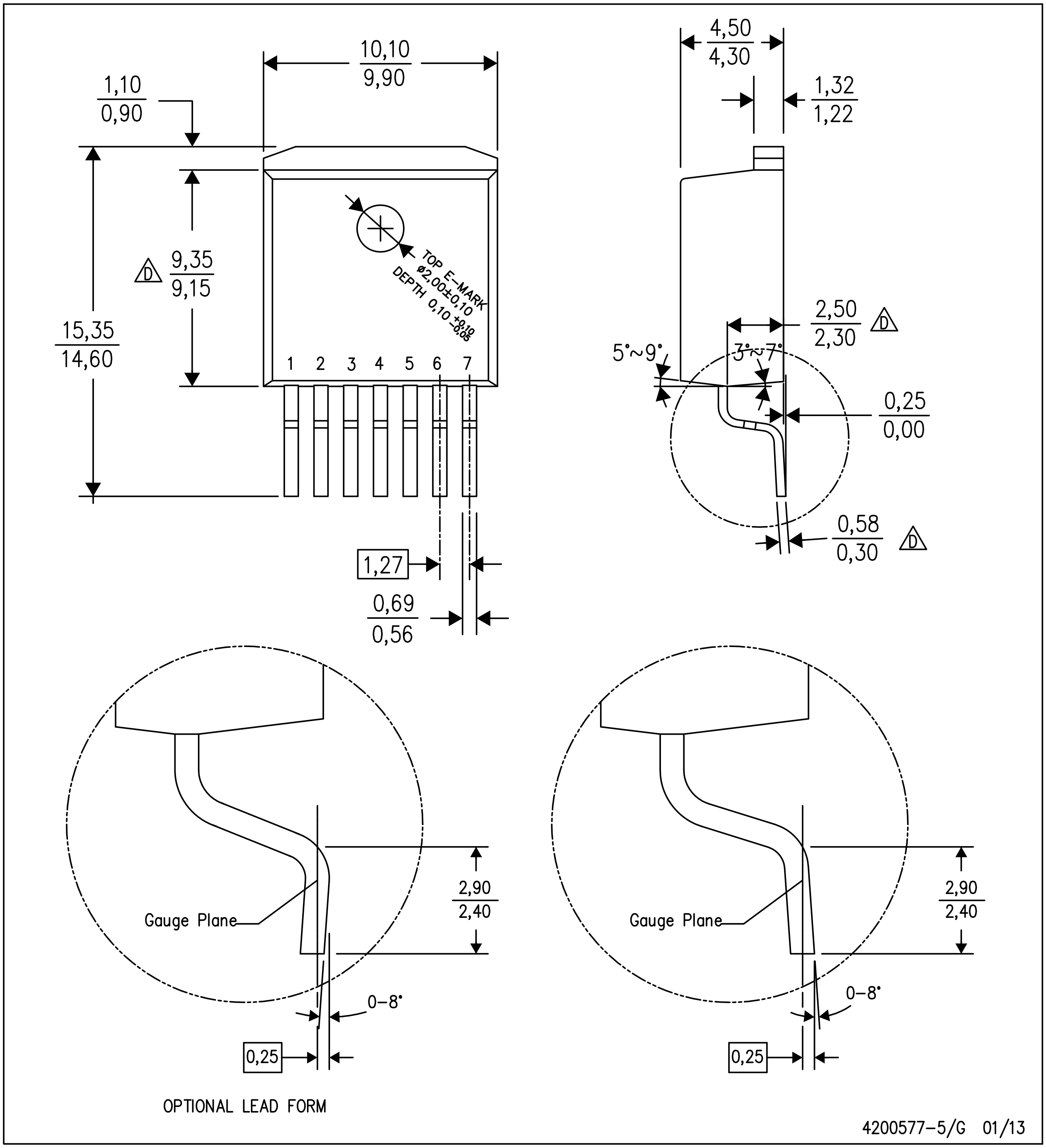
C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

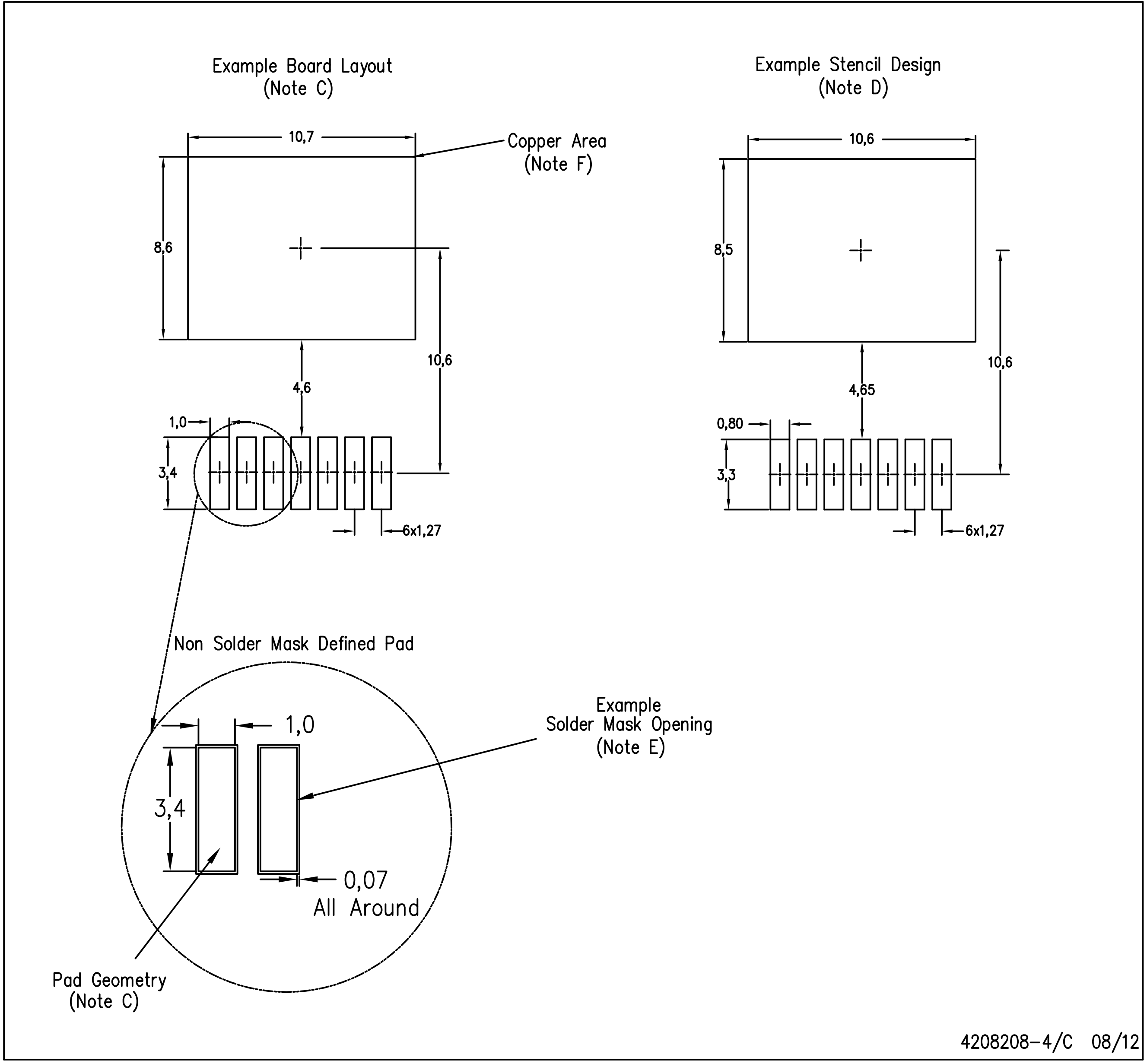
KTT (R–PSFM–G7) PLASTIC FLANGE–MOUNT PACKAGE



4200577–5/G 01/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0,13 per side.
- D. Falls within JEDEC TO–263 AB.

KTT (R–PSFM–G7) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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