PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE

Check for Samples: TL4050-Q1

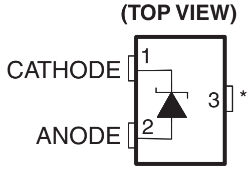
FEATURES

- **Qualified for Automotive Applications**
- **Fixed Output Voltages of 2.048 V, 2.5 V, 4.096 V, 5 V**
- **Tight Output Tolerances and Low Temperature Coefficient**
  - **Max 0.1%, 50 ppm/°C – A Grade**
  - **Max 0.2%, 50 ppm/°C – B Grade**
  - **Max 0.5%, 50 ppm/°C – C Grade**
- **Low Output Noise: 41 μV_{RMS} Typ**
- **Wide Operating Current Range: 60 μA Typ to 15 mA**
- **Stable With All Capacitive Loads; No Output Capacitor Required**
- **Available in Extended Temperature Range: –40°C to 125°C**

APPLICATIONS

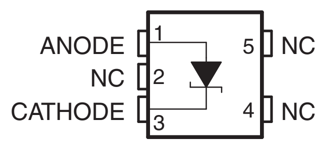
- **Data-Acquisition Systems**
- **Power Supplies and Power-Supply Monitors**
- **Instrumentation and Test Equipment**
- **Process Controls**
- **Precision Audio**
- **Automotive Electronics**
- **Energy Management**
- **Battery-Powered Equipment**

DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



*Pin 3 is attached to Substrate and must be connected to ANODE or left open.

DCK (SC-70) PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The TL4050-Q1 family of shunt voltage references are versatile easy-to-use references suitable for a wide array of applications. The two-terminal fixed-output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures.

The TL4050-Q1 is available in three initial tolerances, ranging from 0.1% (maximum) for the A grade to 0.5% (maximum) for the C grade. Thus, a great deal of flexibility is available to designers in choosing the best cost-to-performance ratio for their applications. Packaged in the space-saving SOT-23-3 and SC-70 packages and requiring a minimum current of 45 μA (typical), the TL4050-Q1 also is ideal for portable applications.

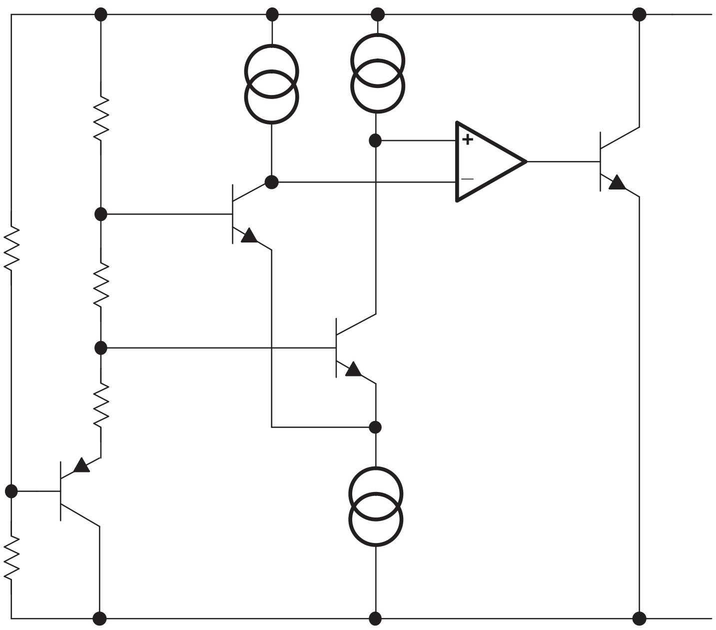
The TL4050x-Q1 characterization is for operation over an ambient temperature range of –40°C to 125°C.

PACKAGE AND ORDERING INFORMATION

For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_Z	Continuous cathode current	–10	20	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		TL4050-Q1		UNIT
		DBZ	DCK	
		3 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	331.1	289.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	107.5	56.4	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	63.4	93	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	4.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	61.7	91.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
I_Z	Cathode current		[1]	15	mA
T_A	Free-air temperature	I temperature	–40	85	°C
		Q temperature	–40	125	

(1) See parametric tables

TL4050x20-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050A20-Q1			TL4050B20-Q1			TL4050C20-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100 µA	25°C		2.048			2.048			2.048		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100 µA	25°C	–2.048		2.048	–4.096		4.096	–10.24		10.24	mV
			Full range	–12.288		12.288	–14.7456		14.7456	–17.2032		17.2032	
$I_{Z,min}$	Minimum cathode current		25°C		41	60		41	60		41	60	µA
			Full range			65			65			65	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10 mA	25°C		±20			±20			±20		ppm/°C
		I_Z = 1 mA	25°C		±15			±15			±15		
		I_Z = 100 µA	25°C		±15			±15			±15		
			Full range			±50			±50			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min}$ < I_Z < 1 mA	25°C		0.3	0.8		0.3	0.8		0.3	0.8	mV
			Full range			1.2			1.2			1.2	
		1 mA < I_Z < 15 mA	25°C		2.3	6		2.3	6		2.3	6	
			Full range			8			8			8	
Z_Z	Reverse dynamic impedance	I_Z = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_Z	25°C		0.3			0.3			0.3		Ω
e_N	Wideband noise	I_Z = 100 µA, 10 Hz ≤ f ≤ 10 kHz	25°C		34			34			34		µV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000 h, T_A = 25°C ± 0.1°C, I_Z = 100 µA			120			120			120		ppm
V_{HYST}	Thermal hysteresis (1)	ΔT_A = –40°C to 125°C			0.7			0.7			0.7		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

TL4050x25-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050B25-Q1 MIN	TYP	MAX	UNIT
V_Z	Reverse breakdown voltage	I_Z = 100 μA	25°C		2.5		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100 μA	25°C	–5		5	mV
			Full range	–18		18	
$I_{Z,min}$	Minimum cathode current		25°C		41	60	μA
			Full range			65	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10 mA	25°C		±20		ppm/°C
		I_Z = 1 mA	25°C		±15		
		I_Z = 100 μA	25°C		±15		
			Full range			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z <$ 1 mA	25°C		0.3	0.8	mV
			Full range			1.2	
		1 mA $< I_Z <$ 15 mA	25°C		2.3	6	
			Full range			8	
Z_Z	Reverse dynamic impedance	I_Z = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_Z	25°C		0.3		Ω
e_N	Wideband noise	I_Z = 100 μA, 10 Hz ≤ f ≤ 10 kHz	25°C		41		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000 h, T_A = 25°C ± 0.1°C, I_Z = 100 μA			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			0.7		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

TL4050x41-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050B41-Q1 MIN	TYP	MAX	UNIT
V_Z	Reverse breakdown voltage	I_Z = 100 µA	25°C		4.096		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100 µA	25°C	–8.2		8.2	mV
			Full range	–29		29	
$I_{Z,min}$	Minimum cathode current		25°C		52	68	µA
			Full range			78	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10 mA	25°C		±30		ppm/°C
		I_Z = 1 mA	25°C		±20		
		I_Z = 100 µA	25°C		±20		
			Full range			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z <$ 1 mA	25°C		0.2	0.9	mV
			Full range			1.2	
		1 mA < I_Z < 15 mA	25°C		2	7	
			Full range			10	
Z_Z	Reverse dynamic impedance	I_Z = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_Z$	25°C		0.5		Ω
e_N	Wideband noise	I_Z = 100 µA, 10 Hz ≤ f ≤ 10 kHz	25°C		93		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000 h, T_A = 25°C ± 0.1°C, I_Z = 100 µA			120		ppm
V_{HYST}	Thermal hysteresis (1)	ΔT_A = –40°C to 125°C			1.148		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

TL4050x50-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050A50-Q1			TL4050B50-Q1			TL4050C50-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100 µA	25°C		5			5			5		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100 µA	25°C	–5		5	–10		10	–25		25	mV
			Full range	–30		30	–35		35	–50		50	
$I_{Z,min}$	Minimum cathode current		25°C		56	74		56	74		56	74	µA
			Full range			90			90			90	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10 mA	25°C		±30			±30			±30		ppm/°C
		I_Z = 1 mA	25°C		±20			±20			±20		
		I_Z = 100 µA	25°C		±20			±20			±20		
			Full range			±50			±50			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z < 1$ mA	25°C		0.2	1		0.2	1		0.2	1	mV
			Full range			1.4			1.4			1.4	
		1 mA $< I_Z <$ 15 mA	25°C		2	8		2	8		2	8	
			Full range			12			12			12	
Z_Z	Reverse dynamic impedance	I_Z = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_Z$	25°C		0.5			0.5			0.5		Ω
e_N	Wideband noise	I_Z = 100 µA, 10 Hz ≤ f ≤ 10 kHz	25°C		93			93			93		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000 h, T_A = 25°C ± 0.1°C, I_Z = 100 µA			120			120			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			1.4			1.4			1.4		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

TYPICAL CHARACTERISTICS

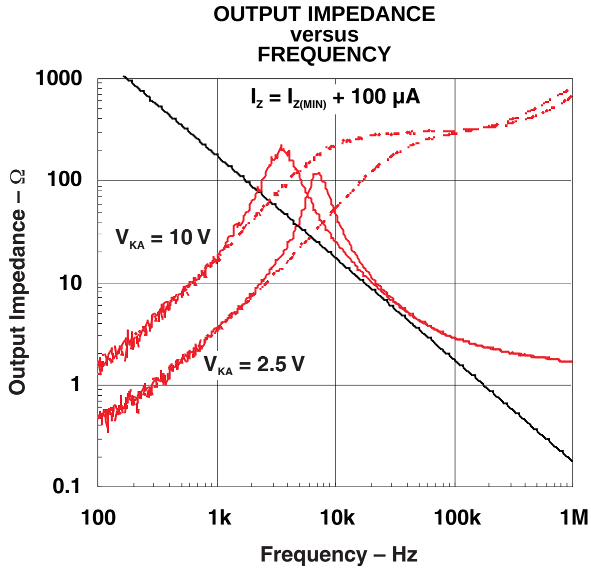


Figure 1.

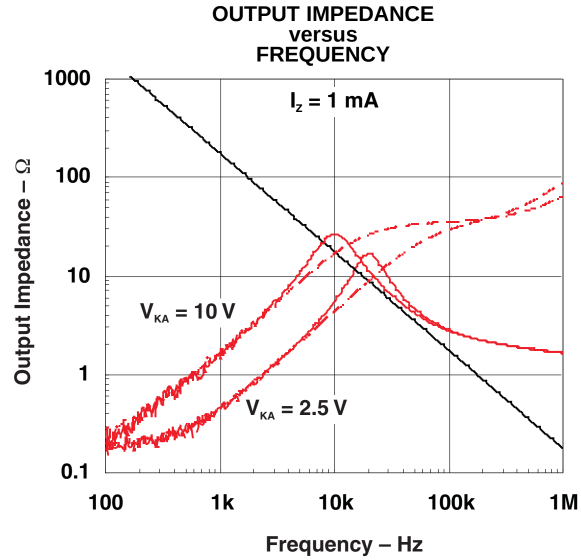


Figure 2.

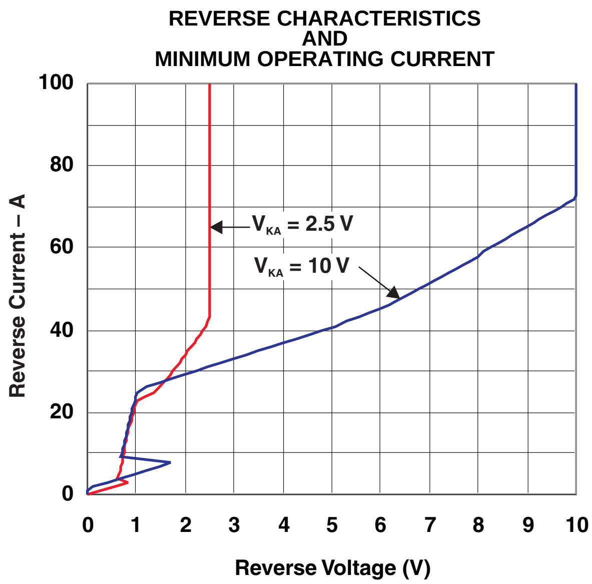


Figure 3.

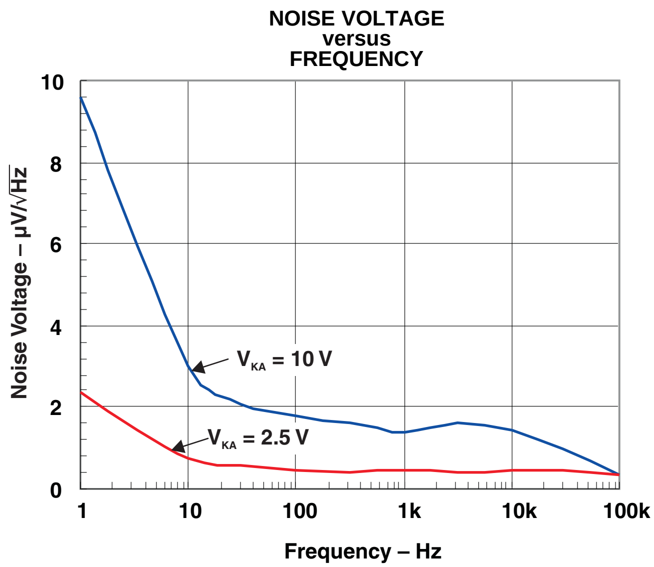


Figure 4.

TYPICAL CHARACTERISTICS (continued)

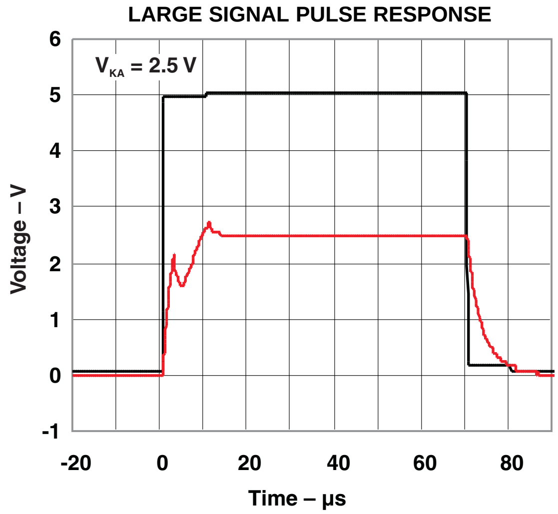


Figure 5.

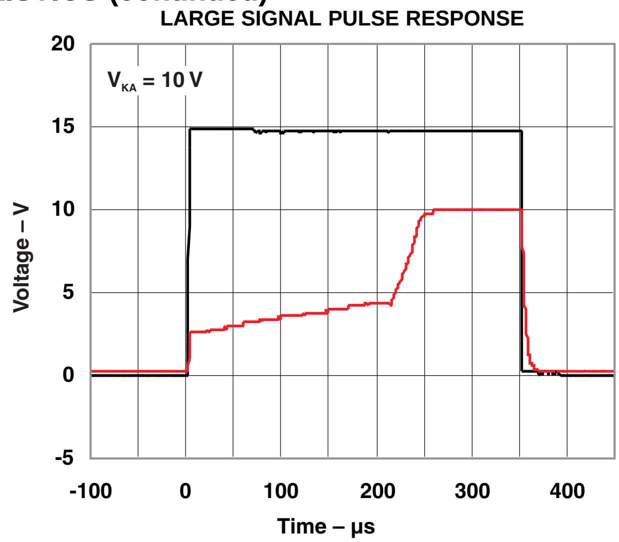


Figure 6.

APPLICATION INFORMATION

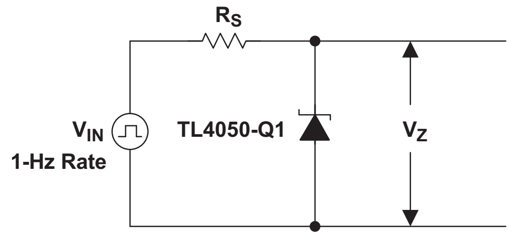


Figure 7. Start-Up Test Circuit

Output Capacitor

The TL4050-Q1 does not require an output capacitor across cathode and anode for stability. However, in an application using an output bypass capacitor, the TL4050-Q1 is stable with all capacitive loads.

SOT-23-3 Pin Connections

There is a parasitic Schottky diode connected between pins 2 and 3 of the SOT-23-3 packaged device. Thus, pin 3 of the SOT-23-3 package must be left floating or connected to pin 2.

Use With ADCs or DACs

The design of the TL4050x41-Q1 is as a cost-effective voltage reference, as required in 12-bit data-acquisition systems. For 12-bit systems operating from 5-V supplies, such as the ADS7842 (see Figure 8), the TL4050x41-Q1 (4.096 V) permits operation with an LSB of 1 mV.

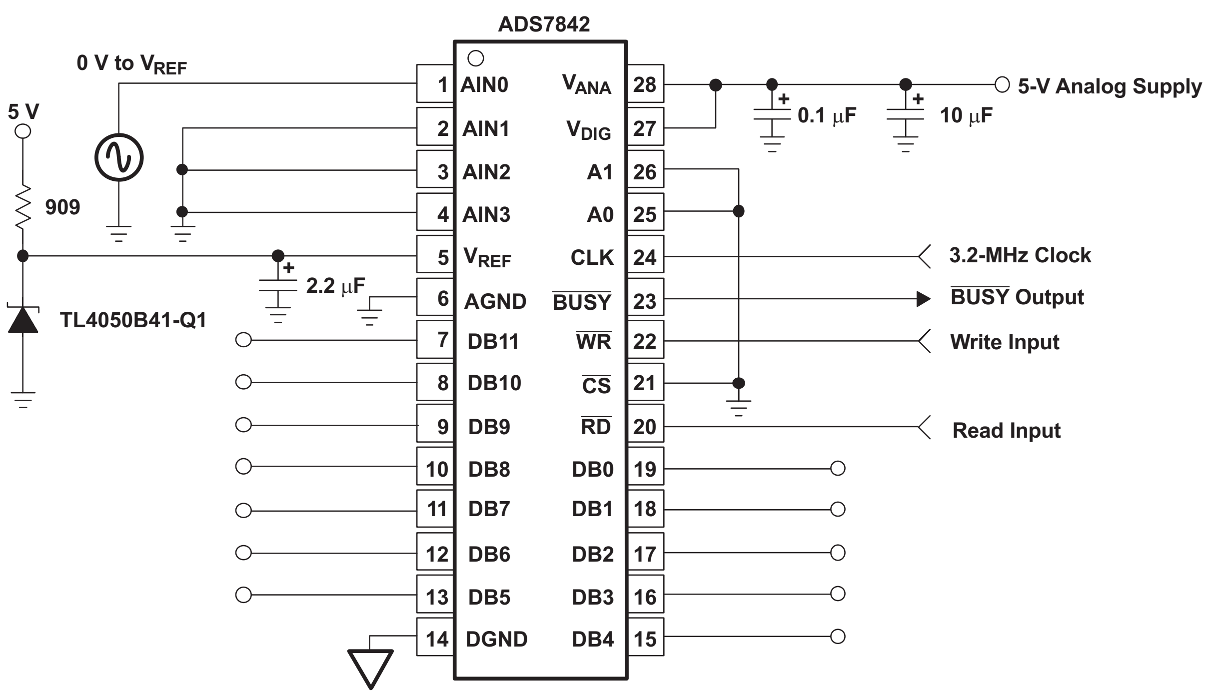


Figure 8. Data-Acquisition Circuit With TL4050x41-Q1

Cathode and Load Currents

In a typical shunt-regulator configuration (see Figure 9), an external resistor, R_S, connects between the supply and the cathode of the TL4050-Q1. Proper choice of R_S is essential, as R_S sets the total current available to supply the load (I_L) and bias the TL4050-Q1 (I_Z). In all cases, I_Z must stay within a specified range for proper operation of the reference. Taking into consideration one extreme in the variation of the load and supply voltage (maximum I_L and minimum V_S), R_S must be small enough to supply the minimum I_Z required for operation of the regulator, as given by data-sheet parameters. At the other extreme, maximum V_S and minimum I_L, R_S must be large enough to limit I_Z to less than its maximum-rated value of 15 mA.

Equation 1 calculates R_S:

$$R_S = \frac{(V_S - V_Z)}{(I_L + I_Z)} \tag{1}$$

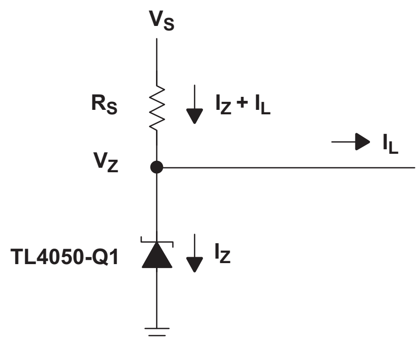


Figure 9. Shunt Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL4050A50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLGU	Samples
TL4050A50QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7GU	Samples
TL4050B25QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLHU	Samples
TL4050B25QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7HU	Samples
TL4050B41QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMXU	Samples
TL4050B50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLJU	Samples
TL4050B50QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7JU	Samples
TL4050C20QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMYU	Samples
TL4050C50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TKZU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TL4050A50-Q1, TL4050B25-Q1, TL4050B41-Q1, TL4050B50-Q1, TL4050C50-Q1 :

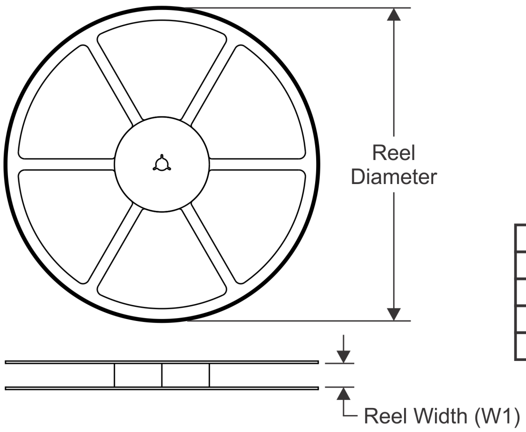
- Catalog: TL4050A50, TL4050B25, TL4050B41, TL4050B50, TL4050C50

NOTE: Qualified Version Definitions:

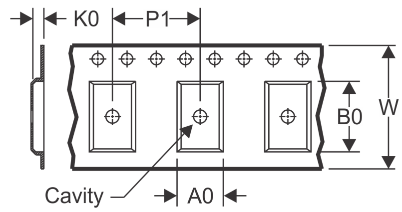
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

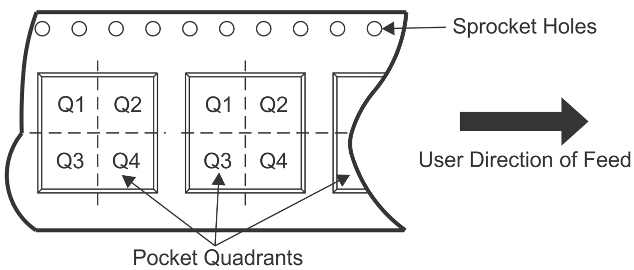


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

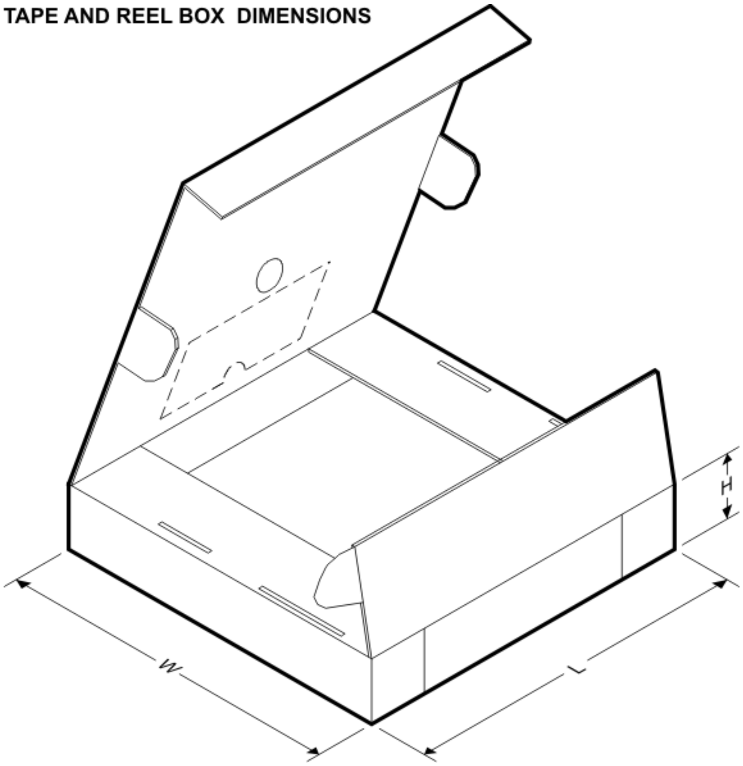
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050A50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B25QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

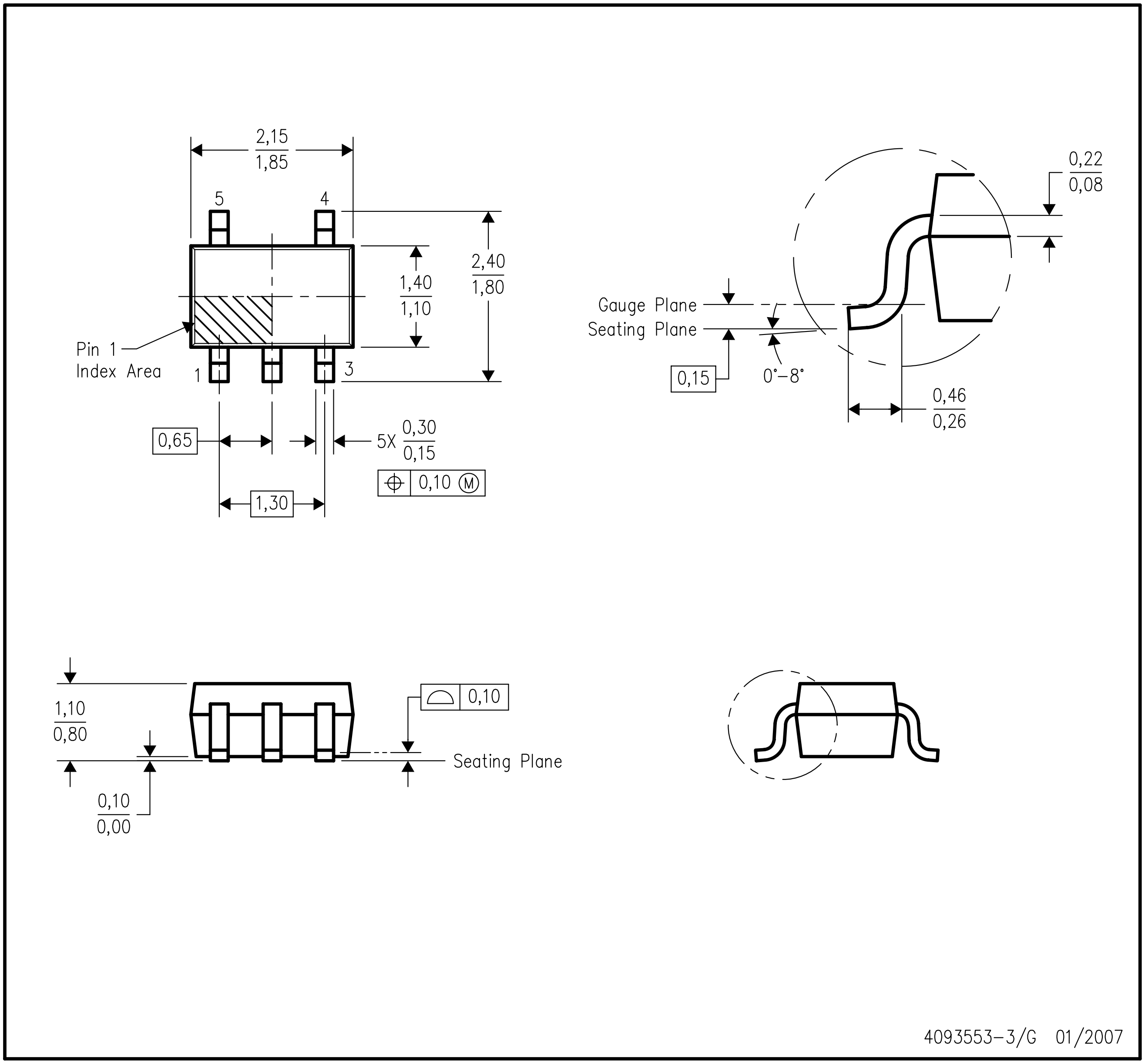
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

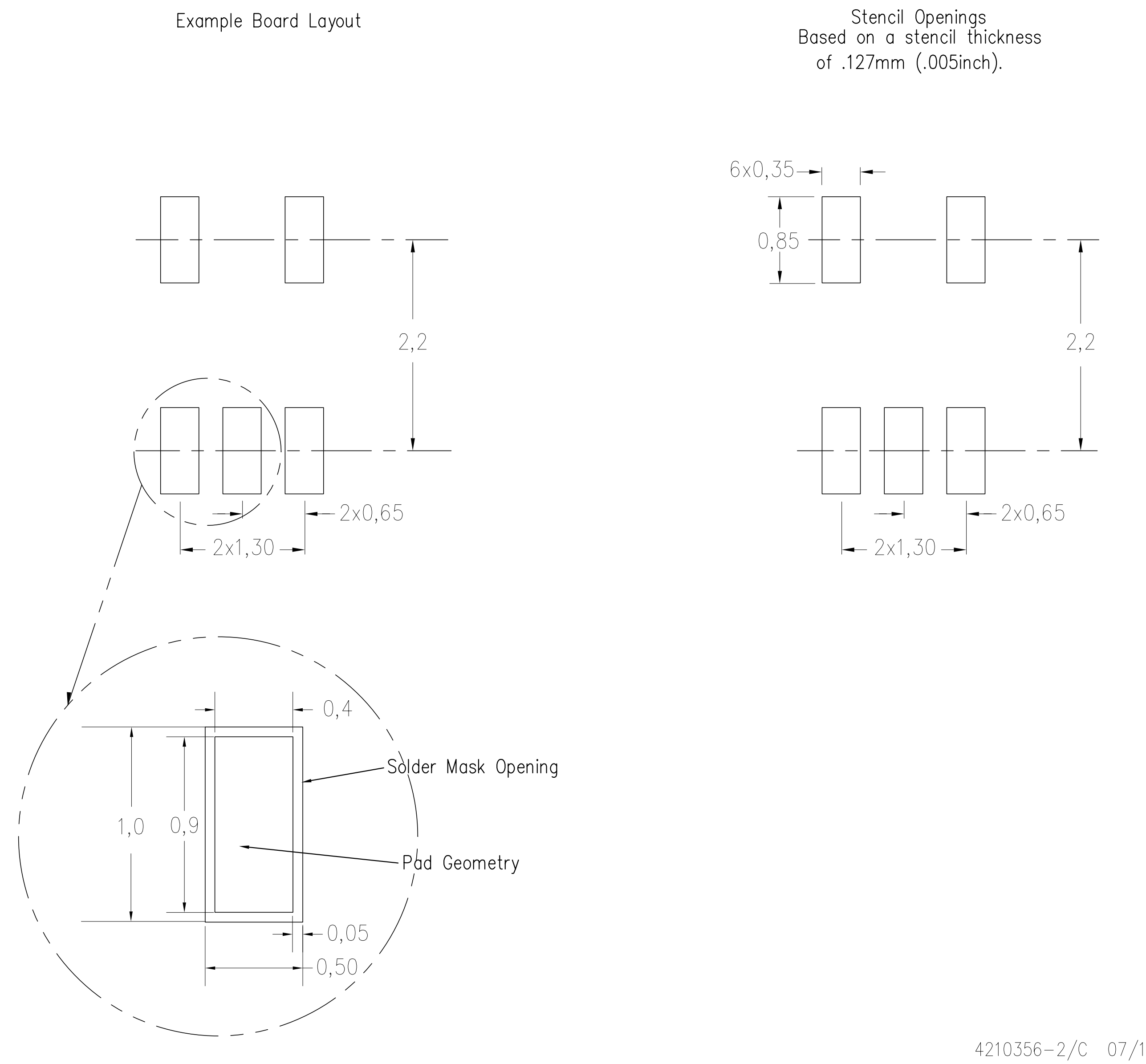
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL4050A50QDCKRQ1	SC70	DCK	5	3000	203.0	203.0	35.0
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL4050B25QDCKRQ1	SC70	DCK	5	3000	203.0	203.0	35.0
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL4050B50QDCKRQ1	SC70	DCK	5	3000	203.0	203.0	35.0
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

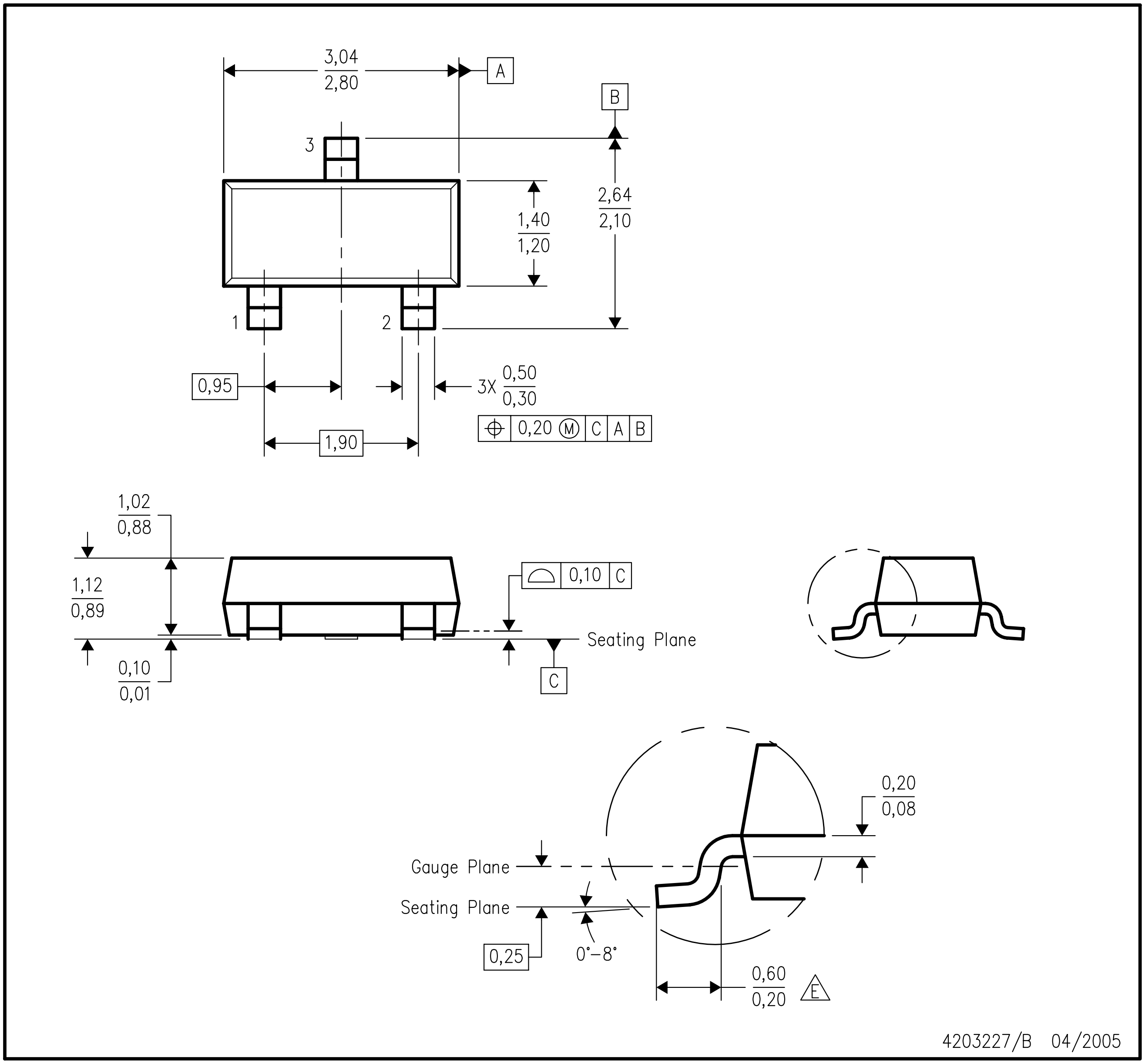
DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



4210356–2/C 07/11

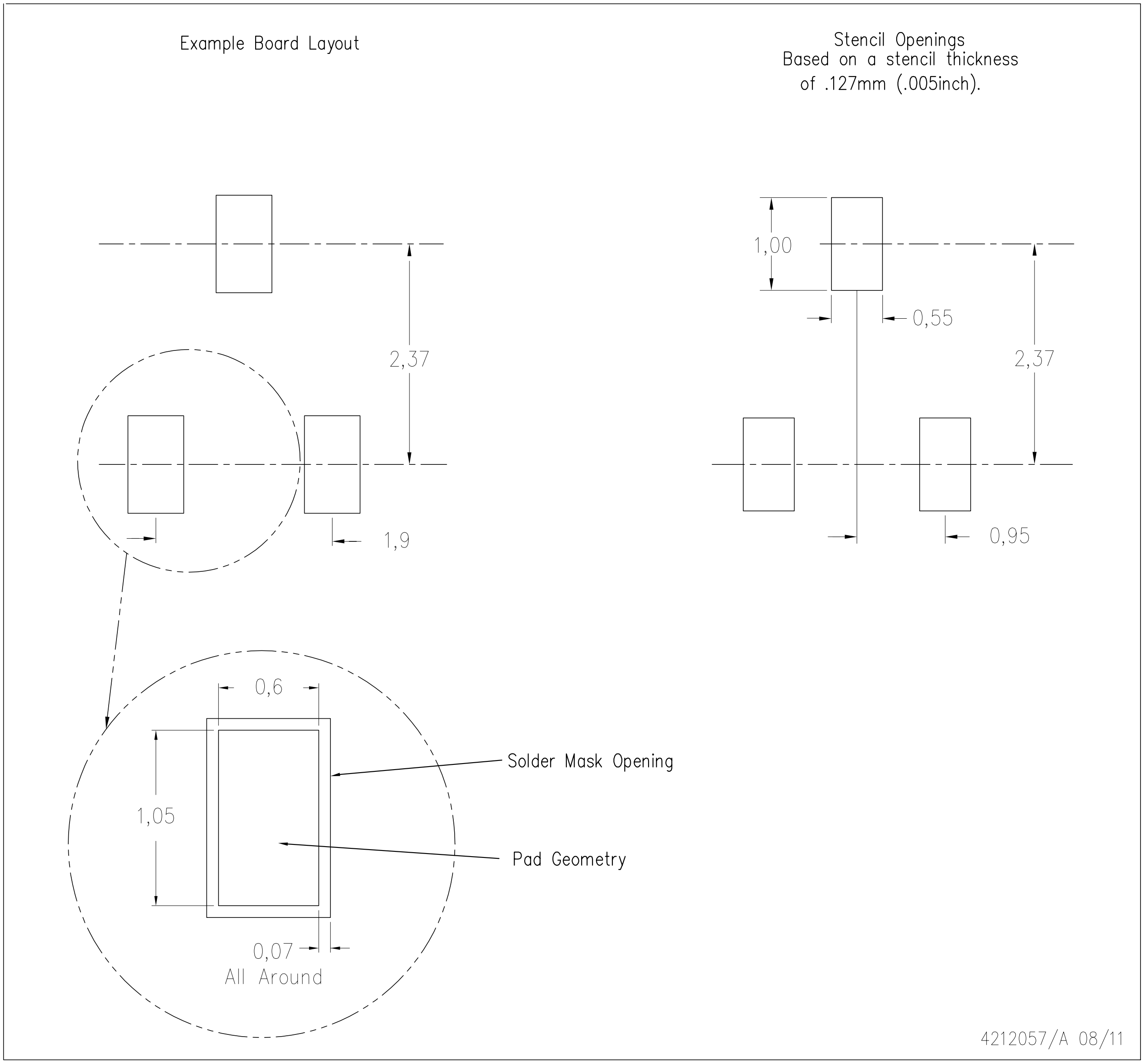
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBZ (R-PDSO-G3) PLASTIC SMALL-OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Lead dimensions are inclusive of plating.
- D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
- E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DBZ (R–PDSO–G3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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