TJA1080ATS/2

FlexRay transceiver

Rev. 04 — 19 February 2009 Product data sheet

1. General description

The TJA1080ATS/2 is a FlexRay transceiver that is fully compliant with the FlexRay electrical physical layer specification V2.1 Rev. A (see Ref. 1) and partly complies with version V2.1 Rev. B. It is primarily intended for communication systems from 1 Mbit/s to 10 Mbit/s, and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network.

The TJA1080ATS/2 can be configured to be used as an active star transceiver or as a node transceiver.

The TJA1080ATS/2 provides differential transmit capability to the network and differential receive capability to the FlexRay controller. It offers excellent EMC performance as well as high ESD protection.

The TJA1080ATS/2 actively monitors the system performance using dedicated error and status information (readable by any microcontroller), as well as internal voltage and temperature monitoring.

The TJA1080ATS/2 supports the mode control as used in NXP Semiconductors TJA1054 (see Ref. 2) and TJA1041 (see Ref. 3) CAN transceivers.

The TJA1080ATS/2 is the next step up from the TJA1080 FlexRay transceiver (Ref. 4). Being fully pin compatible and offering the same excellent ESD protection, the TJA1080ATS/2 also features:

- Improved power-on reset concept
- Improved ElectroMagnetic Emission (EME)
- Support of 60 ns minimum bit time
- Improved bus error detection functionality

This makes the TJA1080ATS/2 an excellent choice in any kind of FlexRay node.

See Section 14 for a detailed overview of differences between the TJA1080 and the TJA1080ATS/2.

2. Features

2.1 Optimized for time triggered communication systems

- Compliant with FlexRay electrical physical layer specification V2.1 Rev. A (see Ref. 1)
- Automotive product qualification in accordance with AEC-Q100
- Data transfer up to 10 Mbit/s
- Support of 60 ns minimum bit time

- Very low EME to support unshielded cable
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Usable for 14 V and 42 V powered systems
- Bus guardian interface included
- Independent power supply ramp-up for V_{BAT}, V_{CC} and V_{IO}
- Transceiver can be used for linear passive bus topologies as well as active star topologies

2.2 Low power management

- Low power management including two inhibit switches
- Very low current in Sleep and Standby modes
- Local and remote wake-up
- Supports remote wake-up via dedicated data frames
- Wake-up source recognition
- Automatic power-down (in Star-sleep mode) in star configuration

2.3 Diagnosis (detection and signalling)

- Overtemperature detection
- Short-circuit on bus lines
- V_{BAT} power-on flag (first battery connection and cold start)
- Pin TXEN and pin BGE clamping
- Undervoltage detection on pins V_{BAT}, V_{CC} and V_{IO}
- Wake source indication

2.4 Protections

- Bus pins protected against 8 kV HBM ESD pulses
- Bus pins protected against transients in automotive environment (ISO 7637 class C compliant)
- Bus pins short-circuit proof to battery voltage (14 V and 42 V) and ground
- Fail-safe mode in case of an undervoltage on pins V_{BAT}, V_{CC} or V_{IO}
- Passive behavior of bus lines in the event that transceiver is not powered

2.5 Functional classes according to FlexRay electrical physical layer specification (see Ref. 1)

- Bus driver voltage regulator control
- Bus driver - bus guardian control interface
- Bus driver logic level adaptation
- Active star - communication controller interface
- Active star - bus guardian interface
- Active star voltage regulator control

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1080ATS/2	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1

4. Block diagram

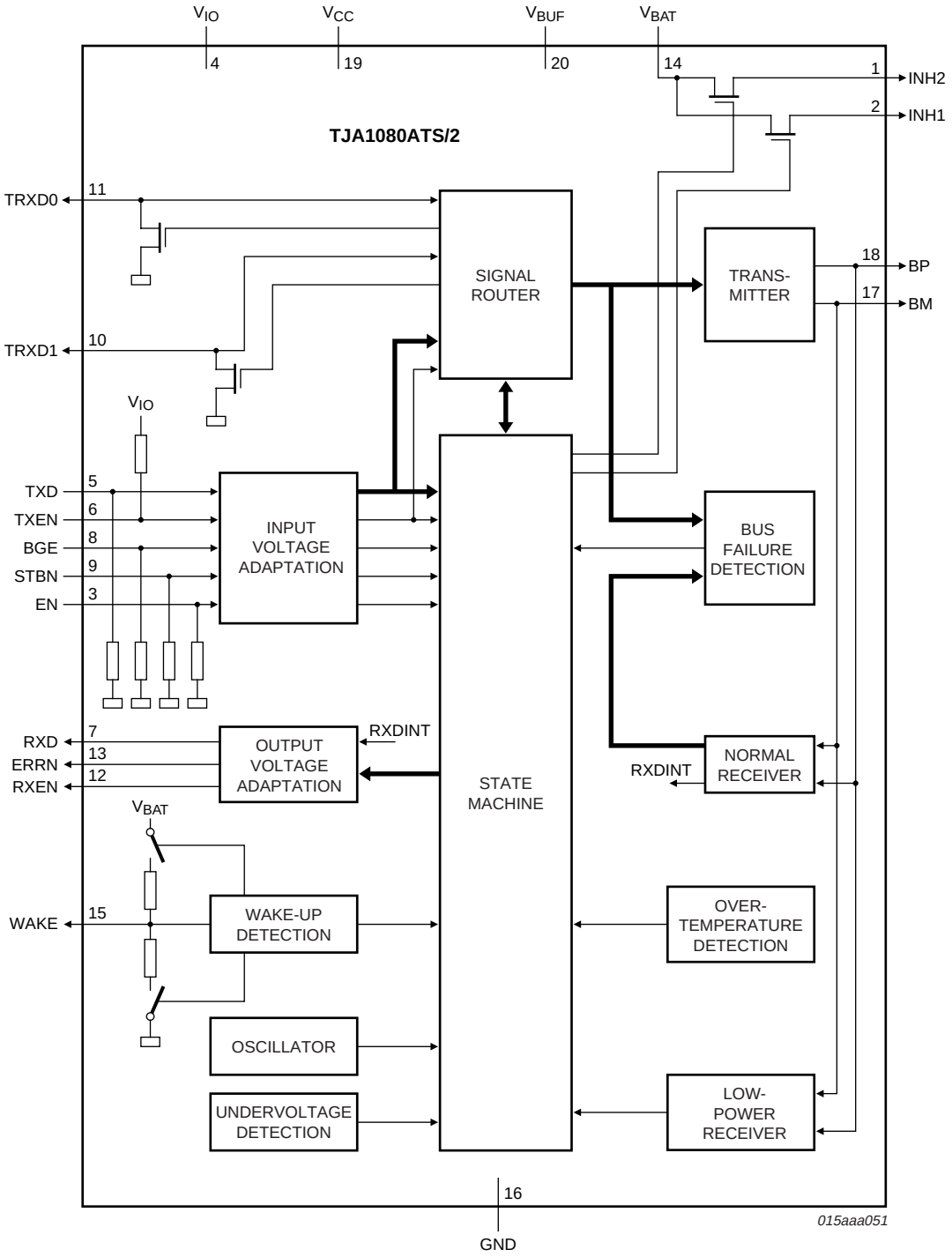


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

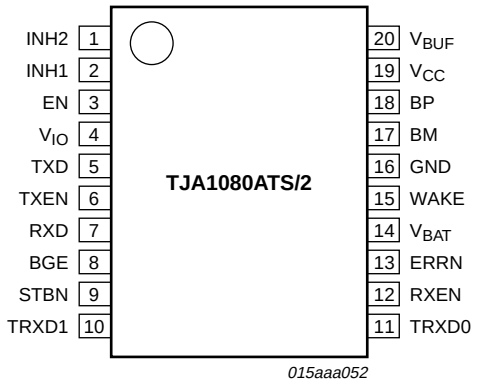


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
INH2	1	O	inhibit 2 output for switching external voltage regulator
INH1	2	O	inhibit 1 output for switching external voltage regulator
EN	3	I	enable input; when HIGH enabled; internal pull-down
V_{IO}	4	P	supply voltage for V_{IO} voltage level adaptation
TXD	5	I	transmit data input; internal pull-down
TXEN	6	I	transmitter enable input; when HIGH transmitter disabled; internal pull-up
RXD	7	O	receive data output
BGE	8	I	bus guardian enable input; when LOW transmitter disabled; internal pull-down
STBN	9	I	standby input; low-power mode when LOW; internal pull-down
TRXD1	10	I/O	data bus line 1 for inner star connection
TRXD0	11	I/O	data bus line 0 for inner star connection
RXEN	12	O	receive data enable output; when LOW bus activity detected
ERRN	13	O	error diagnoses output; when LOW error detected
V_{BAT}	14	P	battery supply voltage
WAKE	15	I	local wake-up input; internal pull-up or pull-down (depends on voltage at pin WAKE)
GND	16	P	ground
BM	17	I/O	bus line minus
BP	18	I/O	bus line plus
V_{CC}	19	P	supply voltage (+5 V)
V_{BUF}	20	P	buffer supply voltage

6. Functional description

The block diagram of the total transceiver is illustrated in Figure 1.

6.1 Operating configurations

6.1.1 Node configuration

In node configuration the transceiver operates as a stand-alone transceiver.

The transceiver can be configured as node by connecting pins TRXD0 and TRXD1 to ground during a power-on situation (PWON flag is set). The configuration will be latched when the PWON flag is reset, see Section 6.7.4.

The following operating modes are available:

- Normal (normal power mode)
- Receive-only (normal power mode)
- Standby (low power mode)
- Go-to-sleep (low power mode)
- Sleep (low power mode)

6.1.2 Star configuration

In star configuration the transceiver operates as a branch of a FlexRay active star.

The transceiver can be configured as star by connecting pin TRXD0 or TRXD1 to V_{BUF} during a PWON situation (PWON flag is set). The configuration will be latched when the PWON flag is reset, see Section 6.7.4 “Power-on flag”.

It is possible to redirect data from one branch to other branches via the inner bus. It is also possible to send data to all branches via pin TXD, if pins TXEN and BGE have the correct polarity.

The following operating modes are available:

- Star-idle (normal power mode)
- Star-transmit (normal power mode)
- Star-receive (normal power mode)
- Star-sleep (low power mode)
- Star-standby (low power mode)
- Star-locked (normal power mode)

In the star configuration all modes are autonomously controlled by the transceiver, except in the case of a wake-up.

6.1.3 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid for node and star configurations in normal power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, then activity is detected on the bus lines and pin RXEN is switched to LOW which results in pin RXD being released:
  - If, after bus activity detection, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
  - If, after bus activity detection, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, then idle is detected on the bus lines and pin RXEN is switched to HIGH. This results in pin RXD being blocked (pin RXD is switched to HIGH or stays HIGH)

Additionally, in star configuration, activity and idle can be detected (see Figure 6 for state transitions due to activity/idle detection in star configuration):

- If pin TXEN is LOW for longer than $t_{det(act)(TXEN)}$, activity is detected on pin TXEN
- If pin TXEN is HIGH for longer than $t_{det(idle)(TXEN)}$, idle is detected on pin TXEN
- If pin TRXD0 or TRXD1 is LOW for longer than $t_{det(act)(TRXD)}$, activity is detected on pins TRXD0 and TRXD1
- If pin TRXD0 and TRXD1 is HIGH for longer than $t_{det(idle)(TRXD)}$, idle is detected on pins TRXD0 and TRXD1

6.2 Operating modes in node configuration

The TJA1080ATS/2 provides two control pins STBN and EN in order to select one of the modes of operation in node configuration. See Table 3 for a detailed description of the pin signalling in node configuration, and Figure 3 for the timing diagram.

All modes are directly controlled via pins EN and STBN unless an undervoltage situation is present.

If V_{IO} and (V_{BUF} or V_{BAT}) are within their operating range, pin ERRN indicates the status of the error flag.

Table 3. Pin signalling in node configuration

Mode	STBN	EN	ERRN[1]		RXEN		RXD		Transmitter	INH1	INH2
			LOW	HIGH	LOW	HIGH	LOW	HIGH			
Normal	HIGH	HIGH	error flag set	error flag reset	bus activity	bus idle	bus DATA_0	bus DATA_1 or idle	enabled	HIGH	HIGH
Receive-only	HIGH	LOW							disabled		
Go-to-sleep	LOW	HIGH	error flag set[2]	error flag reset	wake flag set[2]	wake flag reset	wake flag set[2]	wake flag reset			float[3]
Standby	LOW	LOW									
Sleep	LOW	X								float	float

[1] Pin ERRN provides a serial interface for retrieving diagnostic information.

[2] Valid if V_{IO} and (V_{BUF} or V_{BAT}) are present.

[3] If wake flag is not set.

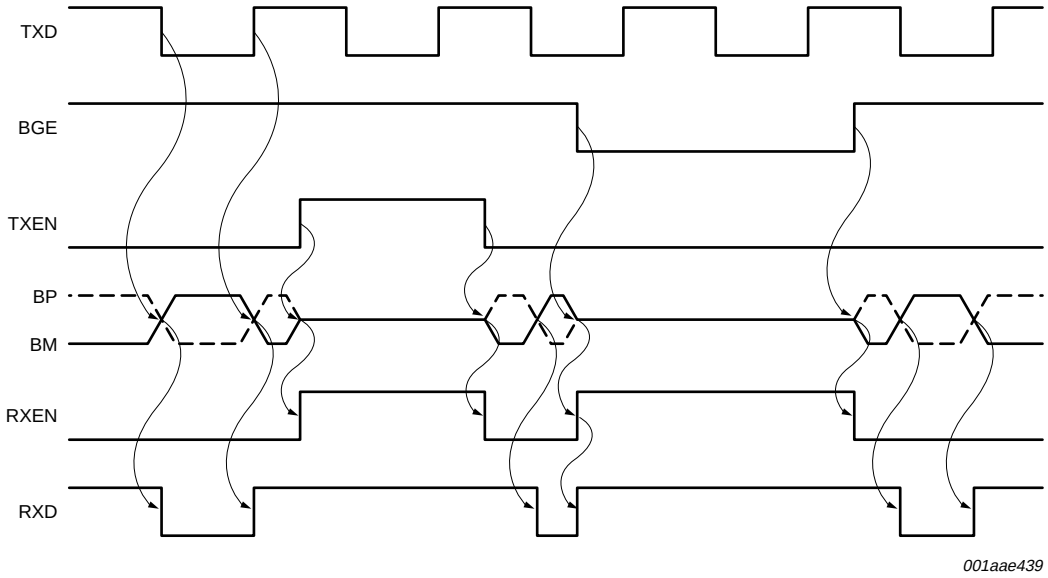


Fig 3. Timing diagram in Normal mode node configuration

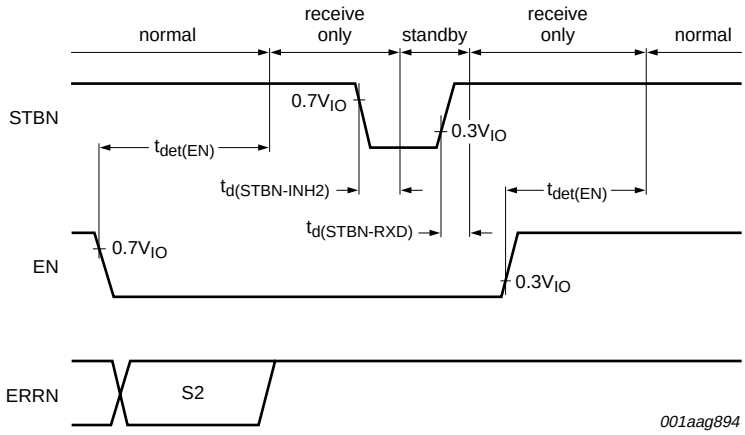
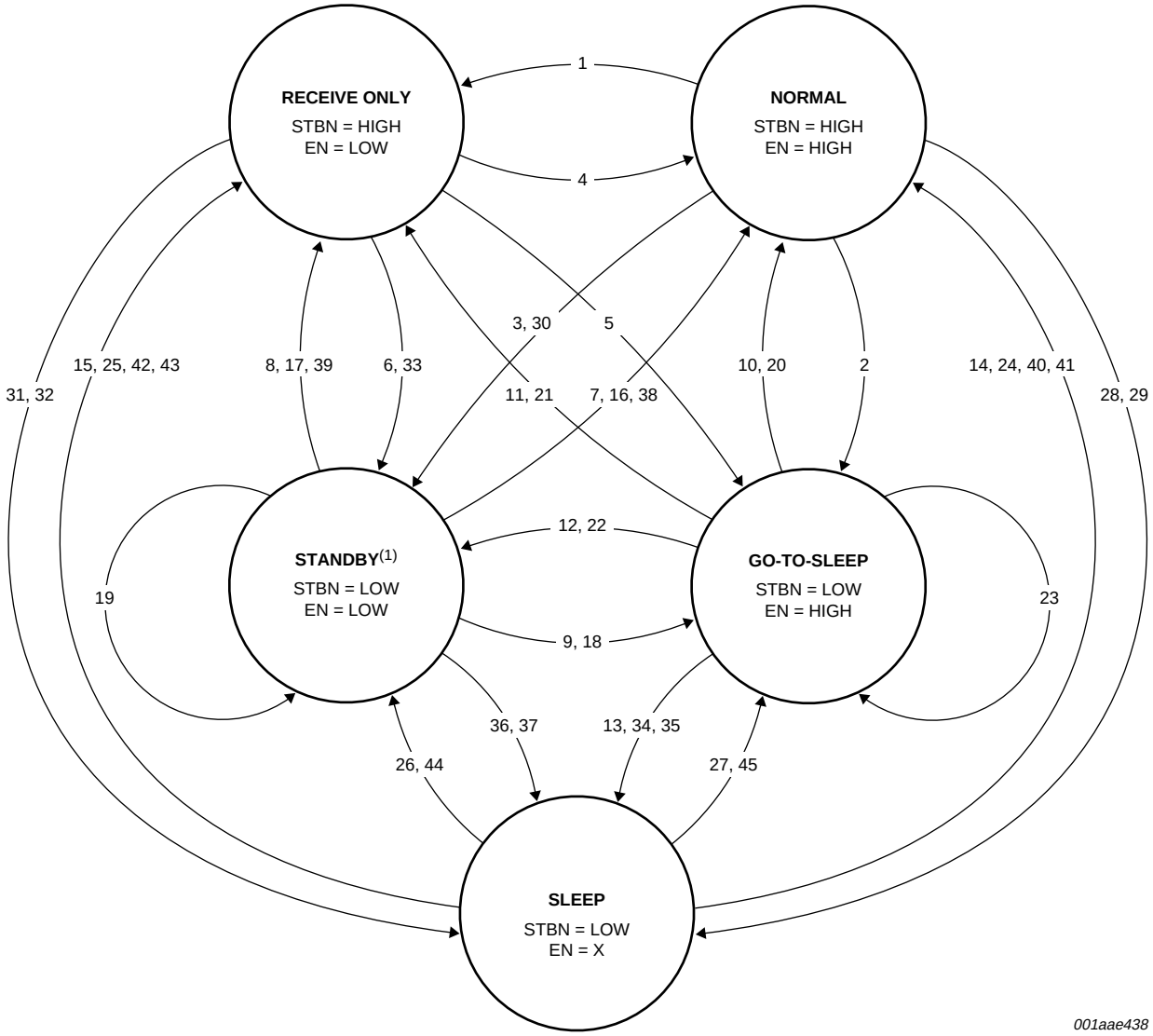


Fig 4. Timing diagram of control pins EN and STBN

The state diagram in node configuration is illustrated in Figure 5.



(1) At the first battery connection the transceiver will enter the Standby mode.

Fig 5. State diagram in node configuration

The state transitions are represented with numbers, which correspond with the numbers in column 3 of Table 4 to Table 7.

Table 4. State transitions forced by EN and STBN (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Normal	Receive-only	1	H	→ L	cleared	cleared	cleared	cleared	cleared	
	Go-to-sleep	2	→ L	H	cleared	cleared	cleared	cleared	cleared	
	Standby	3	→ L	→ L	cleared	cleared	cleared	cleared	cleared	[1]
Receive-only	Normal	4	H	→ H	cleared	cleared	cleared	X	X	
	Go-to-sleep	5	→ L	→ H	cleared	cleared	cleared	X	X	
	Standby	6	→ L	L	cleared	cleared	cleared	X	X	
Standby	Normal	7	→ H	→ H	cleared	cleared	2 → cleared	X	1 → cleared	[2][3]
	Receive-only	8	→ H	L	cleared	cleared	2 → cleared	X	1 → set	[2][3]
	Go-to-sleep	9	L	→ H	cleared	cleared	X	X	X	
Go-to-sleep	Normal	10	→ H	H	cleared	cleared	cleared	X	1 → cleared	[2][4]
	Receive-only	11	→ H	→ L	cleared	cleared	cleared	X	1 → set	[2][4]
	Standby	12	L	→ L	cleared	cleared	X	X	X	[4]
	Sleep	13	L	H	cleared	cleared	X	X	cleared	[5]
Sleep	Normal	14	→ H	H	2 → cleared	2 → cleared	2 → cleared	X	1 → cleared	[2][3]
	Receive-only	15	→ H	L	2 → cleared	2 → cleared	2 → cleared	X	1 → set	[2][3]

[1] STBN must be set to LOW at least $t_{det(EN)}$ after the falling edge on EN.

[2] Positive edge on pin STBN sets the wake flag. In the case of a transition to Normal mode the wake flag is immediately cleared.

[3] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flags.

[4] Hold time of go-to-sleep is less than $t_{h(gotosleep)}$.

[5] Hold time of go-to-sleep becomes greater than $t_{h(gotosleep)}$.

Table 5. State transitions forced by a wake-up (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Standby	Normal	16	H	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Receive-only	17	H	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	18	L	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Standby	19	L	L	cleared	cleared	1 → cleared	X	→ set	[1]
Go-to-sleep	Normal	20	H	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Receive-only	21	H	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Standby	22	L	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	23	L	H	cleared	cleared	1 → cleared	X	→ set	[1]
Sleep	Normal	24	H	H	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]
	Receive-only	25	H	L	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]
	Standby	26	L	L	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	27	L	H	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]

[1] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flag.

[2] Transition via Standby mode.

Table 6. State transitions forced by an undervoltage condition (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Flag					Note
			UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Normal	Sleep	28	→ set	cleared	cleared	cleared	cleared	[1]
	Sleep	29	cleared	→ set	cleared	cleared	cleared	[1]
	Standby	30	cleared	cleared	→ set	cleared	cleared	[1]
Receive-only	Sleep	31	→ set	cleared	cleared	X	1 → cleared	[1]
	Sleep	32	cleared	→ set	cleared	X	1 → cleared	[1]
	Standby	33	cleared	cleared	→ set	X	1 → cleared	[1]
Go-to-sleep	Sleep	34	→ set	cleared	cleared	X	1 → cleared	[1]
	Sleep	35	cleared	→ set	cleared	X	1 → cleared	[1]
Standby	Sleep	36	→ set	cleared	X	X	1 → cleared	[1][2]
	Sleep	37	cleared	→ set	X	X	1 → cleared	[1][3]

[1] UV_{VIO}, UV_{VBAT} or UV_{VCC} detected clears the wake flag.

[2] UV_{VIO} overrules UV_{VCC}.

[3] UV_{VBAT} overrules UV_{VCC}.

Table 7. State transitions forced by an undervoltage recovery (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Standby	Normal	38	H	H	cleared	cleared	→ cleared	X	X	[1]
	Receive-only	39	H	L	cleared	cleared	→ cleared	X	X	[1]
Sleep	Normal	40	H	H	cleared	→ cleared	cleared	X	1 → cleared	[2][3]
	Normal	41	H	H	→ cleared	cleared	cleared	X	X	[4]
	Receive-only	42	H	L	cleared	→ cleared	cleared	X	1 → set	[2][3]
	Receive-only	43	H	L	→ cleared	cleared	cleared	X	X	[4]
	Standby	44	L	L	cleared	→ cleared	cleared	X	1 → set	[2][3]
	Sleep	45	L	X	→ cleared	cleared	cleared	X	cleared	[4]
	Go-to-sleep	46	L	H	cleared	→ cleared	cleared	X	1 → set	[2][3]
	Sleep	47	L	X	→ cleared	cleared	cleared	X	cleared	[4]

[1] Recovery of UV_{VCC} flag.

[2] Recovery of UV_{VBAT} flag.

[3] Clearing the UV_{VBAT} flag sets the wake flag. In the case of a transition to Normal mode the wake flag is immediately cleared.

[4] Recovery of UV_{VIO} flag.

6.2.1 Normal mode

In Normal mode the transceiver is able to transmit and receive data via the bus lines BP and BM. The output of the normal receiver is directly connected to pin RXD.

The transmitter behavior in Normal mode of operation, with no time-out present on pins TXEN and BGE and the temperature flag not set, is given in Table 8.

In this mode pins INH1 and INH2 are set HIGH.

Table 8. Transmitter function table

BGE	TXEN	TXD	Transmitter
L	X	X	transmitter is disabled
X	H	X	transmitter is disabled
H	L	H	transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW
H	L	L	transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH

6.2.2 Receive-only mode

In Receive-only mode the transceiver can only receive data. The transmitter is disabled, regardless of the voltages on pins BGE and TXEN.

In this mode pins INH1 and INH2 are set HIGH.

6.2.3 Standby mode

In Standby mode the transceiver has entered a low power mode which means very low current consumption. In the Standby mode the device is not able to transmit or receive data and the low power receiver is activated to monitor for bus wake-up patterns.

Standby mode can be entered if the correct polarity is applied to pins EN and STBN (see Figure 5 and Table 4) or an undervoltage is present on pin V_{CC}; see Figure 5.

In this mode, pin INH1 is set HIGH.

If the wake flag is set, pin INH2 is set to HIGH and pins RXEN and RXD are set to LOW, otherwise pin INH2 is floating and pins RXEN and RXD are set to HIGH; see Section 6.5.

6.2.4 Go-to-sleep mode

In this mode the transceiver behaves as in Standby mode. If this mode is selected for a longer time than the go-to-sleep hold time parameter (minimum hold time) and the wake flag has been previously cleared, the transceiver will enter Sleep mode, regardless of the voltage on pin EN.

6.2.5 Sleep mode

In Sleep mode the transceiver has entered a low power mode. The only difference with Standby mode is that pin INH1 is also set floating. Sleep mode is also entered if the UV_{VIO} or UV_{VBAT} flag is set.

In case of an undervoltage on pin V_{CC} or V_{BAT} while V_{IO} is present, the wake flag is set by a positive edge on pin STBN.

The undervoltage flags will be reset by setting the wake flag, and therefore the transceiver will enter the mode indicated on pins EN and STBN if V_{IO} is present.

A detailed description of the wake-up mechanism is given in Section 6.5.

6.3 Operating modes in star configuration

In star configuration mode control via pins EN and STBN is not possible. The transceiver autonomously controls the operating modes except in the case of wake-up.

The timing diagram of a transceiver configured in star configuration is illustrated in Figure 7. The state diagram in star configuration is illustrated in Figure 6. A detailed description of the pin signalling in star configuration is given in Table 9.

If V_{IO} and (V_{BUF} or V_{BAT}) are within their operating range, pin ERRN will indicate the error flag.

Table 9. Pin signalling in star configuration

Mode	TRXD0 / TRXD1	ERRN[1]		RXEN		RXD		Transmitter	INH1	INH2
		LOW	HIGH	LOW	HIGH	LOW	HIGH			
Star-transmit	output[2] input[3]	error flag set	error flag reset	bus activity	bus idle	bus DATA_0	bus DATA_1 or idle	enabled	HIGH	HIGH
Star-receive	output							disabled		
Star-idle	input									
Star-locked	input									
Star-standby	input	error flag set[4]	error flag reset	wake flag set[4]	wake flag reset	wake flag set[4]	wake flag reset			
Star-sleep	input								float	float

[1] Pin ERRN provides a serial interface for retrieving diagnostic information.

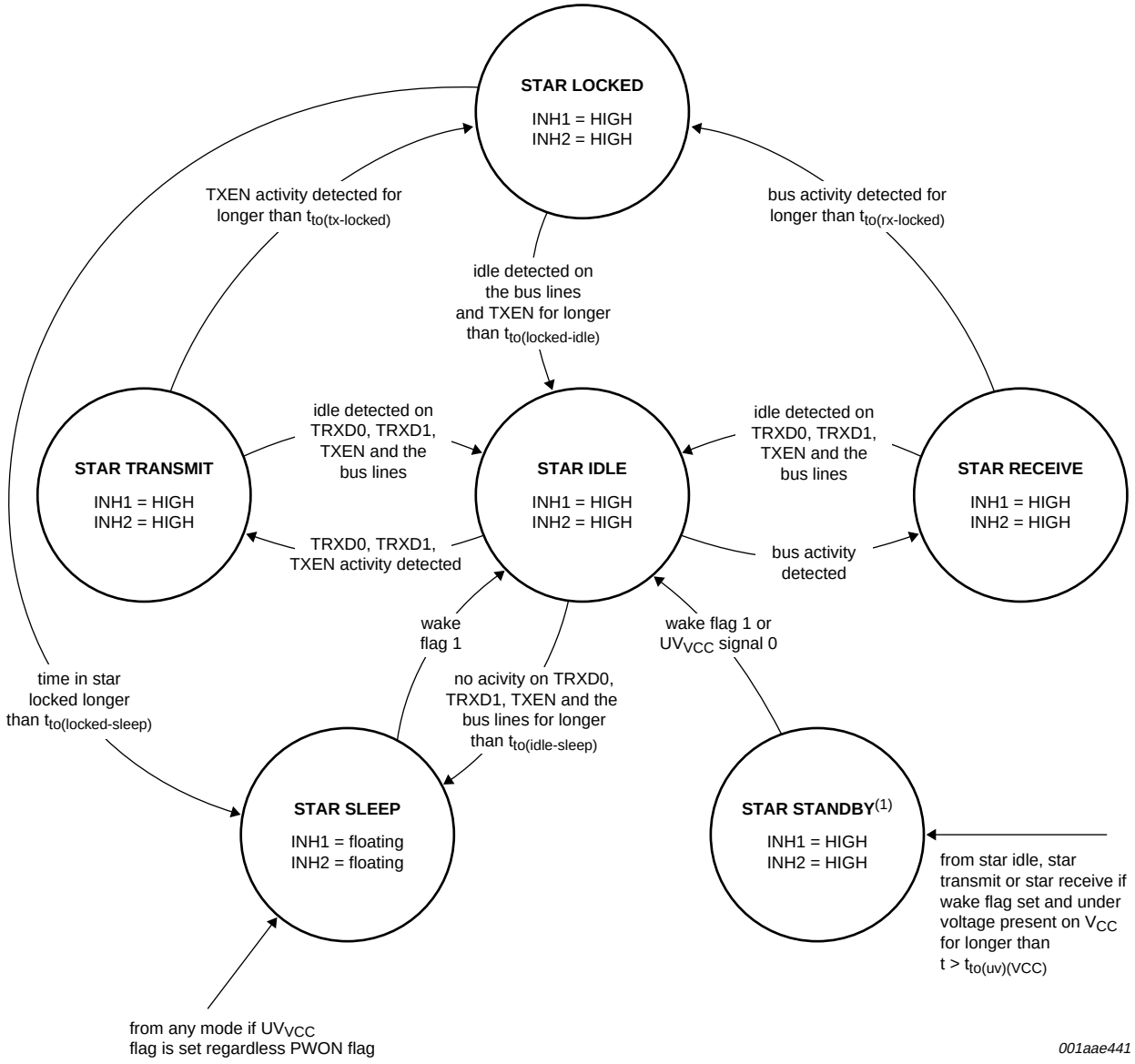
[2] TRXD lines switched as output if TXEN activity is the initiator for Star-transmit mode.

[3] TRXD lines are switched as input if TRXD activity is the initiator for Star-transmit mode.

[4] Valid if V_{IO} and (V_{BUF} or V_{BAT}) are present.

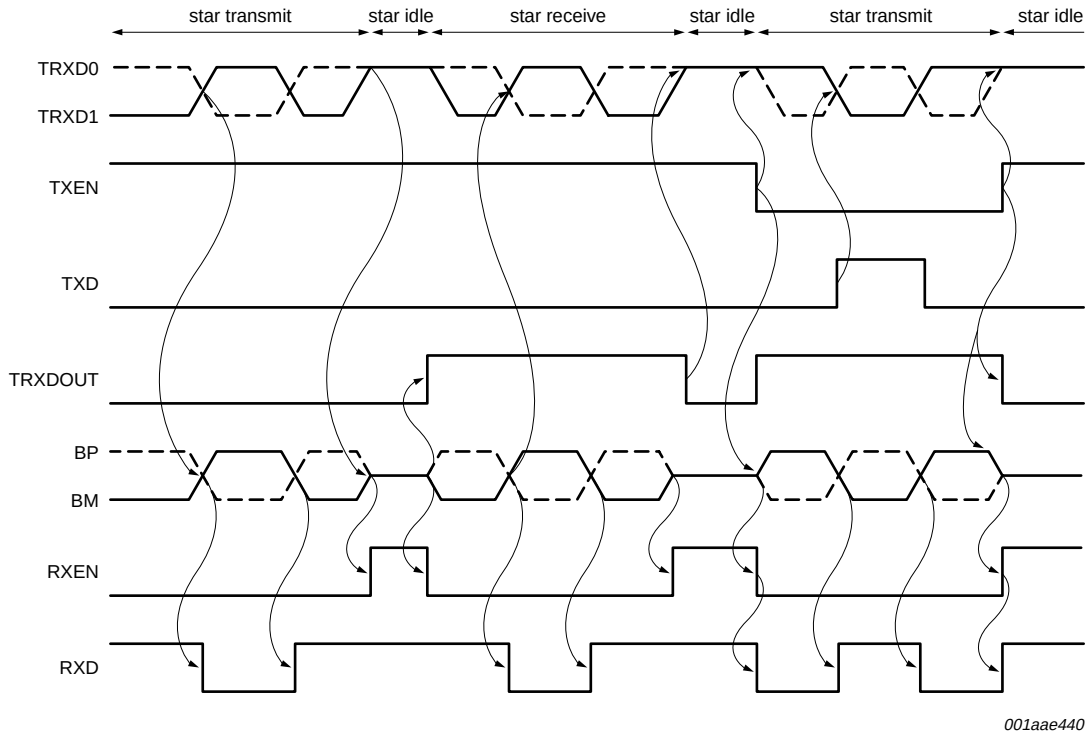
Pin BGE must be HIGH in order to enable the transmitter via pin TXEN. If pin BGE is LOW, it is not possible to activate the transmitter via pin TXEN. If pin TXEN is not used (no controller connected to the transceiver), it has to be connected to pin GND in order to prevent TXEN activity detection.

In all normal modes pin RXD is connected to the output of the normal mode receiver and therefore represents the data on the bus lines.



(1) At the first battery connection the transceiver will enter the Star-standby mode.

Fig 6. State diagram in star configuration



TRXDOUT is a virtual signal that indicates the state of the TRXD lines. TRXDOUT HIGH means TRXD lines switched as output. TRXDOUT LOW means TRXD lines switched as input.

Fig 7. Timing diagram in star configuration

6.3.1 Star-idle mode

This mode is entered if one of the following events occurs:

- From Star-receive mode and Star-transmit mode if idle is detected on the bus lines, on pin TXEN and on pins TRXD0 and TRXD1.
- If the transceiver is in Star-locked mode and idle is detected on the bus lines and pin TXEN for longer than $t_{to(locked\text{-}idle)}$.
- If the transceiver is in Star-standby mode and the wake flag is set or no undervoltage is present.
- If the transceiver is in Star-sleep mode and the wake flag is set, the transceiver enters Star-idle mode in order to obtain a stable starting point (no glitches on the bus lines etc.).

In Star-idle mode the transceiver monitors pins TXEN, TRXD0 and TRXD1 and the bus lines for activity. In this mode the transmitter is disabled.

6.3.2 Star-transmit mode

This mode is entered if one of the following events occur:

- If the transceiver is in Star-idle mode and activity is detected on pin TXEN.
- If the transceiver is in Star-idle mode and activity is detected on pins TRXD0 and TRXD1.

In Star-transmit mode the transmitter is enabled and the transceiver can transmit data on the bus lines and on the TRXD lines. It transmits the data received on pins TXD or TRXD0 and TRXD1, depending on where activity is detected:

- If activity is detected on the TRXD lines, the transceiver transmits data from pins TRXD0 and TRXD1 to the bus.
- If activity is detected on the TXEN, the transceiver transmits data from pin TXD to the bus and to the TRXD lines.

6.3.3 Star-receive mode

This mode is entered if the transceiver is in Star-idle mode and activity has been detected on the bus lines.

In Star-receive mode the transceiver transmits data received on the bus via the TRXD0 and TRXD1 lines to other transceivers connected to the TRXD lines. The transmitter is always disabled. RXD, which represents the data on the bus lines, is output at TRXD0 and TRXD1.

6.3.4 Star-standby mode

This mode is entered if one of the following events occur:

- From Star-idle, Star-transmit or Star-receive modes if the wake flag is set and an undervoltage on pin V_{CC} is present for longer than $t_{to(uv)(VCC)}$.
- If the PWON flag is set.

In Star-standby mode the transceiver has entered a low power mode. In this mode the current consumption is as low as possible to prevent discharging the capacitor at pin V_{BUF}.

If pins V_{IO} and V_{BUF} are within their operating range, pins RXD and RXEN will indicate the wake flag.

6.3.5 Star-sleep mode

This mode is entered if one of the following events occur:

- From any mode if an undervoltage on pin V_{CC} is present for longer than $t_{det(uv)(VCC)}$.
- If the transceiver is in Star-idle mode and no activity is detected on the bus lines and pins TXEN, TRXD0 and TRXD1 for longer than $t_{to(idle-sleep)}$.
- If Star-locked mode is active for longer than $t_{to(locked-sleep)}$.

In Star-sleep mode the transceiver has entered a low power mode. In this mode the current consumption is as low as possible to prevent the car battery from discharging. The inhibit switches are switched off.

In this mode the wake flag wakes the transceiver. A detailed description of the wake-up mechanism is given in Section 6.5.

If pins V_{IO} and V_{BUF} are within their operating range, pins RXD and RXEN will indicate the wake flag.

6.3.6 Star-locked mode

This mode is entered if one of the following events occur:

- If the transceiver is in Star-transmit mode and activity on pin TXEN is detected for longer than $t_{to(tx-locked)}$.
- If the transceiver is in Star-receive mode and activity is detected on the bus lines for longer than $t_{to(rx-locked)}$.

This mode is a fail-silent mode and in this mode the transmitter is disabled.

6.4 Start-up

The TJA1080ATS/2 initialization is independent of the way the voltage supplies V_{BAT}, V_{CC} and V_{IO} ramp up. A dedicated power-up sequence is not necessary.

6.4.1 Node configuration

Node configuration can be selected by applying a voltage lower than $0.3V_{BUF}$ to pins TRXD0 and TRXD1 during power-on. Node configuration is latched by resetting the PWON flag while the voltage on pins TRXD0 and TRXD1 is lower than $0.3V_{BUF}$; see Section 6.7.4 for (re)setting the PWON flag.

6.4.2 Star configuration

Star configuration can be selected by applying a voltage higher than $0.7V_{BUF}$ to pins TRXD0 or TRXD1 during power-on. Star configuration is latched by resetting the PWON flag while one of the voltages on pins TRXD0 or TRXD1 is higher than $0.7V_{BUF}$. See Section 6.7.4 for (re)setting the PWON flag. In this case the transceiver goes from Star-standby mode to Star-idle mode.

6.5 Wake-up mechanism

6.5.1 Node configuration

In Sleep mode (pins INH1 and INH2 are switched off), the transceiver will enter Standby mode or Go-to-sleep mode (depending on the value at pin EN), if the wake flag is set. Consequently, pins INH1 and INH2 are switched on.

If no undervoltage is present on pins V_{IO} and V_{BAT}, the transceiver switches immediately to the mode indicated on pins EN and STBN.

In Standby, Go-to-sleep and Sleep modes pins RXD and RXEN are driven LOW if the wake flag is set.

6.5.2 Star configuration

In Star-sleep mode (pins INH1 and INH2 are switched off), the transceiver will enter Star-idle mode (pins INH1 and INH2 are switched on) if the wake flag is set. After entering Star-idle mode the transceiver monitors for activity to choose the appropriate mode transition (see Figure 6).

6.5.3 Remote wake-up

6.5.3.1 Bus wake-up via wake-up pattern

Bus wake-up is detected if two consecutive DATA_0 of at least $t_{det(wake)DATA\_0}$ separated by an idle or DATA_1 of at least $t_{det(wake)idle}$, followed by an idle or DATA_1 of at least $t_{det(wake)idle}$ are present on the bus lines within $t_{det(wake)tot}$.

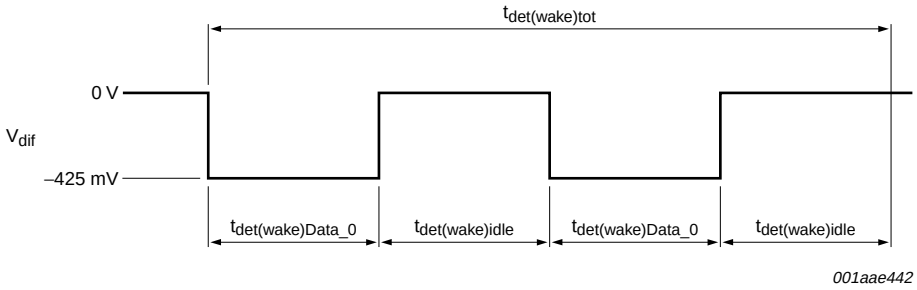


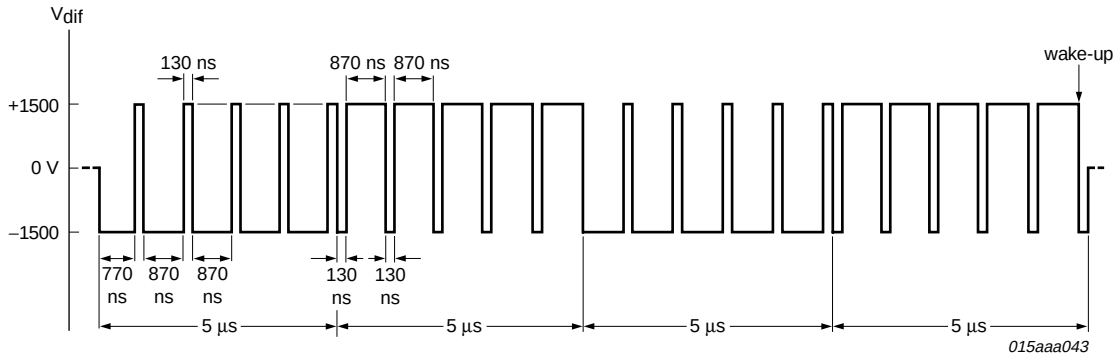
Fig 8. Bus wake-up timing

6.5.3.2 Bus wake-up via dedicated FlexRay data frame

The reception of a dedicated data frame, emulating a valid wake-up pattern, as shown in Figure 9, sets the wake-up flag of the TJA1080ATS/2.

Due to the Byte Start Sequence (BSS), preceding each byte, the DATA_0 and DATA_1 phases for the wake-up symbol are interrupted every 1 µs. For 10 Mbit/s the maximum interruption time is 130 ns. Such interruptions do not prevent the transceiver from recognizing the wake-up pattern in the payload of a data frame.

The wake-up flag will not be set upon reception of an invalid wake-up pattern.



Each interruption is 130 ns.

The transition time from Data_0 to Data_1 and from Data_1 to Data_0 is about 20 ns.

The TJA1080ATS/2 wake-up flag will be set with the following pattern:

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

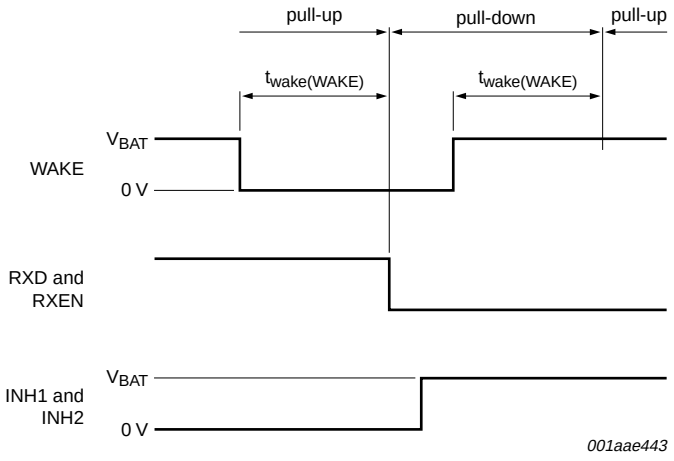
FFh, FFh, FFh, FFh, FFh, FFh

Fig 9. Minimum bus pattern for bus wake-up

6.5.4 Local wake-up via pin WAKE

If the voltage on pin WAKE is lower than $V_{th(det)(WAKE)}$ for longer than $t_{wake(WAKE)}$ (falling edge on pin WAKE) a local wake-up event on pin WAKE is detected. At the same time, the biasing of this pin is switched to pull-down.

If the voltage on pin WAKE is higher than $V_{th(det)(WAKE)}$ for longer than $t_{wake(WAKE)}$, the biasing of this pin is switched to pull-up, and no local wake-up will be detected.



Sleep mode: V_{IO} and (V_{BAT} or V_{CC}) still provided.

Fig 10. Local wake-up timing via pin WAKE

6.6 Fail silent behavior

In order to be fail silent, undervoltage detection and a reset mechanism for the digital state machine is implemented.

If an undervoltage is detected on pins V_{CC}, V_{IO} and/or V_{BAT}, the transceiver will enter a low power mode. This ensures a passive and defined behavior of the transmitter and receiver in case of an undervoltage detection.

In the region between the minimum operating voltage and the undervoltage detection threshold, the principle function of the transmitter and receiver is maintained. However, in this region parameters (e.g. thresholds and delays of the transmitter and receiver) may deviate from the range specified for the operating range.

The digital state machine is supplied by V_{CC}, V_{IO} or V_{BAT}, depending on which voltage is available. Therefore, the digital state machine will be properly supplied as long as the voltage on pin V_{CC} or pin V_{IO} remains above 4.75 V or the voltage on pin V_{BAT} remains above 6.5 V.

If the voltage on all pins V_{CC}, V_{IO} and V_{BAT} breaks down, a reset signal will be given to the digital state machine as soon as the internal supply voltage for the digital state machine is not sufficient for proper operation of the state machine. This ensures a passive and defined behavior of the digital state machine in case of an overall supply voltage breakdown.

6.6.1 V_{BAT} undervoltage

- Node configuration: If the UV_{VBAT} flag is set the transceiver will enter Sleep mode (pins INH1 and INH2 are switched off) regardless of the voltage present on pins EN and STBN. If the undervoltage recovers the wake flag will be set and the transceiver will enter the mode determined by the voltages on pins EN and STBN.
- Star configuration: The TJA1080ATS/2 in star configuration is able to transmit and receive data as long as V_{CC} and V_{IO} are within their operating ranges, regardless of the undervoltage on V_{BAT}.

6.6.2 V_{CC} undervoltage

- Node configuration: If the UV_{VCC} flag is set the transceiver will enter the Standby mode (pin INH2 is switched off) regardless of the voltage present on pins EN and STBN. If the undervoltage recovers or the wake flag is set mode switching via pins EN and STBN is possible.
- Star configuration: If the UV_{VCC} flag is set the transceiver will enter the Star-sleep mode.

6.6.3 V_{IO} undervoltage

- Node configuration: If the voltage on pin V_{IO} is lower than $V_{uvd(VIO)}$ (even if the UV_{VIO} flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the UV_{VIO} flag is set the transceiver will enter Sleep mode (pins INH1 and INH2 are switched off). If the undervoltage recovers or the wake flag is set, mode switching via pins EN and STBN is possible.

- Star configuration: If an undervoltage is present on pin V_{IO} (even if the UV_{VIO} flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the UV_{VIO} flag is set, pin INH1 is switched off. If an undervoltage is present on pin V_{IO} and V_{CC} is within the operating range, the TJA1080ATS/2 will forward the received data on TRXD or bus lines to all other branches.

6.7 Flags

6.7.1 Local wake-up source flag

The local wake-up source flag can only be set in a low power mode. When a wake-up event on pin WAKE is detected (see Section 6.5.4) it sets the local wake-up source flag. The local wake-up source flag is reset by entering a low power mode.

6.7.2 Remote wake-up source flag

The remote wake-up source flag can only be set in a low power mode if pin V_{BAT} is within its operating range. When a remote wake-up event is detected on the bus lines (see Section 6.5.3) it sets the remote wake-up source flag. The remote wake-up source flag is reset by entering a low power mode.

6.7.3 Wake flag

The wake flag is set if one of the following events occurs:

- The local or remote wake-up source flag is set (edge sensitive)
- A positive edge is detected on pin STBN if V_{IO} is present
- Recovery of the UV_{VBAT} flag (only in node configuration)
- By recognizing activity on pins TRXD0 and TRXD1 (only in star configuration)

In node configuration the wake flag is reset by entering Normal mode, a low power mode or setting one of the undervoltage flags. In star configuration the wake flag is reset by entering a low power mode or by recovery of the UV_{VCC} signal (without $t_{rec(uv)(VCC)}$).

6.7.4 Power-on flag

The PWON flag is set if the internal supply voltage for the digital part becomes higher than the lowest value it needs to operate. In node configuration, entering Normal mode resets the PWON flag. In star configuration the PWON flag is reset when the UV_{VCC} signal goes LOW (no undervoltage detected).

6.7.5 Node configuration flag

Configuration flag set means node configuration.

6.7.6 Temperature medium flag

The temperature medium flag is set if the junction temperature exceeds $T_{j(warn)(medium)}$ in a normal power mode while pin V_{BAT} is within its operating range. The temperature medium flag is reset when the junction temperature drops below $T_{j(warn)(medium)}$ in a normal power mode with pin V_{BAT} within its operating range or after a read of the status register in a low power mode while pin V_{BAT} is within its operating range. No action will be taken if this flag is set.

6.7.7 Temperature high flag

The temperature high flag is set if the junction temperature exceeds $T_{j(dis)(high)}$ in a normal power mode while pin V_{BAT} is within its operating range.

In node configuration the temperature high flag is reset if a negative edge is applied to pin TXEN while the junction temperature is lower than $T_{j(dis)(high)}$ in a normal power mode with pin V_{BAT} within its operating range. In star configuration, the temperature high flag is reset by any activity detection (edge) while the junction temperature is lower than $T_{j(dis)(high)}$ in a normal power mode while pin V_{BAT} is within its operating range.

If the temperature high flag is set the transmitter is disabled and pins TRXD0 and TRXD1 are switched off.

6.7.8 TXEN_BGE clamped flag

The TXEN_BGE clamped flag is set if pin TXEN is LOW and pin BGE is HIGH for longer than $t_{detCL(TXEN\_BGE)}$. The TXEN_BGE clamped flag is reset if pin TXEN is HIGH or pin BGE is LOW. If the TXEN_BGE flag is set, the transmitter is disabled.

6.7.9 Bus error flag

The bus error flag is set if pin TXEN is LOW and pin BGE is HIGH and the data received from the bus lines (pins BP and BM) is different to that received on pin TXD. Additionally in star configuration the bus error flag is also set if the data received on the bus lines is different to that received on pins TRXD0 and TRXD1. The transmission of any valid communication element, including a wake-up pattern, does not lead to bus error indication.

The error flag is reset if the data on the bus lines (pins BP and BM) is the same as on pin TXD or if the transmitter is disabled. No action will be taken if the bus error flag is set.

6.7.10 UV_{VBAT} flag

The UV_{VBAT} flag is set if the voltage on pin V_{BAT} is lower than $V_{uvd(VBAT)}$. The UV_{VBAT} flag is reset if the voltage is higher than $V_{uvd(VBAT)}$ or by setting the wake flag; see Section 6.6.1.

6.7.11 UV_{VCC} flag

The UV_{VCC} flag is set if the voltage on pin V_{CC} is lower than $V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$. The flag is reset if the voltage on pin V_{CC} is higher than $V_{uvd(VCC)}$ for longer than $t_{rec(uv)(VCC)}$ or the wake flag is set; see Section 6.6.2.

6.7.12 UV_{VIO} flag

The UV_{VIO} flag is set if the voltage on pin V_{IO} is lower than $V_{uvd(VIO)}$ for longer than $t_{det(uv)(VIO)}$. The flag is reset if the voltage on pin V_{IO} is higher than $V_{uvd(VIO)}$ or the wake flag is set; see Section 6.6.3.

6.7.13 Error flag

The error flag is set if one of the status bits S4 to S12 is set. The error flag is reset if none of the S4 to S12 status bits are set; see Table 10.

6.8 TRXD collision

A TRXD collision is detected when both TRXD lines are LOW for more than the TRXD collision detection time ($t_{det(col)(TRXD)}$) in star configuration.

6.9 Status register

The status register can be read out on pin ERRN by using pin EN as clock; the status bits are given in Table 10. The timing diagram is illustrated in Figure 11.

The status register is accessible if:

- UV_{VIO} flag is not set and the voltage on pin V_{IO} is between 4.75 V and 5.25 V
- UV_{VCC} flag is not set and the voltage on pin V_{IO} is between 2.2 V and 4.75 V

After reading the status register, if no edge is detected on pin EN for longer than $t_{det(EN)}$, the status bits (S4 to S12) will be cleared if the corresponding flag has been reset. Pin ERRN is LOW if the corresponding status bit is set.

Table 10. Status bits

Bit number	Status bit	Description
S0	LOCAL WAKEUP	local wake-up source flag is redirected to this bit
S1	REMOTE WAKEUP	remote wake-up source flag is redirected to this bit
S2	NODE CONFIG	node configuration flag is redirected to this bit
S3	PWON	status bit set means PWON flag has been set previously
S4	BUS ERROR	status bit set means bus error flag has been set previously
S5	TEMP HIGH	status bit set means temperature high flag has been set previously
S6	TEMP MEDIUM	status bit set means temperature medium flag has been set previously
S7	TXEN_BGE CLAMPED	status bit set means TXEN_BGE clamped flag has been set previously
S8	UVVBAT	status bit set means UV_{VBAT} flag has been set previously
S9	UVVCC	status bit set means UV_{VCC} flag has been set previously
S10	UVVIO	status bit set means UV_{VIO} flag has been set previously
S11	STAR LOCKED	status bit is set if Star-locked mode has been entered previously
S12	TRXD COLLISION	status bit is set if a TRXD collision has been detected previously

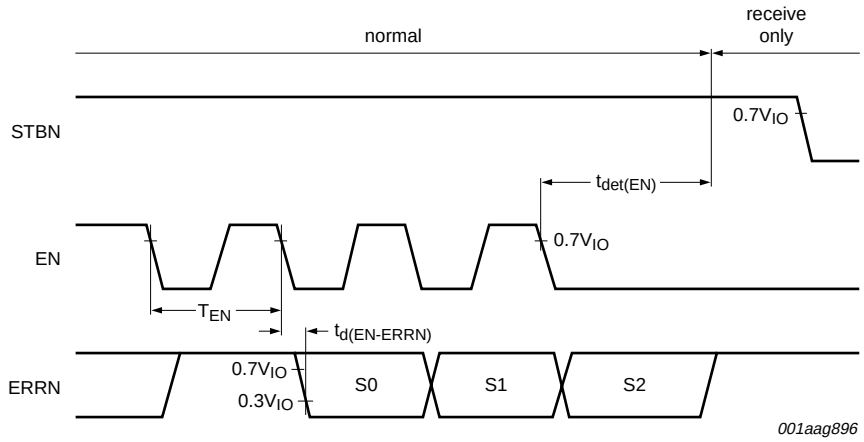


Fig 11. Timing diagram for status bits

7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	supply voltage on pin V_{BAT}	no time limit		–0.3	+60	V
		operating range		6.5	60	V
V_{CC}	supply voltage	no time limit		–0.3	+5.5	V
		operating range		4.75	5.25	V
V_{BUF}	supply voltage on pin V_{BUF}	no time limit		–0.3	+5.5	V
		operating range		4.75	5.25	V
V_{IO}	supply voltage on pin V_{IO}	no time limit		–0.3	+5.5	V
		operating range		2.2	5.25	V
V_{INH1}	voltage on pin INH1			–0.3	V_{BAT} + 0.3	V
V_{INH2}	voltage on pin INH2			–0.3	V_{BAT} + 0.3	V
V_{WAKE}	voltage on pin WAKE			–0.3	V_{BAT} + 0.3	V
$I_{o(WAKE)}$	output current on pin WAKE	pin GND not connected		–15	-	mA
V_{BGE}	voltage on pin BGE	no time limit		–0.3	+5.5	V
V_{TXEN}	voltage on pin TXEN	no time limit		–0.3	+5.5	V
V_{TXD}	voltage on pin TXD	no time limit		–0.3	+5.5	V
V_{ERRN}	voltage on pin ERRN	no time limit		–0.3	V_{IO} + 0.3	V
V_{RXD}	voltage on pin RXD	no time limit		–0.3	V_{IO} + 0.3	V
V_{RXEN}	voltage on pin RXEN	no time limit		–0.3	V_{IO} + 0.3	V
V_{EN}	voltage on pin EN	no time limit		–0.3	+5.5	V
V_{STBN}	voltage on pin STBN	no time limit		–0.3	+5.5	V
V_{TRXD0}	voltage on pin TRXD0	no time limit		–0.3	+5.5	V
V_{TRXD1}	voltage on pin TRXD1	no time limit		–0.3	+5.5	V
V_{BP}	voltage on pin BP	no time limit		–60	+60	V
V_{BM}	voltage on pin BM	no time limit		–60	+60	V
V_{trt}	transient voltage	on pins BP and BM	[1]	–200	+200	V
		on pin V_{BAT}	[2]	–200	+200	V
		on pin V_{BAT}	[3]	6.5	60	V
		on pin V_{BAT}	[4]	-	60	V
T_{stg}	storage temperature			–55	+150	°C
T_{vj}	virtual junction temperature		[5]	–40	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM on pins BP and BM to ground	[6]	–8.0	+8.0	kV
		HBM at any other pin	[7]	–4.0	+4.0	kV
		MM on all pins	[8]	–200	+200	V
		CDM on all pins	[9]	–1000	+1000	V

[1] According to ISO 7637, part 3 test pulses a and b; Class C; see Figure 15; R_L = 45 Ω; C_L = 100 pF.

[2] According to ISO 7637, part 2 test pulses 1, 2, 3a and 3b; Class C; see Figure 15; R_L = 45 Ω; C_L = 100 pF.

[3] According to ISO 7637, part 2 test pulse 4; Class C; see Figure 15; R_L = 45 Ω; C_L = 100 pF.

[4] According to ISO 7637, part 2 test pulse 5b; Class C; see Figure 15; R_L = 45 Ω; C_L = 100 pF; V_{BAT} = 24 V.

[5] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[6] HBM: C = 100 pF; R = 1.5 kΩ.

[7] HBM: C = 100 pF; R = 1.5 kΩ.

[8] MM: C = 200 pF; L = 0.75 µH; R = 10 Ω.

[9] CDM: R = 1 Ω.

8. Thermal characteristics

Table 12. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	126	K/W

9. Static characteristics

Table 13. Static characteristics

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin V_{BAT}							
I_{BAT}	supply current on pin V_{BAT}	low power modes in node configuration; no load on pins IHN1 and IHN2		-	-	55	µA
		Star-sleep mode		-	-	55	µA
		Star-standby mode; no load on pins IHN1 and IHN2		-	-	150	µA
		normal power modes		-	-	1	mA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}			2.75	-	4.5	V
Pin V_{CC}							
I_{CC}	supply current	low power modes		−1	0	+10	µA
		Normal mode; V_{BGE} = 0 V; V_{TXEN} = V_{IO}; Receive-only mode; Star-idle mode		-	-	15	mA
		Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V; V_{BUF} open	[1]	-	-	35	mA
		Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V; R_{bus} = ∞ Ω		-	-	15	mA
		Star-transmit mode		-	-	62	mA
		Star-receive mode		-	-	42	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	V_{BAT} > 5.5 V		2.75	-	4.5	V
Pin V_{IO}							
I_{IO}	supply current on pin V_{IO}	low power modes		−1	+1	+10	µA
		Normal and Receive-only modes; V_{TXD} = V_{IO}		-	-	1000	µA

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}			1	-	2	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin V_{IO}			1	-	2.2	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin V_{IO}	V_{BAT} > 5.5 V		25	-	200	mV
Pin V_{BUF}							
I_{BUF}	supply current on pin V_{BUF}	low power modes in node configuration		−1	0	+10	µA
		low power modes in star configuration					
		V_{BUF} = 0 V; V_{CC} = 0 V		−40	−20	+1	µA
		V_{BUF} = 5.25 V		−1	0	+15	µA
		Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V; V_{BUF} = V_{CC}	[1]	-	-	35	mA
		Star-transmit mode		-	-	62	mA
		Star-receive mode		-	-	42	mA
		Normal mode; V_{BGE} = 0 V; V_{TXEN} = V_{IO}; Receive-only mode; Star-idle mode		-	-	15	mA
$V_{BUF(on)}$	on-state voltage on pin V_{BUF}	V_{CC} switch is switched on; Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V; V_{CC} > maximum value of $V_{uvd(VCC)}$		V_{CC} − 0.25	-	V_{CC}	V
$V_{BUF(off)}$	off-state voltage on pin V_{BUF}	V_{CC} switch is switched off; low power modes in star configuration; V_{CC} < minimum value of $V_{uvd(VCC)}$		4.5	-	5.25	V
Pin EN							
$V_{IH(EN)}$	HIGH-level input voltage on pin EN			0.7V_{IO}	-	5.5	V
$V_{IL(EN)}$	LOW-level input voltage on pin EN			−0.3	-	0.3V_{IO}	V
$I_{IH(EN)}$	HIGH-level input current on pin EN	V_{EN} = 0.7V_{IO}		3	-	11	µA
$I_{IL(EN)}$	LOW-level input current on pin EN	V_{EN} = 0 V		−1	0	+1	µA

Table 13. Static characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin STBN							
$V_{IH(STBN)}$	HIGH-level input voltage on pin STBN			$0.7V_{IO}$	-	5.5	V
$V_{IL(STBN)}$	LOW-level input voltage on pin STBN			−0.3	-	$0.3V_{IO}$	V
$I_{IH(STBN)}$	HIGH-level input current on pin STBN	$V_{STBN} = 0.7V_{IO}$		3	-	11	µA
$I_{IL(STBN)}$	LOW-level input current on pin STBN	V_{STBN} = 0 V		−1	0	+1	µA
Pin TXEN							
$V_{IH(TXEN)}$	HIGH-level input voltage on pin TXEN			$0.7V_{IO}$	-	5.5	V
$V_{IL(TXEN)}$	LOW-level input voltage on pin TXEN			−0.3	-	$0.3V_{IO}$	V
$I_{IH(TXEN)}$	HIGH-level input current on pin TXEN	$V_{TXEN} = V_{IO}$		−1	0	+1	µA
$I_{IL(TXEN)}$	LOW-level input current on pin TXEN	$V_{TXEN} = 0.3V_{IO}$		−15	-	−3	µA
$I_{L(TXEN)}$	leakage current on pin TXEN	V_{TXEN} = 5.25 V; V_{IO} = 0 V		−1	0	+1	µA
Pin BGE							
$V_{IH(BGE)}$	HIGH-level input voltage on pin BGE			$0.7V_{IO}$	-	5.5	V
$V_{IL(BGE)}$	LOW-level input voltage on pin BGE			−0.3	-	$0.3V_{IO}$	V
$I_{IH(BGE)}$	HIGH-level input current on pin BGE	$V_{BGE} = 0.7V_{IO}$		3	-	11	µA
$I_{IL(BGE)}$	LOW-level input current on pin BGE	V_{BGE} = 0 V		−1	0	+1	µA
Pin TXD							
$V_{IH(TXD)}$	HIGH-level input voltage on pin TXD	normal power modes		$0.7V_{IO}$	-	V_{IO} + 0.3	V
$V_{IL(TXD)}$	LOW-level input voltage on pin TXD	normal power modes		−0.3	-	$0.3V_{IO}$	V
$I_{IH(TXD)}$	HIGH-level input current on pin TXD	$V_{TXD} = V_{IO}$		70	300	650	µA
$I_{IL(TXD)}$	LOW-level input current on pin TXD	normal power modes; V_{TXD} = 0 V		−5	0	+5	µA
		low power modes		−1	0	+1	µA
$I_{LI(TXD)}$	input leakage current on pin TXD	V_{TXD} = 5.25 V; V_{IO} = 0 V		−1	0	+1	µA
$C_{i(TXD)}$	input capacitance on pin TXD	not tested; with respect to all other pins at ground; V_{TXD} = 100 mV; f = 5 MHz	[2]	-	5	10	pF

Table 13. Static characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin RXD						
$I_{OH(RXD)}$	HIGH-level output current on pin RXD	$V_{RXD} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$	−20	-	−2	mA
$I_{OL(RXD)}$	LOW-level output current on pin RXD	V_{RXD} = 0.4 V	2	-	20	mA
Pin ERRN						
$I_{OH(ERRN)}$	HIGH-level output current on pin ERRN	node configuration; $V_{ERRN} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$	−1500	−550	−100	µA
		star configuration; $V_{ERRN} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$	−1	0	+1	µA
$I_{OL(ERRN)}$	LOW-level output current on pin ERRN	V_{ERRN} = 0.4 V	300	700	1500	µA
Pin RXEN						
$I_{OH(RXEN)}$	HIGH-level output current on pin RXEN	$V_{RXEN} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$	−4	−1.5	−0.5	mA
$I_{OL(RXEN)}$	LOW-level output current on pin RXEN	V_{RXEN} = 0.4 V	1	3	8	mA
Pins TRXD0 and TRXD1						
$V_{IH(TRXD0)}$	HIGH-level input voltage on pin TRXD0	Star-idle and Star-transmit modes	$0.7V_{BUF}$	-	V_{BUF} + 0.3	V
$V_{IL(TRXD0)}$	LOW-level input voltage on pin TRXD0	Star-idle and Star-transmit modes	−0.3	-	$0.3V_{BUF}$	V
$V_{OL(TRXD0)}$	LOW-level output voltage on pin TRXD0	R_{pu} = 200 Ω	−0.3	-	+0.8	V
$V_{IH(TRXD1)}$	HIGH-level input voltage on pin TRXD1	Star-idle and Star-transmit modes	$0.7V_{BUF}$	-	V_{BUF} + 0.3	V
$V_{IL(TRXD1)}$	LOW-level input voltage on pin TRXD1	Star-idle and Star-transmit modes	−0.3	-	$0.3V_{BUF}$	V
$V_{OL(TRXD1)}$	LOW-level output voltage on pin TRXD1	R_{pu} = 200 Ω	−0.3	-	+0.8	V
Pins BP and BM						
$V_{o(idle)(BP)}$	idle output voltage on pin BP	Normal, Receive-only, Star-idle, Star-transmit and Star-receive modes; $V_{TXEN} = V_{IO}$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
		Standby, Go-to-sleep, Sleep, Star-standby and Star-sleep modes	−0.1	0	+0.1	V

Table 13. Static characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(idle)(BM)}$	idle output voltage on pin BM	Normal, Receive-only, Star-idle, Star-transmit and Star-receive modes; $V_{TXEN} = V_{IO}$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
		Standby, Go-to-sleep, Sleep, Star-standby and Star-sleep modes	−0.1	0	+0.1	V
$I_{o(idle)BP}$	idle output current on pin BP	−60 V ≤ $\|V_{BP}\|$ ≤ +60 V	−7.5	-	+7.5	mA
$I_{o(idle)BM}$	idle output current on pin BM	−60 V ≤ $\|V_{BM}\|$ ≤ +60 V	−7.5	-	+7.5	mA
$V_{o(idle)(dif)}$	differential idle output voltage		−25	0	+25	mV
$V_{OH(dif)}$	differential HIGH-level output voltage	40 Ω ≤ R_{bus} ≤ 55 Ω $V_{CC} = V_{BUF}$ = 5 V	600	800	1500	mV
$V_{OL(dif)}$	differential LOW-level output voltage	40 Ω ≤ R_{bus} ≤ 55 Ω $V_{CC} = V_{BUF}$ = 5 V	−1500	−800	−600	mV
$V_{IH(dif)}$	differential HIGH-level input voltage	normal power modes −10 V ≤ V_{BP} ≤ +15 V −10 V ≤ V_{BM} ≤ +15 V	150	225	300	mV
$V_{IL(dif)}$	differential LOW-level input voltage	normal power modes −10 V ≤ V_{BP} ≤ +15 V −10 V ≤ V_{BM} ≤ +15 V	−300	−225	−150	mV
		low power modes −10 V ≤ V_{BP} ≤ +15 V −10 V ≤ V_{BM} ≤ +15 V	−400	−225	−125	mV
$\Delta V_{i(dif)(H-L)}$	differential input voltage difference between HIGH-level and LOW-level	normal power modes (V_{BP} + V_{BM}) / 2 = 2.5 V	-	-	10	%
$\|V_{i(dif)det(act)}\|$	activity detection differential input voltage (absolute value)	normal power modes	150	225	300	mV
$\|I_{o(sc)(BP)}\|$	short-circuit output current on pin BP (absolute value)	V_{BP} = 0 V, 60 V	10	20	35	mA
$\|I_{o(sc)(BM)}\|$	short-circuit output current on pin BM (absolute value)	V_{BM} = 0 V, 60 V	10	20	35	mA
$R_{i(BP)}$	input resistance on pin BP	idle level; R_{bus} = ∞ Ω	10	20	40	kΩ
$R_{i(BM)}$	input resistance on pin BM	idle level; R_{bus} = ∞ Ω	10	20	40	kΩ
$R_{i(dif)(BP-BM)}$	differential input resistance between pin BP and pin BM	idle level; R_{bus} = ∞ Ω	20	40	80	kΩ
$I_{LI(BP)}$	input leakage current on pin BP	V_{BP} = 5 V; $V_{BAT} = V_{CC} = V_{IO}$ = 0 V	−10	0	+10	µA

Table 13. Static characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{LI(BM)}$	input leakage current on pin BM	V_{BM} = 5 V; $V_{BAT} = V_{CC} = V_{IO}$ = 0 V		−10	0	+10	µA
$V_{cm(bus)(DATA\_0)}$	DATA_0 bus common-mode voltage	R_{bus} = 45 Ω		$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
$V_{cm(bus)(DATA\_1)}$	DATA_1 bus common-mode voltage	R_{bus} = 45 Ω		$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
$\Delta V_{cm(bus)}$	bus common-mode voltage difference	R_{bus} = 45 Ω		−25	0	+25	mV
$C_{i(BP)}$	input capacitance on pin BP	not tested; with respect to all other pins at ground; V_{BP} = 100 mV; f = 5 MHz	[2]	-	8	15	pF
$C_{i(BM)}$	input capacitance on pin BM	not tested; with respect to all other pins at ground; V_{BM} = 100 mV; f = 5 MHz	[2]	-	8	15	pF
$C_{i(dif)(BP-BM)}$	differential input capacitance between pin BP and pin BM	not tested; with respect to all other pins at ground; $V_{(BM-BP)}$ = 100 mV; f = 5 MHz	[2]	-	2	5	pF
Pin INH1							
$V_{OH(INH1)}$	HIGH-level output voltage on pin INH1	I_{INH1} = −0.2 mA		V_{BAT} − 0.8	-	V_{BAT}	V
$I_{L(INH1)}$	leakage current on pin INH1	Sleep mode		−5	0	+5	µA
$I_{OL(INH1)}$	LOW-level output current on pin INH1	V_{INH1} = 0 V		−15	-	-	mA
Pin INH2							
$V_{OH(INH2)}$	HIGH-level output voltage on pin INH2	I_{INH2} = −0.2 mA		V_{BAT} − 0.8	-	V_{BAT}	V
$I_{L(INH2)}$	leakage current on pin INH2	Sleep mode		−5	0	+5	µA
$I_{OL(INH2)}$	LOW-level output current on pin INH2	V_{INH2} = 0 V		−15	-	-	mA
Pin WAKE							
$V_{th(det)(WAKE)}$	detection threshold voltage on pin WAKE	low power mode		2.5	-	4.5	V
$I_{IL(WAKE)}$	LOW-level input current on pin WAKE	V_{WAKE} = 2.4 V for $t > t_{wake(WAKE)}$		3	-	11	µA
$I_{IH(WAKE)}$	HIGH-level input current on pin WAKE	V_{WAKE} = 4.6 V for $t > t_{wake(WAKE)}$		−11	-	−3	µA
Temperature protection							
$T_{j(warn)(medium)}$	medium warning junction temperature	V_{BAT} > 5.5 V		155	165	175	°C
$T_{j(dis)(high)}$	high disable junction temperature	V_{BAT} > 5.5 V		180	190	200	°C

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power-on reset						
$V_{th(det)POR}$	power-on reset detection threshold voltage		3.0	-	3.4	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage		3.1	-	3.5	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		100	-	200	mV

[1] Current flows from V_{CC} to V_{BUF}. This means that the maximum sum current I_{CC} + I_{BUF} is 35 mA.

[2] These values are based on measurements taken on several samples (less than 10 pieces). These measurements have taken place in the laboratory and have been done at T_{amb} = 25 °C and T_{amb} = 125 °C. No characterization has been done for these parameters. No industrial test will be performed on production products.

10. Dynamic characteristics

Table 14. Dynamic characteristics

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pins BP and BM							
$t_{d(TXD-bus)}$	delay time from TXD to bus	Normal or Star-transmit mode	[1]				
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
$\Delta t_{d(TXD-bus)}$	delay time difference from TXD to bus	Normal or Star-transmit mode; between DATA_0 and DATA_1	[1]	-	-	4	ns
$t_{d(TRXD-bus)}$	delay time from TRXD to bus	Star-transmit mode	[2]				
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
$\Delta t_{d(TRXD-bus)}$	delay time difference from TRXD to bus	Star-transmit mode; between DATA_0 and DATA_1	[2][3]	-	-	5	ns
$t_{d(bus-RXD)}$	delay time from bus to RXD	Normal or Star-transmit mode; C_{RXD} = 15 pF; see Figure 13					
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
$\Delta t_{d(bus-RXD)}$	delay time difference from bus to RXD	Normal or Star-transmit mode; C_{RXD} = 15 pF; between DATA_0 and DATA_1; see Figure 13		-	-	5	ns
$t_{d(bus-TRXD)}$	delay time from bus to TRXD	Star-receive mode; see Figure 13					
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns

Table 14. Dynamic characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta t_{d(bus-TRXD)}$	delay time difference from bus to TRXD	Star-receive mode; between DATA_0 and DATA_1; see Figure 13	[3]	-	-	5	ns
$t_{d(TXEN-busidle)}$	delay time from TXEN to bus idle	Normal mode		-	-	100	ns
$t_{d(TXEN-busact)}$	delay time from TXEN to bus active	Normal mode		-	-	75	ns
$t_{d(BGE-busidle)}$	delay time from BGE to bus idle	Normal mode		-	-	100	ns
$t_{d(BGE-busact)}$	delay time from BGE to bus active	Normal mode		-	-	75	ns
$t_{d(bus)(idle-act)}$	bus delay time from idle to active	Normal mode		-	-	30	ns
$t_{d(bus)(act-idle)}$	bus delay time from active to idle	Normal mode		-	-	30	ns
$t_{r(dif)(bus)}$	bus differential rise time	10 % to 90 % R_L = 45 Ω; C_L = 100 pF		5	12	25	ns
$t_{f(dif)(bus)}$	bus differential fall time	90 % to 10 % R_L = 45 Ω C_L = 100 pF		5	12	25	ns
WAKE symbol detection							
$t_{det(wake)DATA\_0}$	DATA_0 wake-up detection time	Standby, Sleep, Star-standby or Star-sleep modes 10 V ≤ V_{BP} ≤ +15 V 10 V ≤ V_{BM} ≤ +15 V		1	-	4	µs
$t_{det(wake)idle}$	idle wake-up detection time			1	-	4	µs
$t_{det(wake)tot}$	total wake-up detection time			50	-	115	µs
Undervoltage							
$t_{det(uv)(VCC)}$	undervoltage detection time on pin V_{CC}			100	-	670	ms
$t_{rec(uv)(VCC)}$	undervoltage recovery time on pin V_{CC}			1	-	5.2	ms
$t_{det(uv)(VIO)}$	undervoltage detection time on pin V_{IO}			100	-	670	ms
$t_{to(uv)(VCC)}$	undervoltage time-out time on pin V_{CC} for entering Standby mode	star configuration; wake flag is set		432	-	900	µs
$t_{det(uv)(VBAT)}$	undervoltage detection time on pin V_{BAT}			-	-	1	ms
Activity detection							
$t_{det(act)(TXEN)}$	activity detection time on pin TXEN	star configuration		100	-	200	ns
$t_{det(act)(TRXD)}$	activity detection time on pin TRXD	star configuration		100	-	200	ns
$t_{det(act)(bus)}$	activity detection time on bus pins	V_{dif}: 0 mV → 400 mV		100	-	250	ns
$t_{det(idle)(TXEN)}$	idle detection time on pin TXEN	star configuration		100	-	200	ns
$t_{det(idle)(TRXD)}$	idle detection time on pin TRXD	star configuration		50	-	100	ns
$t_{det(idle)(bus)}$	idle detection time on bus pins	V_{dif}: 400 mV → 0 mV		100	-	250	ns
Star modes							

Table 14. Dynamic characteristics *…continued*

All parameters are guaranteed for V_{BAT} = 6.5 V to 60 V; V_{CC} = 4.75 V to 5.25 V; V_{BUF} = 4.75 V to 5.25 V; V_{IO} = 2.2 V to 5.25 V; T_{vj} = −40 °C to +150 °C; R_{bus} = 45 Ω; R_{TRXD} = 200 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(idle-sleep)}$	idle to sleep time-out time		640	-	2660	ms
$t_{to(tx-locked)}$	transmit to locked time-out time		2600	-	10400	µs
$t_{to(rx-locked)}$	receive to locked time-out time		2600	-	10400	µs
$t_{to(locked-sleep)}$	locked to sleep time-out time		64	-	333	ms
$t_{to(locked-idle)}$	locked to idle time-out time		1.4	-	5.1	µs
Node modes						
$t_{d(STBN-RXD)}$	STBN to RXD delay time	STBN HIGH to RXD HIGH; wake flag set	-	-	2	µs
$t_{d(STBN-INH2)}$	STBN to INH2 delay time	STBN LOW to INH2 floating; Normal mode	-	-	10	µs
$t_{h(gotosleep)}$	go-to-sleep hold time		20	35	50	µs
Status register						
$t_{det(EN)}$	detection time on pin EN	for mode control	20	-	80	µs
T_{EN}	time period on pin EN	for reading status bits	4	-	20	µs
$t_{d(EN-ERRN)}$	delay time from EN to ERRN	for reading status bits	-	-	2	µs
WAKE						
$t_{wake(WAKE)}$	wake-up time on pin WAKE	low power mode; falling edge on pin WAKE; 6.5 V ≤ V_{BAT} ≤ 27 V	5	25	100	µs
		low power mode; falling edge on pin WAKE; 27 V < V_{BAT} ≤ 60 V	25	75	175	µs
Miscellaneous						
$t_{detCL(TXEN\_BGE)}$	TXEN_BGE clamp detection time		2600	-	10400	µs
$t_{det(col)(TRXD)}$	TRXD collision detection time	TRXD0 and TRXD1	20	-	-	ns

[1] Rise and fall time (10 % to 90 %) of $t_{r(TXD)}$ and $t_{f(TXD)}$ = 5 ns ± 1ns.

[2] Rise and fall time (10 % to 90 %) of $t_{r(TRXD)}$ and $t_{f(TRXD)}$ = 5 ns ± 1ns.

[3] The worst case asymmetry from one branch to another is the sum of the delay difference from TRXD0 and TRXD1 to DATA_0 and DATA_1 plus the delay difference from DATA_0 and DATA_1 to TRXD0 and TRXD1.

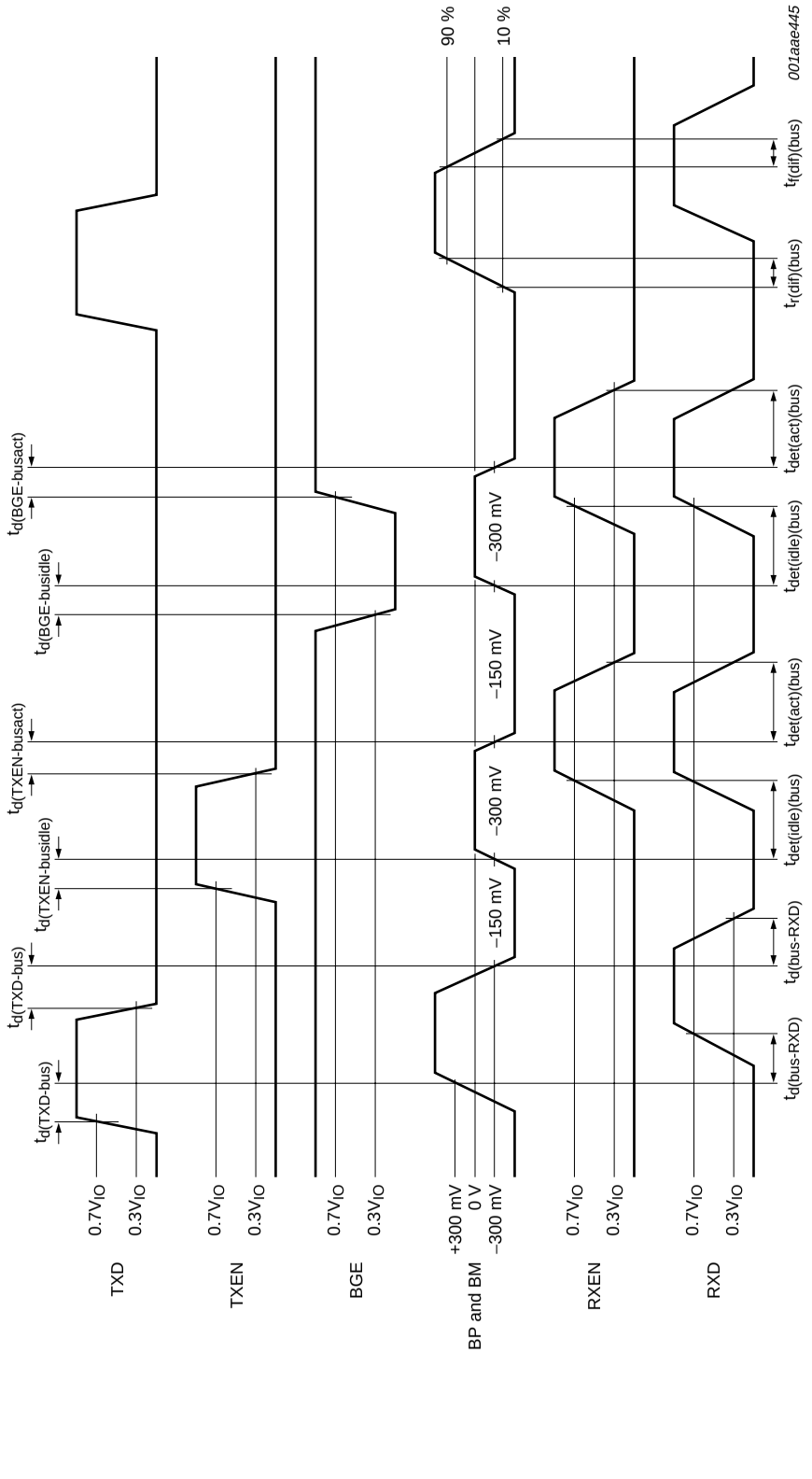
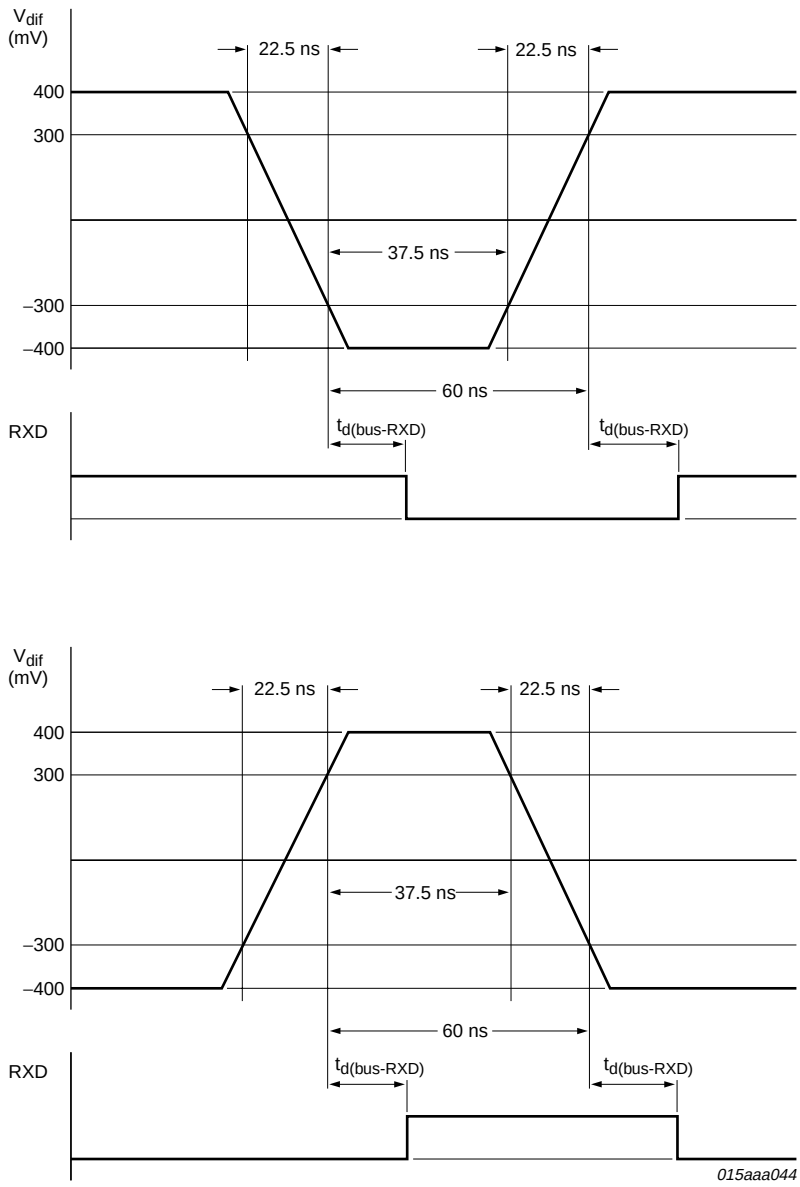


Fig 12. Detailed timing diagram in node configuration



V_{dif} is the receiver test signal.

Fig 13. Receiver test signal

11. Test information

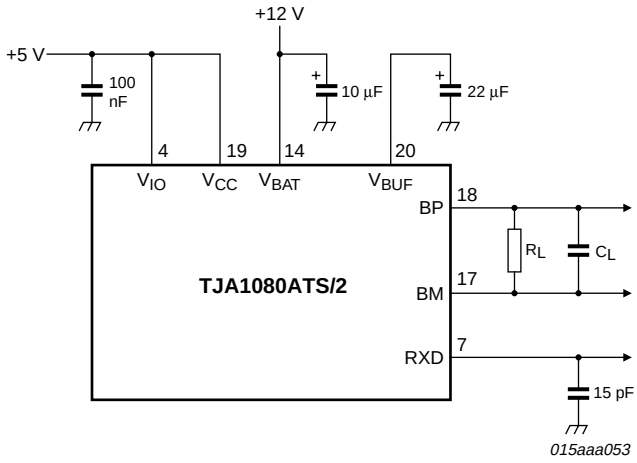
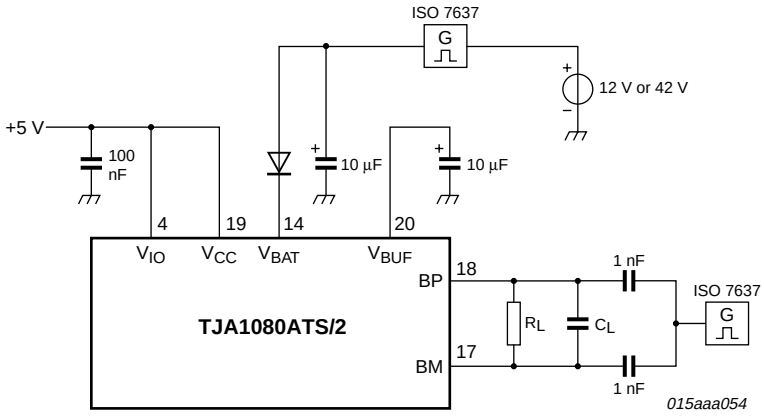


Fig 14. Test circuit for dynamic characteristics



The waveforms of the applied transients are in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 4 and 5.

Test conditions:

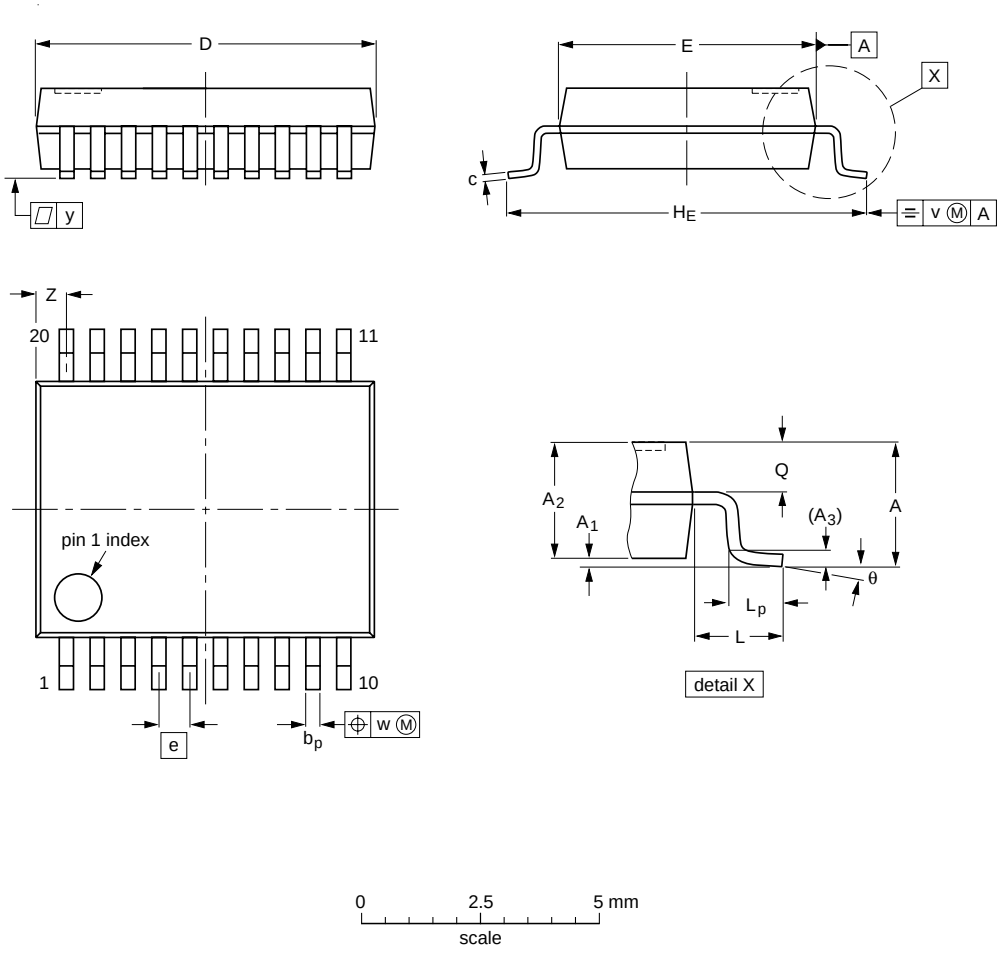
Normal mode: bus idle

Normal mode: bus active; TXD at 5 MHz and TXEN at 1 kHz

Fig 15. Test circuit for automotive transients

12. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT339-1 (SSOP20)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020C)

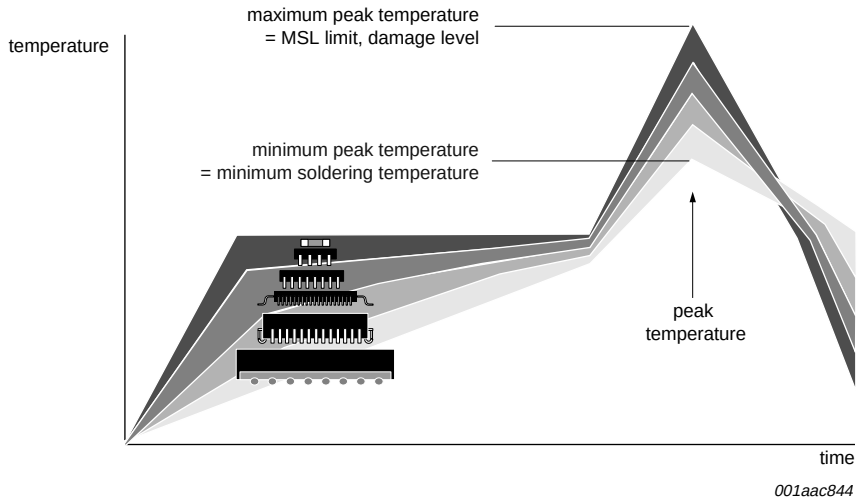
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Appendix

14.1 Differences between TJA1080 and TJA1080ATS/2

14.1.1 Start-up

Table 17. Start-up differences between TJA1080 and TJA1080ATS/2

TJA1080	TJA1080ATS/2
At power-up V_{BAT} should be supplied first. When V_{BAT} reaches 6.5 V, V_{CC} and V_{IO} may be switched on with a delay of at least 60 µs with respect to V_{BAT}.	The TJA1080ATS/2 initialization is independent of the way the voltage supplies V_{BAT}, V_{CC} and V_{IO} ramp up. A dedicated power-up sequence is not necessary.

14.1.2 Bus error detection

Table 18. Bus error detection differences between TJA1080 and TJA1080ATS/2

TJA1080	TJA1080ATS/2
The TJA1080 expects that a data frame begins with a bit value other than the last bit of the previous data frame. This is the case for a valid data frame which begins with the DATA_0 period of the Transmission Start Sequence (TSS) and ends with the DATA_1 bit of the Frame End Sequence (FES). Any violation of this frame format will be detected by the TJA1080. Consequently, when transmitting a wake-up pattern, a bus error will be signalled. This error indication should be ignored and the status register should be cleared by reading the vector.	The transmission of any valid communication element, including a wake-up pattern, does not lead to bus error indication.

14.1.3 Wake-up signalling via RXD pin

Table 19. Wake-up signalling via RXD differences between TJA1080 and TJA1080ATS/2

TJA1080	TJA1080ATS/2
In case of an undervoltage condition at V_{CC}, pin RXD might go to LOW level. For a correct wake-up recognition during a V_{CC} undervoltage condition, pin RXEN can be used.	In case of an undervoltage condition at V_{CC}, pin RXD can be used for correct wake-up signalling.

14.1.4 Asymmetric delay and minimum bit time

Table 20. Minimum bit time differences between TJA1080 and TJA1080ATS/2

TJA1080	TJA1080ATS/2
The TJA1080 guarantees minimum bit times of 80 ns for a receiver test signal of 600 mV (see Figure 13) and asymmetric delay time of ±5 ns (see Table 14).	The TJA1080ATS/2 guarantees minimum bit times of 60 ns for a receiver test signal of 400 mV (see Figure 13) and asymmetric delay time of less than ±5 ns (see Table 14).

14.1.5 Transmitter symmetry

The transmitter symmetry has been improved with respect to the TJA1080. With this improvement, the TJA1080ATS/2 features less EME than the TJA1080.

14.1.6 Impact of input signals on pin EN

Table 21. Input signals on pin EN: differences between TJA1080 and TJA1080ATS/2

TJA1080	TJA1080ATS/2
Certain pulses on pin EN may lead to a hang-up of the digital input of pin EN.	This issue has been resolved in the TJA1080ATS/2

15. Abbreviations

Table 22. Abbreviations

Abbreviation	Description
BSS	Byte Start Sequence
CAN	Controller Area Network
CDM	Charged Device Model
EMC	ElectroMagnetic Compatibility
EME	ElectroMagnetic Emission
EMI	ElectroMagnetic Immunity
ESD	ElectroStatic Discharge
FES	Frame End Sequence
HBM	Human Body Model
MM	Machine Model
PWON	Power-on
TSS	Transmission Start Sequence

16. References

[1] **EPL —** FlexRay Communications System Electrical Physical Layer Specification Version 2.1 Rev. A, FlexRay Consortium, Dec. 2005

[2] **PS54 —** Product specification: TJA1054; Fault-tolerant CAN transceiver, www.nxp.com

[3] **PS41 —** Product specification: TJA1041; High speed CAN transceiver, www.nxp.com

[4] **DS80 —** Product data sheet: TJA1080; FlexRay transceiver, www.nxp.com

17. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1080A_4	20090219	Preliminary data sheet	-	TJA1080A_3
Modifications:	• Product name changed to TJA1080ATS/2 • Table 13: table note section revised • Table 14: table note section revised			
TJA1080A_3	20090115	Preliminary data sheet	-	TJA1080A_2
TJA1080A_2	20080826	Preliminary data sheet	-	TJA1080A_1
TJA1080A_1	20071029	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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