TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6564AHQ (THB6064AH)

PWM Chopper-Type bipolar
Stepping Motor Driver IC

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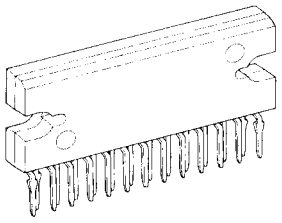


HZIP25-P-1.27

Weight:
HZIP25-P-1.27: 9.86 g (typ.)

The TB6564AHQ(THB6064AH) is a PWM chopper-type sinusoidal micro-step bipolar stepping motor driver IC.
It supports 8 kind of excitation modes and forward/reverse mode and is capable of low-vibration, high-performance drive of 2-phase bipolar type stepping motors using only a clock signal.

Features

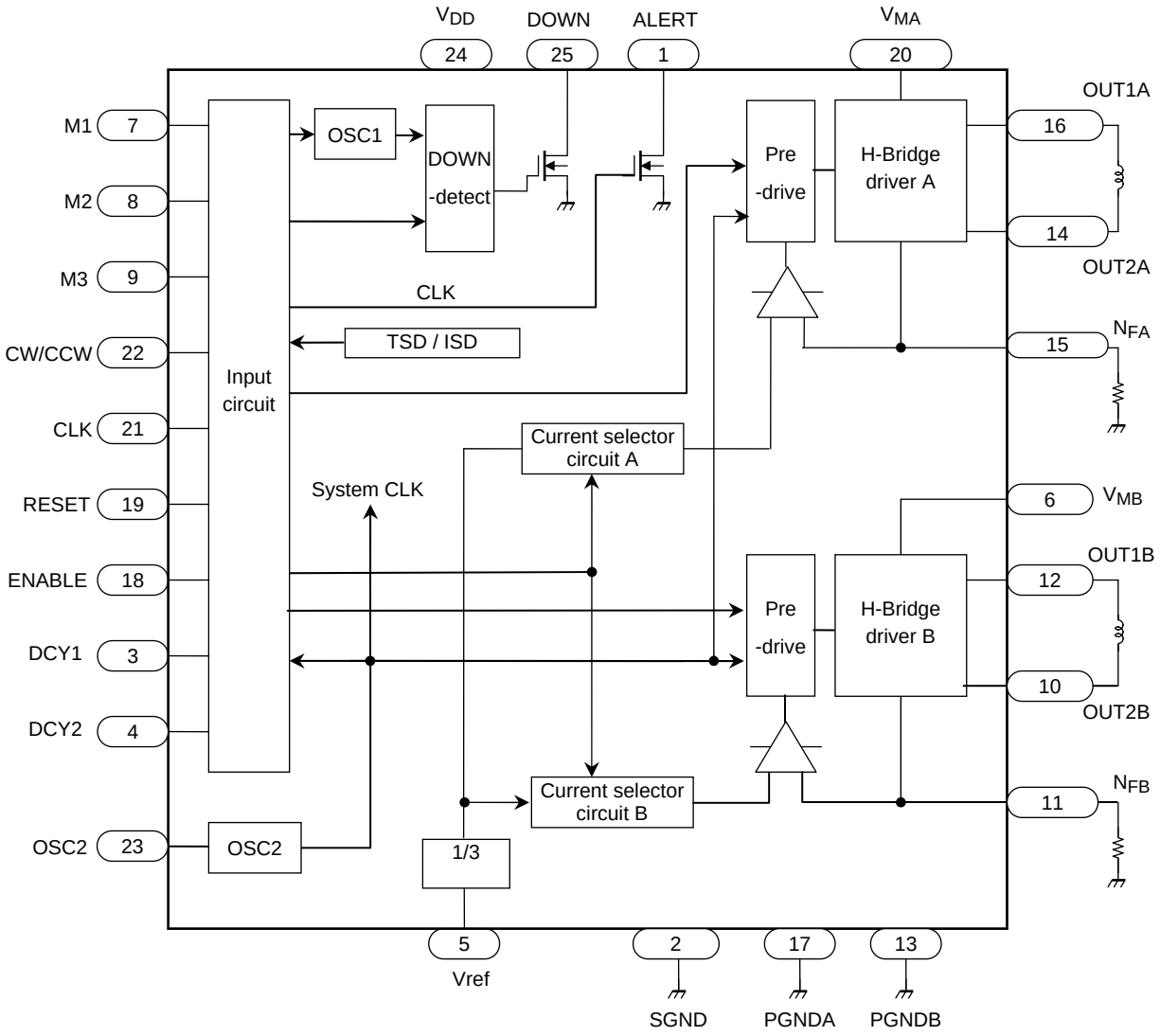
- Single-chip bipolar sinusoidal micro-step stepping motor driver
- Uses high withstand voltage BiCD process:
  Ron (upper, lower) = 0.4 Ω (typ.)
- Forward and reverse rotation control available
- Selectable phase drive (1/2,1/8,1/10, 1/16, 1/20, 1/32, 1/40, 1/64 step)
- Output withstand voltage: VDSS = 50 V
- Output current: I_{OUT} = 4.5 A (absolute maximum ratings, peak, within 100ms)
  I_{OUT} = 4.0 A (operating range, maximal value)
- Packages: HZIP25-P-1.27
- Output monitor pins (DOWN / ALERT)
- Equipped with reset and enable pins
- Built-in thermal shutdown(TSD) and over-current detection(ISD) circuit

The TB6564AHQ(THB6064AH) is a Sn-Ag plated product including Pb.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

These ICs are highly sensitive to electrostatic discharge. When handling them, ensure that the environment is protected against electrostatic discharge. Ensure also that the ambient temperature and relative humidity are maintained at reasonable level.

ESD(Electro-Static Discharge) : HBM±1500V, MM±150V (design target value)

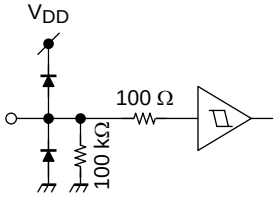
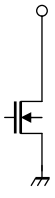
Block Diagram



Pin Functions

Pin No.	I/O	Symbol	Functional Description	Remark
1	Output	ALERT	TSD / ISD monitor pin	
2	—	SGND	Signal ground	
3	Input	DCY1	Mixed decay ratio setting pin	Built-in pull-down resistor
4	Input	DCY2	Mixed decay ratio setting pin	Built-in pull-down resistor
5	Input	Vref	Voltage input for 100% current level	
6	Input	V_{MB}	Power supply	
7	Input	M1	Excitation mode setting input pin	Built-in pull-down resistor
8	Input	M2	Excitation mode setting input pin	Built-in pull-down resistor
9	Input	M3	Excitation mode setting input pin	Built-in pull-down resistor
10	Output	OUT2B	B channel output 2	
11	—	N_{FB}	B channel output current detection pin	Connect external resistor
12	Output	OUT1B	B channel output 1	
13	—	PGNDB	Power ground	
14	Output	OUT2A	A channel output 2	
15	—	N_{FA}	B channel output current detection pin	Connect external resistor
16	Output	OUT1A	A channel output 1	
17	—	PGNDA	Power ground	
18	Input	ENABLE	Enable signal input pin	H: Enable, L: all output off Built-in pull-down resistor
19	Input	RESET	Reset signal input pin	Built-in pull-down resistor
20	Input	V_{MA}	Power supply	
21	Input	CLK	CLK pulse input pin	Built-in pull-down resistor
22	Input	CW/CCW	Forward/reverse control pin	L: Forward, H: reverse Built-in pull-down resistor
23	—	OSC2	Resistor connection pin for chopping frequency setting	Connect external resistor
24	input	V_{DD}	Control side power pin	
25	Output	DOWN	CLK frequency monitor pin	

<Terminal circuits>

Input pins (M1, M2, M3, CLK, CW/CCW, DCY1, DCY2, ENABLE and RESET)	Output pins (DOWN and ALERT)
	

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{DD}	6	V
	$V_{MA/B}$	50	
Output current	$I_{O\ (PEAK)}$	4.5(Note 1)	A/phase
Drain current (ALERT, DOWN)	I_{ALERT}	1	mA
	I_{DOWN}		
Input voltage	V_{IN}	5.5	V
Power dissipation	P_D	5 (Note 2)	W
		43 (Note 3)	
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: T = 100ms

Note 2: Ta = 25°C, No heat sink.

Note 3: Ta = 25°C, with infinite heat sink.

Operating Range (Ta = –30 to 85°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	$V_{MA/B}$	$V_{MA/B} \geqq V_{DD}$	4.5	—	42	
Output current	I_{OUT}	—	—	—	4	A
Input voltage	V_{IN}	—	0	—	5.5	V
	V_{ref}(*)	—	0.5	—	3.0	
Clock frequency(**)	f_{CLK}	—	—	—	200	kHz
Chopping frequency	f_{chop}	(design target value)	15	40	65	kHz
OSC frequency	f_{OSC2}		2.6	4.0	5.4	MHz

(*) Do not apply 3.5V or over to the Vref terminal.

(**) IC can not be damaged within 200kHz. However, the customer can accept that a motor does not always rotate at high frequency of CLK.

Electrical Characteristics (Ta = 25°C, V_{DD} = 5V, V_M = 24V)

Control circuit

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE, DCY1, DCY2	2.0	—	V_{DD}	V
	Low	$V_{IN\ (L)}$		−0.2	—	0.8	
Input hysteresis voltage		V_H		—	400	—	mV
Input current		$I_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE, DCY1, DCY2 V_{IN} = 5.0 V	—	55	80	μA
		$I_{IN\ (L)}$	V_{IN} = 0 V	—	—	1	
VDD supply current		I_{DD1}	Output open, RESET: H, ENABLE: H M1:L, M2:L, M3:L (1/2-step mode)	—	3	7	mA
		I_{DD2}	RESET: L, ENABLE: H	—	2	7	
		I_{DD3}	RESET: L, ENABLE: L	—	2	7	
V_M supply current		I_{M1}	RESET: H/L, ENABLE: L	—	0.5	—	mA
		I_{M2}	RESET: H/L, ENABLE: H	—	1	—	
Vref input circuit	Input current	$I_{IN(ref)}$	Vref=3.0V	—	—	1	μA
	Divider ratio	V_{ref}/V_{NF}	Maximum current : 100%	—	3	—	—
Minimum CLK pulse width		t_{CLKH}		2.3	—	—	μs
		t_{CLKL}					
Output residual voltage		V_{OL} DOWN	I_{OL} = 1 mA	—	—	0.5	V
		V_{OL} ALERT					
TSD operation temperature(Note)		TSD	(Design target value)	—	170	—	°C
TSD hysteresis (Note)		TSDhys	(Design target value)	—	40	—	°C
Oscillation frequency		fosc1	using built-in capacitor and resistor	50	100	200	kHz
Oscillation frequency		fosc2	R_{OSC} = 51kΩ	2.6	4.0	5.4	MHz
Oscillation circuit for CLK monitor	Detection CLK frequency	fdetect	using built-in capacitor and resistor	1.0	2.0	4.0	Hz

Note: Pre-shipment testing is not performed.

Output Block

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Output ON resistor		$Ron_H + Ron_L$	I_{OUT} = 4 A	—	0.4	0.6	Ω
Output transistor switching characteristics		t_r	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF	—	1.5	—	μs
		t_f		—	0.5	—	
Output leakage current	Upper side	I_{LH}	V_M = 50 V	—	—	5	μA
	Lower side	I_{LL}		—	—	5	

Description of Functions

1. Excitation Settings

The excitation mode can be selected from the following eight modes using the M1, M2 and M3 inputs. (The default is 1/2 excitation using the internal pull-down.)

Please be sure to set up 'Low' or 'High' always at M1, M2 and M3 terminals.

Although M1、M2 and M3 terminals have built-in pull-down resistors, please do not keep M1、M2 and M3 terminals open. New excitation mode starts from the initial mode when M1, M2, or M3 inputs are shifted during motor operation. (Specifications of the TB6564HQ are the same as the TB6564AHQ about it.)

Input			Mode (Excitation)
M1	M2	M3	
L	L	L	1/2
L	L	H	1/8
L	H	L	1/10
L	H	H	1/16
H	L	L	1/20
H	L	H	1/32
H	H	L	1/40
H	H	H	1/64

2. Function

When the ENABLE signal goes Low level, it sets an OFF on the output. The output changes to the Initial mode shown in the table below when the RESET signal goes Low level. In this mode, the status of the CLK and CW/CCW pins are irrelevant.

Input				Output Mode
CLK	CW/CCW	RESET	ENABLE	
↑	L	H	H	CW
↑	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't care

3. Initial Mode

When RESET is used, the phase currents are as follows.

Excitation Mode	A Phase Current	B Phase Current
1/2 step	100%	0%
1/8 step	100%	0%
1/10 step	100%	0%
1/16 step	100%	0%
1/20 step	100%	0%
1/32 step	100%	0%
1/40 step	100%	0%
1/64 step	100%	0%

4. 100% current Settings (Current Value)

100% current value is determined by Vref inputted from external part and the external resistance for detecting output current.
Vref is doubled 1/3 inside IC, and compared with VRS.

Io(100%) = Vref x 1/3 x 1/Rs

The average current is lower than the calculated value because this IC has the method of peak current detection.

5. OSC1 and OSC2

(1)OSC1 :

Triangle wave is generated internally by CR oscillation with the capacitor and the resistor in the IC.

fosc1 = 100 kHz

(2)OSC2 :

Triangle wave is generated internally by CR oscillation by connecting external resistor to OSC2 terminal.

Rosc2: 24kΩ ≦ Rosc2 ≦ 180kΩ

Relation of external resistor and frequency (fchop) is as follows;
Values of the table below are design target values.

Rosc2(kΩ)	fchop(kHz)
180	15
51	40
24	65

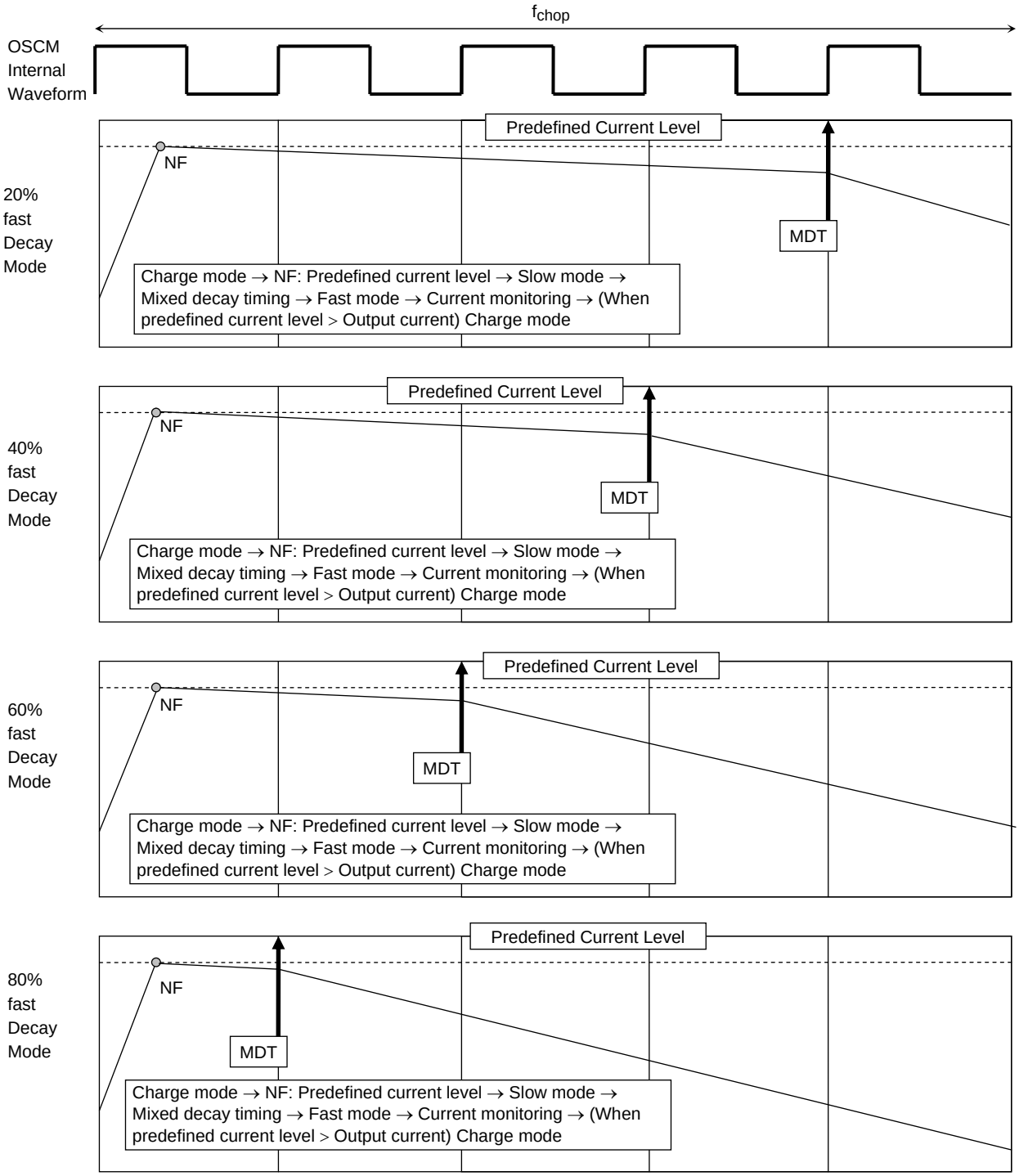
6. Decay Mode Settings

It takes approximately five OSC cycles for discharging a current in PWM mode. The 20% fast decay mode is created by inducing decay during the last cycle in Fast Decay mode; the 40% fast Decay mode is created by inducing decay during the last two cycles in Fast Decay mode; the 60% fast Decay mode is created by inducing decay during the last three cycles in Fast Decay mode; the 80% fast Decay mode is created by inducing decay during the last four cycles in Fast Decay mode.
Since the DCY1 and DCY2 pins have internal pull-down resistors, the 20% fast decay mode is selected when DCY1 and DCY2 are undriven.

Dcy2	Dcy1	Current Decay Setting
L	L	20% Fast Decay
L	H	40% Fast Decay
H	L	60% Fast Decay
H	H	80% Fast Decay

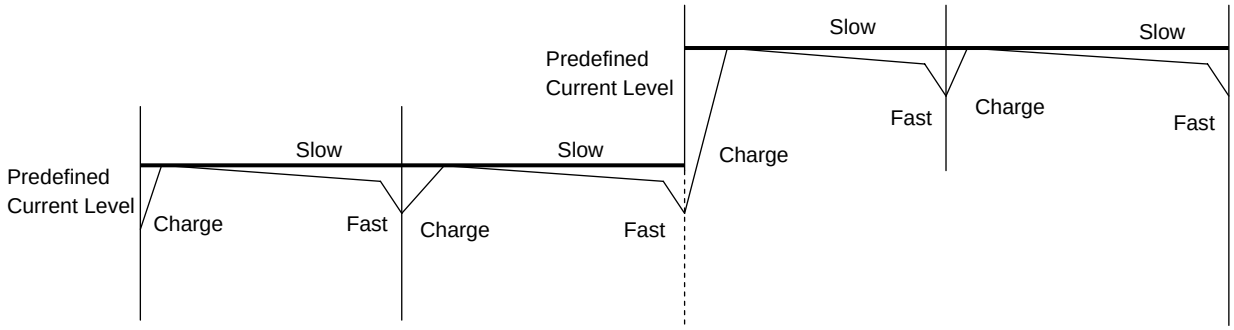
7. Current Waveforms and Mixed Decay Mode Settings

The period of PWM operation is equal to five periods of OSCM. OSCM is equal to 1/20 of OSC2. The current decay rate of the Decay mode operation can be determined by the DCY1 and DCY2 inputs for constant-current control.
The "NF" refers to the point at which the output current reaches its predefined current level.
The smaller the MDT value, the smaller the current ripple amplitude. However, the current decay rate decreases.

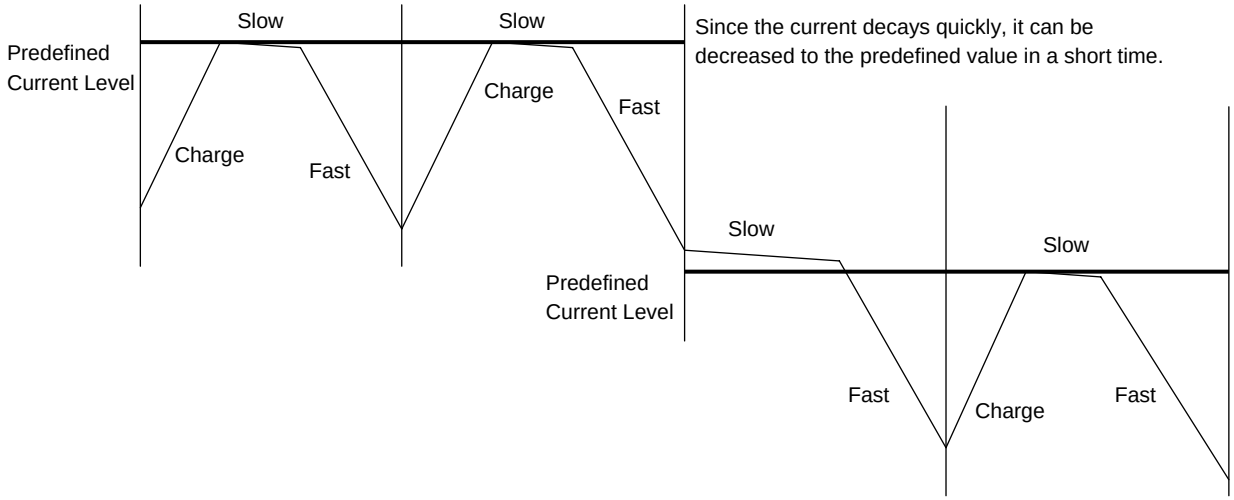


8. Current Control Modes (Effects of Decay Modes)

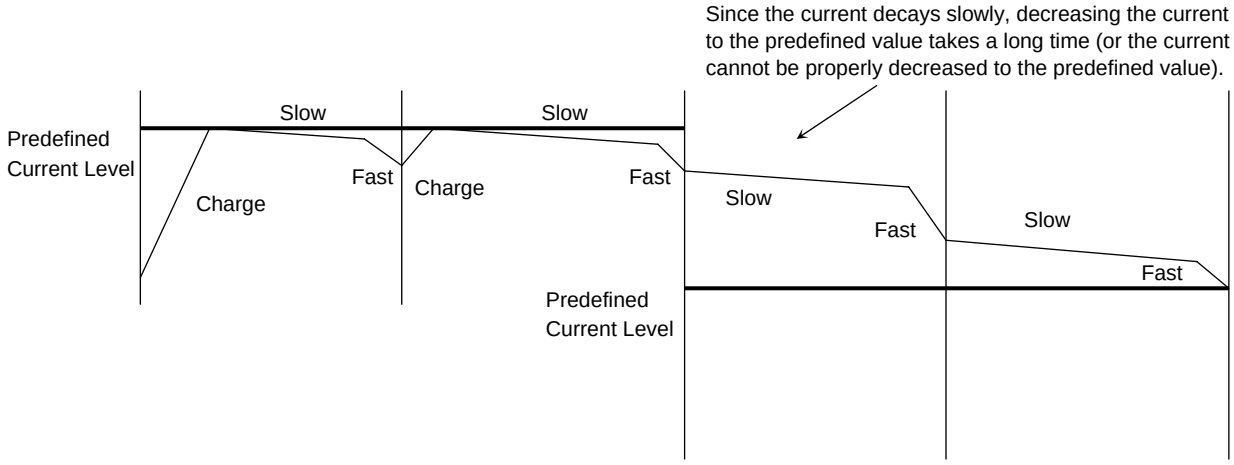
- Increasing the current (sine wave)



- Decreasing the current with a high decay rate (The current decay rate in Mixed Decay mode is the ratio between the time in Fast-Decay mode (discharge time after MDT) and the remainder of the period.)



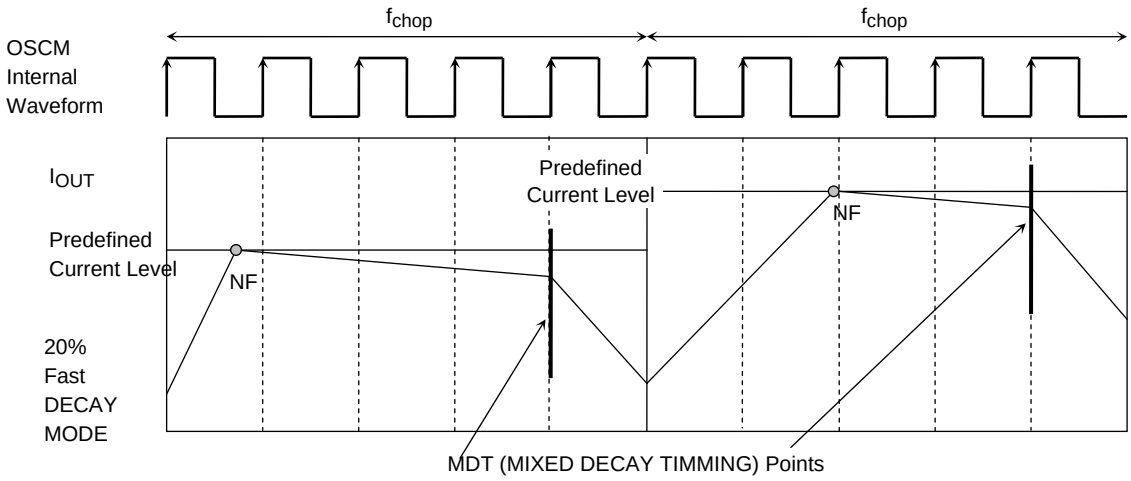
- Decreasing the current with a low decay rate (The current decay rate in Mixed Decay mode is the ratio between the time in Fast-Decay mode (discharge time after MDT) and the remainder of the period.)



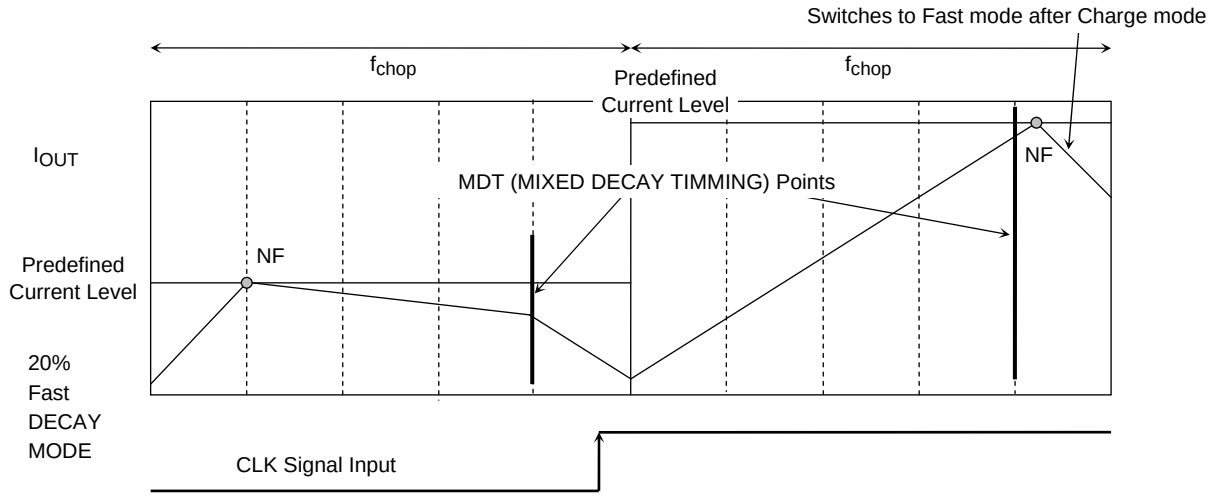
During Mixed Decay and Fast Decay modes, if the predefined current level is less than the output current at the RNF (current monitoring point), the Charge mode in the next chopping cycle will disappear (though the current control mode is briefly switched to Charge mode in actual operations for current sensing) and the current is controlled in Slow and Fast Decay modes (mode switching from Slow Decay mode to Fast Decay mode at the MDT point).

Note: The above figures are rough illustration of the output current. In actual current waveforms, transient response curves can be observed.

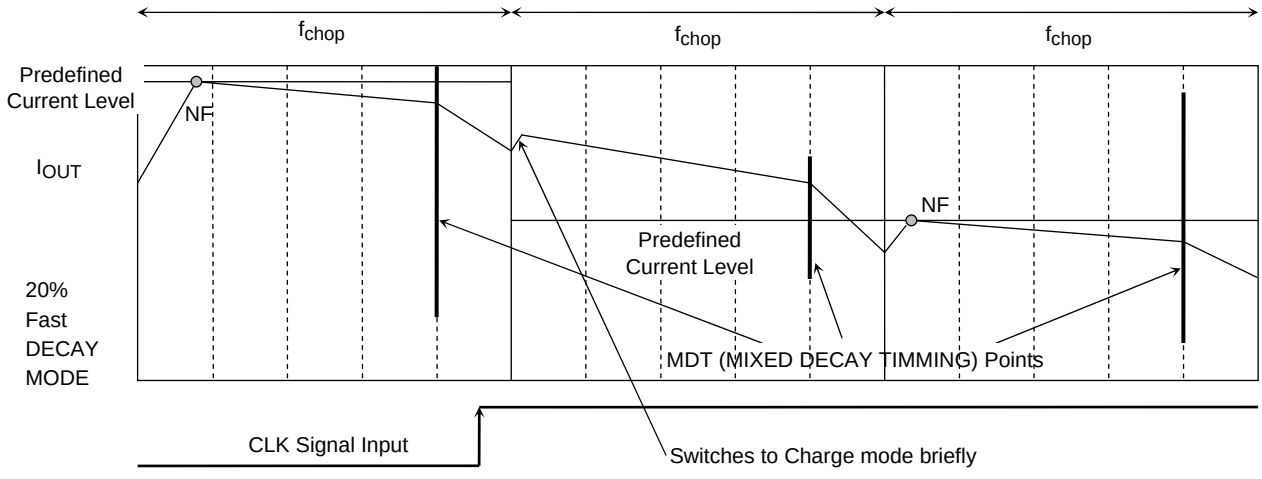
9. Current Waveforms in Mixed Decay Mode



- When the NF points come after Mixed Decay Timing points



- When the output current value > predefined current level in Mixed Decay mode

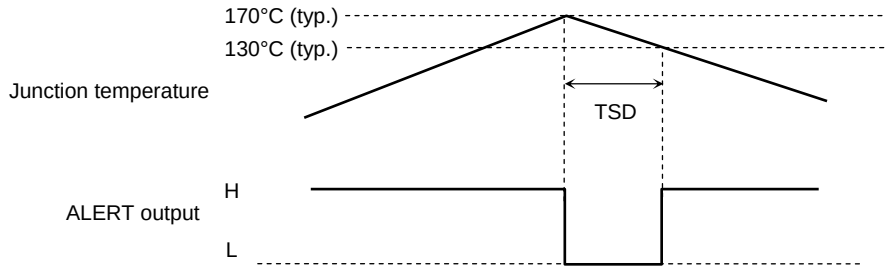


*: Even if the output current rises above the predefined current at the RNF point, the current control mode is briefly switched to Charge mode for current sensing.

13.Thermal Shut-Down circuit

The IC incorporates a thermal shutdown circuit. When the junction temperature (T_j) reaches 170°C (typ.), the output power MOSFETs are turned off.
The output power MOSFETs are turned on automatically.
The IC has 40°C of temperature hysteresis.

TSD = 170°C (target spec) (Note)
ΔTSD = 40°C (target spec) (Note)

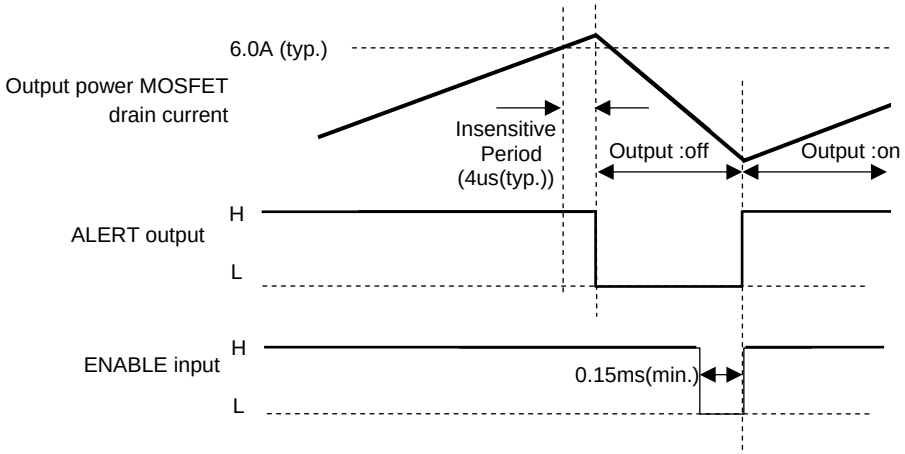


Note: Pre-shipment testing is not performed.

14. ISD (Over current detection)

Current that flow through output power MOSFETs are monitored individually. If over-current is detected in at least one of all output power MOSFETs, all output power MOSFETs are turned off then this status is kept until ENABLE signal is input. Target value in design is 6A and dispersion of ±1.5A should be considered.

ISD = 6A (typ.) ±1.5A (Note)



Note: Pre-shipment testing is not performed.

15. Low voltage detection (UVLO) circuit

（1）V_{DD} :

Outputs are shutoff by operating at 3.9V (Typ.) of V_{DD} or less.
It has a hysteresis of 0.1V(Typ.) and recover to output when V_{DD} reaches 4.0V(Typ.).

（2）V_M :

Outputs are shutoff by operating at 3.9V (Typ.) of V_M or less.
It has a hysteresis of 0.1V(Typ.) and recover to output when V_{DD} reaches 4.0V(Typ.).

・The state of internal IC when the ULVO circuit is driving

The states of the internal IC, outputs, and the IC after recovery correspond to both the enable mode and the initial mode.

When VDD or VM falls to around 3.9V and UVLO operates, output turns off.
It recovers automatically from the initial state when both VDD and VM rise to around 4.0V or more.

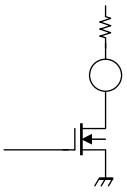
16. ALERT output

ALERT pin outputs the state of TSD and ISD. When TSD or ISD circuit is under detection, ALERT pin state changes from high impedance to low.

V_{ALERT} = 0.5V (max.) at 1mA

TSD	ISD	ALERT pin
Under TSD detection	Under TSD detection	Low
Normal	Under TSD detection	
Under TSD detection	Normal	
Normal	Normal	Z

Open-drain connection



17. DOWN

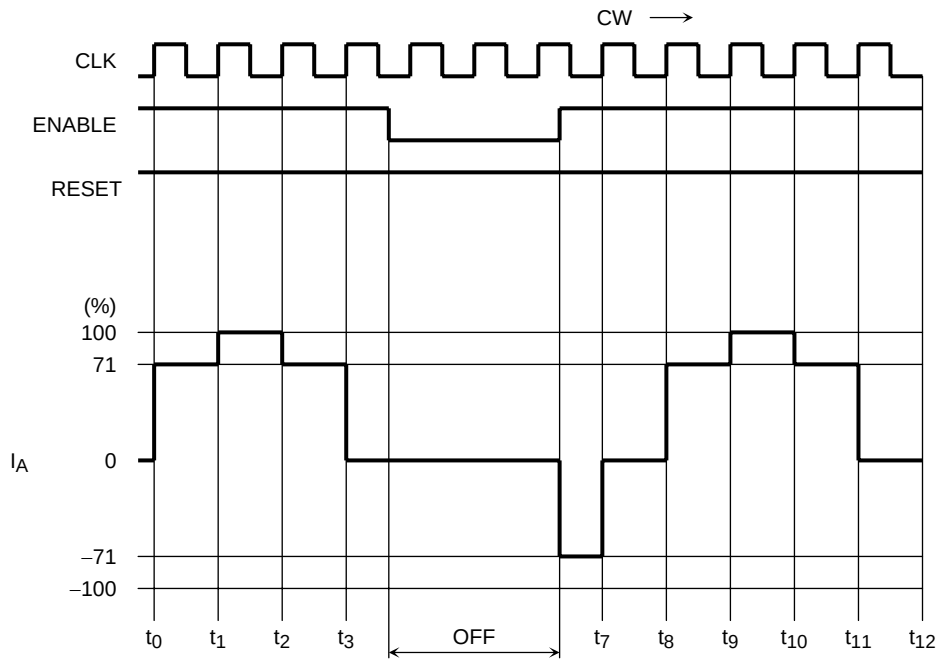
When IC detects CLK frequency less than 2.0Hz, output of DOWN pin turns to LOW.

Pin State	DOWN
Low	$f_{CLK} \leqq 2.0Hz$
Z	$f_{CLK} > 2.0Hz$

f_{detect} = 1.0Hz(min.) ～ 4.0Hz(max.)

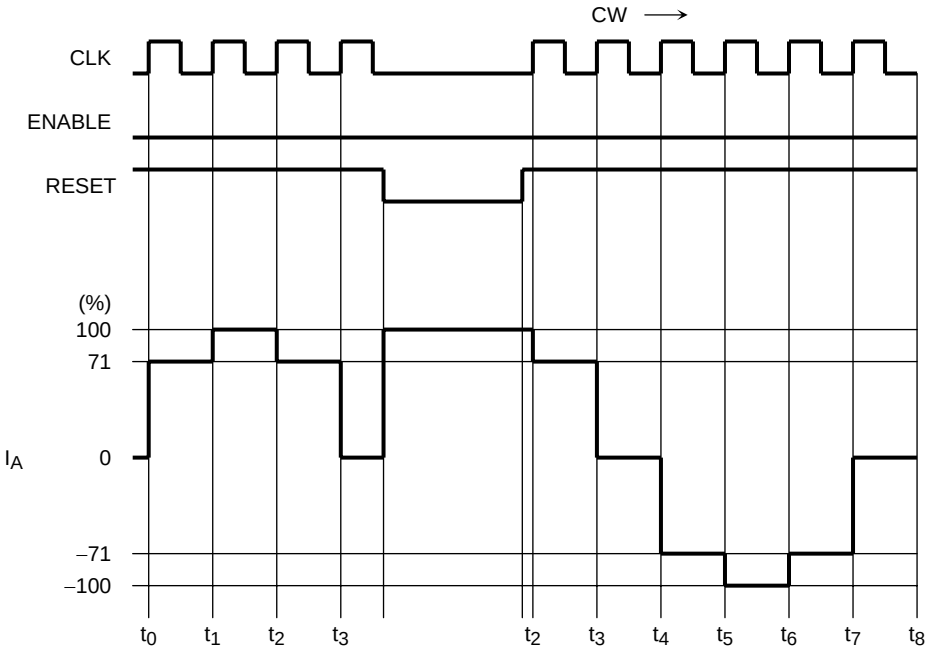
Relationship between Enable, RESET and Output (OUT)

Ex-1: ENABLE 1/2-step mode(M1: L, M2: L, M3: L)



The ENABLE signal at Low level disables only the output signals. Internal logic functions proceed in accordance with input clock signals and without regard to the ENABLE signal. Therefore output current is initiated by the timing of the internal logic circuit after release of disable mode.

Ex-2: RESET 1/2-step mode (M1: L, M2: L, M3: L)

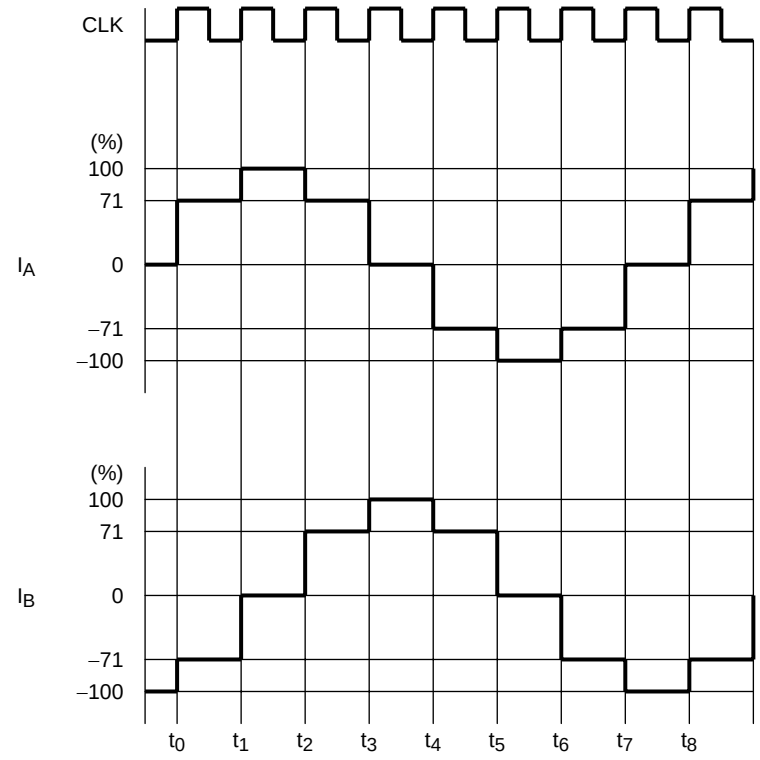


When the RESET signal goes Low level, output goes Initial state (Initial state: A Channel output current is 100%).

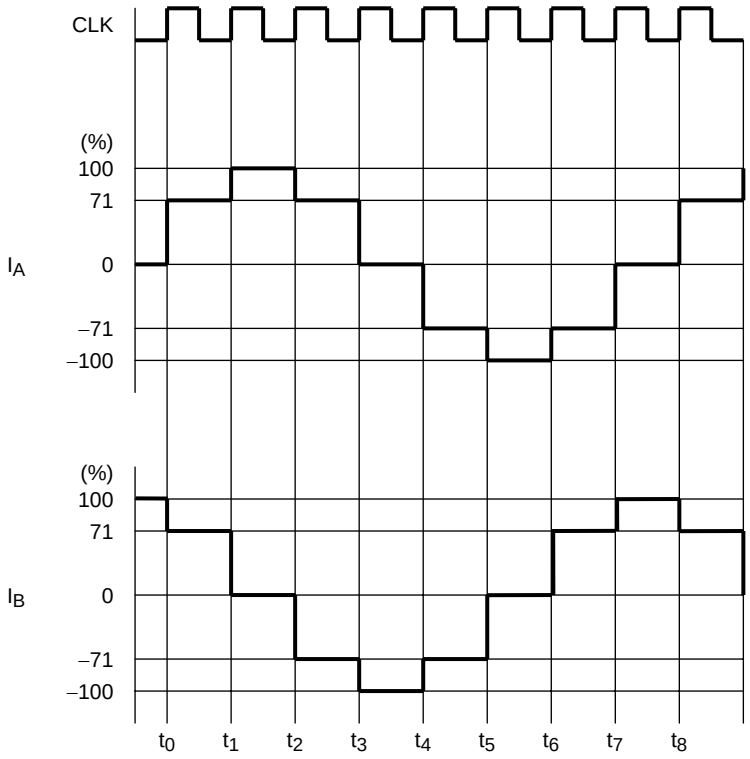
Once the RESET signal returns to High level, output continues from the next state after Initial from the next raise in the Clock signal.

Sequences of output waveform I_A/I_B at each excitation mode

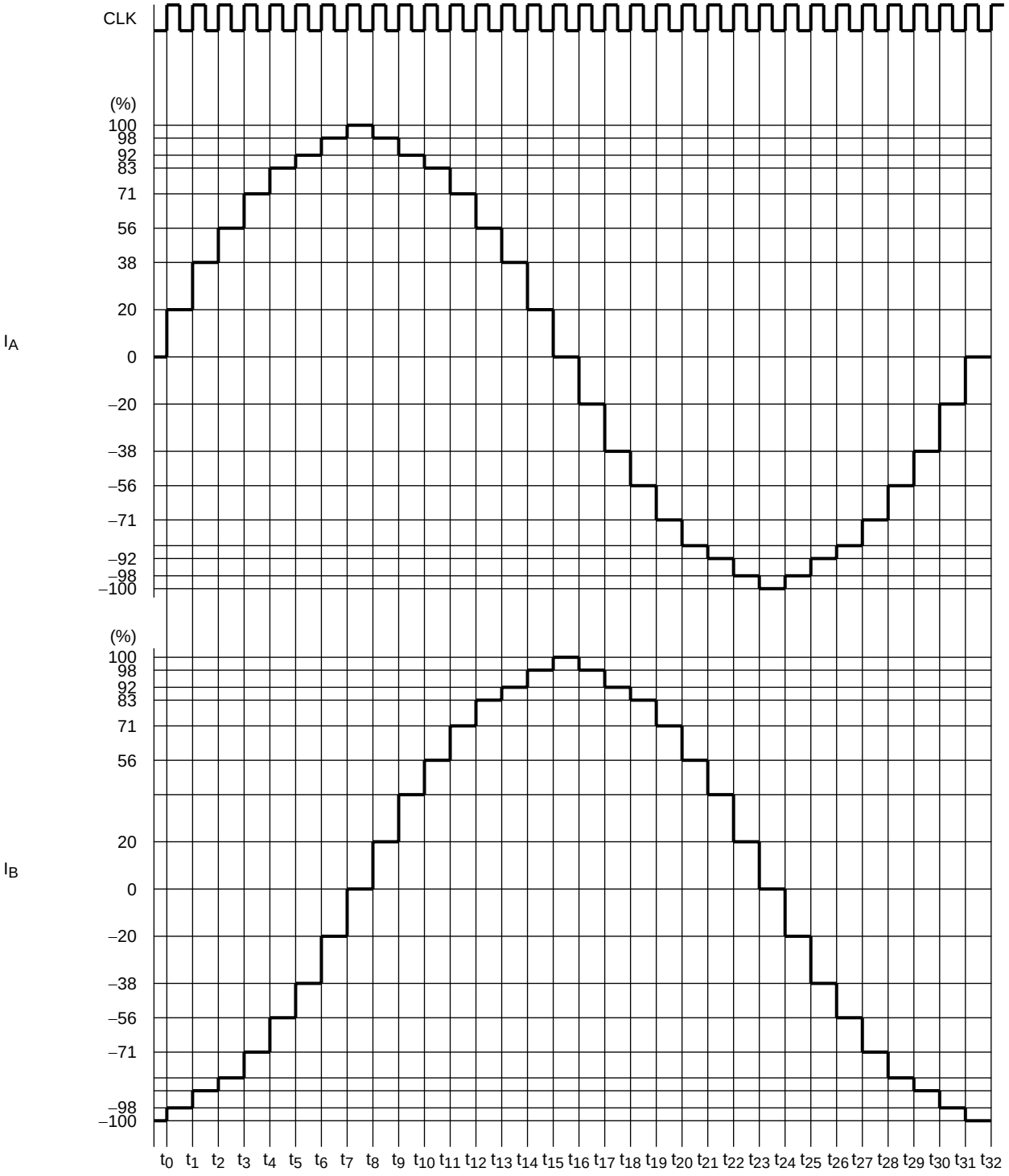
1/2-step Excitation Mode (M1: L, M2: L, M3: L, CW Mode)



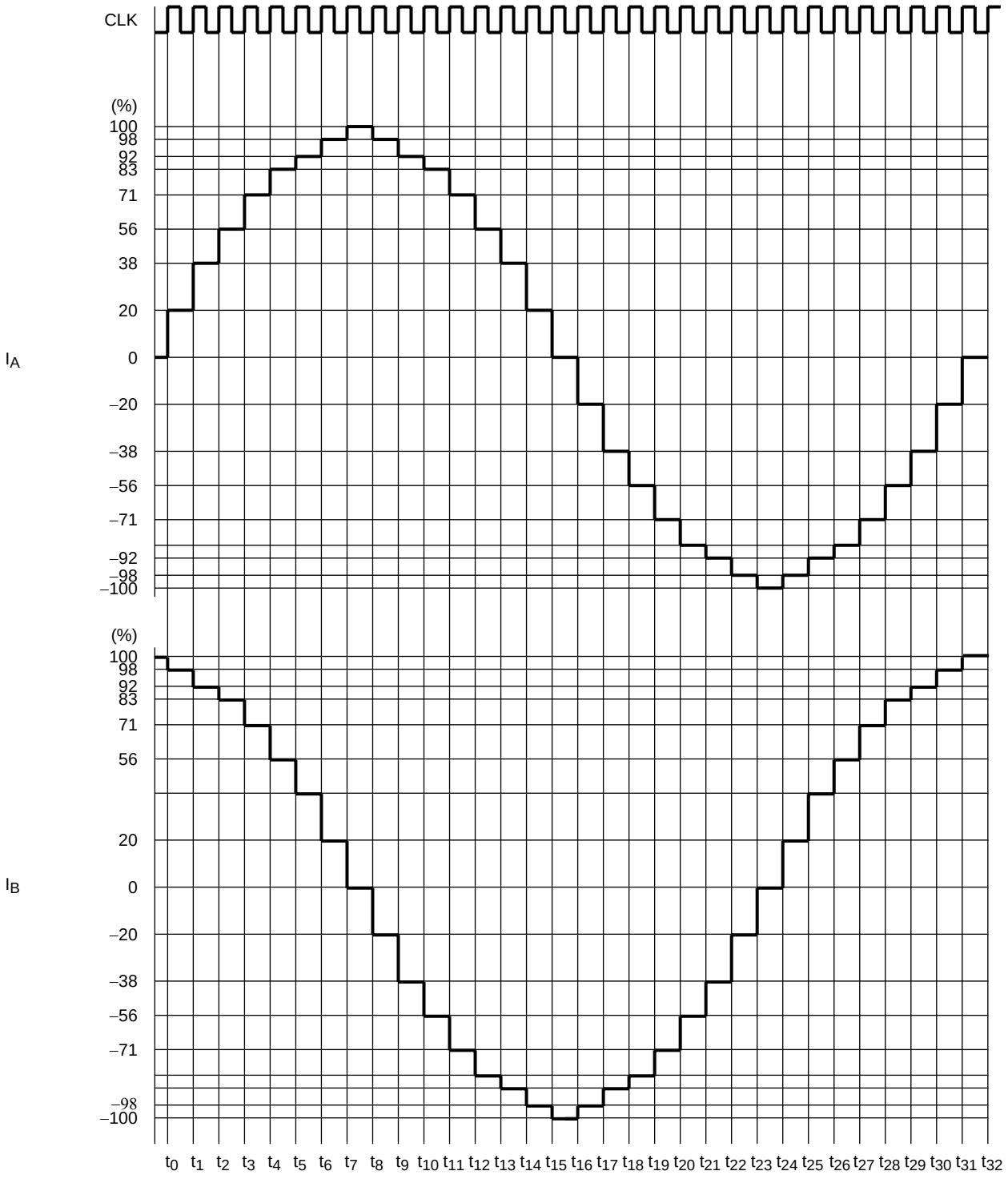
1/2-step Excitation Mode (M1: L, M2: L, M3: L, CCW Mode)



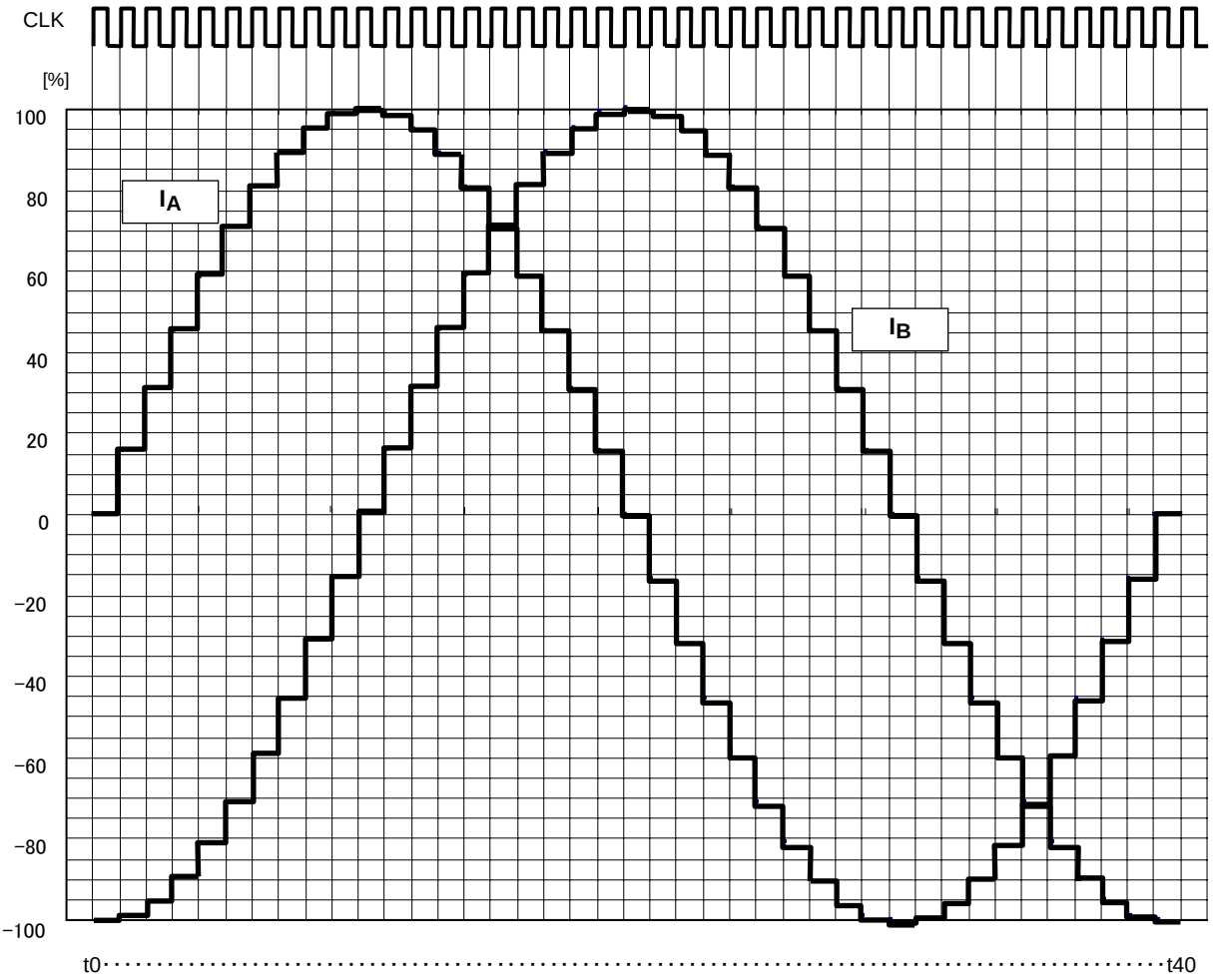
1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CW Mode)



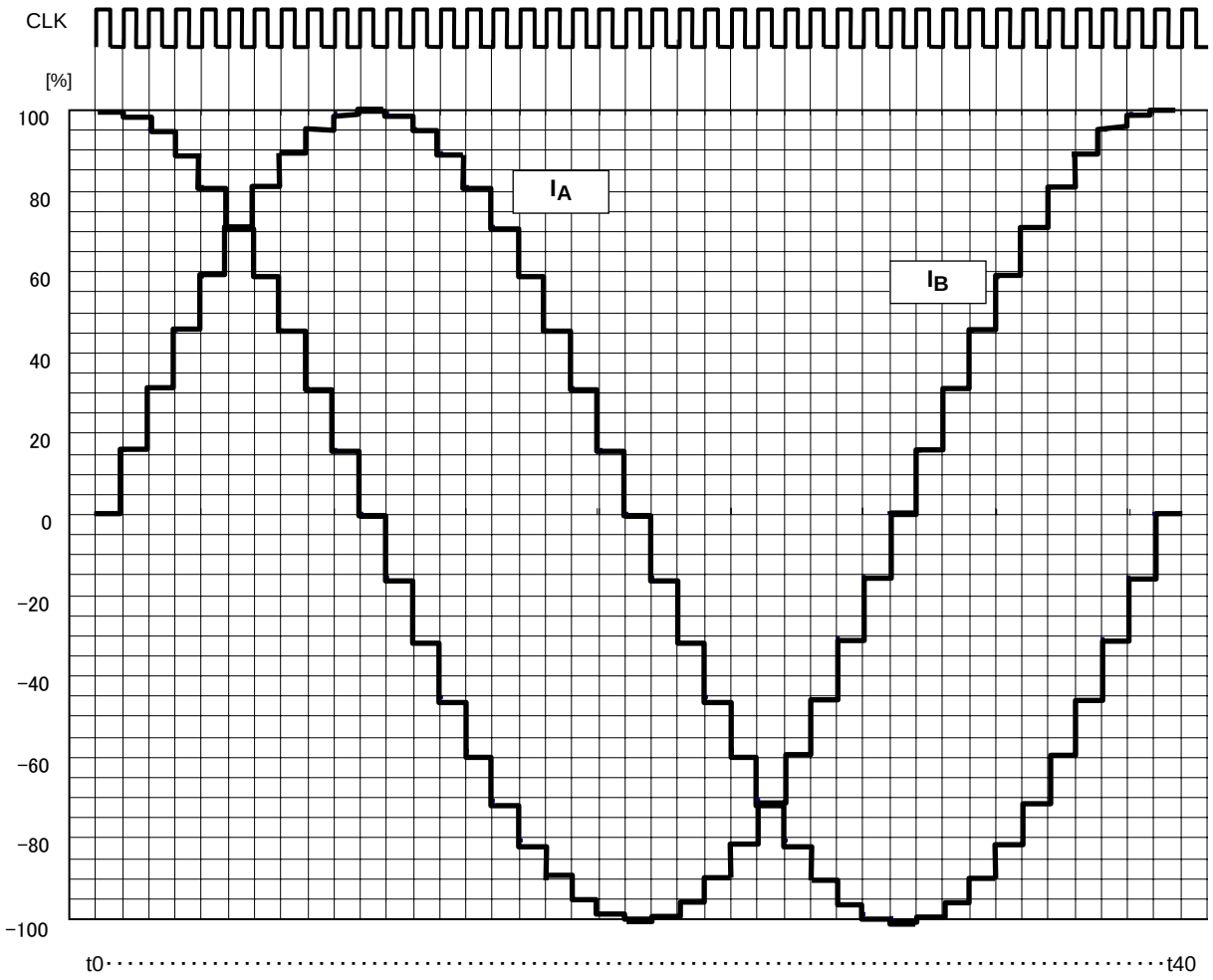
1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CCW Mode)



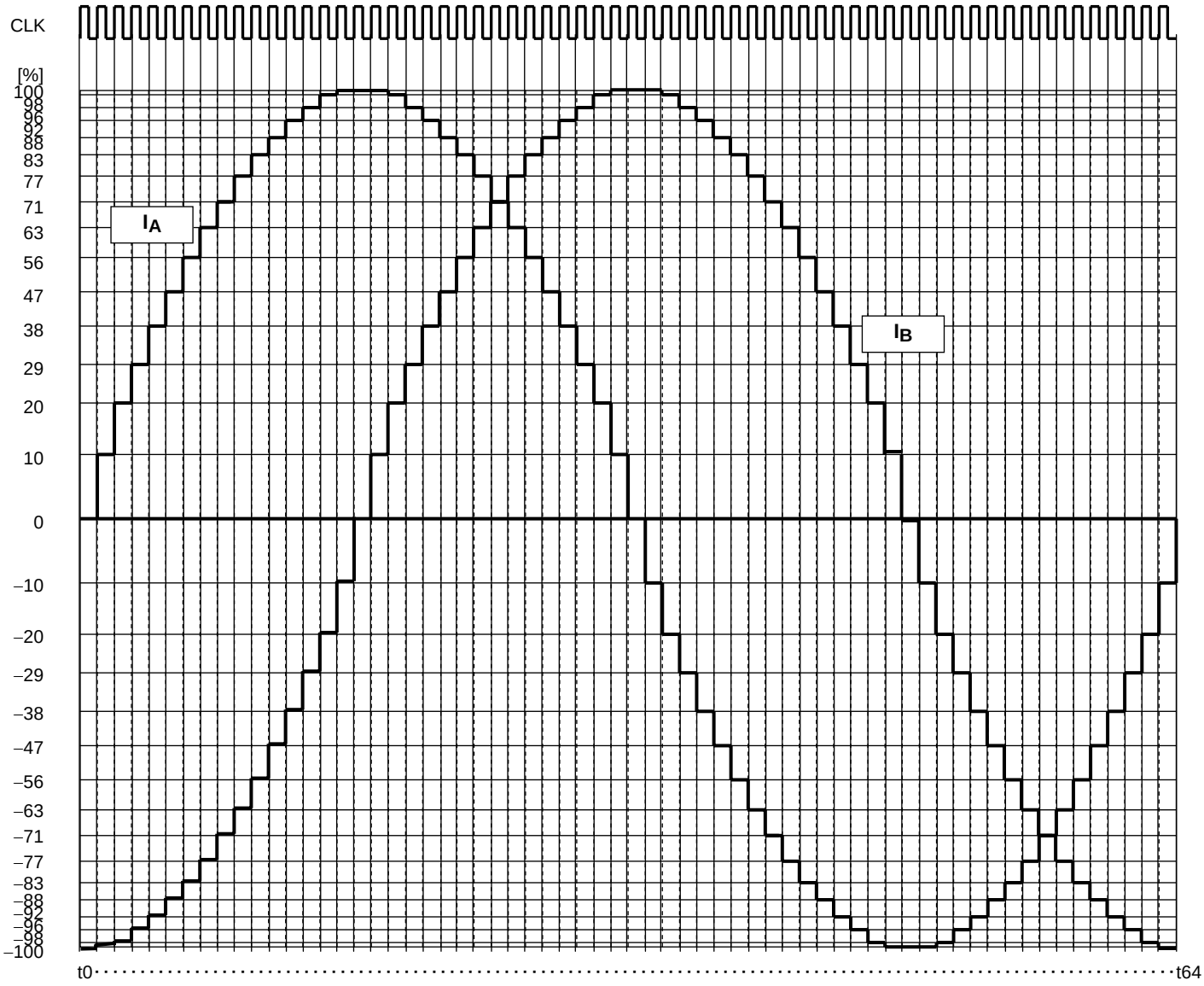
1/10-step Excitation Mode (M1: L, M2: H, M3: L, CW Mode)



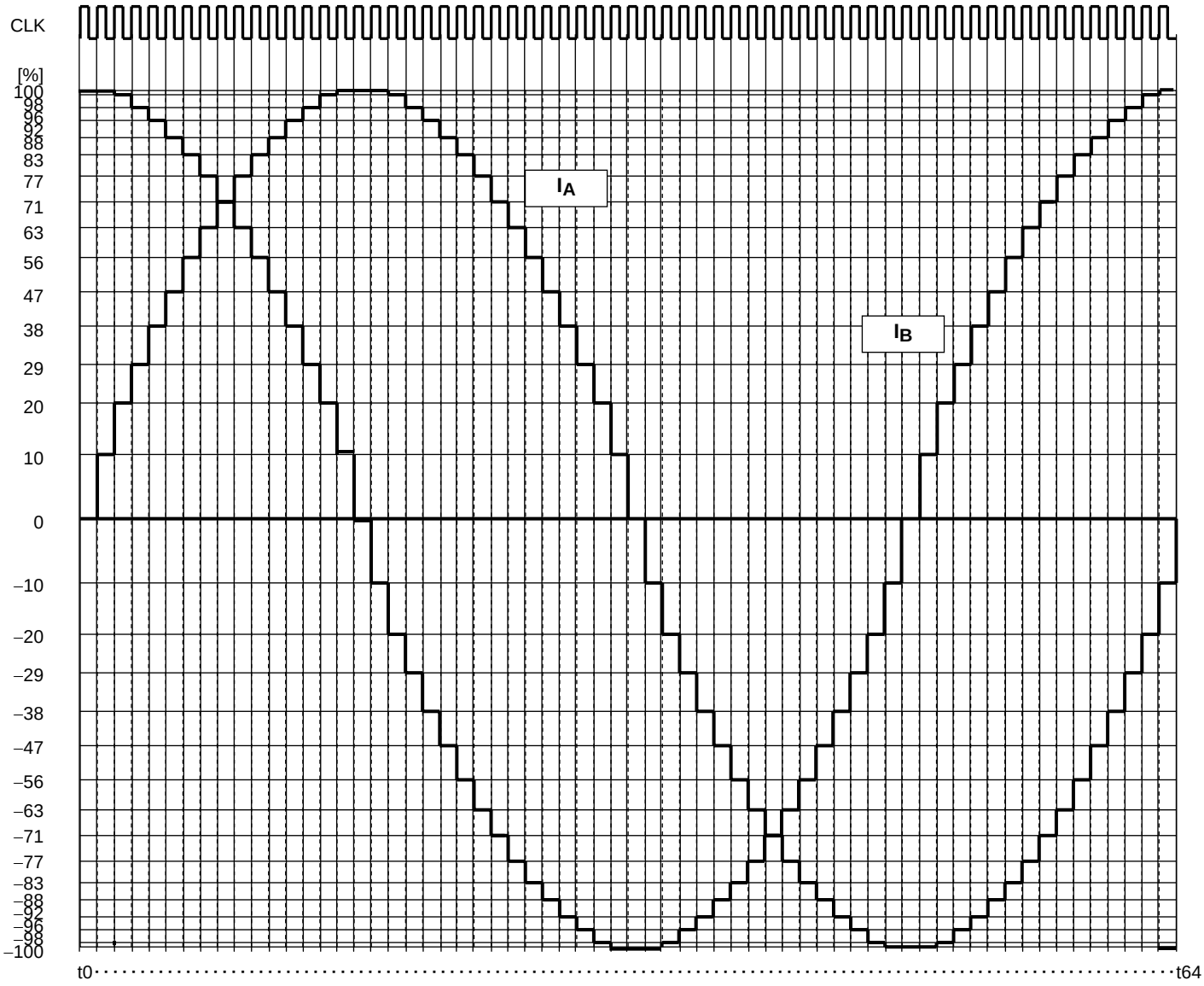
1/10-step Excitation Mode (M1: L, M2: H, M3: L, CCW Mode)



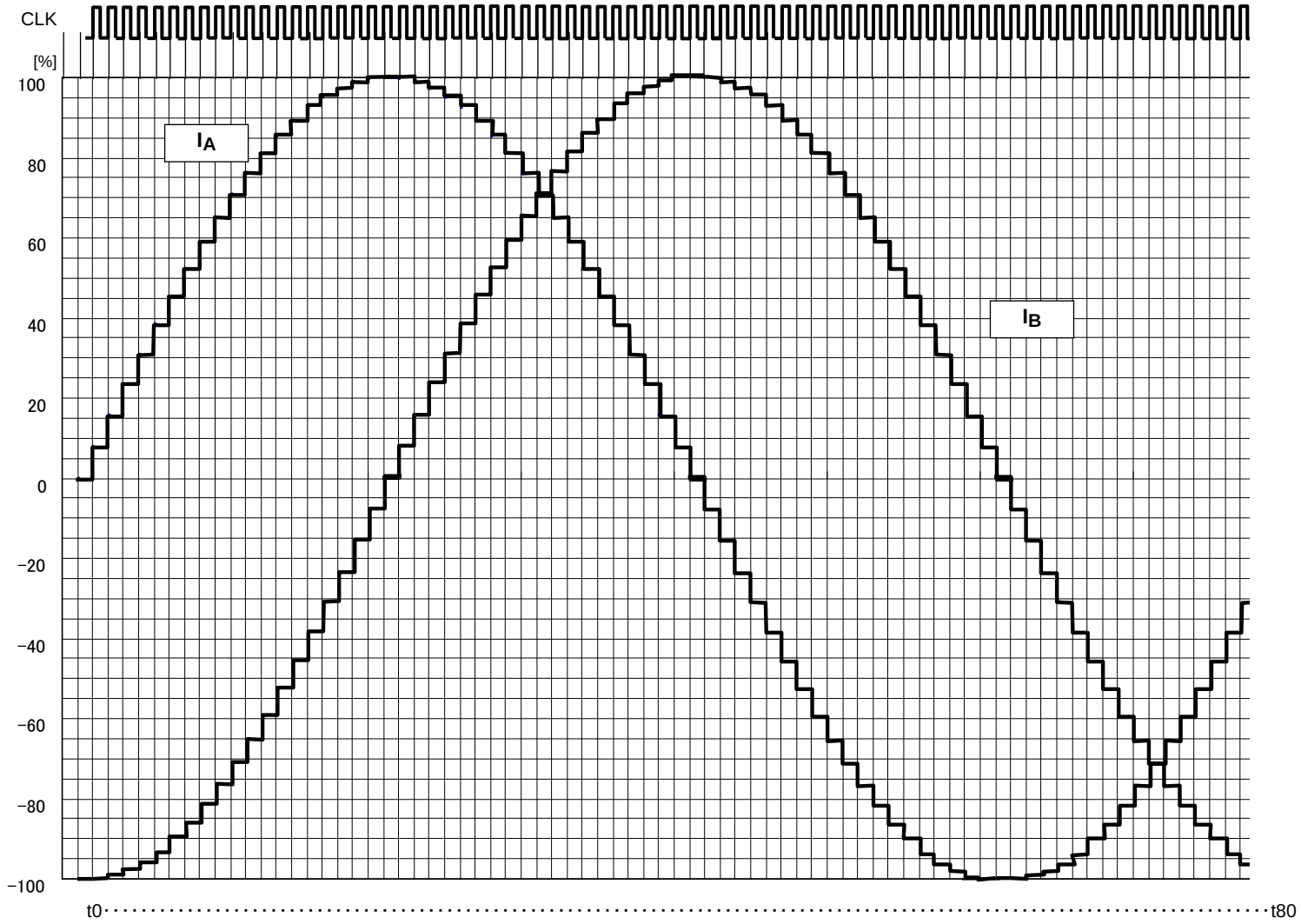
1/16-step Excitation Mode (M1: L, M2: H, M3: H, CW Mode)



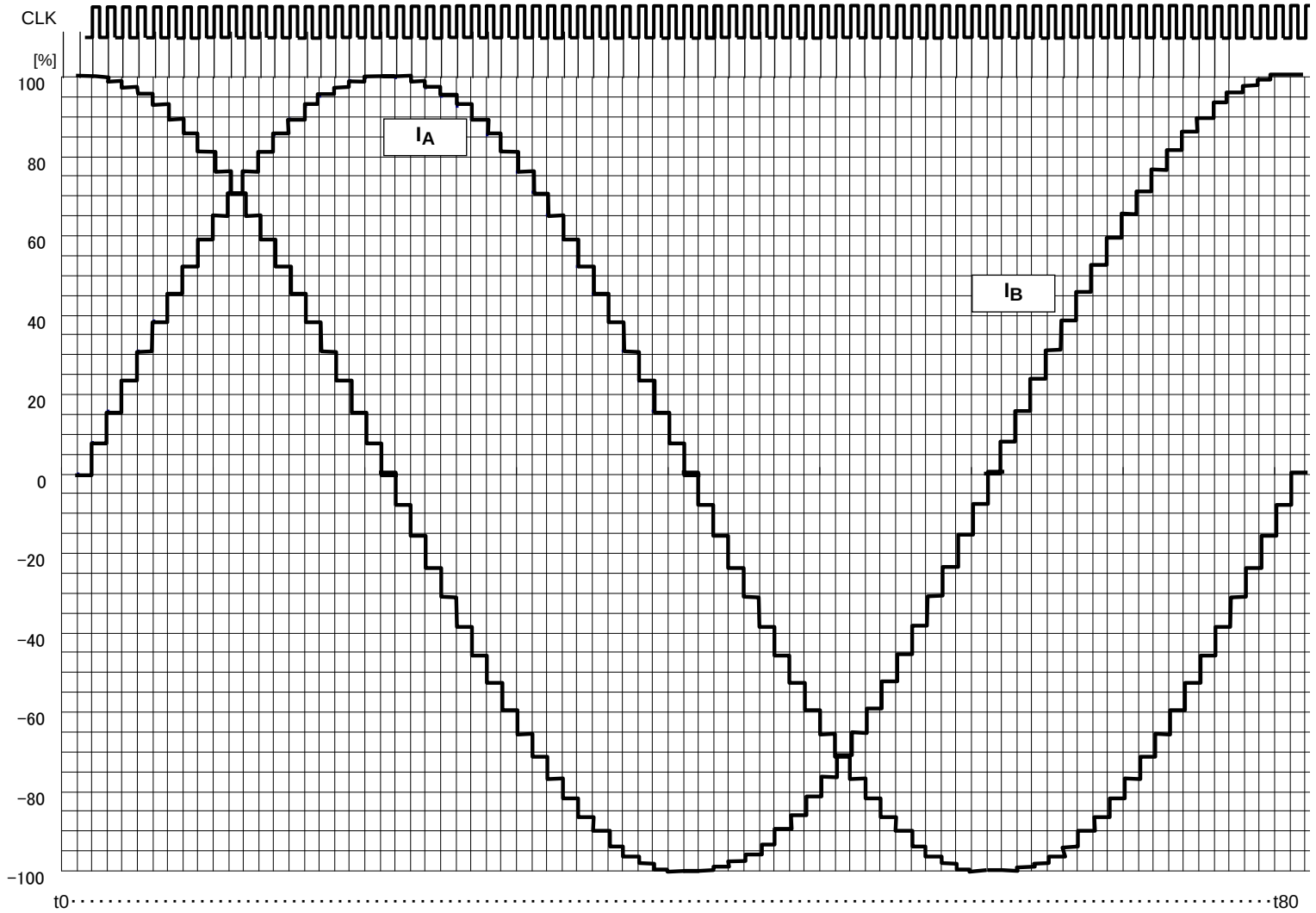
1/16-step Excitation Mode (M1: L, M2: H, M3: H, CCW Mode)



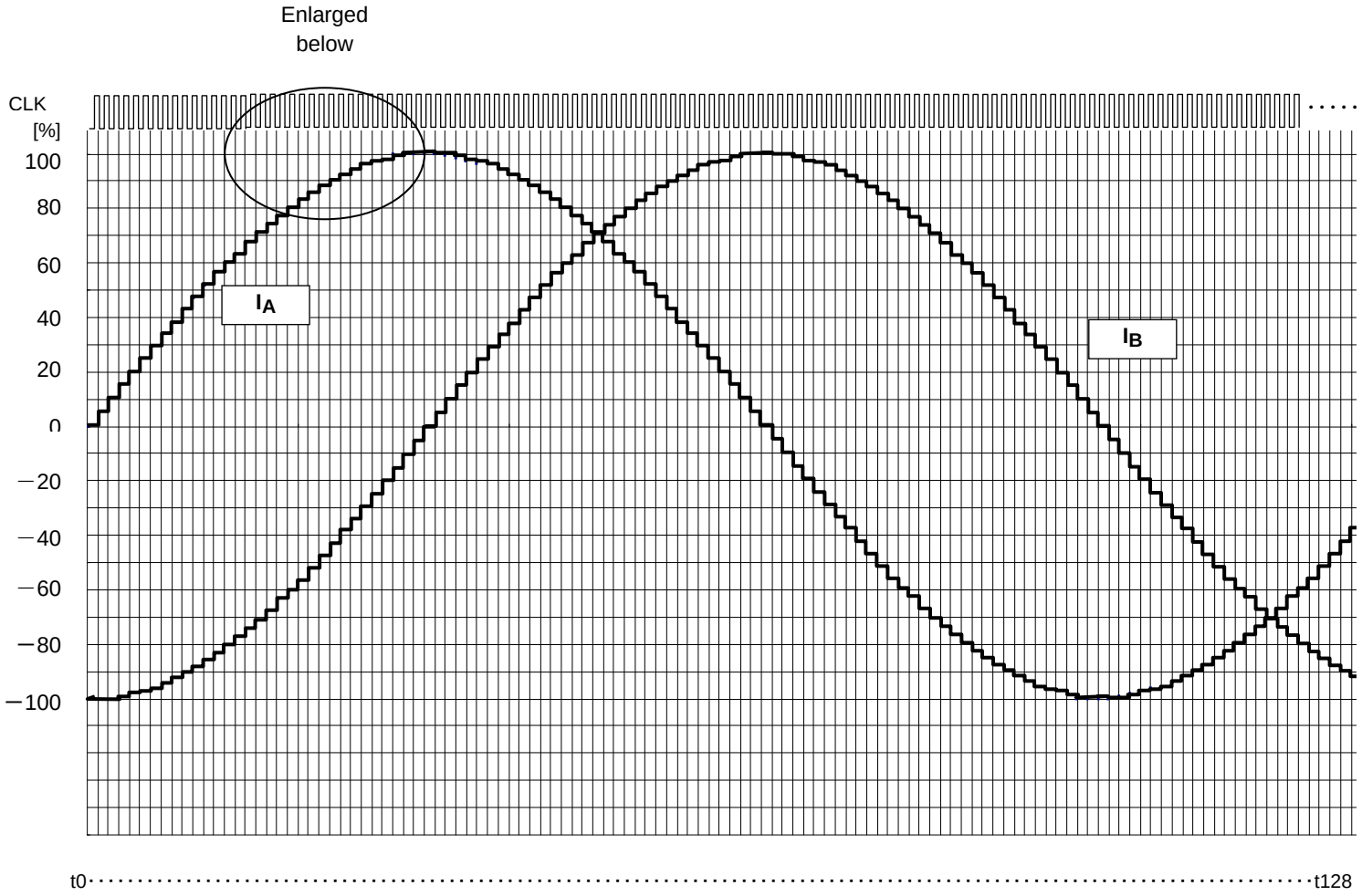
1/20-step Excitation Mode (M1: H, M2: L, M3: L, CW Mode)

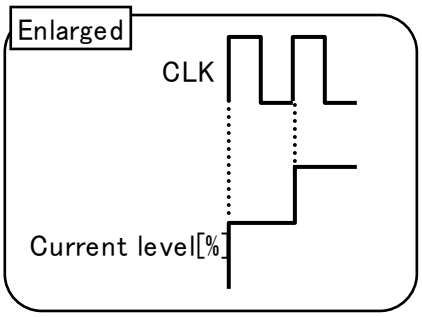


1/20-step Excitation Mode (M1: H, M2: L, M3: L, CCW Mode)

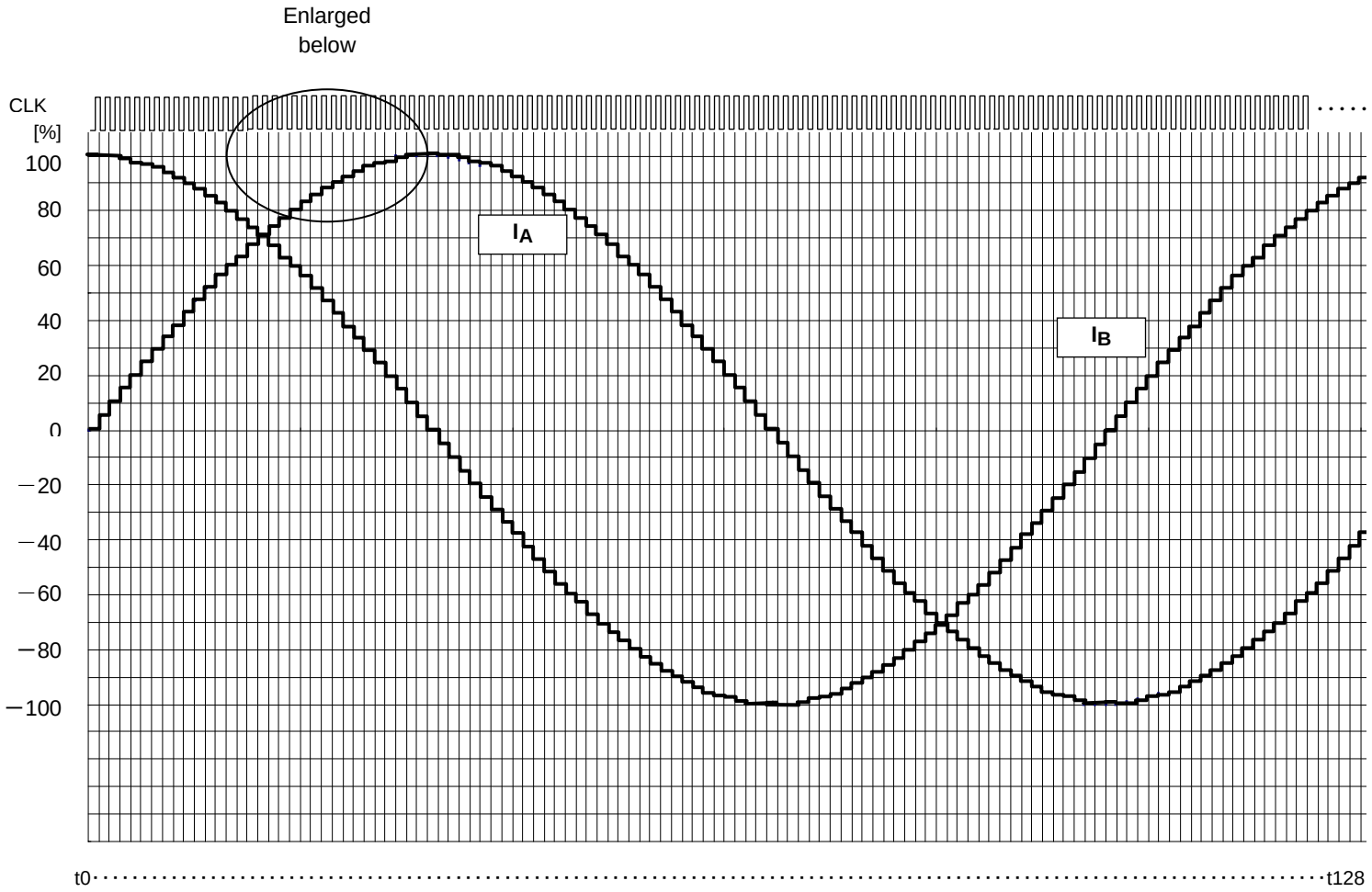


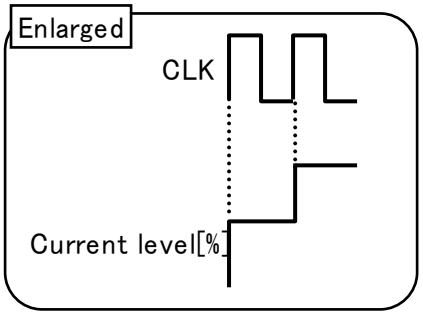
1/32-step Excitation Mode (M1: H, M2: L, M3: H, CW Mode)



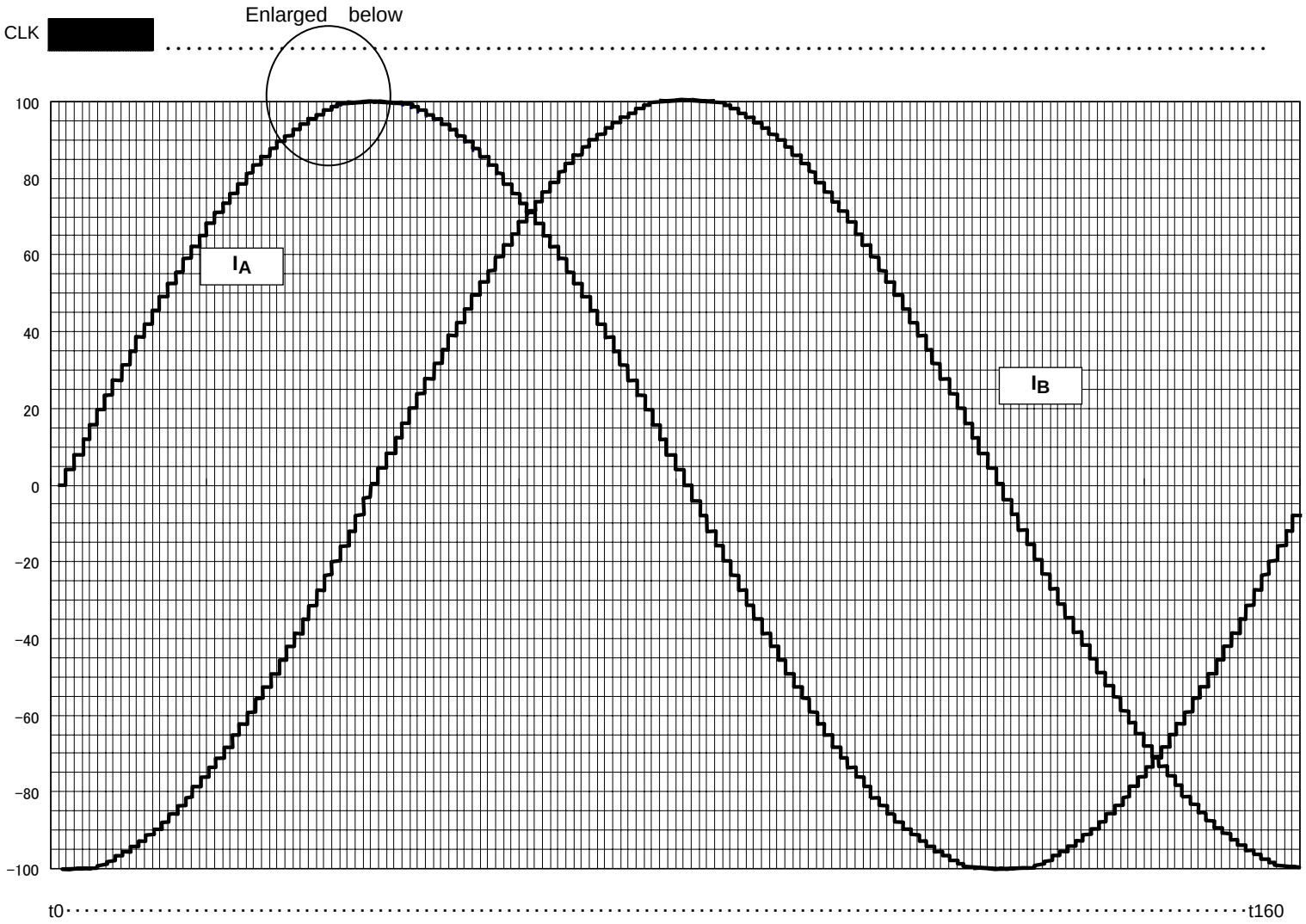


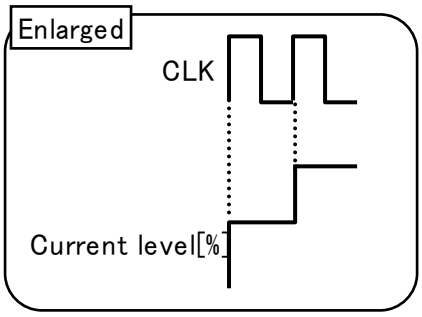
1/32-step Excitation Mode (M1: H, M2: L, M3: H, CCW Mode)



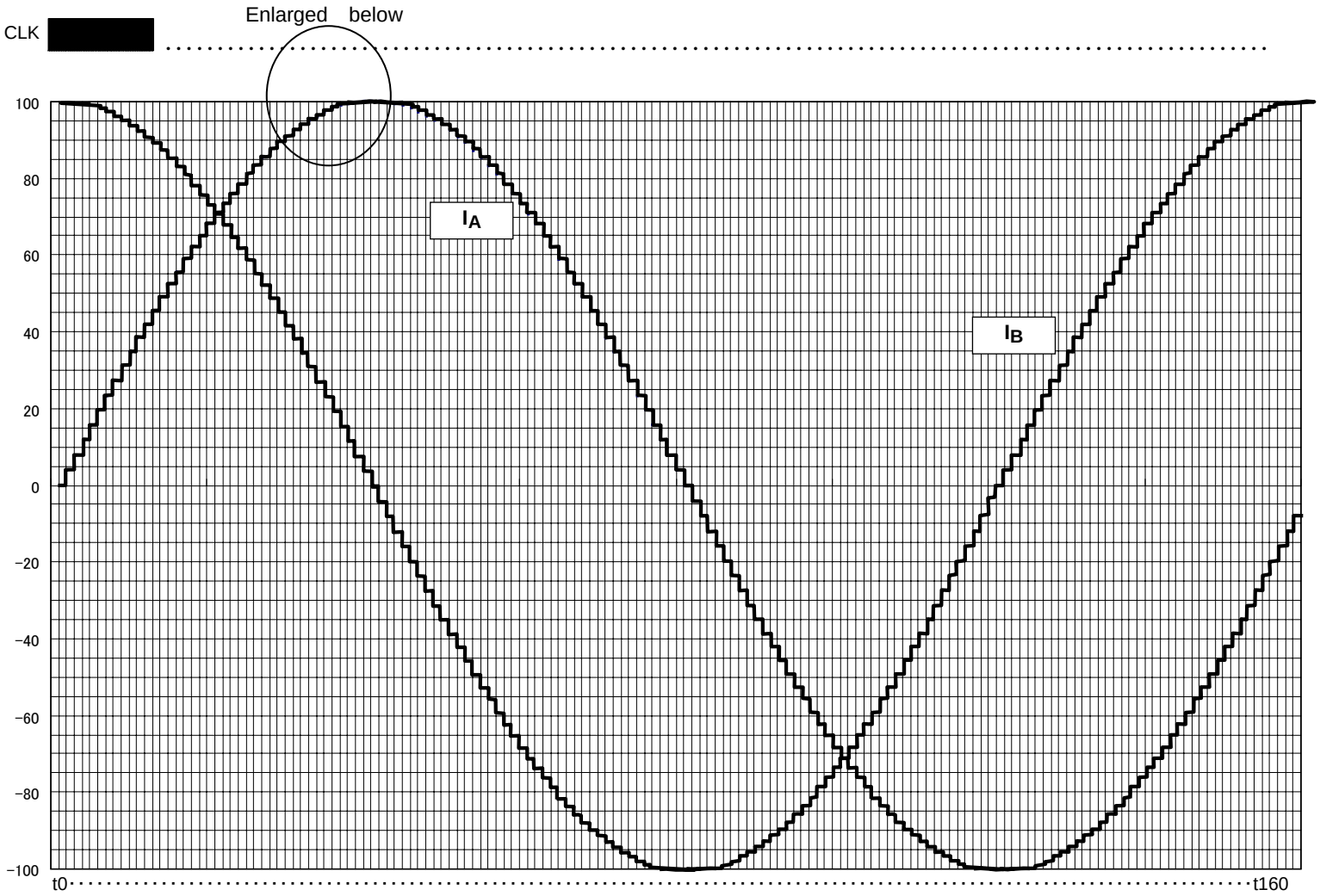


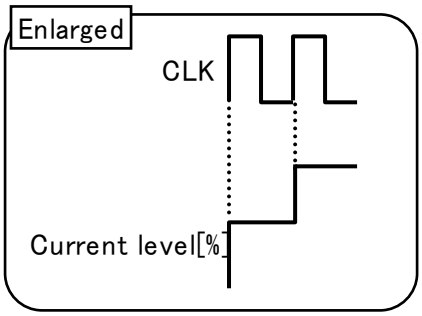
1/40-step Excitation Mode (M1: H, M2: H, M3: L, CW Mode)



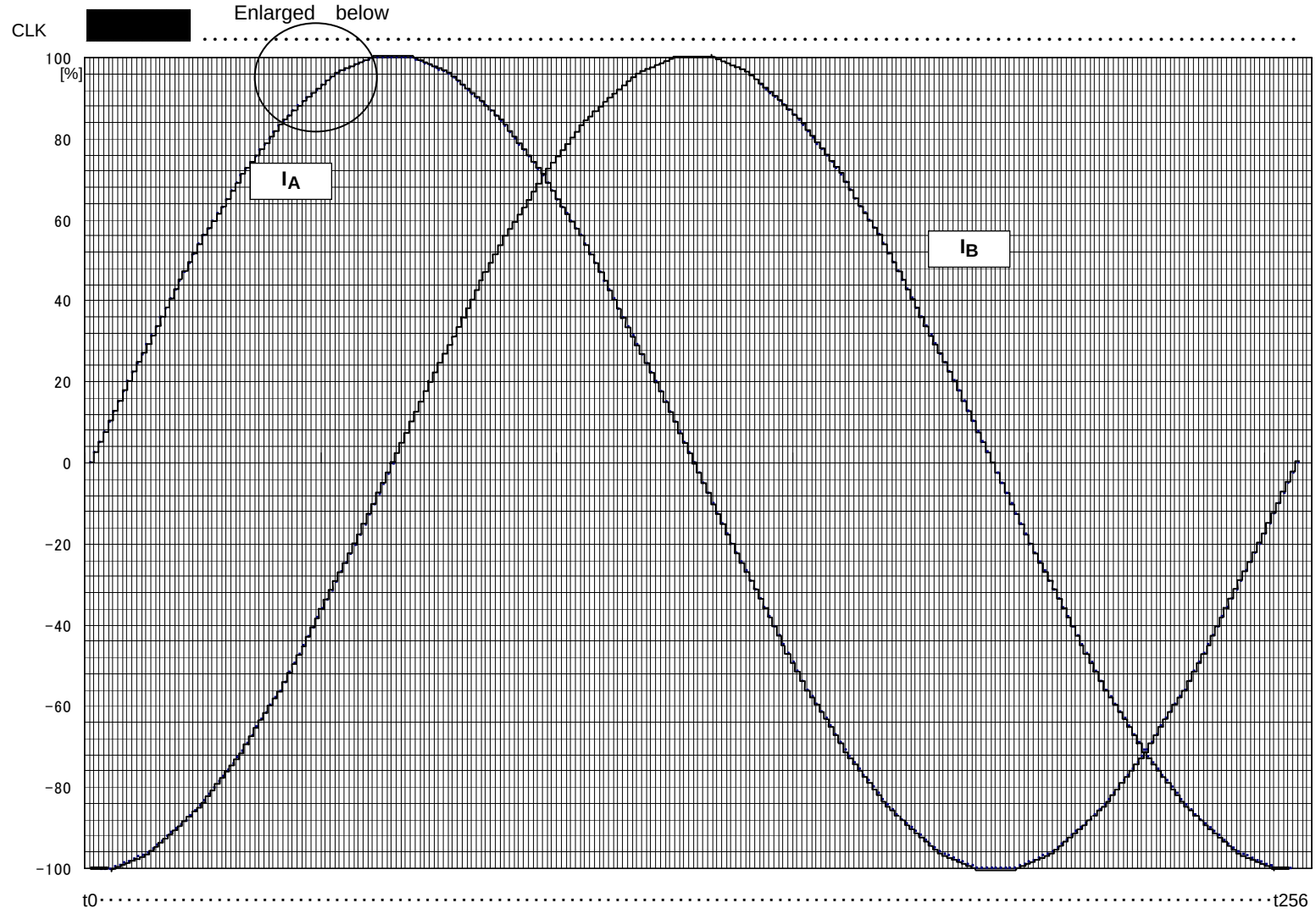


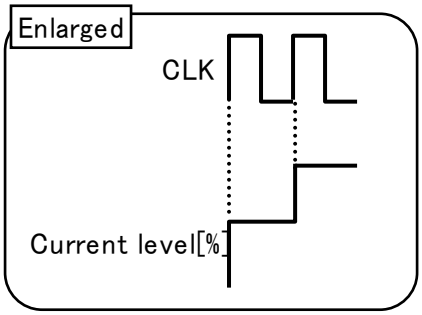
1/40-step Excitation Mode (M1: H, M2: H, M3: L, CCW Mode)



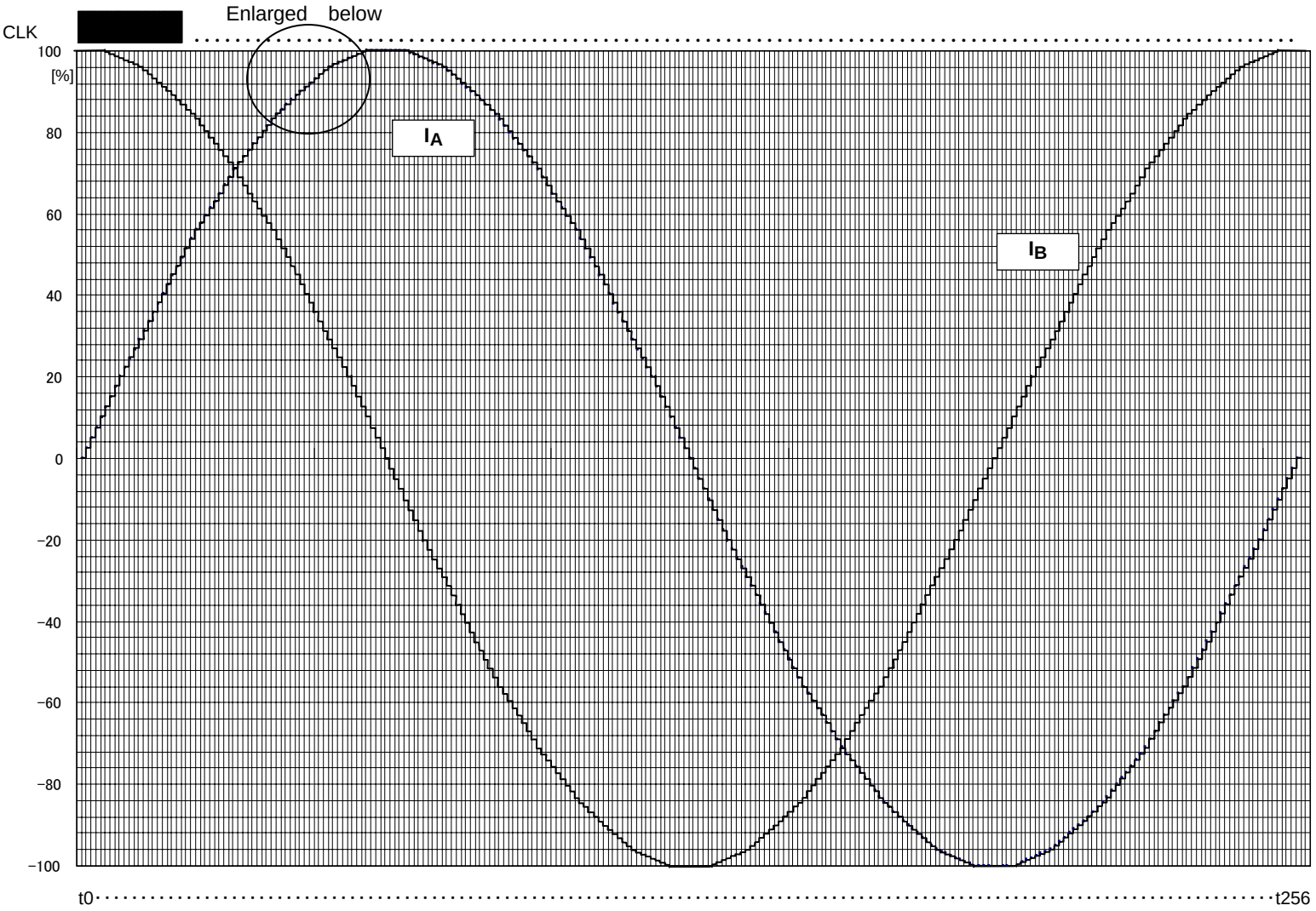


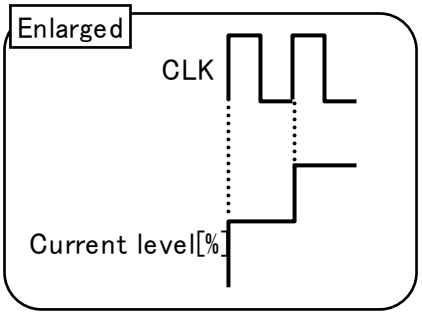
1/64-step Excitation Mode (M1: H, M2: H, M3: H, CW Mode)





1/64-step Excitation Mode (M1: H, M2: H, M3: H, CCW Mode)





Current level

Current level (1/64, 1/32, 1/16, 1/8, 1/2)

1/64, 1/32,1/16, 1/8,1/2	Min.	Typ.	Max.	Unit
θ 64	---	100.0	---	%
θ 63	96.0	100.0	100.0	
θ 62	95.9	99.9	100.0	
θ 61	95.7	99.7	100.0	
θ 60	95.5	99.5	100.0	
θ 59	95.2	99.2	100.0	
θ 58	94.9	98.9	100.0	
θ 57	94.5	98.5	100.0	
θ 56	94.1	98.1	100.0	
θ 55	93.6	97.6	100.0	
θ 54	93.0	97.0	100.0	
θ 53	92.4	96.4	100.0	
θ 52	91.7	95.7	99.7	
θ 51	91.0	95.0	99.0	
θ 50	90.2	94.2	98.2	
θ 49	89.3	93.3	97.3	
θ 48	88.4	92.4	96.4	
θ 47	87.4	91.4	95.4	
θ 46	86.4	90.4	94.4	
θ 45	85.3	89.3	93.3	
θ 44	84.2	88.2	92.2	
θ 43	83.0	87.0	91.0	
θ 42	81.8	85.8	89.8	
θ 41	80.5	84.5	88.5	
θ 40	79.1	83.1	87.1	
θ 39	77.8	81.8	85.8	
θ 38	76.3	80.3	84.3	
θ 37	74.8	78.8	82.8	
θ 36	73.3	77.3	81.3	
θ 35	71.7	75.7	79.7	
θ 34	70.1	74.1	78.1	
θ 33	68.4	72.4	76.4	

1/64, 1/32,1/16, 1/8,1/2	Min.	Typ.	Max.	Unit
θ 32	66.7	70.7	74.7	%
θ 31	65.0	69.0	73.0	
θ 30	63.2	67.2	71.2	
θ 29	61.3	65.3	69.3	
θ 28	59.4	63.4	67.4	
θ 27	57.5	61.5	65.5	
θ 26	55.6	59.6	63.6	
θ 25	53.6	57.6	61.6	
θ 24	51.6	55.6	59.6	
θ 23	49.5	53.5	57.5	
θ 22	47.4	51.4	55.4	
θ 21	45.3	49.3	53.3	
θ 20	43.1	47.1	51.1	
θ 19	41.0	45.0	49.0	
θ 18	38.8	42.8	46.8	
θ 17	36.5	40.5	44.5	
θ 16	34.3	38.3	42.3	
θ 15	32.0	36.0	40.0	
θ 14	29.7	33.7	37.7	
θ 13	27.4	31.4	35.4	
θ 12	25.0	29.0	33.0	
θ 11	22.7	26.7	30.7	
θ 10	20.3	24.3	28.3	
θ 9	17.9	21.9	25.9	
θ 8	15.5	19.5	23.5	
θ 7	13.1	17.1	21.1	
θ 6	10.7	14.7	18.7	
θ 5	8.2	12.2	16.2	
θ 4	5.8	9.8	13.8	
θ 3	3.4	7.4	11.4	
θ 2	0.9	4.9	8.9	
θ 1	0.0	2.5	6.5	
θ 0	---	0.0	---	

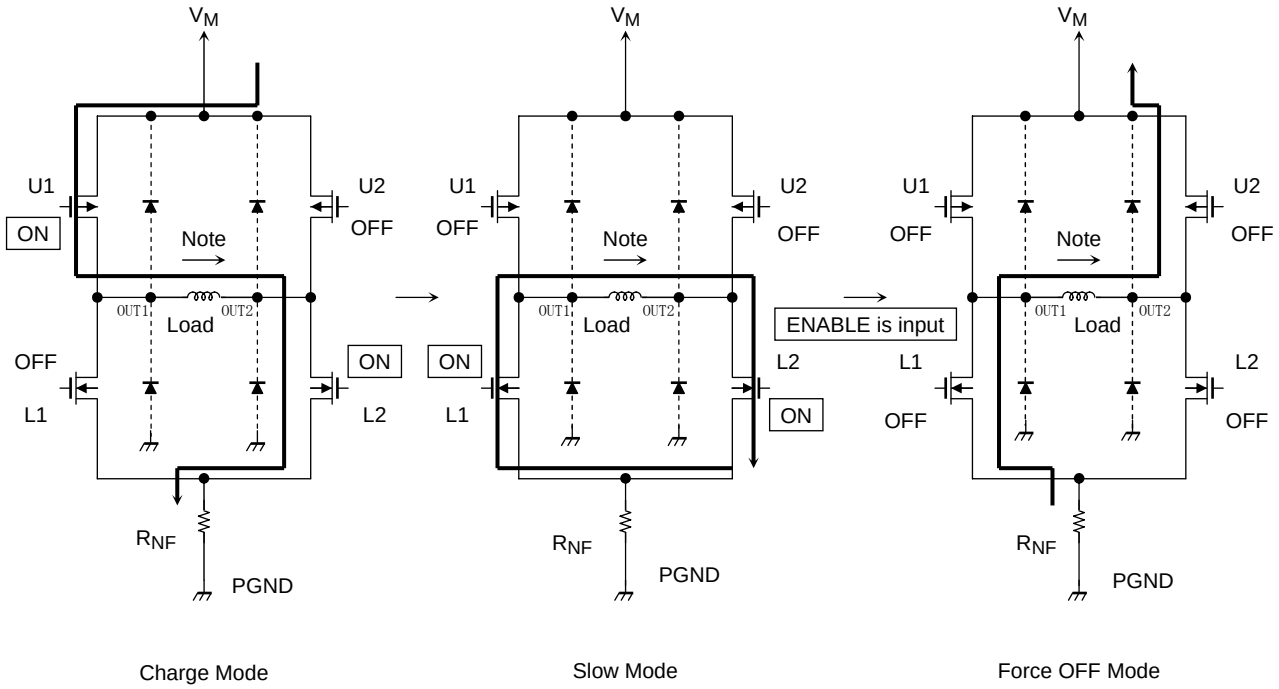
Current level (1/40, 1/20, 1/10)

1/40, 1/20, 1/10	Min.	Typ.	Max.	Unit
θ40	---	100.0	---	
θ39	95.9	99.9	100.0	
θ38	95.7	99.7	100.0	
θ37	95.3	99.3	100.0	
θ36	94.8	98.8	100.0	
θ35	94.1	98.1	100.0	
θ34	93.2	97.2	100.0	
θ33	92.2	96.2	100.0	
θ32	91.1	95.1	99.1	
θ31	89.8	93.8	97.8	
θ30	88.4	92.4	96.4	
θ29	86.8	90.8	94.8	
θ28	85.1	89.1	93.1	
θ27	83.2	87.2	91.2	
θ26	81.3	85.3	89.3	
θ25	79.1	83.1	87.1	
θ24	76.9	80.9	84.9	
θ23	74.5	78.5	82.5	
θ22	72.0	76.0	80.0	
θ21	69.4	73.4	77.4	
θ20	66.7	70.7	74.7	%
θ19	63.9	67.9	71.9	
θ18	60.9	64.9	68.9	
θ17	57.9	61.9	65.9	
θ16	54.8	58.8	62.8	
θ15	51.6	55.6	59.6	
θ14	48.2	52.2	56.2	
θ13	44.9	48.9	52.9	
θ12	41.4	45.4	49.4	
θ11	37.9	41.9	45.9	
θ10	34.3	38.3	42.3	
θ9	30.6	34.6	38.6	
θ8	26.9	30.9	34.9	
θ7	23.1	27.1	31.1	
θ6	19.3	23.3	27.3	
θ5	15.5	19.5	23.5	
θ4	11.6	15.6	19.6	
θ3	7.8	11.8	15.8	
θ2	3.8	7.8	11.8	
θ1	0.0	3.9	7.9	
θ0	---	0.0	---	

Current Draw-out Path when ENABLE is Input in Mid Operation

When all the output transistors are forced OFF during Slow mode, the coil energy is drawn out in the following modes:

Note: Parasitic diodes are indicated on the designed lines. However, these are not normally used in Mixed Decay mode.

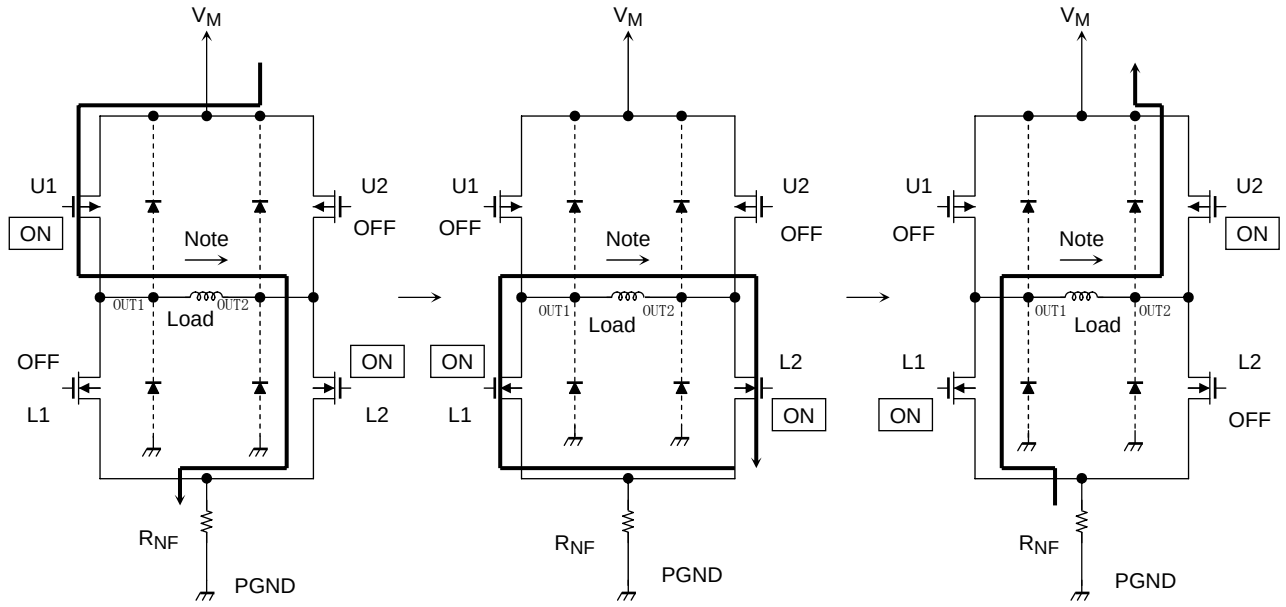


Charge Mode Slow Mode Force OFF Mode

As shown in the figure above, an output transistor has parasitic diodes.

Normally, when the energy of the coil is drawn out, each transistor is turned ON and the power flows in the opposite-to-normal direction; as a result, the parasitic diode is not used. However, when all the output transistors are forced OFF, the coil energy is drawn out via the parasitic diode.

Output Stage Transistor Operation Mode



Output Stage Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above chart shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following chart:

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Upon transitions of above-mentioned functions, a dead time of about 300 ns (Design target value) is inserted respectively.

Measurement Waveform

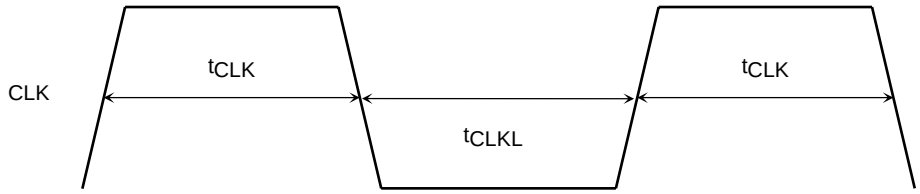


Figure 1 Timing Waveforms and Names

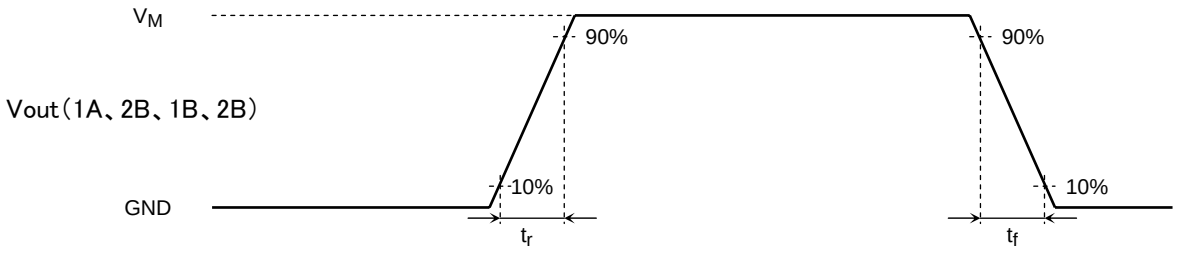
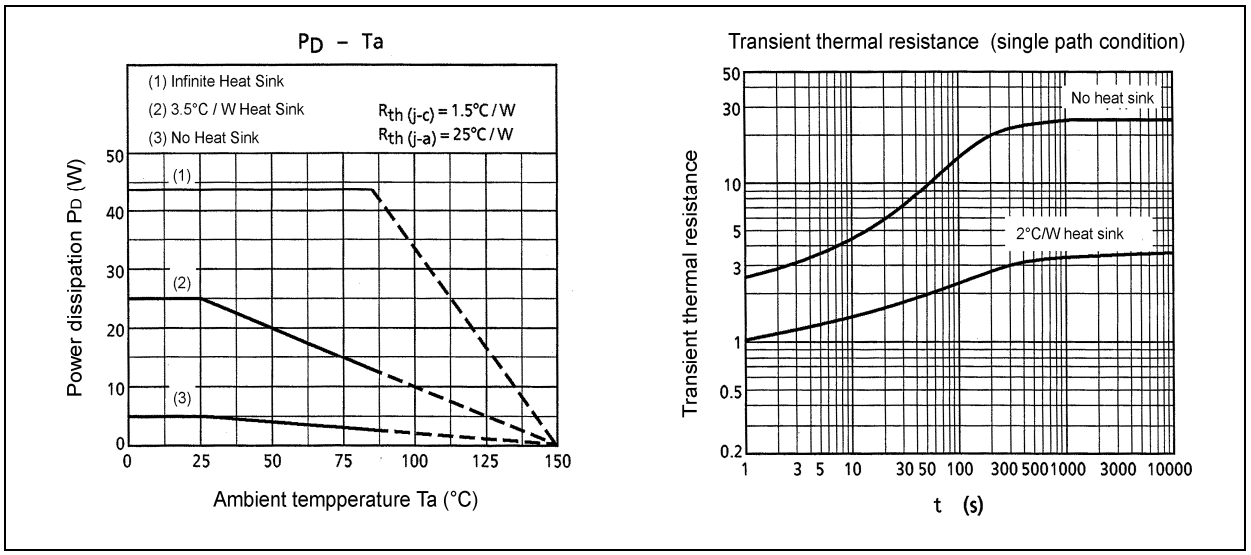


Figure 2 Timing Waveforms and Names

Power Dissipation

TB6564AHQ （THB6064AH）

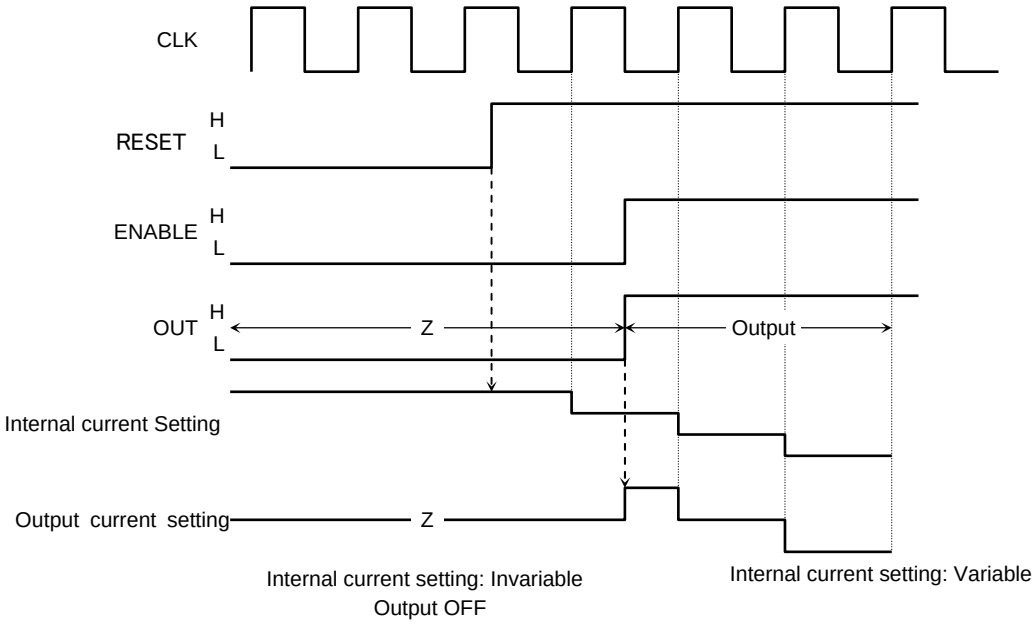


1. How to Turn on the Power

We would like to recommend a way to turn on the power as shown below. However, if you do not do what we mentioned, IC can not break.

Turn on V_{DD}. When the voltage has stabilized, turn on $V_{MA/B}$.
In addition, set the Control Input pins to Low when inputting the power.
(All the Control Input pins are pulled down internally.)
Once the power is on, the CLK signal is received and excitation advances when RESET goes high and excitation is output when ENABLE goes high. If only RESET goes high, excitation won't be output and only the internal counter will advance. Likewise, if only ENABLE goes high, excitation won't advance even if the CLK signal is input and it will remain in the initial state.
The following is an example:

<Recommended Control Input Sequence>



2. Power Dissipation

The IC power dissipation is determined by the following equation:

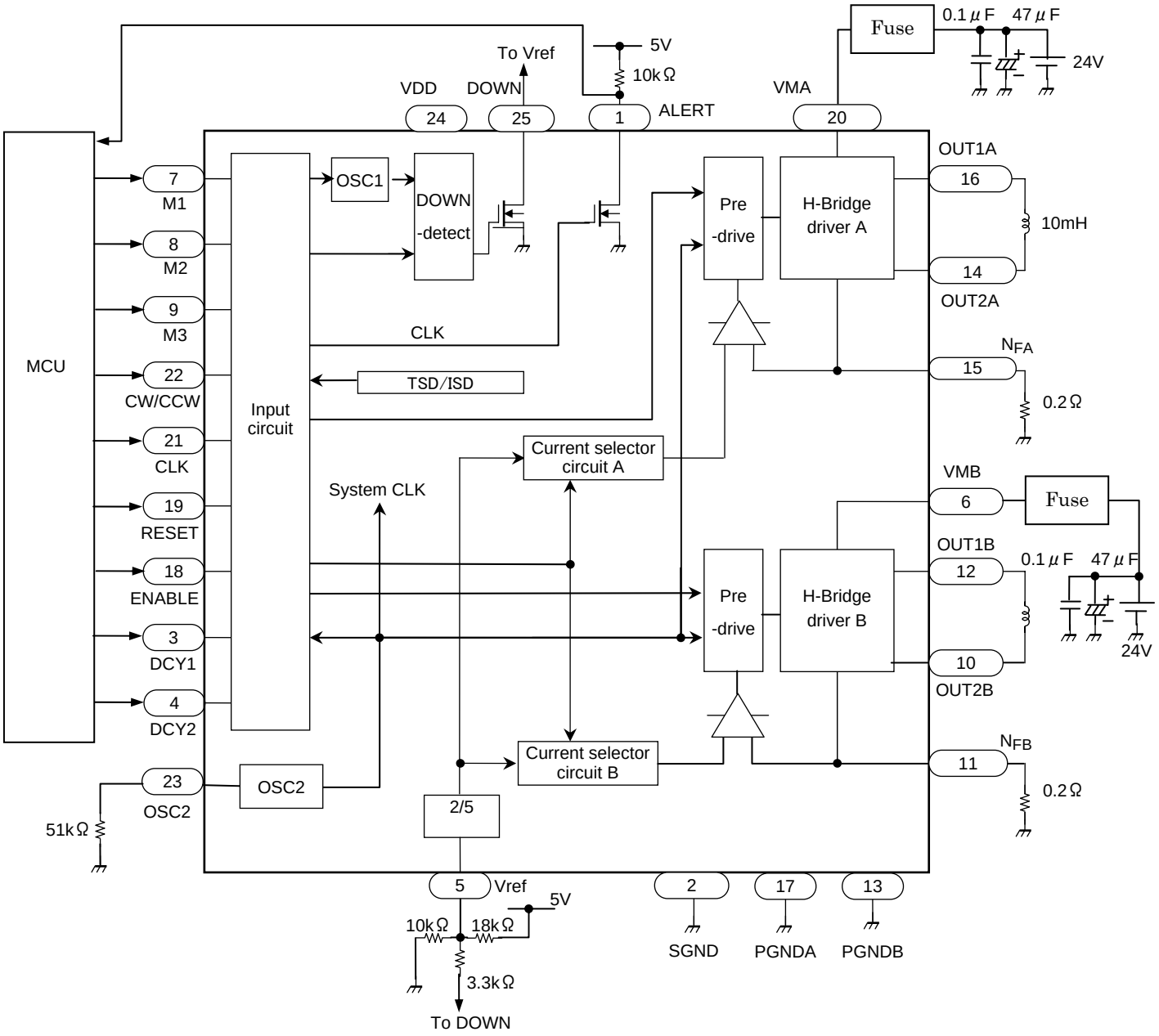
$P = V_{DD} \times I_{DD} + I_{OUT} \times I_{OUT}$ x Ron × 2 drivers

The higher the ambient temperature, the smaller the power dissipation.
Check the PD-Ta curve, and be sure to design the heat dissipation with a sufficient margin.

3. Heat Sink Fin Processing

The IC fin (rear) is electrically connected to the rear of the chip. If current flows to the fin, the IC will malfunction. If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

Application example



Note: Capacitors for the power supply lines should be connected as close to the IC as possible.

Usage Considerations

A large current might abruptly flow through the IC in case of a short-circuit across its outputs, a short-circuit to power supply or a short-circuit to ground, leading to a damage of the IC. Also, the IC or peripheral parts may be permanently damaged or emit smoke or fire resulting in injury especially if a power supply pin (V_{DD}, V_{MA} and V_{MB}) or an output pin (OUT1A, OUT2A, OUT1B and OUT2B) is short-circuited to adjacent or any other pins. These possibilities should be fully considered in the design of the output, V_{DD}, V_M, and ground lines.

A fuse should be connected to the power supply line.

(As for above notes, a possibility that the TB6564AHQ is damaged by large current is the same as the TB6564HQ because specifications of the TB6564HQ are the same as the TB6564AHQ about it.)

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

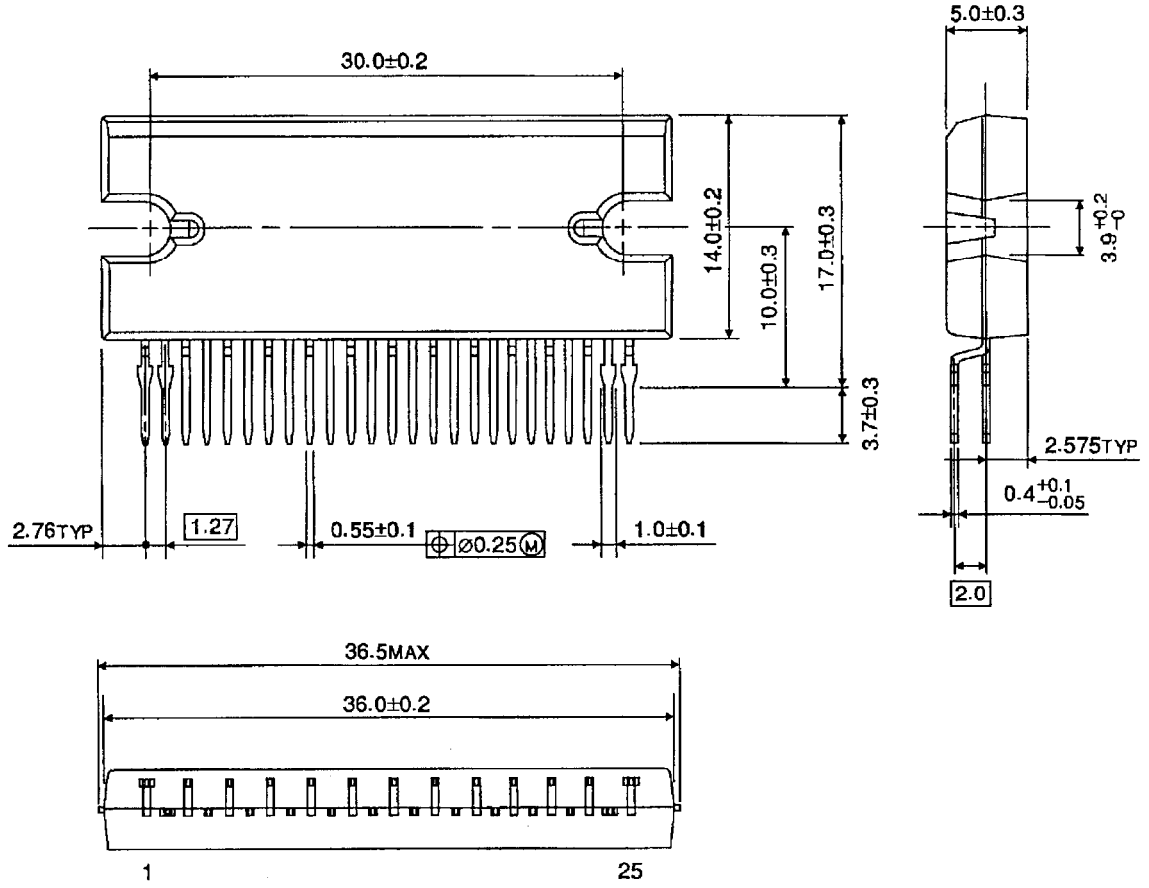
[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Package Dimensions

HZIP25-P-1.27 Unit : mm



Weight: 9.86 g (typ.)

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