TOSHIBA
NAND memory
Toggle DDR1.0
Technical Data Sheet

Rev. 0.6

2013 – 07 – 10

TOSHIBA
Semiconductor & Storage Products
Memory Division

CONTENTS

LIST of FIGURES

LIST of TABLES

1. INTRODUCTION

1.1. General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.

Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.

Toggle DDR1.0 NAND supports the interface speed of up to 100 MHz, which is faster than the data transfer rate offered by SDR NAND. Toggle DDR NAND transfers data at high speed using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

This device supports both SDR interface and Toggle DDR interface. When starting, the device is activated in SDR mode. The interface mode can be changed into Toggle DDR interface utilizing specific command issued by the Host.

1.2. Definitions and Abbreviations

SDR
Acronym for single data rate.

DDR
Acronym for double data rate.

Address
The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

Column
The byte location within the page register.

Row
Refer to the block and page to be accessed.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Plane
The unit that consists of a number of blocks. There are one or more Planes per LUN.

Page register
Register used to transfer data to and from the Flash Array.

Cache register
Register used to transfer data to and from the Host.

Defect area
The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2

Device
The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)
The minimum unit that can independently execute commands and report status. There are one or more LUNs per $\overline{CE}$.

Target
An independent NAND Flash component with its own $\overline{CE}$ signal.

SR[x] (Status Read)
SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to section 5.13 for the definition of bit meanings within the status register.

1.3. Features

- **Product Organization**

Table 1 Product Organization

Parameter	TC58TEG6DDK	TH58TEG7DDK	TH58TEG8DDK
Part number (T_{OPER}: 0~70℃)	TC58TEG6DDKTA00	TH58TEG7DDKTA20	TH58TEG8DDKTA20
Part number (T_{OPER}: -40~85℃)	TC58TEG6DDKTAI0	TH58TEG7DDKTAK0	TH58TEG8DDKTAK0
Device capacity	17664×256×2132×8 bits	17664×256×2132×8×2 bits	17664×256×2132×8×4 bits
Page size	17664 Bytes	17664 Bytes	17664 Bytes
Block size	(4M + 320 K) Bytes	(4M + 320 K) Bytes	(4M + 320 K) Bytes
Plane size	4820434944Bytes	4820434944Bytes	4820434944Bytes
Plane per one LUN	2 Planes	2 Planes	2 Planes
LUN per one target	1 LUNs	1 LUNs	2LUNs
Target per one device	1 target	2 targets	2 targets
Number of valid blocks per a device (min)	2018(TENTATIVE)	4036(TENTATIVE)	8072(TENTATIVE)
Number of valid blocks per a device (max)	2132(TENTATIVE)	4264(TENTATIVE)	8528(TENTATIVE)
Package weight	TBD g	TBD g	TBD g

- **Modes**

Basic Operation
Page Read Operation (with Random Data Output), Data Out After Status Read, Sequential Cache Read Operation, Random Cache Read Operation, Page Program Operation (with Random Data Input), Cache Program Operation, Block Erase Operation, Copy-Back Program Operation (with Random Data Input), Set Feature Operation, Get Feature Operation, Read ID Operation, Read Status Operation, Reset Operation, Reset LUN Operation

Extended Operation
Multi Page Read Operation, Multi Sequential Cache Read Operation, Multi Page Random Cache Read Operation, Multi Page Program Operation, Multi Cache Program Operation, Multi Block Erase Operation, Multi Copy-Back Program Operation,
Page Copy (2) Operation, Multi Page Copy (2) Operation,
Device Identification Table Read Operation, Read Status Enhanced Operation, Read LUN #0 Status Operation

Interleaving Operation
Interleaving Page Program, Interleaving Page Read, Interleaving Block Erase, Interleaving Multi Page Program, Interleaving Multi Block Erase, Interleaving Read to Page Program, Interleaving Copy-Back Program, Interleaving Multi Copy Back Program

Table 2 Supported Operation Modes

Operation Mode	TC58TEG6DDK	TH58TEG7DDK	TH58TEG8DDK
Basic Operation	Supported	Supported	Supported
Extended Operation	Supported	Supported	Supported
Interleaving Operation	Not supported	Not supported	Supported

NOTE :
1) Read LUN #1 Status Operation is supported only if the Target has more than 2 LUNs.

- **Mode control**
  Serial input/output
  Command control

- **Power supply**
  V_{CC} = 2.7 V to 3.6 V
  V_{CCQ} = 2.7 V to 3.6 V / 1.7 V to 1.95V

- **Access time**
  - Cell array to register TBD μs max
    TBD μs typ.
  - Data Transfer rate 100 MHz

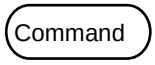
- **Program/Erase time**
  - Auto Page Program TBD μs/page typ.
  - Auto Block Erase TBD ms/block typ.

- **Operating current**
  - Read TBD mA max. (per 1 chip)
  - Program (avg.) TBD mA max. (per 1 chip)
  - Erase (avg.) TBD mA max. (per 1 chip)

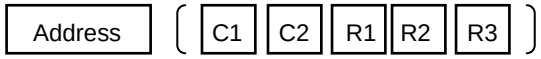
- **Reliability**
  - Refer to APPLICATION NOTES AND COMMENTS.

1.4. Diagram Legend

Diagrams in the Toggle DDR1.0 datasheet use the following legend:

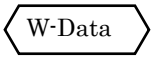


This legend shows the command data. Refer to the Table 31 for more information about the command data.

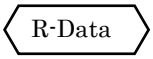


This legend shows the Address data. The addresses are comprised of 2 cycles column address and 3 cycles row address.

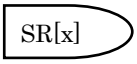
C1: Column address 1
C2: Column address 2
R1: Row address 1
R2: Row address 2
R3: Row address 3



This legend shows Host writing data (data input) to the device.



This legend shows Host reading data (data output) from the device.



This legend shows Host reading the status register within a particular LUN.

2. PHYSICAL INTERFACE

2.1. Pin Descriptions

Table 3 Pin Descriptions

SDR	Toggle DDR1.0	Pin Function
DQ[7:0]	DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE	ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one.
$\overline{WE}$	$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
-	DQS	**DATA STROBE** Output with read data, input with write data. Edge-aligned with read data, centered in write data.
Vcc	Vcc	**POWER** VCC is the power supply for device.
VccQ	VccQ	**DQ POWER** The VccQ is the power supply for input and/or output signals.
Vss	Vss	**GROUND**
VssQ	VssQ	**DQ GROUND** The VssQ is the power supply ground
V_{PP}	V_{PP}	**External V_{PP}** The V_{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improved power efficiency).
NC	NC	**No connection** NCs are not internally connected. They can be driven or left unconnected.
NU	NU	**Not use** NUs must be left unconnected.

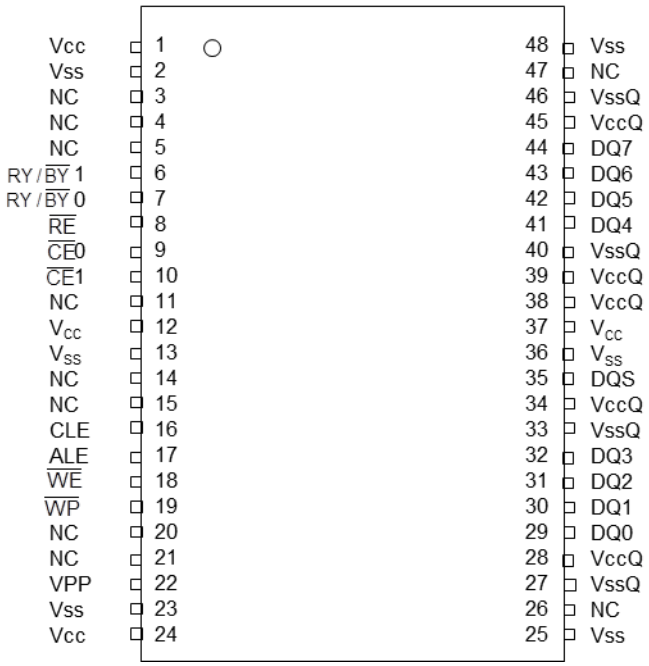
NOTE:

1) Connect all Vcc and Vss pins of each device to common power supply outputs.

2) Do not leave all Vcc, VccQ, Vss and VssQ disconnected.

2.2. PIN ASSIGNMENT (TOP VIEW)

Tx58TEGxDDK



NOTE:

1) The Pin assignment supports 2CE/2RB.

2.3. BLOCK DIAGRAM

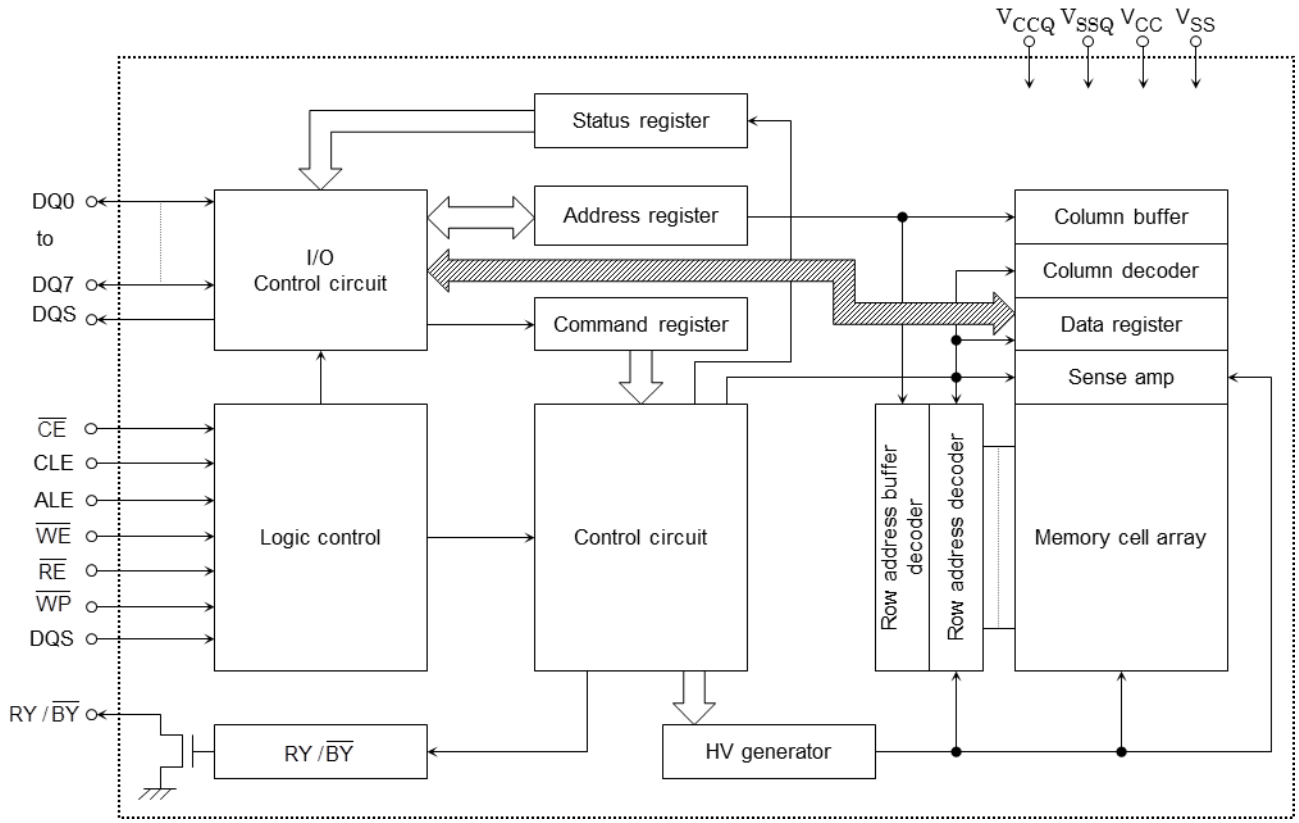


Figure 1. Block Diagram (TC58TEG6DDK)

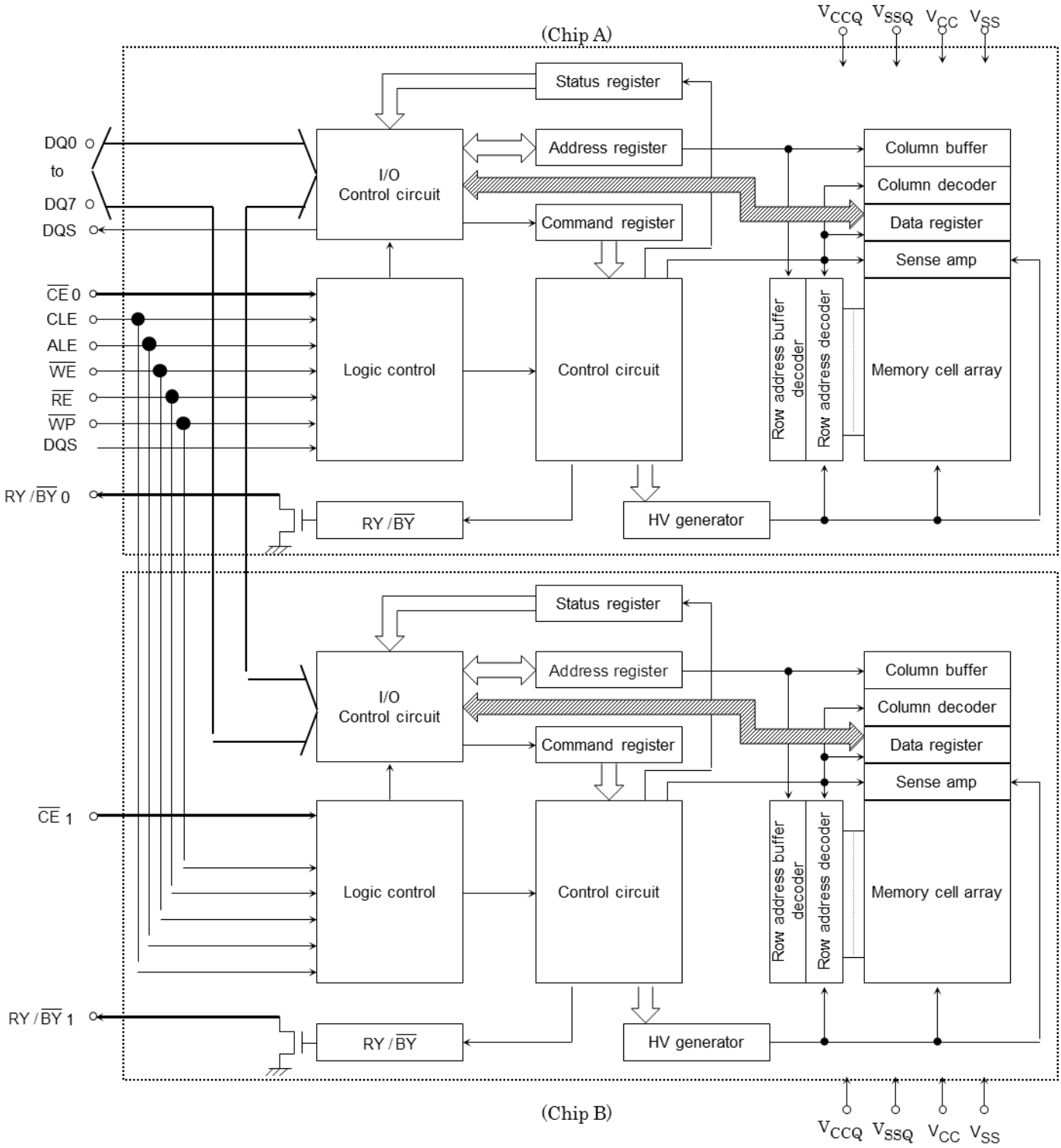


Figure 2. Block Diagram (TH58TEG7DDK)

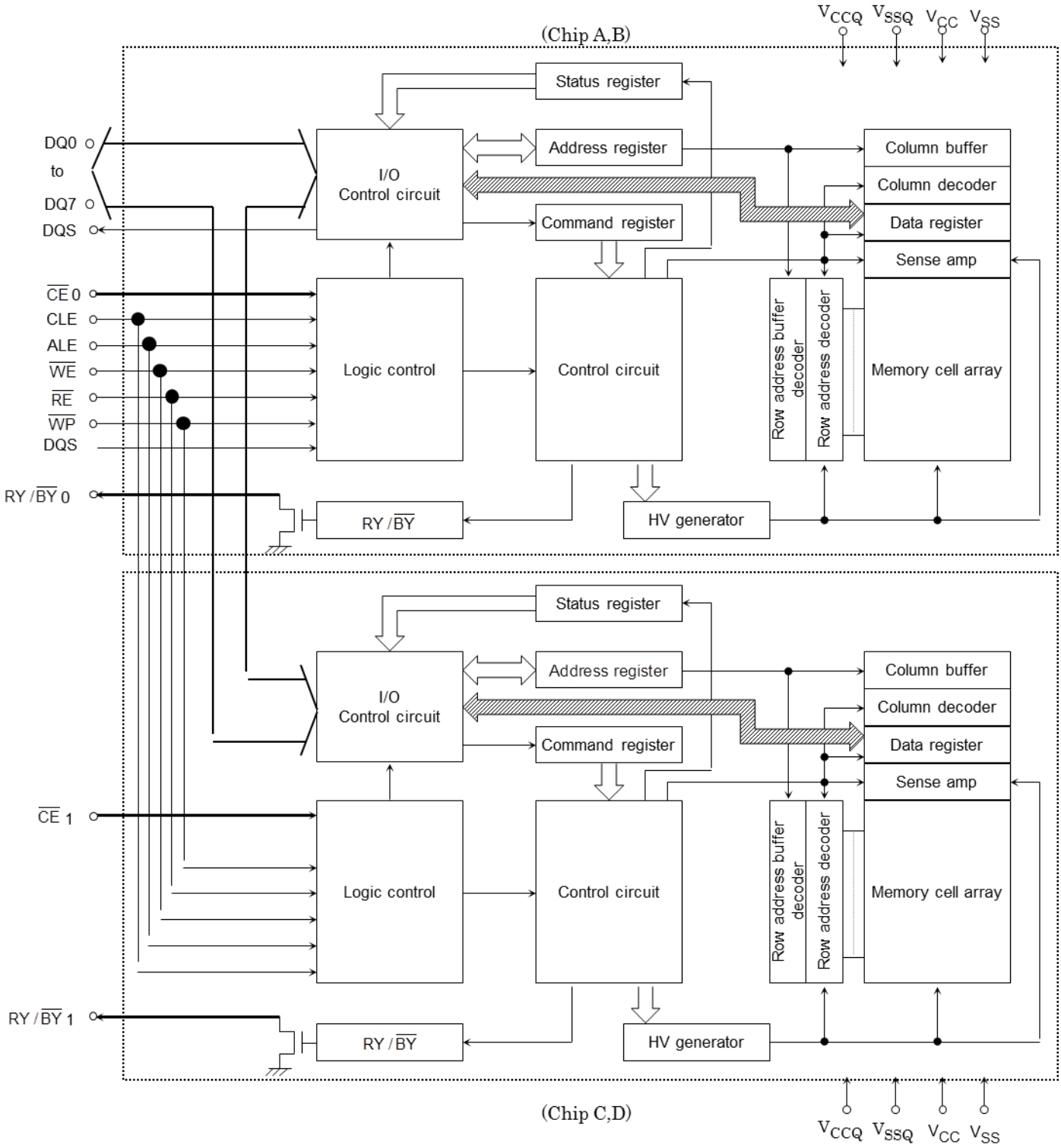


Figure 3. Block Diagram (TH58TEG8DDK)

2.4. Independent Data Buses

There may be two independent 8-bit data buses in some packages, with two, four or eight $\overline{CE}$ signals. If the device supports two independent data buses, then $\overline{CE}1$, $\overline{CE}3$, $\overline{CE}5$, and $\overline{CE}7$ (if connected) shall use the second data bus. $\overline{CE}0$, $\overline{CE}2$ $\overline{CE}4$, and $\overline{CE}6$ shall always use the first data bus pins. Note that all $\overline{CE}$s may use the first data bus and the first set of control signals ($\overline{RE}0$, CLE0, ALE0, $\overline{WE}0$, and $\overline{WP}0$) if the device does not support independent data buses. Table 4 defines the control signal to $\overline{CE}$ signal mapping when there are two independent x8 data buses.

Table 4 Dual Channel(x8) Data Bus Signal to $\overline{CE}$ mapping

Signal Name	CE
R/$\overline{B}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 4
R/$\overline{B}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 5
R/$\overline{B}$ 2	$\overline{CE}$ 2, $\overline{CE}$ 6
R/$\overline{B}$ 3	$\overline{CE}$ 3, $\overline{CE}$ 7
$\overline{RE}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{RE}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
CLE0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
CLE1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
ALE0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
ALE1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
$\overline{WE}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{WE}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
$\overline{WP}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{WP}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
DQS0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
DQS1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7

Implementations may tie the data lines and control signals ($\overline{RE}$, CLE, ALE, $\overline{WE}$, $\overline{WP}$, and DQS) together for the two independent 8-bit data buses externally to the device.

2.5. Absolute Maximum DC Rating

Stresses greater than those listing in Table 5 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 6 is not recommended. Extended exposure beyond these conditions may affect device reliability.

Table 5 Absolute Maximum Rating

Parameter	Symbol		Rating	Unit
Voltage on any pin relative to VSS	VCC		-0.6 to +4.6	V
	VCCQ		-0.6 to +4.6	
	VIN	VccQ(3.3V)	-0.6 to +4.6	
		VccQ(1.8V)	-0.2 to +2.4	
	VI/O	VccQ(3.3V)	-0.6 to +4.6	
		VccQ(1.8V)	-0.2 to +2.4	
	VPP		-0.6 to 16.0	

2.6. Operating Temperature Condition

Table 6 Operating Temperature Condition

Symbol	Parameter	Part Number	Rating	Unit
TOPER	Operating Temperature Range for Commercial	TC58TEG6DDKTA00	0～70	℃
	Operating Temperature Range for Industrial	TC58TEG6DDKTAI0	-40～+85	
	Operating Temperature Range for Commercial	TH58TEG7DDKTA20	0～70	
	Operating Temperature Range for Industrial	TH58TEG7DDKTAK0	-40～+85	
	Operating Temperature Range for Commercial	TH58TEG8DDKTA20	0～70	
	Operating Temperature Range for Industrial	TH58TEG8DDKTAK0	-40～+85	
T_{SOLDER}	Soldering Temperature (10 s)		260	
T_{STG}	Storage Temperature		-55～+150	

NOTE:

1) Operating Temperature (T_{OPER}) is the case surface temperature on the center/top side of the NAND.

2) Operating Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between the range specified in the table under all operating conditions.

2.7. Recommended Operating Conditions

Table 7 Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Ground Voltage	VSS	0	0	0	V
Supply Voltage for 1.8V I/O signaling	VccQ	1.7	1.8	1.95	V
Supply Voltage for 3.3V I/O signaling	VccQ	2.7	3.3	3.6	V
Ground Voltage for I/O signaling	VssQ	0	0	0	V

VccQ and Vcc may be distinct and unique voltages. The device shall support one of the following VccQ/Vcc combinations,

Vcc = 3.3V, VccQ = 3.3V
Vcc = 3.3V, VccQ = 1.8V

All parameters, timing modes and other characteristics are related to the supported voltage combination.

2.8. Valid Blocks

Table 8 Valid Blocks

Number of Valid Blocks per a device	TC58TEG6DDK	TH58TEG7DDK	TH58TEG8DDK
Min	2018(TENTATIVE)	4036(TENTATIVE)	8072(TENTATIVE)
Max	2132(TENTATIVE)	4264(TENTATIVE)	8528(TENTATIVE)

NOTE:

1) The device occasionally contains unusable blocks.

2) The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

3) The specification for the minimum number of valid blocks is applicable over the device lifetime.

4) The number of valid blocks includes extended blocks.

2.9. AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from VccQ and VssQ levels. Table 9 defines the maximum values that the AC overshoot or undershoot may attain. These values apply for both 3.3V and 1.8V VccQ levels.

Table 9 AC Overshoot/Undershoot Specification

Parameter	Maximum Value				Unit
	~50Mhz	51~66Mhz	67~83Mhz	84~100Mhz	
Max. peak amplitude allowed for overshoot area	1	1	1	1	V
Max. peak amplitude allowed for undershoot area	1	1	1	1	V
Max. overshoot area above VccQ	3	2.25	1.8	1.5	V*ns
Max. undershoot area above VssQ	3	2.25	1.8	1.5	V*ns

NOTE:

1) This specification is intended for devices with no clamp protection and is guaranteed by design.

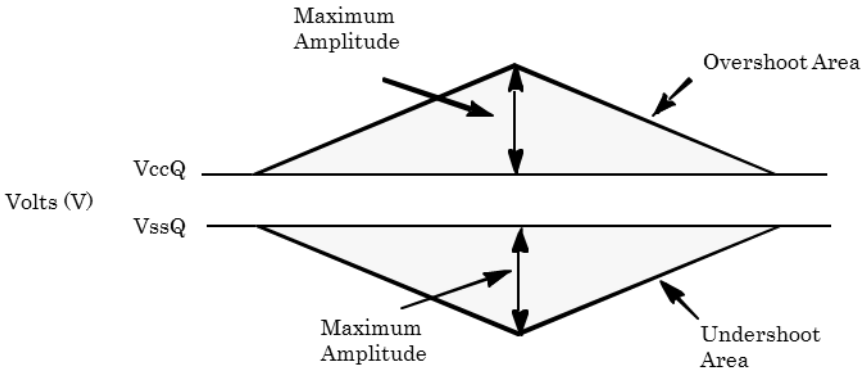


Figure 4. Overshoot/Undershoot Diagram

2.10. DC Operating Characteristics

Table 10 DC & Operating Characteristics for Toggle VccQ=3.3V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Operation Current	I_{CC1}	-	-	-	TBD	mA
Page Program Operation Current	I_{CC2}	-	-	-	TBD	
Erase Operation Current	I_{CC3}	-	-	-	TBD	
DQ Burst Read Current for Vcc	I_{CC4R}	t_{RC}= t_{RC}(min.), Half data switchiing	-	-	80	
DQ Burst Write Current for Vcc	I_{CC4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	80	
DQ Burst Write Current for Vccq	I_{CCQ4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	10	
Bus Idle Current	I_{CC5}	-	-	-	10	
Stand-by Current(CMOS)	I_{SB}	$\overline{CE}$ =VccQ-0.2, $\overline{WP}$ =0V/VccQ	-	-	NOTE 5)	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to VccQ(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to VccQ(max)	-	-	NOTE 7)	
V_{PP} Current	I_{PP}	V_{PP} is enabled	-	-	5	mA
AC Input High Voltage	V_{IH} (AC)	-	0.8 xVccQ	-	NOTE 8)	V
DC Input High Voltage	V_{IH} (DC)	-	0.7 xVccQ	-	VccQ +0.3	
AC Input Low Voltage	V_{IL} (AC)	-	NOTE 8)	-	0.2 xVccQ	
DC Input Low Voltage	V_{IL} (DC)	-	-0.3	-	0.3 xVccQ	
Output High Voltage Level	V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1mA	-	-	0.4	
External Vpp	Vpp	-	11.5	12	12.5	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE: The values in this table are preliminary and subject to change.

1) Typical value is measured at Vcc=3.3V, T_{OPER} =25℃. Not 100% tested.

2) V_{OH} and V_{OL} should be available on these two conditions; Output Strength is nominal and VccQ=3.3V, Rpd/Rpu are all VccQx0.5. If the drive strength settings are supported, Table 14shall be used to derive the output driver impedance values.

3) Icc1,2 are without data cache.

4) Icc1/2/3, ICC4R, ICC4W, ICCQ4W and ICC5 are the value of one active logical unit.

5) TC58TEG6DDK=TBDµA,TH58TEG7DDK=TBDµA,and TH58TEG8DDK=TBDµA.

6) DQ, DQS and RE apply I_{LO} characteristic. Other pins apply I_{LI} characteristic.

7) TC58TEG6DDK=±10µA,TH58TEG7DDK=±20µA,and TH58TEG8DDK=±40µA.

8) Refer to AC Overshoot and Undershoot requirements.

Table 11 DC & Operating Characteristics for Toggle VccQ=1.8V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Operation Current	I_{CC1}	-	-	-	TBD	mA
Page Program Operation Current	I_{CC2}	-	-	-	TBD	
Erase Operation Current	I_{CC3}	-	-	-	TBD	
DQ Burst Read Current for Vcc	I_{CC4R}	t_{RC}= t_{RC}(min.) Half data switchiing	-	-	80	
DQ Burst Write Current for Vcc	I_{CC4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	80	
DQ Burst Write Current for Vccq	I_{CCQ4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	10	
Bus Idle Current	I_{CC5}	-	-	-	10	
V_{PP} Current	I_{PP}	V_{PP} is enabled	-	-	5	mA
Stand-by Current(CMOS)	I_{SB}	$\overline{CE}$ =VccQ-0.2, $\overline{WP}$ =0V/VccQ	-	-	NOTE 5)	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to VccQ(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to VccQ(max)	-	-	NOTE 7)	
AC Input High Voltage	V_{IH} (AC)	-	0.8 xVccQ	-	NOTE 8)	V
DC Input High Voltage	V_{IH} (DC)	-	0.7 xVccQ		VccQ +0.3	
AC Input Low Voltage	V_{IL} (AC)	-	NOTE 8)	-	0.2 xVccQ	
DC Input Low Voltage	V_{IL} (DC)	-	-0.3	-	0.3 xVccQ	
Output High Voltage Level	V_{OH}	I_{OH}=-100µA	VccQ-0.1	-	-	
Output Low Voltage Level	V_{OL}	I_{OL}= 100µ A	-	-	0.1	
External Vpp	Vpp	-	11.5	12	12.5	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.2V	3	4	-	mA

NOTE: The values in this table are preliminary and subject to change.

1) Typical value is measured at Vcc=3.3V, T_{OPER}=25℃. Not 100% tested.

2) VOH and VOL should be available on these two conditions; Output Strength is nominal and VccQ=1.8V, Rpd/Rpu are all VccQx0.5. If the drive strength settings are supported, Table 14 shall be used to derive the output driver impedance values.

3) Icc1,2 are without data cache.

4) Icc1/2/3, ICC4R, ICC4W, ICCQ4W and ICC5 are the value of one active logical unit.

5) TC58TEG6DDK=TBDµA,TH58TEG7DDK=TBDµA,and TH58TEG8DDK=TBDµA.

6) DQ, DQS and RE apply I_{LO} characteristic. Other pins apply I_{LI} characteristic.

7) TC58TEG6DDK=±10µA,TH58TEG7DDK=±20µA,and TH58TEG8DDK=±40µA.

8) Refer to AC Overshoot and Undershoot requirements.

Table 12 DC & Operating Characteristics for SDR VccQ=1.8V and 3.3V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IL}	V_{IN} = 0 V to V_{CC}	—	—	±10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 V to V_{CC}	—	—	NOTE 3)	
Power On Reset Current	I_{CCO0} *1,*5	$\overline{CE}$ = V_{IL}	—	—	TBD	mA
Read Mode Current	I_{CCO1} *2,*5	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	TBD	
Auto Page Program Current	I_{CCO2} *2,*5	—	—	—	TBD	
Auto Block Erase current	$I_{CCO3,*5}$	—	—	—	TBD	
Standby Current	I_{CCS}	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	NOTE 4)	µA
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	—	0.4	
Output current of RY/$\overline{BY}$ pin	I_{OL} (RY/$\overline{BY}$)	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	8	—	mA

NOTE: The values in this table are preliminary and subject to change.

1)*1: Icco0 is the average current during R/B signal="Busy" state.

2)*2: All operation current are without data cache.

3)*3: TC58TEG6DDK=±10µA,TH58TEG7DDK=±20µA,and TH58TEG8DDK=±40µA.

4)*4: TC58TEG6DDK=TBDµA,TH58TEG7DDK=TBDµA,and TH58TEG8DDK=TBDµA.

5)*5: Icco0/1/2 and 3 are the value of one active logical unit.

2.11. Input/Output Capacitance (T_{OPER} =25℃, f=1MHz)

Table 13 Input/ Output capacitance

SYMBOL	Parameter	Test Condition	Min	Max			Unit
				TC58TEG6DDK	TH58TEG7DDK	TH58TEG8DDK	
C_{IN}	Input	V_{IN}=0V	-	10	20	40	pF
C_{OUT}	Output	V_{OUT}=0V	-	10	20	40	pF

2.12. DQ Driver Strength

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive, Nominal, Overdrive 1 options. The Toggle DDR1.0 supports all three driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section. A device is only required to meet driver strength values for either 3.3V VccQ or 1.8V VccQ, and is not required to meet driver strength values for both 3.3V VccQ and 1.8V VccQ.

Table 14 DQ Drive Strength Settings

Setting	Driver Strength	VccQ
Overdrive 1	1.4x = 25 Ohms	3.3 V
Nominal	1.0x = 35 Ohms	
Underdrive	0.7x = 50 Ohms	
Overdrive 1	1.4x = 25 Ohms	1.8 V
Nominal	1.0x = 35 Ohms	
Underdrive	0.7x = 50 Ohms	

The impedance values corresponding to several different VccQ values are defined in Table 16 for 3.3V and 1.8V VccQ. The test conditions that shall be used to verify the impedance values are specified in Table 15. The terms T_{OPER}(Min) and T_{OPER}(Max) are in reference to the minimum and maximum operating temperature defined for the device.

Table 15 Testing Conditions for Impedance Values

Condition	Temperature	VccQ (3.3V)	VccQ (1.8V)	Process
Minimum Impedance	TOPER (Min) degrees Celsius	3.6 V	1.95 V	Fast - fast
Nominal Impedance	25 degrees Celsius	3.3 V	1.8 V	Typical
Maximum Impedance	TOPER (Max) degrees Celsius	2.7 V	1.7 V	Slow-slow

Table 16 Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to VssQ	Minimum		Nominal		Maximum		Units
			VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	
Overdrive1	Rpd	VccQ 0.2	8.0	10.5	15.0	19.0	30.0	44.0	ohms
		VccQ 0.5	15.0	13.0	25.0	25.0	45.0	47.0	ohms
		VccQ 0.8	20.0	16.0	35.0	32.5	65.0	61.5	ohms
	Rpu	VccQ 0.2	20.0	16.0	35.0	32.5	65.0	61.5	ohms
		VccQ 0.5	15.0	13.0	25.0	25.0	45.0	47.0	ohms
		VccQ 0.8	8.0	10.5	15.0	19.0	30.0	44.0	ohms
Nominal	Rpd	VccQ 0.2	12.0	15.0	22.0	27.0	40.0	62.5	ohms
		VccQ 0.5	20.0	18.0	35.0	35.0	65.0	66.5	ohms
		VccQ 0.8	25.0	22.0	50.0	52.0	100.0	88.0	ohms
	Rpu	VccQ 0.2	25.0	22.0	50.0	52.0	100.0	88.0	ohms
		VccQ 0.5	20.0	18.0	35.0	35.0	65.0	66.5	ohms
		VccQ 0.8	12.0	15.0	22.0	27.0	40.0	62.5	ohms
Underdrive	Rpd	VccQ 0.2	18.0	21.5	32.0	39.0	55.0	90.0	ohms
		VccQ 0.5	29.0	26.0	50.0	50.0	100.0	95.0	ohms
		VccQ 0.8	40.0	31.5	75.0	66.5	150.0	126.5	ohms
	Rpu	VccQ 0.2	40.0	31.5	75.0	66.5	150.0	126.5	ohms
		VccQ 0.5	29.0	26.0	50.0	50.0	100.0	95.0	ohms
		VccQ 0.8	18.0	21.5	32.0	39.0	55.0	90.0	ohms

Table 17 Pull-up and Pull-down Output Impedance Mismatch

Drive Strength	Minimum	Maximum	Unit
Overdrive 1	0.0	8.8	ohms
Nominal	0.0	12.3	ohms
Underdrive	0.0	17.5	ohms

NOTE:

1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.

2) Test conditions: VccQ = VccQ(min), Vout = VccQ×0.5

2.13. Input/Output Slew rate

The input slew rate requirements that the device shall comply with are defined in Table 18. The output slew rate requirements that the device shall comply with are defined in Table 20. The testing conditions that shall be used to verify the input slew rate and output slew rate are listed in Table 19 and Table 21 respectively.

Table 18 Input Slew Rate

Vccq	Minimum slew rate
3.3V	1.0V/ns
1.8V	1.0V/ns

Table 19 Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	VIL (DC) to VIH (AC)
Negative Input Transition	VIH (DC) to VIL (AC)

Table 20 Output Slew Rate Requirements

Parameter	VccQ=3.3V		VccQ=1.8V		Unit
	Minimum	Maximum	Minimum	Maximum	
Overdrive 1	1.5	9.0	0.85	5.0	V/ns
Nominal	1.2	7.0	0.75	4.0	V/ns
Underdrive	1.0	5.5	0.60	4.0	V/ns

NOTE :

1) Measured with a test load of 5pF connected to VssQ.
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Table 21 Testing Conditions for Output Slew Rate

Parameter	Value
V_{OL} (DC)	0.3 * VccQ
V_{OH} (DC)	0.7 * VccQ
V_{OL} (AC)	0.2 * VccQ
V_{OH} (AC)	0.8 * VccQ
Positive Output Transition	V_{OL} (DC) to V_{OH} (AC)
Negative Output Transition	V_{OH} (DC) to V_{OL} (AC)
t_{RISE}(1)	Time during Rising Edge from V_{OL} (DC) to V_{OH} (AC)
t_{FALL}(1)	Time during Falling Edge from V_{OH} (DC) to V_{OL} (AC)
Output Slew Rate Rising Edge	(V_{OH} (AC) - V_{OL} (DC)) / t_{RISE}
Output Slew Rate Falling Edge	(V_{OH} (DC) - V_{OL} (AC)) / t_{FALL}
Output Capacitive load	50 Ohms to Vtt (Vtt=0.5*VCCQ)

NOTE :

1) Refer to Figure 5.
2) Output slew rate is verified by design and characterization. It may not be subject to production test.
3) The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.

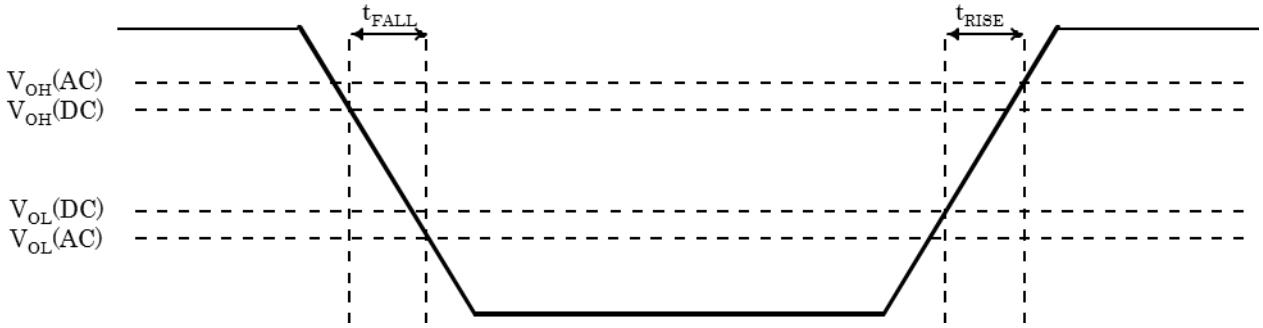


Figure 5. t_{RISE} and t_{FALL} Definition for Output Slew Rate

2.14. High Speed Toggle DDR with ODT

2.14.1. ODT (On die termination)

On Die Termination (ODT) is a feature that allows a NAND Flash device to turn on/off termination resistance for each DQ and DQS/$\overline{\text{DQS}}$. The ODT feature is designed to improve signal integrity of the memory channel by allowing the NAND Flash controller to independently turn on/off termination resistance for a selected target. NAND Flash memory supports self-termination only.

2.14.2. ODT setting

ODT setting is configured by 'SET FEATURE' operation. Refer to 5.2.9 for the further information. Figure 6 defines an ODT setting sequence.

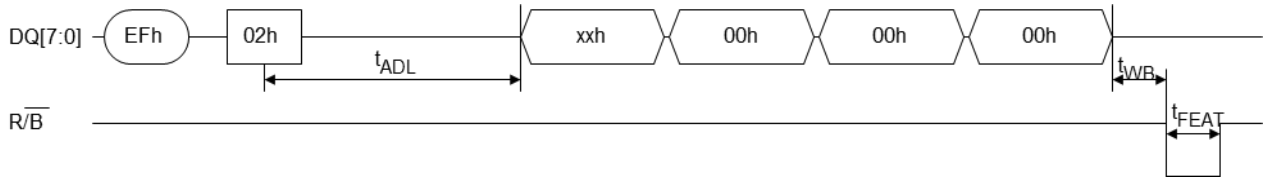


Figure 6. ODT setting through 'SET FEATURE'

2.14.3. ODT behavior during Read operation

ODT is enabled within Read pre-amble period after $\overline{\text{RE}}$ falling, and disabled on $\overline{\text{CE}}$ rising or one of CLE and ALE rising while $\overline{\text{CE}}$ is low. Figure 7 defines ODT enable/disable behavior and timings during data output.

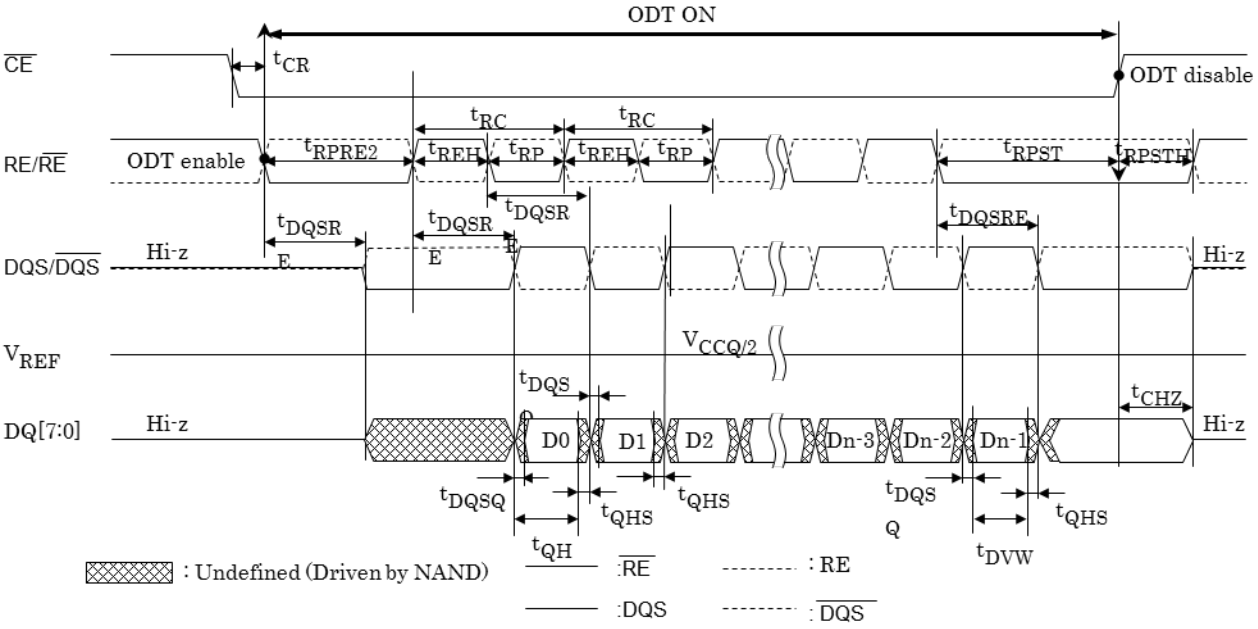


Figure 7. ODT enable/disable during Read

2.14.4. ODT behavior during Write operation

ODT is enabled within Write pre-amble period while ALE, CLE and DQS is low and disabled on $\overline{CE}$ rising or one of CLE and ALE rising while $\overline{CE}$ is low. Figure 8 defines ODT enable/disable behavior and timings during data input.

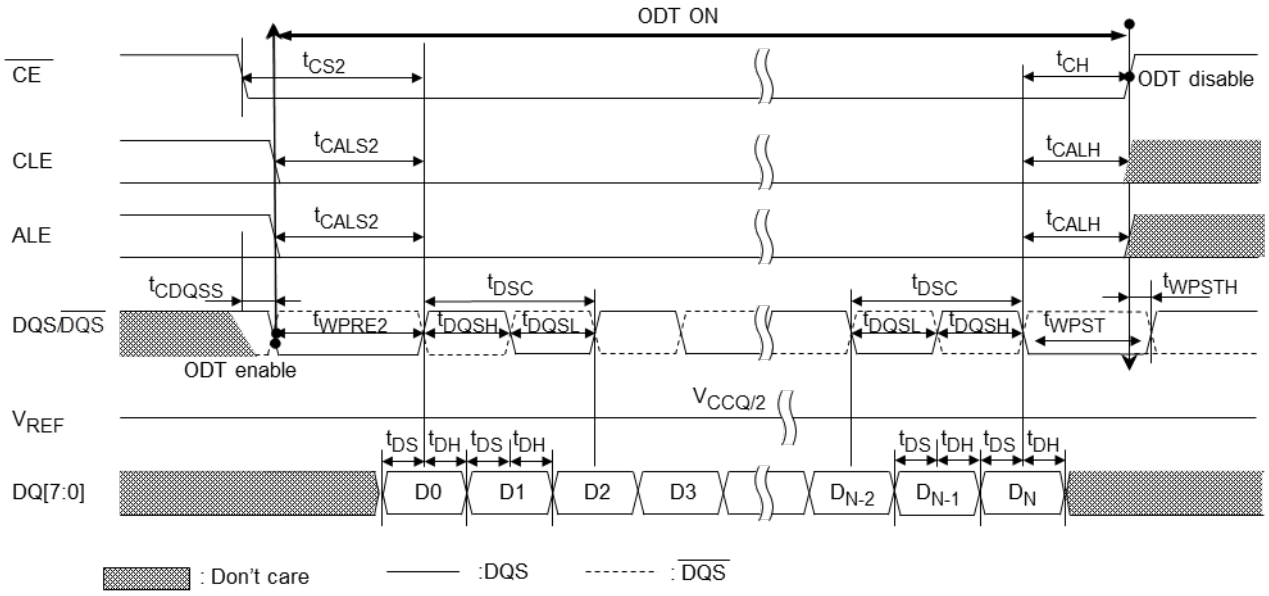


Figure 8. ODT enable/disable during Write

2.14.5. Functional Representation of ODT

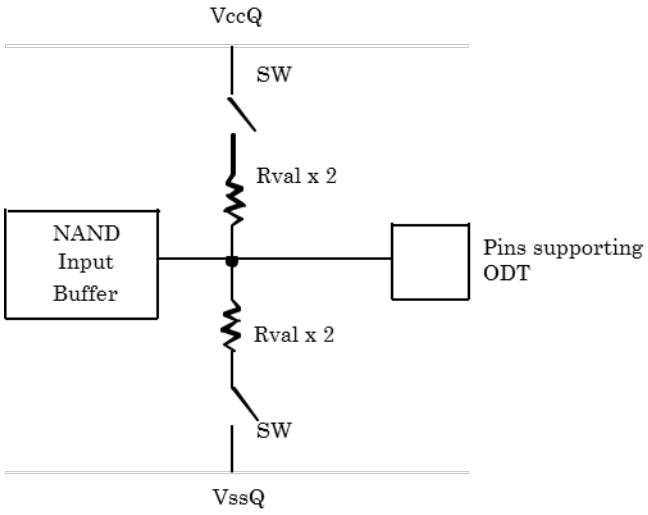


Figure 9. Functional Representation of ODT

2.15. R/$\overline{B}$ and SR[6] Relationship

R/$\overline{B}$ represents the status of the selected target. R/$\overline{B}$ goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

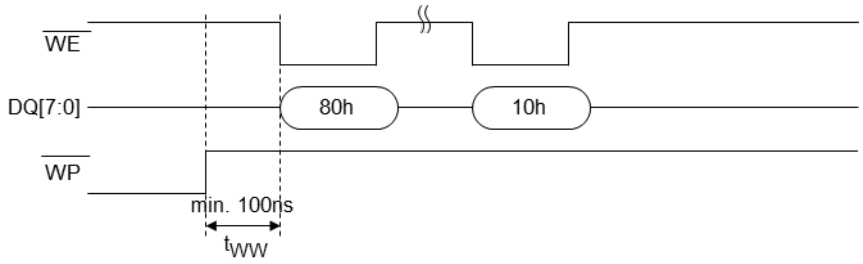
2.16. Write Protect

When $\overline{WP}$ is active low, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after t_{WW} once $\overline{WP}$ is active low.

Figure 10 describes the t_{WW} timing requirement, shown with the start of a Program command. And Figure 11 shows with the start of a Erase command.

Note that following requirements shall be applied to the other Programming and Erase sequences, e.g. Program Operation with Random Data Input, Multi Page Program Operation, Multi Block Erase Operation and etc.

1. Enable Programming



2. Disable Programming

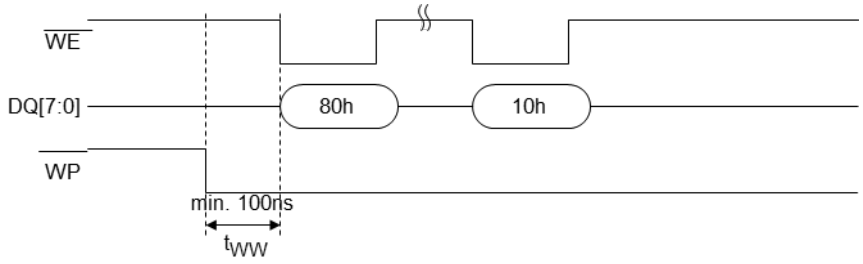
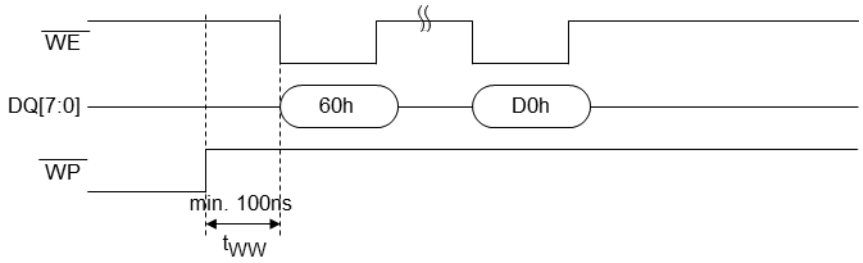


Figure 10. Write Protect timing requirements of the Program operation

1. Enable Erasing



2. Disable Erasing

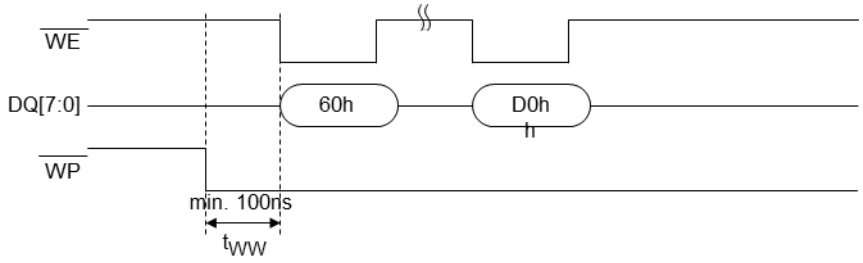


Figure 11. Write Protect timing requirements of the Erase operation

3. MEMORY ORGANIZATION

A device contains one or more targets. A target is controlled by one $\overline{CE}$ signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1.

A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of plane operations supported for the LUN. The Flash array contains a number of blocks.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages. A page is the smallest addressable unit for read and program operations.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

There are several mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, plane addressing may be used to execute additional dependent operations in parallel. Additionally, parallel page operations within a plane may be used if its functionality is supported by the device. Each of above operations shall be executed in accordance with the requirements dependent on the memory organization of the device.

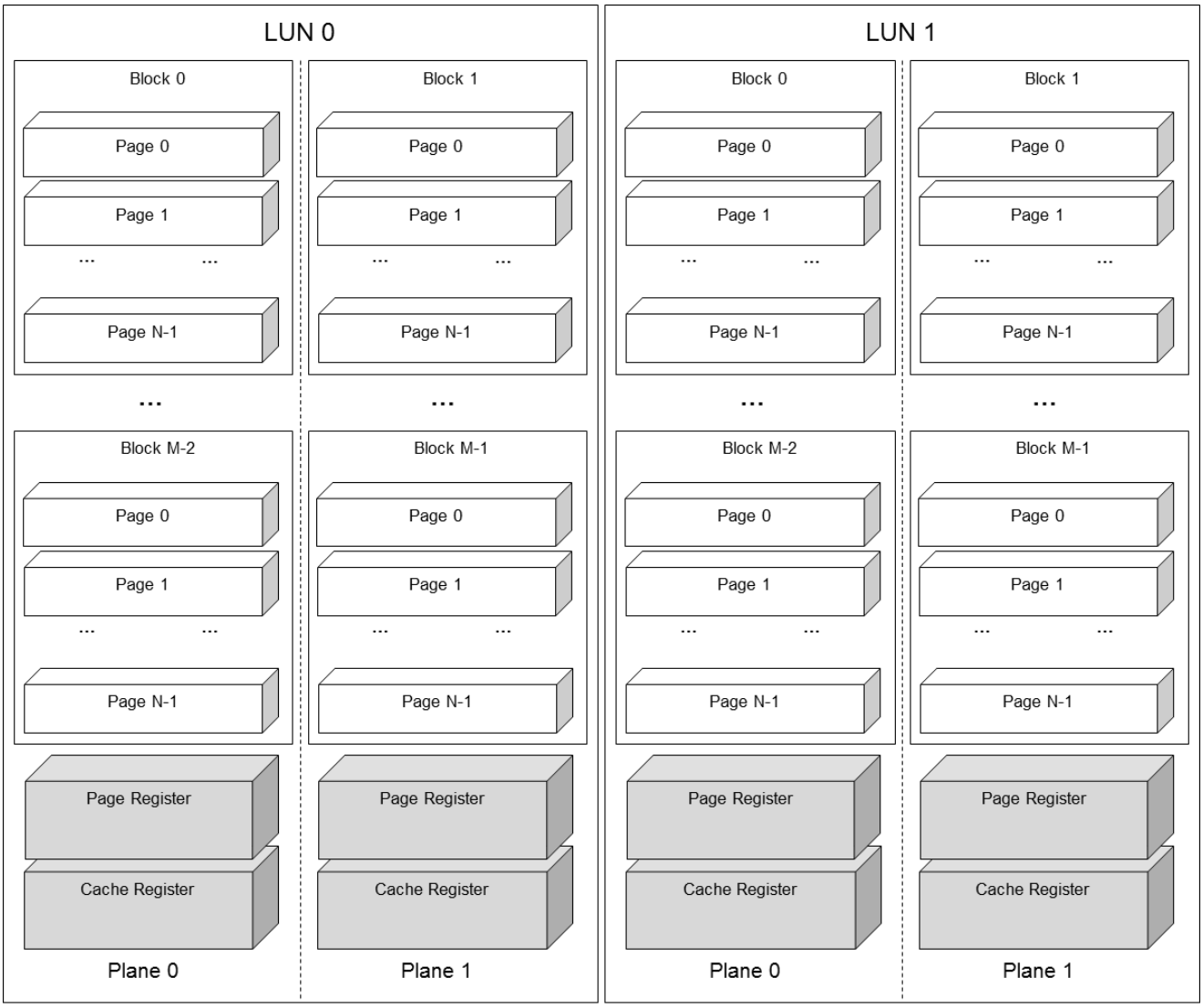


Figure 12. Target Organization

3.1. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs. When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses are not issued. For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero. The row address structure is shown in Figure 13 with the least significant row address bit to the right and the most significant row address bit to the left.

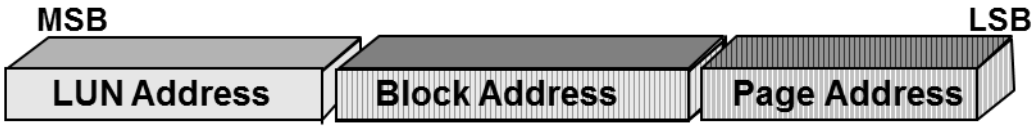


Figure 13. Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address. A host shall not access an address of a page or block beyond maximum page address or block address. The addressing of this device is shown in Figure 27.

Table 22 The addressing of this device.

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First cycle (Column address 1)	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
Second cycle (Column address 2)	L	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
Third cycle (Row address 1)	R1-7	R1-6	R1-5	R1-4	R1-3	R1-2	R1-1	R1-0
Fourth cycle (Row address 2)	R2-7	R2-6	R2-5	R2-4	R2-3	R2-2	R2-1	R2-0
Fifth cycle (Row address 3)	L	L	L	R3-4 (Note)	R3-3	R3-2	R3-1	R3-0

R1-0 to R1-7: Page address

R2-0 to R3-3: Block address

R3-4: LUN address (Note)

NOTE :

1) The least significant bit of Block address is also regarded as Plane Address bit. Refer to 3.1.1.
2) If the target of the device has only one LUN, no LUN Address bit is assigned.
3) LUN address in the above table is only for the device having multiple LUNs per a target. The LUN address is L for the device having single LUN per a target.

3.1.1. Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in Figure 14. The plane address is used when performing a multi-plane operation on a particular LUN. Regarding the restriction of address setting sequences for multi-plane operation, refer to Address Input Restrictions for Multi Page Operation in 5.3.2

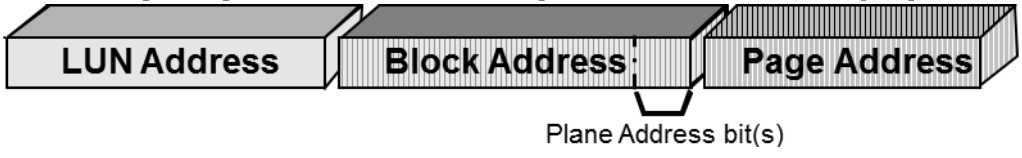


Figure 14. Position of Plane Address

3.1.2. Extended Blocks Arrangement

The device has 42 extended blocks per plane (Extended Blocks) to increase valid blocks. Extended Blocks can be accessed by the following addressing.

Table 23 Extended Blocks Arrangement for LUN #0

Row Address	Block Assignment	
000000h	Block 0(Plane 0)	LUN #0 Internal Chip (A/C) Main Blocks (2048 blocks)
000100h	Block 1(Plane 1)	
000200h	Block 2(Plane 0)	
000300h	Block 3(Plane 1)	
000400h	Block 4(Plane 0)	
000500h	Block 5(Plane 1)	
|	|	
07FE00h	Block 2046(Plane 0)	
07FF00h	Block 2047(Plane 1)	
80000h	Block 2048(Plane 0)	LUN #0 Internal Chip (A/C) Extended Blocks (42x2 blocks)
80100h	Block 2049(Plane 1)	
|	|	
85200h	Block 2130(Plane 0)	
85300h	Block 2131(Plane 1)	
85400h – 0FFFFFh	**Address Gap**	

Table 24 Extended Blocks Arrangement for LUN #1

100000h	Block 4096(Plane 0)	LUN #1 Internal Chip (B/D) Main Blocks (2048 blocks)
100100h	Block 4097 (Plane 1)	
100200h	Block 4098(Plane 0)	
100300h	Block 4099(Plane 1)	
100400h	Block 4100(Plane 0)	
100500h	Block 4101(Plane 1)	
|	|	
17FE00h	Block 6142(Plane 0)	
17FF00h	Block 6143(Plane 1)	
180000h	Block 6144 (Plane 0)	LUN #1 Internal Chip (B/D) Extended Blocks (42x2 blocks)
180100h	Block 6155 (Plane 1)	
|	|	
185200h	Block 6226(Plane 0)	
185300h	Block 6227(Plane 1)	
185400h – FFFFFFh	**Address Gap**	

NOTE :

1) Table 24 is only for the device having multiple LUNs per a target and shall be ignored for the device having single LUN per a target.

3.2. Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

3.2.1. Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure 15, of the first or last page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

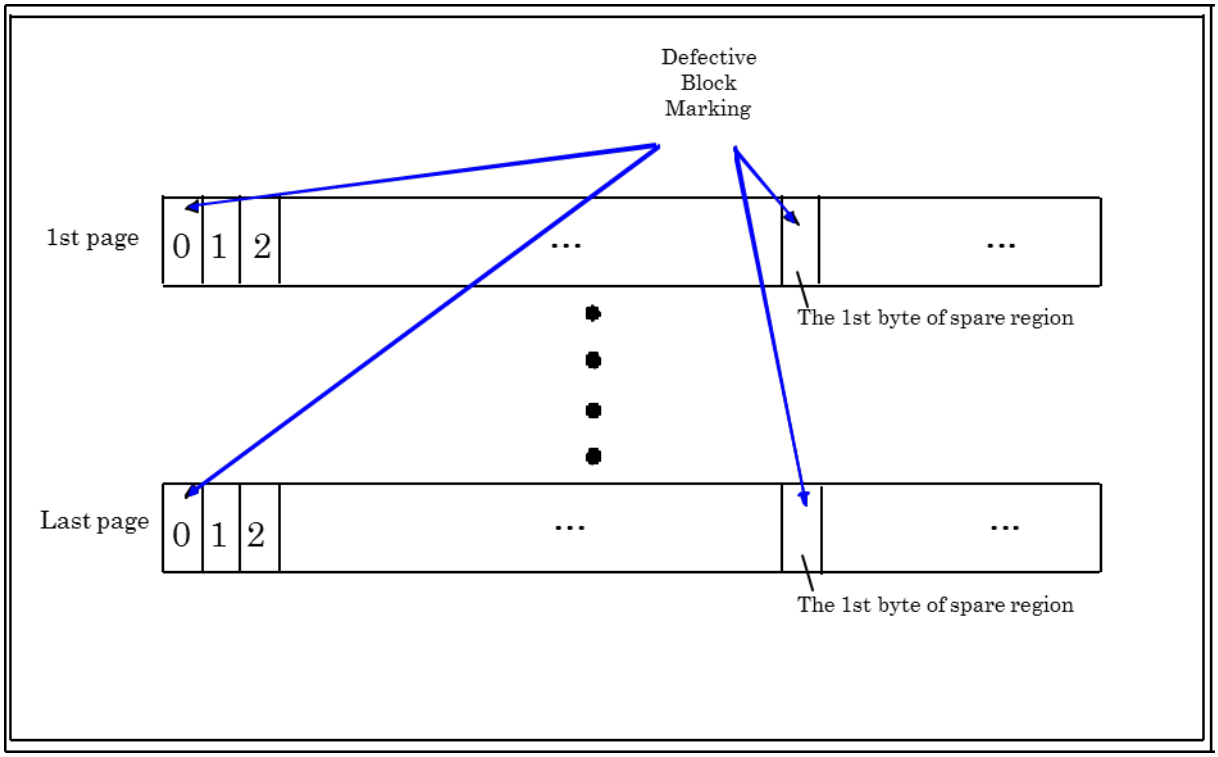


Figure 15. Area marked in first or last page of block indicating defect

3.2.2. Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 16 outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. All pages in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or last page of the block. The host shall check the Defective Block Marking location of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE :
Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

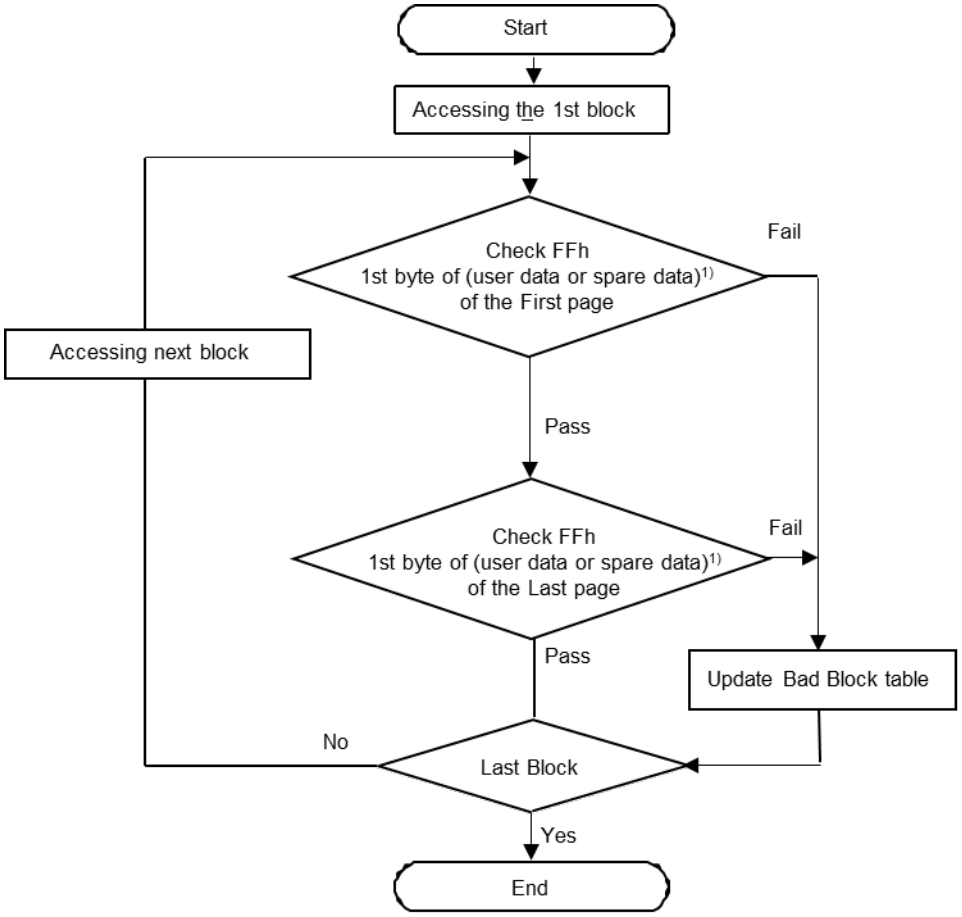


Figure 16. Flow chart to create initial invalid block table

NOTE :
1) The location for the initial invalid block may vary depending on vendors

4. FUNCTION DESCRIPTION

4.1. Discovery and Initialization

4.1.1. Power-on/off sequence

Power-on/off sequence are necessary to follow the timing sequence shown in the figure below. The device internal initialization starts with FFh command after the power supply reaches an appropriate level and wait 100us. During the initialization, the device RY/$\overline{BY}$ signal indicates the Busy state and the device consumes power-on initialize current which is defined on DC characteristics table. The acceptable commands are FFh or 70h during this period. The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.

During Power-off sequence, when Vcc level is less than 2.5V, Vcc must set below 0.5V and stay 1ms at least.

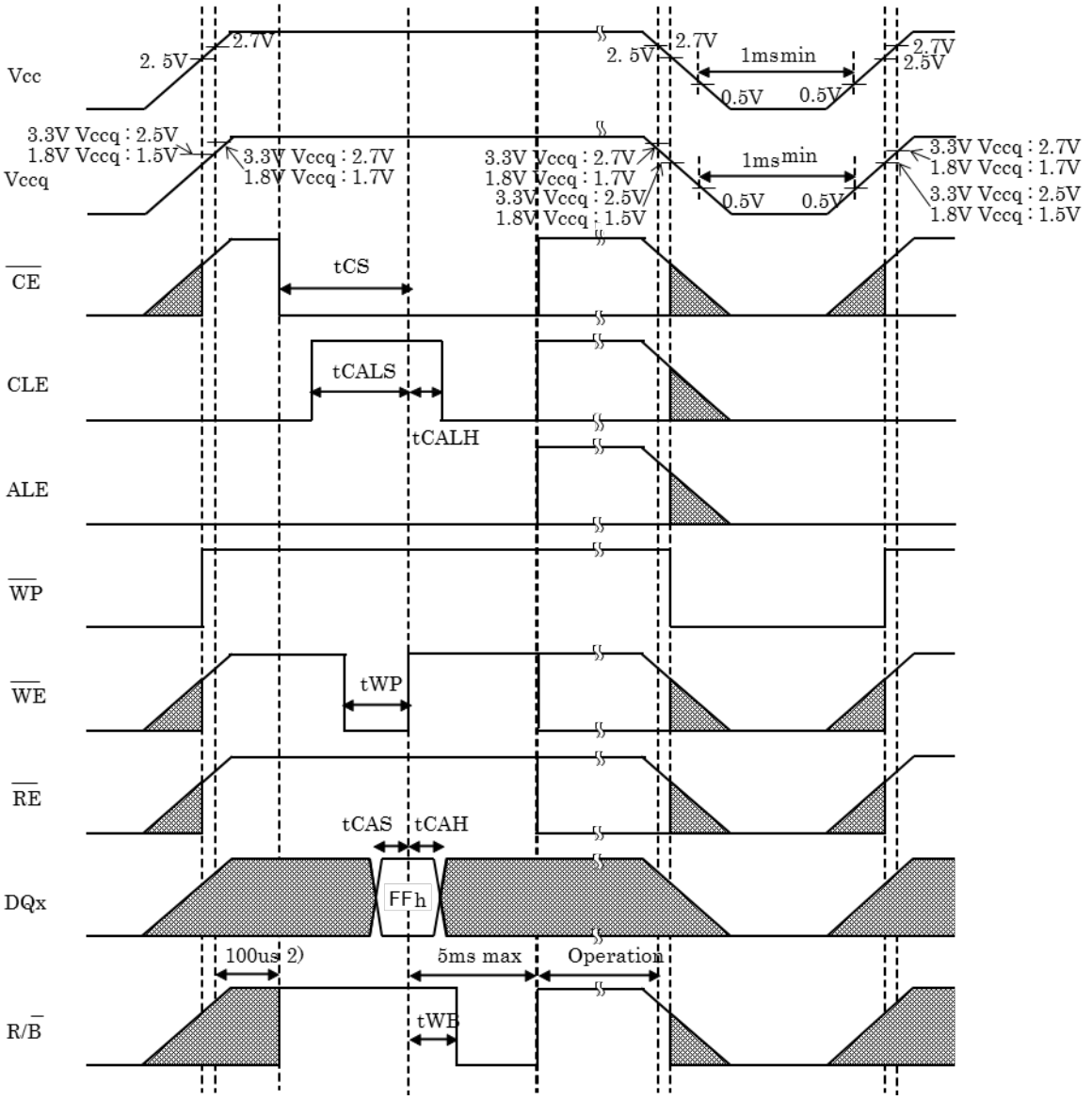


Figure 17. Initialization Timing

NOTE:

1) During the initialization, the device consumes a maximum current of I_{CC1}.

The R/$\overline{B}$ signal becomes valid after 100us since both VCC and VCCQ reaches 2.7V (1.7V for 1.8V VCCQ).

4.1.2. V_{PP} Initialization

To enable V_{PP}, following conditions shall be satisfied:

- V_{CC} must be successfully ramped prior to the start of ramping V_{PP}.
- V_{PP} shall be ramped to meet its valid range prior to issuing the SET FEATURES (EFh) command to enable the V_{PP} functionality. The valid range is specified in Table 10 and Table 11.
- The SET FEATURES (EFh) command shall be issued after the device is successfully powered-on.
- Once V_{PP} is enabled, V_{PP} shall be maintained to keep the valid range.

Regarding power-down when V_{PP} is enabled , following conditions shall be satisfied:

- V_{PP} must go down to 0V before VCC ramping down.
- The device shall not be turned to power-down during busy period.

4.1.3. Single Channel Discovery

Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command (FFh) to the target. Following the reset, the host should then issue the Read ID command to the target. If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected. If the ID values are not returned or any error is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done.

4.1.4. Dual Channel Discovery

If there are dual channel in a package, host should issues the Reset command (FFh) to both channels to initialize all LUNs. Note that the relationships are described between several $\overline{CE}$ and dual channels. See the Table 4 for further information.

The sequence of initialization is the same as the sequence for single channel discovery. Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command (FFh) to the target. Following the reset, the host should then issue a Read ID command to the target. If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected. If the ID values are not returned or any error is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done.

4.2. Mode Selection

After initialization, the SDR interface is active for all targets on the device. Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target. The interface can be changed by Set Feature Command defined in section 5.2.9.

Table 25 describes the bus state for the Toggle DDR1.0. Command, address and data are all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ pins. Host reads or writes data to the device using DQS signal. And data are latched on both falling and rising edges of DQS on data input.

Table 25 Toggle DDR1.0 Interface Mode Selection

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$
Command Input	H	L	L	↑	H	X(1)	X
Address Input	L	H	L	↑	H	X	X
Command Input	H	L	L	↑	H	X	H
Address Input	L	H	L	↑	H	X	H
Data Input	L	L	L	H	H	↓↑	H
Data Output	L	L	L	H	↓	↓↑	X
During Read(Busy)	X	X	X	X	H	X	X
During Program(Busy)	X	X	X	X	X	X	H
During Erase(Busy)	X	X	X	X	X	X	H
Write Protect	X	X	X	X	X	X	L
Stand-by	X	X	H	X	X	X	0V/Vcc(2)
Bus Idle	L	L	L	H	H	H/L	H

NOTE:

1) X can be VIL or VIH.

2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Table 26 describes the bus state for the SDR interface. Command, address and data are all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ pins. Host reads the data to the device using $\overline{RE}$ signal and writes the data to the device using $\overline{WE}$ signal.

Table 26 SDR Interface Mode Selection

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	H
Address input	L	H	L	↑	H	*
Serial Data Output	L	L	L	H	↓	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Stand-by	*	*	H	*	*	0 V/V_{CC}
Bus Idle	L	L	L	H	H	H

NOTE:

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

4.2.1. Toggle DDR1.0 General Timing

4.2.1.1. Command Latch Cycle

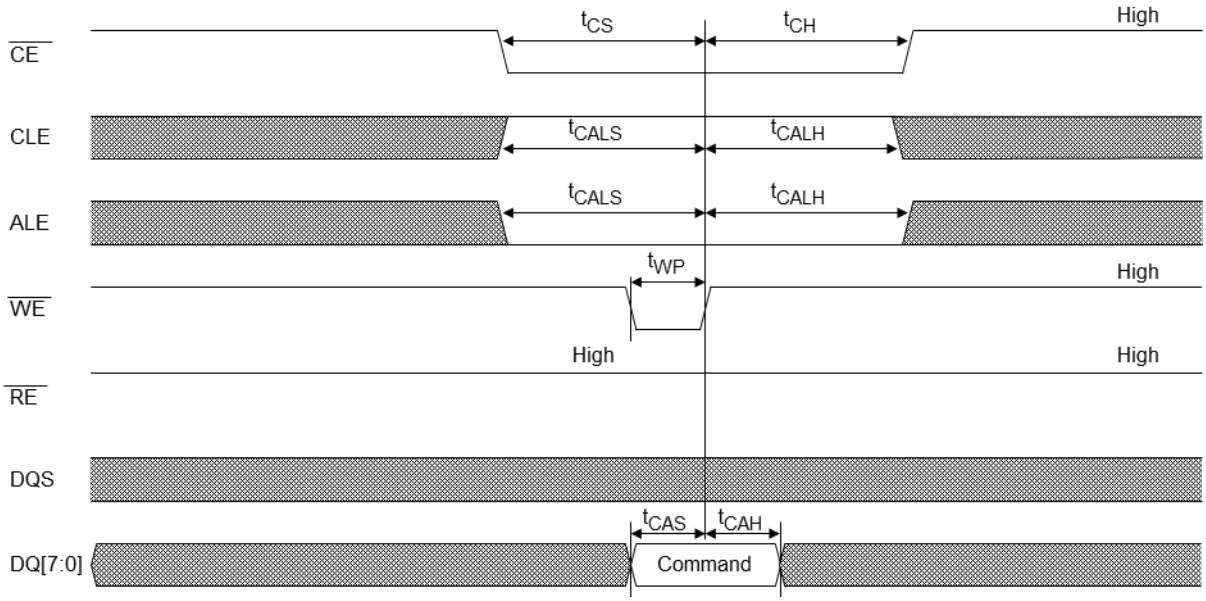


Figure 18. Command Latch Cycle Timing

NOTE :
1) Command Information is latched by $\overline{WE}$ going 'High', when $\overline{CE}$ is 'Low', CLE is 'High', and ALE is 'Low'.
2) DQS shall be set to Low when these commands (85h, 10h, 11h, or 15h) are input.

4.2.1.2. Address Latch Cycle

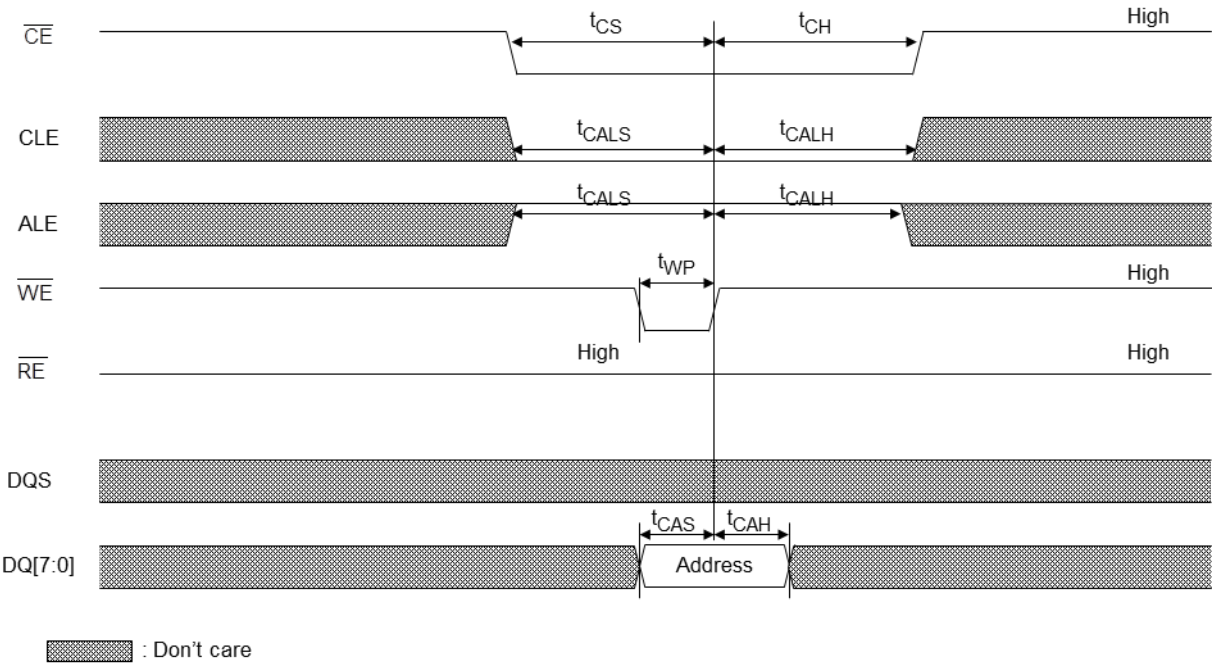


Figure 19. Address Latch Cycle Timing

NOTE :
1) Address Information is latched by $\overline{WE}$ going 'High', when $\overline{CE}$ is 'Low', CLE is 'Low', and ALE is 'High'.

4.2.1.3. Basic Data Input Timing

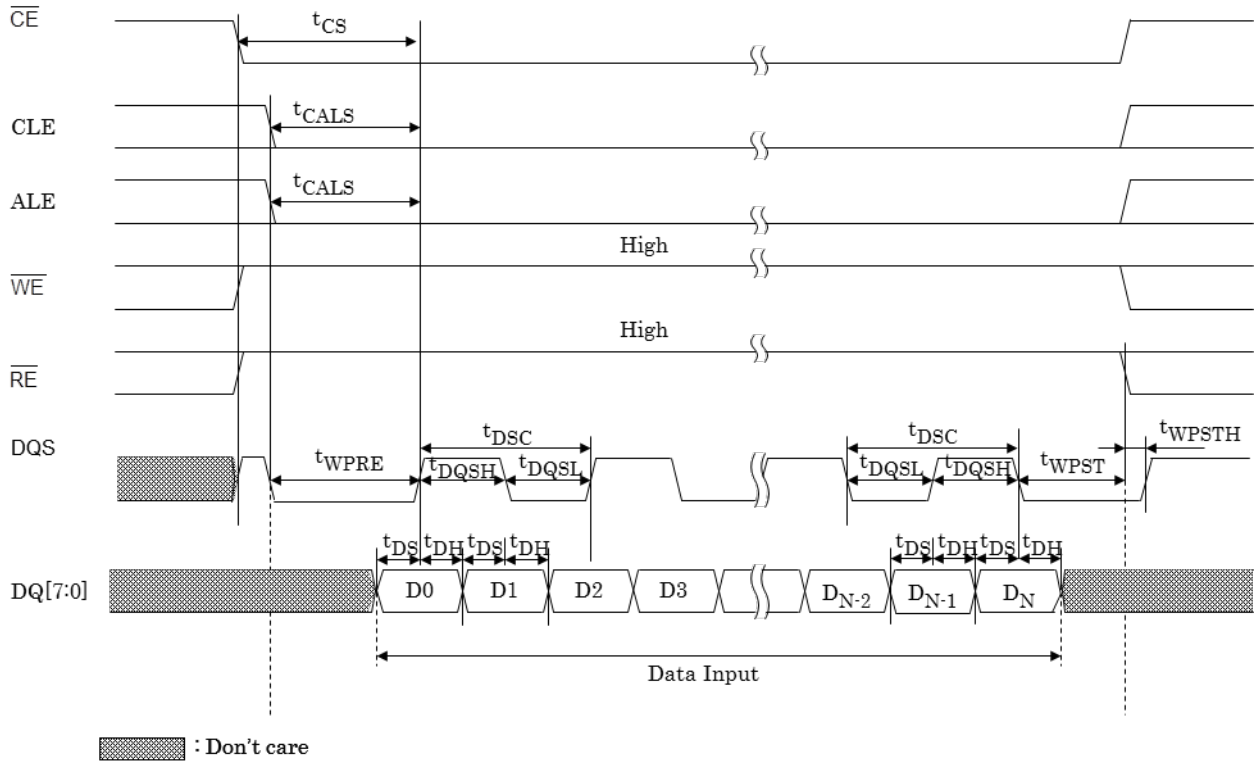


Figure 20. Basic Data Input Timing

NOTE:

1) DQS, and Data input buffers are turned-on when $\overline{CE}$ and DQS goes 'Low' and Data inputs begin with DQS, toggling simultaneously.
2) ALE and CLE should not toggle during t_{WPRE} period regardless of t_{CALS}.
3) DQS and Data input buffers are turned-off if either CLE or $\overline{CE}$ goes 'High'.
4) The least significant bit of the column address shall always be zero.
5) DQS, shall be either high or low before data-input condition is set.

4.2.1.4. Basic Data Output Timing

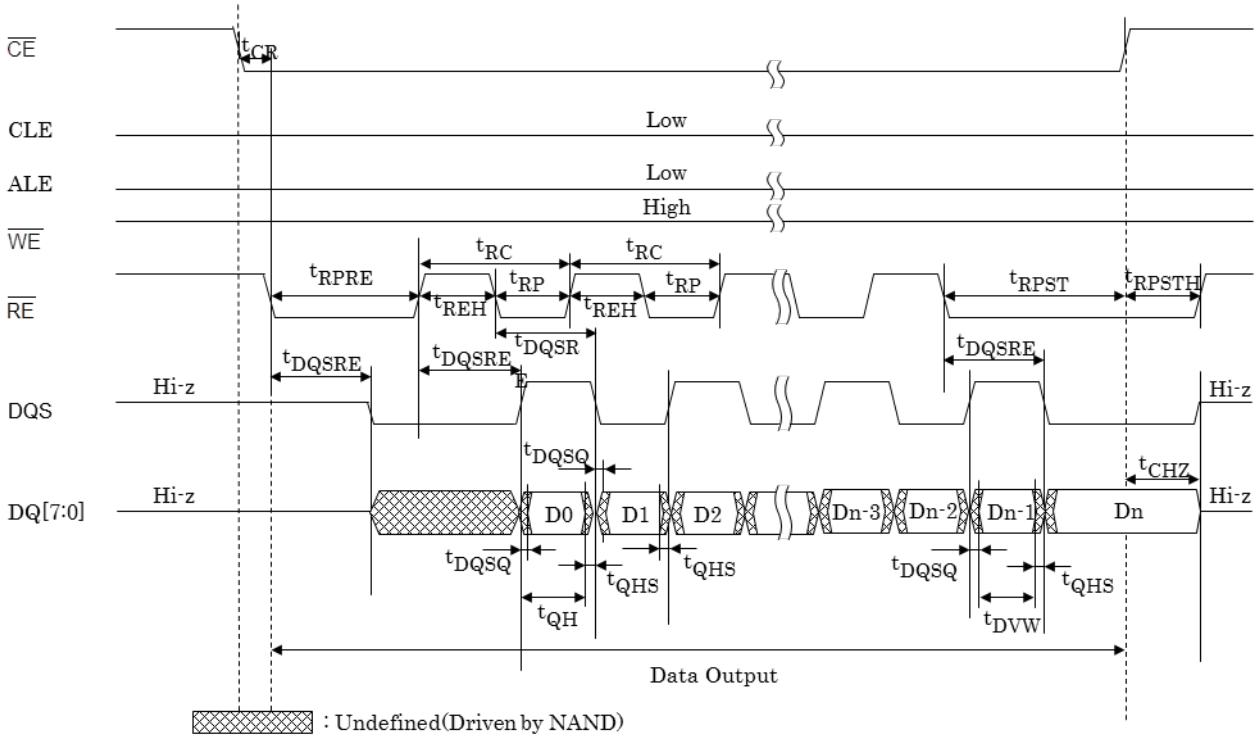


Figure 21. Basic Data Output Timing

NOTE:

1) DQS, and DQ drivers are turned-on when $\overline{CE}$ and $\overline{RE}$ goes Low for data out operation.
2) ALE and CLE should not toggle during t_{RPRE} period regardless of t_{CALS}.
3) DQS and DQ drivers turn from valid to high-z if either CLE or $\overline{CE}$ goes high.
4) The least significant bit of the column address shall always be zero.

4.2.1.5. Read ID Operation

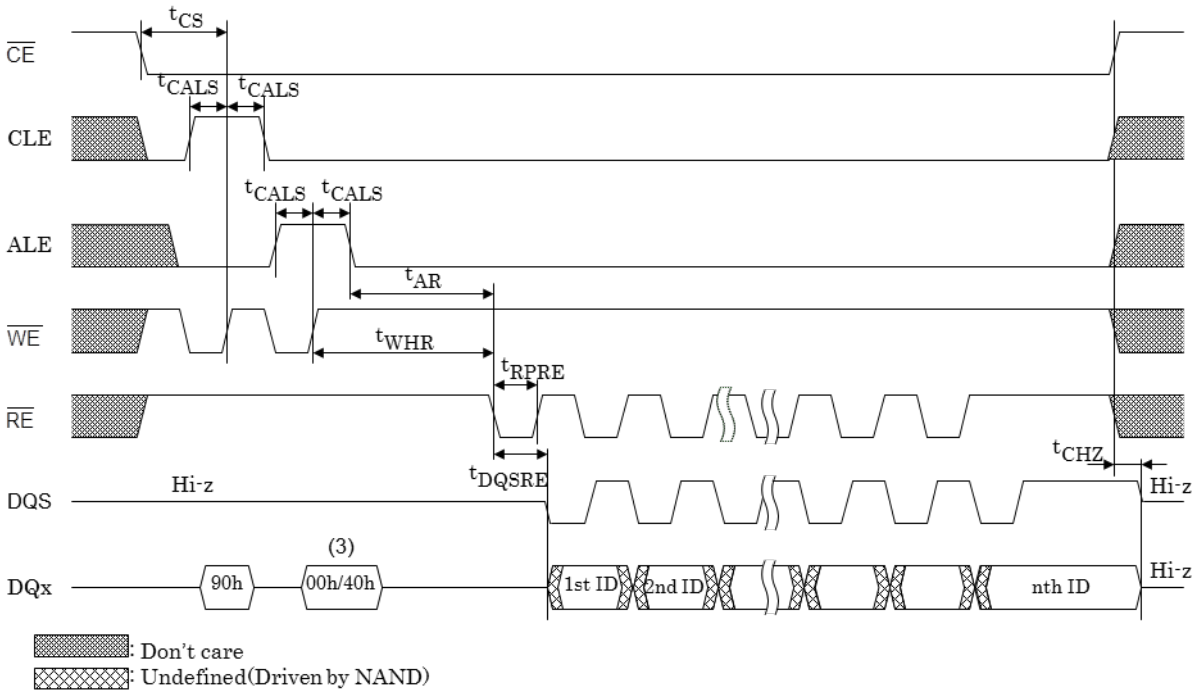


Figure 22. Read ID Operation Timing

NOTE:

1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, READ ID operation repeats each data byte twice, so that READ ID timing becomes identical to that conventional NAND
2) DQS and DQ drivers turn from valid to high-z when $\overline{CE}$ or CLE goes high.
3) Address 00h is for Toshiba conventional NAND and 40h is for new JEDEC ID information.

4.2.1.6. Status Read Cycle

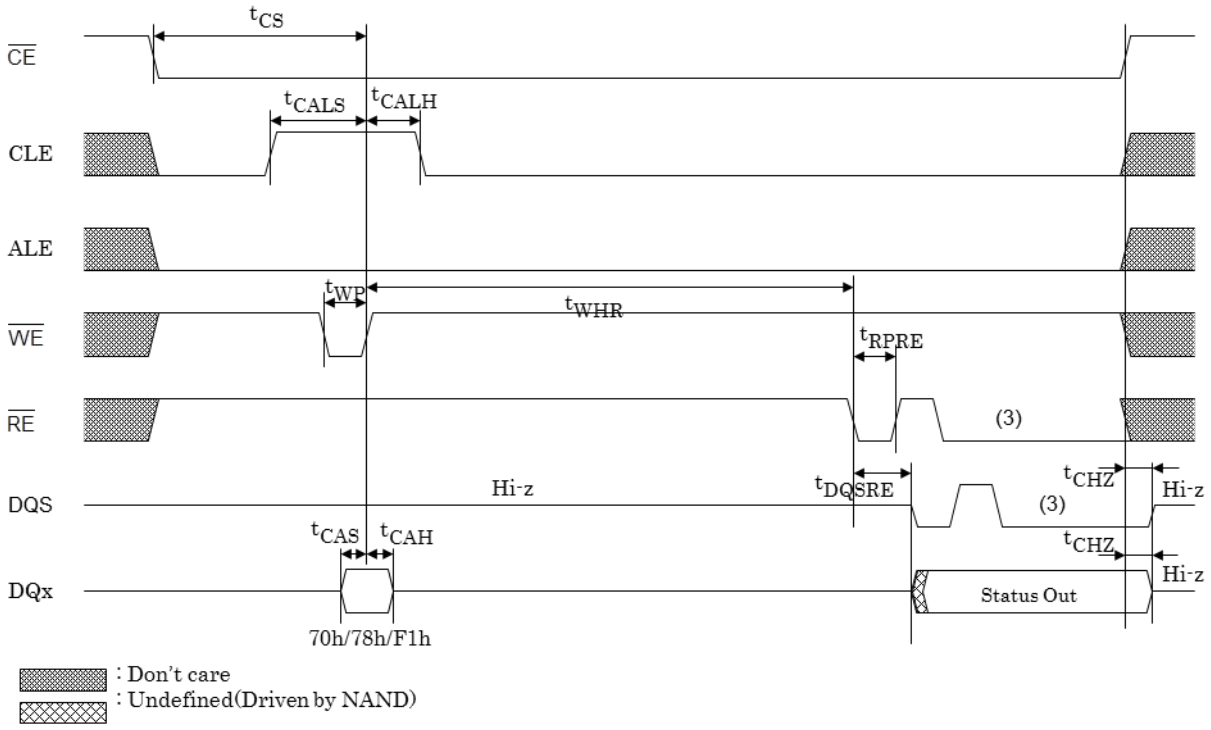


Figure 23. Status Read Cycle Timing

NOTE:

1) It is required that "Status read" outputs are read by using low- or high-going edges of DQS, although the output would repeat samevalue if the device internal status doesn't change.
2) DQS and Data out buffers turn from valid value to high-z when $\overline{CE}$ or $\overline{CLE}$ goes high.
3) $\overline{RE}$ can toggle more than once.
4) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure. tWHR is defined by /WE High to /RE Low after row address setting.

4.2.1.7. Set Feature

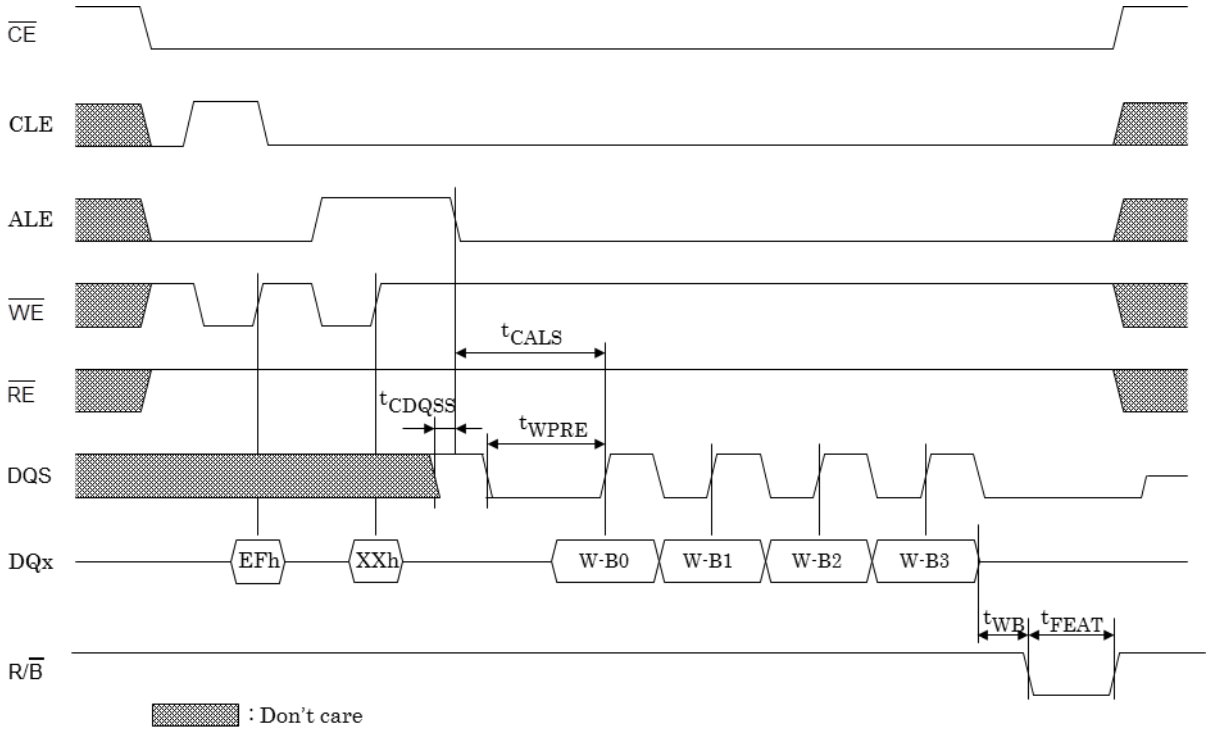


Figure 24. Set Feature Timing

4.2.1.8. Get Feature

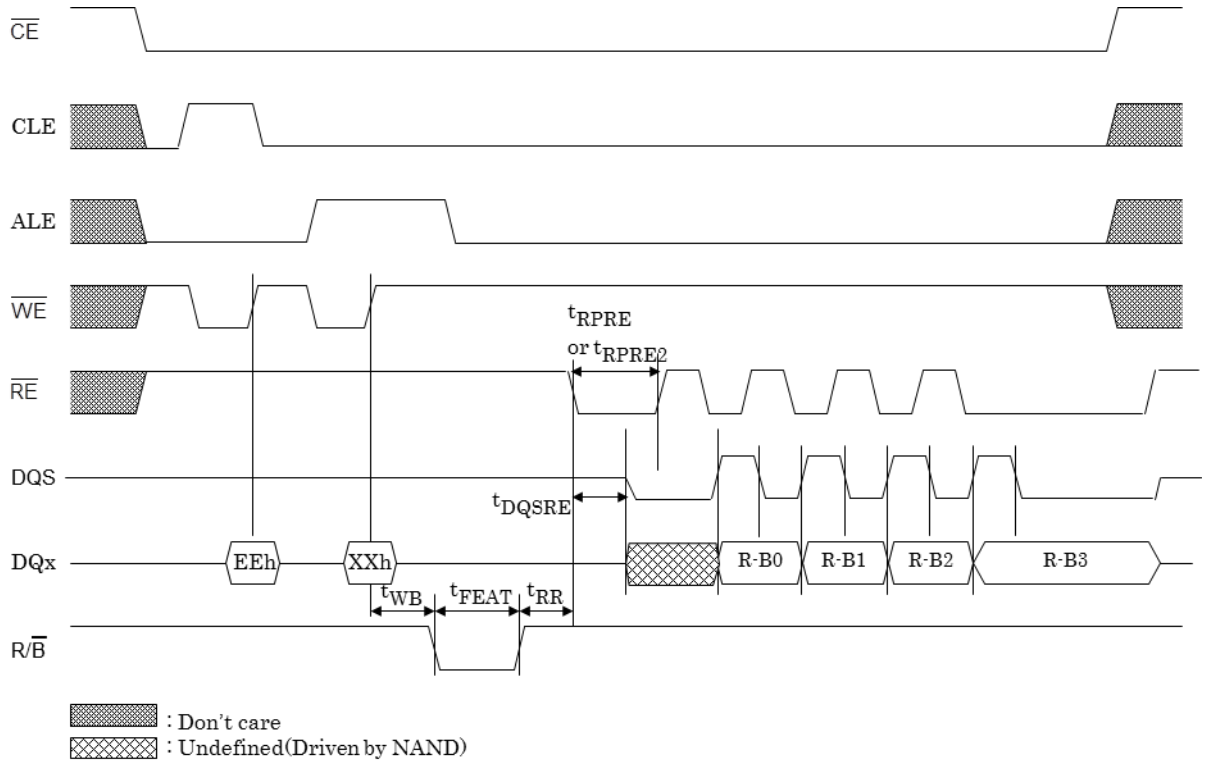


Figure 25. Get Feature Timing

4.2.1.9. Page Read Operation

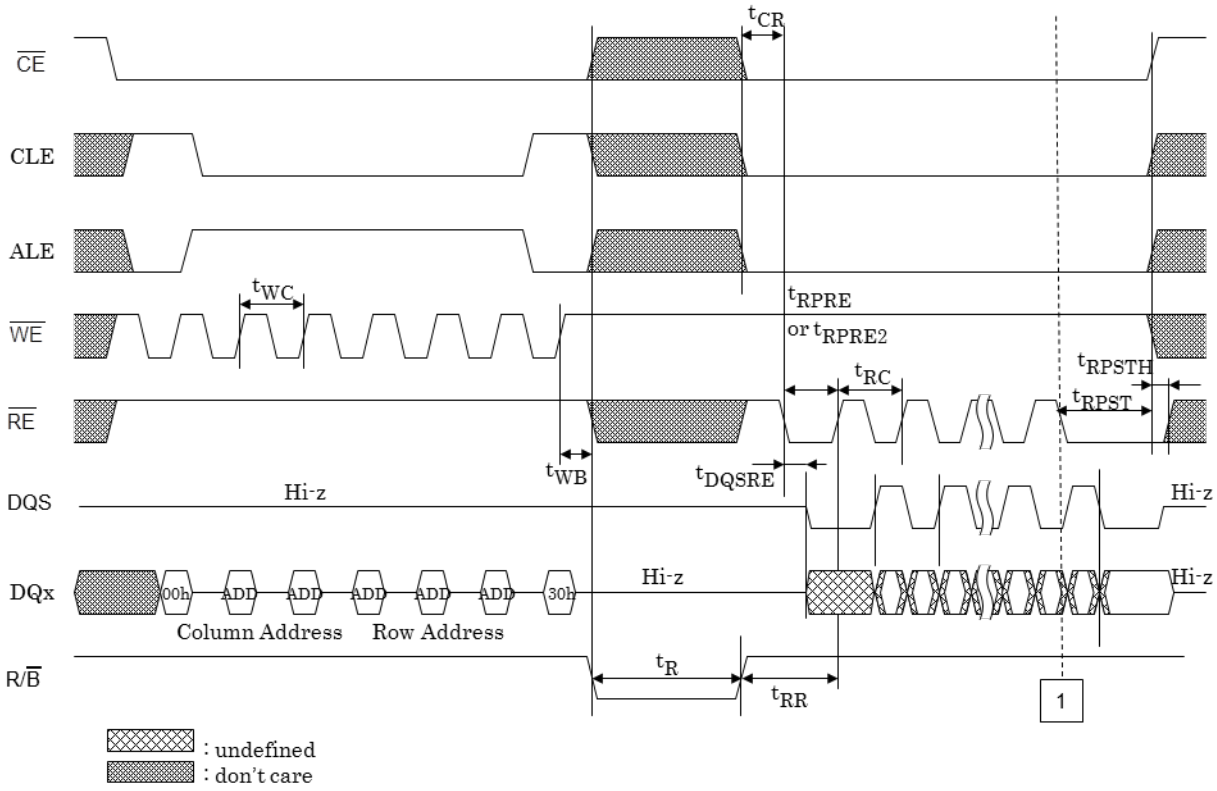


Figure 26. Page Read Operation Timing

NOTE:

1) During Busy Period, $\overline{RE}$ shall not be toggled although it may vary when the chip is disabled via $\overline{CE}$ high or the chip is de-selected via asserting LUN address of the other chip at interleave operation or Status Read Operation is performed.

Read Hold Operation with $\overline{CE}$ High is below

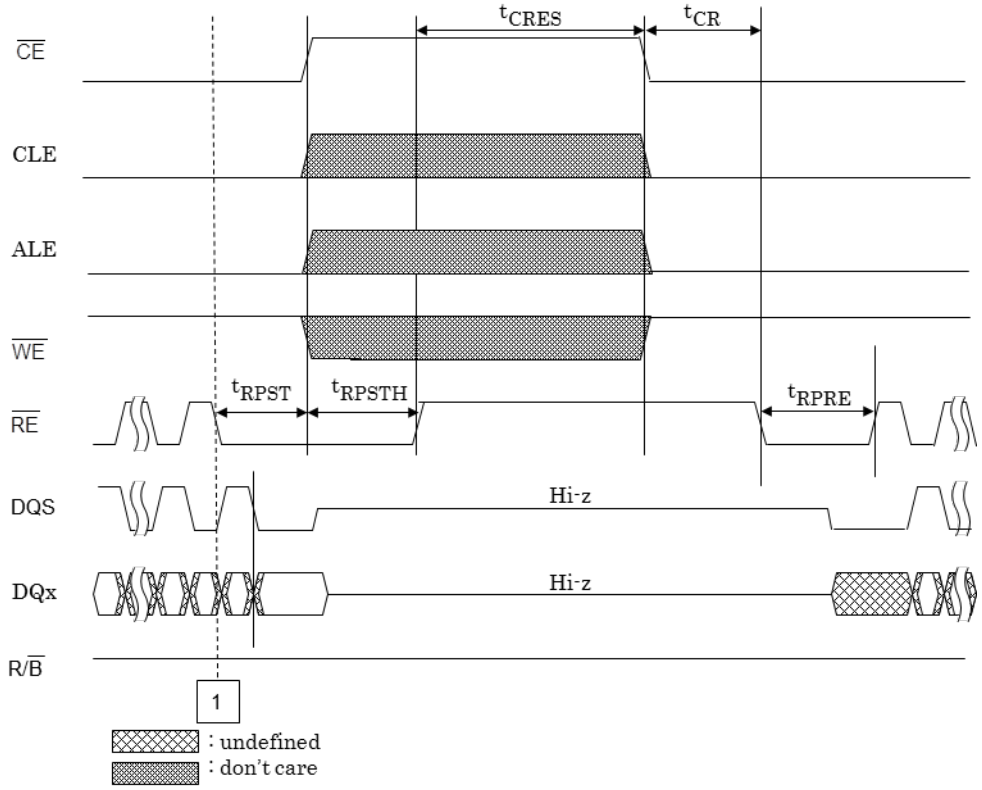


Figure 27. Read Hold Operation with $\overline{CE}$ high

4.2.1.10. Page Program Operation

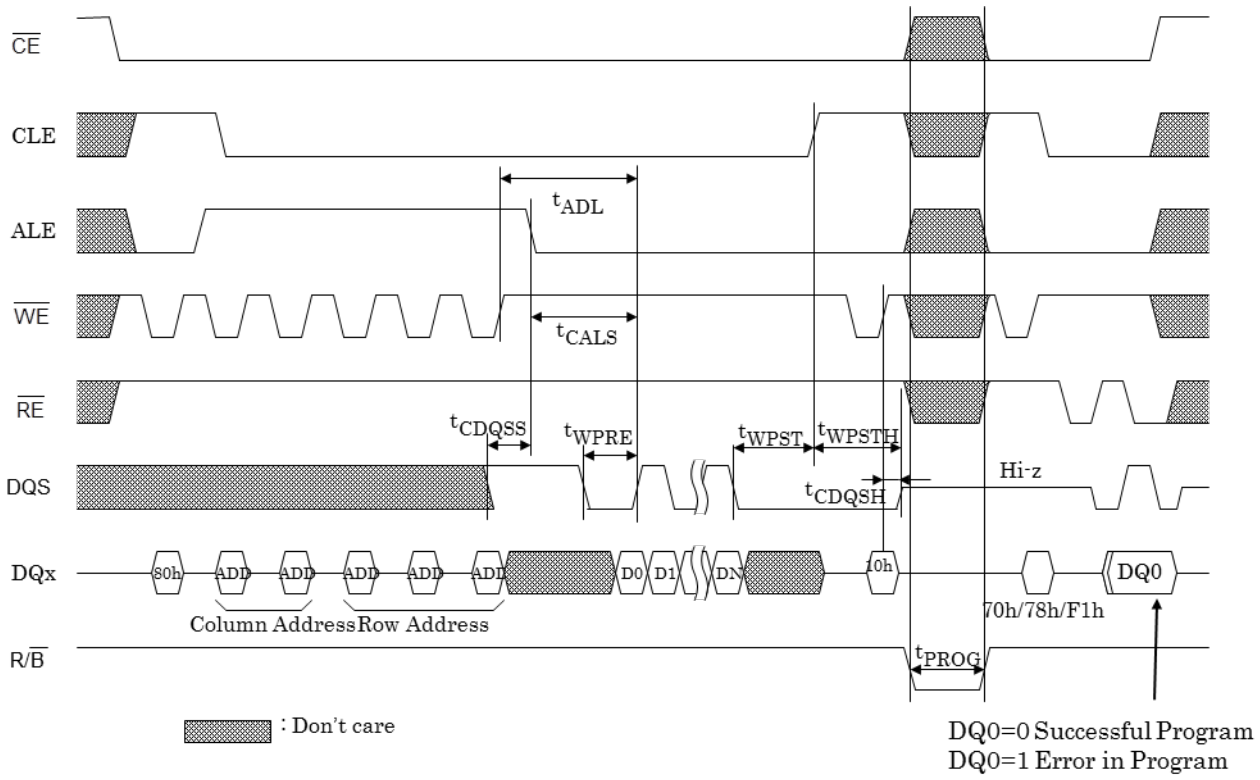


Figure 28. Page Program Operation Timing

NOTE:

1) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.

4.2.2. SDR General Timing

4.2.2.1. Command Latch Cycle

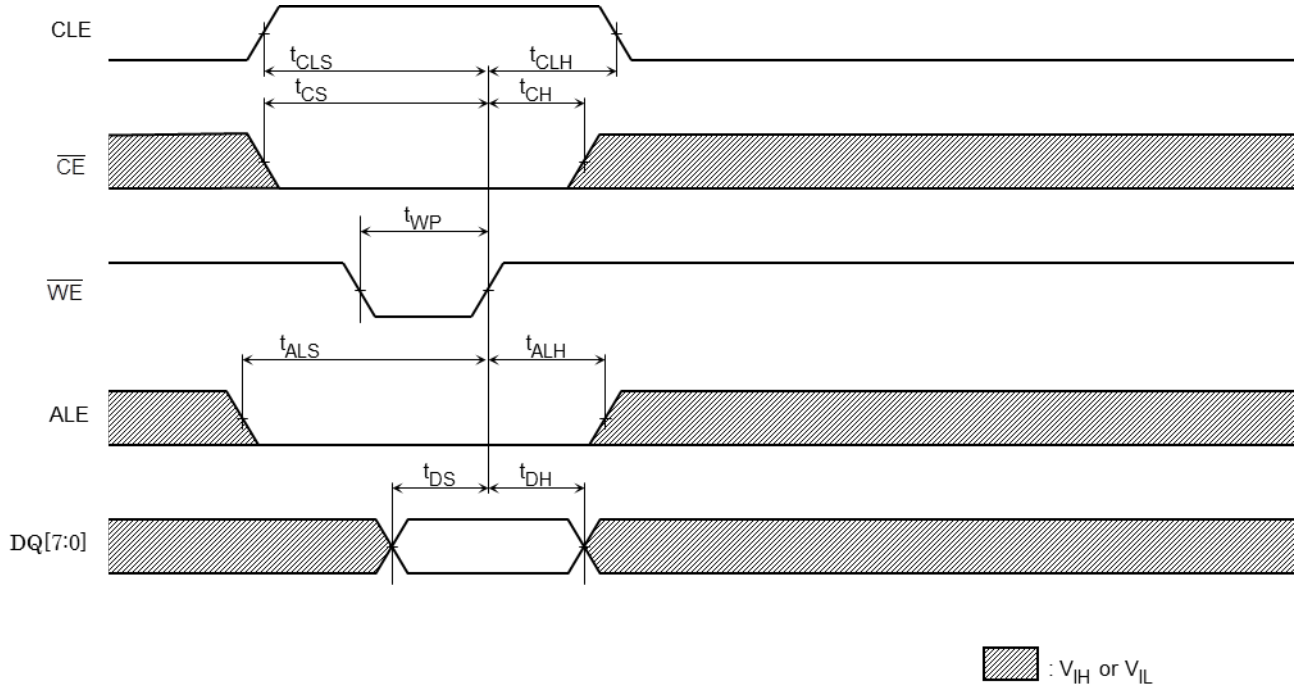


Figure 29. Command Latch Cycle Timing

4.2.2.2. Address Latch Cycle

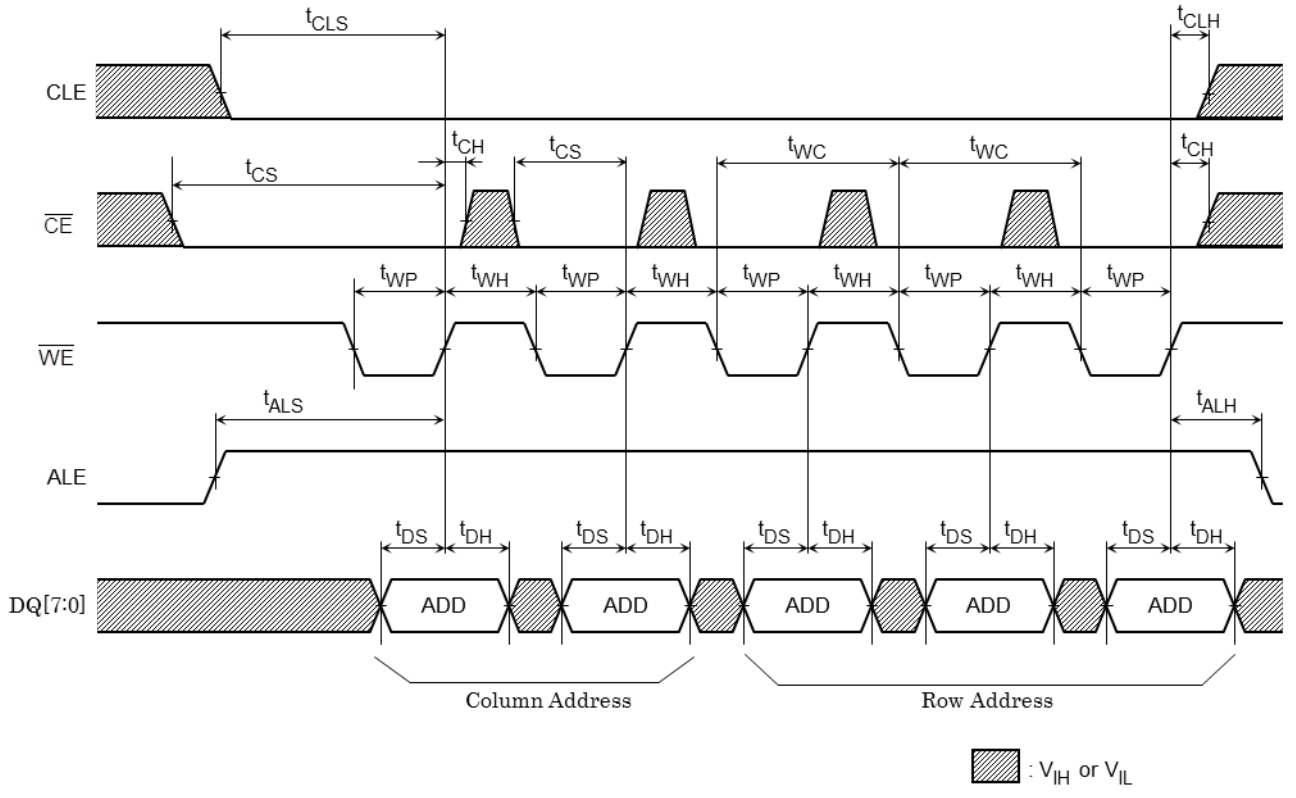


Figure 30. Address Latch Cycle Timing

4.2.2.3. Basic Data Input Timing

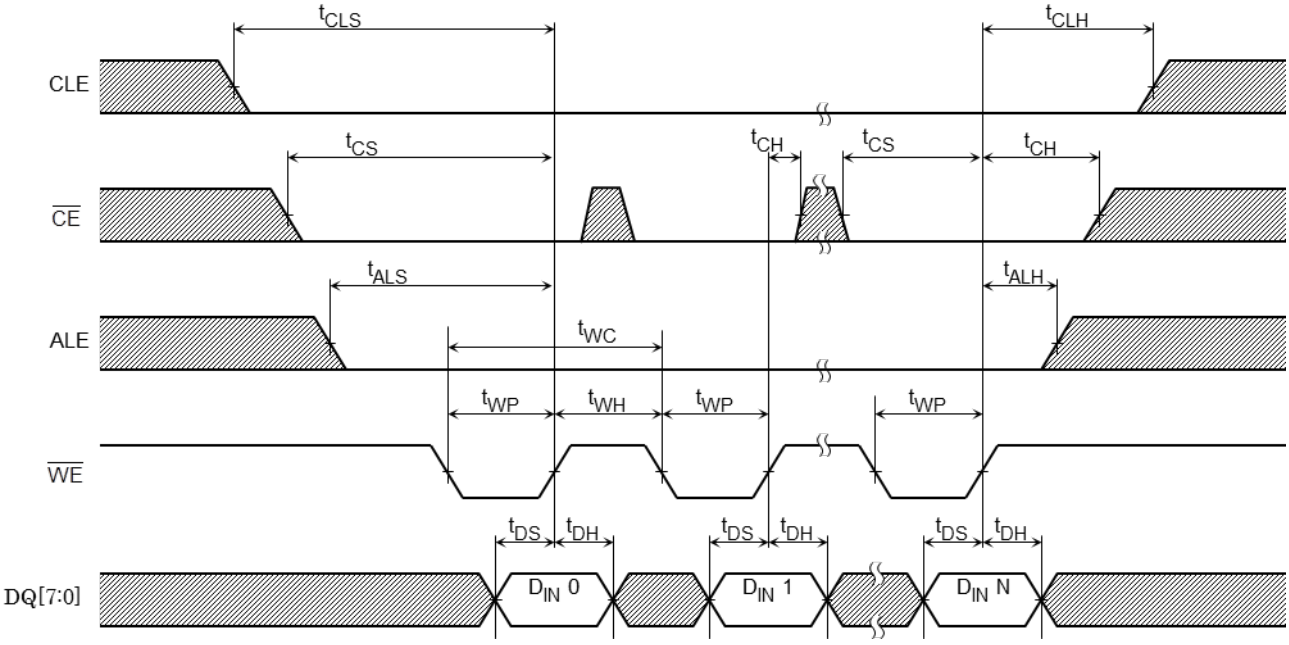


Figure 31. Basic Data Input Timing

4.2.2.4. Basic Data Output Timing

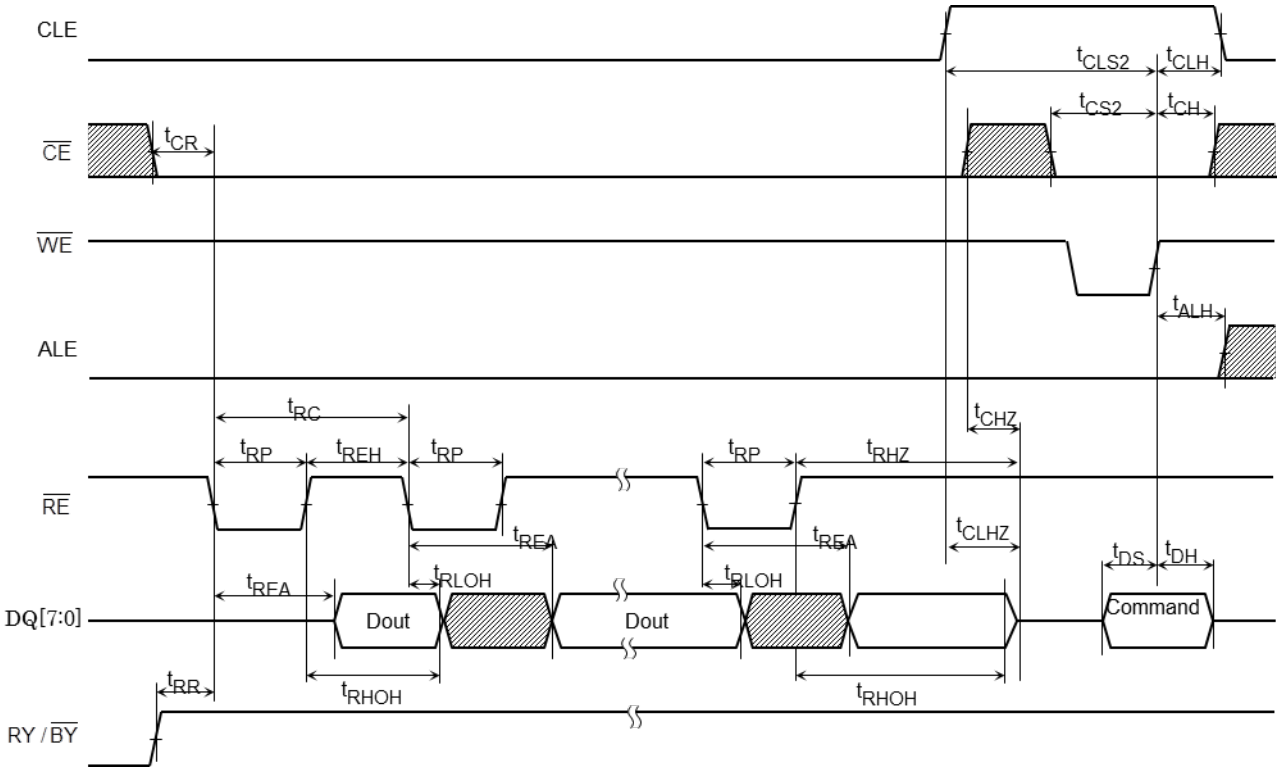


Figure 32. Basic Data Output Timing

4.2.2.5. Read ID Operation

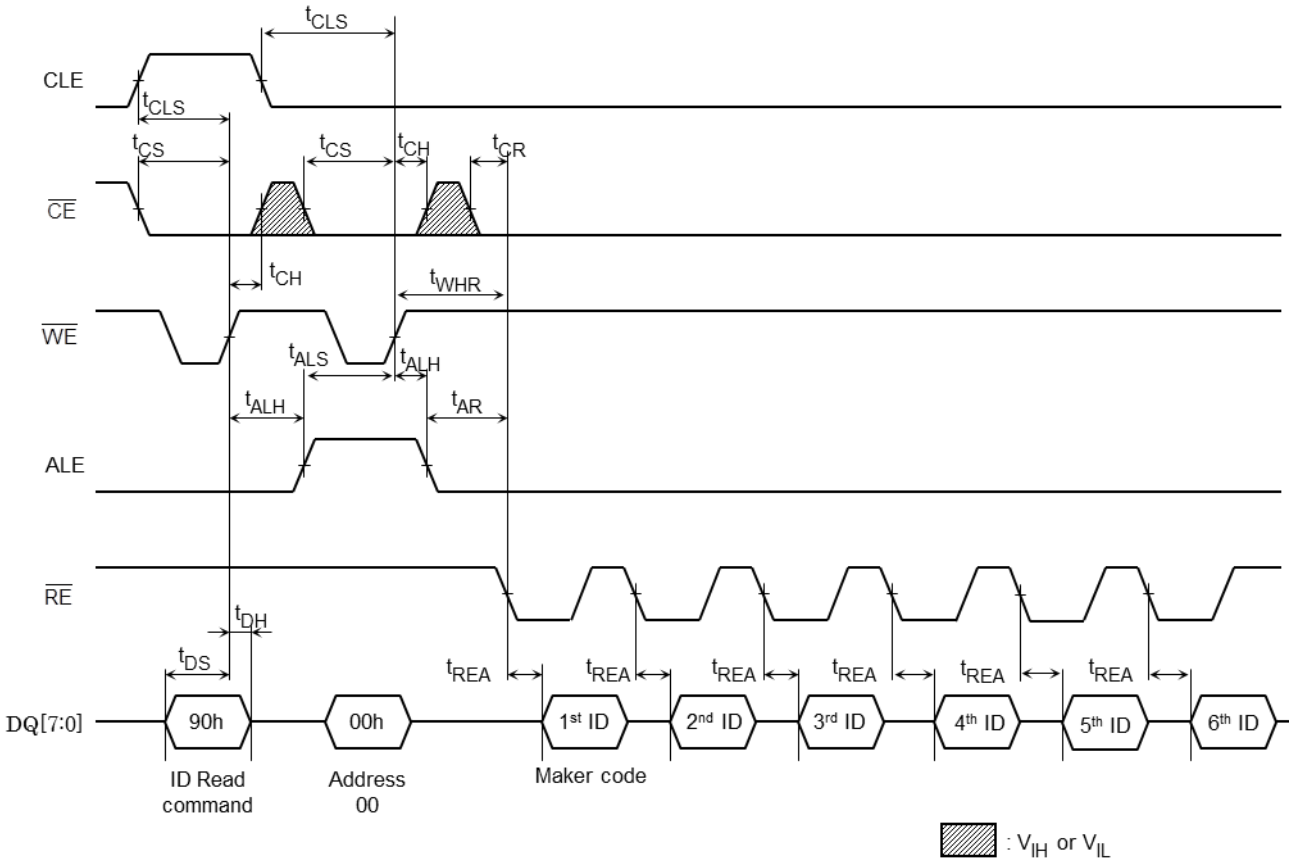


Figure 33. Read ID Operation Timing

4.2.2.6. Status Read Cycle

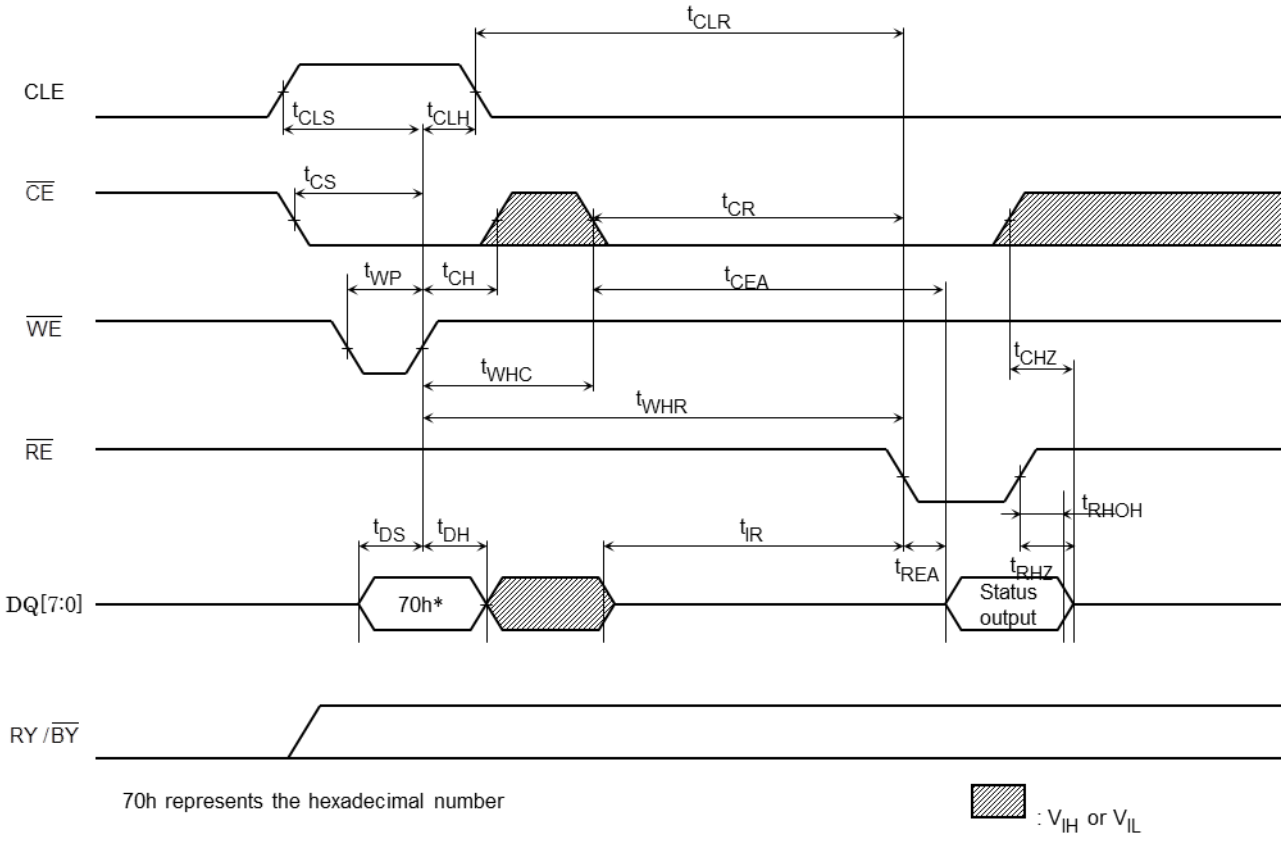


Figure 34. Status Read Cycle Timing

4.2.2.7. Set Feature

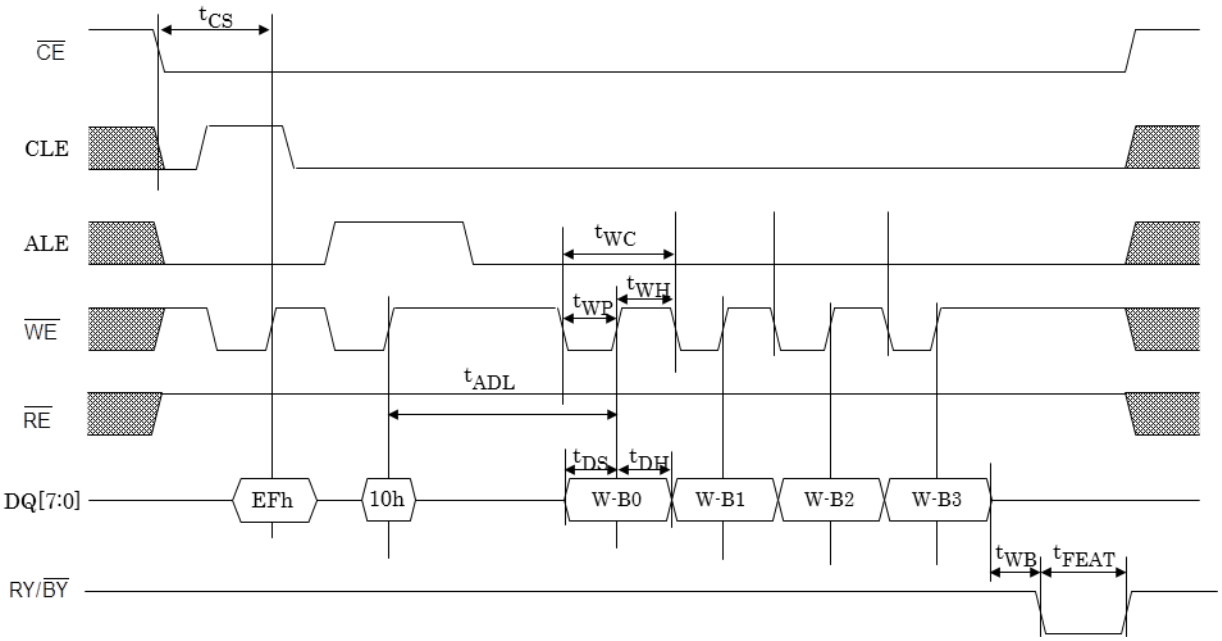


Figure 35. Set Feature Timing

4.2.2.8. Get Feature

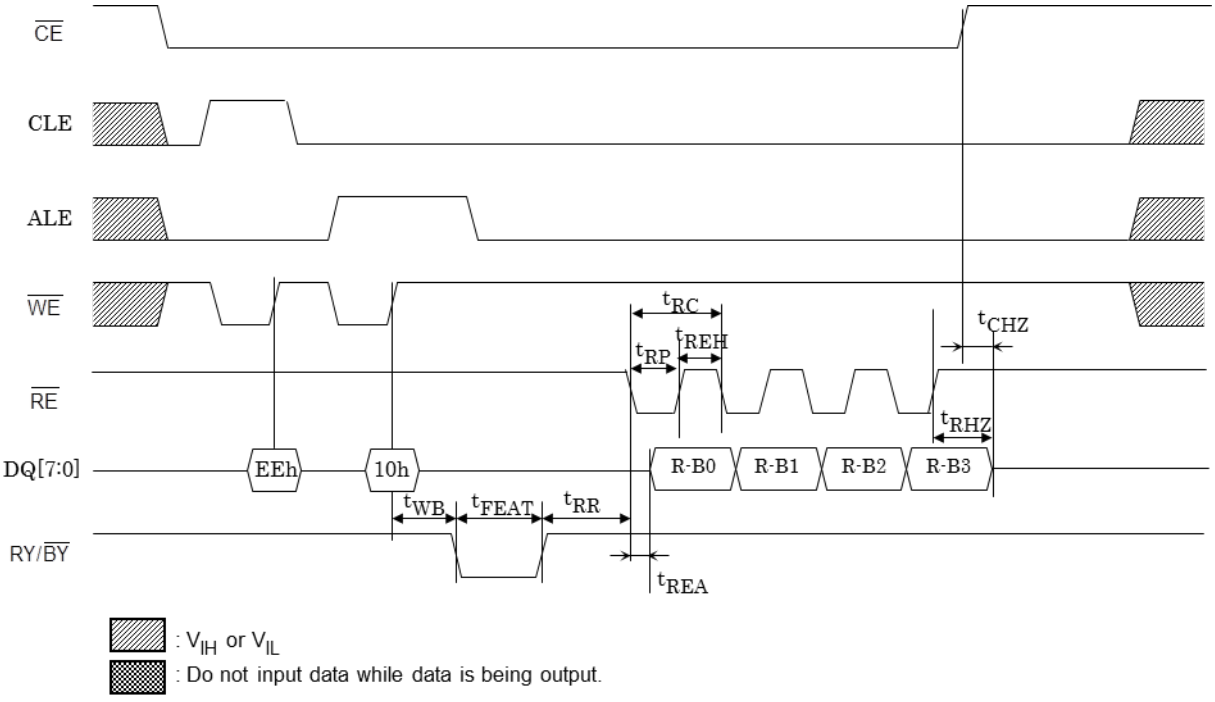


Figure 36. Get Feature Timing

4.2.2.9. Page Read Operation

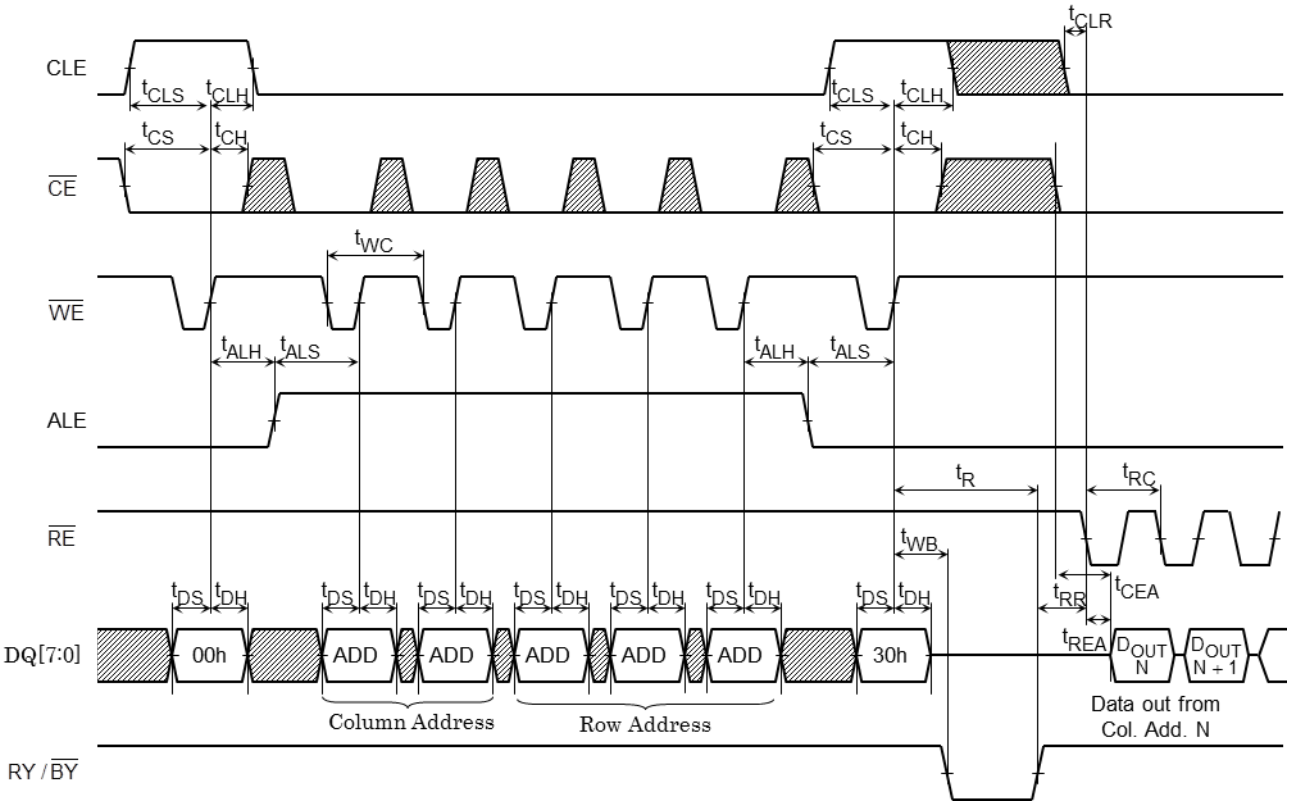


Figure 37. Page Read Operation Timing

4.2.2.10. Page Program Operation

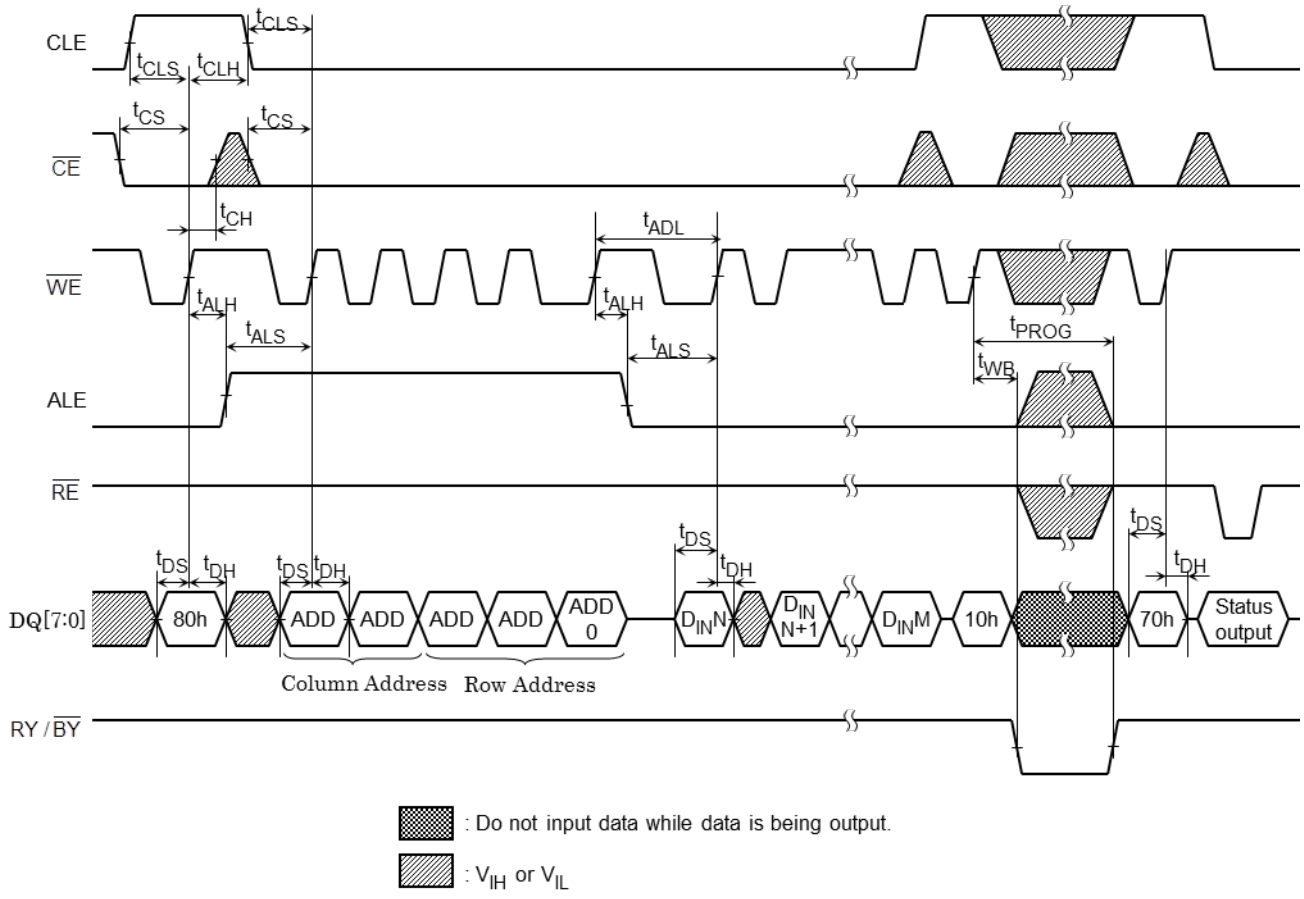


Figure 38. Page Program Operation Timing

4.3. AC Timing Characteristics

4.3.1. Timing Parameters Description

Table 27 Timing Parameters Description
Toggle DDR1.0

Parameter	Description
t_R	Data Transfer from Flash array to Register
t_{PROG}	Program Time
t_{BERASE}	Erase Time
t_{ADL}	Address to Data Loading Time
t_{AR}	ALE Low to $\overline{RE}$ Low
t_{CALH}	CLE/ALE Hold Time
t_{CALS}	CLE/ALE Setup Time
t_{CAH}	Command/Address Hold Time
t_{CAS}	Command/Address Setup Time
t_{CH}	$\overline{CE}$ Hold Time
t_{CDQSH}	DQS Hold Time for data input mode finish
t_{CDQSS}	DQS Setup Time for data input mode start
t_{CHZ}	$\overline{CE}$ High to Output Hi-Z
t_{CLHZ}	CLE High to Output Hi-Z
t_{CLR}	CLE to $\overline{RE}$ Low
t_{COH}	Data Hold Time after $\overline{CE}$ disable
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low
t_{CRES}	$\overline{RE}$ Setup Time before $\overline{CE}$ Low
t_{CS}	$\overline{CE}$ Setup Time
t_{CWAW}	Command Write Cycle to Address Write Cycle Time for Random Data Input
t_{DH}	Data Hold Time
t_{DQSH}	DQS Input High Pulse Width
t_{DQSL}	DQS Input Low Pulse Width
t_{DQSQ}	Output skew among data output and corresponding DQS
t_{DQSRE}	$\overline{RE}$ to DQS and DQ delay
t_{DSC}	Data Strobe Cycle Time
t_{DS}	Data Setup Time
t_{DVW}	Output data valid window
t_{FEAT}	Busy time for Set Feature and Get Feature
t_{QH}	Output hold time from DQS
t_{QHS}	DQS hold skew factor
t_{RC}	Read Cycle Time
t_{REH}	$\overline{RE}$ High pulse width
t_{RP}	$\overline{RE}$ Low pulse width
t_{RPP}	$\overline{RE}$ Low pulse width for Read Status at Power-up sequence
t_{RPRE}	Read Preamble
t_{RPST}	Read Postamble
t_{RPSTH}	Read Postamble Hold Time
t_{RR}	Ready to $\overline{RE}$ High
t_{RST}	Device Resetting Time(Read/Program/Erase)
t_{WB}	$\overline{WE}$ High to Busy
t_{WC}	Write Cycle Time
t_{WH}	$\overline{WE}$ High pulse width
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low
t_{WHR2}	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
t_{WP}	$\overline{WE}$ Low pulse Width
t_{WPRE}	Write Preamble

t_{WPST}	Write Postamble
t_{WPSTH}	Write Postamble Hold Time
t_{WW}	$\overline{WP}$ High/Low to $\overline{WE}$ E low
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)
t_{DCBSYR}	Cache Busy in Read Cache
$t_{DCBSYR2}$	Dummy Busy Time for Page Copy(2) Read

SDR

Parameter	Description
t_{CLS}	CLE Setup Time
t_{CLS2}	CLE Setup Time
t_{CLH}	CLE Hold Time
t_{CS}	$\overline{CE}$ Setup Time
t_{CS2}	$\overline{CE}$ Setup Time
t_{CH}	$\overline{CE}$ Hold Time
t_{WP}	$\overline{WE}$ Low pulse Width
t_{ALS}	ALE Setup Time
t_{ALH}	ALE Hold Time
t_{DS}	Data Setup Time
t_{DH}	Data Hold Time
t_{WC}	Write Cycle Time
t_{WH}	$\overline{WE}$ High pulse width
t_{ADL*}	Address to Data Loading Time
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low
t_{RR}	Ready to $\overline{RE}$ Falling Edge
t_{RW}	Ready to $\overline{WE}$ Falling Edge
t_{RP}	$\overline{RE}$ Low pulse width
t_{RC}	Read Cycle Time
t_{REA}	$\overline{RE}$ Access Time
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low
t_{CLR}	CLE Low to $\overline{RE}$ Low
t_{AR}	ALE Low to $\overline{RE}$ Low
t_{RHOH}	Data Output Hold Time from $\overline{RE}$ High
t_{RLOH}	Data Output Hold Time from $\overline{RE}$ Low
t_{RHZ}	$\overline{RE}$ High to Output High Impedance
t_{CHZ}	$\overline{CE}$ High to Output Hi-Z
t_{CLHZ}	CLE High to Output Hi-Z
t_{REH}	$\overline{RE}$ High pulse width
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)
t_{WHR2}	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
t_{WB}	$\overline{WE}$ High to Busy
t_{RST}	Device Resetting Time(Read/Program/Erase)
t_{CEA}	$\overline{CE}$ Access Time
t_{FEAT}	Busy time for Set Feature and Get Feature

4.3.2. Timing Parameters Table (TENTATIVE)

Table 28 AC Timing Charateristics

Toggle DDR1.0

Parameter	Symbol	100Mhz		Unit
		Min	Max	
Address to Data Loading Time	t_{ADL}	300	-	ns
ALE Low to /RE Low	t_{AR}	10	-	ns
CLE/ALE Hold Time	t_{CALH}	5	-	ns
CLE/ALE Setup Time	t_{CALS}	15	-	ns
Command/Address Hold Time	t_{CAH}	5	-	ns
Command/Address Setup Time	t_{CAS}	5	-	ns
DQS Hold Time for data input mode finish	t_{CDQSH}	100	-	ns
DQS Setup Time for data input mode start	t_{CDQSS}	100	-	ns
/CE Hold Time	t_{CH}	5	-	ns
/CE High to Output Hi-Z	t_{CHZ}	-	30	ns
CLE High to Output Hi-Z	t_{CLHZ}	-	30	ns
CLE to RE Low	t_{CLR}	10	-	ns
Data Hold Time after CE disable	t_{COH}	5	-	ns
/CE Low to /RE Low	t_{CR}	10	-	ns
/RE Setup Time before /CE Low	t_{CRES}	10	-	ns
/CE Setup Time	t_{CS}	20	-	ns
Command Write cycle to Address Write cycle Time for Random data input	t_{CWAW}	300	-	ns
Data Hold Time	t_{DH}	0.9	-	ns
DQS Input High Pulse Width	t_{DQSH}	$0.4*t_{DSC}$	-	ns
DQS Input Low Pulse Width	t_{DQSL}	$0.4*t_{DSC}$	-	ns
Output skew among data output and corresponding DQS	t_{DQSQ}	-	0.8 *	ns
/RE to DQS and DQ delay	t_{DQSRE}	-	25	ns
Data Strobe Cycle Time	t_{DSC}	10	-	ns
Data Setup Time	t_{DS}	0.9	-	ns
Output data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$		ns
Busy time for Set Feature and Get Feature	t_{FEAT}	-	1	µs
Output hold time from DQS	t_{QH}	$t_{QH} = \min[t_{REH}, t_{RP}] - t_{QHS}$		ns
DQS hold skew factor	t_{QHS}	-	0.8 *	ns
/RE Read Cycle Time	t_{RC}	10	-	ns
/RE High pulse width	t_{REH}	$0.4*t_{RC}$	-	ns
/RE Low pulse width	t_{RP}	$0.4*t_{RC}$	-	ns
RE Low pulse width for Read Status at Power-up sequence	t_{RPP}	30	-	ns
Read Preamble	t_{RPRE}	15	-	ns
Read Postamble	t_{RPST}	t_{DQSRE} + 0.5xtRC	-	ns
Read Postamble Hold Time	t_{RPSTH}	25	-	ns
Ready to /RE High	t_{RR}	5	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	10 /30 /100	µs
/WE High to Busy	t_{WB}	-	100	ns
Write Cycle Time	t_{WC}	25	-	ns
/WE High pulse width	t_{WH}	11	-	ns
/WE High to Low	t_{WHR}	120	-	ns
/WE High to /RE Low for Random data out	t_{WHR2}	300	-	ns

/WE Low pulse Width	t_{WP}	11	-	ns
Write Preamble	t_{WPRE}	15	-	ns
Write Postamble	t_{WPST}	6.5	-	ns
Write Postamble Hold Time	t_{WPSTH}	25	-	ns
/WP High/Low to /WE low	t_{WW}	100	-	ns

NOTE : The values in this table are preliminary and subject to change.
In case of 4stack TSOP(TH58TEG8DDKTA20), t_{DQSQ} and t_{QHS} are 1.0ns.

SDR

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}	10	—	ns
CLE Setup Time	t_{CLS2}	40	—	ns
CLE Hold Time	t_{CLH}	5	—	ns
$\overline{CE}$ Setup Time	t_{CS}	15	—	ns
$\overline{CE}$ Setup Time	t_{CS2}	32	—	ns
$\overline{CE}$ Hold Time	t_{CH}	5	—	ns
Write Pulse Width	t_{WP}	10	—	ns
ALE Setup Time	t_{ALS}	10	—	ns
ALE Hold Time	t_{ALH}	5	—	ns
Data Setup Time	t_{DS}	5	—	ns
Data Hold Time	t_{DH}	5	—	ns
Write Cycle Time	t_{WC}	20	—	ns
$\overline{WE}$ High Hold Time	t_{WH}	7	—	ns
Address to Data Loading Time	t_{ADL*}	300	—	ns
$\overline{WP}$ High to $\overline{WE}$ Low	t_{WW}	100	—	ns
Ready to $\overline{RE}$ Falling Edge	t_{RR}	20	—	ns
Ready to $\overline{WE}$ Falling Edge	t_{RW}	20	—	ns
Read Pulse Width	t_{RP}	10	—	ns
Read Cycle Time	t_{RC}	20	—	ns
$\overline{RE}$ Access Time	t_{REA}	—	16	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	9	—	ns
CLE Low to $\overline{RE}$ Low	t_{CLR}	10	—	ns
ALE Low to $\overline{RE}$ Low	t_{AR}	10	—	ns
Data Output Hold Time from $\overline{RE}$ High	t_{RHOH}	25	—	ns
Data Output Hold Time from $\overline{RE}$ Low	t_{RLOH}	5	—	ns
$\overline{RE}$ High to Output High Impedance	t_{RHZ}	—	60	ns
$\overline{CE}$ High to Output High Impedance	t_{CHZ}	—	30	ns
CLE High to Output High Impedance	t_{CLHZ}	—	30	ns
$\overline{RE}$ High Hold Time	t_{REH}	7	—	ns
Output-High-impedance-to-$\overline{RE}$ Falling Edge	t_{IR}	0	—	ns
$\overline{WE}$ High to $\overline{CE}$ Low	t_{WHC}	30	—	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	120	—	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random data out	t_{WHR2}	300	—	ns
$\overline{WE}$ High to Busy	t_{WB}	—	100	ns
Device Reset Time (Ready/Read/Program/Erase)	t_{RST}	—	10/30/100	μs
$\overline{CE}$ Access Time	t_{CEA}	—	25	ns
Busy time for Set Feature and Get Feature	t_{FEAT}	—	1	μs

NOTE : The values in this table are preliminary and subject to change.

Table 29 AC Test Conditions

Parameter	Condition
Input Pulse Levels	VIL to VIH
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	VccQ/2
Output Load	50 Ohms to Vtt (Vtt=0.5*VCCQ)

Table 30 Read/Program/Erase Timing Characteristics

Description	Parameter	Typ.	Max.	Unit
Data Transfer from Cell to Register	t_R	TBD	TBD	μs
Average Programming Time	t_{PROG}	TBD	TBD	μs
Block Erasing Time	t_{BERASE}	TBD	TBD	ms
Data Cache Busy Time in Write Cache (following 11h or 32h)	$t_{DCBSYW1}$	TBD	TBD	μs
Data Cache Busy Time in Write Cache (following 15h)	$t_{DCBSYW2}$	-	TBD	μs
Cache Busy in Read Cache	t_{DCBSYR}	-	TBD	μs
Dummy Busy Time for Page Copy(2) Read	$t_{DCBSYR2}$	-	TBD	μs
Number of Partial Program Cycles in the Same Page	-	-	-	Cycle

NOTE : The values in this table are preliminary and subject to change.

1)t_{PROG} is the internal program time from a cache or page register to NAND array. t_R is the internal loading time from NAND array to the a cache or page register.

2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

3) tPROG and tDCBSYW2 are the average busy time in a block. The absolute maximum for one page operation is TBDμs.

5. COMMAND DESCRIPTION AND DEVICE OPERATION

5.1. Basic Command Sets

Toggle DDR1.0 NAND Flash Memory has addresses multiplexed into 8 I/Os. Command, address and data are all written through DQ [7:0] by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 31 below defines the basic command sets.

Table 31 Basic Command Sets

Function	Primary or Secondary	1st Set	Address Cycles	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
Page Read	Primary	00h	5	30h		Y
Sequential Cache Read	Primary	31h	-	-		Y
Read Start for Last Page Cache Read	Primary	3Fh	-	-		Y
Random Cache Read	Primary	00h	5	31h		Y
Page Program	Primary	80h	5	10h		Y
Cache Program	Primary	80h	5	15h		Y
Block Erase	Primary	60h	3	D0h		Y
Read for Copy-Back	Primary	00h	5	35h		Y
Copy-Back Program	Primary	85h	5	10h		Y
Random Data Input(1)	Primary	85h	2	-		Y
Random Data Output(1)	Primary	05h	2	E0h		Y
Set Feature	Primary	EFh	1	-		
Get Feature	Primary	EEh	1	-		
Read ID	Primary	90h	1	-		Y
Read Status	Primary	70h	-	-	Y	Y
Read Status2	Primary	71h	-	-	Y	Y
Reset	Primary	FFh	-	-	Y	Y
Reset LUN	-	FAh	3	-	Y	Y

NOTE:

1) Random Data Input/Output can be executed in a page.

Caution:

Any undefined command inputs are prohibited except for above command set.

5.2. Basic Operation

5.2.1. Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure 39 defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

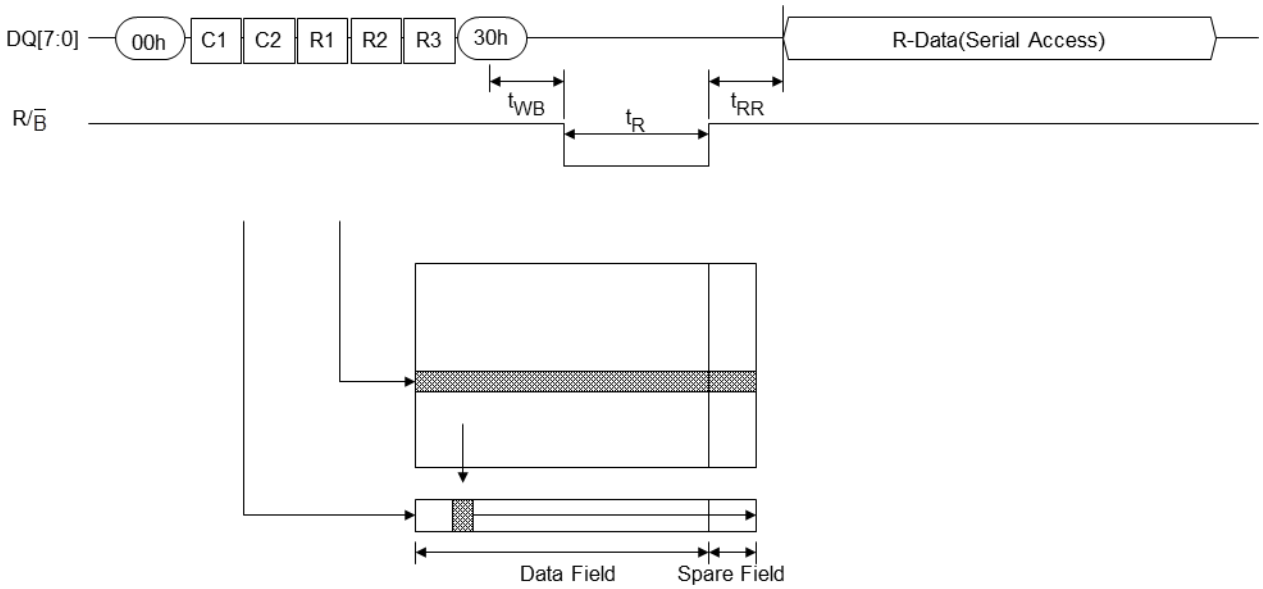


Figure 39. Page Read Timing

5.2.1.1. Page Read Operation with Random Data Output

The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure 40 defines the Random Data Output behavior and timings. The host shall not read data from the LUN until t_{WHR2}(ns) after the second(i.e. E0h) is written to the LUN.

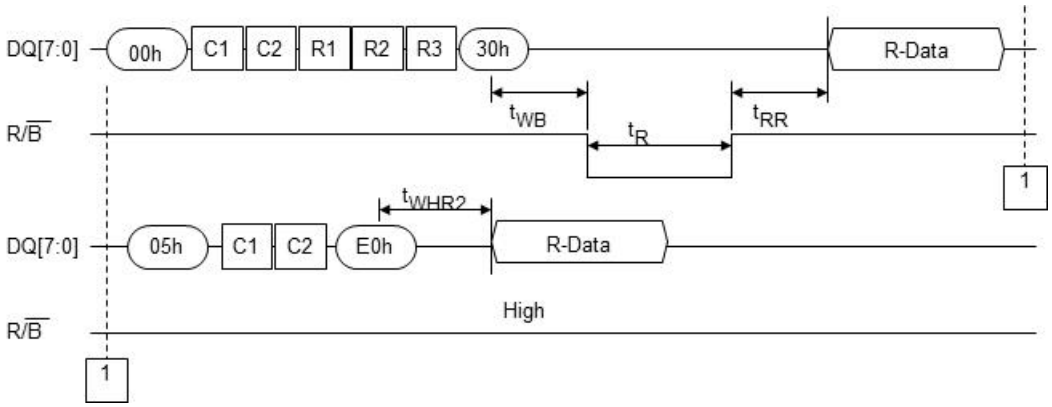


Figure 40. Page Read with Random Data Output Timing

5.2.1.2. Data Out After Status Read

While monitoring the read status to determine when the t_R (transfer from Flash array to a page register) is complete, the host shall re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

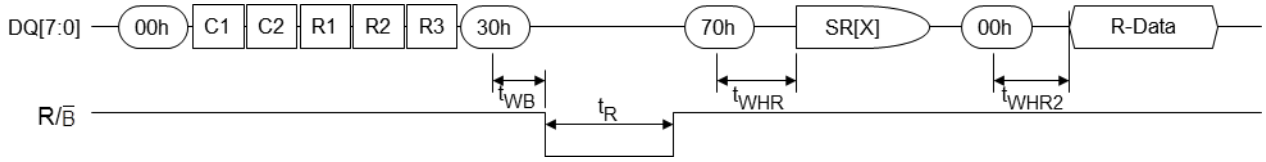


Figure 41. Data Out After Status Read Timing

5.2.2. Sequential Cache Read Operation

The Sequential Cache Read operation permits a page to be read from the page register while another page is simultaneously read from the Flash array for the selected LUN. A Read Page command shall be issued prior to the initial Sequential Cache Read command in a cache read sequence. A Sequential Cache Read command shall be issued prior to the Read Start for Last Page Cache Read command (3Fh) being issued.

The Sequential Cache Read command may be issued after the Read function is complete (i.e. SR[6] is set to one). Data output always begins at column address 00h. When the Sequential Cache Read command (i.e. 31h) is issued, SR[6] is cleared to zero (i.e. busy). After the operation finishes, SR[6] turns to one (i.e. ready) and the host may begin to read the data loaded by the previous Sequential Cache Read operation. The data loaded by a Sequential Cache Read command from Flash array to a page register is copied to a cache register by a following Sequential Cache Read command. And the data of a final page loaded onto a page register is transferred to a cache register by 3Fh command. The host shall not issue a Sequential Cache Read command (31h) after the last page of a block is read. Figure 42 defines the Sequential Cache Read behavior and timings.
Read Status may be performed just after issuing 30h, 31h or 3Fh command. Once Read Status is performed during this operation, Random Data Output for Cache Read shall be operated to output the data from the page register. Random Data Output for Cache Read may be performed just before or within R-Data.

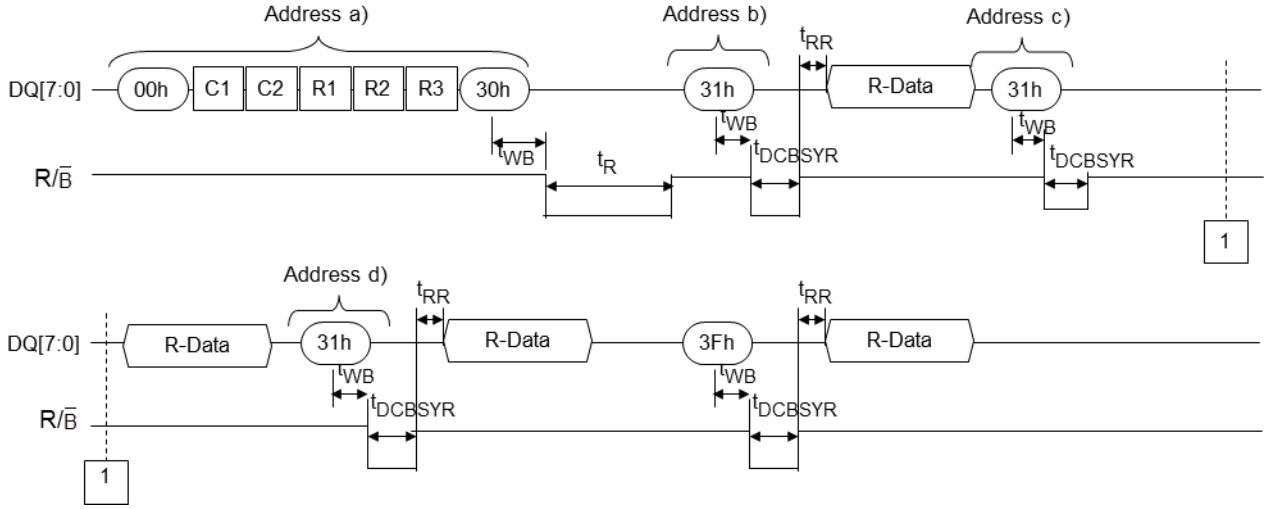


Figure 42. Sequential Cache Read Timing

5.2.3. Random Cache Read Operation

A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. A Random Cache Read command shall be issued prior to the Read Start for Last Page Cache Read command (3Fh) being issued. The page and block address can be accessed in a random manner. Data output always begins at column address 00h. Figure 43 defines the Random Cache Read behavior and timings.

Read Status may be performed just after issuing 30h, 31h or 3Fh command. Once Read Status is performed during this operation, Random Data Output for Cache Read shall be operated to output the data from the page register. Random Data Output for Cache Read may be performed just before or within R-Data.

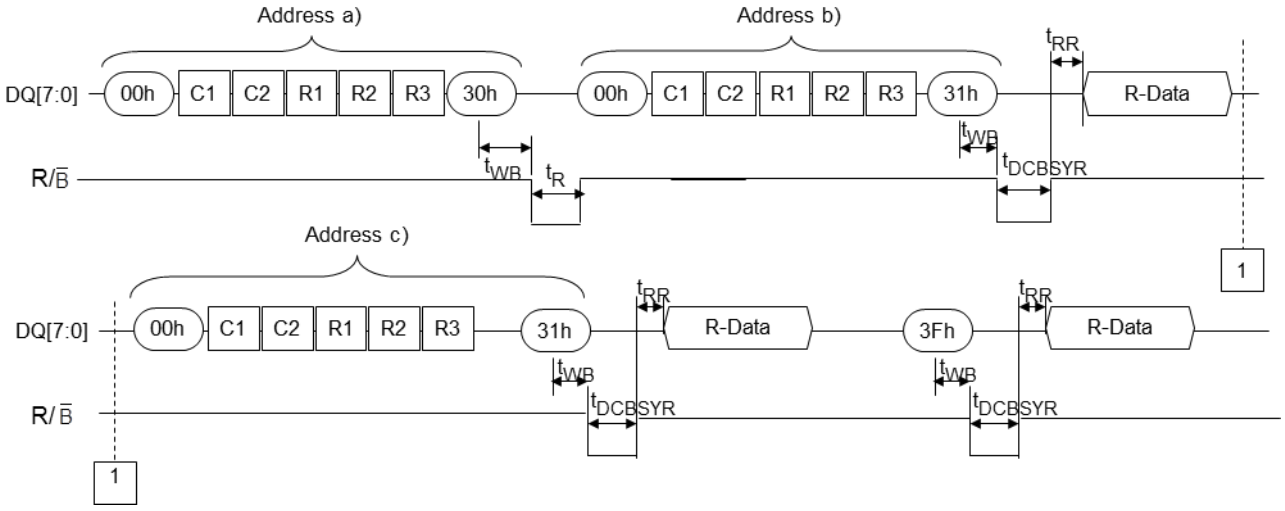


Figure 43. Random Cache Read Timing

5.2.4. Random Data Output for Cache Read

The Random Data Output for Cache Read function changes the column address from which data is being read in the page register for the selected LUN. Note that this function shall not be used as standalone and may be used within Sequential Cache Read Operation or Random Cache Read Operation. The timing when this function may be used is defined in each operation sequence. Figure 40 defines the behavior and timings. The host shall not read data from the LUN until t_{WHR2}(ns) after the second(i.e. E0h) is written to the LUN. The address shall be identical with the address of R-Data.

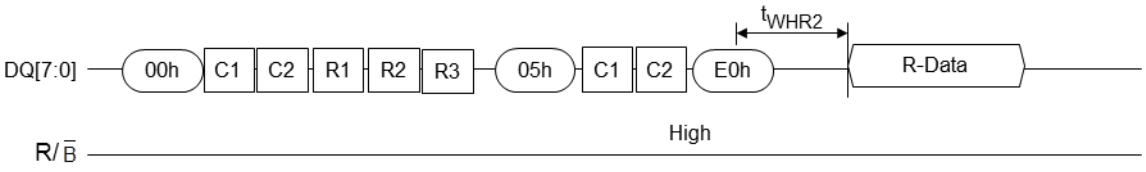


Figure 44. Random Data Output for Cache Read Timing

5.2.5. Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 45 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

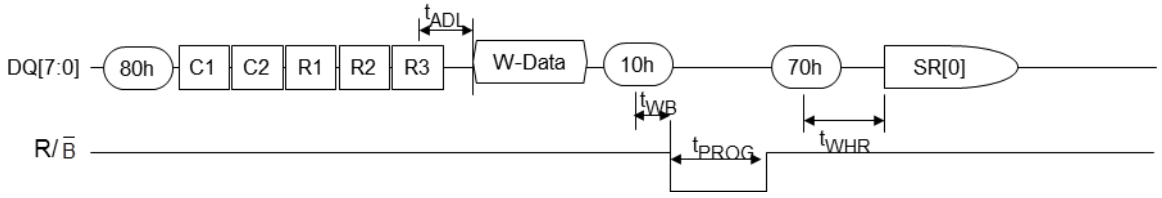


Figure 45. Page Program Timing

5.2.5.1. Program Operation with Random Data Input

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command (i.e. 85h). Random data input may be operated multiple times without limitation.

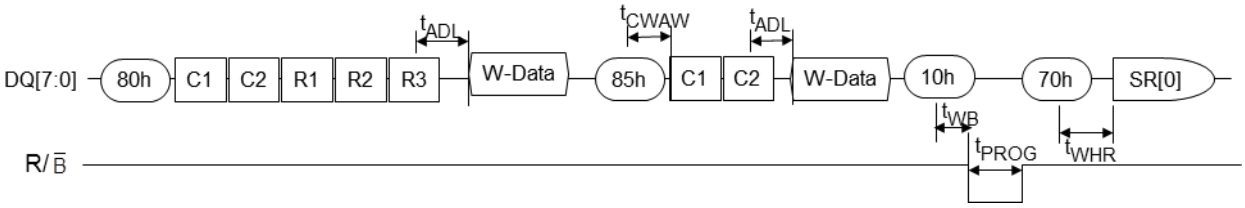


Figure 46. Program operation with Random Data Input Timing

5.2.6. Cache Program Operation

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/$\overline{B}$ returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. However, when command 10h is issued for the final page, R/$\overline{B}$ turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure 47 defines the Cache Program behavior and timings. Note that t_{PROG} at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

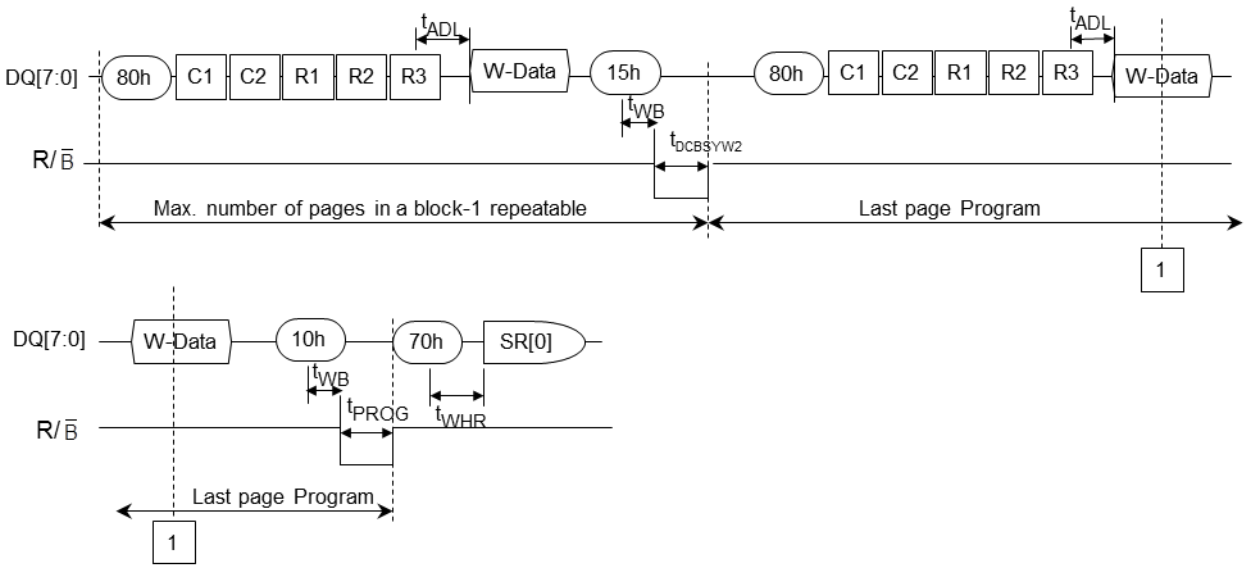


Figure 47. Cache Program Timing

5.2.7. Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while plane and block address are valid. After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure 48defines the Block Erase behavior and timings.

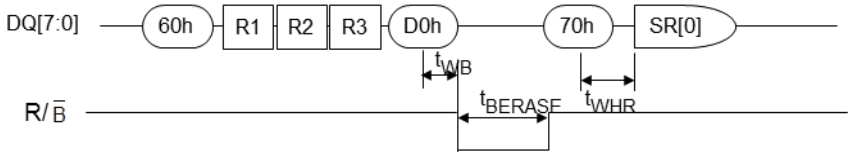


Figure 48. Block Erase Timing

5.2.8. Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page of a block to a page of the other block without data re-loading when no error within the page is found. Since the time-consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Copy-Back Program Operation shall work only within the same plane. Figure 49 defines the Copy-Back Program behavior and timings.

NOTE:

The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.

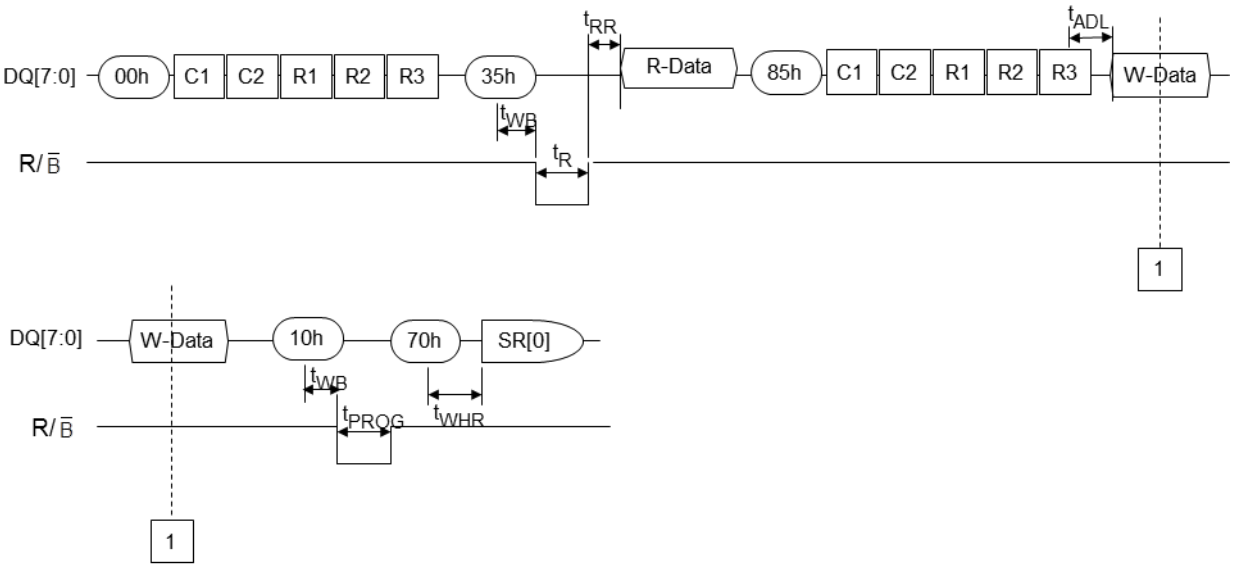


Figure 49. Copy-Back Program Timing

5.2.8.1. Copy-Back Program Operation with Random Data Input

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure 50 defines the Copy-Back Program with Random Data Input behavior and timings.

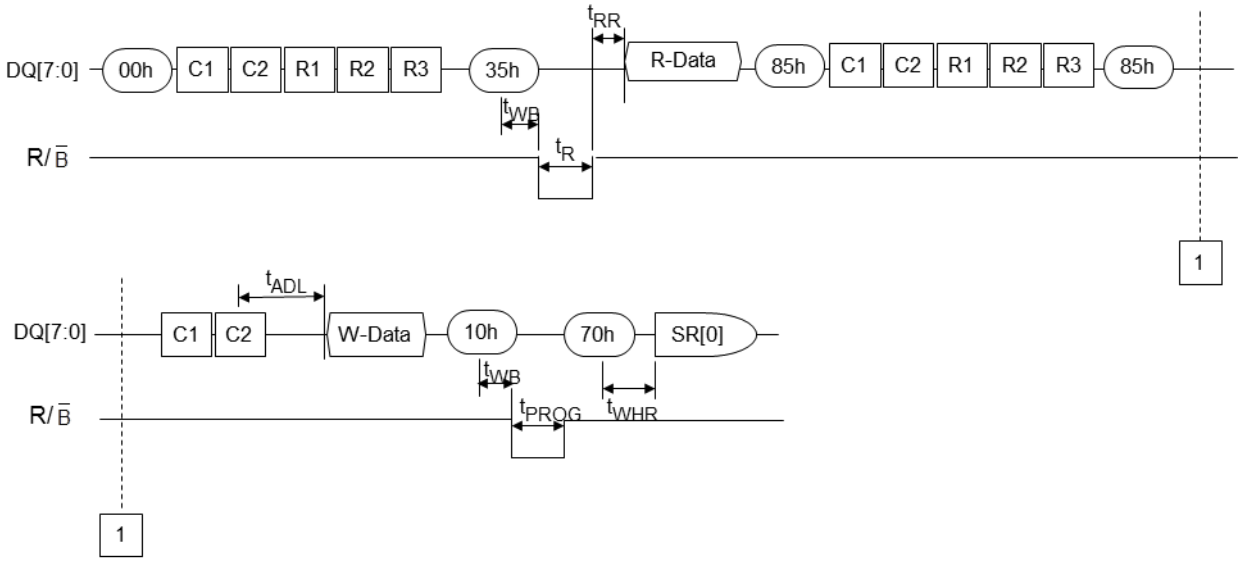


Figure 50. Copy-Back Program with Random Data Input Timing

5.2.9. Set Feature Operation

Users may set particular features using 'Set Feature' operation. Figure 51 defines the Set Features behavior and timings and Table 32 defines features that users can change. Once Set Feature operation begins, the operation shall be completed without any disturbance and interruption such as Reset operation.

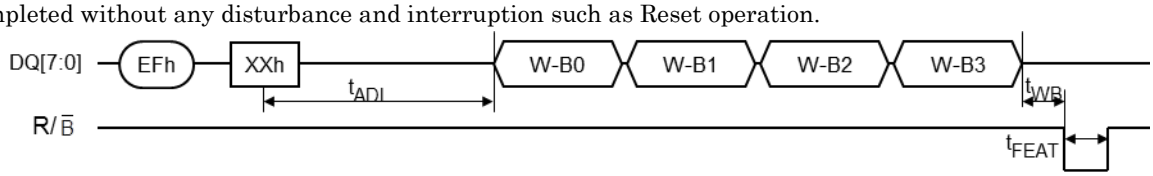


Figure 51. Set Feature Timing

NOTE:
The feature-setting shall work on lower than 133Mbps.

Table 32 Set feature addresses

1st Cycle	2nd Cycle	Description
EFh	02	ODT setting
	10h	Driver strength setting
	30h	External V_{PP} Setting
	80h	Interface change

5.2.9.1. ODT specific setting (02h)

This setting is required in order to use ODT.

Table 33 ODT Specific Setting Data

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
B0	ODT (with Rtt value)				Reserve	0	0	0

Table 34 ODT Specific Setting Data Definition

	Description
ODT	0000 : Disabled (default) 0001 : Enabled with 150ohm 0010 : Enabled with 100ohm 0011 : Enabled with 75ohm 0100 : Enabled with 50ohm

5.2.9.2. Driver strength setting (10h)

Driver strength is configured according to the B0 value.

Table 35 Driver Strength Setting Data

B0 Value	Description
00h ~ 01h	Reserved
02h	Driver Multiplier : Underdrive
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	Driver Multiplier : Overdrive 1
07h	Reserved
08h	Reserved
09h ~ FFh	Reserved

NOTE:
B1, B2 and B3 are reserved and shall be written with 00h.

Table 36 Interface change Setting Data

B0 Value								Description
DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	
0	0	0	0	0	0	0	0	to Toggle DDR1.0
0	0	0	0	0	0	0	1	to SDR

5.2.9.3. External V_{PP}(30h)

This setting controls whether external V_{PP} is enabled. External V_{PP} is configured according to the B0 value. V_{PP} must be validly supplied prior to the Set Feature that enables V_{PP}.

Table 37 External V_{PP} Setting Data

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
B0	Reserved							V_{PP}

Table 38 External V_{PP} Setting Data Definition

	Description
V_{PP}	0 : Disabled (default) 1 : Enabled

NOTE:
B1, B2 and B3 are reserved and shall be written with 00h.

5.2.10. Get Feature Operation

Users find how the target is set through 'Get Feature' command. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. B0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure 52 defines the Get Features behavior and timings.

If Read Status (or Read Status Enhanced) is used to monitor whether the t_{FEAT} time is complete, the host shall issue Read command (i.e. 00h) to read B0-B1-B2-B3.

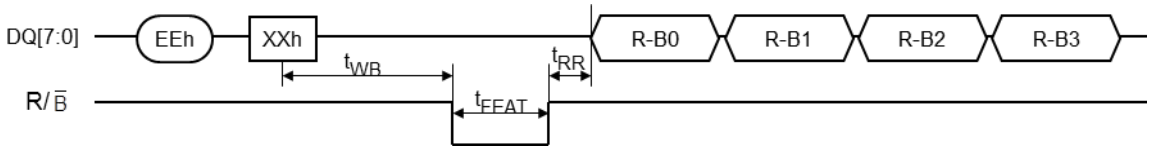


Figure 52. Get Feature Timing

NOTE:
The feature-getting shall work on lower than 133Mbps.

5.2.11. Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Figure 53 defines Read ID operation behavior and timings.

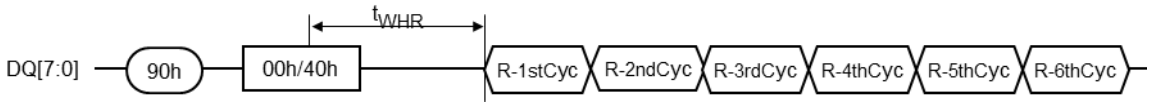


Figure 53. Read ID Timing

5.2.11.1. 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecture information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

Table 39 00h Address ID Definition Table

Cycle	Description	TC58TEG6DDK	TH58TEG7DDK	TH58TEG8DDK
1st Data	Maker Code	98h	98h	98h
2nd Data	Device Code	DEh	DEh	3Ah
3rd Data	Number of LUN per Target, Cell Type, Etc.	94h	94h	95h
4th Data	Page Size, Block Size,etc.	93h	93h	93h
5th Data	Plane Number,etc.	76h	76h	7Ah
6th Data	Technology Code	50h	50h	50h

Table 40 2nd ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Memory Density per Target	8 Gbits	1	1	0	1	0	0	1	1	D3h
	16 Gbits	1	1	0	1	0	1	0	1	D5h
	32 Gbits	1	1	0	1	0	1	1	1	D7h
	64 Gbits	1	1	0	1	1	1	1	0	DEh
	128 Gbits	0	0	1	1	1	0	1	0	3Ah
	256 Gbits	0	0	1	1	1	1	0	0	3Ch

Table 41 3rd ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Number of LUN per Target	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		

Table 42 4th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size (w/o redundant area)	2KB							0	0
	4KB							0	1
	8KB							1	0
	16KB							1	1
Block Size (w/o redundant area)	128KB	0		0	0				
	256KB	0		0	1				
	512KB	0		1	0				
	1MB	0		1	1				
	2MB	1		0	0				
	4MB	1		0	1				
	Reserved	1		X	X				

*X : either 0 or 1

Table 43 5th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Number of Plane per Target	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		

Table 44 6th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Technology Code	90 nm process						0	0	1
	70 nm process						0	1	0
	56 nm process						0	1	1
	43 nm process						1	0	0
	32 nm process						1	0	1
	24 nm process						1	1	0
	19 nm process						1	1	1
	1Y nm process						0	0	0
Interface	Conventional	0							
	Toggle DDR1.0 Mode	1							

NOTE:

As for Table 44 “6th ID data”, even if the interface is changed into Toggle DDR1.0 by SetFeature, the value of "Interface" is still 0.

5.2.11.2. 40h Address ID Definition

Toggle DDR1.0 NAND also provides six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

Table 45 40h Address ID Cycle

1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	01h

Table 46 40h Address ID Definition

Cycle	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0	1	0	1	0
2nd	E	0	1	0	0	0	1	0	1
3rd	D	0	1	0	0	0	1	0	0
4th	E	0	1	0	0	0	1	0	1
5th	C	0	1	0	0	0	0	1	1
6th	Conventional Asynchronous SDR	0	0	0	0	0	0	0	1
	Toggle DDR1.0					0	0	1	0
	Synchronous DDR					0	1	0	0

5.2.12. Read Status Operation

In the case of non-multi-plane operations, the 70h Read Status function retrieves a status value for the last operation issued. If multi-plane operations are in progress on a single LUN, then 70h Read Status returns the composite status value. Specifically, 70h Read Status shall return the combined status value of the independent status register bits according to Table 47. On the other hands, 71h Read Status returns statuses of two planes on a single LUN according to Table 48. Figure 54 defines the Read Status behavior and timings.

Table 47 Read Status Definition for 70h

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Copy-Back	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0 is only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0 is only valid when DQ 5 shows the Ready state, and DQ 1 is only valid when DQ 6 shows the Ready state.

Table 48 Read Status Definition for 71h

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail	Pass/Fail for Plane#0 (N)	Pass/Fail for Plane#1 (N)	Pass/Fail for Plane#0 (N-1)	Pass/Fail for Plane#1 (N-1)	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Copy-Back	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ 5 shows the Ready state, and DQ 3 and DQ 4 are only valid when DQ 6 shows the Ready state.

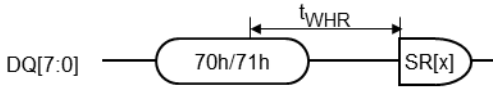


Figure 54. Read Status Timing

5.2.13. Reset Operation

Toggle DDR1.0 NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations. The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Reset during the operation with a cache register (e.g. Cache Program operation) may not just stop the most recent page operation but it may also stop the previous page operation depending on when the FF reset is input. Although the device is already in process of reset operation, a new reset command will be accepted. Figure 55 defines the Reset behavior and timings.

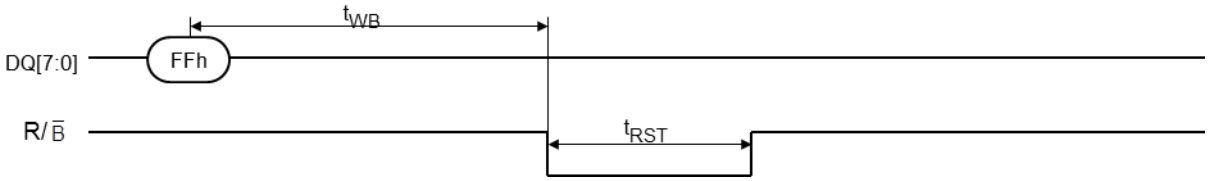


Figure 55. Reset timing

When Reset (FFh) command is input during Program operation

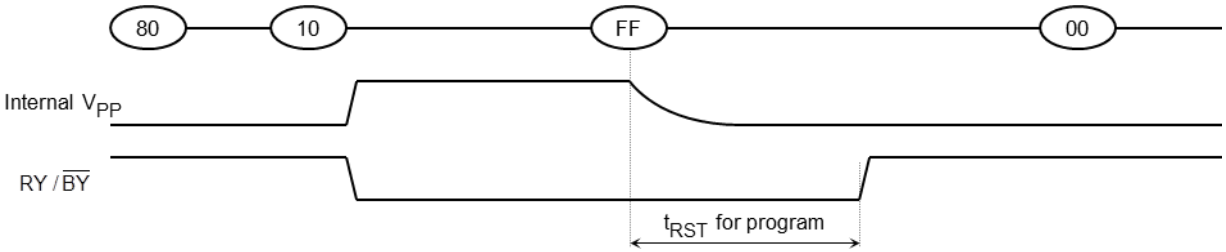


Figure 56. Reset timing during Program operation

When Reset (FFh) command is input during Erase operation

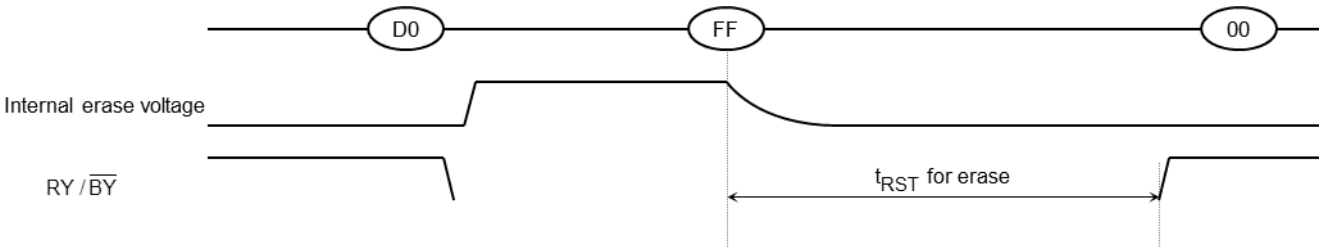


Figure 57. Reset timing during Erase operation

When Reset (FFh) command is input during Read operation

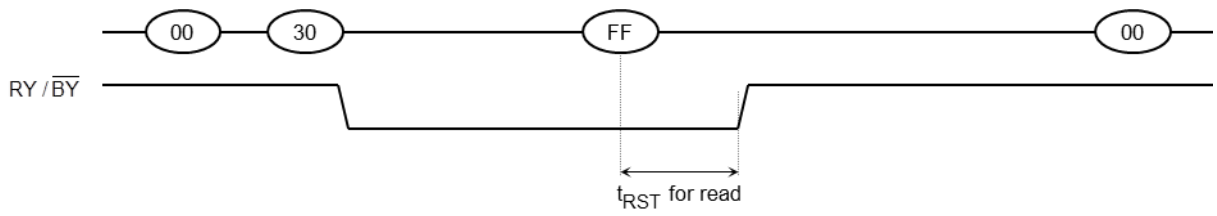


Figure 58. Reset timing during Read operation

When Read Status command (70h) is input after Reset operation

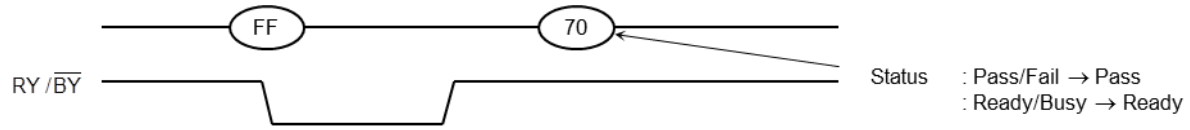


Figure 59. Status Read after Reset operation

When two or more Reset commands are input in succession

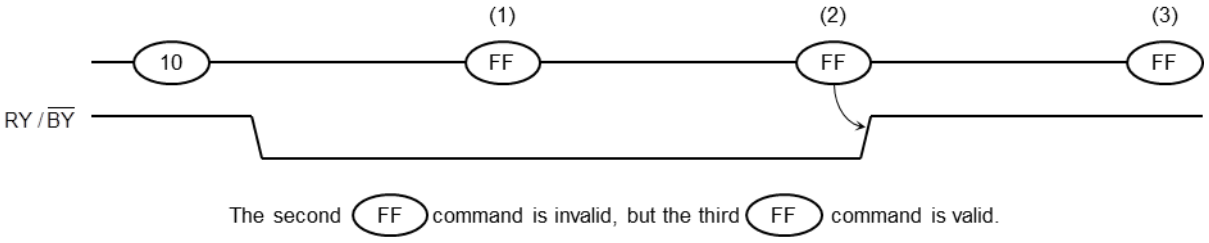


Figure 60. Successive Reset operation

5.2.14. Reset LUN Operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure 61 defines the Reset LUN behavior and timings.

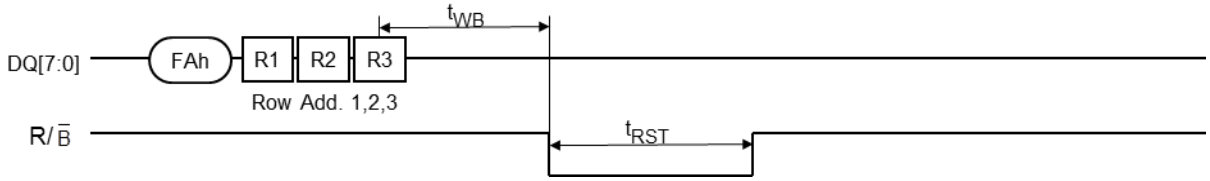


Figure 61. Single LUN Reset Timing

NOTE :
If there are multiple LUNs on a target, R/$\overline{B}$ is also affected by the rest of LUN(s) on the same target.

5.3. Extended Operation

5.3.1. Extended Command Sets

Table 49 defines the Extended Command Sets. Primary and Secondary Commands are also categorized in the table. Primary commands are recommended to use when a particular function is implemented, while Secondary commands are for alternative implementation for backward compatibility.

Table 49 Extended Command Sets

Function	Primary or secondary	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set
Multi Page Read / Multi Page Cache Read	Primary	00h--32h	5	00h--30h	5
Multi Page Read	Secondary	60h--	3	--30h	-
Multi Page Cache Read	Secondary	60h--	3	--30h	-
Multi Page Random Cache Read	Primary	00h--32h	5	00h--31h	5
Multi Page Random Data Output	Primary	00h---05h	5	---E0h	2
Multi Page Program	Primary	80h--11h	5	81h--11h or 81h--10h	5
Multi Page Cache Program	Primary	80h--11h	5	81h--11h or 81h--15h	5
Multi Block Erase	Primary	60h--	3	--D0h	-
Multi Read for Copy-Back	Primary	00h--32h	5	00h--35h	5
Multi Read for Copy-Back	Secondary	60h--	5	--35h	-
Multi Copy-Back Program	Primary	85h--11h	5	81h--11h or 81h--10h	5
Page Copy (2) Read	Primary	00h--	5	--3Ah	-
Page Copy (2) Program	Primary	8Ch--	5	--15h	-
Page Copy (2) Program for Last Page	Primary	8Ch--	5	--10h	-
Multi Page Copy (2) Read	Primary	00h--32h	5	00h--3Ah	5
Multi Page Copy (2) Read	Secondary	60h--	3	--3Ah	-
Multi Page Copy (2) Program	Primary	8Ch--11h	5	8Ch--15h	5
Multi Page Copy (2) Program for Last Page	Primary	8Ch--11h	5	8Ch--10h	5
Device Identification Table Read	Primary	ECh--	1	-	-
Read status enhanced	Primary	78h--	3	-	-
Read LUN#0 Status	Secondary	F1h	-	-	-
Read LUN#1 Status	Secondary	F2h	-	-	-

NOTE:

1) Multi Page Random Data out must be used after Multi Page Read or Multi Page Cache Read operation.
2) Any command between 11h and 80h/81h/85h is prohibited except 70h/71h/78h/F1h and FFh.
3) Read LUN#1 Status command is only for the device having two LUNs per a target.

5.3.2. Address Input Restrictions for Multi Page Operation

Multi Page operation requires specific address input restrictions described as below.

- Address Input Restrictions for Multi Page Operation:

1) Mode A: Multi Page operation over multiple planes
   In this mode, multiple page addresses may be set over multiple planes. When setting page address of each plane, the page addresses shall be identical although block addresses may differ. The same plane address shall not be set twice or more within a set of address setting sequence. The number of planes which are set for this operation shall be even. Multi Page Operation in this mode is also regarded as multi-plane operation.

5.3.3. Multi Page Read Operation

The Multi Page Read operation is an extension of the Page Read operation. The device supporting Multi Page Read operation also allows multiple Random data-output from each page (i.e. Multi Page Random Data Output) once multi-pages are loaded to page registers. With the primary command, R/$\overline{B}$ returns to ready in a short time (i.e. $t_{DCBSYW1}$) after the first command 32h since it does not load data from a selected page and the selected page data are transferred to the cache registers via page registers in less than t_R after command 30h. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2.

Once the data are loaded into the cache registers, the data on the first page can be read out by issuing the Multi Page Random Data Output command. The data on other pages can be also read out using the identical command sequences. Figure 62 and Figure 63 define Multi Page Read and Multi Page Random Data Output behavior and timings. In the case of secondary command, make sure $\overline{WP}$ is held to High level when Multi Page Read operation is performed.

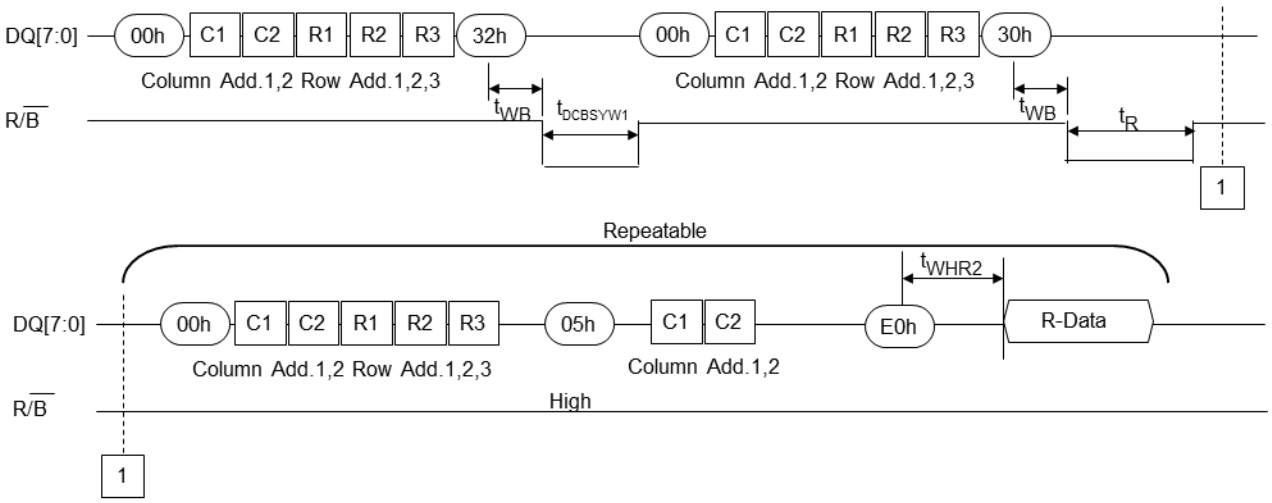


Figure 62. Example Timing with Multi Page Read (Primary)

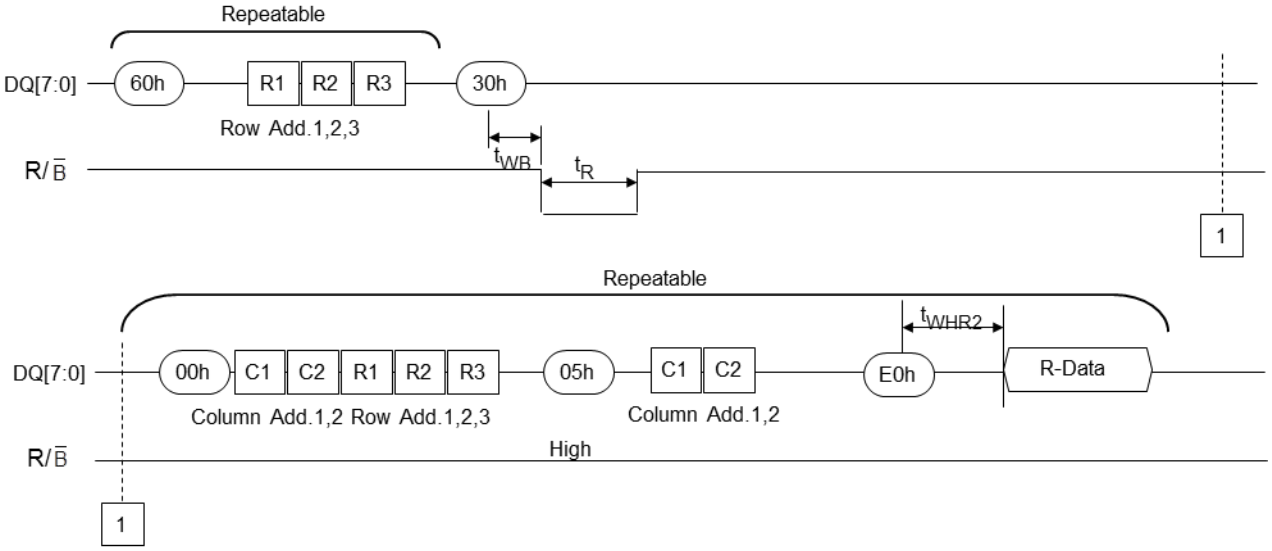


Figure 63. Example Timing with Multi Page Read (Secondary)

5.3.4. Multi Page Sequential Cache Read Operation

Multi Page Sequential Cache Read operation provides fast sequential read function after the initial Multi Page Read operation is set. With the primary command, once Multi Page Read operation performs, next page data can be loaded to page register by command 31h without additional address setting while a host reads data, which is loaded by Multi Page Read operation, from cache registers. Since the next page data are loaded to page registers during host read-out period, R/$\overline{B}$ turns to high (i.e. ready) in a short time after command 31h although data loading by command 31h is being performed internally. If the previous data is still being loaded after command 31h, R/$\overline{B}$ busy state may take as long as t_R, hence the maximum time of t_{DCBSYR} is identical to t_R. At the last page, command 3Fh shall be issued to transfer data from page registers to cache registers. Multi Page Sequential Cache Read operation shall work only within a block of each plane and shall not be continued over the boundary of plane. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2. Figure 64 and Figure 65 defines Multi Page Sequential Cache Read behavior and timings. In the case of secondary command, make sure $\overline{WP}$ is held to High level when Multi Page Sequential Cache Read operation is performed.

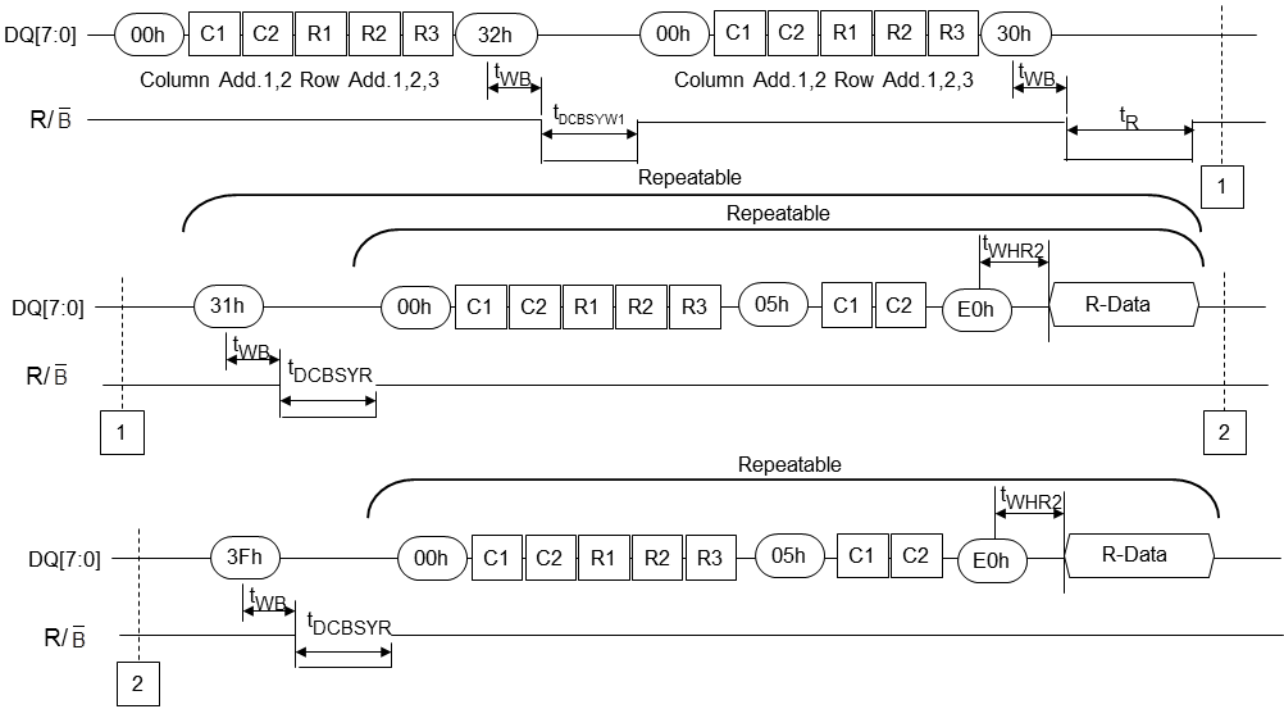


Figure 64. Example Timing with Multi Page Cache Read (Primary)

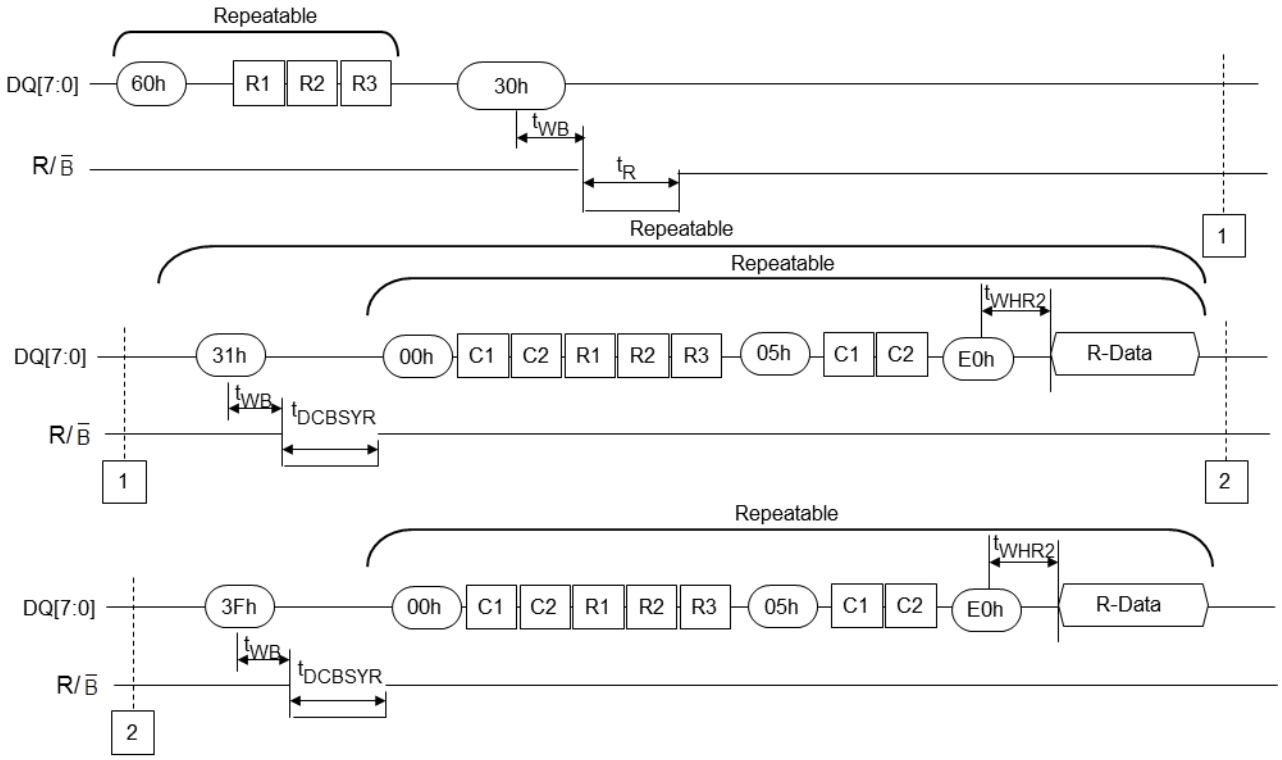


Figure 65. Example Timing with Multi Page Cache Read (Secondary)

5.3.5. Multi Page Random Cache Read Operation

Multi Page Random Cache Read function requires multiple address settings ahead of command 31h to load data of particular pages. Since the selected pages are loaded to page register while a host read data from cache register where previous data are loaded, R/$\overline{B}$ returns high (i.e. ready) in a short time unless the previous data are still being loaded. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2 The activated planes for the first Multi Page Random Cache Read shall be kept using in the next address sequence until the Multi Page Random Cache operation is completed by command 3Fh. Figure 66 defines Multi Page Random Cache Read behavior and timings.

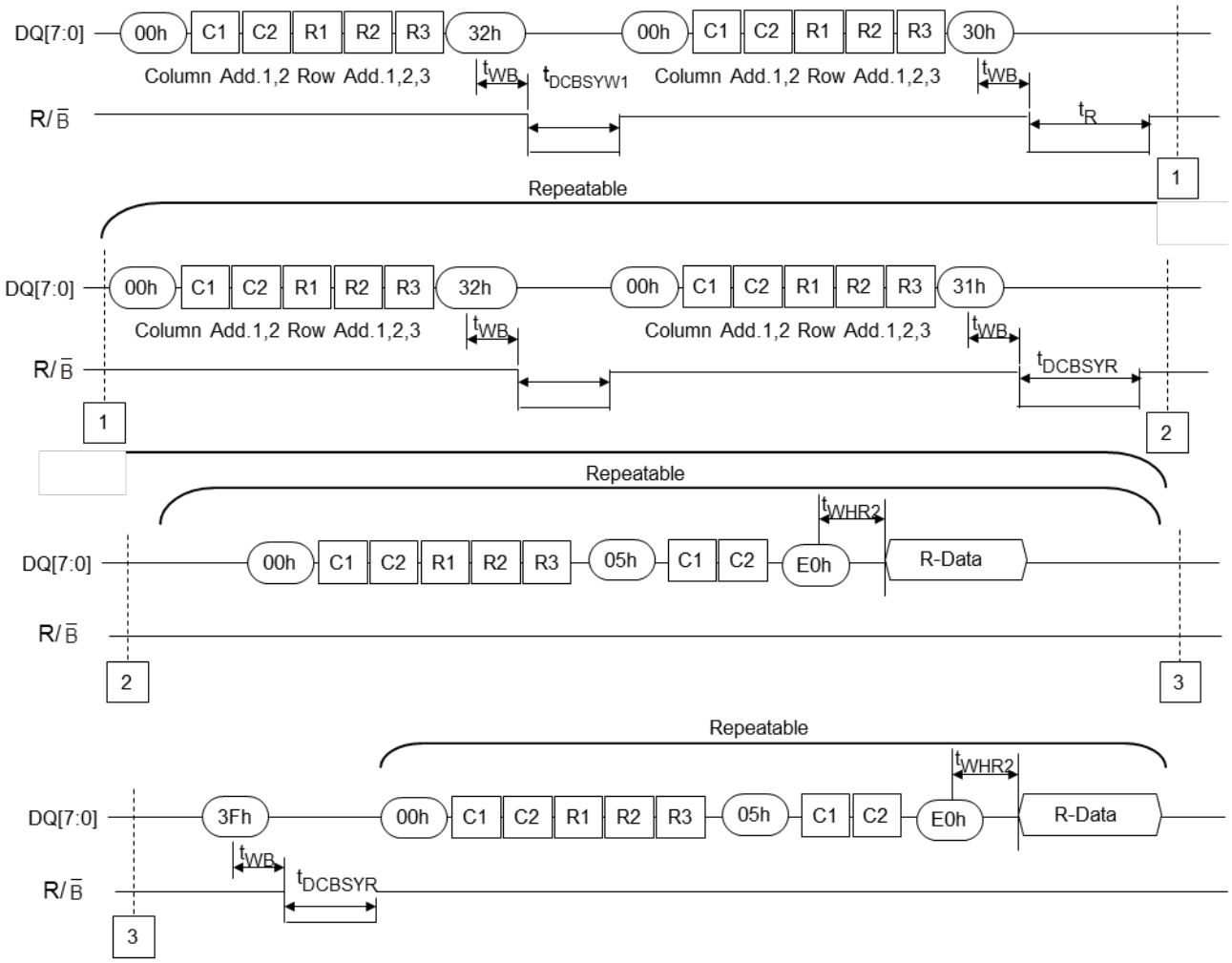


Figure 66. Example Timing with Multi Page Cache Read (Primary)

5.3.6. Multi Page Program Operation

Multi Page Program function extends an effective programmable page size using multiple pages.
When a host moves to load data for another page, command 11h for the second command is used. After 11h command, R/$\overline{B}$ returns high (i.e. ready) in a short period of time since it is not actual programming operation. At the last page loading, command 81h is issued before loading data and command 10h after data loading is issued for the second command. After command 10h, all loaded data in each page starts to be programmed to Flash array simultaneously. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section5.3.2. Figure 67 define s Multi Page Program behavior and timings. "PRG" in the figure shall be either 80h or 81h. Within a set of repeatable sequences which ends up with command 11h, command 80h shall be issued at the first sequence and command 81h shall be issued at the subsequent sequence.

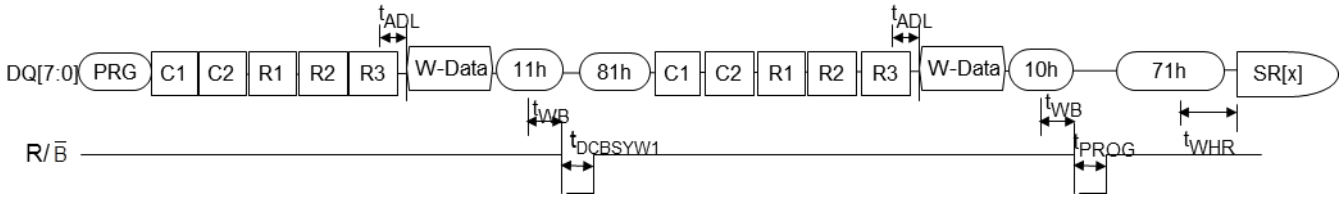


Figure 67. Example Timing with Multi Page Program

5.3.7. Multi Page Cache Program Operation

The Multi Page Cache Program is an extension of the Cache Program. After loading pages for Multi Page Cache Program, command 15h is issued. After command 15h, R/$\overline{B}$ returns high once transferring data from cache register to page register is completed. Internal program operation is in progress after R/$\overline{B}$ returns while other pages are loaded by a host. At the last page loading for the entire Multi Page Cache Program, command 10h is required to finalize the operation and R/$\overline{B}$ stays busy as long as t_{PROG}. Multi Page Cache Program operation shall work only within a block of each plane and shall not be continued over the boundary of plane. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2. The activated planes for the first Multi Page Cache Program shall be kept using in the next address sequence until the Multi Page Cache Program operation is completed by command 10h. Figure 68 defines Multi Page Cache Program behavior and timings. "PRG" in the figure shall be either 80h or 81h. Within a set of repeatable sequences which ends up with command 11h, command 80h shall be issued at the first sequence and command 81h shall be issued at the subsequent sequence.

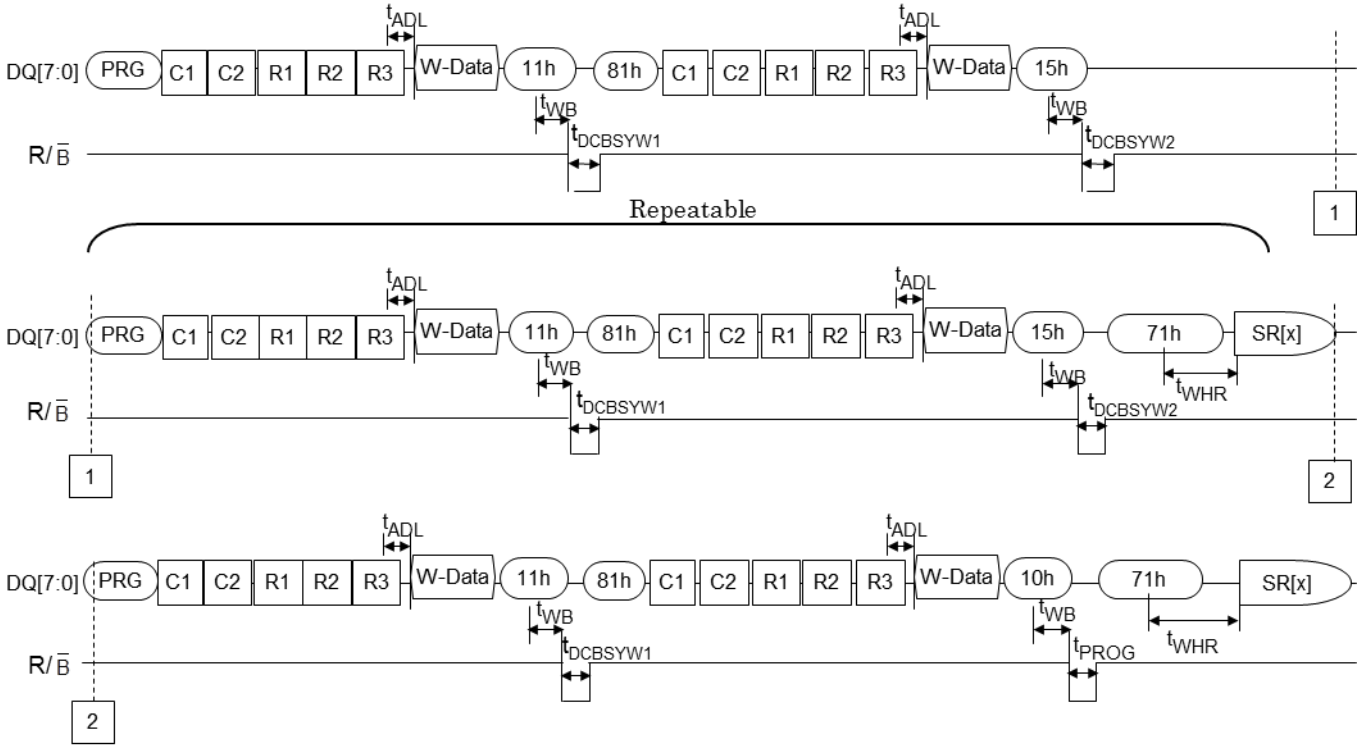


Figure 68. Example Timing with Multi Page Cache Program

5.3.8. Multi Block Erase Operation

Multi Block Erase allows users to erase multiple blocks comprising a block of each plane simultaneously.
The same plane address shall not be set twice within a set of address setting sequence for the Multi Block Erase Operation. Figure 69 defines Multi Block Erase behavior and timings.

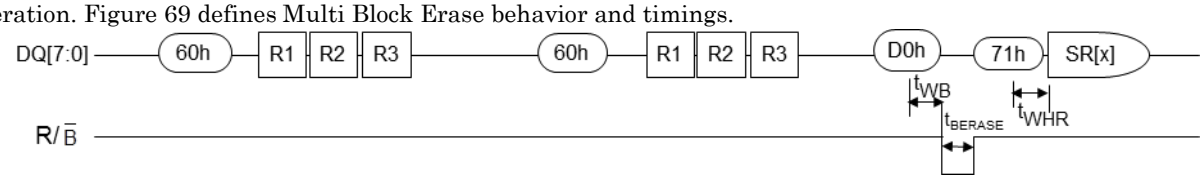


Figure 69. Example Timing with Multi Block Erase

5.3.9. Multi Copy-Back Program Operation

The Multi Copy-Back Program is an extension of the Copy-back Program. Multi Copy-Back Program operation is executed two sets of commands, Multi Read for Copy-Back and Multi Copy-Back Program. Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2. The read Data shall be copied back to a page in the same plane. Make sure $\overline{WP}$ is held to High level when Multi Copy-Back operation is performed. Figure 70 and Figure 71 defines Multi Copy-Back Program behavior and timings. "PRG" in the figure shall be either 85h or 81h. Within a set of repeatable sequences which ends up with command 11h, command 85h shall be issued at the first sequence and command 81h shall be issued at the subsequent sequence.

NOTE:
The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.

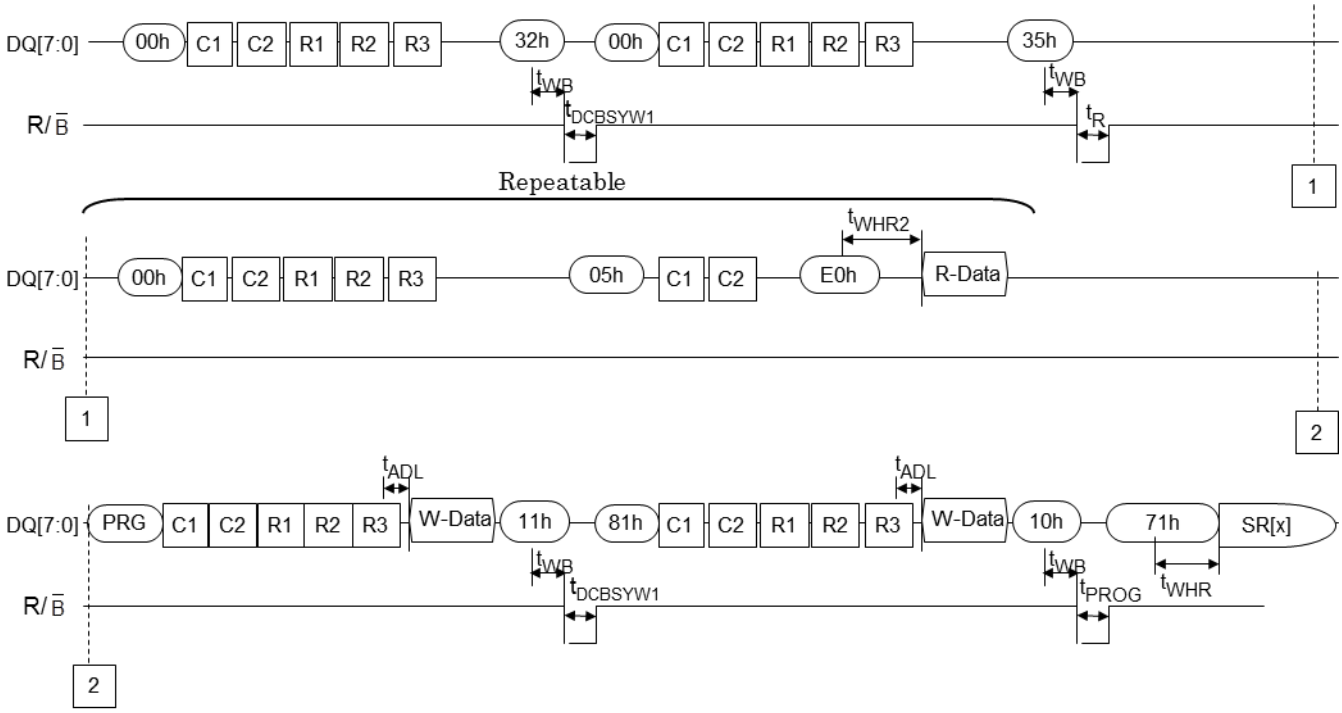


Figure 70. Example Timing with Multi Copy-Back Program (Primary)

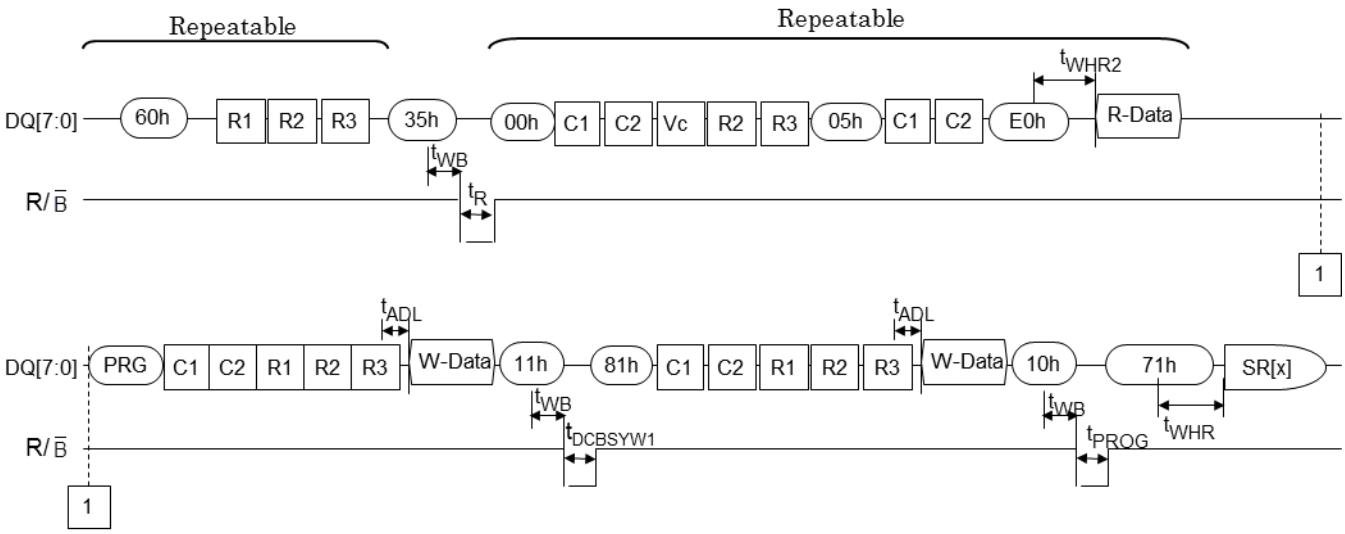


Figure 71. Example Timing with Multi Copy-Back Program (Secondary)

5.3.10. Page Copy (2) Operation

By using Page Copy (2), data in a page of a block can be copied to a page of the other block after the data has been read out. This operation needs to be executed within a plane. If the block address is changed, this sequence shall be started from the beginning. Data input is required only if previous data output needs to be changed. If the data needs to be changed, locate the desired address with the column and row address input after 8Ch command, and change only the data that needs to be changed. Make sure $\overline{WP}$ is held to High level when Page Copy (2) operation is performed.

Figure 72 defines Page Copy (2) behavior and timings.

NOTE:

The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.

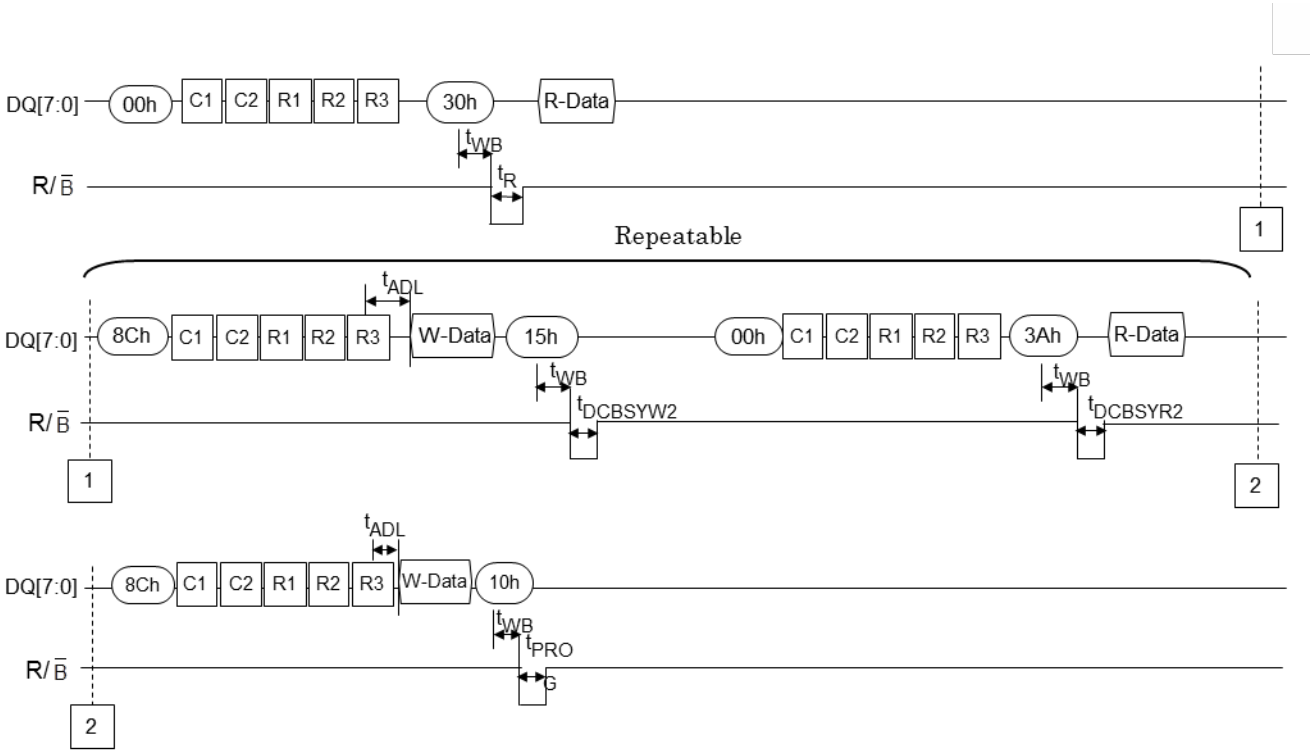


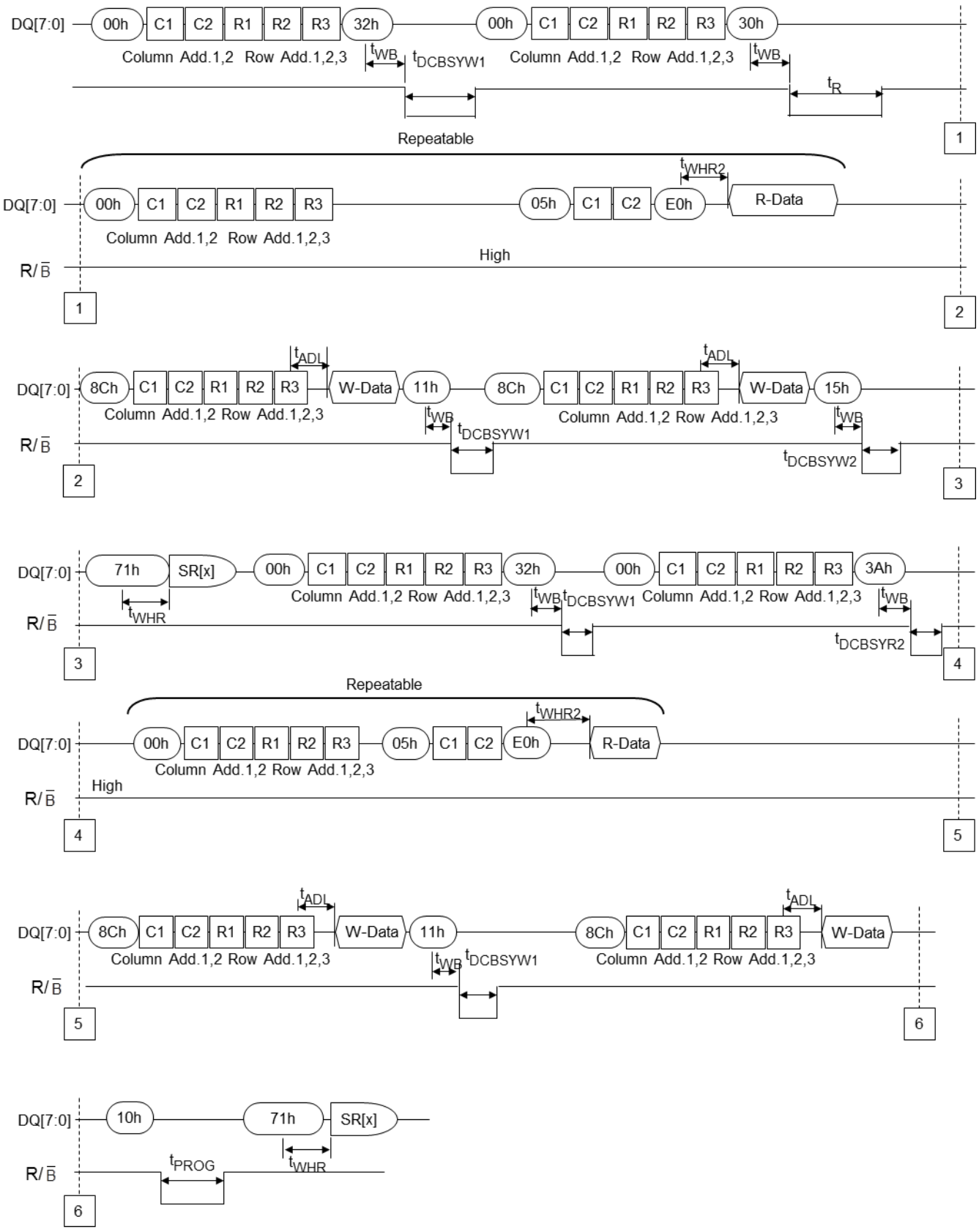
Figure 72. Example Timing with Page Copy (2)

5.3.11. Multi Page Copy (2) Operation

The Multi Page Copy (2) is an extension of the Page Copy (2). Note that the multi page addresses shall be set through 1st Set and 2nd Set of command with the Address Input Restrictions for Multi Page Operation specified in section 5.3.2. This operation needs to be executed within each plane. If the block address is changed, this sequence shall be started from the beginning. Data input is required only if previous data output needs to be changed. If the data needs to be changed, locate the desired address with the column and row address input after 8Ch command, and change only the data that needs to be changed. Make sure $\overline{WP}$ is held to High level when Multi Page Copy (2) operation is performed. Figure 73 and Figure 74 defines Multi Page Copy (2) behavior and timings.

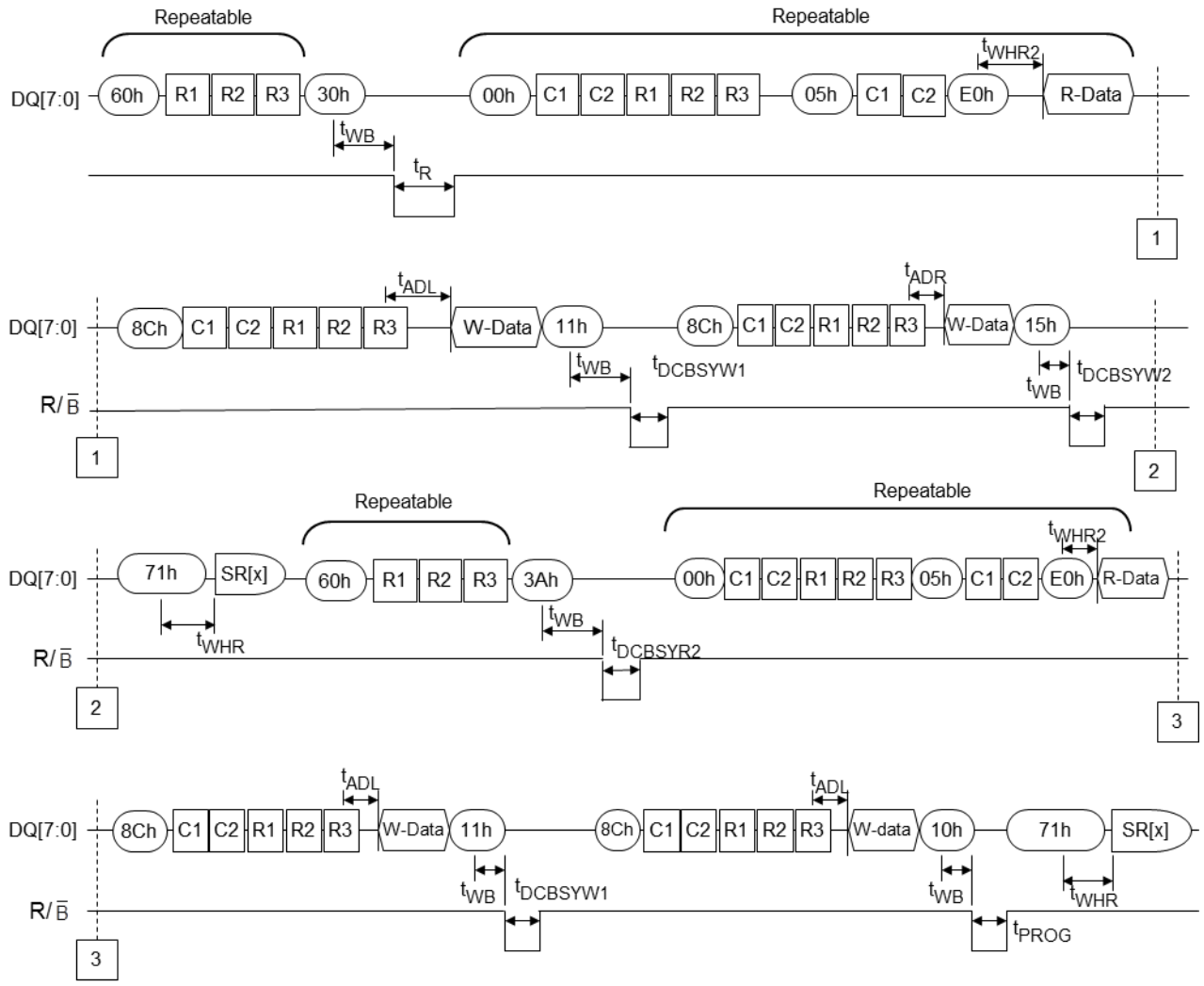
NOTE:

The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.



The sequence from 1 to 4 is repeatable.

Figure 73. Example Timing with Multi Page Copy (2)



The sequence from 1 to 3 is repeatable.

Figure 74. Example Timing with Multi Page Copy (2)

5.3.12. Device Identification Table Read Operation

The device returns a JEDEC standard formatted Parameter Page which equivalent to Device ID Table during the data out phase of the Device ID Table Read command when address 40h is inputted. The Device ID Table Read command is a ECh value for the command cycle and a 40h value for the address cycle, and the bytes of the Parameter Page are returned in the data output (DOUT) cycles.

After the command ECh address 40h is received by the NAND device, it will go busy for a period of time (t_R in the figure) after which, the Parameter Page can be read from the device. The length and contents of the Parameter Page is defined in section 5.3.13.

The READ ID command is used by the controller to identify the device that is attached. This command is used by the controller to gather information about the target flash device. Figure 75 defines the behavior and timings.

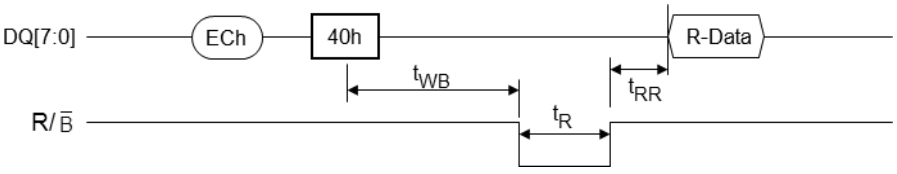


Figure 75. Device Identification Table Read Timing

5.3.13. Parameter Page Definition

Table 50 defines the Parameter Page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the Parameter Page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page. All optional parameters that are not implemented shall be cleared to 00h by the target.

When the information is read from the device, the host shall calculate CRC to check the data prior to taking action on that data. If the CRC of the first Parameter Page read is not valid, the host shall read redundant Parameter Page copies. The host shall then check the CRC of that redundant Parameter Page.
If the CRC is correct, the host may take action based on the contents of that redundant Parameter Page. If the CRC is incorrect, then the host shall attempt to read the next redundant Paramter Page by the same procedure.
There may be a case where the number of error exceeds the error detectability of CRC. In this case, the retrieved data with valid CRC may contain errors. To be prepared for this case, the host should compare two or more sets of the retrieved data to check equality.
All Parameter Pages returned by the Target may have invalid CRC values; however, bit-wise majority of other ECC techniques may be used to recover the contents of the Paramter Page by the host.
If necessary, the data successfully read should be safely kept by the host in its own manner for further protection.

If there are any discrepancies between the content in Paramter Page and the content in this or the other documents separately provided, the latter shall take precedence.

Table 50 Parameter Page Definitions

Byte	O/M	Description	Value
Revision information and features block			
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)	4Ah, 45h, 53h, 44h
4-5	M	Revision number 3-15: Reserved (0) 2: 1 = supports Parameter Page revision 1.0 and standard revision 1.0 1: 1 = supports vendor specific Parameter Page 0: Reserved (0)	04h, 00h
6-7	M	Features supported 9-15 Reserved (0) 8: 1 = supports program page register clear enhancement 7: 1 = supports external Vpp 6: 1 = supports Toggle Mode DDR 5: 1 = supports Synchronous DDR 4: 1 = supports multi-plane read operations 3: 1 = supports multi-plane program and erase operations 2: 1 = supports non-sequential page programming 1: 1 = supports multiple LUN operations 0: 1 = supports 16-bit data bus width	D8h, 01h (TC58TEG6DDKTA/TH58TEG7DDKTA) DAh, 01h (TH58TEG8DDKTA)
8-10	M	Optional commands supported 11-23: Reserved (0) 10: 1 = supports Synchronous Reset 9: 1 = supports Reset LUN (Primary) 8: 1 = supports Small Data Move 7: 1 = supports Multi-plane Copyback Program (Primary) 6: 1 = supports Random Data Out (Primary) 5: 1 = supports Read Unique ID 4: 1 = supports Copyback	DFh, 02h, 00h

		3: 1 = supports Read Status Enhanced (Primary) 2: 1 = supports Get Features and Set Features 1: 1 = supports Read Cache commands 0: 1 = supports Page Cache Program command	
11-12	O	Secondary commands supported 8-15: Reserved (0) 7: 1 = supports secondary Read Status Enhanced 6: 1 = supports secondary Multi-plane Block Erase 5: 1 = supports secondary Multi-plane Copyback Program 4: 1 = supports secondary Multi-plane Program 3: 1 = supports secondary Random Data Out 2: 1 = supports secondary Multi-plane Copyback Read 1: 1 = supports secondary Multi-plane Read Cache Random 0: 1 = supports secondary Multi-plane Read	85h, 00h
13	O	Number of Parameter Pages	20h
14-31		Reserved (0)	All 00h
Manufacturer information block			
32-43	M	Device manufacturer (12 ASCII characters) TOSHIBA	54h, 4Fh, 53h, 48h 49h, 42h, 41h, 20h 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	54h, 43h, 35h, 38h, 54h, 45h, 47h,36h, 44h, 44h, 4Bh, 54h, 41h, 30h, 30h, 20h 20h, 20h, 20h, 20h (TC58TEG6DDKTA00)
			54h, 48h, 35h, 38h, 54h, 45h, 47h, 37h, 44h, 44h, 4Bh, 54h, 41h, 32h, 30h, 20h 20h, 20h, 20h, 20h (TH58TEG7DDKTA20)
			54h, 48h, 35h, 38h, 54h, 45h, 47h, 38h, 44h, 44h, 4Bh, 54h, 41h, 32h, 30h, 20h 20h, 20h, 20h, 20h (TH58TEG8DDKTA20)
			54h, 43h, 35h, 38h, 54h, 45h, 47h, 36h 44h, 44h, 4Bh, 54h, 41h, 49h, 30h, 20h 20h, 20h, 20h, 20h (TC58TEG6DDKTAI0)
			54h, 48h, 35h, 38h, 54h, 45h, 47h, 37h, 44h, 44h, 4Bh, 54h, 41h, 4Bh, 30h, 20h 20h, 20h, 20h, 20h (TH58TEG7DDKTAK0)
			54h, 48h, 35h, 38h, 54h, 45h, 47h, 38h, 44h, 44h, 4Bh, 54h, 41h, 4Bh, 30h, 20h 20h, 20h, 20h, 20h (TH58TEG8DDKTAK0)
64-69	M	JEDEC manufacturer ID (6 bytes)	98h, 00h, 00h, 00h, 00h, 00h
70-79		Reserved (0)	All 00h
Memory organization block			
80-83	M	Number of data bytes per page	00h, 40h, 00h, 00h
84-85	M	Number of spare bytes per page	00h, 05h
86-91		Reserved (0)	All 00h
92-95	M	Number of pages per block	00h, 01h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	54h, 08h, 00h, 00h
100	M	Number of logical units (LUNs)	01h (TC58TEG6DDK, TH58TEG7DDK) 02h (TH58TEG8DDK)
Memory organization block			
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles	23h
102	M	Number of bits per cell	02h
103	M	Number of programs per page	01h
104	M	Multi-plane addressing 4-7: Reserved (0)	01h

		0-3: Number of plane address bits	
105	M	Multi-plane operation attributes 3-7: Reserved (0) 2: 1= read cache supported 1: 1 = program cache supported 0: 1= No multi-plane block address restrictions	07h
106-143		Reserved (0)	All 00h
Electrical parameters block			
144-145	O	Asynchronous SDR speed grade 6-15: Reserved (0) 5: 1 = supports 20 ns speed grade (50 MHz) 4: 1 = supports 25 ns speed grade (40 MHz) 3: 1 = supports 30 ns speed grade (~33 MHz) 2: 1 = supports 35 ns speed grade (~28 MHz) 1: 1 = supports 50 ns speed grade (20 MHz) 0: 1 = supports 100 ns speed grade (10 MHz)	00h, 00h
146-147	O	Toggle DDR speed grade 5-15: Reserved (0) 4: 1 = supports 10 ns speed grade (~100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz) 0: 1 = supports 30 ns speed grade (~33 MHz)	1Fh, 00h
148-149	O	Synchronous DDR speed grade 6-15: Reserved (0) 5: 1 = supports 10 ns speed grade (100 MHz) 4: 1 = supports 12 ns speed grade (~83 MHz) 3: 1 = supports 15 ns speed grade (~66 MHz) 2: 1 = supports 20 ns speed grade (50 MHz) 1: 1 = supports 30 ns speed grade (~33 MHz) 0: 1 = supports 50 ns speed grade (20 MHz)	00h, 00h
150	O	Asynchronous SDR features 0-7: Reserved (0)	00h
151	O	Toggle-mode DDR features 0-7: Reserved (0)	00h
152	O	Synchronous DDR features 0-7: Reserved (0)	00h
153-154	M	tPROG Maximum page program time (µs)	TBD
155-156	M	tBERS Maximum block erase time (µs)	TBD
157-158	M	tR Maximum page read time (µs)	TBD
159-160	O	tR Maximum multi-plane page read time (µs)	00h
161-162	O	tCCS Minimum change column setup time (ns)	00h
163-164	M	I/O pin capacitance, typical or maximum	64h, 00h (TC58TEG6DDKTA) C8h, 00h (TH58TEG7DDKTA) 90h, 01h (TH58TEG8DDKTA)
165-166	M	Input pin capacitance, typical or maximum	64h, 00h (TC58TEG6DDKTA) C8h, 00h (TH58TEG7DDKTA) 90h, 01h (TH58TEG8DDKTA)
167-168	O	CK pin capacitance, typical or maximum	00h, 00h
169	M	Driver strength support 3-7: Reserved (0) 2: 1 = supports 18 ohm drive strength 1: 1 = supports 25 ohm drive strength 0: 1 = supports 35ohm/50ohm drive strength	03h
170-171	O	tADL Program page register clear enhancement tADL value (ns)	00h, 00h
172-207		Reserved (0)	All 00h
ECC and endurance block			

208	O	Guaranteed valid blocks of target	00h
209-210	O	Block endurance for guaranteed valid blocks	00h, 00h
211-218	M	ECC and endurance information block 0 Byte 211: Number of bits ECC correctability Byte 212: Codeword size Byte 213-214: Maximum value of average bad blocks per LUN Byte 215-216: Block endurance Byte 217-218: Reserved (0)	TBD
219-226	O	ECC and endurance information block 1 Byte 219: Number of bits ECC correctability Byte 220: Codeword size Byte 221-222: Maximum value of average bad blocks per LUN Byte 223-224: Block endurance Byte 225-226: Reserved (0)	All 00h
227-234	O	ECC and endurance information block 2 Byte 227: Number of bits ECC correctability Byte 228: Codeword size Byte 229-230: Maximum value of average bad blocks per LUN Byte 231-232: Block endurance Byte 233-234: Reserved (0)	All 00h
235-242	O	ECC and endurance information block 3 Byte 235: Number of bits ECC correctability Byte 236: Codeword size Byte 237-238: Maximum value of average bad blocks per LUN Byte 239-240: Block endurance Byte 241-242: Reserved (0)	All 00h
243-419		Reserved (0)	All 00h
Vendor specific block			
420-421	M	Vendorr Specific Revision Number	Vendor specific
422-509		Vendor specific	Vendor specific
CRC for Parameter Page			
510-511	M	Integrity CRC	CRC Value
Redundant Parameter Pages			
512-1023		Value of bytes 0-511	Value of bytes 0-511
1024-1535		Value of bytes 0-511	Value of bytes 0-511
…			
15872-16383		Value of bytes 0-511	Value of bytes 0-511

Byte 0-3: Parameter page signature
This field contains the Parameter Page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the Paramter Page is present.

Byte 0 shall be set to 4Ah.
Byte 1 shall be set to 45h.
Byte 2 shall be set to 53h.
Byte 3 shall be set to 44h.

Byte 4-5: Revision number
This field indicates the revisions of the Paramter Page and standard that the target complies to. The target may support multiple revisions of the standard. This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.
Bit 1 when set to one indicates that the target supports vender specific Paramter Page.
Bit 2 when set to one indicates that the target supports Paramter Page revision 1.0 and standard revision 1.0.
Bits 3-15 are reserved and shall be cleared to zero.

Byte 6-7: Features supported
This field indicates the optional features that the target supports.

Bit 0 when set to one indicates that the target's data bus width is 16-bits. Bit 0 when cleared to zero indicates that the target's data bus width is 8-bits. The host shall use the indicated data bus width for all commands that are defined to be transferred at the bus width (x8 or x16). Note that some commands, like Read ID, always transfer data as 8-bit only.

Bit 1 when set to one indicates that the target supports multiple LUN operations. If bit 1 is cleared to zero, then the host shall not issue commands to a LUN unless all other LUNs on the target are idle (i.e. R/B_n is set to one).

Bit 2 when set to one indicates that the target supports non-sequential page programming operations, such that the host may program pages within a block in arbitrary order. Bit 2 when cleared to zero indicates that the target does not support non-sequential page programming operations. If bit 2 is cleared to zero, the host shall program all pages within a block in order starting with page 0.

Bit 3 when set to one indicates that the target supports multi-plane program and erase operations.

Bit 4 when set to one indicates that the target supports multi-plane read operations.

Bit 5 when set to one indicates that the Synchronous DDR data interface is supported by the target. If bit 5 is set to one, then the target shall indicate the Synchronous DDR timing modes supported in the Synchronous DDR timing mode support field. Bit 5 when cleared to zero indicates that the Synchronous DDR data interface is not supported by the target.

Bit 6 when set to one indicates that the Toggle Mode DDR data interface is supported by the target. If bit 6 is set to one, then the target shall indicate the Toggle Mode DDR timing modes supported in the Toggle Mode DDR timing mode support field. Bit 6 when cleared to zero indicates that the Toggle Mode DDR data interface is not supported by the target.

Bit 7 when set to one indicates that the target supports external Vpp. If bit 7 is cleared to zero, then the target does not support external Vpp.

Bit 8 when set to one indicates that the target supports clearing only the page register for the LUN addressed with the Program (80h) command. If bit 8 is cleared to zero, then a Program (80h) command clears the page register for each LUN that is part of the target. At power-on, the device clears the page register for each LUN that is part of the target.

Bits 9-15 are reserved and shall be cleared to zero.

Byte 8-10: Optional commands supported
This field indicates the optional commands that the target supports.

Bit 0 when set to one indicates that the target supports the Page Cache Program command. If bit 0 is cleared to zero, the host shall not issue the Page Cache Program command to the target.

Bit 1 when set to one indicates that the target supports the Read Cache Random, Read Cache Sequential, and Read Cache End commands. If bit 1 is cleared to zero, the host shall not issue the Read Cache Sequential, Read Cache Random, or Read Cache End commands to the target.

Bit 2 when set to one indicates that the target supports the Get Features and Set Features commands. If bit 2 is cleared to zero, the host shall not issue the Get Features or Set Features commands to the target.

Bit 3 when set to one indicates that the target supports the Read Status Enhanced command. If bit 3 is cleared to zero, the host shall not issue the Read Status Enhanced command to the target. Read Status Enhanced shall be supported if the target has multiple LUNs or supports multi-plane operations.

Bit 4 when set to one indicates that the target supports the Copyback Program and Copyback Read commands. If bit 4 is cleared to zero, the host shall not issue the Copyback Program or Copyback Read commands to the target.

Bit 5 when set to one indicates that the target supports the Read Unique ID command. If bit 5 is cleared to zero, the host shall not issue the Read Unique ID command to the target.

Bit 6 when set to one indicates that the target supports the Random Data Out command. If bit 6 is cleared to zero, the host shall not issue the Random Data Out command to the target.

Bit 7 when set to one indicates that the target supports the Multi-plane Copyback Program command. If bit 7 is cleared to zero, the host shall not issue the Multi-plane Copyback Program command to the target.

Bit 8 when set to one indicates that the target supports the Small Data Move command for both Program and Copyback operations. If bit 8 is cleared to zero, the target does not support the Small Data Move command for Program or Copyback operations. The Small Data Move command is mutually exclusive with overlapped multi-plane support. When bit 8 is set to one, the device shall support the 11h command to flush any internal data pipeline regardless of whether multi-plane operations are supported.

Bit 9 when set to one indicates that the target supports the Reset LUN command. If bit 9 is cleared to zero, the host shall not issue the Reset LUN command.

Bit 10 when set to one indicates that the target supports the Synchronous Reset command. If bit 10 is cleared to zero, the host shall not issue the Synchronous Reset command.

Bits 11-23 are reserved and shall be cleared to zero.

Byte 11-12: Secondary commands supported
This field indicates the secondary commands that the target supports.

Bit 0 when set to one indicates that the target supports the secondary Multi-plane Read command. If bit 0 is cleared to zero, the host shall not issue the secondary Multi-plane Read command to the target.

Bit 1 when set to one indicates that the target supports the secondary Multi-plane Read Cache Random command. If bit 1 is cleared to zero, the host shall not issue the secondary Multi-plane Read Cache Random command to the target.

Bit 2 when set to one indicates that the target supports the secondary Multi-plane Copyback Read command. If bit 2 is cleared to zero, the host shall not issue the secondary Multi-plane Copyback Read command to the target.

Bit 3 when set to one indicates that the target supports the secondary Random Data Out command. If bit 3 is cleared to zero, the host shall not issue the secondary Random Data Out command to the target.

Bit 4 when set to one indicates that the target supports the secondary Multi-plane Program command. If bit 4 is

cleared to zero, the host shall not issue the secondary Multi-plane Program command to the target.

Bit 5 when set to one indicates that the target supports the secondary Multi-plane Copyback Program command. If bit 5 is cleared to zero, the host shall not issue the secondary Multi-plane Copyback Program command to the target.

Bit 6 when set to one indicates that the target supports the secondary Multi-plane Block Erase command. If bit 6 is cleared to zero, the host shall not issue the secondary Multi-plane Block Erase command to the target.

Bit 7 when set to one indicates that the target supports the secondary Read Status Enhanced command. If bit 7 is cleared to zero, the host shall not issue the secondary Read Status Enhanced command to the target.

Bits 8-15 are reserved and shall be cleared to zero.

Byte 13: Number of Parameter Pages
This field specifies the number of Parameter Pages present, including the original and the subsequent redundant versions.

Byte 32-43: Device manufacturer
This field contains the manufacturer of the device. The content of this field is an ASCII character string of twelve bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string. If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

Byte 44-63: Device model
This field contains the model number of the device. The content of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

Byte 64-69: JEDEC manufacturer ID
This field contains the JEDEC manufacturer ID for the manufacturer of the device.

Byte 80-83: Number of data bytes per page
This field contains the number of data bytes per page. The value reported in this field shall be a power of two. The minimum value that shall be reported is 512 bytes.

Byte 84-85: Number of spare bytes per page
This field contains the number of spare bytes per page. There are no restrictions on the value.

Byte 92-95: Number of pages per block
This field contains the number of pages per block.

Byte 96-99: Number of blocks per logical unit
This field contains the number of blocks per logical unit. There are no restrictions on this value.

Byte 100: Number of logical units (LUNs)
This field indicates the number of logical units the target supports. Logical unit numbers are sequential, beginning with a LUN address of zero. This field shall be greater than zero.

Byte 101: Number of Address Cycles
This field indicates the number of address cycles used for row and column addresses. The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.
Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE :
Throughout these standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

Byte 102: Number of bits per cell
This field indicates the number of bits per cell in the Flash array. This field shall be greater than zero. The value reported in this field shall be a power of two.

Byte 103: Number of programs per page
This field indicates the maximum number of times a portion of a page may be programmed without an erase operation. After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page. This field shall be greater than zero.

Byte 104: Multi-plane addressing
This field describes parameters for multi-plane addressing.

Bits 0-3 indicate the number of bits that are used for plane addresses. This value shall be greater than 0h when multi-plane operations are supported.

Bits 4-7 are reserved.

Byte 105: Multi-plane operation attributes
This field describes attributes for multi-plane operations. This byte is mandatory when multi-plane operations are supported as indicated in the Features supported field.

Bit 0 indicates that there are no block address restrictions for the multi-plane operation. If set to one all block address bits may be different between multi-plane operations. If cleared to zero, there are block address restrictions.

Bit 1 indicates whether program cache is supported with multi-plane programs. If set to one then program cache is supported for multi-plane program operations. If cleared to zero then program cache is not supported for multi-plane program operations. Note that program cache shall not be used with multi-plane copyback program operations.

Bit 2 indicates whether read cache is supported with multi-plane reads. If set to one then read cache is supported for multi-plane read operations. If cleared to zero then read cache is not supported for multiplane read operations. Note that read cache shall not be used with multi-plane copyback read operations.

Bits 3-7 are reserved.

Byte 144-145: Asynchronous SDR speed grade
This field indicates the asynchronous SDR speed grades supported.

Bit 0 when set to one indicates that the target supports the 100 ns speed grade (10 MHz).
Bit 1 when set to one indicates that the target supports the 50 ns speed grade (20 MHz).
Bit 2 when set to one indicates that the target supports the 35 ns speed grade (~28 MHz).
Bit 3 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 4 when set to one indicates that the target supports the 25 ns speed grade (40 MHz).
Bit 5 when set to one indicates that the target supports the 20 ns speed grade (50 MHz).
Bits 6-15 are reserved and shall be cleared to zero.

Byte 146-147: Toggle DDR1.0 speed grade
This field indicates the Toggle DDR1.0 speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz).
Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz).

Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz).
Bit 4 when set to one indicates that the target supports the 10 ns speed grade (~100 MHz).
Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz).
Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz).
Bit 7 when set to one indicates that the target supports the 5 ns speed grade (~200 MHz).
Bits 8-15 are reserved and shall be cleared to zero.

Byte 148-149: Synchronous DDR speed grade
This field indicates the synchronous DDR speed grades supported. The target shall support an inclusive range of speed grades.
Bit 0 when set to one indicates that the target supports the 50 ns speed grade (20 MHz).
Bit 1 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 2 when set to one indicates that the target supports the 20 ns speed grade (50 MHz).
Bit 3 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz).
Bit 4 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz).
Bit 5 when set to one indicates that the target supports the 10 ns speed grade (100 MHz).
Bits 6-15 are reserved and shall be cleared to zero.

Byte 150: Asynchronous SDR features
This field describes features and attributes for asynchronous SDR operation. This byte is mandatory when the asynchronous SDR data interface is supported.
Bits 0-7 are reserved.

Byte 151: Toggle-mode DDR features
This field describes features and attributes for Toggle-mode DDR operation. This byte is mandatory when the Toggle-mode DDR data interface is supported.
Bits 0-7 are reserved.

Byte 152: Synchronous DDR features
This field describes features and attributes for synchronous DDR operation. This byte is mandatory when the synchronous DDR data interface is supported.

Bit 0 indicates the tCAD value that shall be used by the host. If bit 0 is set to one, then the host shall use the tCADs (slow) value in synchronous DDR command, address and data transfers. If bit 0 is cleared to zero, then the host shall use the tCADf (fast) value in synchronous DDR command, address and data transfers.

Bit 1 indicates that the device supports the CK being stopped during data input. If bit 1 is set to one, then the host may optionally stop the CK during data input for power savings. If bit 1 is set to one, the host may pause data while the CK is stopped. If bit 1 is cleared to zero, then the host shall leave CK running during data input.

Bits 2-7 are reserved.

Byte 153-154: Maximum page program time
This field indicates the maximum page program time (tPROG) in microseconds.

Byte 155-156: Maximum block erase time
This field indicates the maximum block erase time (tBERS) in microseconds.

Byte 157-158: Maximum page read time
This field indicates the maximum page read time (tR) in microseconds.

Byte 159-160: Maximum multi-plane page read time
This field indicates the maximum page read time (tR) for multi-plane page reads in microseconds. Multiplane page read times may be longer than single page read times. This field shall be supported if the target supports multi-plane reads as indicated in the Features supported field.

Byte 161-162: Minimum change column setup time.
This field indicates the minimum change column setup time (tCCS) in nanoseconds. This parameter is used for the asynchronous SDR and synchronous DDR data interfaces.

After issuing a Change Read Column command, the host shall not read data until a minimum of tCCS time has elapsed. After issuing a Change Write Column command including all column address cycles, the host shall not write data until a minimum of tCCS time has elapsed. The value of tCCS shall always be longer than or equal to tWHR and tADL when the Toggle-mode DDR or Synchronous DDR data interface is supported.

Byte 163-164: I/O pin capacitance, typical or maximum

This field indicates the typical or maximum I/O pin capacitance for the target. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. If vendor datasheet is specifying the maximum value, then this field is indicating the maximum capacitance value. If vendor datasheet is specifying a typical value, then this field is indicating the typical capacitance value.

Byte 165-166: Input pin capacitance, typical or maximum

This field indicates the typical or maximum input pin capacitance for the target. This value applies to all inputs except the following: CK, CK_n, CE_n and WP_n signals. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. If vendor datasheet is specifying the maximum value, then this field is indicating the maximum capacitance value. If vendor datasheet is specifying a typical value, then this field is indicating the typical capacitance value.

Byte 167-168: CK input pin capacitance, typical or maximum

This field indicates the typical or maximum CK input pin capacitance for the target. This value applies to the CK and CK_n signals. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. This field shall be supported if the Synchronous DDR data interface is supported. If vendor datasheet is specifying the maximum value, then this field is indicating the maximum capacitance value. If vendor datasheet is specifying a typical value, then this field is indicating the typical capacitance value.

Byte 169: Driver strength support

This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings. If this bit is set to one, then the device shall support both the Nominal and Underdrive settings. If this bit is set to one, then the device shall power-on with a driver strength at the Nominal value. If this bit is cleared to zero, then the driver strength at power-on is undefined. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 1 when set to one indicates that the target supports the Overdrive 1 setting for use in the I/O Drive Strength setting. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 2 when set to one indicates that the target supports the 18 ohm setting in Table TBD for use in the I/O.

Bits 3-7 are reserved.

Byte 170-171: Program page register clear enhancement tADL value

This field indicates the ALE to data loading time (tADL) in nanoseconds when the program page register clear enhancement is enabled. If the program page register clear enhancement is disabled, then the tADL value is as defined for the selected timing mode. This increased tADL value only applies to Program (80h) command sequences; it does not apply for Set Features, Copyback, or other commands.

Byte 208: Guaranteed valid blocks at beginning of target

This field indicates the number of guaranteed valid blocks starting at block address 0 of the target. The minimum value for this field is 1h. The blocks are guaranteed to be valid for the endurance specified for this area when the host follows the specified number of bits to correct in ECC information block 0.

Byte 209-210: Block endurance for guaranteed valid blocks

This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area. This value requires that the host is using at least the minimum ECC correctability reported in ECC information block 0. This value is not encoded. If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

Byte 211-218: ECC information block 0

This block of parameters describes a set of ECC and endurance information. The parameters are related, and thus

the parameters are specified as a set.
The device may report additional ECC information in the Parameter Page. The required ECC correctability is closely related to other device parameters, like the number of valid blocks and the number of program/erase cycles supported. The additional ECC information stored in the ECC information blocks allow the device to specify multiple valid methods for using the device. Bytes 211-218 provide one valid method (i.e. ECC information block 0) for using the device. Other methods can be specified in ECC information blocks 1-3 stored in Bytes 219-242

Byte 211: Number of bits ECC correctability. This field indicates the number of bits that the host should be able to correct per codeword. The codeword size is reported in byte 212. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in bytes 215-216. When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 213-214 shall not be exceeded by the device. All used bytes in the page shall be protected by ECC including the spare bytes if the ECC requirement reported in byte 211 has a value greater than zero. When this value is cleared to zero, the target shall return valid data.

Byte 212: Codeword size. The number of bits of ECC correctability specified in byte 211 is based on a particular ECC codeword size. The ECC codeword size is specified in this field as a power of two. The minimum value that shall be reported is 512 bytes (a value of 9).

Byte 213-214: Maximum value of average bad blocks per LUN. This field contains the maximum number of average bad blocks that may be defective at manufacture and over the life of the device. The average bad blocks per LUN value can be determined by averaging the bad blocks per LUN for either the number LUNs per package or number of LUNs per target. The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this ECC and endurance information block.

Byte 215-216: Block endurance. This field indicates the maximum number of program/erase cycles per addressable page/block. This value assumes that the host is using the ECC correctability reported in byte 211. The block endurance is reported in terms of a value and a multiplier according to the following equation: value x 10multiplier. Byte 215 comprises the value. Byte 216 comprises the multiplier. For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 103). The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 105). If the value is 0000h, then no maximum number of cycles is specified.

Byte 219-226: ECC information block 1
This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 227-234: ECC information block 2
This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 235-242: ECC information block 3
This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 420-421: Vendor specific Revision number
This field indicates a vendor specific revision number. This field should be used by vendors to indicate the supported layout for the vendor specific Parameter Page area and the vendor specific feature addresses. The format of this field is vendor specific.

Byte 422-509: Vendor specific
This field is reserved for vendor specific use.

Byte 510-511: Integrity CRC
The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the Parameter Page were transferred correctly to the host. The CRC of the Parameter Page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 509 of the Parameter Page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the Parameter Page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:
G(X) = X16 + X15 + X2 + 1
This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Byte 512-1023: Redundant Parameter Page 1
This field shall contain the values of bytes 0-511 of the Parameter Page. Byte 512 is the value of byte 0.

The redundant Parameter Page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1024-1535: Redundant Parameter Page 2
This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant Parameter Page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

5.3.14. Read Status Enhanced

Read Status Enhanced function is used to check status of selected LUN and Plane specified by row address setting. Thus, the function requires row address setting steps before reading status value. Table 51 defines status values of each operation and Figure 76 defines Read Status Enhanced behavior and timings.

Table 51 Read Status Enhanced Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : “0” Not Protected : “1”
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Copy-Back	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0 is only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0 is only valid when DQ 5 shows the Ready state, and DQ 1 is only valid when DQ 6 shows the Ready state.

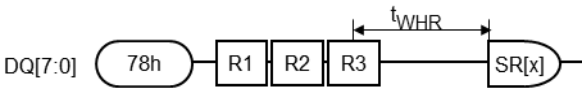


Figure 76. Read Status Timing

5.3.15. Read LUN #0 Status Operation

Read LUN#0 Status provides status value of LUN#0 without address setting. The function retrieves plane0 and plane1 status only. Table 52 defines the status values and Figure 77 defines Read LUN#0 Status behavior and timings.

Table 52 Read LUN#0 Status Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for LUN#0	Pass/Fail for Plane#0 (N)	Pass/Fail for Plane#1(N)	Pass/Fail for Plane#0 (N-1)	Pass/Fail for Plane#1(N-1)	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Copy-Back	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ 5 shows the Ready state, and DQ 3 and DQ 4 are only valid when DQ 6 shows the Ready state.

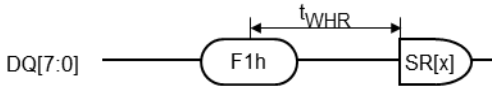


Figure 77. Read LUN#0 Status Timing

5.4. _Interleaving Operation

When multiple LUNs share a common $\overline{CE}$, it provides interleaving operation between LUNs.
At first, the host issues an operation command to one of the LSB chips, say (LUN #0). Due to DDP device goes into busy state. During this time, MSB chip (LUN #1) is in ready state. So it can execute the operation command issued by the host.
After the execution of operation by LSB chip (LUN #0), it can execute another operation regardless of MSB chip (LUN #1). Before that the host needs to check the status of LSB chip (LUN #0) by issuing 78h/F1h command. Only when the status of LSB chip (LUN #0) becomes ready status, host can issue another operation command. If LSB chip (LUN #0) is in busy state, the host has to wait for LSB chip (LUN #0) to get into ready state.
Similarly, MSB chip (LUN #1) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (LUN #1) by issuing 78h/F2h command. When MSB chip (LUN #1) goes ready state, host can issue another operation command to MSB chip (LUN #1).
This interleaving operation helps the system improve the system throughput.

NOTE :
During interleave operations, the following command input and operations are prohibited.
Command Input : 70h/71h command input.
Operations : Sequential/Random Cache Read, Multi Page Cache Read, Multi Page Random Cache Read, Cache Program, Multi Page Cache Program, Page Copy (2), Multi Page Copy (2), and combination of these operations.

5.4.1. Interleaving Page Program

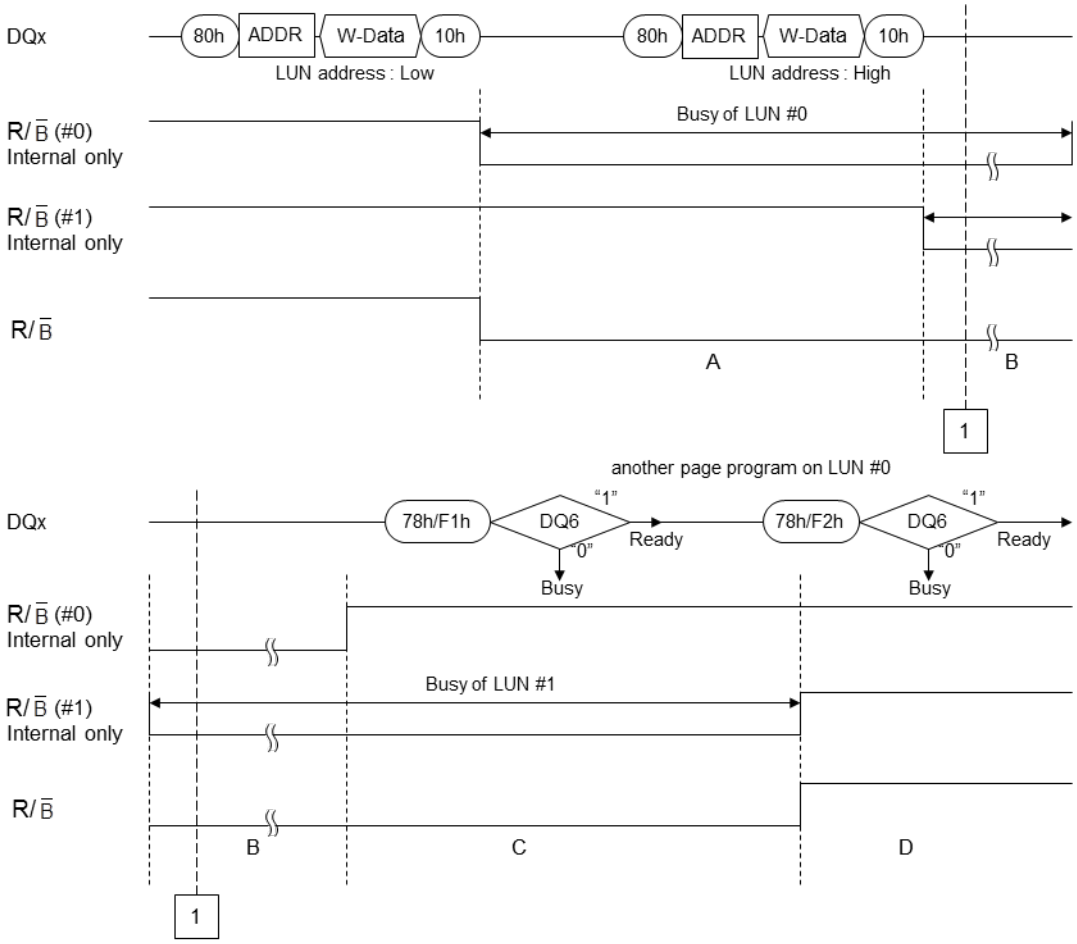


Figure 78. Example Timing with Interleaving Page Program

State A : LUN #0 is executing page program operation and LUN #1 is in ready state. So the host can issue page program command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing page program operation.

State C : Page program on LUN #0 is completed, but page program on LUN #1 is still ongoing. And the system should issue 78h/F1h command to detect the status of LUN #0. If LUN #0 is ready, status DQ6 is "1" and the system can issue another page program command to LUN #0.

State D : Both of LUN #0 and LUN #1 are ready.

According to the above process, the system can operate page program on LUN #0 and LUN #1 alternately.

5.4.2. Interleaving Page Read

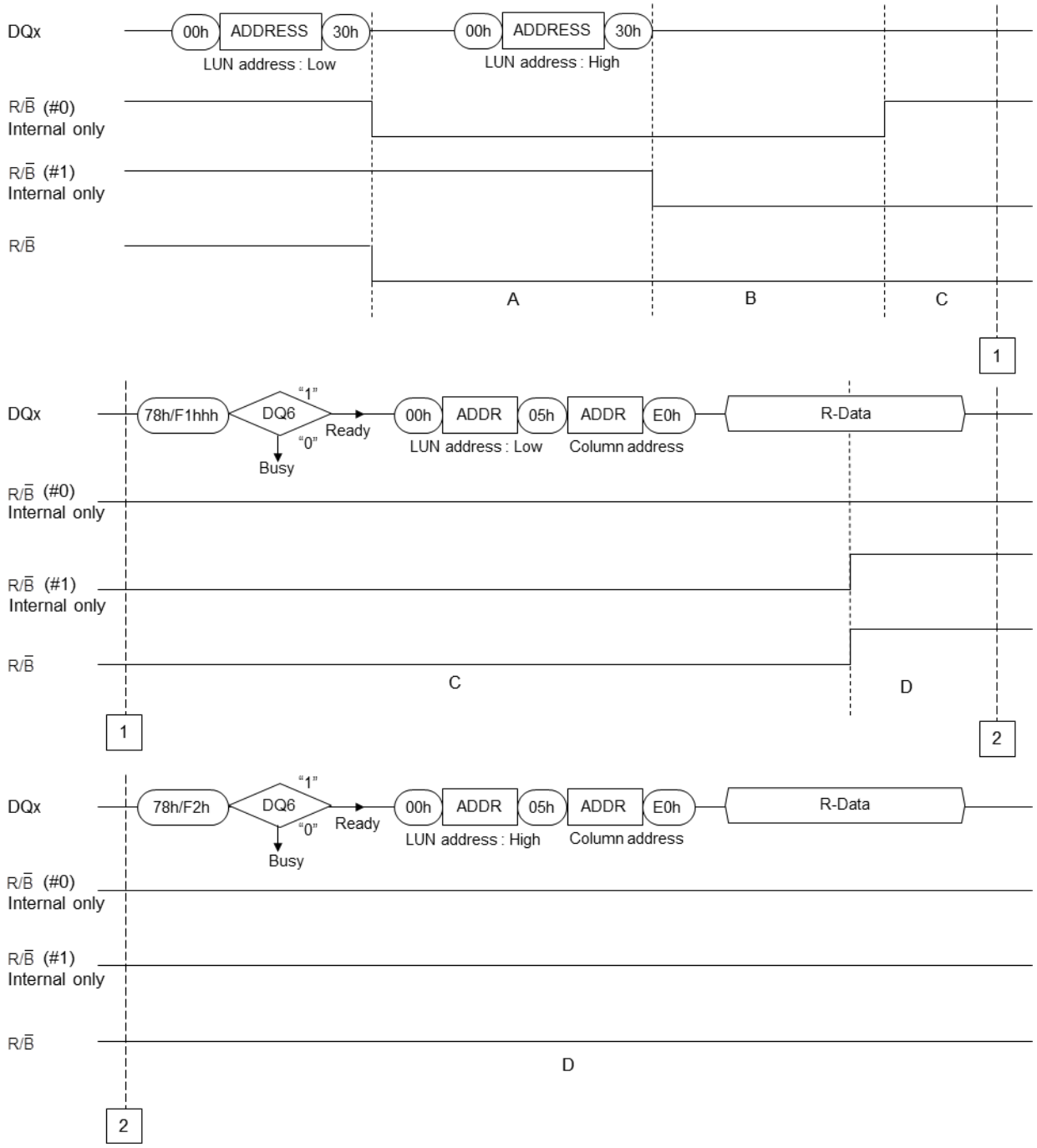


Figure 79. Example Timing with Interleaving Page Read

State A : LUN #0 is executing page read operation, and LUN #1 is in ready state. So the host can issue page read command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing page read operation.

State C : Page read on LUN #0 is completed and LUN #1 is still executing page read operation. Before the host read the data, the host shall check the Ready/Busy status for LUN0 by 78h/F1h commands. Host can read the data from the LUN0 whose status indicates Ready state.

State D : Page read on LUN#1 is completed. Before the host read the data, the host shall check the Ready/Busy status for LUN1 by 78h/F2h commands. Host can read the data from the LUN1 whose status indicates Ready state.

NOTE :

*78h/F1h command is required to check the status of LUN #0.

*78h/F2h command is required to check the status of LUN #1.

5.4.3. Interleaving Block Erase

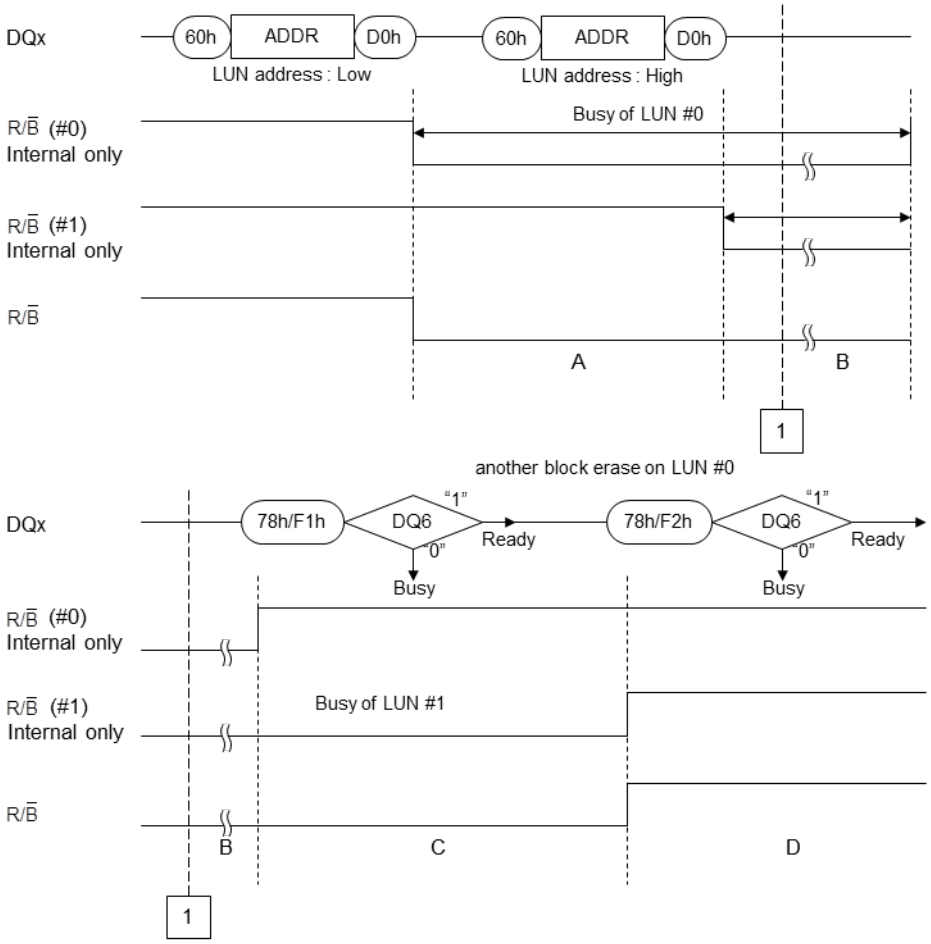


Figure 80. Example Timing with Interleaving Block Erase

State A : LUN #0 is executing block erase operation, and LUN #1 is in ready state. So the host can issue block erase command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing block erase operation.

State C : Block erase on LUN #0 is completed, but block erase on LUN #1 is still operating. And the system should issue F1h command to detect the status of LUN #0. If LUN #0 is ready, status DQ6 is "1" and the system can issue another block erase command to LUN #0.

State D : LUN #0 and LUN #1 are ready.

According to the above process, the system can operate block erase on LUN #0 and LUN #1 alternately.

5.4.4. Interleaving Multi Page Program

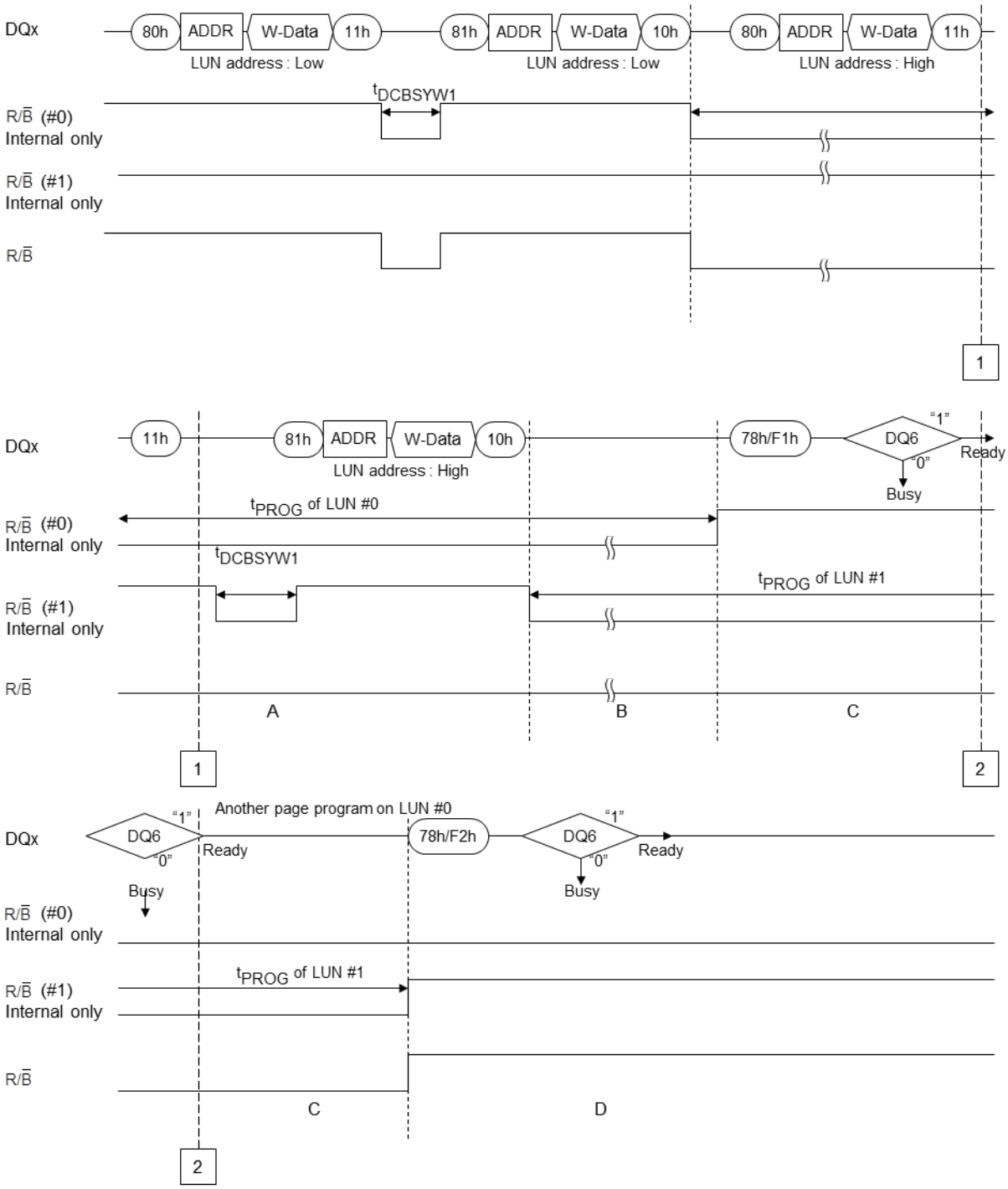


Figure 81. Example Timing with Interleaving Multi Page Program

State A : LUN #0 is executing Multi Page Program operation, and LUN #1 is in ready state. So the host can issue Multi Page Program command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing Multi Page Program operation.

State C : Multi Page Program on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Multi Page Program operation.

State D : Both LUN #0 and LUN #1 are ready.

According to the above process, the system can operate multi page program on LUN #0 and LUN #1 alternately.

NOTE :

*78h/F1h command is required to check the status of LUN #0 to issue the next page program command to LUN #0.

*78h/F2h command is required to check the status of LUN #1 to issue the next page program command to LUN #1.

5.4.5. Interleaving Multi Page Read

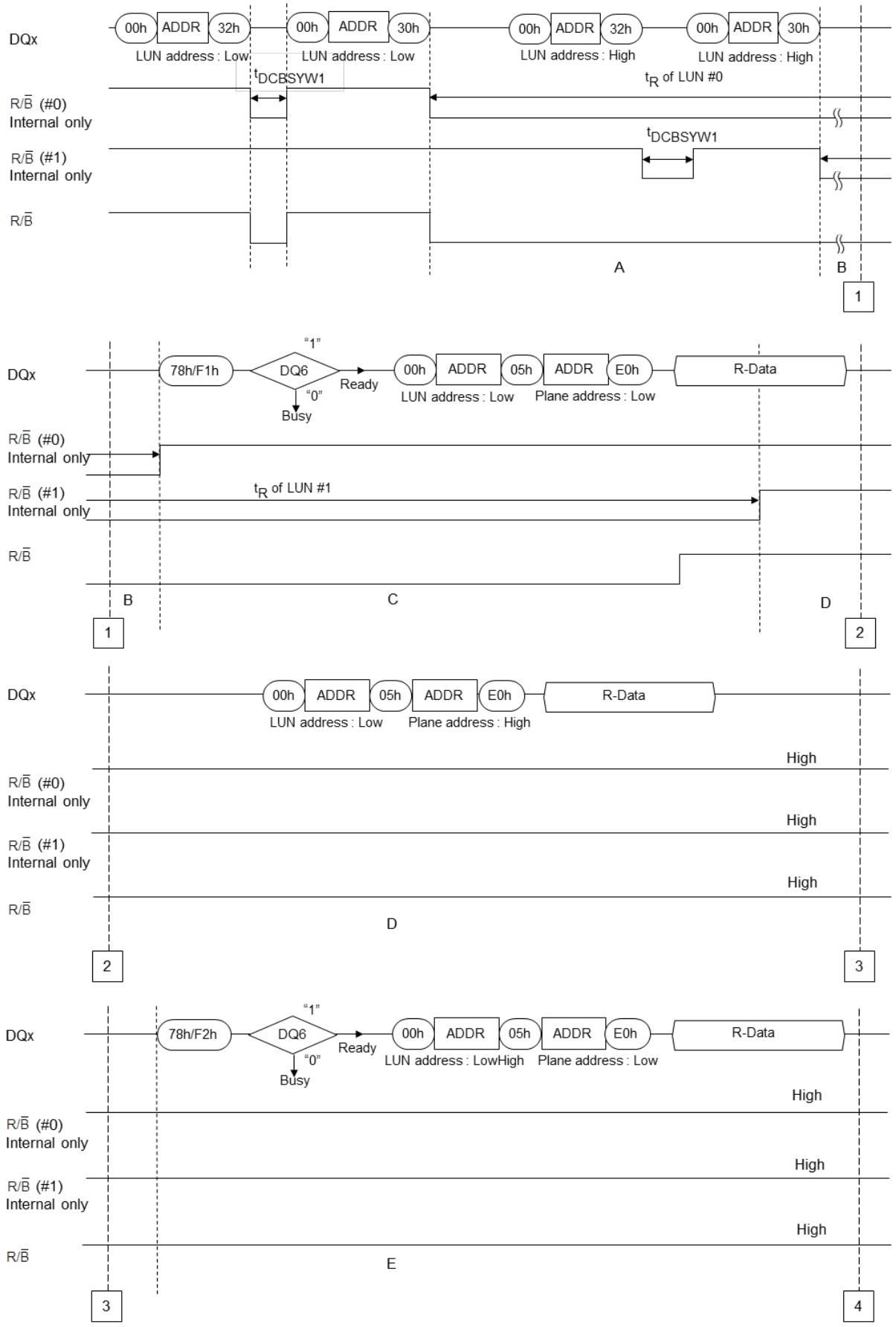


Figure 82 Example Timing with Interleaving Multi Page Read

State A : LUN #0 is executing Multi Page Read operation, and LUN #1 is in ready state. So the host can issue Multi Page Read command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing Multi Page Read operation.

State C : Multi Page Read on LUN #0 is completed and LUN #1 is still executing Multi Page Read operation. Before the host read the data, the host shall check the Ready/Busy status for LUN0 by 78/F1h commands. Host can read he data from the LUN#0 whose status indicates Ready state.

State D : Multi Page Read on LUN#1 is completed. Both LUN #0 and LUN #1 are ready.

State E : Before the host read the data from LUN#1, the host shall check the Ready/Busy status for LUN#1 by 78/F2h commands. Host can read he data from the LUN#1 whose status indicates Ready state.

According to the above process, the system can operate multi page read on LUN #0 and LUN #1 alternately.

NOTE :

*78h/F1h command is required to check the status of LUN #0 to issue the next page read command to LUN #0.

*78h/F2h command is required to check the status of LUN #1 to issue the next page read command to LUN #1.

5.4.6. Interleaving Multi Block Erase

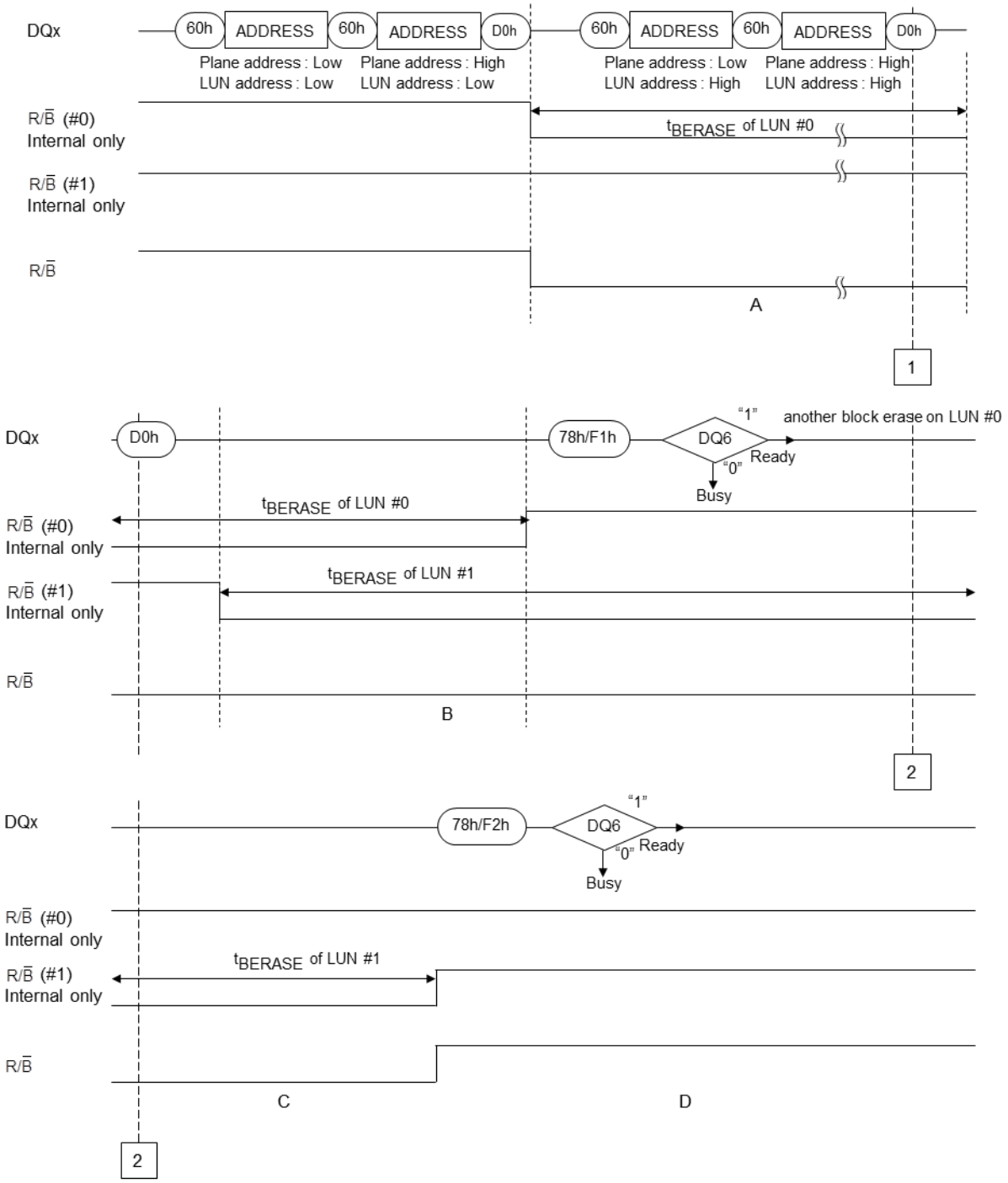


Figure 83. Example Timing with Interleaving Multi Block Erase

State A : LUN #0 is executing Multi Block Erase operation, and LUN #1 is in ready state. So the host can issue Multi Block Erase command to LUN #1.

State B : Both LUN #0 and LUN #1 are executing Multi Block Erase operation.

State C : Multi Block Erase on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Multi Block Erase operation.

State D : Both LUN #0 and LUN #1 are ready.

According to the above process, the system can operate multi block erase on LUN #0 and LUN #1 alternately.

NOTE :

*78h/F1h command is required to check the status of LUN #0 to issue the next block erase command to LUN #0.

*78h/F2h command is required to check the status of LUN #1 to issue the next block erase command to LUN #1.

5.4.7. Interleaving Read to Page Program

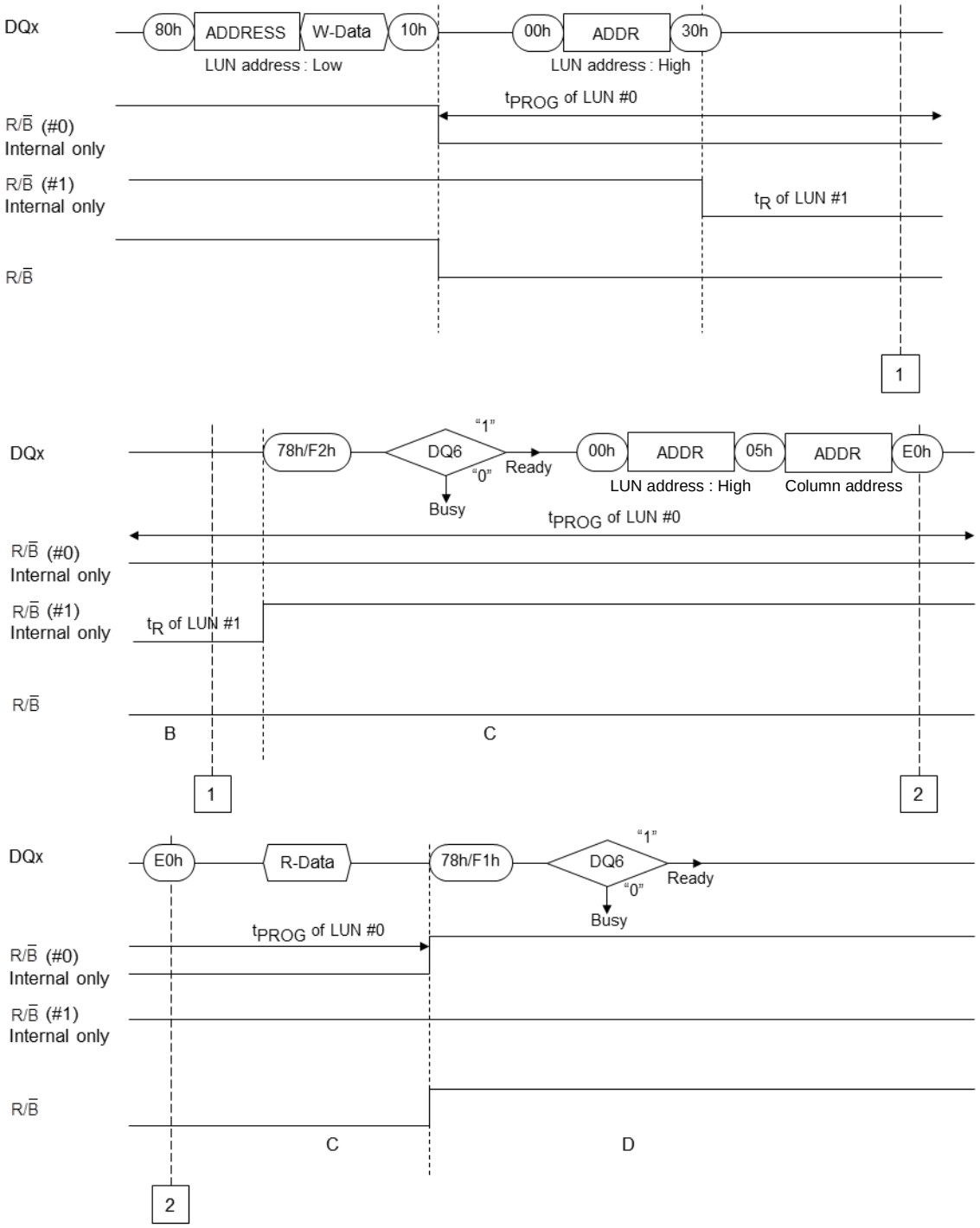


Figure 84. Example Timing with Interleaving Read to Page Program

State A : LUN #0 is executing page program operation, and LUN #1 is in ready state. So the host can issue read command to LUN #1.

State B : Both LUN #0 is executing page program operation and LUN #1 is executing read operation.

State C : Read operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing page program operation.

State D : Both LUN #0 and LUN #1 are ready.

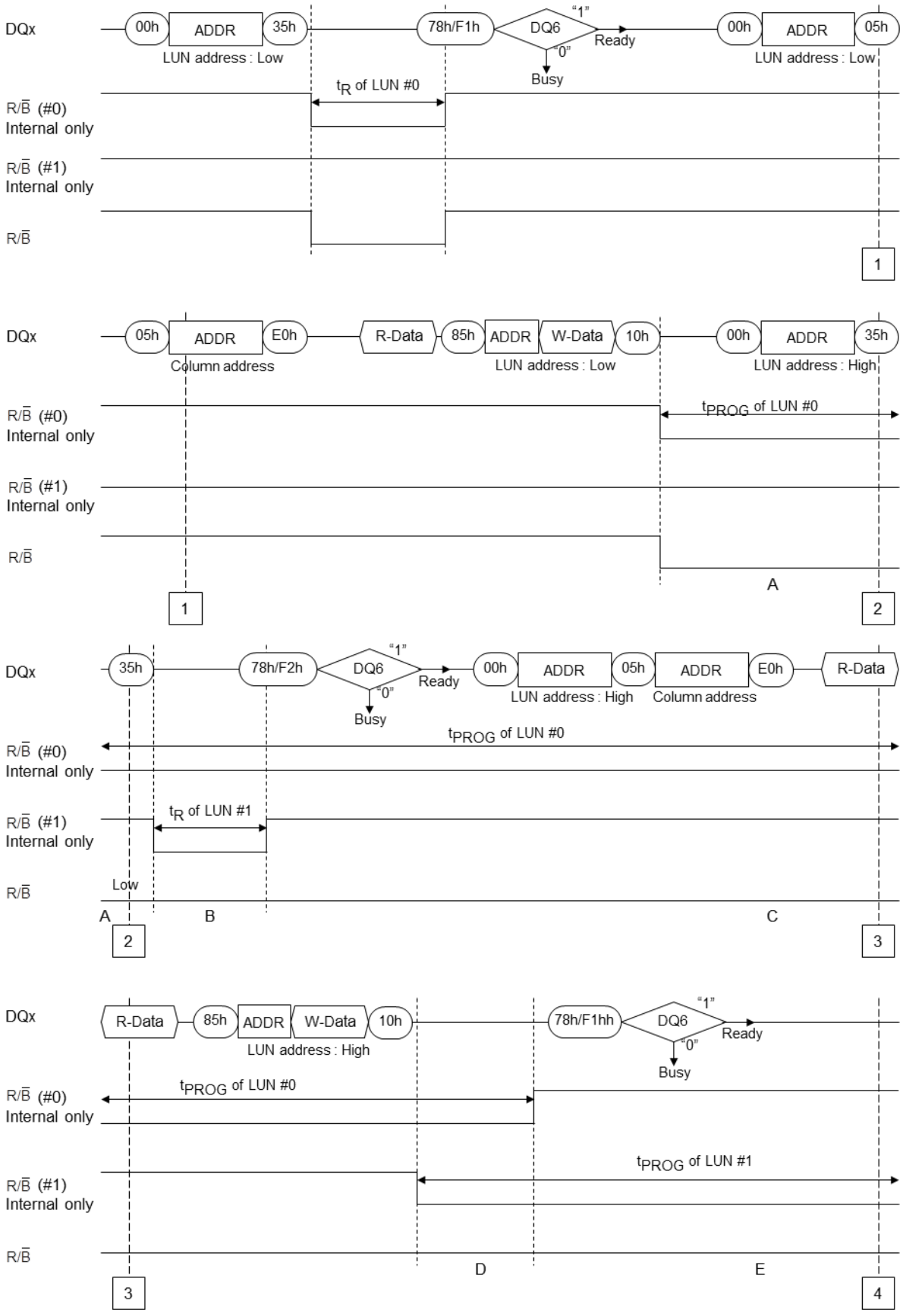
According to the above process, the system can operate read to page program on LUN #0 and LUN #1 alternatively.

NOTE :

*78h/F1h command is required to check the status of LUN #0 to issue the next command to LUN #0.

*78h/F2h command is required to check the status of LUN #1 to issue the next command to LUN #1.

5.4.8. Interleaving Copy-Back Program (1/2)



5.4.9. Interleaving Copy-Back Program (2/2)

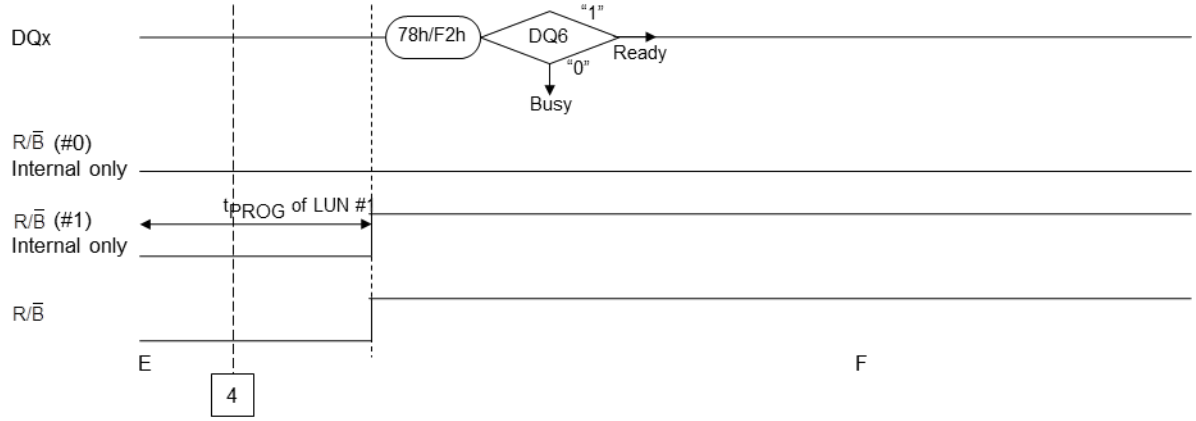


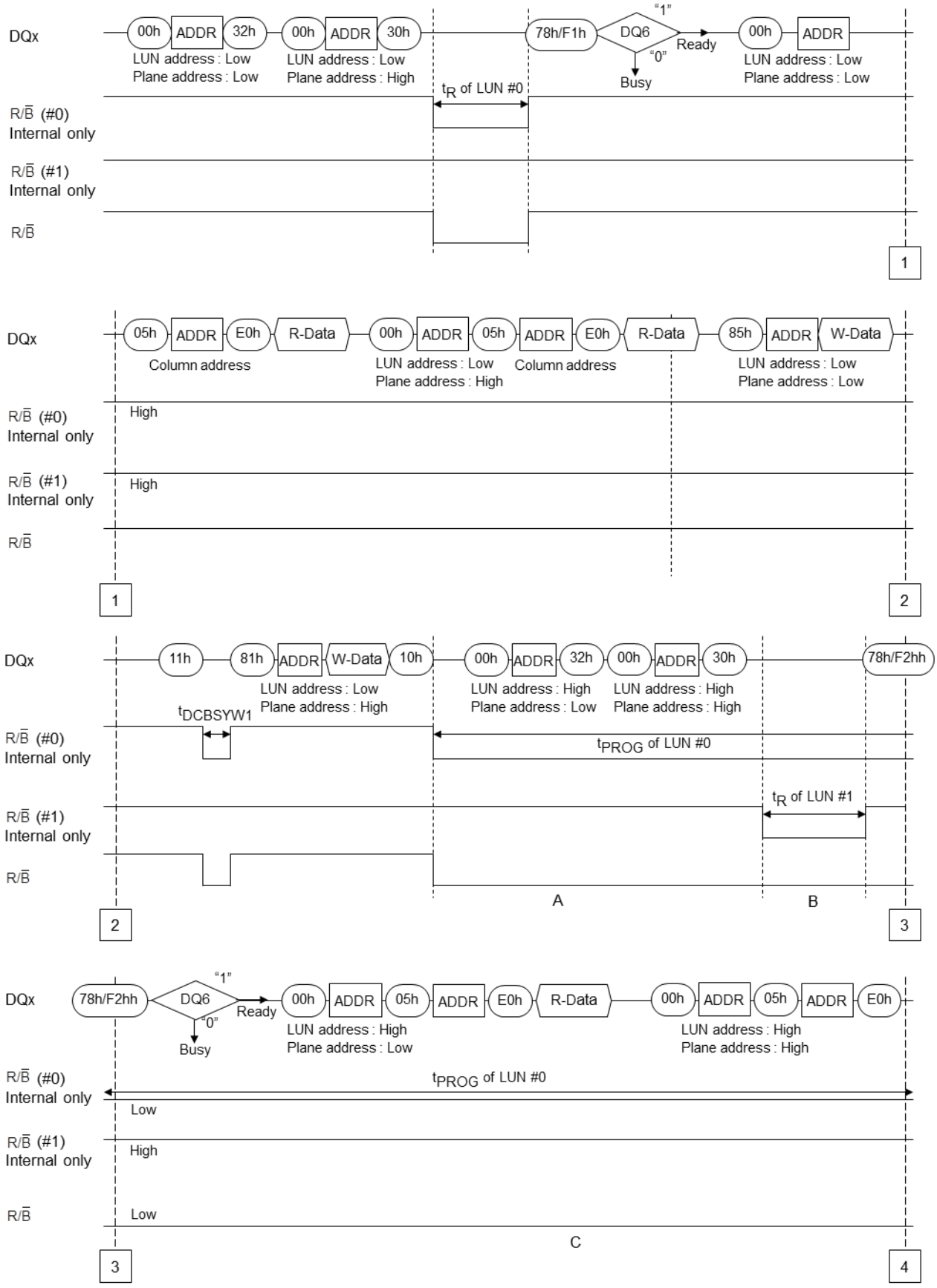
Figure 85. Example Timing with Interleaving Copy-Back Program

State A : LUN #0 is executing copy-back program operation, and LUN #1 is in ready state. So the host can issue read for copy-back command to LUN #1.
State B : LUN #0 is executing copy-back program operation and LUN #1 is executing read for copy-back operation.
State C : Read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing copy-back program operation.
State D : Both LUN #0 and LUN #1 are executing copy-back program operation.
State E : LUN #1 is still executing a copy-back program operation, and LUN #0 is in ready for the next operation.
State F : Both LUN #0 and LUN #1 are ready.

NOTE :
*78h/F1h command is required to check the status of LUN #0 to issue the next command to LUN #0.
*78h/F2h command is required to check the status of LUN #1 to issue the next command to LUN #1

According to the above process, the system can operate Interleave copy-back program on LUN #0 and LUN #1 alternatively

5.4.10. Interleaving Multi Copy Back Program (1/2)



5.4.11. Interleaving Multi Copy Back Program (2/2)

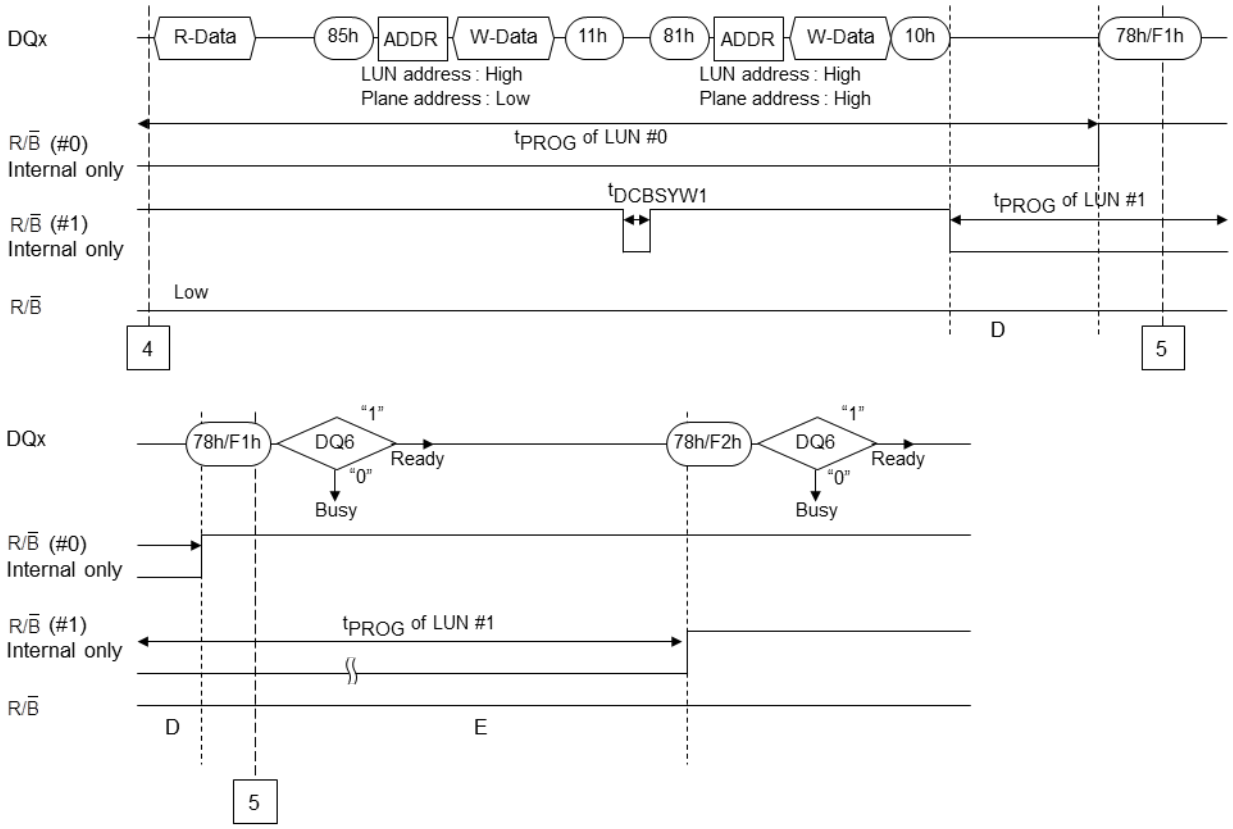


Figure 86. Example Timing with Interleaving Multi Copy-Back Program

State A : LUN #0 is executing Multi Copy-Back Program operation, and LUN #1 is in ready state. So the host can issue Multi Read for copy-back command to LUN #1.

State B : LUN #0 is executing Multi Copy-Back Program operation and LUN #1 is executing Multi Read for copy-back operation.

State C : Multi Read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing Multi Copy-Back Program operation.

State D : Both LUN #0 and LUN #1 are executing Multi Copy-Back Program operation.

State E : LUN #1 is still executing a Multi Copy-Back Program operation, and LUN #0 is in ready for the next operation.

State F : Both LUN #0 and LUN #1 are ready.

NOTE :

*78h/F1h command is required to check the status of LUN #0 to issue the next command to LUN #0.

*78h/F2h command is required to check the status of LUN #1 to issue the next command to LUN #1.

According to the above process, the system can operate Interleave Multi Copy-Back Program on LUN #0 and LUN #1 alternatively.

6. APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

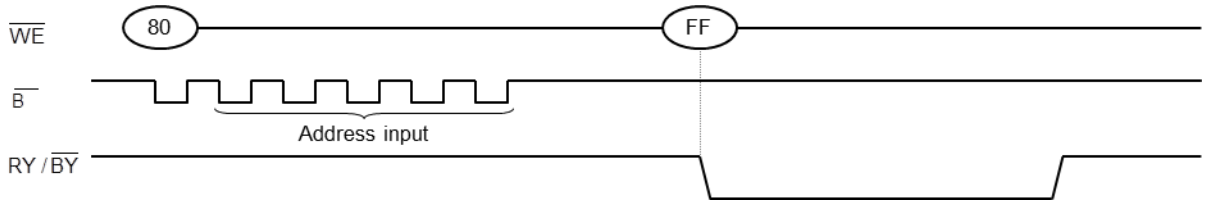
Input of a command other than those specified in this document is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Restriction of commands while in the Busy state

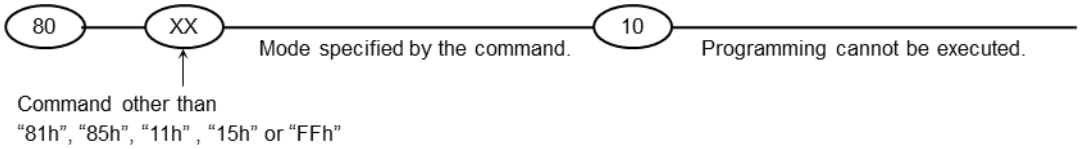
During the Busy state, do not input any command except 70h, 71h, 78h, F1h and FFh.

(3) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Multi Page Program command "81h", the Random Data Input command "85h", Multi Page Program command "11h", Cache Program command "15h" or the Reset command "FFh" until Page Program command "10h" is input.

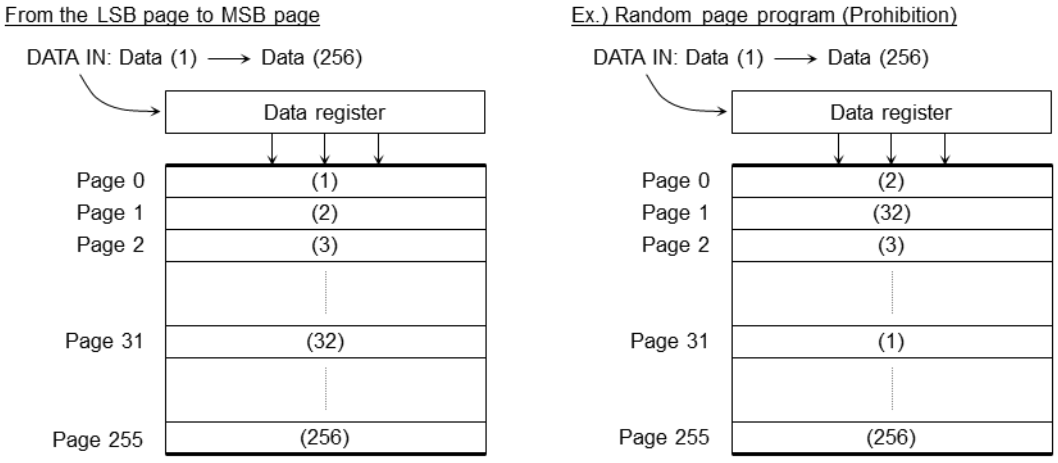


If a command other than "81h", "85h", "11h" , "15h"or "FFh" command is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

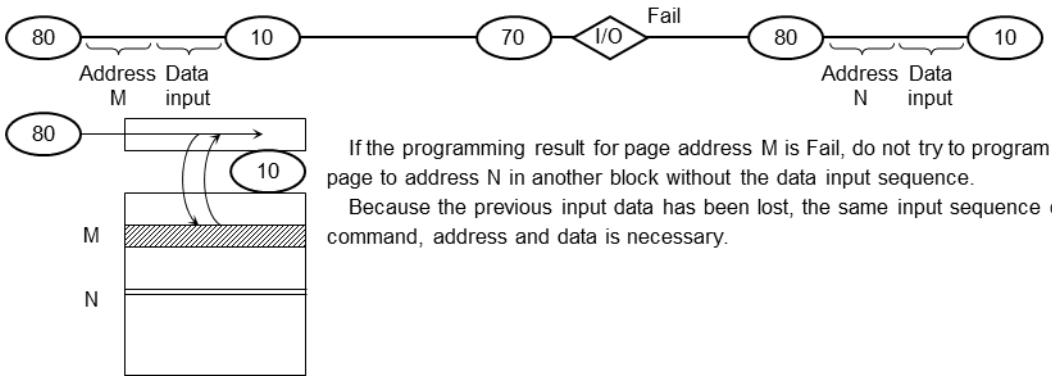


(4) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.



(5) Programming failure

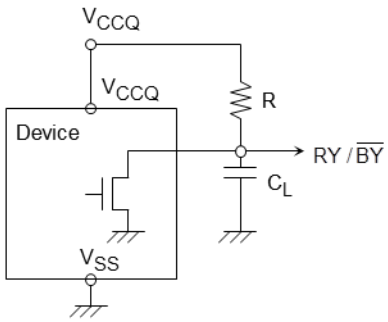


If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

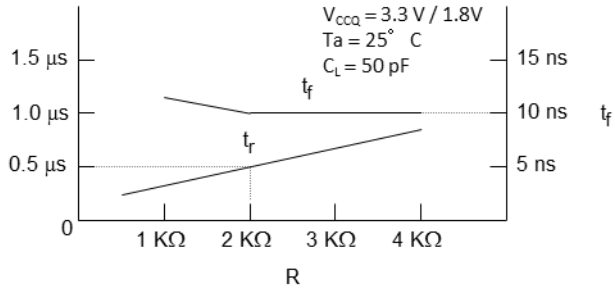
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(6) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.

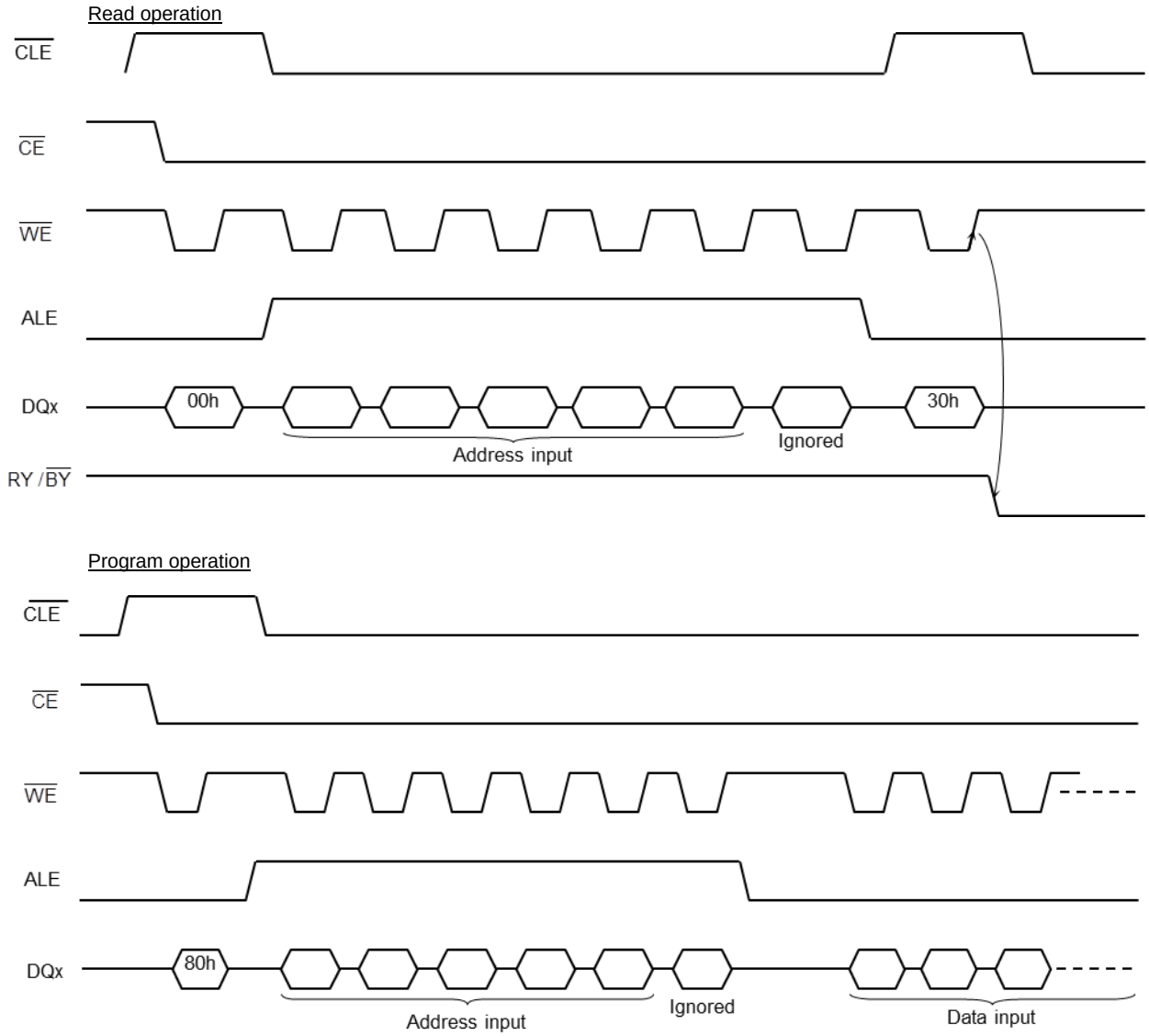


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.



(7) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

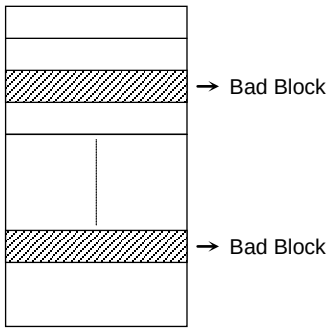


(8) Several programming cycles on the same page (Partial Page Program)

This device does not support partial page programming.

(9) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

Refer to section 2.8 for the number of valid blocks over the device lifetime.

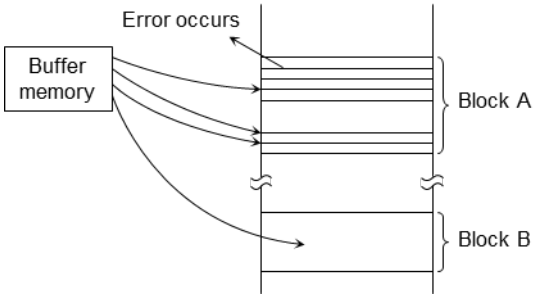
(10) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Random Bit	Programming Failure “1 to 0”	ECC

- ECC: TBD
- Block Replacement

Program



Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(11) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(12) If FF reset command is input before completion of write operation to page B, it may cause damage to data not only to the programmed page, but also to the adjacent page A as follows.

Page A	Page B	Page A	Page B
0	2	⋮	⋮
1	4	⋮	⋮
3	6	⋮	
5	8	225	228
7	10	227	230
9	12	229	232
11	14	231	234
13	16	233	236
15	18	235	238
17	20	237	240
19	22	239	242
21	24	241	244
23	26	243	246
25	28	245	248
27	30	247	250
⋮	⋮	249	252
⋮	⋮	251	254
⋮	⋮	253	255

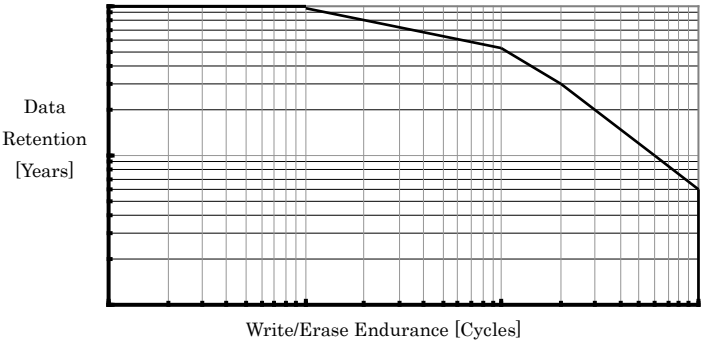
(13) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using MLC NAND flash with TBD
For detailed reliability data, please refer to TOSHIBA's reliability note.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad.
Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The other failure modes may be recovered by a block erase.
ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

- **Write/Erase Endurance**
  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either a program or a block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- **Data Retention**
  The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

  Here is the combined characteristics image of Write/Erase Endurance and Data Retention.

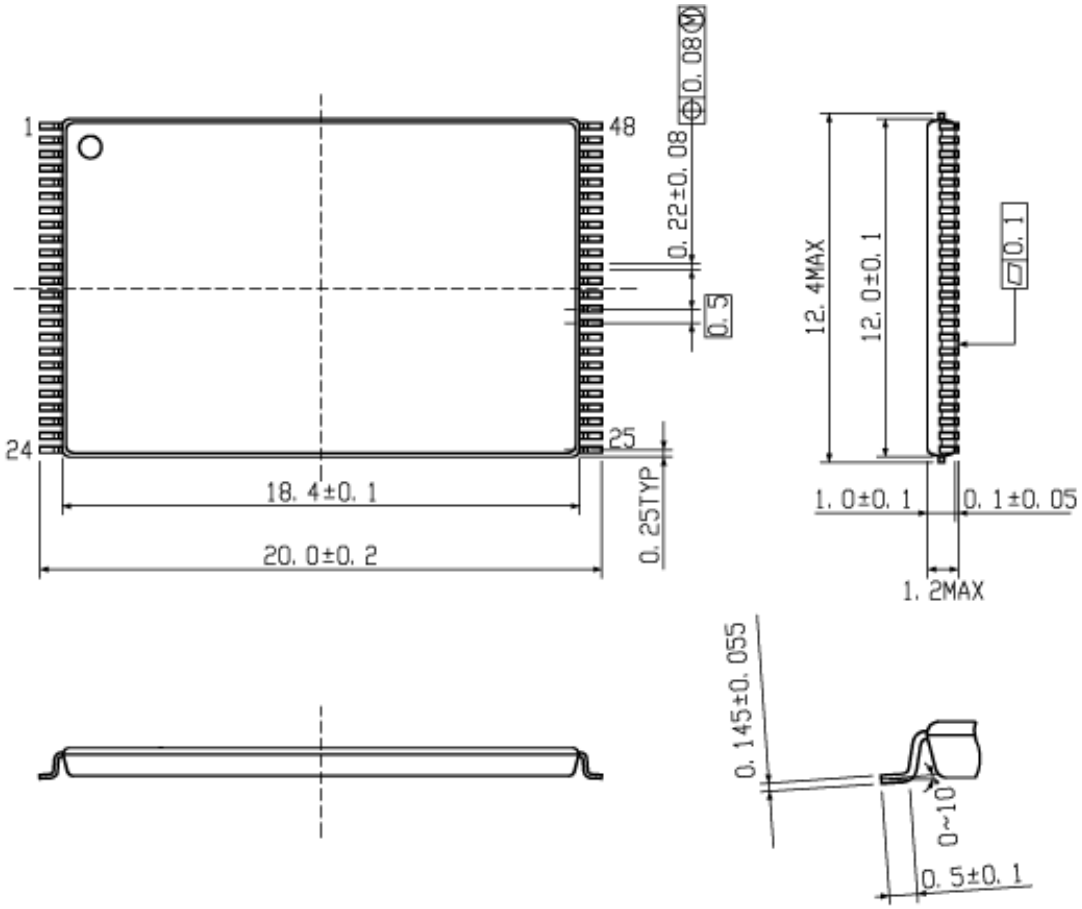


- **Read Disturb**
  A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

(14) Randomizing function

Controller shall employ randomizing function. All the columns within a page and across all pages within a block shall be filled with randomized data at programming. The randomized data for a block shall be differentiated by each programming and erase cycle.

7. Package Dimensions



8. Revision History

Date	Rev.	Description
2012-11-28	0.0	Initial issue
2013-04-02	0.1	Corrected the typographical errors.
2013-04-05	0.2	Corrected the valid block number.
2013-04-12	0.3	Updated the Parameter Page definition
2013-04-26	0.4	Ammended VPP related items (VPP Initialization, VPP current). Updated figure for Functional Representation of ODT.
2013-06-24	0.5	Amended Power-on/off sequence description. Added Interleaving Multi Page Read Operation. Amended Interleaving Page Read Operation. Clarification for Status Read Cycle. Editorial correction for tWHR/tWHR1 in SDR mode. AC Test Condition Updates.
2013-07-10	0.6	Corrected the figure of Target Organization.

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). ** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**