TEA6420

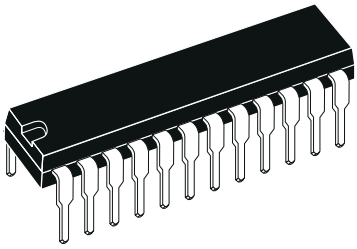
BUS-CONTROLLED AUDIO MATRIX SWITCH

- 5 Stereo Inputs
- 4 Stereo Ouputs
- Gain Control 0/2/4/6dB/Mute for each Output
- cascadable (2 different addresses)
- Serial Bus Controlled
- Very low Noise
- Very low Distorsion

DESCRIPTION

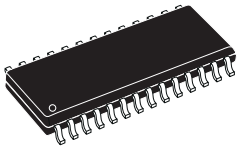
The TEA6420 switches 5 stereo audio inputs on 4stereo outputs.

All the switching possibilities are changed through the I^2C bus.



SHRINK DIP 24
(Plastic Package)

ORDER CODE: TEA6420



SO28
(Plastic Micropackage)

ORDER CODE: TEA6420D

Figure 1. PIN CONNECTIONS

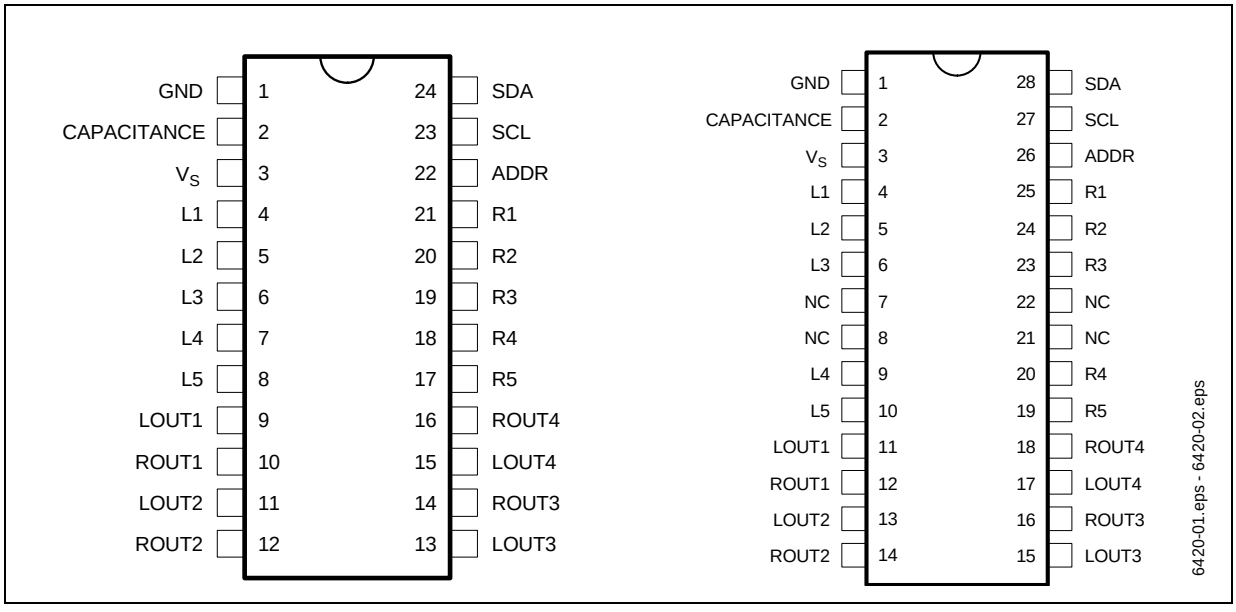
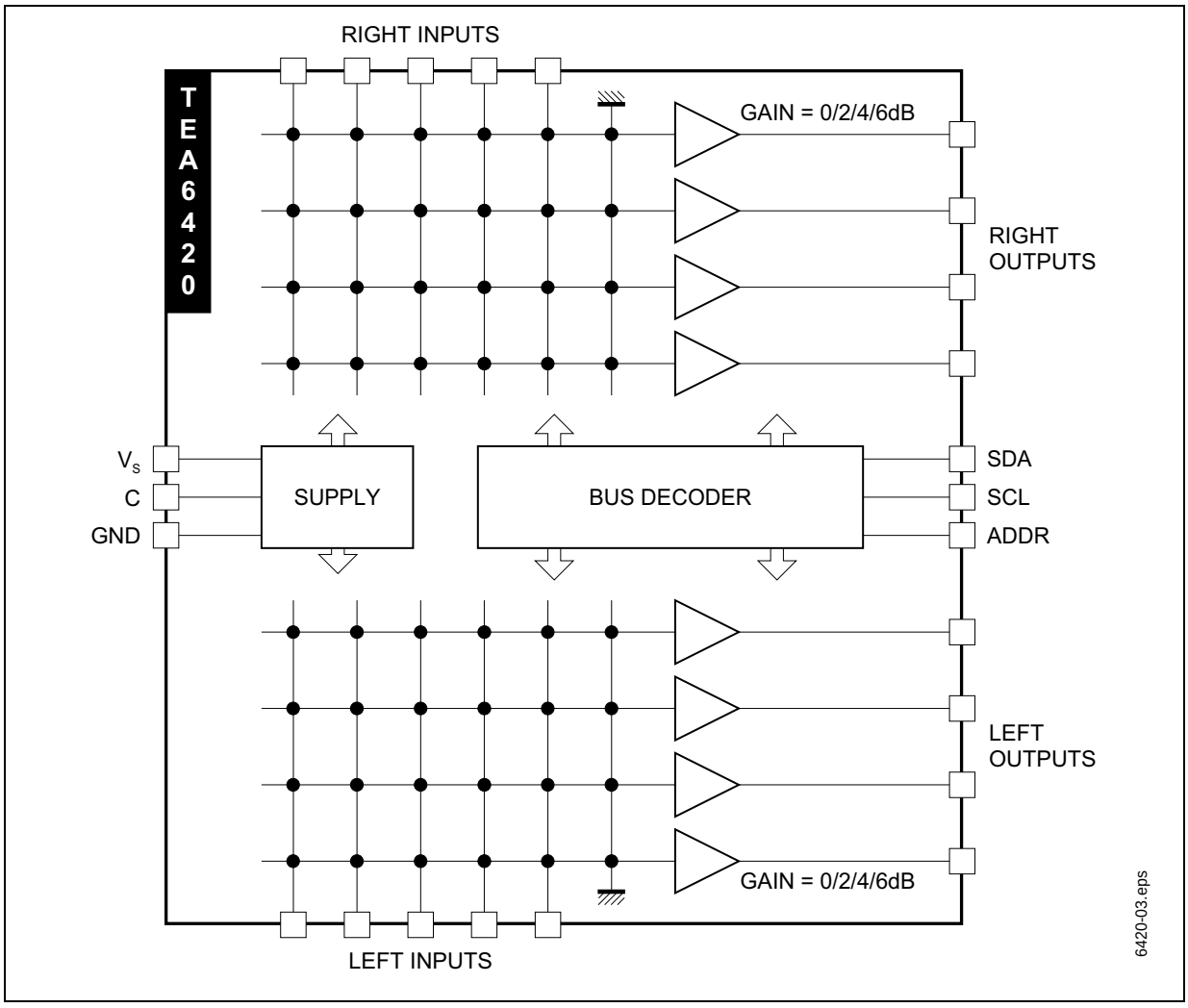


Figure 2. BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 9)	12	V
T_{OPER}	Operating Ambient Temperature Range	0 to +70	^oC
T_{stg}	Storage Temperature Range	-20 to +150	^oC

THERMAL DATA

Symbol	Parameter+		Value	Unit
R_{th}(j-a)	Junction-Ambient Thermal Resistance	SDIP24 SO28	75 75	$^oC/W$

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_S = 10V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	9	10.2	V
I_S	Supply Current			5	8	mA
SVR	Ripple Rejection	$V_{IN} = 500mV_{RMS}$, BW = 20 - 20kHz	70	80		dB
MATRIX						
V_{IN}	Input DC Level		4.5	5	5.5	V
R_I	Input Resistance		30	50	100	kΩ
C_S	Channel Separation	$V_{IN} = 2V_{RMS}$ Gain = 0dB f = 1kHz Gain = 6dB	80 70	90 82		dB dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level		4.5	5	5.5	V
R_{OUT}	Output Resistance			70	200	W
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		µV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G_{min}	Min. Gain		-1	0	+ 1	dB
G_{max}	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			kΩ
BUS INPUT						
V_{IL}	Input Low Voltage				1.5	V
V_{IN}	Input High Voltage		3			V
I_I	Input Current		- 10		10	µA
V_O	Output Voltage	I_O = 3mA ; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note	40	50		kΩ

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select								
X	0 0 1 1	0 1 0 1	G_1	G_0	I_2	I_1	I_0	Output 1 Output 2 Output 3 Output 4
Input select								
X	Q_1	Q0	G_1	G_0	0 0 0 0 1 1	0 0 1 1 0 0	0 1 0 1 0 1	Input 1 Input 2 Input 3 Input 4 Input 5 Mute
Gain select								
X	Q_1	Q0	0 0 1 1	0 1 0 1	I_2	I_1	I_0	Gain = 6 dB Gain = 4 dB Gain = 2 dB Gain = 0 dB

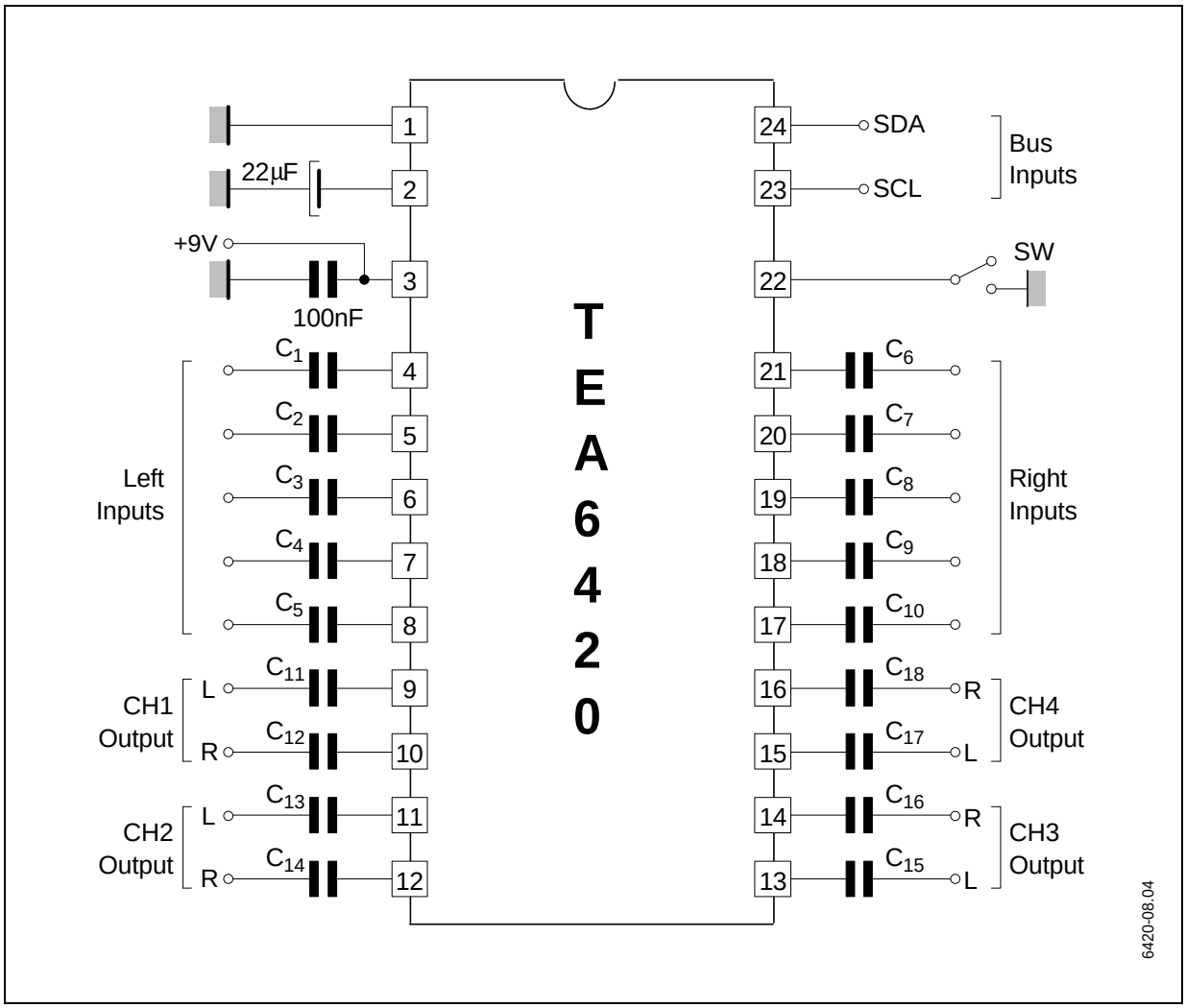
X = don't care - MSB is transmitted first

Example : X1001100 connects output 3 with input 5 at a gain of 4dB

The following are selected after power-on reset : input 5 selected for all outputs ; gain = 0dB.

TYPICAL APPLICATION

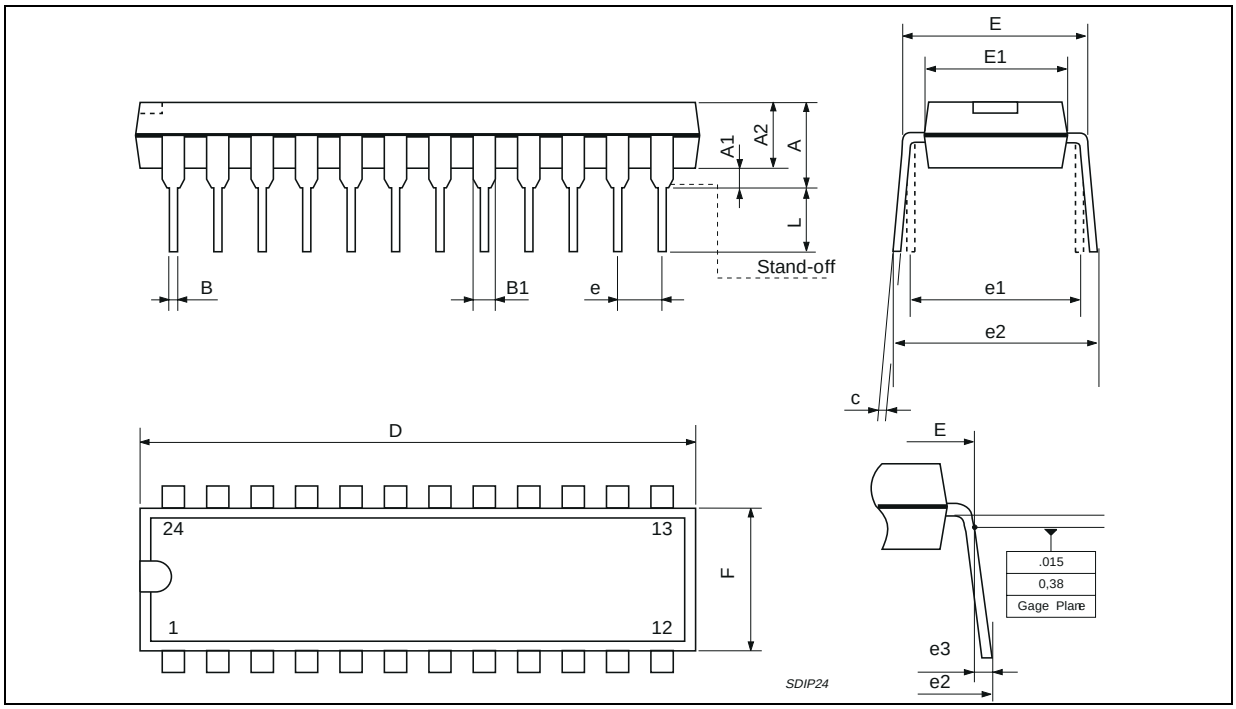
Figure 3.



PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP

Figure 4. 24-Pin Package



28 PINS - PLASTIC SO

Figure 5. 28-Pin Package