# TEA2016AAT/2

## Digital controller for high-efficiency resonant power supply

Rev. 1 — 15 February 2023 Product data sheet

## 1 General description

The TEA2016AAT is a digital configurable LLC and PFC combo controller for high-efficiency resonant power supplies. It includes both the LLC controller functionality and PFC controller operating in DCM and QR mode. The TEA2016AAT enables building a complete resonant power supply which is easy to design and has a very low component count. The TEA2016AAT comes in a low profile and narrow body-width SO16 package.

The TEA2016AAT digital architecture is based on a high-speed configurable hardware state machine ensuring very reliable real-time performance. During the power supply development, many operation and protection settings of the LLC and PFC controller can be adjusted by loading new settings into the device to meet specific application requirements. The configurations can be fully secured to prevent unauthorized copying of the proprietary TEA2016AAT configuration content.

In contrast to traditional resonant topologies, the TEA2016AAT shows a very high efficiency at low loads due to the low-power mode. This mode operates in the power region between continuous switching (also called high-power mode) and burst mode.

Because the TEA2016AAT regulates the output voltage of the system via the primary capacitor voltage, it has accurate information about the power delivered to the output. This measured output power defines the mode of operation (burst mode, low-power mode, or high-power mode). The transition levels of the operating modes can be easily programmed into the device.

The TEA2016AAT contains all protections like overtemperature protection (OTP), overcurrent protection (OCP), overvoltage protection (OVP), overpower protection (OPP), open-loop protection (OLP), and capacitive mode regulation (CMR). Each of these protections can be configured independently and accurately by programming parameters inside the device.

The device contains both a low-voltage and high-voltage silicon technology for high-voltage start-up, integrated drivers, level shifter, protections, and circuitry assuring zero-voltage switching.

The TEA2016AAT/TEA2095T combination gives an easy to design, highly efficient, and reliable power supply, providing 90 W to 500 W, with a minimum of external components. The system provides a very low no-load input power (< 75 mW; total system including the TEA2016AAT/TEA2095T combination) and high efficiency from minimum to maximum load. This power supply meets the efficiency regulations of Energy Star, the Department of Energy, the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. So, any auxiliary low-power supply can be omitted.

# 2 Features and benefits

## 2.1 Distinctive features

- Complete functionality of LLC and PFC controller in single small-size SO16 package
- Integrated high-voltage start-up
- Integrated drivers and high-voltage level shifter (LS)
- High-side driver directly supplied from the low-side driver output (patent nr 82059363US01)
- Accurate boost voltage regulation
- Integrated X-capacitor discharge without additional external components
- Power good function
- Several parameters can easily be configured, like:
  - Operating frequencies to be outside the audible area at all operating modes
  - Soft start and soft stop in burst mode, reducing the audible noise
  - Accurate transition levels between operation modes (high-power mode/low-power mode/burst mode)

## 2.2 Green features

- Valley/zero voltage switching for minimum switching losses
- Extremely high efficiency from low load to high load
- Compliant with latest energy-saving standards and directives (Energy Star, EuP)
- Excellent no-load input power (< 75 mW for TEA2016AAT/TEA2095T combination)

## 2.3 Protection features

- Independently configurable levels and timers
- All protections can independently be set to latched, safe restart, or latched after several attempts to restart (Patent nr. 82096505US01)
- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- Internal and external overtemperature protection (OTP)
- Capacitive mode regulation (CMR)
- Accurate overvoltage protection (OVP)
- Overcurrent protection (OCP)
- Inrush current protection (ICP)
- Brownin/brownout protection
- Disable input

# 3 Applications

- Desktop and all-in-one PCs
- Gaming power supplies
- Notebook adapter and general-purpose adapters
- Printers
- UHD LED television

# 4 Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TEA2016AAT/2 | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

# 5 Marking

**Table 2. Marking code**

| Type number | Marking code |
|---|---|
| TEA2016AAT/2 | TEA2016AAT |

# 6 Block diagram

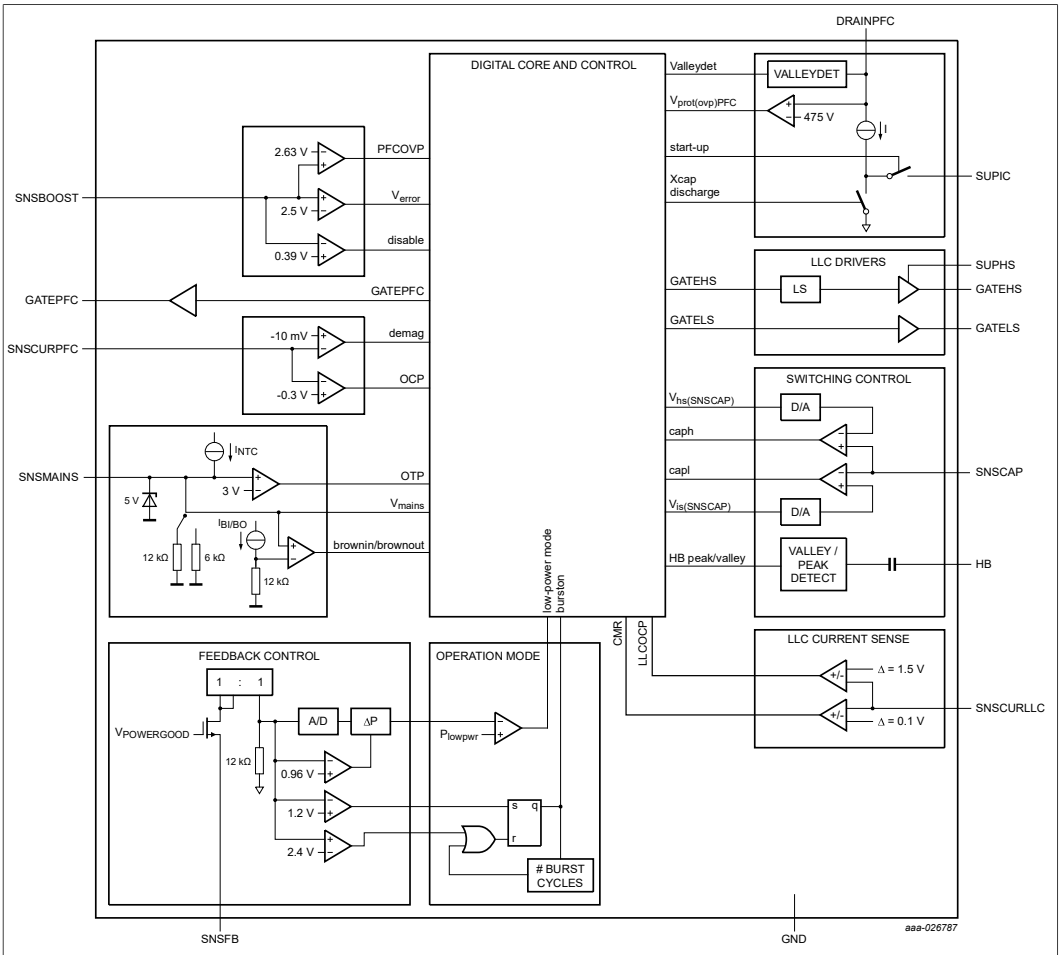



**Figure 1. Block diagram**

# 7 Pinning information

## 7.1 Pinning

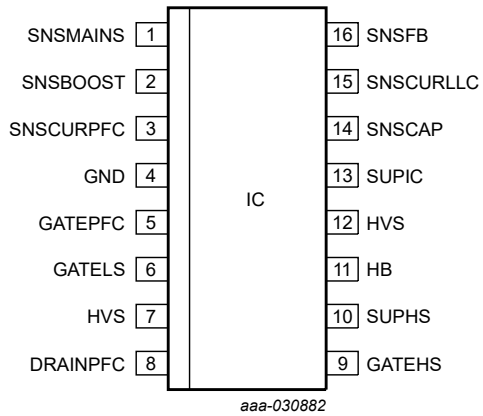



**Figure 2. TEA2016AAT pin configuration (SOT109-1)**

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| SNSMAINS | 1 | sense input for mains voltage and external temperature |
| SNSBOOST | 2 | sense input for boost voltage; externally connected to resistive divided boost voltage |
| SNSCURPFC | 3 | PFC current sense input |
| GND | 4 | ground |
| GATEPFC | 5 | PFC MOSFET gate driver output |
| GATELS | 6 | LLC low-side MOSFET gate driver output and supply for bootstrap capacitor |
| HVS | 7 | high-voltage spacer. Not to be connected. |
| DRAINPFC | 8 | internal HV start-up source also used for X- capacitor discharge, valley detection, and PFC OVP detection; connected to (PFC) drain voltage |
| GATEHS | 9 | LLC high-side MOSFET gate driver output |
| SUPHS | 10 | high-side driver supply input; externally connected to bootstrap capacitor ($C_{SUPHS}$) |
| HB | 11 | low-level reference for high-side driver and input for half-bridge slope detection; externally connected to half-bridge node HB between the LLC MOSFETs |
| HVS | 12 | high-voltage spacer. Not to be connected. |
| SUPIC | 13 | input supply voltage and output of internal HV start-up source; externally connected to an auxiliary winding of the LLC via a diode or to an external DC supply |
| SNSCAP | 14 | LLC capacitor voltage sense input; externally connected to divider across LLC capacitor |

**Table 3. Pin description***...continued*

| Symbol | Pin | Description |
|---|---|---|
| SNSCURLLC | 15 | LLC current sense input; externally connected to the resonant current sense resistor |
| SNSFB | 16 | output voltage regulation feedback sense input; externally connected to an optocoupler. Output for power good function. |

# 8 Functional description

## 8.1 Supply voltages

The TEA2016AAT includes:

- A high-voltage supply pin for start-up (DRAINPFC)
- A general supply to be connected to an external auxiliary winding (SUPIC pin)
- A floating supply for the high-side driver (SUPHS pin)

### 8.1.1 Start-up and supply voltage

Initially, the capacitor on the SUPIC pin is charged via the DRAINPFC pin. The DRAINPFC pin is connected to the drain voltage of the PFC MOSFET. Internally, a high-voltage current source is located between the DRAINPFC and SUPIC pins (see Figure 3).

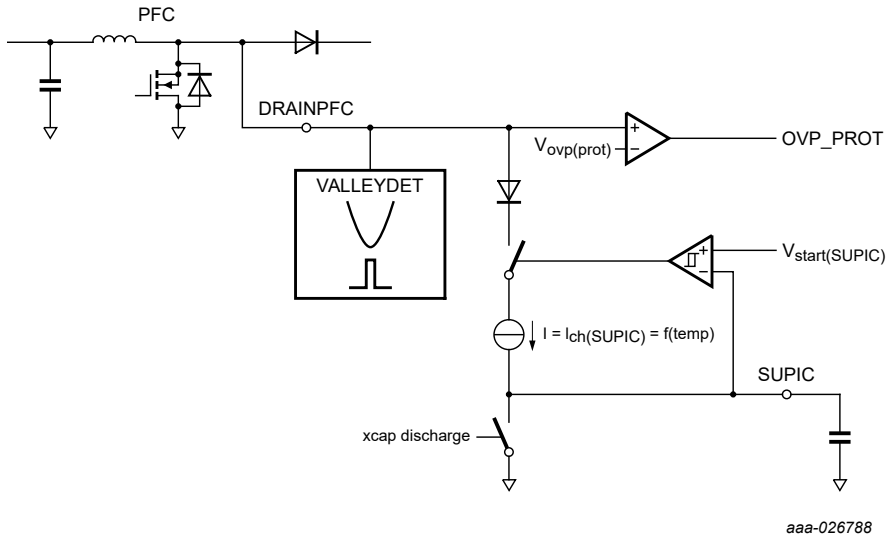



**Figure 3. HV start-up**

The maximum current of the internal current source is limited to $I_{ch(SUPIC)}$. To limit the IC dissipation, the charge current is reduced when the current source exceeds its maximum temperature ($T_{SUPICcharger}$).

When the SUPIC reaches the $V_{start(SUPIC)}$ level, it is continuously regulated to this start level with a hysteresis ($V_{start(hys)SUPIC}$). It activates the current source between the DRAINPFC and SUPIC pins when the SUPIC voltage drops to below $V_{start(SUPIC)} - V_{start(hys)SUPIC}$. When it exceeds $V_{start(SUPIC)}$, it deactivates the switch.

When the start level is reached, it reads the internal MTP (multi-time programmable memory) and defines the settings.

When the SUPIC voltage drops to below its stop levels, the TEA2016AAT enters the no-supply state. It recharges the SUPIC pin to its start level via the DRAINPFC pin. During the no-supply state and the reading of the MTP, the LLC and PFC are disabled. When the settings have been defined, the PFC starts up. When the SNSBOOST reaches the minimum level $V_{start(SNSBOOST)}$, the LLC also starts switching (see Figure 4 and Figure 5).

When start-up is complete and the LLC controller is operating, the LLC transformer auxiliary winding supplies the SUPIC pin. In this operational state, the HV start-up source is disabled.

When the system enters the protection mode, it cannot be supplied via the auxiliary winding. So, the SUPIC pin is regulated to $V_{start(SUPIC)}$ via the DRAINPFC pin.

During the non-switching period of the burst mode, the SUPIC is regulated to the $V_{low(SUPIC)}$ when SUPIC drops to below this level. It regulates the voltage with a hysteresis of $V_{low(hys)SUPIC}$. In this way, the system avoids that the SUPIC undervoltage protection ($V_{uvp(SUPIC)}$) is triggered because of a long non-switching period in burst mode.

The DRAINPFC pin is also used for valley detection, for X-capacitor discharge, and for providing a second PFC OVP protection.

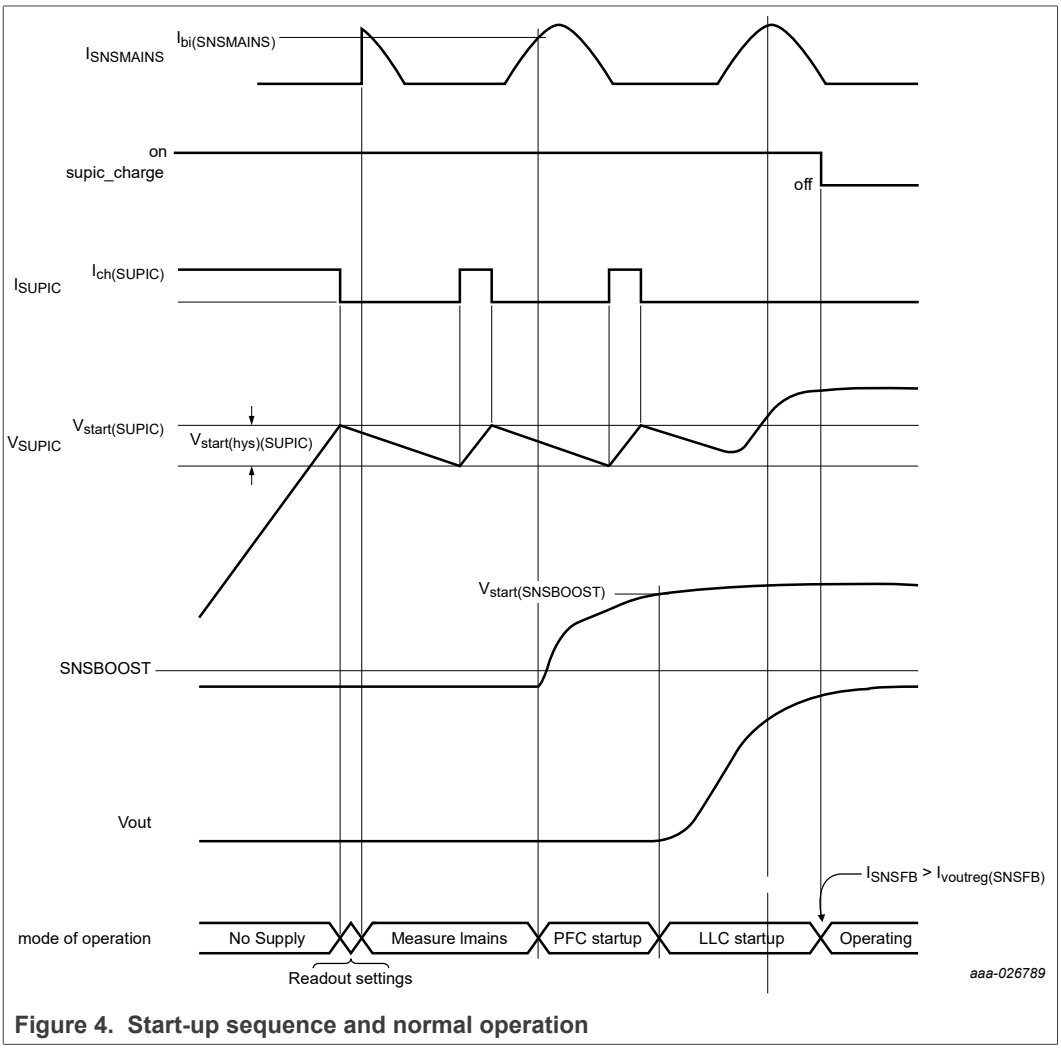



**Figure 4. Start-up sequence and normal operation**

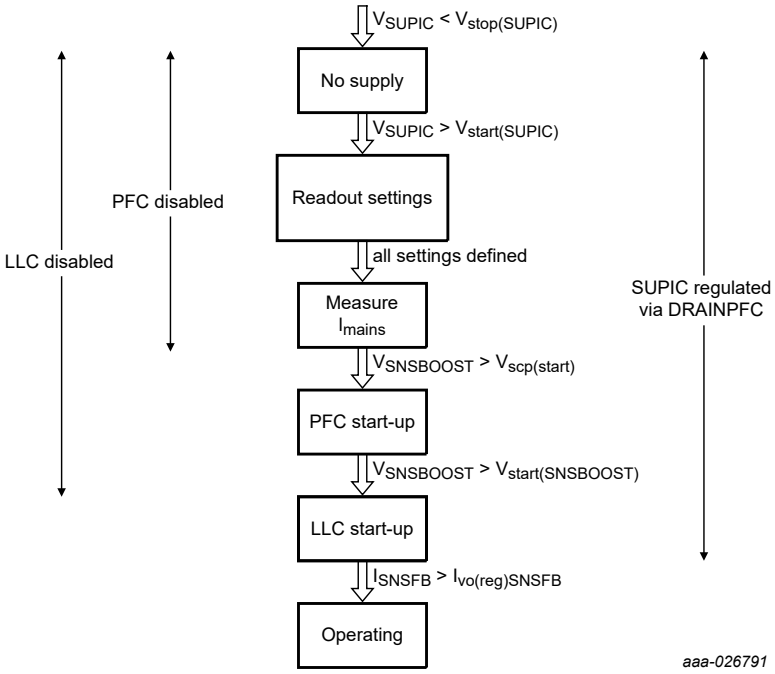



**Figure 5. LLC controller flow diagram**

### 8.1.2 High-side driver floating supply (SUPHS pin)

As the voltage range on the SUPIC pin exceeds that of the maximum external MOSFETs gate-source voltage, the external bootstrap capacitor $C_{SUPHS}$ cannot directly be supplied from the SUPIC.

To provide an external supply for the high-side driver without the need of additional external components, the GateLS output is designed such that it can drive the low-side MOSFET and supply the high-side MOSFET (patent number 82059363US01; see Figure 6).

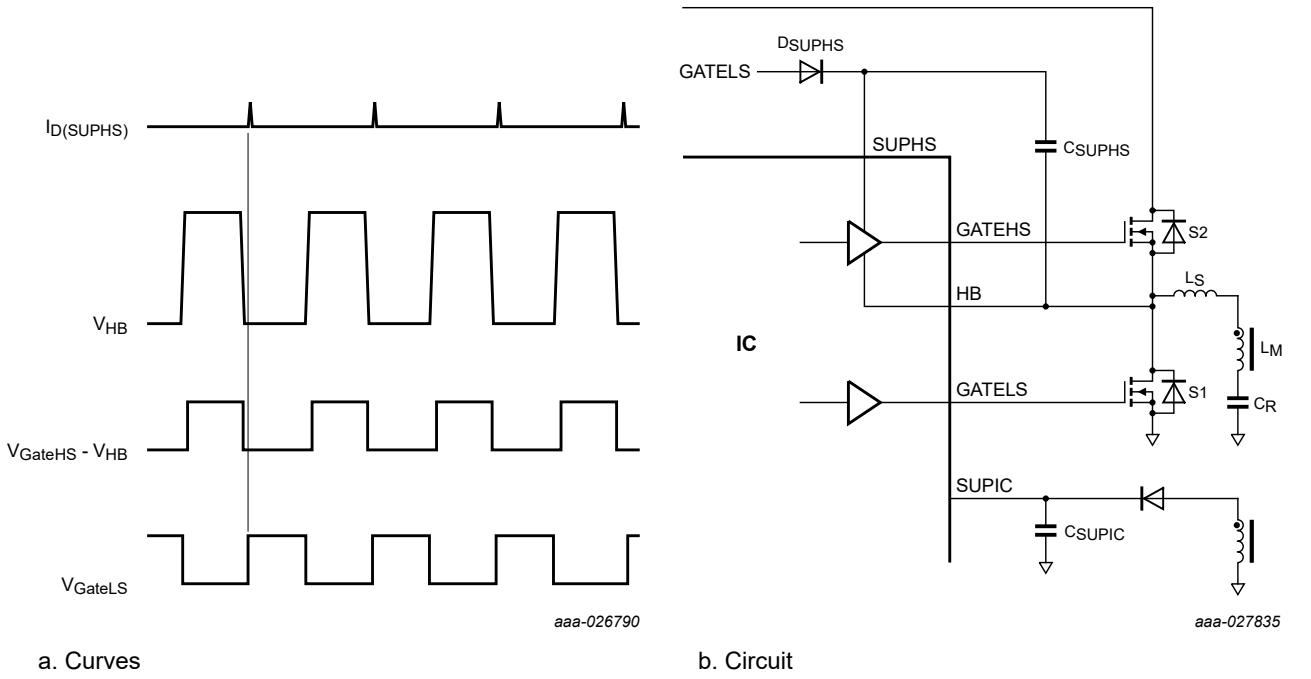



**Figure 6. High-side driver supply**

The external bootstrap buffer capacitor $C_{SUPHS}$ supplies the high-side driver. The bootstrap capacitor is connected to the low-side driver supply, the GATELS pin, and the half-bridge node (HB) via an external diode ($D_{SUPHS}$). When GATELS is active high and the HB node is pulled low, $C_{SUPHS}$ is charged.

Careful selection of the appropriate diode minimizes the voltage drop between the GATELS and SUPHS pins, especially when large MOSFETs and high switching frequencies are used. A great voltage drop across the diode reduces the gate drive of the high-side MOSFET.

## 8.2 LLC system regulation

A typical resonant controller regulates the output power by adapting the operating frequency.

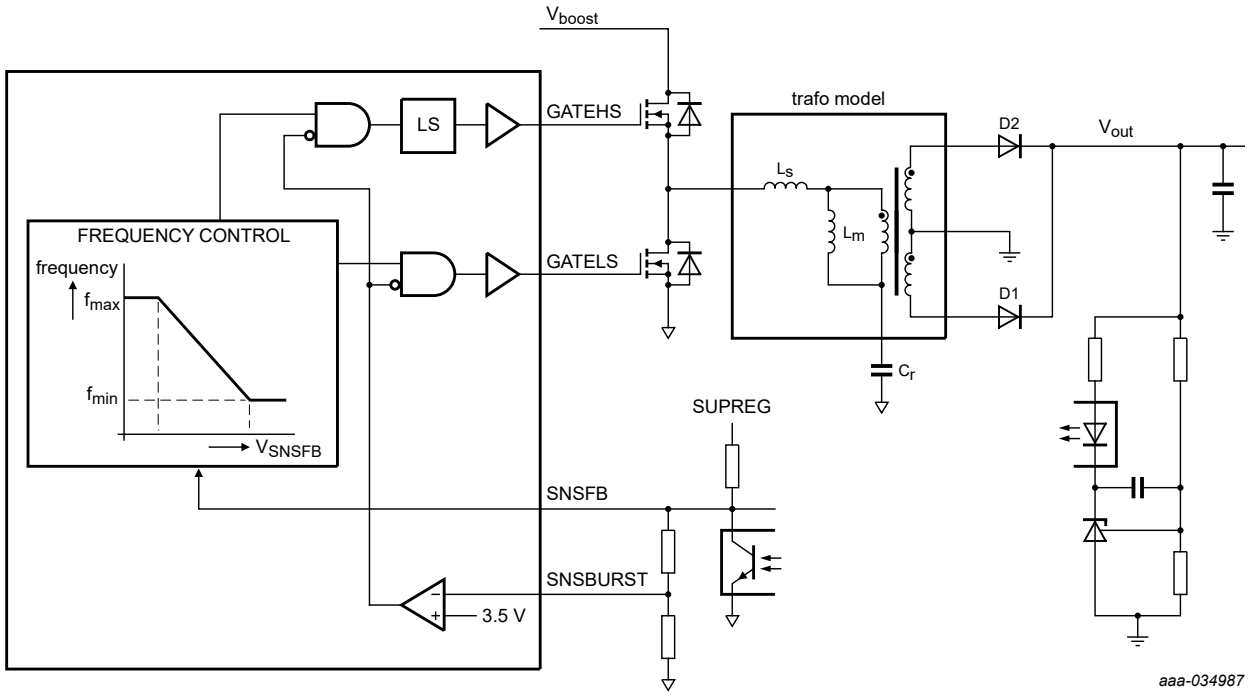



**Figure 7. Resonant frequency controller**

If the requested power at the outputs decreases, the output voltage of the LLC converter exceeds the targeted regulation level (12 V or 19.5 V typical), the optocurrent increases, and the voltage at the SNSFB decreases (see Figure 7). The resonant controller then increases the frequency according to its internal frequency control curve. Because of the higher frequency, the power to the output is reduced and the output voltage decreases. If the output voltage becomes too low, the controller lowers the system frequency, increasing the output power. In this way, the system regulates the output power to the required level.

As a small change in frequency gives a significant change in output power, frequency control has a high gain of the control loop. To increase the efficiency at low loads, most converters switch to burst mode as soon as the output power is below a minimum level. The burst mode level is mostly derived from the voltage on the SNSFB pin. For a frequency controlled resonant converter, it implies that the burst mode is entered at a certain frequency instead of at a certain load. A small variation of the resonant components results in a significant variation in power level at which the burst mode is activated.

In the TEA2016AAT, the control mechanism is different. The advantage is a constant gain of the control loop and a burst mode which is derived from the output power. The TEA2016AAT does not regulate the output power by adjusting the frequency but by the voltage across the primary capacitor.

The input power (related to the output power) of a resonant converter can be calculated with Equation 1:

$$P_{in} = V_{boost} \times I_{boost} = V_{boost} \times \Delta V_{Cr} \times C_r \times f_{sw} \quad (1)$$

Equation 1 shows that the input power has a linear relationship with the capacitor voltage difference $\Delta V_{Cr}$.

Figure 8 shows an alternative explanation of the linear relationship between the input power and the energy stored in the resonant capacitor.

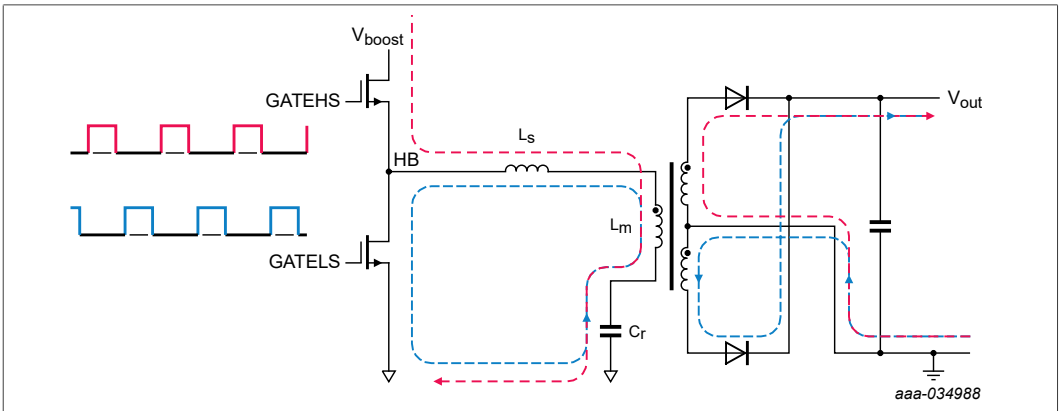



**Figure 8. Linear relationship between input power and energy stored in $C_r$**

When the high-side switch is on, a primary current is flowing through the transformer and resonant capacitor $C_r$ as indicated by the red line. Half the energy the input delivers is transferred to the output. The other half charges resonant capacitor $C_r$. The voltage across the resonant capacitor increases.

When the high-side switch is off and the low-side switch is on, the energy which is stored in resonant capacitor $C_r$ is transferred to the output and its voltage decreases. In this way, the linear relationship between the increase of the resonant capacitor voltage and the output power can be seen.

Although the TEA2016AAT uses the primary capacitor voltage as a regulation parameter, all application values, like the resonant inductances, resonant capacitor, and primary MOSFETs remain unchanged compared to a frequency controlled LLC converter. A secondary TL431 circuitry in combination with an optocoupler connected to the primary SNSFB pin continuously regulates the output voltage.

### 8.2.1 Output power regulation loop

Figure 9 shows the output power regulation loop of $V_{cap}$ control as used by the TEA2016AAT. Figure 10 shows a corresponding timing diagram.

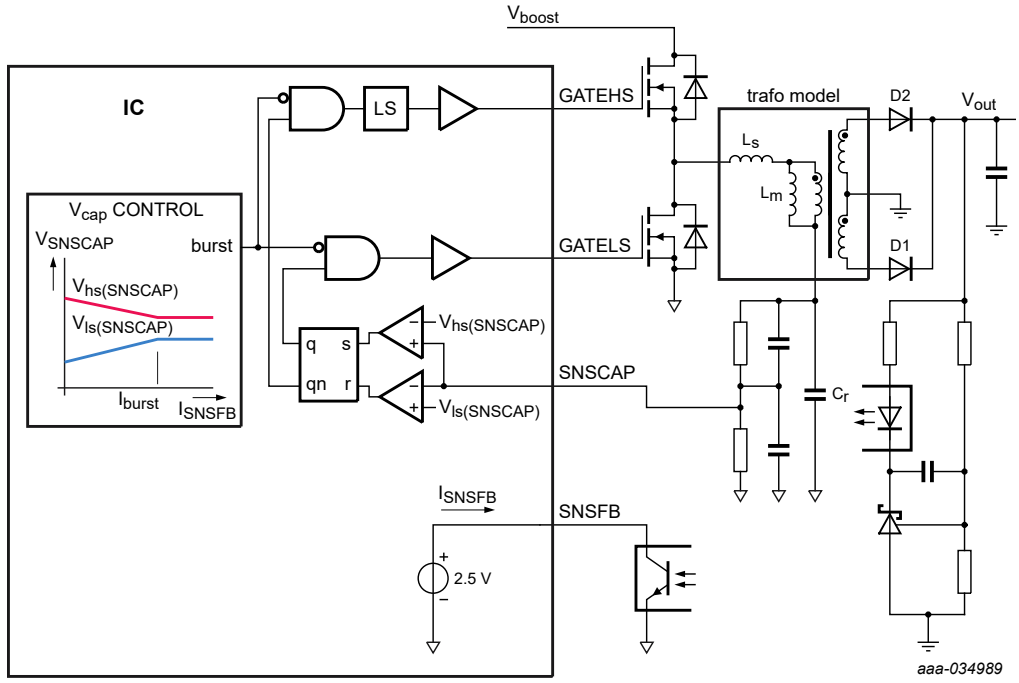



**Figure 9. Regulation loop $V_{cap}$ control**

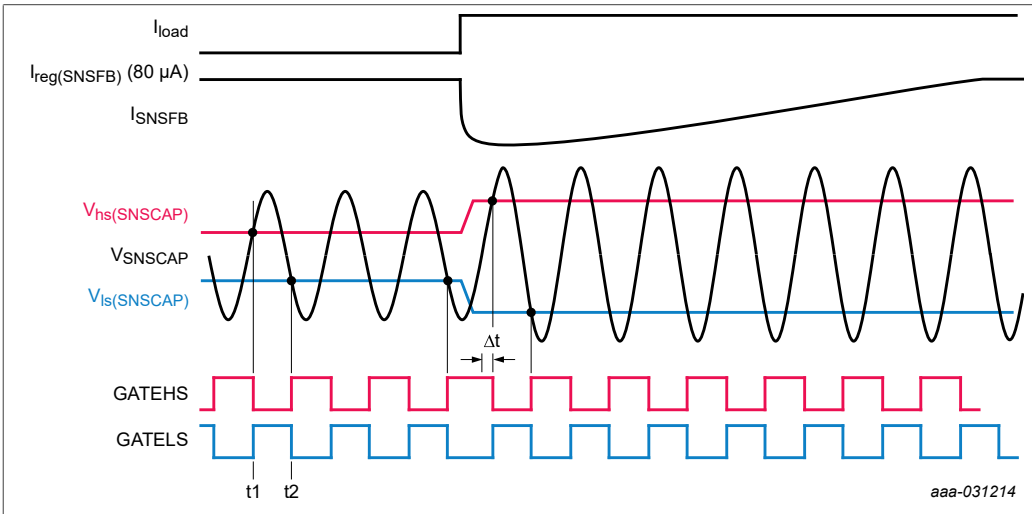



**Figure 10. Timing diagram of the regulation loop**

When the divided resonant capacitor voltage ($V_{SNSCAP}$) exceeds the capacitor voltage high level ($V_{hs(SNSCAP)}$), the high-side MOSFET is switched off (see Figure 10 (t1)). After a short delay, the low-side MOSFET is switched on. Because of the resonant current, the resonant capacitor voltage initially increases further but eventually drops.

When the divided capacitor voltage ($V_{SNSCAP}$) drops to below the capacitor voltage low level ($V_{ls(SNSCAP)}$), the low-side MOSFET is switched off (see Figure 10 (t2)). After a short delay, the high-side MOSFET is switched on. Figure 10 shows that the switching frequency is a result of this switching behavior. In a frequency controlled system, the frequency is a control parameter and the output power is a result. The TEA2016AAT regulates the power and the frequency is a result.

The difference between the high and low capacitor voltage level is a measure of the delivered output power. The value of the primary optocurrent, defined by the secondary TL431 circuitry, determines the difference between the high and low capacitor voltages.

Figure 10 also shows the behavior at a transient. If the output load increases, the current pulled out of the SNSFB pin decreases. The result is that the TEA2016AAT increases the high-level capacitor voltage and lowers the low-level capacitor voltage. According to Equation 1 in Section 8.2, the output power increases and eventually the output voltage increases to its regulation level.

To minimize no-load input power of the system, the primary current into the optocoupler is continuously regulated to 85 µA (see Section 8.4).

### 8.2.2 Output voltage start-up

The system controls the output power by regulating the primary $V_{Cr}$ (see Section 8.2). When the system is in regulation and the output voltage is stabilized, a small change in $\Delta V_{Cr}$ corresponds to a small change in the output current (see Equation 2).

$$P_{out} = V_{out} \times I_{out} \sim V_{boost} \times I_{boost} = \Delta V_{Cr} \times C_r \times f_{sw} \times V_{boost} \quad (2)$$

$$I_{out} \approx C_r \times f_{sw} \times V_{boost} \times \frac{\Delta V_{Cr}}{V_{out}}$$

However, before start-up, when the output voltage is around zero, a small capacitor voltage increase ($\Delta V_{Cr}$) corresponds to a substantial output current increase. So, at start-up, the divided $\Delta V_{Cr}$ voltage ($\Delta V_{SNSCAP}$) is slowly increased from a minimum value to the regulation level. As a result, the system starts up at a higher frequency.

While the system increases the $\Delta V_{SNSCAP}$, it continuously monitors the primary current via the SNSCURLLC pin. When the voltage at this pin exceeds the $V_{lmtr(ocp)}$ level, increasing the $\Delta V_{SNSCAP}$ is on hold until the voltage at the SNSCURLLC pin drops below the $V_{lmtr(ocp)}$ level again (see Figure 11). The output current is regulated and its voltage shows a nice ramp during start-up. It also avoids that during start-up the overcurrent protection (OCP) is triggered. In this way, the LLC converter behaves like a limited current source during start-up.

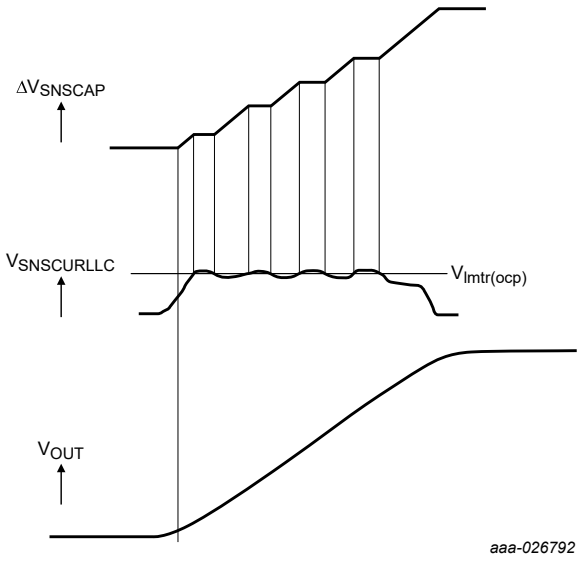



**Figure 11. LLC start-up behavior**

## 8.3 Modes of operation

Figure 12 shows the control curve between the output power and the voltage difference between the high and low capacitor voltage levels.

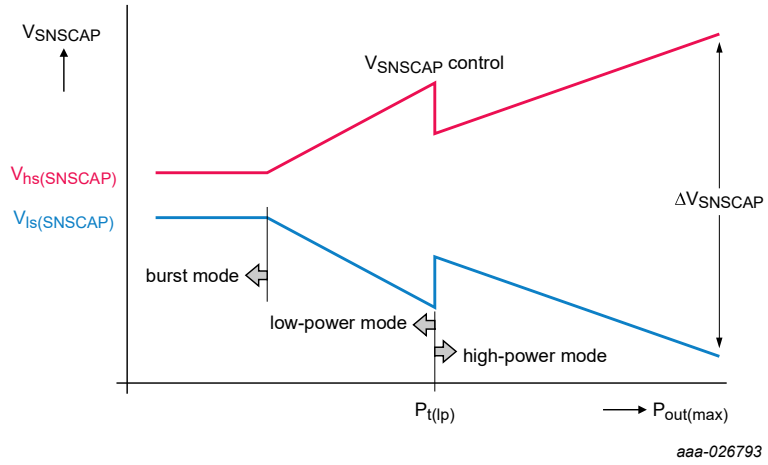



**Figure 12. TEA2016AAT control curve**

When the output power ($P_{out}$) is at its maximum, the low capacitor voltage level ($V_{ls(SNSCAP)}$) is at its minimum, and the high capacitor voltage ($V_{hs(SNSCAP)}$) is at its maximum level. According to Equation 1 in Section 8.2, the maximum $\Delta V_{SNSCAP}$ ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$), which is the divided $\Delta V_{Cr}$ voltage, corresponds to the maximum output power.

When the output load decreases, the $\Delta V_{SNSCAP}$ voltage decreases. As a result, the output power decreases and the output voltage is regulated. This mode is called high-power mode. Figure 10 shows a timing diagram of the system operating in high-power mode.

When the output power drops to below the transition level ($P_{t(lp)}$), the system enters the low-power mode. The $P_{t(lp)}$ level can be initialized via the MTP.

To compensate for the non-switching period in low-power mode, also called hold period, $\Delta V_{SNSCAP}$ is initially increased at entering the low-power mode (see Section 8.3.2). In low-power mode, the output power is regulated by adapting $\Delta V_{SNSCAP}$, until it reaches a minimum. The system then enters the burst mode (see Section 8.3.3).

### 8.3.1 High-power mode

In high-power mode, the system operates as described in Section 8.2.1. Figure 13 shows a flow diagram of the high-power mode.

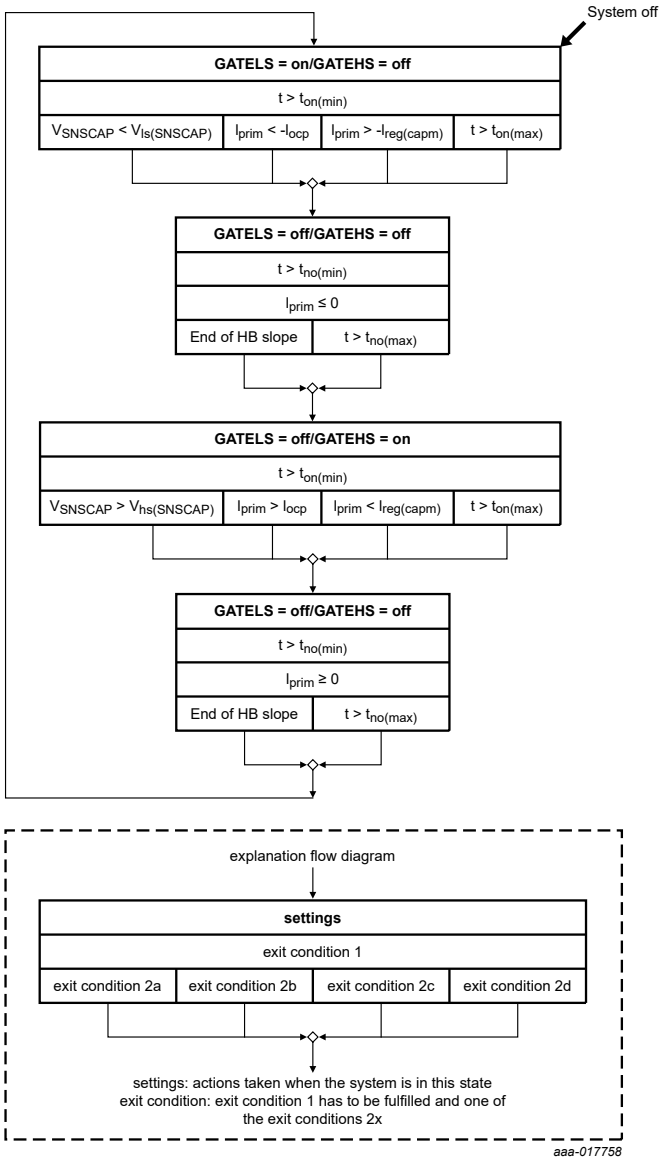



**Figure 13. High-power mode flow diagram**

Initially, GATELS is on and GATEHS is off. The external bootstrap buffer capacitor ($C_{SUPHS}$) is charged via the GATELS pin and an external diode. The system remains in this state for at least the minimum on-time ($t_{on(min)}$) of GATELS. Before entering the next state, one of the following conditions must be fulfilled:

- The $V_{SNSCAP}$ voltage drops to below the minimum $V_{SNSCAP}$ voltage ($V_{ls(SNSCAP)}$)
- The measured current exceeds the OCP level (see Section 8.6.15)
- The system is close to capacitive mode (see Section 8.6.14)
- The maximum on-time ($t_{on(max)}$), a protection that maximizes the time the high-side or low-side MOSFET is kept on, is exceeded.

In the next state, to avoid false detection of the HB peak voltage, the system waits until the minimum non-overlap time ($t_{no(min)}$) is exceeded. When it is exceeded, the system starts to detect the end (= peak voltage) of the HB node. When it detects the peak of the HB node and the measured resonant current is negative (or zero), it enters the next state.

If the system does not detect a peak at the HB node, it also enters the next state when the maximum non-overlap time ($t_{no(max)}$) is exceeded under the condition of a negative (or zero) resonant current.

Finally, the third and fourth states (see Figure 13) describe the GATEHS and GATEHS to GATELS transition criteria which are the inverse of the first two states.

### 8.3.2 Low-power mode

At low loads, the operating frequency of a resonant converter increases. As a result, the magnetization and switching losses increase. For this reason, the efficiency of a resonant converter drops at low loads. A newly introduced low-power mode ensures high efficiency at lower loads as well.

When the output power drops to below the $P_{t(lp)}$ level, the system enters the low-power mode (see Figure 12 and Figure 14). It continues switching for 3 half-cycles (low-side, high-side, low-side) with an MTP selectable duty cycle. To ensure a constant output power level, it increases the energy per cycle ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) at the same time.

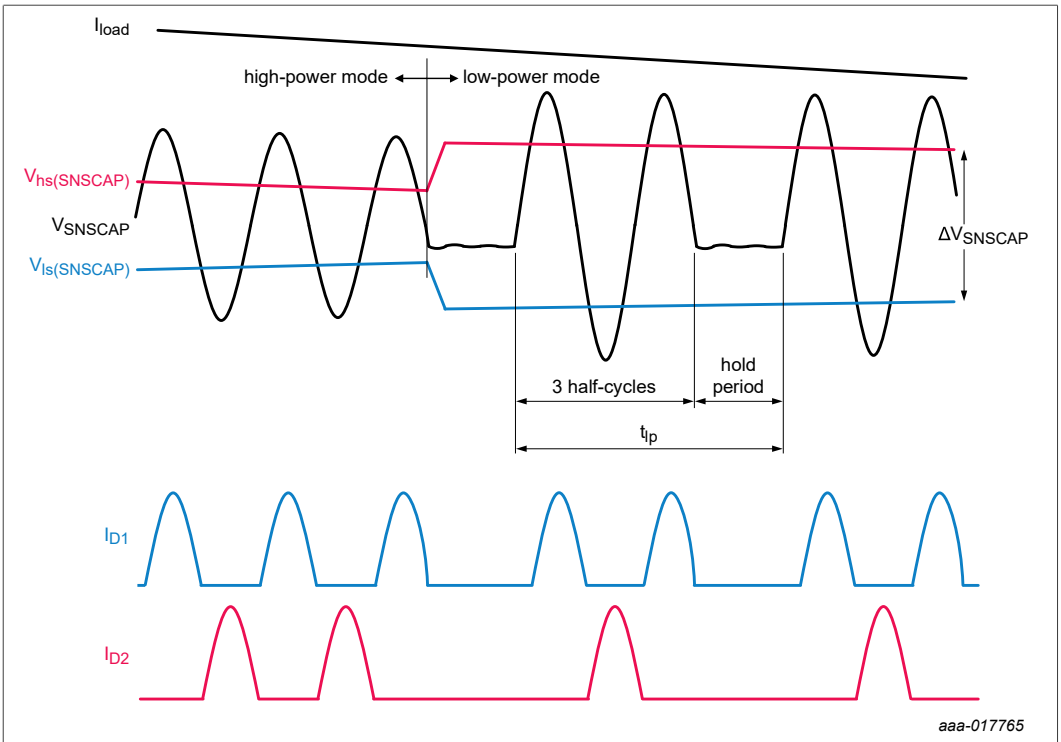



**Figure 14. Timing diagram transition high-power mode to low-power mode**

As the system continuously tracks the primary capacitor voltage, it knows exactly when to enter the "hold" period. It can also continue again at exactly the correct voltage and current levels of the resonant converter. In this way, a "hold" period can be introduced which reduces the magnetization and switching losses without any additional losses. The currents $I_{D1}$ and $I_{D2}$ (see Figure 14) are the secondary currents through diodes D1 and D2 (see Figure 25).

When in low-power mode the output power is further reduced, the amount of energy per cycle (= $\Delta V_{SNSCAP}$) is reduced and the duty cycle remains the same (see Figure 15).

When in low-power mode the system reaches the programmable minimum energy per cycle (= $\Delta V_{SNSCAP}$), it enters burst mode.

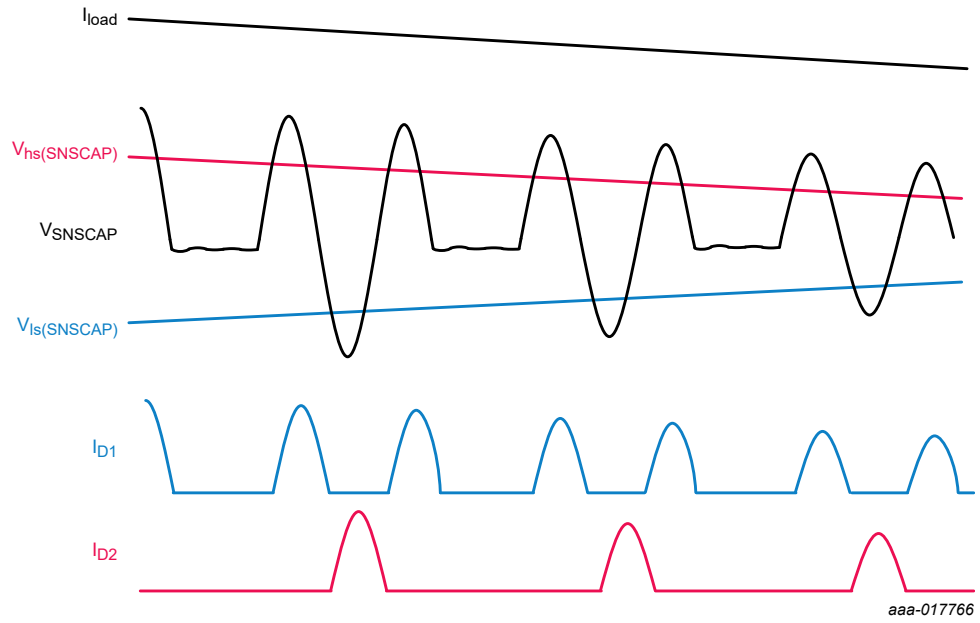



**Figure 15. Low-power mode: Lowering the energy-per-cycle ($\Delta V_{SNCAP}$)**

### 8.3.3 Burst mode

In burst mode, the system alternates between operating in low-power mode and an extended hold state (see Figure 16). Because of this additional extended hold period, the magnetization and switching losses are further reduced. So, the efficiency of the system is increased.

Figure 16 shows all operating frequencies outside the audible area. The minimum low-power frequency can be set with a parameter. Within a low-power period, the system is switching at the resonant frequency of the converter, which is typically between 50 kHz and 200 kHz.

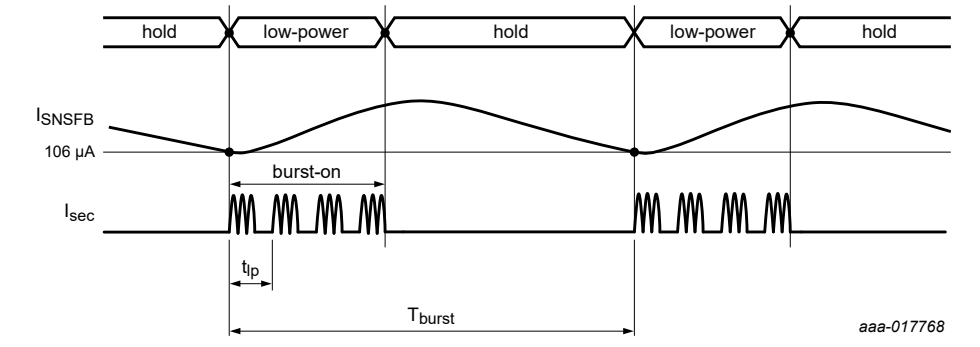



**Figure 16. Burst mode**

#### 8.3.3.1 Frequency regulation

The burst frequency (1 / $t_{burst}$) is continuously regulated to a predefined value, which can be set with a parameter. As both the low power and burst frequency can be accurately set with parameters, they can be chosen such that they are outside the audible area. $I_{sec}$ is the secondary current flowing through either diode D1 or D2 (see Figure 25).

When the primary optocurrent ($I_{SNSFB}$) drops to below $I_{start(burst)}$ (100 µA), a new burst-on period is started. The end of the burst-on period depends on the calculated number of low-power cycles. The number of low-power cycles within a burst-on is continuously adjusted so that the burst period is at least the period defined by the setting (see Figure 17).

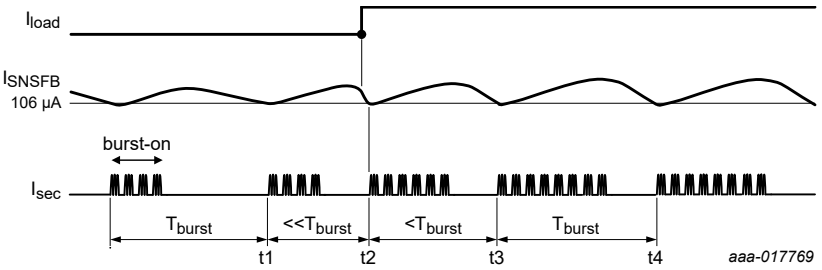



**Figure 17. Burst mode: Regulating the number of low-power cycles**

The system continuously measures the burst period from the start of the previous burst-on period to a new burst-on period. At t1, the measured burst period ($t_{burst}$) equals the required $T_{burst}$. So, the next number of low-power cycles equals the number of previous low-power cycles. At a constant output power, the system expects that when the next burst-on period has the same number of low-power cycles as the previous burst-on period, the burst period ($T_{burst}$) remains constant.

At a positive transient (t2), a new low-power cycle is started immediately to minimize the drop in output voltage. The measured time period, at time t2, is below the targeted burst period. The system increases the number of burst cycles. At t3, it measures the burst period again. In this example, the burst period is still below the targeted burst period. So, the system increases the number of low-power cycles again and again until the measured burst period equals the target burst period, which occurs at t4.

#### 8.3.3.2 Transient

When the system operates in burst mode, it defines the new number of cycles at the start of a new burst cycle. If the output load is reduced just after the start of a new burst cycle, the output voltage shows an overshoot (see Figure 18).

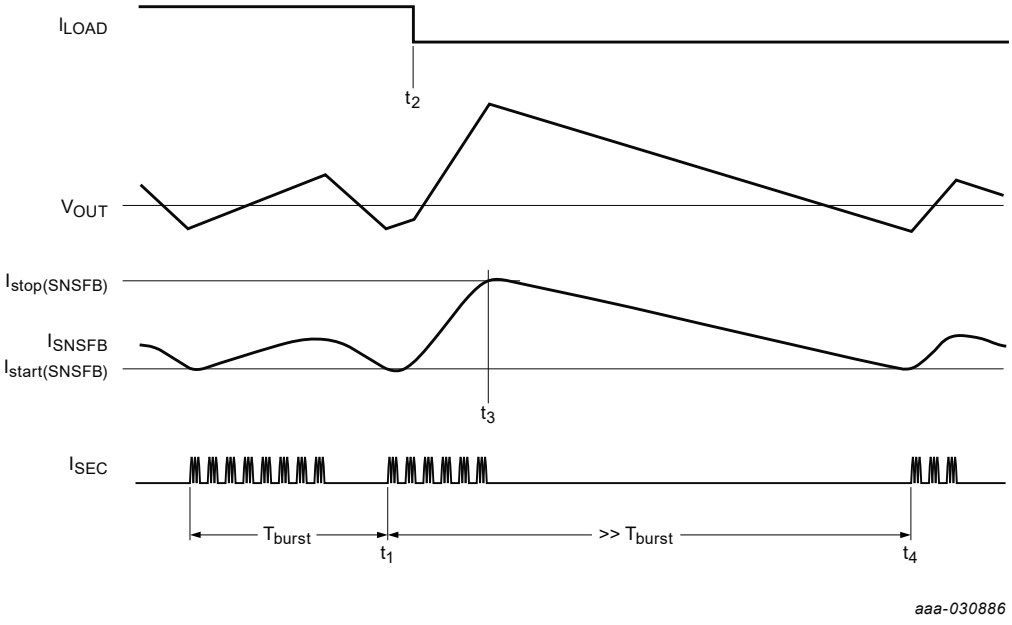



**Figure 18. Burst mode - transient**

At t1, the system starts with a new burst cycle period. Shortly later at t2, the output load is reduced. As a result the output voltage shows an overshoot and the optocoupler current increases. To limit the overshoot, the system also ends the burst cycle when the optocoupler current exceeds the $I_{stop(burst)}$ level.

## 8.4 Optobias regulation

In a typical application, the output voltage is sensed using a TL431 and connected to the SNSFB pin of the TEA2016AAT via an optocoupler (see Figure 25). Because of the behavior of the TL431, the current through the optocoupler is at the maximum level when the output power is at the minimum level. It is therefore one of the most critical parameters to achieve the required no-load input power. To achieve maximum efficiency at low load/no load, the TEA2016AAT continuously regulates the optocurrent to a low level that is independent of the output load.

Because of the parasitic capacitance at the optocoupler collector, a very low optocurrent reduces the transient response of the system. So, the TEA2016AAT applies a fixed voltage at the SNSFB pin. It measures the current through the optocoupler which defines the required output power. The optocurrent is continuously (slowly) regulated to the $I_{reg(SNSFB)}$ level (= 80 µA) via an additional internal circuitry, which adds an offset to the required output power. This level is independent of the output power.

At a positive load transient, the optocurrent initially decreases (see Figure 10; $I_{SNSFB}$). The TEA2016AAT immediately increases the $\Delta V_{SNSCAP}$ which again increases the output power.

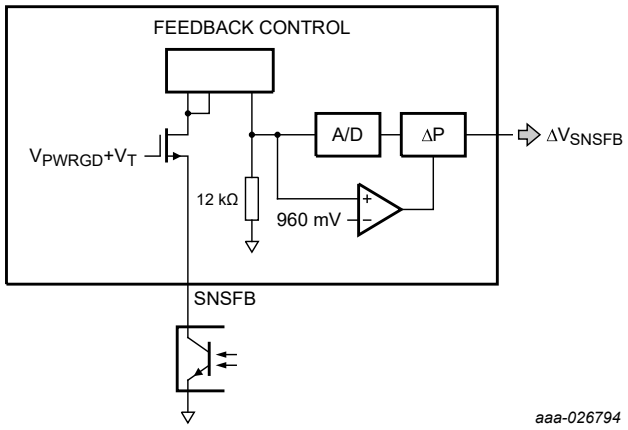



**Figure 19. Optobias regulation**

Figure 19 shows that when the optocurrent decreases, the internal voltage across the 12 kΩ resistor drops to below the targeted level of 960 mV (= 80 µA × 12 kΩ). The TEA2016AAT then slowly increases an additional offset at the power level (ΔP). It continues to increase the additional offset until the optocurrent reaches the target of 80 µA. When the optocurrent increases due to a transient, the additional offset to the power level is decreased. As a result, the output voltage decreases which again decreases the optocurrent. In this way, the optocurrent is continuously regulated to the $I_{reg(SNSFB)}$ level (see Figure 10).

The behavior of the internal circuitry connected to the SNSFB pin is the same as the behavior of the traditional circuitry. The fixed voltage at the SNSFB pin and the continuous regulation of the optocurrent level does not influence the regulation level. The advantage, however, is a reduction in no-load input power and an optimization of the transient response.

When the system operates in low-power mode at the minimum energy per cycle and at minimum duty cycle, it can no longer reduce the optocurrent level to the $I_{reg(SNSFB)}$ target (» 80 µA). If the output power decreases further and the optocurrent increases to above the level of Istart(burst) (» 100 µA), the burst mode is triggered. When the output power drops to below this level again, a new burst cycle is started (see Figure 16 and Figure 17).

## 8.5 Power factor correction (PFC) regulation

The power factor correction circuit operates in quasi-resonant or discontinuous conduction mode with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. To detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch, the control IC continuously monitors the voltage across the PFC MOSFET and the current through the PFC circuitry.

### 8.5.1 Soft start (SNSCUR pin)

To prevent audible transformer noise at start-up, the soft start function slowly increases the on-time (see Figure 20).

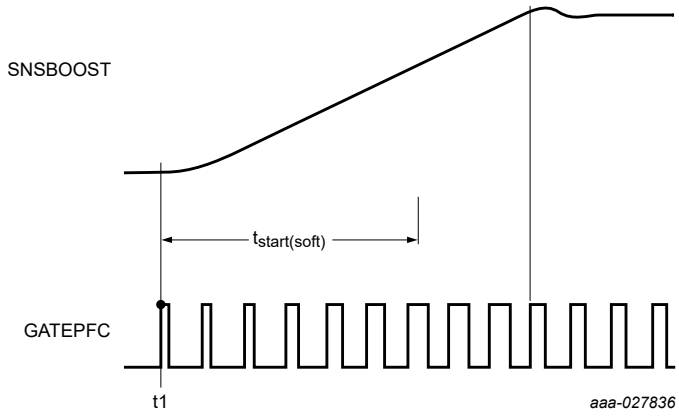



**Figure 20. PFC start-up**

At t1, all conditions to start up the PFC are fulfilled. When the PFC starts switching, the maximum on-time is increased cycle-by-cycle from zero until the $t_{on}$ regulation limits the on-time of the PFC external MOSFET.

### 8.5.2 $t_{on}$ control

The power factor correction circuit is operated in $t_{on}$ control. The resulting mains harmonic reduction of a typical application is well within the class-D requirements.

The following circuits determine the on-time of the external PFC MOSFET:

- The internal digital control loop, including the loop compensation.
- Mains compensation which uses the current through the SNSMAINS pin to represent the mains input voltage level.

### 8.5.3 PFC error amplifier (SNSBOOST pin)

The boost voltage is divided using a high-ohmic resistive divider and is supplied to the SNSBOOST pin. The internal digital control loop, which compares the SNSBOOST voltage with an accurate trimmed reference voltage ($V_{reg(SNSBOOST)}$) regulates the output voltage by adjusting the on-time.

### 8.5.4 Valley switching and demagnetization

To ensure that the TEA2016AAT operates in discontinuous or quasi-resonant mode, the PFC MOSFET is switched on after the transformer is demagnetized. To reduce switching losses and electromagnetic interference (EMI), the next stroke is started when the PFC MOSFET drain-source voltage is at its minimum (valley switching). The demagnetization and valley detection are measured via the SNSCURPFC and the DRAINPFC pin.

If no valley signal is detected on the DRAINPFC pin, the controller generates a valley signal ($t_{to(vrec)}$; 10 µs typical) after demagnetization is detected.

### 8.5.5 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation exceeds the $f_{sw(PFC)max}$ limit, the system enters discontinuous conduction mode (DCM). When the system is in DCM, the PFC MOSFET switches on at a minimum voltage across the switch (valley switching).

To ensure correct control of the PFC MOSFET under all circumstances, the minimum off-time is limited at $t_{off(PFC)min}$.

### 8.5.6 Mains voltage compensation (SNSMAINS pin)

The equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, the result is a low bandwidth for low mains input voltages. At high mains input voltages, the Mains Harmonic Reduction (MHR) requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA2016AAT contains a correction circuit. The input voltage is measured via the SNSMAINS pin (see Section 8.6.4) and the information is fed to an internal mains compensation circuit (see Figure 1). With this compensation, it is possible to keep the regulation loop bandwidth constant over the full mains input range. The result is that a mains voltage independent transient response on load steps is yielded, while still complying with class-D MHR requirements.

### 8.5.7 Active X-capacitor discharge

The TEA2016AAT provides an active X-capacitor discharge after the mains voltage is disconnected. When the mains input voltage (and so also the measured current into the SNSMAINS pin) increases, the system assumes the presence of a mains voltage. When the mains voltage does not increase for a minimum period of $t_{d(xcap-dch)}$, the active X-capacitor discharge is activated.

When the active X-capacitor discharge function is activated, the X-capacitor is discharged via the DRAINPFC pin.

While the DRAINPFC pin discharges the X-capacitor, the mains can be reconnected. In that case, the discharge current is disabled again.

## 8.6 Protections

Table 4 gives an overview of the available protections.

**Table 4. Protections overview**

| Protection | Description | Action | PFC | LLC | Protection register |
|---|---|---|---|---|---|
| **General protections** | | | | | |
| UVP SUPIC | undervoltage protection SUPIC pins | recharge via DRAINPFC; restart when $V_{SUPIC} > V_{start(SUPIC)}$ | off | off | - |
| MTPfail | reading of the internal MTP failed | continue reading until the data is valid; only checked once at start-up | off | off | Y |
| OTPint | internal overtemperature protection | LLC and PFC are either latched or safe restart | off | off | - |
| OTPext | external overtemperature protection | Both LLC and PFC are either latched or safe restart | off | off | - |
| SCP SNSBOOST/ fast disable | short-circuit protection/ disable PFC and LLC | restart when $V_{SNSBOOST} > V_{scp(start)}$ | off | off | Y |
| **PFC protections** | | | | | |
| brownout-mains | undervoltage protection mains | restart when the mains voltage exceeds the brownin level | off | on/ off [1] | - |
| OVP SNSBOOST | overvoltage protection boost voltage | restart when $V_{SNSBOOST} < V_{ovp(SNSBOOST)}$ | off | on/ off [1] | - |
| OVP DRAINPFC | overvoltage protection DRAINPFC voltage | LLC and PFC are either latched or safe restart protections | off | off | Y |
| OCP | overcurrent protection | PFC MOSFET switched off; continue operation | - | - | Y |
| PFCcoil short | - | LLC and PFC are off, followed by a safe restart | off | off | - |
| Iinrush | inrush current protection | PFC MOSFET switched off; PFC switching extended | off | - | - |

**Table 4. Protections overview***...continued*

| Protection | Description | Action | PFC | LLC | Protection register |
|---|---|---|---|---|---|
| **LLC protections** | | | | | |
| UVP SUPHS | undervoltage protection SUPHS pin | GATEHS = off | - | off | - |
| UVP SNSBOOST | undervoltage protection boost | restart when $V_{SNSBOOST} > V_{start(SNSBOOST)}$ | - | off | - |
| OVP SUPIC | output overvoltage protection; measured via the SUPIC pin | LLC and PFC are either latched or safe restart | off | off | Y |
| CMR | capacitive mode regulation | system ensures that mode of operation is inductive | - | - | Y |
| OCP | overcurrent protection | switch off cycle-by-cycle; After several consecutive cycles, LLC and PFC are either latched or safe restart | off | off | Y |
| STARTUP MAX | maximum start-up time | LLC and PFC are either latched or safe restart | off | off | Y |
| OPP | overpower protection | LLC and PFC are either latched or safe restart | off | off | Y |

[1] Selectable via a parameter at the MTP.

When the system is in a latched or safe restart protection, the SUPIC voltage is regulated to its start level via the DRAINPFC pin.

### 8.6.1 Undervoltage protection SUPIC

When the voltage on the SUPIC pin is below its undervoltage level $V_{uvp(SUPIC)}$, both the PFC and LLC converter stop switching. The capacitors at the SUPIC pin are recharged via the DRAINPFC pin.

When the SUPIC supply voltage exceeds its start level, the system restarts.

### 8.6.2 MTP fail

When, at start-up, the SUPIC reaches the start level, the system reads the parameters from the internal MTP. If reading the MTP failed, the system retries reading the MTP until it succeeds. During this time, the PFC and LLC remain off. The SUPIC is regulated to the $V_{start(SUPIC)}$ level.

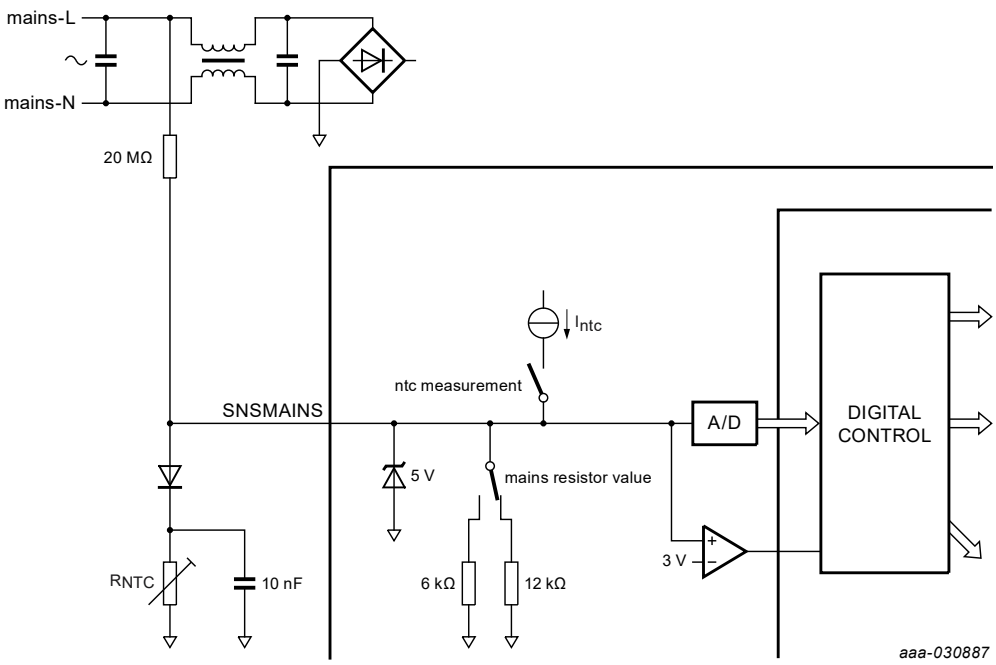
### 8.6.3 Internal overtemperature protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the PFC and the LLC stop switching.

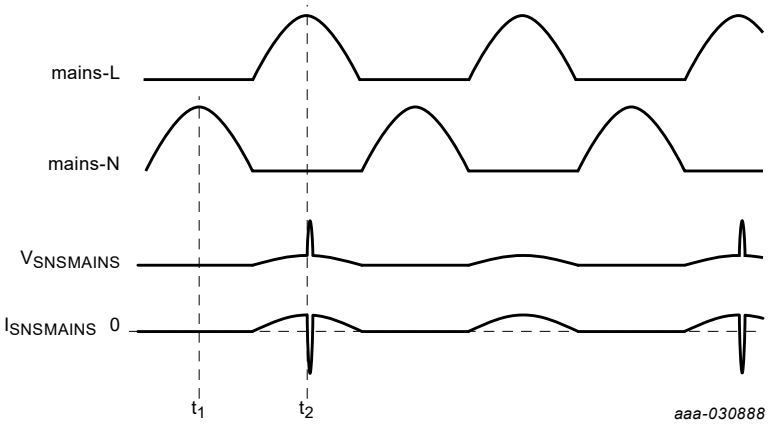
The response of the internal OTP follows the setting of the external OTP. It can be either latched or safe restart.

### 8.6.4 Brownin/brownout and external overtemperature protection

On the TEA2016AAT, the mains measurement and external temperature are combined at the SNSMAINS pin (see Figure 21).




a. Circuit




b. Timing diagram

**Figure 21. Mains and external OTP management**

The TEA2016AAT continuously measures the SNSMAINS voltage via an A/D converter and waits until it detects a peak (t1). This peak value is internally stored and used as an input for the brownout/brownin detection and the mains compensation.

The TEA2016AAT continuously measures the mains voltage. There is an internal counter that counts the number of peaks. During one out of 4 peaks, it measures the external temperature.

### 8.6.5 Short-circuit protection/fast disable

The PFC and LLC do not start switching until the voltage on the SNSBOOST pin exceeds $V_{scp(start)}$. This function acts as short circuit protection for the boost voltage.

When the SNSBOOST pin is shorted to ground or the SNSBOOST pull-up resistor is disconnected, this protection inhibits switching.

This function can also be used as a fast disable. If this pin is shorted to ground via an external MOSFET, the system either stops switching or enters the protection mode followed by safe restart or latched protection. In this way, an additional external protection can be added.

### 8.6.6 Brownout mains

On the TEA2016AAT, the mains measurement and external temperature are combined at the SNSMAINS pin.

To prevent the PFC from operating at very low mains input voltages, the PFC stops switching when the measured mains voltage drops to below the brownout level. When the mains voltage exceeds the brownin level, the PFC restarts with a soft start. To avoid that the system is interrupted during a short mains interruption, a delay can be set before the brownout function is active.

The external resistor, which is connected between the mains input voltage, can be either 20 MΩ or 10 MΩ. These values can be set with a parameter.

Typically, only the PFC stops switching and the LLC continues at a brownout. Due to the large PFC bulk capacitor, the LLC can continue for a long period while the mains is already disconnected. So the option to stop the LLC at a brownout after a given delay can be selected with a parameter.

### 8.6.7 Overvoltage protection (SNSBOOST pin)

To prevent output overvoltage during load steps and mains transients, a PFC output overvoltage protection circuit is built in. When the voltage on the SNSBOOST pin exceeds the $V_{ovp(stop)}$ level, switching of the power factor correction circuit is inhibited. When the SNSBOOST pin voltage drops to below the regulation level ($V_{reg(SNSBOOST)}$) again, the switching of the PFC recommences. The IC always restarts with a soft start.

When an OVP at the SNSBOOST is detected for a minimum period (can be set using a parameter), the LLC can also be disabled.

### 8.6.8 Overvoltage protection (DRAINPFC pin)

To prevent output overvoltage of the PFC due to a disturbed SNSBOOST pin, an additional PFC output overvoltage protection is available. This overvoltage protection is measured via the DRAINPFC pin.

The DRAINPFC overvoltage protection level and the delay before it enters the protection state can be set with parameters.

The DRAINPFC overvoltage protection can be a latched, a safe restart, or a latched after safe restart protection.

### 8.6.9 Overcurrent protection (SNSCURPFC pin)

The PFC current is measured via an external sense resistor ($R_{sense}$) connected to the SNSCURPFC pin. If the voltage drops to below $V_{ocp(PFC)}$, the PFC MOSFET is turned off. It resumes switching at the next cycle. To ensure that the OCP level is not exceeded due to disturbance caused by a turn on of the PFC MOSFET, the OCP level is blanked for 300 ns ($t_{leb}$).

### 8.6.10 PFC coil short protection (SNSCURPFC pin)

When the overcurrent protection is continuously triggered, the cause may be a shorted PFC coil. To avoid overheating, the system enters the protection state when the OCP is continuously triggered for 100 ms ($t_{ocp(PFC)}$). The PFC and LLC converters stop switching and a restart follows.

### 8.6.11 Undervoltage protection SUPHS

To ensure a minimum drive voltage at the high-side driver output (GATEHS), this driver is kept off when its voltage is below the minimum level ($V_{SUPHS} < V_{rst(SUPHS)}$).

### 8.6.12 Undervoltage protection boost

The PFC output voltage is measured via a resistive divider connected to the SNSBOOST pin. The voltage at the SNSBOOST pin must exceed the start level ($V_{SNSBOOST} > V_{start(SNSBOOST)}$) before the LLC converter is allowed to start switching.

When the system is operating and the voltage at the SNSBOOST pin drops to below the minimum level ($V_{SNSBOOST} < V_{uvp(SNSBOOST)}$), the LLC converter stops switching. When it exceeds the start level, it restarts.

### 8.6.13 Overvoltage protection

When the voltage at the SUPIC pin exceeds the $V_{ovp(SUPIC)}$ level for $t_{ovp(SUPIC)}$, the OVP protection is triggered. The voltage at the SUPIC pin is continuously monitored via an internal ADC converter.

The OVP protection level ($V_{OVP(SUPIC)}$) and the OVP delay time can be selected with a parameter.

The OVP function can also be disabled.

### 8.6.14 Capacitive mode regulation (CMR)

The TEA2016AAT has a capacitive mode regulation (CMR) which ensures that the system is always operating in inductive mode and avoids operation in capacitive mode.

At lower input voltage or higher output power and depending on the resonant design, the resonant current can already approach zero before the capacitor voltage reaches the regulation level.

When the resonant current has changed polarity before the switches are turned off and the other switch is turned on, hard switching occurs. This event is called capacitive mode. To avoid that it operates in capacitive mode, the system also switches off the high-side/ low-side switch when the resonant current approaches zero.

Figure 22 shows the signals that occur when a resonant converter is switching in CMR mode. At t1 (and also at t3), the low-side switch is on while the resonant current approaches zero before $V_{SNSCAP}$ reaches $V_{ls(SNSCAP)}$. At t2, the resonant current is also close to changing polarity while the divided capacitor voltage ($V_{SNSCAP}$) has not reached the $V_{hs(SNSCAP)}$ level yet. To avoid a turn-off of the high-side switch at a negative current or the low-side at a positive current, the system also turns off the high-side/low-side switch when the primary current approaches zero. So at t2, the high-side switch is turned off because the primary current is close to zero. At $t_3$ (and also at $t_1$), the low-side switch is turned off, although $V_{SNSCAP}$ did not reach the regulation level ($V_{ls(SNSCAP)}$) yet. The primary current is measured via an external sense resistor connected to the SNSCURLLC pin. The capacitive mode protection levels are $V_{reg(capm)}$ (−100 mV and +100 mV, respectively). These protection levels can be adjusted with a parameter.

In this mode, the amount of output power is reduced and the output voltage decreases.

The TEA2016AAT does not enter a so-called "capacitive mode protection", but avoids this mode of operation.

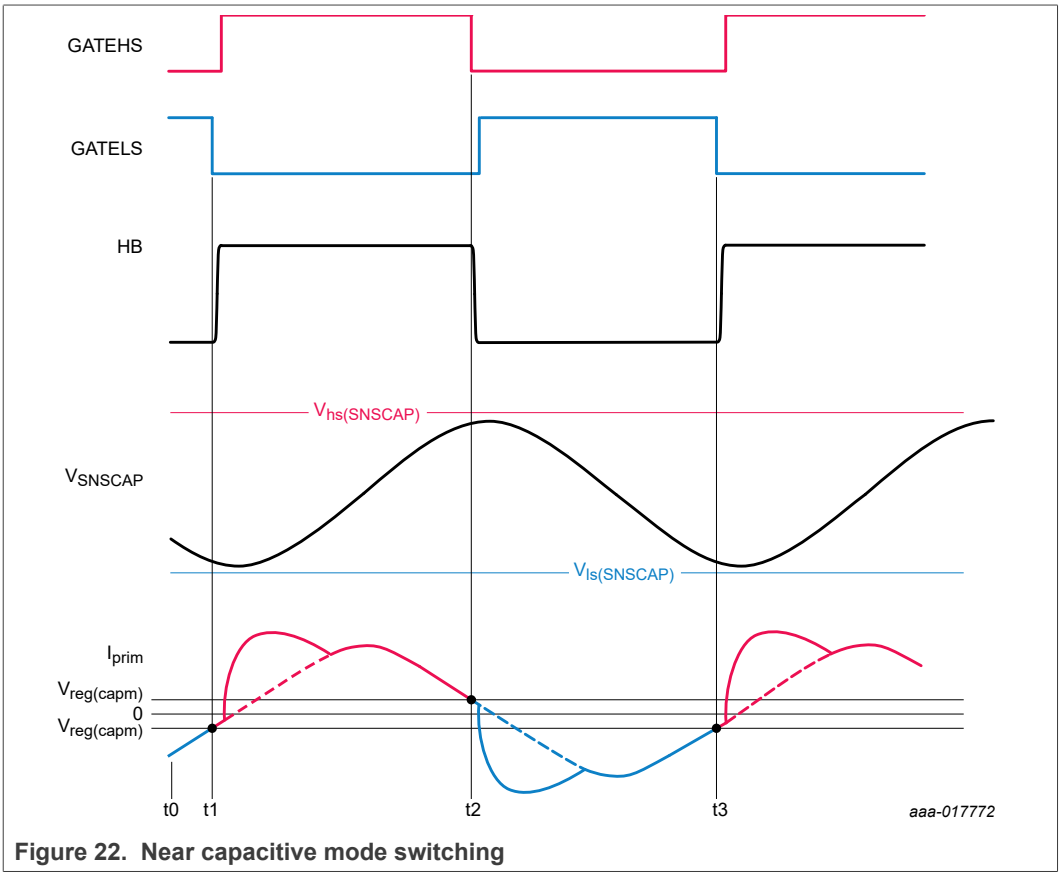



**Figure 22. Near capacitive mode switching**

### 8.6.15 Overcurrent protection

The system measures the primary current continuously via a sense resistor connected to the SNSCURLLC pin. If the measured voltage exceeds the fixed overcurrent level ($V_{ocp}$), the corresponding switch (GATELS/GATEHS) is turned off, but the system continuous switching. In this way, the primary current is limited to the OCP level.

The OCP level can be adjusted via the external sense resistor.

If the OCP is continuously triggered for an adjustable time, the system enters the OCP protection state. The OCP protection state can also be disabled. However, the primary current is always limited to the OCP level.

### 8.6.16 Maximum start-up time

Initially, the PFC starts switching at start-up. When the PFC output voltage exceeds a minimum level, the LLC starts switching as well.

If the output voltage of the LLC is not in regulation within an adjustable time after the PFC has started switching, the maximum start-up time protection is triggered.

The maximum start-up time can be set with parameter “Maximum start-up time”. If this protection is triggered, the system is latched or does a safe restart, which follows the setting of the OPP.

### 8.6.17 Overpower protection

For the overpower protection, three levels can be set:

- Absolute maximum output power, which is the highest output power level.
  When the output power exceeds this maximum level, it is limited cycle-by-cycle. If the output power exceeds this maximum, the output voltage decreases.
  The maximum output power can be set to a percentage of the rated output power.
- A first overpower level, which is below the maximum output power level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. Both PFC and LLC are switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the maximum output power is set to 170 % and this first overpower level is set to −20 %, the timer is started at 150 % of the rated output power.
  The timer of the first overpower level can also be set. The first overpower level can also be disabled.
- A second overpower level, which is typically below the first overpower level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. PFC and LLC are switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the output power is set to 170 % and this second overpower level is set to −50 %, the timer is started at 120 % of the rated output power.
  The timer of the second overpower level can be set to a predefined level. The second overpower level can also be disabled.

The overpower function can be either latched or safe restart. Section 8.6.18 describes this function.

### 8.6.18 Latched, safe restart, or latched after safe restart

When a protection is selected to be latched, the system stops switching when this protection is triggered. The system only restarts after a fast latch reset (see Section 8.6.19) or when the SUPIC supply voltage drops below the UVP level.

When selecting “latched after safe restart”, a protection is initially a safe restart protection. If the failure occurs again within a specific time, it latches eventually.

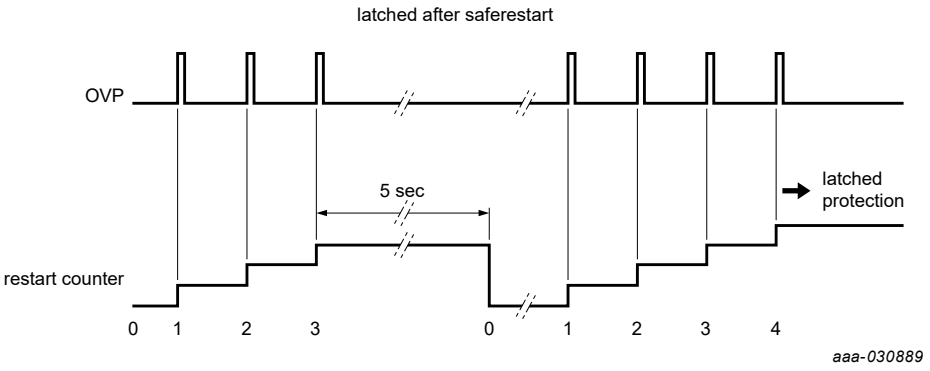



**Figure 23. Latched after safe restart**

Figure 23 shows an example of when the OVP is set to latched after safe restart. Initially at an OVP, the system restarts. An internal counter is then set to ‘1’. If the protection is triggered again after the safe restart, the counter is increased. If the counter reaches the number as set with a parameter, the system latches. If the protection is not triggered within 5 seconds, the counter is reset.

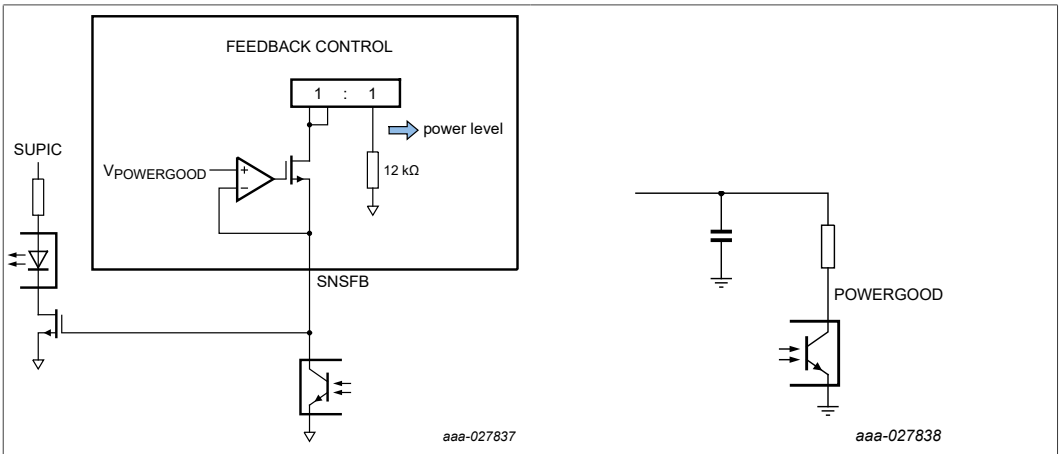
When a protection is selected to be safe restart, the system continuously restarts after a predefined period. This safe restart time is the same for all protection functions. It can be set with a parameter.

### 8.6.19 Fast latch reset

If a protection is triggered, the system enters the protection state. Especially when the protection is latched, this function is inconvenient during production tests. So, when the mains voltage is below the brownout level for a specified time, the system also restarts. This time can be set with a parameter.

## 8.7 Power good function

The TEA2016AAT provides a power good function via the SNSFB pin.




a. Primary side

b. Secondary side

**Figure 24. Power good function**

The primary function of the SNSFB pin is to regulate the output voltage via an optocoupler. So, it measures the current that is drawn from the SNSFB. Via an internal 12 kΩ resistor, it regulates the output power. The output power regulation is independent of the voltage level of the SNSFB pin. So, if the system is about to stop operating, the voltage level at the SNSFB pin is used to indicate; a so-called power good signal. The voltage at the SNSFB pin can be used to generate a secondary power good signal using an external MOSFET and an optocoupler.

At start-up, the SNSFB voltage is at a high level, pulling down the secondary power good signal. As soon as the system enters the operating state (see Figure 5), the SNSFB goes low. The external power good signal becomes active high.

The SNSFB voltage becomes active high, lowering the secondary power good signal when:

- The voltage on the SNSBOOST pin drops to below $V_{det(SNSBOOST)}$ (1.75 V)
- The OPP counter is close to its end value
- The converter is about to stop due to an OTP protection
- When the LLC converter is about to stop due to a mains brownout when this function is enabled

To avoid any disturbance of the regulation loop, the increase and decrease of the SNSFB voltage is in alignment with a predefined ramp.

When the system enters protection mode (OVP, OCP, or UVP), it pulls high the SNSFB pin and stops switching immediately.

## 8.8 Settings

The TEA2016AAT has an internal MTP at which different settings can be programmed.

**Disclaimer:**

The MTP parameter settings can be changed using the “Ringo” GUI software of NXP Semiconductors. Before the user can change any MTP parameters using the GUI, the terms and conditions in the start-up pop-up screen must be accepted.

### 8.8.1 General settings

#### 8.8.1.1 Protection register

When the TEA2016AAT triggers a protection, it can be read which protection was triggered. Even when the root cause of the protection is solved and the converter continues switching, the information about the protection remains until the software program (GUI) clears it.

#### 8.8.1.2 Supply start level

The SUPIC start level can be selected between 12 V and 19 V. Typically, a level of 19 V is selected. When the TEA2016AAT is externally supplied, for instance via a standby supply, the lower start level of 12 V can be used.

#### 8.8.1.3 Read lock

Normally, the software tool can read all the programmed settings. This option can be used to verify the correct settings or for failure analyses.

However, once in production, enabling the "Read lock" bit can protect the parameters. Then it is not possible anymore to read the MTP content. It can however still be reset to the default values and also clear the read lock parameter.

#### 8.8.1.4 Write lock

To avoid that the MTP content (accidentally) gets overwritten, a write-lock bit can be set. It can, however, still be reset to the default values and clear the write lock parameter.

### 8.8.2 PFC settings

#### 8.8.2.1 Soft-start time

For the soft-start time of the PFC, the following periods can be selected: 2 ms, 4 ms, 6 ms, or 8 ms.

#### 8.8.2.2 Active X-capacitor discharge

When the TEA2016AAT detects that the mains is disconnected, the X-capacitor discharge is activated after a delay of $t_{d(dch)Xcap}$. The following delays can be selected: 100 ms, 200 ms, and 400 ms. This function can also be disabled.

#### 8.8.2.3 Mains measurement impedance

To realize a low no-load input power level, the external resistor connected to the SNSMAINS pin for measuring the mains input voltage is typically 20 MΩ.

However, some applications request a maximum resistance of 10 MΩ. With this bit, 10 MΩ or 20 MΩ can be selected for the external resistor without affecting the mains voltage-related levels like brownin and brownout.

#### 8.8.2.4 Burst mode: Output voltage ripple

When the PFC enters burst mode, it stops switching when the SNSBOOST voltage, which reflects the PFC output voltage, reaches its regulation level. When the voltage at the SNSBOOST pin has dropped to a programmed level, the PFC is enabled again. For the difference between these two levels the following values can be selected: 35 mV, 70 mV, and 140 mV. These values typically correspond with a ripple on the PFC output voltage of 6 V, 12 V, or 24 V.

The PFC burst mode can also be synchronized to the LLC burst mode. It then follows the on and off periods of the LLC. However, it ensures that the SNSBOOST reaches its regulation level.

#### 8.8.2.5 Burst mode: Soft-start/soft-stop time

To minimize audible noise of the PFC, a burst mode soft start and soft stop can be independently selected. The selectable values are: 1 ms, 2 ms, and 4 ms. The additional soft-start and soft-stop can also be disabled.

### 8.8.3 LLC settings

#### 8.8.3.1 Start-up

**Maximum (start-up) frequency**

The maximum switching frequency of the LLC is limited to a value, which is defined using a parameter. This value also defines the maximum switching frequency during start-up. The maximum frequency can be set to different values ranging from 150 kHz to 800 kHz.

**LLC soft-start time**

The LLC soft-start time defines the speed at which the converter lowers its switching frequency. A higher speed lowers the start-up time. However, it can cause a high charge current and an overshoot at the output voltage. For the soft-start time, the following values can be selected: 2 ms to 16 ms in steps of 2 ms.

**Maximum primary current during start-up**

At start-up, the LLC starts switching at the maximum frequency and ramps down the frequency until the $\Delta V_{SNSCAP}$ reaches the required level. If during this start-up time the primary current, which reflects the output current, reaches a predefined level, the frequency is temporarily not further reduced until the primary current drops to below the level again. This level is measured via the SNSCURLLC pin. The following values can be selected: 0.5 V, 0.75 V, 1.0 V, or 1.25 V.

#### 8.8.3.2 LLC switching

**$\Delta V_{SNSCAP}$ storage level**

When the system is in low-power mode, a switching period is followed by a waiting period. The system ensures that it continues at the same stage as where it stopped. To reach the maximum efficiency, the end of the last switching cycle can be fine-tuned. For the $\Delta V_{SNSCAP}$ storage level, values between 2.525 V and 2.7 V can be selected in steps of 25 mV.

**Minimum non-overlap time**

To ensure that the GATEHS is properly turned off before the GATELS is turned on, and vice versa, there is a minimum non-overlap time. For the minimum non-overlap time, the following values can be selected: 50 ns, 100 ns, 150 ns, or 200 ns.

**Maximum non-overlap time**

When the system does not detect a valley at the HB node after turning off the GATEHS pin, the system turns on the GATELS after the maximum non-overlap time. The same counts when a peak at the HB node is not detected after turning off the GATELS and turning on the GATEHS. For the maximum non-overlap time, the following values can be selected: 0.5 µs, 0.7 µs, 0.9 µs, or 1.1 µs.

**Maximum on-time**

When the on-time of the GATELS or GATEHS exceeds the maximum on-time, the switch is turned off, and the LLC converter starts the next cycle. For the maximum on-time, the following values can be selected: 10 µs, 20 µs, 30 µs, or 40 µs.

**Capacitive mode regulation**

When the voltage at the SNSCURLLC pin, which reflects the resonant current, drops to below a predefined value, the LLC converter starts the next switching cycle. In this way, the TEA2016AAT avoids that the converter operates in capacitive mode. For the capacitive mode regulation, the following values can be selected: 20 mV to 160 mV in steps of 20 mV.

#### 8.8.3.3 Feedback

**Optocoupler current**

To achieve a low no-load input power, the current through the optocoupler must be set at a low level. However, depending on the selected optocoupler, a higher optocoupler current may be requested. So, the optocoupler current can be set to different values ranging from 80 µA to 1.2 mA.

#### 8.8.3.4 Operation modes

**HP-LP transition level**

When the output power drops to below a predefined level, the system switches from the HP to the LP mode. The HP-LP transition level can be set to different values ranging from 10 % to 54 %.

**HP-LP transition hysteresis**

When the system operates in LP mode, it switches over to HP mode when the output power exceeds the selected HP-LP transition level plus a hysteresis. For the hysteresis, the following values can be selected: 10 %, 20 %, 30 %, or 40 % of the selected HP-LP transition level. So, if the rated output at 100 % is 100 W, the HP-LP transition level is set at 30 % and the hysteresis is set at 10 %. The eventual hysteresis is 3 W.

**LP-BM transition level**

When the output power drops below the LP-BM transition level, the system enters burst mode. The LP-BM transition level can be set to different values ranging from 1 % to 25 %.

**LP-BM transition level tuning**

The LP-BM transition level can be set at very low levels. However, due to delays in the system the output power can increase. Setting the LP-BM transition level can be done in several steps up to a 0.7 % accuracy of the rated output power.

**BM-LP transition level**

When the system operates in burst mode and output power increases to exceed the LP-BM transition level plus a hysteresis level, the system enters low-power mode. For this hysteresis level, the following values can be selected: 25 %, 50 %, 75 %, and 100 % of the selected LP-BM transition level. So, if the rated output at 100 % is 100 W, the LP-BM transition is set at 10 %, and the hysteresis at 50 %. The system switches from burst mode to low-power mode at a level of 15 W.

**BM-LP transition level filter**

When the output power slowly increases, the system ensures a smooth transition when leaving burst mode and entering low-power mode by setting a burst-mode-to-low-power-mode transition filter. When the output power exceeds the BM-LP transition level plus hysteresis for 2, 4, 6, or 8 burst cycles, it leaves the burst mode and enters the low-power mode. At a large transient at the output, the system immediately leaves burst mode.

**BM repetition frequency**

When the system operates in burst mode, it is regulated to a fixed frequency. This frequency can be set to different values ranging from 20 Hz to 3.2 kHz.

**BM E/C (Energy-per-cycle) increase**

As the TEA2016AAT regulates the output via the primary capacitor voltage, it offers the ability to increase the output power per switching cycle when it enters burst mode. For the increase of output power per switching cycle, also called E/C (Energy-per-cycle), different values can be set ranging from 1 to 8. When, for instance, the E/C is set to 4, the system increases the E/C with a factor of 4 when it enters burst mode. The initial duty cycle is then 25 %. Increasing the E/C in burst mode increases the efficiency of the system, but at the cost of a higher output voltage ripple.

**BM soft start/soft stop**

To minimize the audible noise in burst mode, a soft start and a soft stop can be added. The soft start and soft stop can be independently initialized, whereas the number of soft-start/soft-stop cycles can be set between 0 and 6. In this way, the soft-start and soft-stop cycle can be optimized depending on the selected transformer.

**BM minimum cycles**

As additional soft-start and soft-stop cycles reduces the audible noise, it increases the switching losses. To optimize the number of normal switching cycles in relation to the added soft-start and soft-stop switching cycles, the minimum number of normal switching cycles that can be selected ranges from 1 to 12.

**Burst end SNSFB current**

When the system operates in burst mode, it adjusts the number of switching cycles such that burst frequency corresponds to the selected burst frequency. If during these switching cycles the output load decreases, the output voltage increases as the system has calculated the number of required switching cycles. If the measured optocoupler current at the SNSFB pin exceeds a certain level, the system ends the burst switching cycle. This level can be between a factor of 2.5, 3.75, 5, or 7.5 times the selected optocoupler current level.

**Low-power frequency**

The frequency of the low-power mode can be selected by defining the ringing number at which the next low-power cycle must be started. The selection options are from 1 to 8 in steps of 1.

**SNSBOOST compensation**

A ripple at the input voltage of an LLC converter normally results in a ripple in the output voltage. To minimize the ripple at the output voltage, the TEA2016AAT measures the input voltage of the LLC via the SNSBOOST pin and compensates the SNSCAP voltage via a feedforward compensation. To minimize the ripple at the output voltage, it has a feedforward compensation. As the compensation depends on the external components, it can be set at 8 different compensation levels.

### 8.8.4 Protection settings

#### 8.8.4.1 General protections

**Fast latch reset delay time**

When the system does not detect a mains voltage for a programmed period, it assumes that the mains is disconnected and resets all protections. When the mains voltage exceeds the brownin level again, the system restarts. The delay between detecting a brownout (including the brownout delay time) and resetting all protections can be programmed to different values ranging from 0 s to 10 s.

**Safe restart time**

When the system is in protection mode and the triggered protection is programmed as safe restart, it restarts after a safe-restart time. This time can be set at different values ranging from 0.5 s to 10 s.

**External OTP level**

The external application temperature is measured via an NTC connected to the SNSMAINS pin. To be able to set the appropriate NTC value and OTP level, the internal current used to measure the external NTC value can be set between 150 µA and 1050 µA in steps of 150 µA.

To avoid false triggering of the external OTP, a delay can be set at different values ranging from 0.5 s to 8 s. As the NTC measurement follows the mains cycles, the OTP delay varies with the mains frequency.

**Internal OTP level**

The internal OTP is fixed at 135 °C. When the internal OTP is triggered, it follows the same response as selected for the external OTP, being either latched, safe restart, or latched after safe restart.

#### 8.8.4.2 PFC general protections

**Brownin/brownout level**

For the brownin level, several values can be selected ranging from 70 V (AC) to 190 V (AC). For the hysteresis between the brownin and brownout level, several values can be selected from 2 V (AC) to 17 V (AC).

When the mains voltage is below the brownout period for a selectable amount of time, the system enters the brownout state. For this time, several values can be selected ranging from 25 ms to 1.2 s.

**PFC OCP level**

The PFC OCP level is fixed to $V_{ocp(PFC)}$. The external sense resistor can select the corresponding current value.

To avoid false triggering of the OCP function when turning on the PFC MOSFET, a short blanking time occurs after the PFC MOSFET is turned on and the internal OCP function is activated. For this blanking time, the following values can be selected: 200 ns, 300 ns, 400 ns, and 500 ns.

**PFC maximum on-time**

When the on-time of the PFC MOSFET exceeds the maximum on-time, the PFC MOSFET is turned off and turned on again at the next cycle. For the maximum on-time, the following values can be selected: 37.5 µs, 50 µs, 75 µs, and 100 µs.

**PFC output OVP**

The PFC output voltage is measured via the SNSBOOST pin and the DRAINPFC pin. For the OVP at the SNSBOOST pin, the following values can be selected: 2.60 V, 2.63 V, 2.65 V, or 2.70 V.

When an OVP is detected at the SNSBOOST pin, the PFC stops switching and continues again when its voltage drops below the regulation level.

For the OVP at the DRAINPFC pin, the following values can be selected: 475 V, 500 V, 525 V, or 550 V. To avoid false triggering, a delay can be selected between 2 ms, 5 ms, and 20 ms. During this delay, the output voltage of the PFC is limited to this maximum value.

The response of an OVP at the DRAINPFC pin can be latched, safe restart, or latched after safe restart. This function can also be disabled.

**Valley detection timeout**

Normally, a valley is detected within a period after demagnetization. However, when the PFC control loop detects demagnetization but does not detect a valley within a certain time, it assumes that the ringing is too small to detect a valley. So, it assumes a valley after a specified time. For this time, the following values can be selected: 5 µs, 10 µs, 15 µs, or 20 µs.

**PFC minimum off-time**

To avoid false triggering of the demagnetization and valley detection, a minimum off-time of the PFC driver output can be selected. The available values are 250 ns, 500 ns, 1 µs, and 1.5 µs.

**PFC maximum switching frequency**

To increase the efficiency of the PFC, its switching frequency is limited. For the maximum switching frequency of the PFC, the following values can be selected: 75 kHz, 125 kHz, 250 kHz, and 500 kHz.

#### 8.8.4.3 LLC general protections

**Maximum start-up time**

When the system starts switching, it expects that the LLC output voltage reaches its regulation level within a maximum start-up time. For the maximum start-up time, the following values can be selected: 25 ms, 50 ms, 100 ms, and 200 ms. When the PFC starts switching, this timer is started.

**LLC brownout level (SNSBOOST)**

When the voltage at the SNSBOOST drops below a predefined level, the LLC converter enters the protection state. When the SNSBOOST voltage exceeds the start level, the LLC converter starts switching again.

For the LLC brownout level at the SNSBOOST, several levels can be selected ranging from 1.0 V to 1.7 V.

**LLC brownin level (SNSBOOST)**

The LLC brownin level defines the minimum voltage at the SNSBOOST pin before the LLC starts switching. For this level, a value ranging from 2.1 V to 2.4 V can be selected in steps of 0.1 V.

**LLC brownout timer (SNSMAINS)**

When the mains is disconnected, the PFC stops switching after its brownout delay. Normally, the LLC converter continues switching until the input voltage of the LLC drops to below a minimum level. Especially at a minimum load at the output, the LLC dropping to the minimum level can take a long time.

A timer can be initialized that also disables the LLC converter when a brownout is detected at the mains input. For this time, a value can be selected ranging from 125 ms to 6 s. The option that the LLC converter remains switching until its input voltage drops to below a minimum level can also be selected.

#### LLC maximum input voltage (SNSBOOST)

When an OVP is detected on the SNSBOOST pin, the PFC always stops switching. The response of the LLC can be set to either continue operation or to stop switching until the voltage the SNSBOOST drops to below the PFC output voltage regulation level. A delay can be set to either 5 ms, 50 ms, or 500 ms.

#### Power limit

The maximum output power of the converter is limited by the controller. The limitation ensures that the applied load is below the maximum rating-selected components. For the maximum output power, several levels between 100 % and 200 % of the rated power can be selected.

#### OPP level 1

When the output power exceeds a first OPP level, a first counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level between 0 % and −50 % below the selected power limit can be selected.

For the time, a value between 0 s to 3 s can be selected. The response of this protection can be latched, safe restart, or latched after safe restart. This OPP level can also be disabled.

#### OPP level 2

When the output power exceeds a second OPP level, a second counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level in the range from −10 % to −90 % below the selected power limit can be selected.

For the time, a value ranging from 50 ms to 3 s can be selected. The response of this protection follows the selected response of the OPP level 1. This OPP level can also be disabled.

#### OPP duty cycle

When the output power exceeds the OPP with a duty cycle of 50 %, the OPP may or may not be triggered. So, the duty cycle at which the OPP is triggered eventually can be set using a parameter to 11 %, 20 %, 33 %, or 50 %.

#### OVP protection

In a resonant converter, the voltage at the SUPIC pin reflects the output voltage. When the SUPIC voltage exceeds a defined level, the OVP protection is triggered. The level can be set between 1 V and 16 V above the start level in steps of 1 V.

To avoid false triggering, a delay can be set at different values ranging from10 µs to 800 µs. The response of this protection can be latched, safe restart, or latched after safe restart. This OVP function can also be disabled.

#### OVP duty cycle

To minimize the sensitivity of the OVP function, a duty cycle can be set at which the OVP is eventually triggered. This parameter can be set to 11 %, 20 %, 33 %, or 50 %.

**OCP protection**

The current in the resonant tank is measured at the SNSCURLLC pin. When the voltage at this pin exceeds the OCP level, the corresponding switch (GATELS or GATEHS) is turned off and the system starts the next cycle. So, the output power is limited cycle-by-cycle. If the OCP occurs for a defined number of cycles, the OCP protection is triggered. The number of cycles can be set to different values between 5 and 1000.

The response of this protection can be latched, safe restart, or latched after safe restart. The OCP protection function can also be disabled. However, the output power remains limited cycle-by-cycle.

### 8.8.5 Power good settings

The power good function gives a prewarning to the load that the converter is switched off due to disconnected mains or a triggered protection.

**Power good time**

The power good time is the time between the power good signal indicating that the converter is about to be switched off and the time the converter eventually stops switching. This delay can be set to 2 ms, 4 ms, 6 ms, or 8 ms.

**Power good at OTP**

The power good signal can give a prewarning when the converter is switched off due to an OTP detection. The OTP can be either an internal or an external OTP.

The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time. This function can be enabled or disabled.

**Power good at OPP**

The power good signal can give a prewarning when the converter is switched off due to an OPP detection. The prewarning can be given when the output power exceeds the OPP level1 or OPP level2 for the defined time.

The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time. This function can be enabled or disabled.

**Power good at brownout**

The power good signal can give a prewarning when the LLC converter is switched off due to a brownout detection at the mains input of the converter.

The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time. This function can be enabled or disabled.

**Power good at LLC brownout level (SNSBOOST)**

When the measured voltage at the SNSBOOST pin drops to below the selected LLC brownout level, the LLC converter stops switching. It normally occurs due to a disconnected mains.

The power good signal can give a prewarning when the converter is switched off due to this LLC brownout detection. When the voltage at the SNSBOOST drops to below a selectable value, the power good feature is triggered. The level can be selected between 1.1 V and in a range from 1.2 V to 1.9 V in steps of 50 mV.

### LLC maximum input voltage (SNSBOOST)

When an OVP is detected at the SNSBOOST pin, the LLC can be disabled after a specified delay. Disabling the LLC depends on a parameter. The power good signal can give a prewarning when the converter is switched off because of the LLC maximum input voltage. The delay between the transition of the power good signal and the moment that the converter stops switching, equals the power good time. This function can be enabled or disabled.

### Power good ready delay

When the output voltage is in regulation after start-up, power good indicates that the output voltage is in regulation. A delay can be set between the time the output voltage reaches the regulation level and the transition of the power good signal. This delay can be set at different values between 0 s and 1 s.

### Power good transition time

The power good function is combined with the feedback network connected at the SNSFB pin. To avoid that a trigger of the power good function disturbs the regulation loop, its transition time must have a predefined value. This time can be set at 1 ms, 2 ms, 3 ms, or 4 ms.

# 9 Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Voltages** | | | | | |
| $V_{DRAINPFC}$ | voltage on pin DRAINPFC | during mains surge t < 0.5 s; 10 times at a 0.1 Hz interval | −0.4 | +685 | V |
| $SR_{DRAINPFC}$ | slew rate on pin DRAINPFC | | −50 | +50 | V/ns |
| $V_{SUPIC}$ | voltage on pin SUPIC | | −0.4 | +36 | V |
| $V_{SUPHS}$ | voltage on pin SUPHS | during mains surge t < 0.5 s; 10 times at a 0.1 Hz interval | −0.3 | +685 | V |
| | | pin HB | − 0.4 | +13 | V |
| $V_{GATEHS}$ | voltage on pin GATEHS | | $V_{HB}$ − 0.4 | $V_{SUPHS}$ + 0.4 | V |
| $V_{HB}$ | voltage on pin HB | during mains surge; t < 0.5 s; 10 times at a 0.1 Hz interval | −3 | +685 | V |
| | | t < 1 µs | −13 | - | V |
| $SR_{max(HB)}$ | maximum slew rate on pin HB | [1] | −70 | +70 | V/ns |
| $V_{GATELS}$ | voltage on pin GATELS | [2] | −0.4 | +14 | V |
| $V_{GATEPFC}$ | voltage on pin GATEPFC | [2] | −0.4 | +14 | V |
| $V_{SNSCAP}$ | voltage on pin SNSCAP | | −0.4 | +12 | V |
| $V_{SNSCURLLC}$ | voltage on pin SNSCURLLC | | −0.4 | +12 | V |
| $V_{SNSCURPFC}$ | voltage on pin SNSCURPFC | t < 0.1 s; voltage at external series resistance of 100 Ω, connected to pin SNSCURPFC | −18 | +12 | V |
| | | DC; maximum | −0.4 | +12 | V |
| $V_{SNSFB}$ | voltage on pin SNSFB | | −0.4 | +12 | V |
| $V_{SNSBOOST}$ | voltage on pin SNSBOOST | | −0.4 | +12 | V |
| $V_{SNSMAINS}$ | voltage on pin SNSMAINS | | −0.4 | +12 | V |

**Table 5. Limiting values***...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb}$ < 75 °C | - | 0.7 | W |
| $T_j$ | junction temperature | | −40 | +150 | °C |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| **Latch-up** | | | | | |
| $I_{lu}$ | latch-up current | all pins; according to JEDEC; standard 78D | −100 | +100 | mA |
| **Electrostatic discharge** | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | human body model | | | |
| | | SUPHS, GATEHS, HB, SDA, SCL, and DRAINPFC pins | −1000 | +1000 | V |
| | | other pins | −2000 | +2000 | V |
| | | charged device model; all pins | −500 | +500 | V |

[1] To prevent erroneous operation due to high HB dV/dt disturbances, a maximum slew rate of 25 V/ns is recommended. A practical guideline for checking an application for disturbance by high HB dV/dt is provided in the "TEA2016 PFC + LLC controller IC" application note (AN12330).

[2] Although the GATE pins are output pins, the maximum voltage of these pins must not exceed the normal maximum drive output voltage by 20 %.

# 10 Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | In free air; JEDEC test board | 107 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | In free air; JEDEC test board | 60 | K/W |

# 11 Characteristics

**Table 7. Characteristics**

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAINPFC pin** | | | | | | |
| $I_{off(DRAINPFC)}$ | off-state current on pin DRAINPFC | $V_{DRAINPFC}$ = 400 V; $V_{SUPIC}$ = 19 V | 2 | 5 | 8 | µA |
| $V_{DRAINPFC}$ | voltage on pin DRAINPFC | $V_{SUPIC}$ = 19 V; $I_{DRAINPFC}$ = 3 mA | 22 | 26 | 30 | V |
| $I_{ch(SUPIC)}$ | charge current on pin SUPIC | $V_{DRAINPFC}$ = 50 V; $V_{SUPIC}$ = 19 V | −10 | −6.5 | −3 | mA |
| **SUPIC pin** | | | | | | |
| $V_{start(SUPIC)}$ | start voltage on pin SUPIC | | 18.2 | 19.0 | 19.7 | V |
| $V_{start(hys)SUPIC}$ | start voltage hysteresis on pin SUPIC | | −0.9 | −0.7 | −0.5 | V |
| $V_{low(hys)SUPIC}$ | low voltage hysteresis on pin SUPIC | | 0.50 | 0.70 | 0.90 | V |
| $V_{low(SUPIC)}$ | low voltage on pin SUPIC | | 11.50 | 12.00 | 12.50 | V |
| $V_{uvp(SUPIC)}$ | undervoltage protection voltage on pin SUPIC | | 9.6 | 10.00 | 10.40 | V |
| $\Delta_{(vlow-vuvp)SUPIC}$ | low voltage to undervoltage protection voltage difference | $V_{low} - V_{uvp}$ | 1.7 | 2.0 | 2.3 | V |
| $V_{rst(SUPIC)}$ | reset voltage on pin SUPIC | | 8.60 | 9.00 | 9.40 | V |
| $I_{CC(SUPIC)}$ | supply current on pin SUPIC | non-operating mode; $I_{snsfb}$ = −100 µA; $I_{snscap}$ = −100 µA [1] | 700 | 865 | 1100 | µA |
| | | operating mode; $f_{HB}$ = 100 kHz; $I_{snsfb}$ = −80 µA; $I_{snscap}$ = −100 µA; driver pins open [1] | 4.0 | 4.8 | 6.0 | mA |
| Output overvoltage protection | | | | | | |
| $V_{O(ovp)SUPIC}$ | output overvoltage protection voltage on pin SUPIC | OVP level setting = 9.5 V; SUPIC start level setting = 19 V | 27.7 | 28.5 | 29.3 | V |
| $t_{d(ovp)SUPIC}$ | overvoltage protection delay time on pin SUPIC | | 45 | 50 | 55 | µs |
| **Mains voltage sensing (SNSMAINS pin)** | | | | | | |
| $I_{clamp(max)}$ | maximum clamp current | $V_{SNSMAINS}$ = 9.5 V | 2.5 | 3.5 | 4.5 | mA |
| $I_{I(lim)SNSMAINS}$ | limiting input current on pin SNSMAINS | SNSMAINS limit measuring input current | 17.6 | 19.0 | 20.4 | µA |
| $I_{bi}$ | brownin current | | 5.15 | 5.5 | 5.90 | µA |
| $I_{bo}$ | brownout current | | 4.41 | 4.75 | 5.09 | µA |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{bo(hys)}$ | hysteresis of brownout current | $I_{bi} - I_{bo}$ | 660 | 750 | 880 | nA |
| $t_{d(det)bo}$ | brownout detection delay time | PFC | 45 | 50 | 55 | ms |
| | | LLC | 225 | 250 | 275 | ms |
| External overtemperature measurement | | | | | | |
| $I_{o(SNSMAINS)}$ | output current on pin SNSMAINS | | −645 | −600 | −565 | µA |
| $t_{det(max)NTC}$ | NTC maximum detection time | | 45 | 50 | 55 | µs |
| $V_{det(SNSMAINS)}$ | detection voltage on pin SNSMAINS | NTC measurement; $I_{SNSMAINS}$ = −600 µA | 2.80 | 3.0 | 3.16 | V |
| $t_{d(otp)}$ | overtemperature protection delay time | | 3600 | 4000 | 4400 | ms |
| **X-capacitor discharge** | | | | | | |
| $t_{d(dch)}$ | discharge delay time | | 180 | 200 | 220 | ms |
| **SNSCURPFC pin** | | | | | | |
| $I_{o(min)SNSCURPFC}$ | minimum output current on pin SNSCURPFC | for open pin protection; $V_{SNSCURPFC}$ = 500 mV; Gate PFC is on | −1.35 | −1.10 | −0.85 | µA |
| $V_{det(SNSCURPFC)}$ | detection voltage on pin SNSCURPFC | open pin detection level | 190 | 235 | 280 | mV |
| $V_{det(demag)}$ | demagnetization detection voltage | | −16 | −11 | −6 | mV |
| $V_{ocp(PFC)}$ | PFC overcurrent protection voltage | GatePFC is on | −325 | −305 | −285 | mV |
| $t_{d(swoff)driver}$ | driver switch-off delay time | dV/dt ≤ −100 mV/µs | 190 | 265 | 340 | ns |
| $t_{leb}$ | leading edge blanking time | | 270 | 300 | 330 | ns |
| $t_{d(ocp)PFC}$ | PFC overcurrent protection delay time | | 90 | 100 | 110 | ms |
| **Valley sensing (DRAINPFC pin)** | | | | | | |
| $\Delta V_{det(min)}/\Delta t$ | minimum slope detection voltage | | −50 | - | −25 | V/µs |
| $\Delta V_{det(min)}$ | minimum detection voltage change | ringing frequency = 1 MHz | 20 | 25 | 30 | V |
| $t_{to(vrec)}$ | valley recognition time-out time | | 9 | 10 | 11 | µs |
| **PFC** | | | | | | |
| PFC timing | | | | | | |
| $t_{off(PFC)min}$ | PFC minimum off-time | | 1.35 | 1.5 | 1.65 | µs |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PFC start-up soft-start time | | | | | | |
| $t_{start(soft)}$ | soft start time | | 5.4 | 6.0 | 6.6 | ms |
| PFC maximum on-time | | | | | | |
| $t_{on(max)PFC}$ | PFC maximum on-time | low mains voltage (74 V (AC)) | 45 | 50 | 55 | µs |
| | | high mains voltage | 3.6 | 4.0 | 4.4 | µs |
| PFC maximum frequency | | | | | | |
| $f_{sw(PFC)max}$ | maximum PFC switching frequency | | 112.5 | 125 | 137.5 | kHz |
| **GATEPFC pin** | | | | | | |
| $I_{source(peak)}$ | source peak current | $C_{load}$ = 4.7 nF; $V_{SUPIC}$ ≥ 13 V [1] | −1.1 | −0.9 | −0.7 | A |
| $I_{sink(peak)}$ | sink peak current | $C_{load}$ = 4.7 nF; $V_{SUPIC}$ ≥ 13 V [1] | 0.7 | 1.0 | 1.3 | A |
| $R_{OH(GATEPFC)}$ | HIGH-level output resistance on pin GATEPFC | $I_{GATEPFC}$ = −30 mA; $V_{SUPIC}$ = 14.5 V | 8 | 14 | 20 | Ω |
| $R_{OL(GATEPFC)}$ | LOW-level output resistance on pin GATEPFC | $I_{GATEPFC}$ = 30 mA; $V_{SUPIC}$ = 14.5 V | 3 | 4.5 | 6 | Ω |
| $V_{OH(GATEPFC)}$ | HIGH-level output voltage on pin GATEPFC | $V_{SUPIC}$ ≥ 14.5 V; $f_{sw}$ = 50 kHz; $I_{load}$ = 0 [1] | 11.5 | 12.3 | 13.1 | V |
| | | $V_{SUPIC}$ = 9.5 V; $f_{sw}$ = 50 k Hz;`$I_{load}$ = 0 [1] | 9.45 | 9.5 | 9.55 | V |
| $V_{OL(GATEPFC)}$ | LOW-level output voltage on pin GATEPFC | $I_{GATEPFC}$ = 40 mA; $V_{SUPIC}$ ≥ 14.5 V | 0.10 | 0.17 | 0.24 | V |
| $t_{r(GATEPFC)}$ | rise time on pin GATEPFC | 1 V to 9 V; $V_{SUPIC}$ = 13 V; 1 n F load [1] | 10 | 15 | 20 | ns |
| $t_{f(GATEPFC)}$ | fall time on pin GATEPFC | 9 V to 1 V; $V_{SUPIC}$ = 13 V; 1 n F load [1] | 10 | 15 | 20 | ns |
| **SNSBOOST pin** | | | | | | |
| PFC part | | | | | | |
| $I_{pd(SNSBOOST)}$ | pull-down current on pin SNSBOOST | at $V_{SNSBOOST}$ = $V_{scp(stop)}$ | 25 | 50 | 75 | nA |
| $V_{reg(SNSBOOST)}$ | regulation voltage on pin SNSBOOST | | 2.475 | 2.500 | 2.525 | V |
| $V_{stop(ovp)PFC}$ | PFC overvoltage protection stop voltage | | 2.59 | 2.63 | 2.67 | V |
| $V_{prot(ovp)PFC}$ | PFC overvoltage protection protection voltage | via DRAINPFC pin [2] | 450 | 500 | 550 | V |
| $t_{leb(ovp)PFC}$ | PFC overvoltage protection leading-edge blanking time | via pin DRAINPFC | 360 | 400 | 440 | ns |
| LLC part | | | | | | |
| $V_{uvp(SNSBOOST)}$ | undervoltage protection voltage on pin SNSBOOST | | 1.60 | 1.65 | 1.70 | V |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{start(SNSBOOST)}$ | start voltage on pin SNSBOOST | | 2.2 | 2.3 | 2.4 | V |
| $V_{det(SNSBOOST)}$ | detection voltage on pin SNSBOOST | Power good detection voltage | 1.715 | 1.75 | 1.785 | V |
| $\Delta V_{reg-det}$ | voltage difference between regulation and detection | pin SNSBOOST; indication of the power good delay | 0.720 | 0.75 | 0.780 | V |
| **Fast disable function** | | | | | | |
| $V_{scp(stop)}$ | stop short-circuit protection voltage | | 0.37 | 0.39 | 0.41 | V |
| $V_{scp(start)}$ | start short-circuit protection voltage | | 0.40 | 0.45 | 0.50 | V |
| $t_{fltr(scp)}$ | short-circuit protection filter time | | 4.5 | 5.0 | 5.5 | µs |
| **SNSCAP pin** | | | | | | |
| $V_{AV(regd)SNSCAP}$ | regulated average voltage on pin SNSCAP | regulated average of $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ | 2.44 | 2.50 | 2.56 | V |
| $I_{bias(max)SNSCAP}$ | maximum bias current on pin SNSCAP | | −245 | −210 | −175 | µA |
| $V_{range(SNSCAP)}$ | voltage range on pin SNSCAP | SNSCAP voltage range for the high-side comparator, $V_{hs(SNSCAP)}$. | 2.35 | - | 4.50 | V |
| | | SNSCAP voltage range for the low-side comparator, $V_{ls(SNSCAP)}$. | 0.5 | - | 2.65 | V |
| $V_{acc}$ | voltage accuracy | SNSCAP comparator voltage accuracy | −10 | - | +10 | mV |
| $\Delta V_{th(SNSCAP)}$ | threshold voltage difference on pin SNSCAP | $V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; $P_{out}$ = 200 %; $V_{SNSBOOST}$ < 1.9 V | 3.12 | 3.27 | 3.42 | V |
| | | $V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; $P_{out}$ = 100 %; $V_{SNSBOOST}$ = 2.5 V | 0.93 | 1.01 | 1.09 | V |
| $t_d$ | delay time | delay between exceeding $V_{caph}/V_{capl}$ and driver off; dV/dt = 0.1 V/µs | - | - | 125 | ns |
| **SNSCURLLC pin** | | | | | | |
| $V_{bias(SNSCURLLC)}$ | bias voltage on pin SNSCURLLC | | 2.4 | 2.5 | 2.6 | V |
| $R_{O(SNSCURLLC)}$ | output resistance on pin SNSCURLLC | | 45 | 55 | 65 | kΩ |
| $V_{lmtr(ocp)}$ | overcurrent protection voltage limiter | soft-start overcurrent limiter | 0.68 | 0.75 | 0.83 | V |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ocp(LLC)}$ | LLC overcurrent protection voltage | positive level $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$ | 1.35 | 1.50 | 1.65 | V |
| | | negative level $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$ | −1.65 | −1.50 | −1.35 | V |
| $V_{reg(capm)}$ | capacitive mode regulation level | positive level $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$ | 85 | 100 | 115 | mV |
| | | negative level $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$ | −115 | −100 | −85 | mV |
| $V_{det(zero)}$ | zero detection voltage | detected as ≥ 0 | −24 | −13 | −1 | mV |
| | | detected as ≤ 0 | 1 | 13 | 24 | mV |
| **SNSFB pin** | | | | | | |
| $V_{lowSNSFB)}$ | low voltage on pin SNSFB | indicating iPowerGood = '1'; 0 µA < $I_{opto}$ < 3.5 mA. | 0.43 | 0.50 | 0.57 | V |
| $V_{high(SNSFB)}$ | high voltage on pin SNSFB | indicating iPowerGood = '0'; 0 µA < $I_{opto}$ < 3.5 mA. | 3.3 | 3.5 | 3.8 | V |
| $t_t$ | transition time | PowerGood transition time | 1.6 | 1.8 | 1.9 | ms |
| Optobias regulator | | | | | | |
| $I_{reg(SNSFB)}$ | regulation current on pin SNSFB | | −90 | −80 | −70 | µA |
| Burst mode regulator | | | | | | |
| $I_{start(burst)}$ | burst mode start current | LLC burst mode | −110 | −100 | −90 | µA |
| $I_{stop(burst)}$ | burst mode stop current | | −220 | −200 | −180 | µA |
| Burst mode | | | | | | |
| $f_{burst(max)}$ | maximum burst mode frequency | | 720 | 800 | 880 | Hz |
| $\delta_{en(burst)}$ | burst mode duty cycle enable | enable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst time / set LLC burst period | 49 | 50 | 51 | % |
| $N_{cy(en)burst}$ | burst mode enable number of cycles | enable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst time / set LLC burst period | 8 | 8 | 8 | - |
| $\delta_{dis(burst)}$ | burst mode disable duty cycle | enable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst time / set LLC burst period | 74 | 75 | 76 | % |
| $\Delta V_{burst(PFC)}$ | PFC burst mode voltage difference | | 66.5 | 70 | 73.5 | mV |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{start(soft)burst}$ | PFC burst mode soft start time | | 1.8 | 2.0 | 2.2 | ms |
| $t_{stop(soft)burst}$ | PFC burst soft stop time | | 1.8 | 2.0 | 2.2 | ms |
| **LLC timing** | | | | | | |
| $t_{on(min)LLC}$ | LLC minimum on-time | | 1105 | 1230 | 1355 | ns |
| $t_{on(max)LLC}$ | LLC maximum on-time | | 18.0 | 20.0 | 22.0 | µs |
| **Overpower protection** | | | | | | |
| $t_{startup(max)}$ | maximum start-up time | | 90 | 100 | 110 | ms |
| $t_{d(opp)}$ | overpower protection delay time | opp 1 | 45 | 50 | 55 | ms |
| | | opp 2 | 450 | 500 | 550 | ms |
| **Power good characteristics (pin SNSFB)** | | | | | | |
| $t_d$ | delay time | Power good delay after output | 4.5 | 5 | 5.5 | ms |
| | | Power good delay before protection | 3.6 | 4.0 | 4.4 | ms |
| **HB pin** | | | | | | |
| $V_{det(min)}$ | minimum detection voltage | slope detection level at HB node | - | - | 120 | V/µs |
| $V_{det(max)}$ | maximum detection voltage | slope detection level at HB node | 50 | - | - | V/ns |
| $t_{no(min)}$ | minimum non-overlap time | between low side and high side | 243 | 270 | 297 | ns |
| | | between high side and low side | 207 | 230 | 253 | ns |
| $t_{no(max)}$ | maximum non-overlap time | | 0.99 | 1.1 | 1.21 | µs |
| **GATELS pin** | | | | | | |
| $I_{source(peak)}$ | source peak current | $C_{load}$ = 4.7 nF; $V_{SUPIC}$ ≥ 13 V [1] | −1.1 | −0.9 | −0.7 | mA |
| $I_{sink(peak)}$ | sink peak current | $C_{load}$ = 4.7 nF; $V_{SUPIC}$ ≥ 13 V [1] | 0.7 | 1.0 | 1.3 | mA |
| $R_{OH(GATELS)}$ | HIGH-level output resistance on pin GATELS | $I_{GATELS}$ = −30 mA; $V_{SUPIC}$ = 14.5 V | 8 | 14 | 20 | Ω |
| $R_{OL(GATELS)}$ | LOW-level output resistance on pin GATELS | $I_{GATELS}$ = 30 mA; $V_{SUPIC}$ = 14.5 V | 3 | 4.5 | 6 | Ω |
| $V_{OH(GATELS)}$ | HIGH-level output voltage on pin GATELS | $f_{sw}$ = 100 kHz; $I_{load}$ = 0; $V_{SUPIC}$ ≥ 14.5 V [1] | 11.5 | 12.3 | 13.1 | V |
| | | $f_{sw}$ = 100 kHz; $I_{load}$ = 0; $V_{SUPIC}$ = 9.5 V [1] | 9.45 | 9.5 | 9.55 | V |
| $V_{OL(GATELS)}$ | LOW-level output voltage on pin GATELS | $I_{GATELS}$ = 40 mA; $V_{SUPIC}$ ≥ 14.5 V | 0.10 | 0.17 | 0.24 | V |
| $t_{r(GATELS)}$ | rise time on pin GATELS | 1 V to 9 V; $V_{SUPIC}$ = 13 V; 1 nF load [1] | 10 | 15 | 20 | ns |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{SUPIC}$ = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{f(GATELS)}$ | fall time on pin GATELS | 9 V to 1 V; $V_{SUPIC}$ = 13 V; 1 n F load [1] | 10 | 15 | 20 | ns |
| **GATEHS pin** | | | | | | |
| $I_{source(peak)}$ | source peak current | $C_{load}$ = 4.7 nF; $V_{SUPHS} - V_{HB}$ = 12 V [1] | −0.8 | −0.6 | −0.4 | mA |
| $I_{sink(peak)}$ | sink peak current | $C_{load}$ = 4.7 nF; $V_{SUPHS} - V_{HB}$ = 12 V [1] | 0.8 | 1.1 | 1.4 | mA |
| $R_{OH(GATEHS)}$ | HIGH-level output resistance on pin GATEHS | $I_{GATEHS}$ = −30 mA; $V_{SUPIC}$ = 12 V | 6 | 10 | 14 | Ω |
| $R_{OL(GATEHS)}$ | LOW-level output resistance on pin GATEHS | $I_{GATEHS}$ = 30 mA; $V_{SUPIC}$ = 12 V | 3 | 5 | 7 | Ω |
| $V_{OH(GATEHS)}$ | HIGH-level output voltage on pin GATEHS | $f_{sw}$ = 100 kHz; $I_{load}$ = 0; $V_{SUPHS} - V_{HB}$ = 12 V [1] | 11.5 | 12 | 12.5 | V |
| $V_{OL(GATEHS)}$ | LOW-level output voltage on pin GATEHS | $I_{GATELS}$ = 40 mA; $V_{SUPHS} - V_{HB}$ = 12 V | 0.1 | 0.2 | 0.3 | V |
| $t_{r(GATEHS)}$ | rise time on pin GATEHS | 1 V to 9 V; $V_{SUPHS} - V_{HB}$ = 11 V; 1 n F load [1] | 15 | 25 | 35 | ns |
| $t_{f(GATELS)}$ | fall time on pin GATELS | 9 V to 1 V; $V_{SUPHS} - V_{HB}$ = 11 V; 1 n F load [1] | 10 | 15 | 20 | ns |
| **SUPHS pin** | | | | | | |
| $V_{rst(SUPHS)}$ | reset voltage on pin SUPHS | +25 °C < T < 125 °C | 5.5 | 7.2 | 8.2 | V |
| **System protection** | | | | | | |
| $t_{d(restart)}$ | restart delay time | | 0.9 | 1.0 | 1.1 | s |
| $t_{d(flr)}$ | fast latch reset delay time | | 45 | 50 | 55 | ms |
| **$I^2C$ communication** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | - | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 1.4 | - | 5.0 | V |
| $I_{pd(SNSCAP)}$ | pull-down current on pin SNSCAP | To guarantee proper operation, the external pull-up must always be lower than 6.8 mA. [3] | 6.8 | - | - | mA |
| **Overtemperature protection** | | | | | | |
| $T_{otp}$ | overtemperature protection trip | | 120 | 135 | 150 | °C |

[1] Covered by correlating measurement.
[2] TEA2016AAT MTP programming (OVP-DRAINPFC protection delay): infinite.
[3] As the minimum limit determines the application design, the maximum limit is not relevant.

# 12 Application information

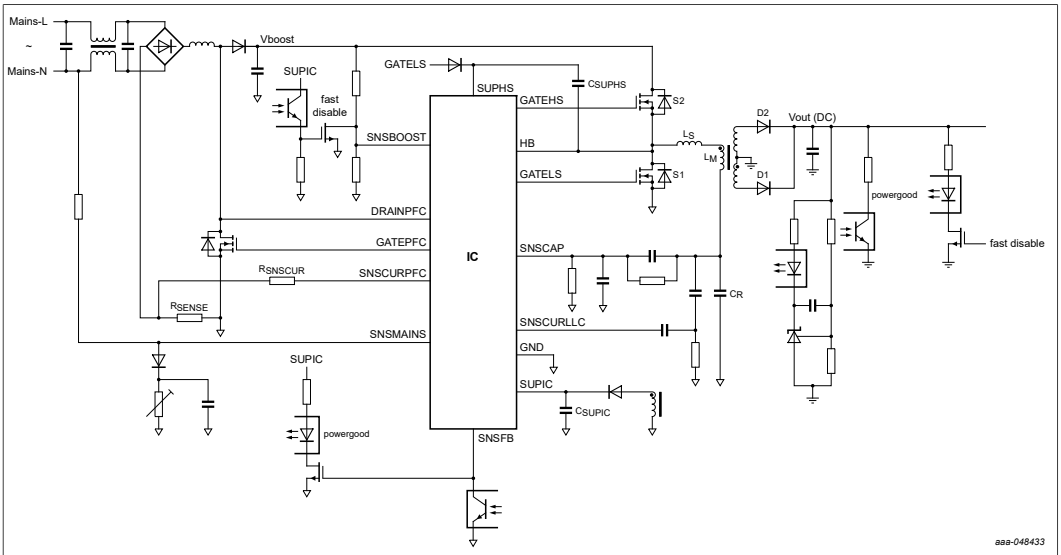
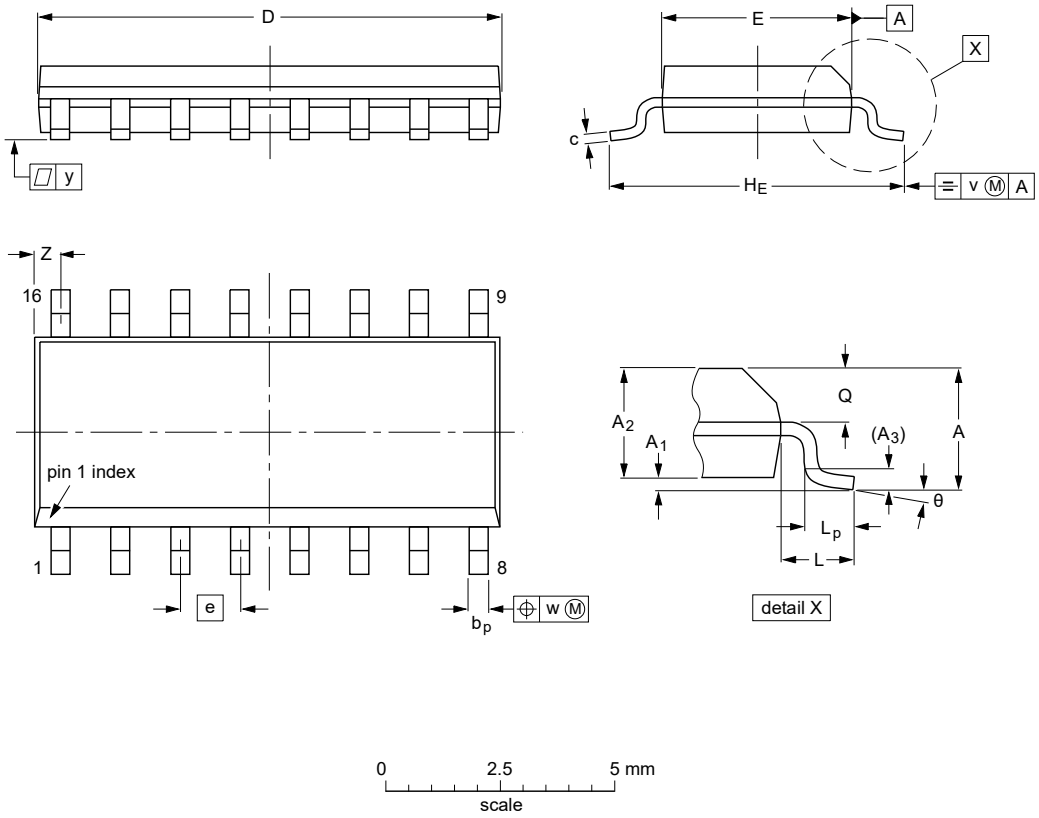



**Figure 25. TEA2016AAT application diagram**

## 13 Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Figure 26. Package outline SOT109-1 (SO16)**

# 14 Appendix: Parameter settings

A table containing the Ringo parameter settings/IC parameter settings is available in the TEA2016AAT/2 data sheet addendum. The data sheet addendum can be requested from NXP Semiconductors.

# 15 Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TEA2016AAT_2 v.1 | 20230215 | Product data sheet | - | - |

# 16 Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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## 16.4 Trademarks

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