TDA8029

Low power single card reader

Rev. 03 — 22 February 2005 Product data sheet

1. General description

The TDA8029 is a complete one chip, low cost, low power, robust smart card reader. Its different power reduction modes and its wide supply voltage range allow its use in portable equipment. Due to specific versatile hardware, a small embedded software program allows the control of most cards available in the market. The control from the host may be done through a standard serial interface.

The TDA8029 may be delivered with standard embedded software, or be masked with specific customer code. For details on software development and on available tools, please refer to application notes *"AN01009"* and *"AN10134"* for the TDA8029HL/C1. For standard embedded software, please refer to *"AN10206"* for the TDA8029HL/C2.

2. Features

- 80C51 core with 16 kB ROM, 256 byte RAM and 512 byte XRAM
- Specific ISO7816 UART, accessible with MOVX instructions for automatic convention processing, variable baud rate, error management at character level for T = 0 and T = 1 protocols, extra guard time, etc.
- Specific versatile 24-bit Elementary Time Unit (ETU) counter for timing processing during Answer To Reset (ATR) and for T = 1 protocol
- V_{CC} generation with controlled rise and fall times:
  - 5 V ± 5 %, maximum current 65 mA
  - 3 V ± 5 %, maximum current 50 mA; maximum current 65 mA if V_{DD} > 3 V
  - 1.8 V ± 5 %, maximum current 30 mA
- Card clock generation up to 20 MHz with three times synchronous frequency doubling (f_{XTAL}, $\frac{1}{2}f_{XTAL}$, $\frac{1}{4}f_{XTAL}$ and $\frac{1}{8}f_{XTAL}$)
- Card clock stop HIGH or LOW or 1.25 MHz from an integrated oscillator for card power reduction modes
- Automatic activation and deactivation sequences through an independent sequencer
- Supports asynchronous protocols T = 0 and T = 1 in accordance with:
  - *ISO 7816* and *EMV 3.1.1* (TDA8029HL/C1 and TDA8029HL/C2)
  - *ISO 7816* and *EMV 2000* (TDA8029HL/C2).
- 1 to 8 characters FIFO in reception mode
- Parity error counter in reception mode and in transmission mode with automatic retransmission
- Versatile 24-bit time-out counter for ATR and waiting times processing
- Specific ETU counter for Block Guard Time (BGT) (22 ETU in T = 1 and 16 ETU in T = 0)

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- Minimum delay between two characters in reception mode:
  - In protocol T = 0:
    12 ETU (TDA8029HL/C1)
    11.8 ETU (TDA8029HL/C2).
  - In protocol T = 1:
    11 ETU (TDA8029HL/C1)
    10.8 ETU (TDA8029HL/C2).
- Supports synchronous cards which do not use C4/C8
- Current limitations on card contacts
- Supply supervisor for power-on/off reset and spikes killing
- DC-to-DC converter (supply voltage from 2.7 to 6 V), doubler, tripler or follower according to V_{CC} and V_{DD}
- Shut-down input for very low power consumption
- Enhanced ESD protection on card contacts (6 kV minimum)
- Software library for easy integration
- Communication with the host through a standard full duplex serial link at programmable baud rates
- One external interrupt input and four general purpose I/Os.

3. Applications

- Portable card readers
- General purpose card readers
- EMV compliant card readers.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.7	-	6.0	V
		NDS conditions	3	-	6.0	V
V_{DCIN}	input voltage for the DC-to-DC converter		V_{DD}	-	6.0	V
$I_{DD(sd)}$	supply current in Shut-down mode	V_{DD} = 3.3 V	-	-	20	µA
$I_{DD(pd)}$	supply current in Power-down mode	V_{DD} = 3.3 V; card inactive; microcontroller in Power-down mode	-	-	110	µA
$I_{DD(sl)}$	supply current in Sleep mode	V_{DD} = 3.3 V; card active at V_{CC} = 5 V; clock stopped; microcontroller in Power-down mode; I_{CC} = 0 A	-	-	800	µA
$I_{DD(om)}$	supply current in operating mode	I_{CC} = 65 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 5 V card; V_{DD} = 2.7 V	-	-	250	mA

Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	card supply voltage	active mode; I_{CC} < 65 mA; 5 V card	4.75	5	5.25	V
		active mode; I_{CC} < 65 mA if V_{DD} > 3.0 V else I_{CC} < 50 mA; 3 V card	2.80	3	3.20	V
		active mode; I_{CC} < 30 mA; 1.8 V card	1.62	1.8	1.98	V
		active mode; current pulses of 40 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 5 V card	4.6	-	5.3	V
		active mode; current pulses of 40 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 3 V card	2.75	-	3.25	V
		active mode; current pulses of 12 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 1.8 V card	1.62	-	1.98	V
I_{CC}	card supply current	5 V card; V_{CC} = 0 V to 5 V	-	-	65	mA
		3 V card; V_{CC} = 0 V to 3 V; V_{DD} > 3.0 V	-	-	65	mA
		3 V card; V_{CC} = 0 V to 3 V; V_{DD} < 3.0 V	-	-	50	mA
		1.8 V card; V_{CC} = 0 V to 1.8 V;	-	-	30	mA
$I_{CC(det)}$	overload detection current		-	100	-	mA
SR_r, SR_f	rise and fall slew rate on V_{CC}	maximum load capacitor 300 nF	0.05	0.16	0.22	V/µs
t_{de}	deactivation sequence duration		-	-	100	µs
t_{act}	activation sequence duration		-	-	225	µs
f_{XTAL}	crystal frequency	V_{DD} = 5 V	4	-	27	MHz
		V_{DD} < 3 V	4	-	16	MHz
		external input	0	-	27	MHz
T_{amb}	ambient temperature		–40	-	+90	°C

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8029HL/C1	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
TDA8029HL/C2			

6. Block diagram

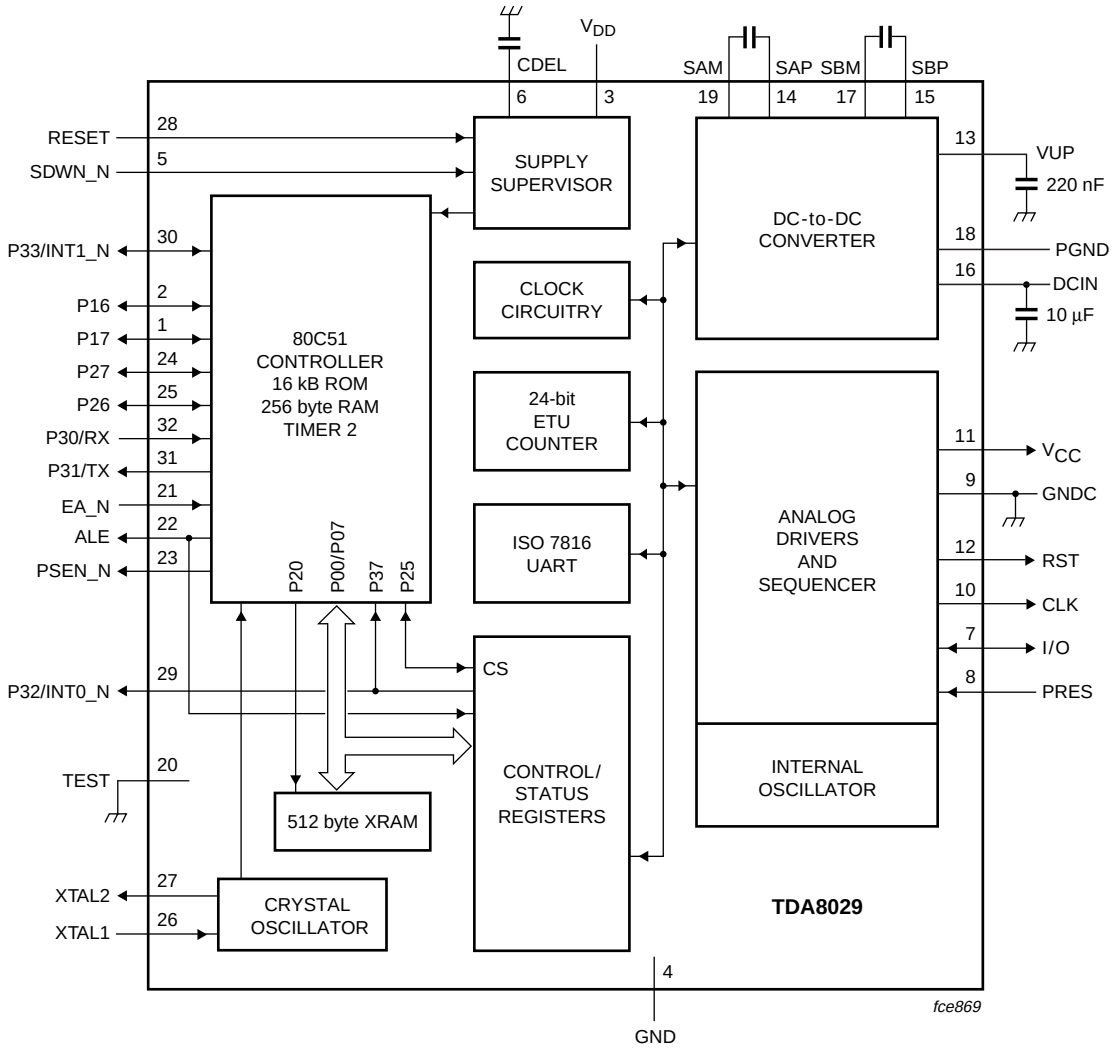


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

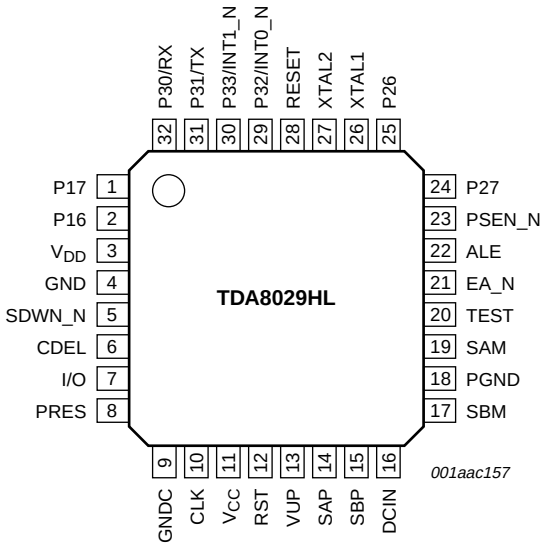


Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P17	1	I/O	general purpose I/O
P16	2	I/O	general purpose I/O
V_{DD}	3	power	supply voltage
GND	4	power	ground connection
SDWN_N	5	I	shut-down signal input (active LOW, no internal pull-up)
CDEL	6	I	connection for an external capacitor determining the power-on reset pulse width (typically 1 ms per 2 nF)
I/O	7	I/O	data input/output to/from the card (C7); 14 kΩ integrated pull-up resistor to V_{CC}
PRES	8	I	card presence detection contact (active HIGH); do not connect to any external pull-up or pull-down resistor; use with a normally open presence switch (see details in Section 8.13)
GNDC	9	power	card ground (C5); connect to GND in the application
CLK	10	O	clock to the card (C3)
V_{CC}	11	O	card supply voltage (C1)
RST	12	O	card reset (C2)
VUP	13	power	output of the DC-to-DC converter (low ESR 220 nF to PGND)

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
SAP	14	I/O	DC-to-DC converter capacitor connection (low ESR 220 nF between SAP and SAM)
SBP	15	I/O	DC-to-DC converter capacitor connection (low ESR 220 nF between SBP and SBM)
DCIN	16	I	power input for the DC-to-DC converter
SBM	17	I/O	DC-to-DC converter capacitor connection (low ESR 220 nF between SBP and SBM)
PGND	18	power	ground for the DC-to-DC converter
SAM	19	I/O	DC-to-DC converter capacitor connection (low ESR 220 nF between SAP and SAM)
TEST	20	I	used for test purpose; connect to GND in the application
EA_N	21	I	control signal for microcontroller; connect to V_{DD} in the application)
ALE	22	O	control signal for the microcontroller; leave open in the application)
PSEN_N	23	O	control signal for the microcontroller; leave open in the application)
P27	24	I/O	general purpose I/O
P26	25	I/O	general purpose I/O
XTAL1	26	I	external crystal connection or input for an external clock signal
XTAL2	27	O	external crystal connection; leave open if an external clock is applied to XTAL1
RESET	28	I	reset input from the host (active HIGH); no integrated pull-down resistor
P32/INT0_N	29	O	interrupt output for test purpose; leave open in the application
P33/INT1_N	30	I/O	external interrupt input, or general purpose I/O; may be left open if not used
P31/TX	31	O	transmission line for serial communication with the host
P30/RX	32	I	reception line for serial communication with the host

8. Functional description

Throughout this specification, it is assumed that the reader is aware of ISO7816 norm terminology.

8.1 Microcontroller

The embedded microcontroller is an 80C51FB with internal 16 kB ROM, 256 byte RAM and 512 byte XRAM. It has the same instruction set as the 80C51.

The controller is clocked by the frequency present on XTAL1.

The controller may be reset by an active HIGH signal on pin RESET, but it is also reset by the power-on reset signal generated by the voltage supervisor.

The external interrupt INT0_N is used by the ISO UART, by the analog drivers and the ETU counters. It must be left open in the application.

The second external interrupt INT1_N is available for the application.

A general description as well as added features are described in this chapter.

The added features to the 80C51 controller are similar to the 8XC51FB controller, except on the wake-up from Power-down mode, which is possible by a falling edge on INT0_N (Internally driven signalling card reader problems, see details in Section 8.10.1.2), on INT1_N or on RX due to the addition of an extra delay counter and enable configuration bits within register UCR2 (see detailed description in Section 8.10.3.2). For any further information please refer to the published specification of the 8XC51FB in *"Data Handbook IC20; 80C51-Based 8-bit Microcontrollers"*.

The controller has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability up to 64 kB, it can be expanded using standard TTL-compatible memories and logic.

Additional features of the controller are:

- 80C51 central processing unit
- Full static operation
- Security bits: ROM - 2 bits
- Encryption array of 64 bits
- 4-level priority structure
- 6 interrupt sources
- Full-duplex enhanced UART with framing error detection and automatic address recognition
- Power control modes; clock can be stopped and resumed, Idle mode and Power-down mode
- Wake-up from power-down by falling edge on INT0_N, INT1_N and RX with an embedded delay counter
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI by inhibit ALE.

Table 4 gives a list of main features to get a better understanding of the differences between a standard 80C51, an 8XC51FB and the embedded controller in the TDA8029.

Table 4: Principal blocks in 80C51, 8XC51FB and TDA8029

Feature	80C51	8XC51FB	TDA8029
ROM	4 kB	16 kB	16 kB
RAM	128 byte	256 byte	256 byte
ERAM (MOVX)	no	256 byte	512 byte
PCA	no	yes	no

Table 4: Principal blocks in 80C51, 8XC51FB and TDA8029

Feature	80C51	8XC51FB	TDA8029
WDT	no	yes	no
T0	yes	yes	yes
T1	yes	yes	yes
T2	no	yes	yes
		lowest interrupt priority-vector at 002BH	lowest interrupt priority-vector at 002BH
4 level priority interrupt	no	yes	yes
enhanced UART	no	yes	yes
delay counter	no	no	yes

Table 5: Embedded C51 controller special function registers

Symbol	Description	Addr (hex)	Bit address, symbol or alternative port function								Reset value (binary)
ACC [1]	accumulator	E0	E7	E6	E5	E4	E3	E2	E1	E0	0000 0000
AUXR [2]	auxiliary	8E	-	-	-	-	-	-	EXTRAM	AO	xxxx xx00
AUXR1 [2]	auxiliary	A2	-	-		LPEP	GF	0	-	DPS	xxx0 00x0
B [1]	B register	F0	F7	F6	F5	F4	F3	F2	F1	F0	0000 0000
DPH	data pointer high	83	-	-	-	-	-	-	-	-	0000 0000
DPL	data pointer low	82	-	-	-	-	-	-	-	-	0000 0000
IE [1]	interrupt enable	A8	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x00 0000
			AF	AE	AD	AC	AB	AA	A9	A8	
IP [1]	interrupt priority	B8	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx00 0000
			BF	BE	BD	BC	BB	BA	B9	B8	
IPH [2]	interrupt priority high	B7	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx00 0000
P0 [1]	port 0	80	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	1111 1111
			87	86	85	84	83	82	81	80	
P1 [1]	port 1	90	-	-	-	-	-	-	T2EX	T2	1111 1111
			97	96	95	94	93	92	91	90	
P2 [1]	Port 2	A0	A15	A14	A13	A12	A11	A10	A9	A8	1111 1111
			A7	A6	A5	A4	A3	A2	A1	A0	
P3 [1]	Port 3	B0	$\overline{RD}$	$\overline{WR}$	T1	T0	INT0_N	INT1_N	TxD	RxD	1111 1111
			B7	B6	B5	B4	B3	B2	B1	B0	
PCON [2] [3]	power control	87	SMOD1	SMOD0	-	POF [4]	GF1	GF0	PD	IDL	00xx 0000
PSW [1]	program status word	D0	CY	AC	F0	RS1	RS0	OV	-	P	0000 00x0
			D7	D6	D5	D4	D3	D2	D1	D0	
RACAP2H [2]	timer 2 capture high	CB	-	-	-	-	-	-	-	-	0000 0000

Table 5: Embedded C51 controller special function registers *...continued*

Symbol	Description	Addr (hex)	Bit address, symbol or alternative port function								Reset value (binary)
RACAP2L [2]	timer 2 capture low	CA	-	-	-	-	-	-	-	-	0000 0000
SADDR [2]	slave address	A9	-	-	-	-	-	-	-	-	0000 0000
SADEN [2]	slave address mask	B9	-	-	-	-	-	-	-	-	0000 0000
SBUF	serial data buffer	99	-	-	-	-	-	-	-	-	xxxx xxxx
SCON [1]	serial control	98	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000
			9F	9E	9D	9C	9B	9A	99	98	
SP	stack pointer	81									0000 0111
TCON [1]	timer control	88	TF1	TR1	TF0	TE0	IE1	IT1	IE0	IT0	0000 0000
			8F	8E	8D	8C	8B	8A	89	88	
T2CON [1]	timer 2 control	C8	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	0000 0000
			CF	CE	CD	CC	CB	CA	C9	C8	
T2MOD [2]	timer 2 mode control	C9	-	-	-	-	-	-	T2OE	DCEN	xxxx xx00
TH0	timer high 0	8C	-	-	-	-	-	-	-	-	0000 0000
TH1	timer high 1	8D	-	-	-	-	-	-	-	-	0000 0000
TH2 [2]	timer high 2	CD	-	-	-	-	-	-	-	-	0000 0000
TL0	timer low 0	8A	-	-	-	-	-	-	-	-	0000 0000
TL1	timer low 1	8B	-	-	-	-	-	-	-	-	0000 0000
TL2 [2]	timer low 2	CC	-	-	-	-	-	-	-	-	0000 0000
TMOD	timer mode	89	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	0000 0000

[1] SFRs are bit addressable.

[2] SFRs are modified from or added to the 80C51 SFRs.

[3] RESET value depends on reset source.

[4] Bit will not be affected by RESET.

8.1.1 Port characteristics

Port 0 (P0.7 to P0.0): Port 0 is an open-drain, bidirectional I/O timer 2 generated commonly used baud rates port. Port 0 pins that have logic 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.

Port 1 (P1.7 to P1.0): Port 1 is an 8-bit bidirectional I/O-port with internal pull-ups. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally

pulled LOW will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during program memory verification. Alternate functions for port 1 include:

- T2 (P1.0): timer/counter 2 external count input/clock out (see programmable clock out)
- T2EX (P1.1): timer/counter 2 reload/capture/direction control.

Port 2 (P2.7 to P2.0): Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled LOW will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting logic 1s. During access to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some port 2 pins receive the high order address bits during EPROM programming and verification.

Port 3 (P3.7 to P3.3, P3.1 and P3.0): Port 3 is a 7-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled LOW will source current because of the pull-ups. Port 3 also serves the special features of the 80C51 family, as listed:

- RxD (P3.0): serial input port
- TxD (P3.1): serial output port
- $\overline{\text{INT0}}$ (P3.2): external interrupt 0 (pin INT0_N)
- $\overline{\text{INT1}}$ (P3.3): external interrupt 1 (pin INT1_N)
- T0 (P3.4): timer 0 external input
- T1 (P3.5): timer 1external input
- $\overline{\text{WR}}$ (P3.6): external data memory write strobe
- $\overline{\text{RD}}$ (P3.7): external data memory read strobe.

8.1.2 Oscillator characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum HIGH and LOW times specified must be observed.

8.1.3 Reset

The microcontroller is reset when the TDA8029 is reset, as described in Section 8.11.

8.1.4 Low power modes

This section describes the low power modes of the microcontroller. Please refer to Section 8.15 for additional information of the TDA8029 power reduction modes.

Stop clock mode: The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and special function registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power-down mode is suggested.

Idle mode: In the Idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the Idle mode is the last instruction executed in the normal operating mode before the Idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a Power-on reset.

Power-down mode: To save even more power, a Power-down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power-down is the last instruction executed.

Either a hardware reset, external interrupt or reception on RX can be used to exit from Power-down mode. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

With INT0_N, INT1_N or RX, the bits in register IE must be enabled. Within the INT0_N interrupt service routine, the controller has to read out the Hardware Status Register (HSR @ 0Fh) and/or the UART Status register (USR @ 0Eh) by means of MOVX-instructions in order to know the exact interrupt reason and to reset the interrupt source.

For enabling a wake up by INT1_N, the bit ENINT1 within UCR2 must be set.

For enabling a wake up by RX, the bits ENINT1 and ENRX within UCR2 must be set.

An integrated delay counter maintains internally INT0_N and INT1_N LOW long enough to allow the oscillator to restart properly, so a falling edge on pins RX, INT0_N and INT1_N is enough for awaking the whole circuit.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into power-down.

Table 6: External pin status during Idle and Power-down mode

Mode	Program memory	ALE	PSEN_N	Port 0	Port 1	Port 2	Port 3
Idle	internal	1	1	data	data	data	data
Idle	external	1	1	float	data	address	data
Power-down	internal	0	0	data	data	data	data
Power-down	external	0	0	float	data	data	data

8.2 Timer 2 operation

Timer 2 is a 16-bit timer and counter which can operate as either an event timer or an event counter, as selected by bit C/$\overline{T2}$ in the special function register T2CON. Timer 2 has three operating modes: capture, auto-reload (up- or down counting), and baud rate generator, which are selected by bits in register T2CON.

8.2.1 Timer/counter 2 control register (T2CON)

Table 7: T2CON - timer/counter 2 control register (address C8h) bit allocation

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 8: T2CON - timer/counter 2 control register (address C8h) bit description

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
6	EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
5	RCLK	Receive clock flag. When set, causes the serial port to use timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes timer 1 overflows to be used for the receive clock.
4	TCLK	Transmit clock flag. When set, causes the serial port to use timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if timer 2 is not being used to clock the serial port. EXEN2 = 0 causes timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for timer 2. TR2 = 1 starts the timer.
1	C/$\overline{T2}$	Counter or timer select timer 2.
		0 = internal timer ($^1/_{12}f_{XTAL1}$)
		1 = external event counter (falling edge triggered).
0	CP/$\overline{RL2}$	Capture or reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on timer 2 overflow.

Table 9: Timer 2 operating modes

Mode	RCLK and TCLK	CP/$\overline{RL2}$	TR2
16-bit auto-reload	0	0	1
Baud-rate generator	1	X	1
Off	X	X	0

8.2.2 Timer/counter 2 mode control register (T2MOD)

Table 10: T2MOD - timer/counter 2 mode control register (address C9h) bit allocation

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Table 11: T2MOD - timer/counter 2 mode control register (address C9h) bit description

Bit	Symbol	Description
7 to 2	-	Not implemented. Reserved for future use.
1	T2OE	Timer 2 output enable.
0	DCEN	Down counter enable. When set, allows timer 2 to be configured as up- or down-counter.

[1] Do not write logic 1s to reserved bits. These bits may be used in future 80C51 family products to invoke new features. In that case, the reset or inactive value of the new bit will be logic 0, and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.2.3 Auto-reload mode (up- or down-counter)

In the 16-bit auto-reload mode, timer 2 can be configured as either a timer or counter (bit C/$\overline{T2}$ in register T2CON) and programmed to count up or down. The counting direction is determined by bit DCEN (down-counter enable) which is located in the T2MOD register. When reset, DCEN = 0 and timer 2 will default to counting up. If DCEN = 1, timer 2 can count up or down depending on the value of T2EX.

When DCEN = 0, timer 2 will count up automatically. In this mode there are two options selected by bit EXEN2 in register T2CON. If EXEN2 = 0, then timer 2 counts up to 0FFFFh and sets the TF2 overflow flag upon overflow. This causes the timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software. If EXEN2 = 1, then a 16-bit reload can be triggered either by an overflow or by a HIGH to LOW transition at controller input T2EX. This transition also sets the EXF2 bit. The timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are logic 1. See Figure 3 for an overview.

DCEN = 1 enables timer 2 to count up- or down. This mode allows T2EX to control the direction of count. When a HIGH level is applied at T2EX timer 2 will count up. Timer 2 will overflow at 0FFFFh and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2. When a LOW level is applied at T2EX this causes timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 overflow flag and causes 0FFFFh to be reloaded into the timer registers TL2 and TH2. See Figure 4 for an overview.

The external flag EXF2 toggles when timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

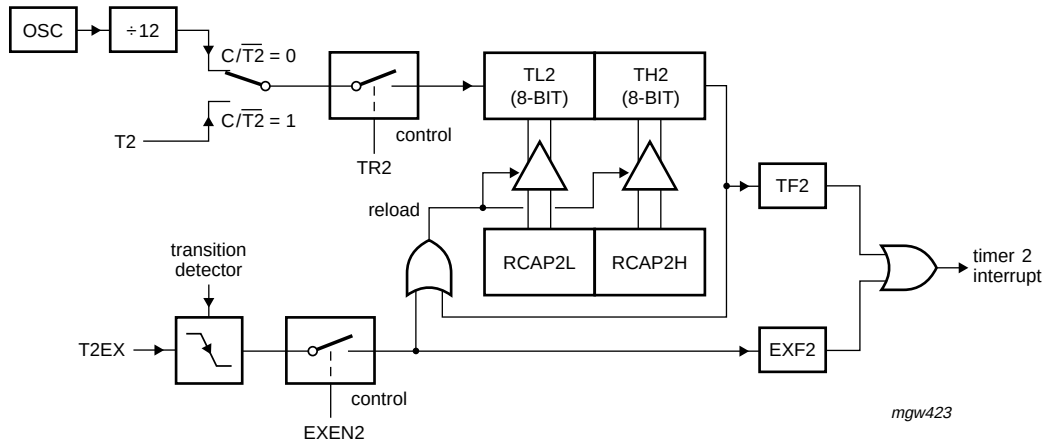


Fig 3. Timer 2 in auto-reload mode with DCEN = 0

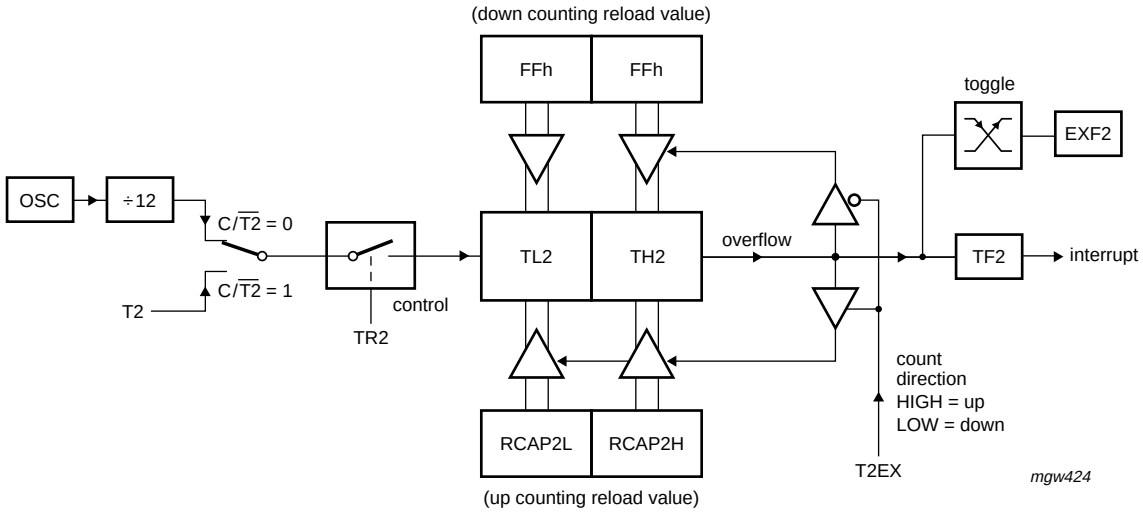


Fig 4. Timer 2 in auto-reload mode with DCEN = 1

8.2.4 Baud rate generator mode

Bits TCLK and/or RCLK in register T2CON allow the serial port transmit and receive baud rates to be derived from either timer 1 or timer 2. When TCLK = 0, timer 1 is used as the serial port transmit baud rate generator. When TCLK = 1, timer 2 is used. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates, one generated by timer 1, the other by timer 2.

The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by the overflow rate of timer 2, given by Equation 1:

$$Baud\ rate = \frac{Timer\ 2\ overflow\ rate}{16} \quad (1)$$

The timer can be configured for either timer or counter operation. In many applications, it is configured for timer operation ($C/\overline{T2} = 0$). Timer operation is different for timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e. $^1/_{12}$ f_{osc}). As a baud rate generator, it increments every state time (i.e. $^1/_2 f_{osc}$). Thus the modes 1 and 3 baud rate formula is as Equation 2:

$$Baud\ rate = \frac{Oscillator\ frequency}{32 \times [65536 - (RCAP2H, RCAP2L)]} \quad (2)$$

Where (RCAP2H, RCAP2L) is the contents of RCAP2H and RCAP2L registers taken as a 16-bit unsigned integer.

The timer 2 as a baud rate generator is valid only if RCLK = 1 and/or TCLK = 1 in the T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the timer 2 interrupt does not have to be disabled when timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable) flag is set, a HIGH to LOW transition on T2EX (timer/counter 2 trigger input) will set the EXF2 (T2 external) flag but will not cause a reload from (RCAP2H and RCAP2L) to (TH2 and TL2). Therefore, when timer 2 is used as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When timer 2 is in the baud rate generator mode, never try to read or write TH2 and TL2. As a baud rate generator, timer 2 is incremented every state time ($^1/_2 f_{osc}$) or asynchronously from controller I/O T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the timer 2 or RCAP2 registers. See Figure 5 for an overview.

Table 12: Timer 2 generated commonly used baud rates

Baud rate (Bd)	Crystal oscillator frequency (MHz)	Timer	
		RCAP2H (hex)	RCAP2L (hex)
375k	12	FF	FF
9.6k	12	FF	D9
2.8k	12	FF	B2
2.4k	12	FF	64
1.2k	12	FE	C8
300	12	FB	1E
110	12	F2	AF
300	6	FD	8F
110	6	F9	57

Summary of baud rate equations: Timer 2 is in baud rate generating mode. If timer 2 is being clocked through T2 (P1.0) the baud rate is:

$$Baud\ rate = \frac{Timer\ 2\ overflow\ rate}{16} \quad (3)$$

If timer 2 is being clocked internally, the baud rate is:

$$Baud\ rate = \frac{Oscillator\ frequency}{32 \times [65536 - (RCAP2H, RCAP2L)]} \quad (4)$$

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \frac{f_{osc}}{32 \times baud\ rate} \quad (5)$$

where f_{osc} = oscillator frequency.

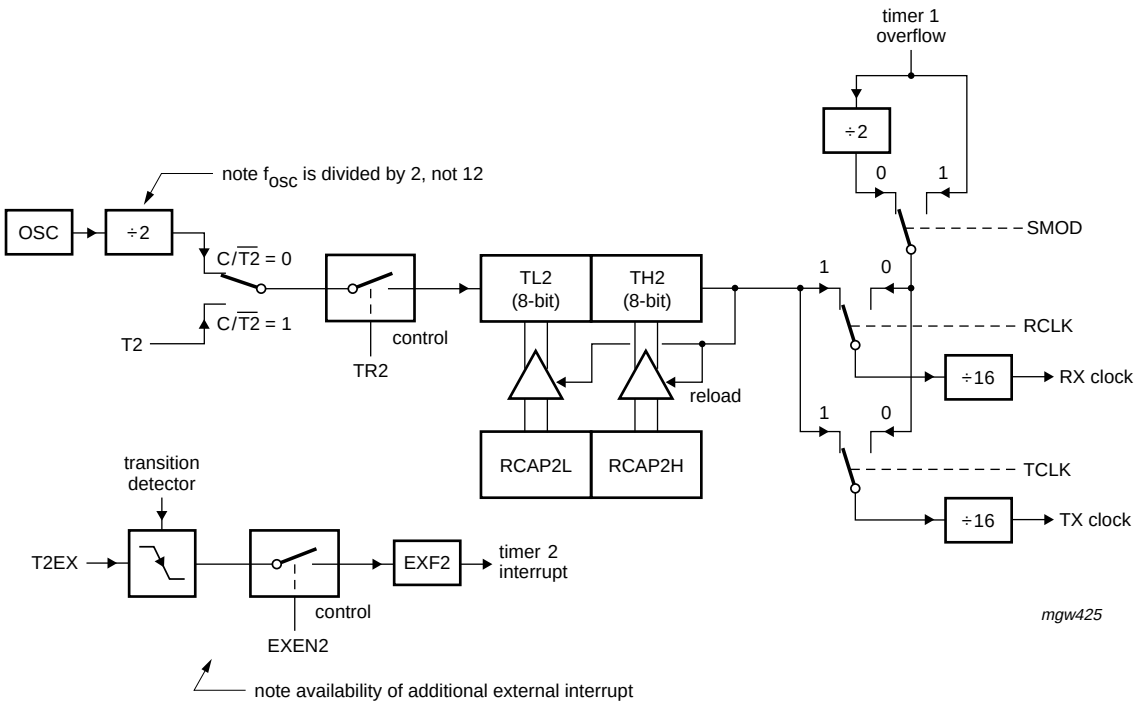


Fig 5. Timer 2 in baud rate generator mode

8.2.5 Timer/counter 2 set-up

Except for the baud rate generator mode, the values given in Table 13 for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on.

Table 13: Timer 2 as a timer

Mode	T2CON	
	Internal control (hex) [1]	External control (hex) [2]
16-bit auto-reload	00	08
Baud rate generator receive and transmit same baud rate	34	36
Receive only	24	26
Transmit only	14	16

[1] Capture/reload occurs only on timer/counter overflow.

[2] Capture/reload on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when timer 2 is used in the baud rate generator mode.

Table 14: Timer 2 as a counter

Mode	T2MOD	
	Internal control (hex) [1]	External control (hex) [2]
16-bit	02	04
Auto-reload	03	0B

[1] Capture/reload occurs only on timer/counter overflow.

[2] Capture/reload on timer/counter overflow and a HIGH-to-LOW transition on T2EX (P1.1) pin except when timer 2 is used in the baud rate generator mode.

8.3 Enhanced UART

The UART operates in all of the usual modes that are described in the first section of "*Data Handbook IC20, 80C51-based 8-bit microcontrollers*". In addition the UART can perform framing error detection by looking for missing stop bits and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detection the UART looks for missing stop bits in the communication. A missing bit will set the bit FE or bit 7 in the SCON register. Bit FE is shared with bit SM0. The function of SCON bit 7 is determined by bit 6 in register PCON (bit SMOD0). If SMOD0 is set then bit 7 of register SCON functions as FE and as SM0 when SMOD0 is cleared. When used as FE this bit can only be cleared by software.

8.3.1 Serial port control register (SCON)

Table 15: SCON - serial port control register (address 98h) bit allocation

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Table 16: SCON - serial port control register (address 98h) bit description

Bit	Symbol	Description
7	SM0/FE	The function of this bit is determined by SMOD0, bit 6 of register PCON. If SMOD0 is set then this bit functions as FE. This bit functions as SM0 when SMOD0 is reset. When used as FE, this bit can only be cleared by software.
		SM0: Serial port mode bit 0. See Table 17.
		FE: Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected; see Figure 6. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit in register PCON must be set to enable access to FE.
6	SM1	Serial port mode bit 1. See Table 17
5	SM2	Serial port mode bit 2. Enables the automatic address recognition feature in modes 2 or 3. If SM2 = 1, bit RI will not be set unless the received 9th data bit (RB8) is logic 1; indicating an address and the received byte is a given or broadcast address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a given or broadcast address. In mode 0, SM2 should be logic 0.
4	REN	Enables serial reception. Set by software to enable reception. Cleared by software to disable reception.
3	TB8	The 9th data bit transmitted in modes 2 and 3. Set or cleared by software as desired. In mode 0, TB8 is not used.
2	RB8	The 9th data bit received in modes 2 and 3. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except if SM2 = 1, as described for SM2). Must be cleared by software.

Table 17: Enhanced UART Modes

SM0	SM1	MODE	DESCRIPTION	BAUD-RATE
0	0	0	shift register	$^1/_{12}f_{XTAL1}$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$^1/_{32}$ or $^1/_{64}f_{XTAL1}$
1	1	3	9-bit UART	variable

8.3.2 Automatic address recognition

Automatic address recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in register SCON. In the 9-bit UART modes (modes 2 and 3), the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘given’ address or the ‘broadcast’ address. The 9-bit mode requires that the 9th information bit is a logic 1 to indicate that the received information is an address and not data. Figure 7 gives a summary.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a given or a broadcast address.

Mode 0 is the shift register mode and SM2 is ignored.

Using the automatic address recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Two special function registers are used to define the slave addresses, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are ‘don’t cares’. The SADEN mask can be logically AND-ed with the SADDR to create the given address which the master will use for addressing each of the slaves. Use of the given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme.

Table 18: Slave 0 address definition; example 1

Register	Value (binary)
SADDR	1100 0000
SADEN	1111 1101
Given	1100 00X0

Table 19: Slave 1 address definition; example 1

Register	Value (binary)
SADDR	1100 0000
SADEN	1111 1110
Given	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires that bit 0 = 0 and ignores bit 1. Slave 1 requires that bit 1 = 0 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires bit 1 = 0. A unique address for slave 1 would be 1100 0001 since bit 0 = 1 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0.

Table 20: Slave 0 address definition; example 2

Register	Value (binary)
SADDR	1100 0000
SADEN	1111 1001
Given	1100 0XX0

Table 21: Slave 1 address definition; example 2

Register	Value (binary)
SADDR	1110 0000
SADEN	1111 1010
Given	1110 0X0X

Table 22: Slave 2 address definition; example 2

Register	Value (binary)
SADDR	1110 0000
SADEN	1111 1100
Given	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select slaves 0 and 1 and exclude slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The broadcast address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FFh.

Upon reset SADDR (SFR address 0A9h) and SADEN (SFR address 0B9h) are leaded with 0s. This produces a given address of all 'don't cares' as well as a broadcast address of all 'don't cares'. This effectively disables the automatic addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

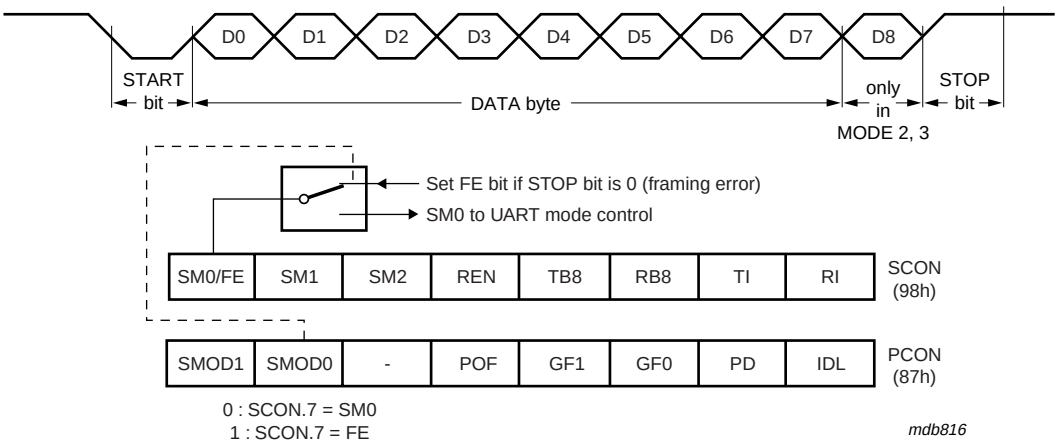
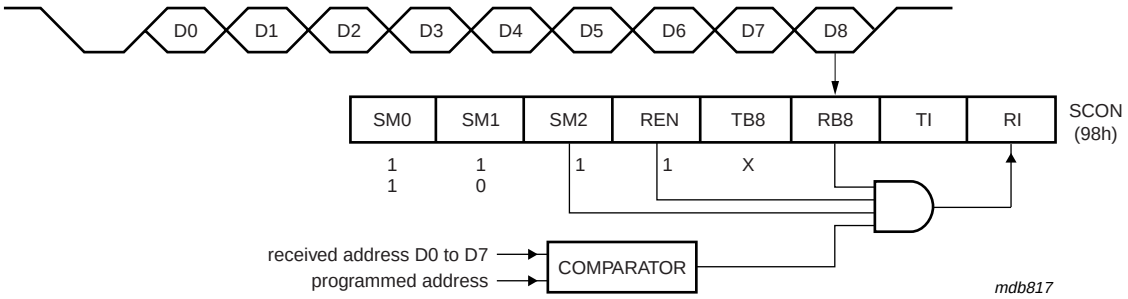


Fig 6. UART framing error detection



UART modes 2 or 3 and SM2 = 1: there is an interrupt if REN = 1, RB8 = 1 and received address is equal to programmed address.

When own address is received, reset SM2 to receive the data bytes. When all data bytes are received, set SM2 to wait for the next address.

Fig 7. UART multiprocessor communication, automatic address recognition

8.4 Interrupt priority structure

The TDA8029 has a 6-source 4-level interrupt structure.

There are three SFRs associated with the 4-level interrupt: IE, IP and IPH. The Interrupt Priority High (IPH) register implements the 4-level interrupt structure. The IPH is located at SFR address B7h.

The function of the IPH is simple and when combined with the IP determines the priority of each interrupt. The priority of each interrupt is determined as shown in Table 23.

Table 23: Priority bits

IPH bit n	IP bit n	Interrupt priority level
0	0	level 0 (lowest priority)
0	1	level 1
1	0	level 2
1	1	level 3 (highest priority)

Table 24: Interrupt Table

Source	Polling priority	Request bits	Hardware clear	Vector address (hex)
X0	1	IE0	N [1], Y [2]	03
T0	2	TF0	Y	0B
X1	3	IE1	N [1], Y [2]	13
T1	4	TF1	Y	1B
SP	5	RI, TI	N	23
T2	6	TF2, EXF2	N	2B

[1] Level activated.

[2] Transition activated.

8.4.1 Interrupt enable register (IE)

Table 25: IE - interrupt enable register (address A8h) bit allocation

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Table 26: IE - interrupt enable register (address A8h) bit description [1]

Bit	Symbol	Description
7	EA	Global disable. If EA = 0, all interrupts are disabled; If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
6	-	Not implemented. Reserved for future use [2]
5	ET2	Timer 2 interrupt enable. ET2 = 1 enables the interrupt; ET2 = 0 disables the interrupt.
4	ES	Serial port interrupt enable. ES = 1 enables the interrupt; ES = 0 disables the interrupt.
3	ET1	Timer 1 interrupt enable. ET1 = 1 enables the interrupt; ET1 = 0 disables the interrupt.
2	EX1	External interrupt 1 enable. EX1 = 1 enables the interrupt; EX1 = 0 disables the interrupt.
1	ET0	Timer 0 interrupt enable. ET0 = 1 enables the interrupt; ET0 = 0 disables the interrupt.
0	EX0	External interrupt 0 enable. EX0 = 1 enables the interrupt; EX0 = 0 disables the interrupt.

[1] Details on interaction with the UART behavior in Power-down mode are described in Section 8.15.

[2] Do not write logic 1s to reserved bits. These bits may be used in future 80C51 family products to invoke new features. In that case, the reset or inactive value of the new bit will be logic 0, and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.4.2 Interrupt priority register (IP)

Table 27: IP - interrupt priority register (address B8h) bit allocation

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Table 28: IP - interrupt priority register (address B8h) bit description

Each interrupt priority is assigned with a bit in register IP and a bit in register IPH, see Table 23.

Bit	Symbol	Description
7 and 6	-	Not implemented. Reserved for future use [1]
5	PT2	Timer 2 interrupt priority.
4	PS	Serial port interrupt priority.
3	PT1	Timer 1 interrupt priority.
2	PX1	External interrupt 1 priority.
1	PT0	Timer 0 interrupt priority.
0	PX0	External interrupt 0 priority.

[1] Do not write logic 1s to reserved bits. These bits may be used in future 80C51 family products to invoke new features. In that case, the reset or inactive value of the new bit will be logic 0, and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.4.3 Interrupt priority high register (IPH)

Table 29: IPH - interrupt priority high register (address B7h) bit allocation

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 30: IPH - interrupt priority high register (address B7h) bit description

Each interrupt priority is assigned with a bit in register IP and a bit in register IPH, see Table 23.

Bit	Symbol	Description
7 and 6	-	Not implemented. Reserved for future use [1]
5	PT2H	Timer 2 interrupt priority.
4	PSH	Serial port interrupt prioritizes.
3	PT1H	Timer 1 interrupt priority.
2	PX1H	External interrupt 1 priority.
1	PT0H	Timer 0 interrupt priority.
0	PX0H	External interrupt 0 priority.

[1] Do not write logic 1s to reserved bits. These bits may be used in future 80C51 family products to invoke new features. In that case, the reset or inactive value of the new bit will be logic 0, and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.5 Dual DPTR

The dual DPTR structure is a way by which the TDA8029 will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS (bit 0 of the AUXR1 register) that allows the program code to switch between them.

The DPS bit should be saved by software when switching between DPTR0 and DPTR1.

The GF bit (bit 2 in register AUXR1) is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a logic 0. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF or LPEP bits.

The instructions that refer to DPTR refer to the data pointer that is currently selected using bit 0 of the AUXR1 register. The six instructions that use the DPTR are listed in Table 31 and an illustration is given in Figure 8.

Table 31: DPTR Instructions

Instruction	Comment
INC DPTR	increments the data pointer by 1
MOV DPTR, #data 16	loads the DPTR with a 16-bit constant
MOV A, @A + DPTR	move code byte relative to DPTR to ACC
MOVX A, @DPTR	move external RAM (16-bit address) to ACC
MOVX @DPTR, A	move ACC to external RAM (16-bit address)
JMP @A + DPTR	jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs.

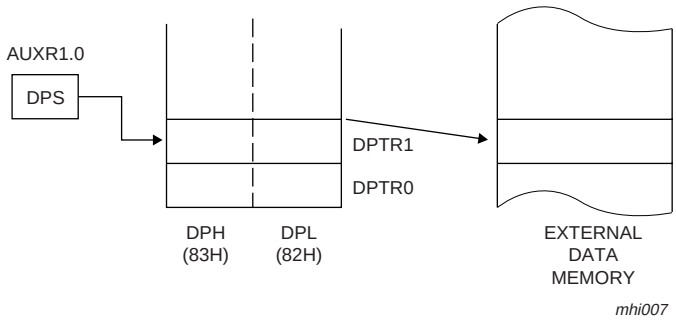


Fig 8. Dual DPTR

8.6 Expanded data RAM addressing

The TDA8029 has internal data memory that is mapped into four separate segments.

The four segments are:

1. The lower 128 byte of RAM (addresses 00h to 7Fh), which are directly and indirectly addressable.
2. The upper 128 byte of RAM (addresses 80h to FFh), which are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80h to FFh), which are directly addressable only.
4. The 512 byte expanded RAM (XRAM 00h to 1FFh) are indirectly accessed by move external instructions, MOVX, if the EXTRAM bit (bit 1 of register AUXR) is cleared.

The lower 128 byte can be accessed by either direct or indirect addressing. The upper 128 byte can be accessed by indirect addressing only. The upper 128 byte occupy the same address space as the SFRs. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7Fh, the CPU knows whether the access is to the upper 128 byte of data RAM or to the SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example: MOV A0h, #data accesses the SFR at location 0A0h (which is register P2).

Instructions that use indirect addressing access the upper 128 byte of data RAM. For example: MOV @R0, #data where R0 contains 0A0h, accesses the data byte at address 0A0h, rather than P2 (whose address is 0A0h).

The XRAM can be accessed by indirect addressing, with EXTRAM bit (register AUXR bit 1) cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 512 byte of external data memory.

When EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to XRAM will not affect ports P0, P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$). P2 is output during external addressing. For example: MOVX @R0, A where R0 contains 0A0h, access the EXTRAM at address 0A0h rather than external memory. An access to external data memory

locations higher than 1FFh (i.e., 0200h to FFFFh) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @Ri will provide an 8-bit address multiplexed with data on port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high order eight address bits (the contents of DPH) while port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 byte RAM (lower and upper RAM) internal data memory. The stack must not be located in the XRAM.

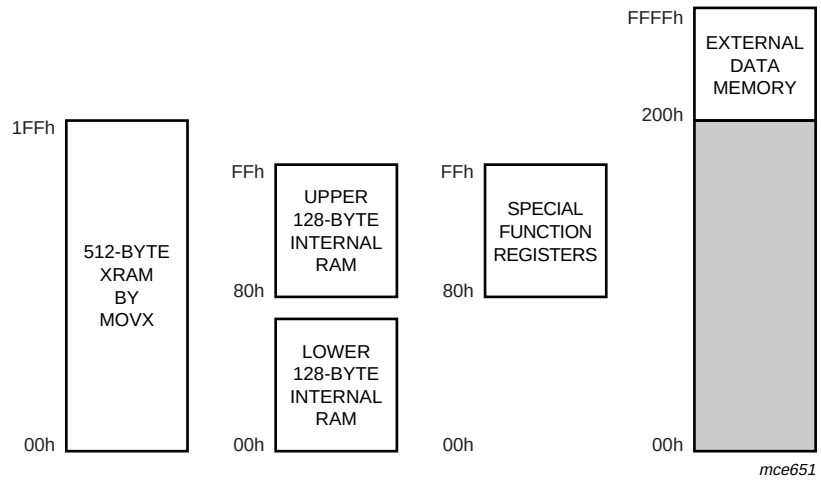


Fig 9. Internal and external data memory address space with EXTRAM = 0

8.6.1 Auxiliary register (AUXR)

Table 32: AUXR - auxiliary register (address 8Eh) bit allocation

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Table 33: AUXR - auxiliary register (address 8Eh) bit description

Bit	Symbol	Description
7 to 2	-	Not implemented. Reserved for future use [1]
1	EXTRAM	External RAM access. Internal or external RAM access using MOVX @Ri/@DPTR. If EXTRAM = 0, internal expanded RAM (0000h to 01FFh) access using MOVX @Ri/@DPTR; if EXTRAM = 1, external data memory access.
0	AO	ALE enable or disable. If AO = 0, ALE is emitted at a constant rate of $^1/_6 f_{XTAL}$; if AO = 1, ALE is active only during a MOVX or MOVC instruction.

[1] Do not write logic 1s to reserved bits. These bits may be used in future 80C51 family products to invoke new features. In that case, the reset or inactive value of the new bit will be logic 0, and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.7 Reduced EMI mode

When bit AO = 1 (bit 0 in the AUXR register), the ALE output is disabled.

8.8 Mask ROM devices

Security bits: With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption array: 64 byte of encryption array are initially unprogrammed (all 1s).

Table 34: Program security bits for TDA8029

Program lock bits [1]		Protection description
SB1	SB2	
no	no	no program security features enabled. If the encryption array is programmed, code verify will still be encrypted.
yes	no	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory
yes	yes	same as above, also verify is disabled

[1] Any other combination of the security bits is not defined.

8.9 ROM code submission for 16 kB ROM device TDA8029HL/C1

When submitting ROM code for 16 kB ROM devices, the following must be specified:

- 16 kB user ROM data
- 64 byte ROM encryption key
- ROM security bits.

8.10 Smart card reader control registers

The TDA8029 has one analog interface for five contacts cards. The data to or from the card are fed into an ISO UART.

The Card Select Register (CSR) contains a bit for resetting the ISO UART (logic 0 = active). This bit is reset after power-on, and must be set to logic 1 before starting any operation. It may be reset by software when necessary.

Dedicated registers allow to set the parameters of the ISO UART:

- Programmable Divider Register (PDR)
- Guard Time Register (GTR)
- UART Control Registers (UCR1 and UCR2)
- Clock Configuration Register (CCR).

The parameters of the ETU counters are set by:

- Time-Out Configuration register (TOC)
- Time-Out Registers (TOR1, TOR2 and TOR3).

The Power Control Register (PCR) is a dedicated register for controlling the power to the card.

When the specific parameters of the card have been programmed, the UART may be used with the following registers:

- UART Receive and Transmit Registers (URR and UTR)
- UART Status Register (USR)
- Mixed Status Register (MSR).

In reception mode, a FIFO of 1 to 8 characters may be used, and is configured with the FIFO Control Register (FCR). This register is also used for the automatic retransmission of NAKed characters in transmission mode.

The Hardware Status Register (HSR) gives the status of the supply voltage, the hardware protections, the SDWN request and the card movements.

USR and HSR give interrupts on INT0_N when some of their bits have been changed.

MSR does not give interrupts, and may be used in polling mode for some operations. For this use, the bit TBE/RBF within USR may be masked.

A 24-bit time-out counter may be started for giving an interrupt after a number of ETU programmed in registers TOR1, TOR2 and TOR3. It will help the controller for processing different real time tasks (ATR, WWT, BWT, etc.) mainly if controllers and card clock are asynchronous.

This counter is configured with register TOC, that may be used as a 24-bit or as a 16-bit + 8-bit counter. Each counter may be set for starting to count once data written, on detection of a start bit on I/O, or as auto-reload.

8.10.1 General registers

8.10.1.1 Card select register (CSR)

This register is used for resetting the ISO UART.

Table 35: CSR - card select register (address 0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	$\overline{RIU}$	-	-	-
Reset	0	0	0	0	0	0	0	0
Access	read and write							

Table 36: CSR - card select register (address 0h) bit description

Bit	Symbol	Description
7 to 4	-	Not used
1	$\overline{RIU}$	Reset ISO UART. If $\overline{RIU}$ = 0, this bit resets a large part of the UART registers to their initial value. Bit $\overline{RIU}$ must be reset to logic 0 for at least 10 ns duration before any activation. Bit $\overline{RIU}$ must be set to logic 1 by software before any action on the UART can take place.
2 to 0	-	Not used

8.10.1.2 Hardware status register (HSR)

This register gives the status of the chip after a hardware problem has been signalled or when pin SDWN_N has been activated.

When PRTL1, PRL1, PTL or SDWN is logic 1, then pin INT0_N is LOW. The bits having caused the interrupt are cleared when HSR is read (two f_{int} cycles after the rising edge of signal $\overline{RD}$).

In case of emergency deactivation by PRTL1, SUPL, PRL1 and PTL, bit START in the power control register is automatically reset by hardware.

Table 37: HSR - hardware status register (address Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SDWN	-	PRTL1	SUPL	-	PRL1	-	PTL
Reset	-	0	0	0	0	0	0	0
Access	read							

Table 38: HSR - hardware status register (address Fh) bit description

Bit	Symbol	Description
7	SDWN	Enter Shut-down mode. This bit is used for entering the Shut-down mode. SDWN is set when the SDWN_N pin is active (LOW). When the software reads the status, it must: • Deactivate the card if active • Set all ports to logic 1 (for minimizing the current consumption) • Inhibit the interrupts • Go to Power-down mode. The same must be done when the chip is powered-on with SDWN_N pin active. The only way to leave Shut-down mode is when pin SDWN_N is HIGH.
6	-	Not used.
5	PRTL1	Protection 1. PRTL1 = 1 when a fault has been detected on the card reader. PRTL1 is the OR of the protection on V_{CC} and on RST.
4	SUPL	Supervisor Latch. SUPL = 1 when the supervisor has been active. At power-on, or after a supply voltage dropout, then SUPL is set and INT0_N is LOW. INT0_N will return to HIGH at the end of the internal Power-on reset pulse defined by CDEL, except if pin SDWN_N was active during power-on. SUPL will be reset only after a status register read-out outside the Power-on reset pulse; see Figure 11. When leaving Shut-down mode, the same situation occurs.
3	-	Not used.
2	PRL1	Presence Latch. PRL1 = 1 when bit PR1 in the mixed status register has changed state.
1	-	Not used.
0	PTL	Overheat. PTL = 1 if an overheating has occurred.

8.10.1.3 Time-out registers (TOR1, TOR2 and TOR3)

Table 39: TOR1 - time-out register 1 (address 9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0
Reset	0	0	0	0	0	0	0	0
Access	write							

Table 40: TOR1 - time-out register 1 (address 9h) bit description

Bit	Symbol	Description
7 to 0	TOL[7:0]	The 8-bit value for the auto-reload counter or the lower 8-bits of the 24-bits counter.

Table 41: TOR2 - time-out register 2 (address Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8
Reset	0	0	0	0	0	0	0	0
Access	write							

Table 42: TOR2 - time-out register 2 (address Ah) bit description

Bit	Symbol	Description
7 to 0	TOL[15:8]	The lower 8-bits of the 16-bits counter or the middle 8-bits of the 24-bits counter.

Table 43: TOR3 - time-out register 3 (address Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16
Reset	0	0	0	0	0	0	0	0
Access	write							

Table 44: TOR3 - time-out register 3 (address Bh) bit description

Bit	Symbol	Description
7 to 0	TOL[23:16]	The upper 8-bits of the 16-bits counter or the upper 8-bits of the 24-bits counter.

8.10.1.4 Time-out configuration register (TOC)

The time-out counter is very useful for processing the clock counting during ATR, the Work Waiting Time (WWT) or the waiting times defined in protocol T = 1. It should be noted that the 200 and n_{max} clock counter (n_{max} = 384 for TDA8029HL/C1 and n_{max} = 368 for TDA8029HL/C2) used during ATR is done by hardware when the start session is set. Specific hardware controls the functionality of BGT in T = 1 and T = 0 protocols and a specific register is available for processing the extra guard time.

Writing to register TOC is not allowed as long as the card is not activated with a running clock.

Before restarting the 16-bit counter (counters 3 and 2) by writing 61h, 65h, 71h, 75h, F1h or F5h in the TOC register, or the 24-bit counter (counters 3, 2 and 1) by writing 68h or 7C in the TOC register, it is mandatory to stop them by writing 00h in the TOC register.

Detailed examples of how to use these specific timers can be found in application note *"AN01010"*.

Table 45: TOC - time-out configuration register (address 8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0
Reset	0	0	0	0	0	0	0	0
Access	read and write							

Table 46: TOC - time-out configuration register (address 8h) bit description

Bit	Symbol	Description
7 to 0	TOC[7:0]	Time-out counter configuration. The time-out configuration register is used for setting different configurations of the time-out counter as given in Table 47, all other configurations are undefined.

Table 47: Time-out counter configurations

TOC[7:0] (hex)	Operating mode
00	All counters are stopped.
05	Counters 2 and 3 are stopped; counter 1 continues to operate in auto-reload mode.
61	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in registers TOR3 and TOR2 is started after 61h is written in register TOC. When the terminal count is reached, an interrupt is given, and bit TO3 in register USR is set. The counter is stopped by writing 00h in register TOC, and should be stopped before reloading new values in registers TOR2 and TOR3.

Table 47: Time-out counter configurations *…continued*

TOC[7:0] (hex)	Operating mode
65	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of register TOR1 on the first start-bit (reception or transmission) detected on pin I/O after 65h is written in register TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of register TOR1 during a count. Counters 3 and 2 are wired as a single 16-bit counter and start counting the value in registers TOR3 and TOR2 when 65h is written in register TOC. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within register USR. Both counters are stopped when 00h is written in register TOC. Counters 3 and 2 shall be stopped by writing 05h in register TOC before reloading new values in registers TOR2 and TOR3.
68	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started after 68h is written in register TOC. The counter is stopped by writing 00h in register TOC. It is not allowed to change the content of registers TOR3, TOR2 and TOR1 within a count.
71	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. After writing this value, counting the value stored in registers TOR3 and TOR2 is started on the first start-bit detected on pin I/O (reception or transmission) and then on each subsequent start-bit. It is possible to change the content of registers TOR3 and TOR2 during a count, the current count will not be affected and the new count value will be taken into account at the next start-bit. The counter is stopped by writing 00h in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
75	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. After 75h is written in register TOC, counter 1 starts counting the content of register TOR1 on the first start-bit (reception or transmission) detected on pin I/O. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set and the counter automatically restarts the same count until it is stopped. Changing the content of register TOR1 during a count is not allowed. Counting the value stored in registers TOR3 and TOR2 is started on the first start-bit detected on pin I/O (reception or transmission) after 75h is written, and then on each subsequent start-bit. It is possible to change the content of registers TOR3 and TOR2 during a count, the current count will not be affected and the new count value will be taken into account at the next start-bit. The counter is stopped by writing 00h in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
7C	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started on the first start-bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent start-bit. It is possible to change the content of registers TOR3, TOR2 and TOR1 during a count. The current count will not be affected and the new count value will be taken into account at the next start-bit. The counter is stopped by writing 00h in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
85	Same as value 05h, except that all the counters will be stopped at the end of the 12th ETU following the first received start-bit detected after 85h has been written in register TOC.
E5	Same configuration as value 65h, except that counter 1 will be stopped at the end of the 12th ETU following the first start-bit detected after E5h has been written in register TOC.
F1	Same configuration as value 71h, except that the 16-bit counter will be stopped at the end of the 12th ETU following the first start-bit detected after F1h has been written in register TOC.
F5	Same configuration as value 75h, except the two counters will be stopped at the end of the 12th ETU following the first start-bit detected after F5h has been written in register TOC.

8.10.2 ISO UART registers

8.10.2.1 UART transmit register (UTR)

Table 48: UTR - UART transmit register (address Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0
Reset	0	0	0	0	0	0	0	0
Access	write							

Table 49: UTR - UART transmit register (address Dh) bit description

Bit	Symbol	Description
7 to 0	UT[7:0]	UART transmit bits. When the microcontroller wants to transmit a character to the card, it writes the data in direct convention in this register. The transmission: • Starts at the end of writing (on the rising edge of signal $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired • Starts at the end of the extra guard time if this one has not expired • Does not start if the transmission of the previous character is not completed • With a synchronous card (bit SAN within register UCR2 is set), only UT0 is relevant and is copied on pin I/O of the card.

8.10.2.2 UART receive register (URR)

Table 50: URR - UART receive register (address Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0
Reset	0	0	0	0	0	0	0	0
Access	read							

Table 51: URR - UART receive register (address Dh) bit description

Bit	Symbol	Description
7 to 0	UR[7:0]	UART receive bits. When the microcontroller wants to read data from the card, it reads it from this register in direct convention: • With a synchronous card, only UR0 is relevant and is a copy of the state of the selected card I/O • When needed, this register may be tied to a FIFO whose length ‘n’ is programmable between 1 and 8; if n > 1, then no interrupt is given until the FIFO is full and the controller may empty the FIFO when required • With a parity error: – In protocol T = 0, the received byte is not stored in the FIFO and the error counter is incremented. The error counter is programmable between 1 and 8. When the programmed number is reached, then bit PE is set in the status register USR and INT0_N falls LOW. The error counter must be reprogrammed to the desired value after its count has been reached – In protocol T = 1, the character is loaded in the FIFO and the bit PE is set to the programmed value in the parity error counter. • When the FIFO is full, then bit RBF in the status register USR is set. This bit is reset when at least one character has been read from URR • When the FIFO is empty, then bit FE is set in the status register USR as long as no character has been received.

8.10.2.3 Mixed status register (MSR)

This register relates the status of the card presence contact PR1, the BGT counter, the FIFO empty indication, the transmit/receive ready indicator TBE/RBF and the completion of clock switching to or from $\frac{1}{2}f_{int}$.

Table 52: MSR - mixed status register (address Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CLKSW	FE	BGT	-	-	PR1	-	TBE/RBF
Reset	-	1	0	-	-	-	-	-
Access	read							

Table 53: MSR - mixed status register (address Ch) bit description

Bit	Symbol	Description
7	CLKSW	Clock Switch. CLKSW is set when the TDA8029 has performed a required clock switch from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$ and is reset when the TDA8029 has performed a required clock switch from $\frac{1}{2}f_{int}$ to $\frac{1}{n}f_{XTAL}$. The application shall wait this bit before entering Power-down mode or restarting sending commands after leaving power-down (only needed when the clock is not stopped during power-down). This bit is also reset by $\overline{RIU}$ and at power-on. When the microcontroller wants to transmit a character to the card, it writes the data in direct convention to this register.
6	FE	FIFO Empty. FE is set when the reception FIFO is empty. It is reset when at least one character has been loaded in the FIFO.
5	BGT	Block Guard Time. In T = 1 protocol, the bit BGT is linked with a 22 ETU counter, which is started at every start-bit on pin I/O. If the count is finished before the next start-bit, BGT is set. This helps checking that the card has not answered before 22 ETU after the last transmitted character, or that the reader is not transmitting a character before 22 ETU after the last received character. In T = 0 protocol, the bit BGT is linked to a 16 ETU counter, which is started at every start-bit on I/O. If the count is finished before the next start-bit, then the bit BGT is set. This helps checking that the reader is not transmitting too early after the last received character.
4 and 3	-	Not used.
2	PR1	Presence 1. PR1 = 1 when the card is present.
1	-	Not used.
0	TBE/RBF	Transmit Buffer Empty / Receive Buffer Full. This bit is set when: • Changing from reception mode to transmission mode • A character has been transmitted by the UART (except when a character has been parity error free transmitted whilst LCT = 1) • The reception buffer is full. This bit is reset: • After power-on • When bit $\overline{RIU}$ in register CSR is reset • When a character has been written in register UTR • When the character has been read from register URR • When changing from transmission mode to reception mode.

8.10.2.4 FIFO control register (FCR)

Table 54: FCR - FIFO control register (address Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	PEC2	PEC1	PEC0	-	FL2	FL1	FL0
Reset	-	0	0	0	-	0	0	0
Access	write							

Table 55: FCR - FIFO control register (address Ch) bit description

Bit	Symbol	Description
7	-	Not used.
6 to 4	PEC[2:0]	Parity Error Counter. These bits determine the number of parity errors before setting bit PE in register USR and pulling INT0_N LOW. PEC[2:0] = 000 means that if only one parity error has occurred, bit PE is set; PEC[2:0] = 111 means that bit PE will be set after 8 parity errors. In protocol T = 0: • If a correct character is received before the programmed error number is reached, the error counter will be reset • If the programmed number of allowed parity errors is reached, bit PE in register USR will be set as long as the USR has not been read • If a transmitted character is NAKed by the card, then the TDA8029 will automatically retransmit it a number of times equal to the value programmed in PEC[2:0]. The character will be resent at 15 ETU. • In transmission mode, if PEC[2:0] = 000, then the automatic retransmission is invalidated. The character manually rewritten in register UTR will start at 13.5 ETU. In protocol T = 1: • The error counter has no action (bit PE is set at the first wrong received character).
3	-	Not used.
2 to 0	FL[2:0]	FIFO Length. These bits determine the depth of the FIFO: FL[2:0] = 000 means length 1, FL[2:0] = 111 means length 8.

8.10.2.5 UART status register (USR)

The UART Status Register (USR) is used by the microcontroller to monitor the activity of the ISO UART and that of the time-out counter. If any of the status bits FER, OVR, PE, EA, TO1, TO2 or TO3 are set, then signal INT0_N = LOW. The bit having caused the interrupt is reset 2 µs after the rising edge of signal $\overline{RD}$ during a read operation of register USR.

If bit TBE/RBF is set and if the mask bit DISTBE/RBF within register UCR2 is not set, then also signal INT0_N = LOW. Bit TBE/RBF is reset three clock cycles after data has been written in register UTR, or three clock cycles after data has been read from register URR, or when changing from transmission mode to reception mode.

If LCT mode is used for transmitting the last character, then bit TBE is not set at the end of the transmission.

Table 56: USR - UART status register (address Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF
Reset	0	0	0	0	0	0	0	0
Access	read							

Table 57: USR - UART status register (address Eh) bit description

Bit	Symbol	Description
7	TO3	Time-out counter 3. TO3 = 1 when counter 3 has reached its terminal count.
6	TO2	Time-out counter 2. TO2 = 1 when counter 2 has reached its terminal count.
5	TO1	Time-out counter 1. TO1 = 1 when counter 1 has reached its terminal count.
4	EA	Early Answer. EA = 1 if the first start-bit on the I/O pin during ATR has been detected between the first 200 and n_{max} clock pulses with pin RST in LOW state (all activities on the I/O during the first 200 clock pulses with pin RST LOW are not taken into account) and before the first n_{max} clock pulses with pin RST in HIGH state. These two features are re-initialized at each toggling of pin RST. n_{max} = 384 for TDA8029HL/C1; n_{max} = 368 for TDA8029HL/C2.
3	PE	Parity error. In protocol T = 0, bit PE = 1 if the UART has detected a number of received characters with parity errors equal to the number written in bits PEC[2:0] or if a transmitted character has been NAKed by the card a number of times equal to the value programmed in bits PEC[2:0]. It is set at 10.5 ETU in the reception mode and at 11.5 ETU in the transmission mode. A character received with a parity error is not stored in register FIFO in protocol T = 0; the card should repeat this character. In protocol T = 1, a character with a parity error is stored in the FIFO and the parity error counter is not active.
2	OVR	Overrun. OVR = 1 if the UART has received a new character whilst URR was full. In this case, at least one character has been lost.
1	FER	Framing Error. FER = 1 when I/O was not in high-impedance state at 10.25 ETU after a start-bit. It is reset when USR has been read.
0	TBE/RBF	Transmit Buffer Empty / Receive Buffer Full. TBE and RBF share the same bit within register USR: when in transmission mode the relevant bit is TBE; when in reception mode it is RBF. TBE = 1 when the UART is in transmission mode and when the microcontroller may write the next character to transmit in register UTR. It is reset when the microcontroller has written data in the transmit register or when bit T/R in register UCR1 has been reset either automatically or by software. After detection of a parity error in transmission, it is necessary to wait 13.5 ETU before rewriting the character which has been NAKed by the card (manual mode, see Table 55). RBF = 1 when register FIFO is full. The microcontroller may read some of the characters in register URR, which clears bit RBF.

8.10.3 Card registers

When working with a card, the following registers are used for programming some specific parameters.

8.10.3.1 Programmable divider register (PDR)

This register is used for counting the card clock cycles forming the ETU. It is an auto-reload 8 bits counter counting from the programmed value down to 0.

Table 58: PDR - programmable divider register (address 2h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Reset	0	0	0	0	0	0	0	0
Access	read and write							

Table 59: PDR - programmable divider register (address 2h) bit description

Bit	Symbol	Description
7 to 0	PD[7:0]	Programmable divider value.

8.10.3.2 UART configuration register 2 (UCR2)

Table 60: UCR2 - UART configuration register 2 (address 3h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ENINT1	DISTBE/RBF	-	ENRX	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC
Reset	0	0	-	0	0	0	0	0
Access	read and write							

Table 61: UCR2 - UART configuration register 2 (address 3h) bit description

Bit	Symbol	Description
7	ENINT1	Enable INT1. If ENINT1 = 1, a HIGH to LOW transition on pin INT1_N will wake-up the TDA8029 from the Power-down mode. Note that in case of reception of a character when in Power-down mode, the start of the frame will be lost. When not in Power-down mode ENINT1 has no effect. For details on Power-down mode see Section 8.15
6	DISTBF/RBF	Disable TBE/RBF interrupts. If DISTBE/RBF is set, then reception or transmission of a character will not generate an interrupt. This feature is useful for increasing communication speed with the card; in this case, the copy of TBE/RBF bit within MSR must be polled, and not the original, in order not to loose priority interrupts which can occur in USR.
5	-	Not used.
4	ENRX	Enable RX. If ENRX = 1, a HIGH to LOW transition on pin RX will wake-up the TDA8029 from the Power-down mode. Note that in case of reception of a character when in Power-down mode, the start of the frame will be lost. When not in Power-down mode ENRX has no effect. For details on Power-down mode see Section 8.15.
3	SAN	Synchronous or asynchronous. SAN is set by software if a synchronous card is expected. The UART is then bypassed and only bit 0 in registers URR and UTR is connected to pin I/O. In this case the clock is controlled by bit SC in register CCR.
2	$\overline{\text{AUTOCONV}}$	Automatic set convention. If $\overline{\text{AUTOCONV}}$ = 1, then the convention is set by software using bit CONV in register UCR1. If $\overline{\text{AUTOCONV}}$ = 0, then the configuration is automatically detected on the first received character whilst the start session (bit SS) is set. $\overline{\text{AUTOCONV}}$ must not be changed during a card session.
1	CKU	Clock Unit. For baud rates other than those given in Table 62, there is the possibility to set bit CKU = 1. In this case, the ETU will last half the number of card clock cycles equal to prescaler PDR. Note that bit CKU = 1 has no effect if $f_{CLK} = f_{XTAL}$. This means, for example, that 76800 baud is not possible when the card is clocked with the frequency on pin XTAL1.
0	PSC	Prescaler value. If PSC = 1, then the prescaler value is 32; if PSC = 0, then the prescaler value is 31. One ETU will last a number of card clock cycles equal to prescaler × PDR. All baud rates specified in ISO 7816 norm are achievable with this configuration. See Figure 10 and Table 62.

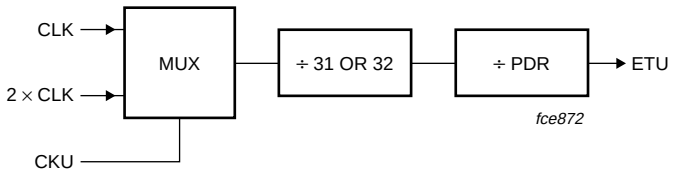


Fig 10. ETU generation

Table 62: Baud rate selection using values F and D

Card clock frequency f_{CLK} = 3.58 MHz for PSC = 31 and f_{CLK} = 4.92 MHz for PSC = 32 (example: in this table; 12 means prescaler set to 31 and PDR set to 12)

D	F											
	0	**1**	**2**	**3**	**4**	**5**	**6**	**9**	**10**	**11**	**12**	**13**
1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16 9600	32;24 6400	32;32 4800	32;48 3200	32;64 2400
2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8 19200	32;12 12800	32;16 9600	32;24 6400	32;32 4800
3	31;3 38400	31;3 38400	-	31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4 38400	32;6 25600	32;8 19200	32;12 12800	32;16 9600
4	-	-	-	31;3 38400	-	31;6 19200	-	32;2 76800	32;3 51300	32;4 38400	32;6 25600	32;8 19200
5	-	-	-	-	-	31;3 38400	-	32;1 153600	-	32;2 76800	32;3 51300	32;4 38400
6	-	-	-	-	-	-	-	-	-	32;1 153600	-	32;2 76800
8	31;1 115200	31;1 115200	-	31;2 57200	31;3 38400	31;4 28800	31;5 23040	-	32;2 76800	-	32;4 38400	-
9	-	-	-	-	-	-	31;3 38400	-	-	-	-	-

8.10.3.3 Guard time register (GTR)

The guard time register is used for storing the number of guard ETUs given by the card during ATR. In transmission mode, the UART will wait this number of ETUs before transmitting the character stored in register UTR.

Table 63: GTR - UART guard time register (address 5h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0
Reset	0	0	0	0	0	0	0	0
Access	read and write							

Table 64: GTR - UART guard time register (address 5h) bit description

Bit	Symbol	Description
7 to 0	GT[7:0]	Guard time value. When GT[7:0] = FFh: • In protocol T = 1: – TDA8029HL/C1 operates at 11 ETU – TDA8029HL/C2 operates at 10.8 ETU. • In protocol T = 0: – TDA8029HL/C1 operates at 12 ETU – TDA8029HL/C2 operates at 11.8 ETU.

8.10.3.4 UART configuration register 1 (UCR1)

This register is used for setting the parameters of the ISO UART.

Table 65: UCR1 - UART configuration register 1 (address 6h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	FIP	FC	PROT	T/R	LCT	SS	CONV
Reset	-	0	0	0	0	0	0	0
Access	read and write							

Table 66: UCR1 - UART configuration register 1 (address 6h) bit description

Bit	Symbol	Description
7	-	Not used.
6	FIP	Force Inverse Parity. If FIP = 1, then the UART will NAK a correct received character, and will transmit characters with wrong parity bit.
5	FC	Test bit. FC must be left to logic 0.
4	PROT	Protocol. If PROT = 1, then protocol type is asynchronous T = 1; if PROT = 0, the protocol is T = 0.
3	T/R	Transmit/Receive. This bit is set by software for transmission mode. A change from logic 0 to logic 1 will set bit TBE in register USR. T/R is automatically reset by hardware if LCT has been used before transmitting the last character.
2	LCT	Last Character to Transmit. This bit is set by software before writing the last character to be transmitted in register UTR. It allows automatic change to reception mode. It is reset by hardware at the end of a successful transmission. When LCT is being reset, the bit T/R is also reset and the ISO 7816 UART is ready for receiving a character.
1	SS	Start Session. This bit is set by software before ATR for automatic convention detection and early answer detection. It is automatically reset by hardware at 10.5 ETU after reception of the initial character.
0	CONV	Convention. This bit is set if the convention is direct. Bit CONV is either automatically written by hardware according to the convention detected during ATR, or by software if bit $\overline{\text{AUTOCONV}}$ in register UCR2 is set.

8.10.3.5 Clock configuration register (CCR)

This register defines the clock to the card and the clock to the ISO UART. Note that if bit CKU in the prescaler register of the selected card (register UCR2) is set, then the ISO UART is clocked at twice the frequency to the card, which allows to reach baud rates not foreseen in ISO 7816 norm.

Table 67: CCR - Clock configuration register (address 1h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SHL	CST	SC	AC2	AC1	AC0
Reset	-	-	0	0	0	0	0	0
Access	read and write							

Table 68: CCR - Clock configuration register (address 1h) bit description

Bit	Symbol	Description
7 and 6	-	Not used.
5	SHL	Select HIGH Level. This bit determines how the clock is stopped when bit CST = 1. If SHL = 0, then the clock is stopped at LOW level, if SHL = 1 at HIGH level.
4	CST	Clock Stop. In case of an asynchronous card, bit CST defines whether the clock to the card is stopped or not. If CST = 1, then the clock is stopped. If CST = 0, then the clock is determined by bits AC[2:0] according to Table 69. All frequency changes are synchronous, ensuring that no spike or unwanted pulse width occurs during changes.
3	SC	Synchronous Clock. In the event of a synchronous card, then pin CLK is the copy of the value of bit SC. In reception mode, the data from the card is available to bit UR0 after a read operation of register URR. In transmission mode, the data is written on the I/O line of the card when register UTR has been written to.
2 to 0	AC[2:0]	Asynchronous card clock. When CST = 0, the clock is determined by the state of these bits according to Table 69. f_{int} is the frequency delivered by the internal oscillator clock circuitry. For switching from $1/n f_{XTAL}$ to $1/2 f_{int}$ and reverse, only the bit AC2 must be changed (AC1 and AC0 must remain the same). For switching from $1/n f_{XTAL}$ or $1/2 f_{int}$ to stopped clock and reverse, only bits CST and SHL must be changed. When switching from $1/n f_{XTAL}$ to $1/2 f_{int}$ and reverse, a delay can occur between the command and the effective frequency change on pin CLK. The fastest switch is from $1/2 f_{XTAL}$ to $1/2 f_{int}$ and reverse, the best regarding duty cycle is from $1/8 f_{XTAL}$ to $1/2 f_{int}$ and reverse. The bit CLKSW in register MSR tells the effective switch moment. In case of $f_{CLK} = f_{XTAL}$, the duty cycle must be ensured by the incoming clock signal on pin XTAL1.

Table 69: CLK value for an asynchronous card

AC2	AC1	AC0	CLK
0	0	0	f_{XTAL}
0	0	1	$1/2 f_{XTAL}$
0	1	0	$1/4 f_{XTAL}$
0	1	1	$1/8 f_{XTAL}$
1	0	0	$1/2 f_{int}$
1	0	1	$1/2 f_{int}$
1	1	0	$1/2 f_{int}$
1	1	1	$1/2 f_{int}$

8.10.3.6 Power control register (PCR)

This register is used for starting or stopping card sessions.

Table 70: PCR - power control register (address 7h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	1V8	RSTIN	3V/5V	START
Reset	-	-	-	-	0	0	0	0
Access	read and write							

Table 71: PCR - power control register (address 7h) bit description

Bit	Symbol	Description
7 to 4	-	Not used.
3	1V8	Select 1.8 V. If 1V8 = 1, then V_{CC} = 1.8 V. It should be noted that specifications are not guaranteed at this voltage when the supply voltage V_{DD} is less than 3 V.
2	RSTIN	Card reset. When the card is activated, pin RST is the copy of the value written in RSTIN.
1	3V/5V	Select 3 V or 5 V. If 3V/5V = 1, then V_{CC} = 3 V. If 3V/5V = 0, then V_{CC} = 5 V.
0	START	Activate and deactivate card. If START = 1 is written by the controller, then the card is activated (see description in Section 8.16 “Activation sequence”). If the controller writes START = 0, then the card is deactivated (see description in Section 8.17 “Deactivation sequence”). START is automatically reset in case of emergency deactivation. For deactivating the card, only bit START should be reset.

8.10.4 Register summary

Table 72: Register summary

Name	Addr. (hex)	R/W	Bit								Value at reset [1]	Value when $\overline{RIU}$ = 0 [1]
			7	6	5	4	3	2	1	0		
CSR	00	R/W	-	-	-	-	$\overline{RIU}$	-	-	-	XXXX 0XXX	XXXX 0XXX
CCR	01	R/W	-	-	SHL	CST	SC	AC2	AC1	AC0	XX00 0000	XXuu uuuu
PDR	02	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	0000 0000	uuuu uuuu
UCR2	03	R/W	ENINT1	DISTBE/ RBF	-	ENRX	SAN	$\overline{AUTO\ CONV}$	CKU	PSC	00X0 0000	uuuu uuuu
GTR	05	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	0000 0000	uuuu uuuu
UCR1	06	R/W	-	FIP	FC	PROT	T/R	LCT	SS	CONV	X000 0000	Xuuu 00uu
PCR	07	R/W	-	-	-	-	1V8	RSTIN	3V/5V	START	XXXX 0000	XXXX uuuu
TOC	08	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	0000 0000	0000 0000
TOR1	09	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	0000 0000	uuuu uuuu
TOR2	0A	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	0000 0000	uuuu uuuu
TOR3	0B	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	0000 0000	uuuu uuuu
FCR	0C	W	-	PEC2	PEC1	PEC0	-	FL2	FL1	FL0	X000 X000	Xuuu Xuuu
MSR	0C	R	CLKSW	FE	BGT	-	-	PR1	-	TBE/ RBF	010X XXX0	u10X XuX0
URR	0D	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	0000 0000	0000 0000
UTR	0D	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	0000 0000	0000 0000
USR	0E	R	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/ RBF	0X00 0000	0000 0000
HSR	0F	R	SDWN	-	PRTL1	SUPL	-	PRL1	-	PTL	XX01 X0X0	uXuu XuXu

[1] X = undefined, u = no change.

8.11 Supply

The circuit operates within a supply voltage range of 2.7 V to 6 V. The supply pins are V_{DD}, DCIN, GND and PGND. Pins DCIN and PGND supply the analog drivers to the cards and have to be externally decoupled because of the large current spikes the card and the step-up converter can create. V_{DD} and GND supply the rest of the chip. An integrated spike killer ensures the contacts to the card to remain inactive during power-up or -down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor, and the V_{CC} generators.

V_{DCIN} may be higher than V_{DD}.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor connected to the CDEL pin, when V_{DD} is too low to ensure proper operation (1 ms per 2 nF typical). This pulse is used as a Power-on reset pulse, and also to block either any spurious signals on card contacts during controllers reset or to force an automatic deactivation of the contacts in the event of supply drop-out (see Section 8.16 and Section 8.17).

After power-on or after a voltage drop, the bit SUPL is set within the Hardware Status Register (HSR) and remains set until HSR is read when the alarm pulse is inactive. As long as the Power-on reset is active, INT0_N is LOW.

The same occurs when leaving Shut-down mode or when the RESET pin has been set active.

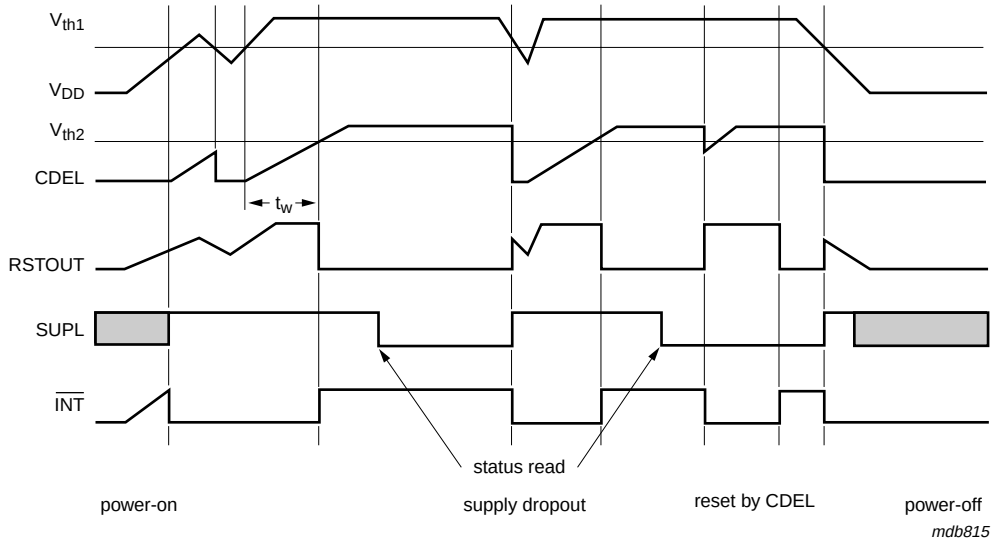


Fig 11. Voltage supervisor

8.12 DC-to-DC converter

Except for V_{CC} generator, and the other card contacts buffers, the whole circuit is powered by V_{DD} and DCIN. If the supply voltage is 2.7 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the DC-to-DC converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency of approximately 2.5 MHz.

There are several possible situations:

- V_{DCIN} = 3 V and V_{CC} = 3 V: In this case the DC-to-DC converter is acting as a doubler with a regulation of about 4.0 V
- V_{DCIN} = 3 V and V_{CC} = 5 V: In this case the DC-to-DC converter is acting as a tripler with a regulation of about 5.5 V
- V_{DCIN} = 5 V and V_{CC} = 3 V: In this case, the DC-to-DC converter is acting as a follower, V_{DD} is applied on VUP
- V_{DCIN} = 5 V and V_{CC} = 5 V. In this case, the DC-to-DC converter is acting as a doubler with a regulation of about 5.5 V
- V_{CC} = 1.8 V. In this case, whatever value of V_{DCIN}, the DC-to-DC converter is acting as a follower, V_{DD} is applied on VUP.

The switch between different modes of the DC-to-DC converter is done by the TDA8029 at about V_{DCIN} = 3.5 V.

The output voltage is fed to the V_{CC} generator. V_{CC} and GNDC are used as a reference for all other card contacts.

8.13 ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (bit START = 1 in register PCR) is only possible if the card is present (pin PRES is HIGH) and if the supply voltage is correct (supervisor not active).

Pin PRES is internally biased with a current source of 45 μA typical to ground when the pin is open (No card present). When pin PRES becomes HIGH, via the detection switch connected to V_{DD}, this internal bias current is reduced to 2.5 μA to ground. This feature allows direct connection of the detect switch to V_{DD} without a pull-down resistor.

The presence of the card is signalled to the controller by the HSR.

Bit PR1 in register MSR is set if the card is present. Bit PRL1 in register HSR is set if PR1 has toggled.

During a session, the sequencer performs an automatic emergency deactivation on the card in the event of card take-off, short-circuit, supply dropout or overheating. The card is also automatically deactivated in case of supply voltage drop or overheating. The HSR register is updated and the INT0_N line falls down, so the system controller is aware of what happened.

8.14 Protections and limitations

The TDA8029 features the following protections and limitations:

- I_{CC} limited to 100 mA, and deactivation when this limit is reached
- Current to or from pin RST limited to 20 mA, and deactivation when this limit is reached
- Deactivation when the temperature of the die exceeds 150 °C
- Current to or from pin I/O limited to 10 mA

- Current to or from pin CLK limited to 70 mA
- ESD protection on all card contacts and pin PRES at minimum 6 kV, thus no need of extra components for protecting against ESD flash caused by a charged card being introduced in the slot
- Short circuit between any card contacts can have any duration without any damage.

8.15 Power reduction modes

On top of the standard controller power reduction features described in the microcontroller section, the TDA8029 has several power reduction modes that allow its use in portable equipment, and help protecting the environment:

1. Shut-down mode: when SDWN_N pin is LOW, then the bit SDWN within HSR will be set, causing an interrupt on INT0_N. The TDA8029 will read the status, deactivate the card if it was active, set all ports to logic 1 and enter Power-down mode by setting bit PD in the controller's PCON register. In this mode, it will consume less than 20 μA, because the internal oscillator is stopped, and all biasing currents are cut.

   When SDWN_N returns to HIGH, a Power-on reset operation is performed, so the chip is in the same state than at power-on.
2. Power-down mode: the microcontroller is in Power-down mode, and the card is deactivated. The bias currents in the chip and the frequency of the internal oscillator are reduced. In this mode, the consumption is less than 100 μA.
3. Sleep mode: the microcontroller is in Power-down mode, the card is activated, but with the clock stopped HIGH or LOW. In this case, the card is supposed not to draw more than 2 mA from V_{CC}. The bias currents and the frequency of the internal oscillator are also reduced. With a current of 100 μA drawn by the card, the consumption is less than 500 μA in tripler mode, 400 μA in doubler mode, or 300 μA in follower mode.

When in Power-down or Sleep mode, card extraction or insertion, overcurrent on pins RST or V_{CC}, or HIGH level on pin RESET will wake up the chip.

The same occurs in case of a falling edge on RX if bit ENRX is set, or on INT1_N if bit ENINT1 is set and if INT1_N is enabled within the controller.

If only INT1_N should wake up the TDA8029, then INT1_N must be enabled in the controller, and ENINT1 only should be set.

If RX should wake up the TDA8029, then INT1_N must be enabled in the controller, and ENRX and ENINT1 should be set.

In case of wake up by RX, then the first received characters may be lost, depending on the baud rate on the serial link. (The controller waits for 1536 clock cycles before leaving Power-down mode).

For more details about the use of these modes, please refer to the application notes *"AN00069"* and *"AN01005"*.

8.16 Activation sequence

When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GNDC. The DC-to-DC converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the system controller may initiate an activation sequence of the card. Figure 12 shows the activation sequence.

After leaving the UART reset mode, and then configuring the necessary parameters for the UART, it may set the bit START in register PCR (t_0). The following sequence will take place:

- The DC-to-DC converter is started (t_1)
- V_{CC} starts rising from 0 V to 5 V or 3 V with a controlled rise time of 0.17 V/µs typically (t_2)
- I/O rises to V_{CC} (t_3), (Integrated 14 kΩ pull-up to V_{CC})
- CLK is sent to the card and RST is enabled (t_4).

After a number of clock pulses that can be counted with the time-out counter, bit RSTIN may be set by software, then pin RST rises to V_{CC}.

The sequencer is clocked by $^{1}/_{64}f_{int}$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $^{3}/_{64}T$, $t_2 = t_1 + {}^{3}/_{2}T$, $t_3 = t_1 + {}^{7}/_{2}T$, and $t_4 = t_1 + 4T$.

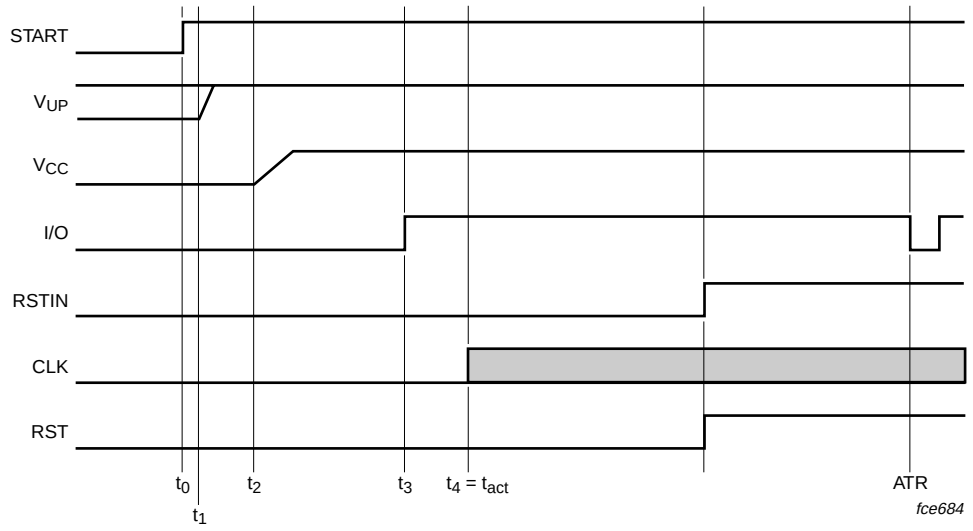


Fig 12. Activation sequence

8.17 Deactivation sequence

When the session is completed, the microcontroller resets bit START (t_{10}). The circuit then executes an automatic deactivation sequence shown in Figure 13:

- Card reset (pin RST falls LOW) (t_{11})
- Clock (pin CLK) is stopped LOW (t_{12})
- Pin I/O falls to 0 V (t_{13})
- V_{CC} falls to 0 V with typical 0.17 V/µs slew rate (t_{14})
- The DC-to-DC converter is stopped and CLK, RST, V_{CC} and I/O become low-impedance to GNDC (t_{15}).

$t_{11} = t_{10} + {}^{3}/_{64}T$, $t_{12} = t_{11} + {}^{1}/_{2}T$, $t_{13} = t_{11} + T$, $t_{14} = t_{11} + {}^{3}/_{2}T$, $t_{15} = t_{11} + {}^{7}/_{2}T$.

t_{de} is the time that V_{CC} needs for going down to less than 0.4 V.

Automatic emergency deactivation is performed in the following cases:

- Withdrawal of the card (PRES LOW)
- Overcurrent detection on V_{CC} (bit PRTL1 set)
- Overcurrent detection on RST (bit PRTL1 set)
- Overheating (bit PTL set)
- V_{DD} low (bit SUPL set)
- RESET pin active HIGH.

If the reason of the deactivation is a card take off, an overcurrent or an overheating, then INT0_N is LOW. The corresponding bit in the hardware status register is set. Bit START is automatically reset.

If the reason is a supply dropout, then the deactivation sequence occurs, and a complete reset of the chip is performed. When the supply will be OK again, then the bit SUPL will be set in HSR.

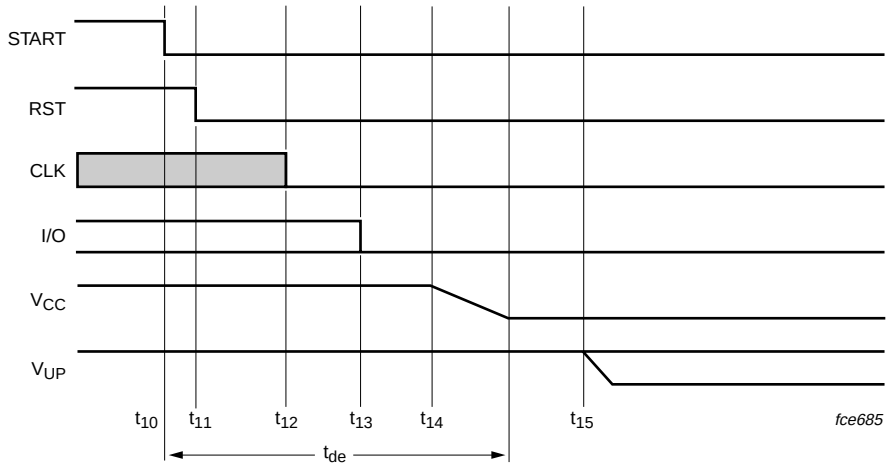


Fig 13. Deactivation sequence

9. Limiting values

Table 73: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DCIN}	input voltage for the DC-to-DC converter		–0.5	+6.5	V
V_{DD}	supply voltage		–0.5	+6.5	V
V_n	voltage limit				
	on pins SAM, SBM, SAP, SBP, VUP		–0.5	+7.5	V
	on all other pins		–0.5	V_{DD} + 0.5	V

Table 73: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	continuous total power dissipation	T_{amb} = –40 °C to +90 °C		-	500	mW
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			-	125	°C
V_{esd}	electrostatic discharge	human body model	[1]			
	on pins I/O, V_{CC}, RST, CLK and GNDC			–6	+6	kV
	on pin PRES			–1.5	+1.5	kV
	on pins SAM and SBM			–1	+1	kV
	on other pins			–2	+2	kV

[1] Human body model as defined in JEDEC Standard JESD22-A114-B, dated June 2000.

10. Thermal characteristics

Table 74: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

11. Characteristics

Table 75: Characteristics

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.7	-	6.0	V
		NDS conditions	3	-	6.0	V
V_{DCIN}	input voltage for the DC-to-DC converter		V_{DD}	-	6.0	V
$I_{DD(sd)}$	supply current in Shut-down mode	V_{DD} = 3.3 V	-	-	20	µA
$I_{DD(pd)}$	supply current in Power-down mode	V_{DD} = 3.3 V; card inactive; microcontroller in Power-down mode	-	-	110	µA
$I_{DD(sl)}$	supply current in Sleep mode	V_{DD} = 3.3 V; card active at V_{CC} = 5 V; clock stopped; microcontroller in Power-down mode; I_{CC} = 0 A	-	-	800	µA

Table 75: Characteristics *...continued*

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(om)}$	supply current operating mode	I_{CC} = 65 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 5 V card; V_{DD} = 2.7 V	-	-	250	mA
		I_{CC} = 50 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 3 V card; V_{DD} = 2.7 V	-	-	125	mA
		I_{CC} = 50 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 3 V card; V_{DD} = 5 V	-	-	65	mA
V_{th1}	threshold voltage on V_{DD} (falling)		2.15	-	2.45	V
V_{hys1}	hysteresis on V_{th1}		50	-	170	mV
V_{th2}	threshold voltage on pin CDEL		-	1.25	-	V
V_{CDEL}	voltage on pin CDEL		-	-	V_{DD} + 0.3	V
I_{CDEL}	output current at CDEL	pin grounded (charge)	-	–2	-	µA
		V_{CDEL} = V_{DD} (discharge)	-	2	-	mA
C_{CDEL}	capacitance value		1	-	-	nF
$t_{W(alarm)}$	alarm pulse width	C_{CDEL} = 22 nF	-	10	-	ms
Crystal oscillator: pins XTAL1 and XTAL2						
f_{XTAL}	crystal frequency		4	-	25	MHz
f_{ext}	external frequency applied on XTAL1		0	-	27	MHz
V_{IH}	HIGH-level input voltage on XTAL1		0.7V_{DD}	-	V_{DD} + 0.2	V
V_{IL}	LOW-level input voltage on XTAL1		–0.3	-	0.3V_{DD}	V
DC-to-DC converter						
f_{int}	oscillation frequency		2	2.6	3.2	MHz
V_{VUP}	voltage on pin VUP	5 V card	-	5.7	-	V
		3 V card	-	4.1	-	V
V_{det}	detection voltage on pin DCIN for × 2/× 3 selection	follower/doubler for 3 V card, doubler/tripler for 5 V card	3.4	3.5	3.6	V
Reset output to the card pin: RST						
$V_{O(inactive)}$	output voltage in inactive mode	no load	0	-	0.1	V
		$I_{O(inactive)}$ = 1 mA	0	-	0.3	V
$I_{O(inactive)}$	current from RST	inactive and pin grounded	0	-	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	-	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	0.9V_{CC}	-	V_{CC}	V
t_r	rise time	C_L = 250 pF	-	-	0.1	µs
t_f	fall time	C_L = 250 pF	-	-	0.1	µs

Table 75: Characteristics *...continued*

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock output to the card pin: CLK						
$V_{O(inactive)}$	output voltage in inactive mode	no load	0	-	0.1	V
		$I_{O(inactive)}$ = 1 mA	0	-	0.3	V
$I_{O(inactive)}$	current from pin CLK	inactive and pin grounded	0	-	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	-	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	$0.9V_{CC}$	-	V_{CC}	V
t_r	rise time	C_L = 35 pF, V_{CC} = 5 V or 3 V	-	-	10	ns
t_f	fall time	C_L = 35 pF, V_{CC} = 5 V or 3 V	-	-	10	ns
f_{CLK}	card clock frequency	internal clock configuration	1	-	1.5	MHz
		external clock configuration	0	-	20	MHz
δ	duty cycle	except for XTAL; C_L = 35 pF	45	-	55	%
SR_r, SR_f	slew rate, rise and fall	C_L = 35 pF	0.2	-	-	V/ns
Card supply voltage: pin V_{CC} [1]						
$V_{O(inactive)}$	output voltage inactive	no load	0	-	0.1	V
		$I_{O(inactive)}$ = 1 mA	0	-	0.3	V
$I_{O(inactive)}$	current from V_{CC}	inactive and pin grounded	-	-	–1	mA
V_{CC}	output voltage	active mode; I_{CC} < 65 mA; 5 V card	4.75	5	5.25	V
		active mode; I_{CC} < 65 mA if V_{DD} > 3.0 V else I_{CC} < 50 mA; 3 V card	2.80	3	3.20	V
		active mode; I_{CC} < 30 mA; 1.8 V card	1.62	1.8	1.98	V
		active mode; current pulses of 40 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 5 V card	4.6	-	5.3	V
		active mode; current pulses of 40 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 3 V card	2.75	-	3.25	V
		active mode; current pulses of 12 nAs with I < 200 mA, t < 400 ns, f < 20 MHz; 1.8 V card	1.62	-	1.98	V

Table 75: Characteristics *...continued*

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	output current	5 V card; V_{CC} = 0 V to 5 V	-	-	65	mA
		3 V card; V_{CC} = 0 V to 3 V; V_{DD} > 3.0 V	-	-	65	mA
		3 V card; V_{CC} = 0 V to 3 V; V_{DD} < 3.0 V	-	-	50	mA
		1.8 V card; V_{CC} = 0 V to 1.8 V;	-	-	30	mA
		V_{CC} shorted to ground (current limitation)	-	-	120	mA
SR_r, SR_f	slew rate, rise and fall	maximum load capacitor = 300 nF	0.05	0.16	0.22	V/µs
$V_{ripple(p-p)}$	ripple voltage on V_{CC} (peak-to-peak value)	20 kHz < f < 200 MHz	-	-	350	mV
Data line: pin I/O, with an integrated 14kΩ pull-up resistor to V_{CC}						
$V_{O(inactive)}$	output voltage inactive	no load	0	-	0.1	V
		$I_{O(inactive)}$ = 1 mA	-	-	0.3	V
$I_{O(inactive)}$	current from I/O	inactive; pin grounded	-	-	–1	mA
V_{OL}	LOW-level output voltage	I/O configured as output; I_{OL} = 1 mA	0	-	0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as output; V_{CC} = 5 V or 3 V				
		I_{OH} < –40 µA	0.75V_{CC}	-	V_{CC} + 0.25	V
		I_{OH} < –20 µA	0.8V_{CC}	-	V_{CC} + 0.25	V
		I_{OH} = 0 A	0.9V_{CC}	-	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	I/O configured as input	–0.3	-	+0.8	V
V_{IH}	HIGH-level input voltage	I/O configured as input	1.5	-	V_{CC}	V
I_{IL}	input current LOW	V_{IL} = 0 V	-	-	500	µA
$I_{LI(H)}$	input leakage current HIGH	V_{IH} = V_{CC}	-	-	10	µA
$t_{i(T)}$	input transition time	C_L ≤ 65 pF	-	-	1	µs
$t_{o(T)}$	output transition time	C_L ≤ 65 pF	-	-	0.1	µs
R_{pu}	internal pull-up resistance between I/O and V_{CC}		11	14	17	kΩ
t_{edge}	width of active pull-up pulse	I/O configured as output, rising from LOW to HIGH	2/f_{XTAL1}	-	3/f_{XTAL1}	ns
I_{edge}	current from I/O when active pull-up	V_{OH} = 0.9V_{CC}, C = 60 pF	–1	-	-	mA
Timings						
t_{act}	activation sequence duration		-	-	130	µs
t_{de}	deactivation sequence duration		-	-	100	µs

Table 75: Characteristics *...continued*

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Protections and limitations						
$I_{CC(sd)}$	shut-down and limitation current at V_{CC}	[2]	-	–100	-	mA
$I_{I/O(lim)}$	limitation current on pin I/O		–15	-	+15	mA
$I_{CLK(lim)}$	limitation current on pin CLK		–70	-	+70	mA
$I_{RST(sd)}$	shut-down current on pin RST		-	-20	-	mA
$I_{RST(lim)}$	limitation current on RST		–20	-	+20	mA
T_{sd}	shut-down temperature		-	150	-	°C
Card presence input: pin PRES						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
I_{IL}	LOW-level input current	$V_I < 0.5V_{DD}$	25	-	100	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$	-	-	10	µA
Shut-down input: pin SDWN_N						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
$I_{LI(L)}$	input leakage current LOW	V_I = 0 V	-	-	±20	µA
$I_{LI(H)}$	input leakage current HIGH	$V_I = V_{DD}$	-	-	±20	µA
I/O: General purpose I/O pins P16, P17, P26 and P27; interrupt pin INT1_N; and serial link pins RX and TX [3]						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD}$ + 0.9	-	-	V
V_{OL}	LOW-level input voltage	I_{OL} = 1.6 mA	-	-	0.4	V
V_{OH}	HIGH-level input voltage	I_{OH} = –30 µA	V_{DD} – 0.7	-	-	V
I_{IL}	input current LOW	V_I = 0.4 V	–1	-	–50	µA
I_{THL}	HIGH to LOW transition current	V_I = 2 V	-	-	–650	µA

Table 75: Characteristics *...continued*

V_{DD} = V_{DCIN} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset input: pin RESET, active HIGH						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V

[1] Two ceramic multilayer capacitances with low ESR of minimum 100 nF should be used in order to meet these specifications.

[2] This is an overload detection.

[3] These ports are standard C51 ports. An active pull-up ensures fast LOW to HIGH transitions.

12. Application information

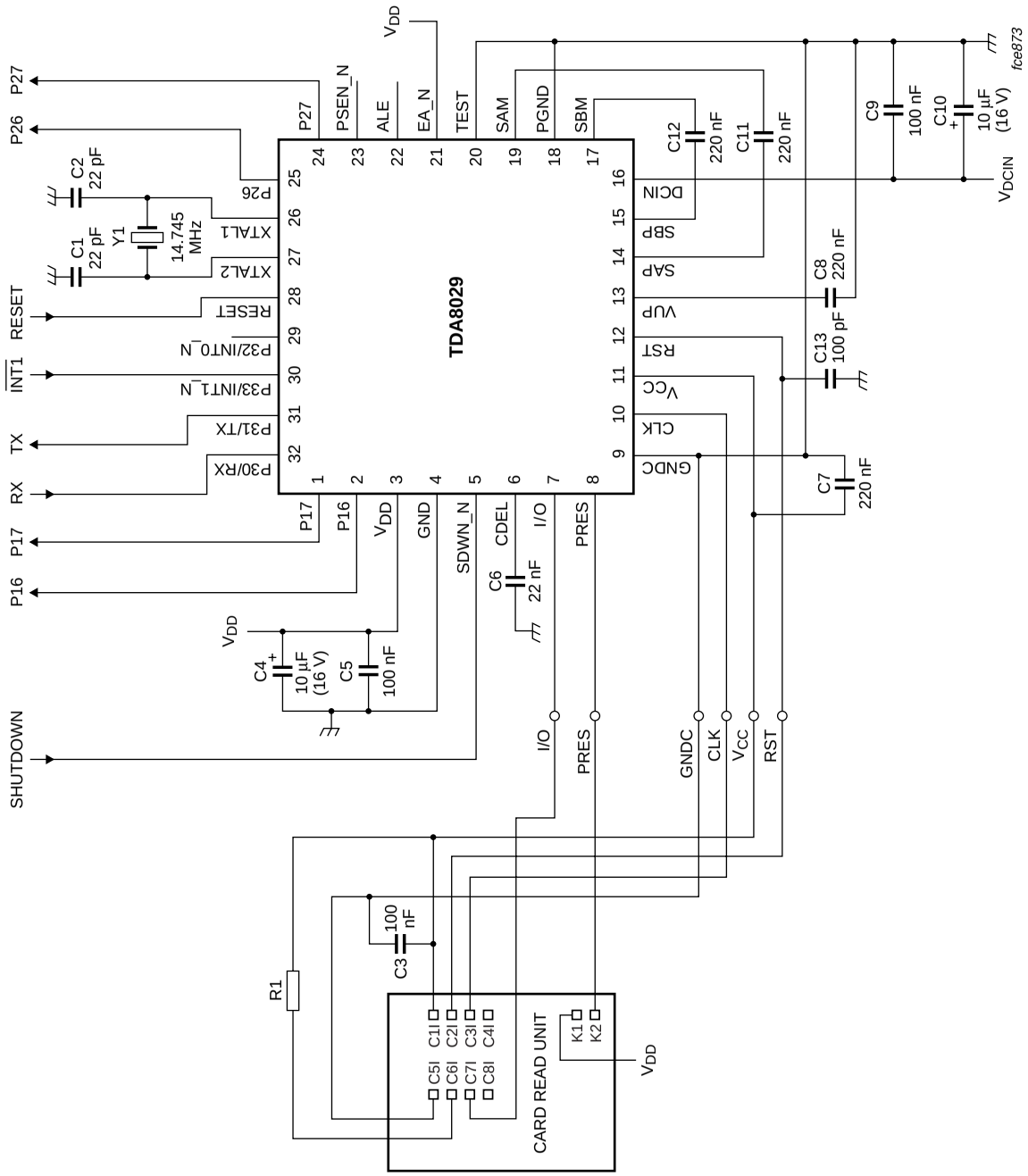
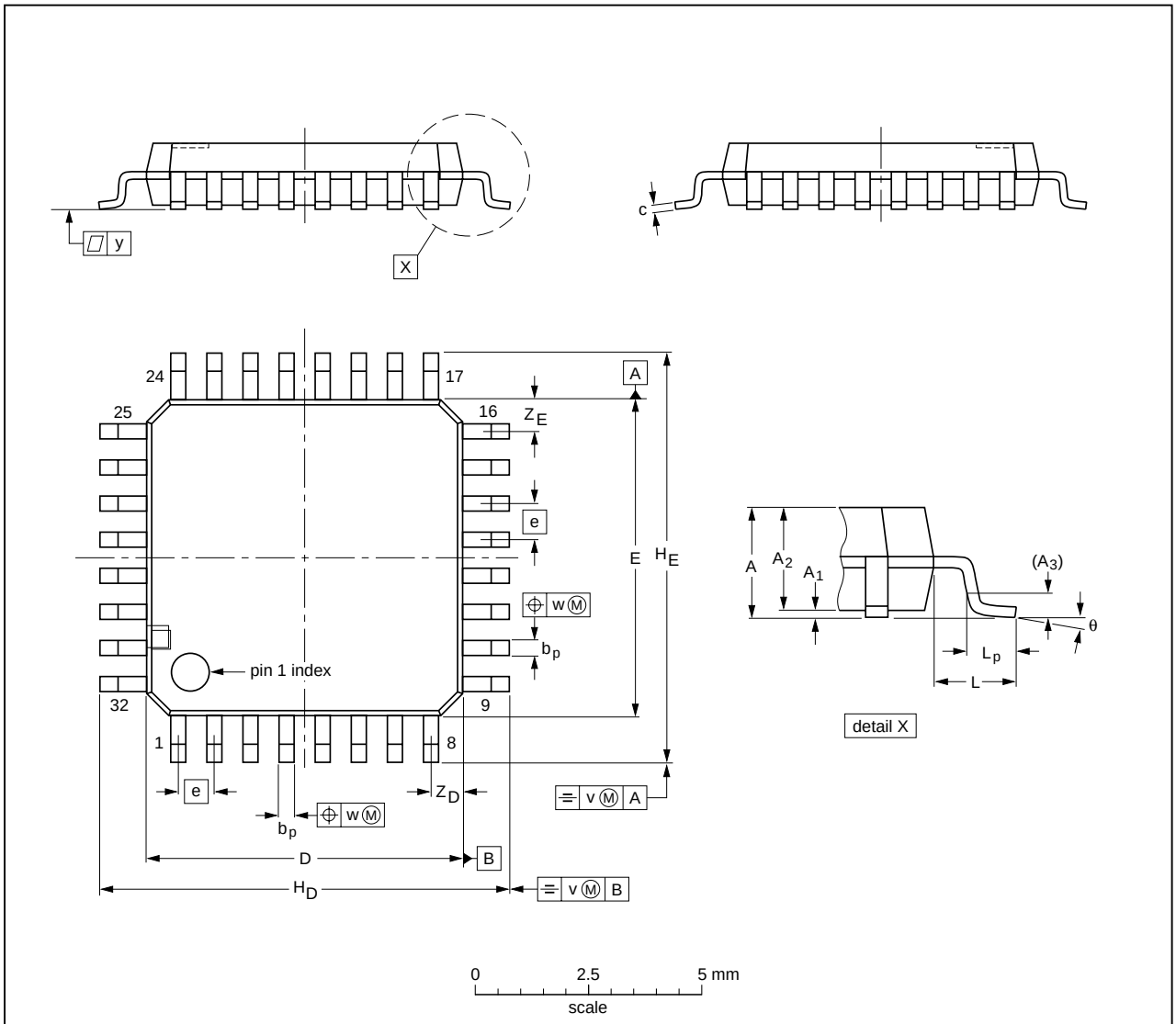


Fig 14. Application diagram

13. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~00-01-19~~ 03-02-25

Fig 15. Package outline SOT358-1 (LQFP32)

14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 76: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 77: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA8029_3	20050222	Product data sheet	-	9397 750 14145	TDA8029_2
Modifications:	• The format of this data sheet has been redesigned to comply with the presentation and information standard of Philips Semiconductors. • Section 2: Modified feature on V_{CC} generation • Section 4: Modified various values and added external crystal frequency specification • Section 7: Modified descriptions of pins 2, 5, 8, 28 and 29; added a pin type column to the pinning table • Section 8.1: Added a reference to the hardware status register description • Section 8.13: Added an additional paragraph describing bias current on pin PRES • Section 8.15: Added information on wake-up • Section 8.17: Added a V_{DD} low condition to emergency deactivation conditions list • Section 11: Modified various values; added external crystal frequency, doubler/tripler voltage, pin PRES input current specifications and added a note for the General purpose I/O • Section 12: Added a capacitor C13 and modified a capacitor C7 in the application diagram				
TDA8029_2	20031030	Product specification	-	9397 750 11827	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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