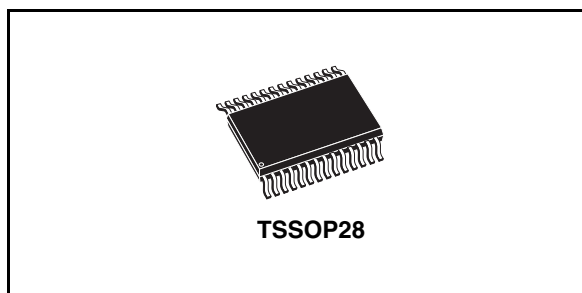


## 3 band car audio processor

### Features

- Input multiplexer
  - Multiple input configuration for different application
- Loudness
  - 2nd order frequency response
  - Programmable center frequency
  - 15dB with 1dB steps
  - Selectable high frequency boost
  - Selectable flat-mode
- Volume
  - +15dB to -15dB with 1dB step resolution
  - Soft-step control with programmable blend times
- Bass
  - 2nd order frequency response
  - Center frequency programmable in 4 steps
  - Q programmable 1.0/1.25/1.5/2.0
  - DC gain programmable
  - -15 to 15dB range with 1dB resolution
- Middle
  - 2nd order frequency response
  - Center frequency programmable in 4 steps
  - Q programmable 0.5/0.75/1.0/1.25
  - -15 to 15dB range with 1dB resolution
- Treble
  - 2nd order frequency response
  - Center frequency programmable in 4 steps
  - -15 to 15dB range with 1dB resolution
- Speaker
  - 4 independent soft step speaker controls
  - 0dB to -79dB with 1dB steps
  - Direct mute
- Subwoofer
  - 2nd order low pass filter with programmable cut off frequency
  - 2 independent soft step level control,



- Mute functions
  - Direct mute
  - Digitally controlled SoftMute with 4 programmable mute-times
- Offset detection
  - Offset voltage detection circuit for on-board power amplifier failure diagnosis
- Level meter
  - Provide rectified level voltage of main source signal (before loudness)
- Rear seat selector
  - Full source selector for rear seat output
- Mixing selector

### Description

The TDA7719 is a high performance signal processor specifically designed for car radio applications. The device includes a high performance audioprocessor with fully integrated audio filters and new Soft Step architecture. The digital control allows programming in a wide range of filter characteristics. By the use of BCMOS-process and liner signal processing low distortion and low noise are obtained.

**Table 1. Device summary**

Order code	Package	Packing
TDA7719	TSSOP28	Tube
TDA7719TR	TSSOP28	Tape and reel

# Contents

- 1      Block circuit diagram ..... 6**
- 2      Pin connections and pin descriptions ..... 7**
  - 2.1    Pin connections ..... 7
  - 2.2    Pin description ..... 7
- 3      Electrical specifications and characteristics ..... 9**
  - 3.1    Thermal data ..... 9
  - 3.2    Absolute maximum ratings ..... 9
  - 3.3    Electrical characteristics ..... 9
- 4      Description ..... 13**
  - 4.1    Input stages ..... 13
  - 4.2    Mixing ..... 15
  - 4.3    Loudness ..... 16
    - 4.3.1    Loudness attenuation ..... 16
    - 4.3.2    Peak frequency ..... 17
    - 4.3.3    High frequency boost ..... 17
    - 4.3.4    Flat mode ..... 18
  - 4.4    SoftMute ..... 18
  - 4.5    SoftStep volume ..... 18
  - 4.6    Bass ..... 18
    - 4.6.1    Bass attenuation ..... 19
    - 4.6.2    Bass center frequency ..... 19
    - 4.6.3    Bass quality factors ..... 20
    - 4.6.4    DC mode ..... 20
  - 4.7    Middle ..... 21
    - 4.7.1    Middle attenuation ..... 21
    - 4.7.2    Middle center frequency ..... 21
    - 4.7.3    Middle quality factors ..... 22
  - 4.8    Treble ..... 22
    - 4.8.1    Treble attenuation ..... 22
    - 4.8.2    Treble center frequency ..... 23

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4.9	Subwoofer Filter .....	23
4.10	Softstep control .....	24
4.11	DC offset detector and level meter option .....	25
4.12	DC offset detector .....	25
4.13	Level meter .....	26
4.14	Output gain control .....	26
4.15	Audioprocessor testing .....	26
4.16	Test circuit (3 x QD + 1 x FD + DC offset detector) .....	27
<b>5</b>	<b>I2C Bus specification .....</b>	<b>28</b>
5.1	Interface protocol .....	28
5.1.1	Receive mode .....	28
5.1.2	Transmission mode .....	28
5.1.3	Reset condition .....	28
5.2	Data byte specification .....	30
<b>6</b>	<b>Package information .....</b>	<b>43</b>
<b>7</b>	<b>Revision history .....</b>	<b>44</b>

## List of tables

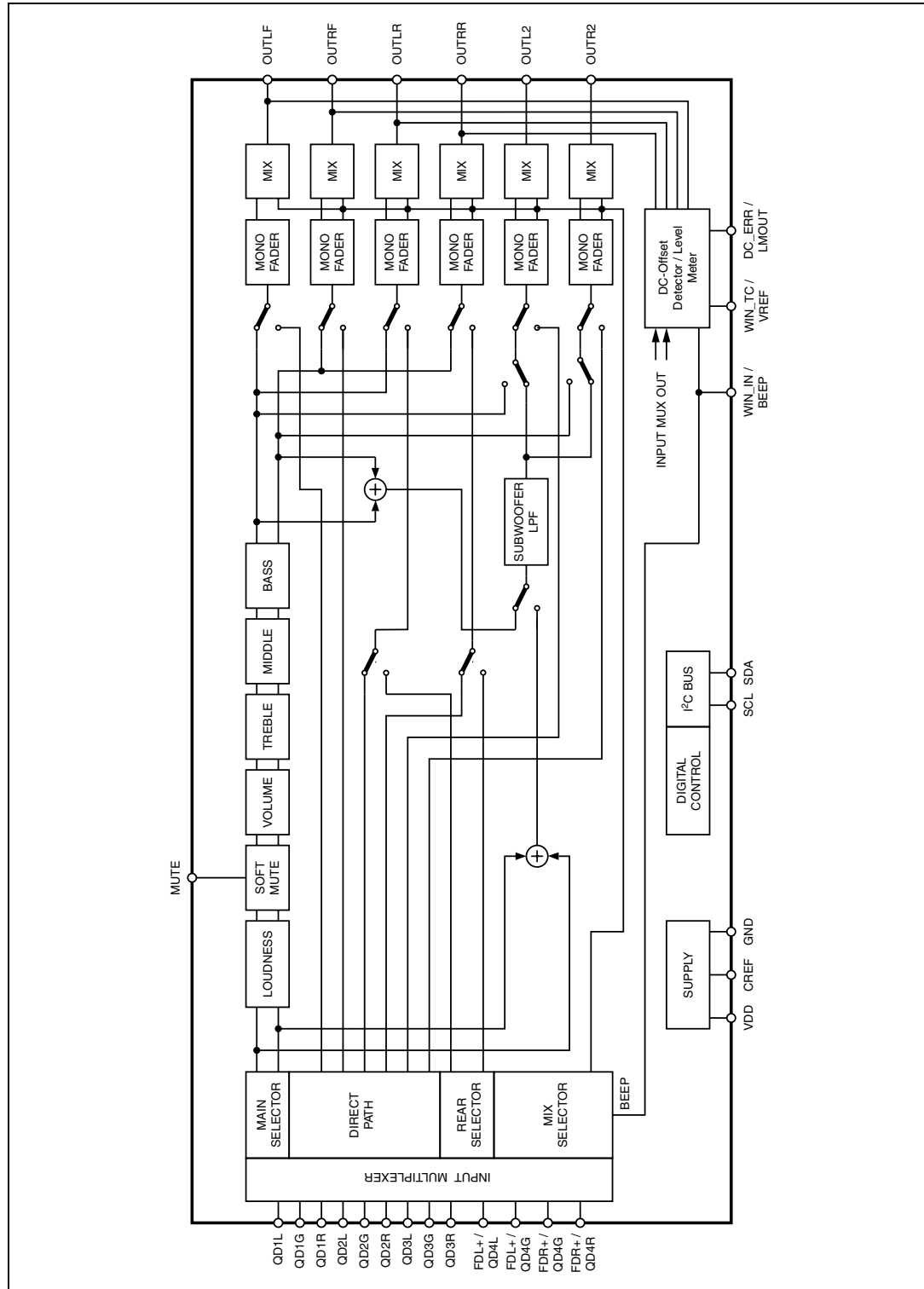
Table 1.	Device summary . . . . .	1
Table 2.	Pin description . . . . .	7
Table 3.	Thermal data . . . . .	9
Table 4.	Absolute maximum ratings . . . . .	9
Table 5.	Electrical characteristics . . . . .	9
Table 6.	Input pin configuration . . . . .	13
Table 7.	Selector configuration matrix . . . . .	14
Table 8.	Available sources for mixing . . . . .	16
Table 9.	Subaddress (receive mode) . . . . .	29
Table 10.	Input configuration / main selector (0) . . . . .	30
Table 11.	2nd Source selector / direct path (1) . . . . .	31
Table 12.	Mixing source / mixing gain (2) . . . . .	32
Table 13.	Mix control / level meter / dc offset detector configure (3) . . . . .	33
Table 14.	Soft mute / others (4) . . . . .	34
Table 15.	SoftStep I (5) . . . . .	35
Table 16.	SoftStep II / DC detector (6) . . . . .	36
Table 17.	Loudness (7) . . . . .	37
Table 18.	Volume / output gain (8) . . . . .	37
Table 19.	Treble filter (9) . . . . .	38
Table 20.	Middle filter (10) . . . . .	38
Table 21.	Bass filter (11) . . . . .	39
Table 22.	Subwoofer / middle / bass (12) . . . . .	39
Table 23.	Speaker attenuation (LF/RF/LR/RR) (13-16) . . . . .	40
Table 24.	Subwoofer attenuation (subwoofer L/subwoofer R) (17-18) . . . . .	40
Table 25.	Testing audio processor 1 (19) . . . . .	41
Table 26.	Testing audio processor 2 (20) . . . . .	42
Table 27.	Document revision history . . . . .	44

## List of figures

Figure 1.	Block circuit diagram. . . . .	6
Figure 2.	Pin connections (top view) . . . . .	7
Figure 3.	QD and FD configuration of QD4/FD4 . . . . .	15
Figure 4.	Block diagram of mixing stage . . . . .	15
Figure 5.	Loudness attenuation @ $f_P = 400\text{Hz}$ . . . . .	16
Figure 6.	Loudness center frequencies @ $\text{Attn.} = 15\text{dB}$ . . . . .	17
Figure 7.	Loudness attenuation, $f_c=2.4\text{kHz}$ . . . . .	17
Figure 8.	Softmute timing . . . . .	18
Figure 9.	Bass Control @ $f_C = 80\text{Hz}$ , $Q = 1$ . . . . .	19
Figure 10.	Bass center frequencies @ $\text{gain} = 14\text{dB}$ , $Q = 1$ . . . . .	19
Figure 11.	Bass quality factors @ $\text{gain} = 14\text{dB}$ , $f_C = 80\text{Hz}$ . . . . .	20
Figure 12.	Bass normal and DC mode @ $\text{Gain} = 14\text{dB}$ , $f_c = 80\text{Hz}$ . . . . .	20
Figure 13.	Middle control @ $f_C = 1\text{kHz}$ , $Q = 1$ . . . . .	21
Figure 14.	Middle center frequencies @ $\text{gain} = 14\text{dB}$ , $Q = 1$ . . . . .	21
Figure 15.	Middle quality factors @ $\text{gain} = 14\text{dB}$ , $f_c = 1\text{kHz}$ . . . . .	22
Figure 16.	Treble Control @ $f_C = 17.5\text{kHz}$ . . . . .	22
Figure 17.	Treble center frequencies @ $\text{gain} = 14\text{dB}$ . . . . .	23
Figure 18.	Subwoofer control . . . . .	23
Figure 19.	DC offset detection circuit (simplified) . . . . .	26
Figure 20.	Test circuit . . . . .	27
Figure 21.	TSSOP28 mechanical data and package dimensions . . . . .	43

# 1 Block circuit diagram

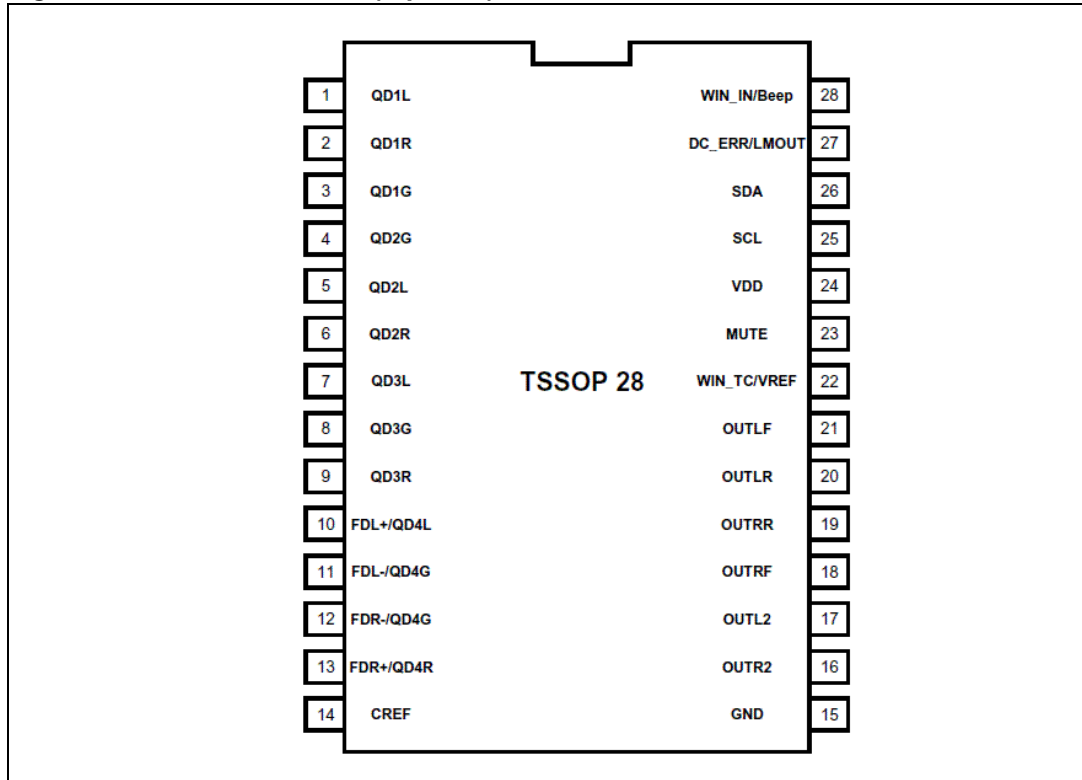
Figure 1. Block circuit diagram



## 2 Pin connections and pin descriptions

### 2.1 Pin connections

Figure 2. Pin connections (top view)



### 2.2 Pin description

Table 2. Pin description

No.	Pin name	Description	I/O
1	QD1L / SE1L / MD3+	QD1 left input or SE1 left or MD3 positive input	I/O
2	QD1R / SE1R / MD3-	QD1 right input or SE1 right input or MD3 negative input	I/O
3	QD1G / SE2L	QD1 common input or SE2 left input	I/O
4	QD2G / SE2R	QD2 common input or SE2 right input	I/O
5	QD2L / SE3L	QD2 left input or SE3 left input	I/O
6	QD2R / SE3R	QD2 right input or SE3 right input	I/O
7	QD3L	QD3 left input	I/O
8	QD3G	QD3 common input	I/O
9	QD3R	QD3 right input	I/O

Table 2. Pin description (continued)

No.	Pin name	Description	I/O
10	QD4L / FD4+ / SE4L / MD1+	QD4 left input or FD4L positive input or SE4 left input or MD1 positive input	I/O
11	QD4G / FD4L- / SE4R / MD1-	QD4 common input or FD4L negative input or SE4 right input or MD1 negative input	I/O
12	QD4G / FD4R- / SE5L / MD2-	QD4 common input or FD4R negative input or SE5 left input or MD2 negative input	I/O
13	QD4R / FD4R+ / SE5R / MD2+	QD4 right input or FD4R positive input or SE5 right input or MD2 positive input	I/O
14	CREF	Reference capacitor	O
15	GND	Ground	S
16	OUTR2	Subwoofer output / 2 <sup>nd</sup> right output	O
17	OUTL2	Subwoofer output / 2 <sup>nd</sup> left output	O
18	OUTRF	Front right output	O
19	OUTRR	Rear right output	O
20	OUTLR	Rear left output	O
21	OUTLF	Front left output	O
22	WinTC / VREF	DC offset detector filter or Vref output	O
23	MUTE	I <sup>2</sup> C bus data	I/O
24	VDD	Supply	S
25	SCL	I <sup>2</sup> C bus clock	I
26	SDA	I <sup>2</sup> C bus data	I/O
27	DC_ERR / LMOUT	DC offset detector output or Level meter output	O
28	WIN_IN / Beep	DC offset detector input or Beep input (Mono Single-Ended input)	I



## 3 Electrical specifications and characteristics

### 3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th-j\ amb}$	Thermal resistance junction to ambient	114	°C/W

### 3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_S$	Operating supply voltage	10.5	V
$V_{in\_max}$	Maximum voltage for signal input pins	7	V
$T_{amb}$	Operating ambient temperature	-40 to 85	°C
$T_{stg}$	Storage temperature range	-55 to 150	°C

### 3.3 Electrical characteristics

$V_S = 8.5V$ ;  $T_{amb} = 25^\circ C$ ;  $R_L = 10k\Omega$ ; all gains = 0dB;  $f = 1kHz$ ; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Supply</b>						
$V_s$	Supply voltage		7.5	8.5	10	V
$I_s$	Supply current		25	35	45	mA
<b>Input selector</b>						
$R_{in}$	Input resistance	All single ended inputs <sup>(1)</sup>	70	100	130	k $\Omega$
$V_{CL}$	Clipping level	Input Gain = 0dB	1.8	2		$V_{RMS}$
$S_{IN}$	Input separation		80	100		dB
<b>Differential stereo inputs</b>						
$R_{in}$	Input resistance	Differential	70	100	130	k $\Omega$
CMRR1	Common mode rejection ratio for main source	$V_{CM}=1\ VRMS@\ 1kHz$	46			dB
		$V_{CM}=1\ VRMS@\ 10kHz$	46	60		dB
CMRR2	Common mode rejection ratio for 2 <sup>nd</sup> source	$V_{CM}=1\ VRMS@\ 1kHz$	46	60		dB
$e_{No}$	Output noise @ speaker outputs	20Hz-20kHz, A-weighted; all stages 0dB		12	30	$\mu V$

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Loudness control</b>						
$A_{MAX}$	Max attenuation		17	15	13	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_{Peak}^{(2)}$	Peak frequency	$f_{P1}$	360	400	440	Hz
		$f_{P2}$	720	800	880	Hz
		$f_{P3}$	2200	2400	2600	Hz
<b>Volume control</b>						
$G_{MAX}$	Max gain		13	15	17	dB
$A_{MAX}$	Max attenuation		-17	-15	-13	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$E_A$	Attenuation set error		-0.75	0	+0.75	dB
$E_T$	Tracking error				2	dB
$V_{DC}$	DC steps	Adjacent attenuation steps		0.1	3	mV
		From 0dB to $G_{MIN}$		0.5	5	mV
<b>Soft mute</b>						
$A_{MUTE}$	Mute attenuation		80	100		dB
$T_D$	Delay time	T1	0.16	0.48	0.80	ms
		T2	0.32	0.96	1.6	ms
		T3	3	8	13	ms
		T4	10	16	20	ms
$V_{TH\ Low}$	Low threshold for SM pin				0.6	V
$V_{TH\ High}$	High threshold for SM pin		2.7			V
$R_{PU}$	Internal pull-up resistor		32	45	58	k $\Omega$
$V_{PU}$	Internal pull-up Voltage		3.1	3.3	3.5	V
<b>Bass control</b>						
$F_c$	Center frequency	$f_{C1}$	54	60	66	Hz
		$f_{C2}$	72	80	88	Hz
		$f_{C3}$	90	100	110	Hz
		$f_{C4}$	180	200	220	Hz
$Q_{BASS}^{(2)}$	Quality factor	$Q_1$	0.9	1	1.1	
		$Q_2$	1.1	1.25	1.4	
		$Q_3$	1.3	1.5	1.7	
		$Q_4$	1.8	2	2.2	
$C_{RANGE}$	Control range		$\pm 14$	$\pm 15$	$\pm 16$	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$DC_{GAIN}$	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on, Gain = $\pm 15$ dB	3.5	$\pm 4.4$	5.5	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Middle control</b>						
$C_{RANGE}$	Control range		±14	±15	±16	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_c^{(2)}$	Center frequency	$f_{C1}$	400	500	600	Hz
		$f_{C2}$	0.8	1	1.2	kHz
		$f_{C3}$	1.2	1.5	1.8	kHz
		$f_{C4}$	2	2.5	3	kHz
$Q_{BASS}^{(2)}$	Quality factor	$Q_1$	0.45	0.5	0.55	
		$Q_2$	0.65	0.75	0.85	
		$Q_3$	0.9	1	1.1	
		$Q_4$	1.1	1.25	1.4	
<b>Treble control</b>						
$C_{RANGE}$	Clipping level		±14	±15	±16	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_c^{(2)}$	Center frequency	$f_{C1}$	8	10	12	kHz
		$f_{C2}$	10	12.5	15	kHz
		$f_{C3}$	12	15	18	kHz
		$f_{C4}$	14	17.5	21	kHz
<b>Speaker attenuators</b>						
$A_{MIN}$	Min attenuation		-1	0	1	dB
$A_{MAX}$	Max attenuation		-89	-79	-69	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$A_{MUTE}$	Mute attenuation		80	90		dB
$E_E$	Attenuation set error				2	dB
$V_{DC}$	DC steps	Adjacent attenuation steps		0.1	5	mV
<b>Audio outputs</b>						
$V_{CL}$	Clipping level	$d = 0.3\%$ ; Byte8_D6=1	2			$V_{RMS}$
		$d = 1\%$ ; Byte8_D6=0	2.2			$V_{RMS}$
$R_{OUT}$	Output impedance			30	100	$\Omega$
$R_L$	Output load resistance		2			k $\Omega$
$C_L$	Output load capacitor				10	nF
$V_{DC}$	DC voltage level		3.8	4.0	4.2	V
<b>Subwoofer attenuator</b>						
$G_{MAX}$	Max gain		14	15	16	dB
$A_{MAX}$	Max attenuation		-89	-79	-69	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$A_{MUTE}$	Mute attenuation		80	90		dB
$E_E$	Attenuation set error				2	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>DC</sub>	DC steps	Adjacent attenuation steps		0.1	5	mV
<b>Subwoofer lowpass</b>						
f <sub>LP</sub> <sup>(2)</sup>	Lowpass corner frequency	f <sub>LP1</sub>	72	80	88	Hz
		f <sub>LP2</sub>	108	120	132	Hz
		f <sub>LP3</sub>	144	160	176	Hz
<b>DC offset detection circuit</b>						
V <sub>th</sub>	Zero comp window size	V2	±20	±50	±80	mV
		V3	±30	±75	±110	mV
		V4	±60	±100	±140	mV
t <sub>sp</sub>	Max rejected spike length		5	11	25	µs
			10	22	50	µs
			15	33	75	µs
			20	44	100	µs
I <sub>CHDCerr</sub>	DCErr charge current		1	5	10	µA
I <sub>DISDCerr</sub>	DCErr discharge current		3.5	5	6.5	mA
V <sub>OutH</sub>	DCErr high volotage		3	3.3	3.6	V
V <sub>OutL</sub>	DCErr low voltage			100	300	mV
<b>Level meter</b>						
V <sub>out</sub>	Output voltage range		0		3.4	V
V <sub>LEVEL</sub>	Output level	V <sub>in</sub> = 1Vrms	1.2	1.6	2.0	V
		V <sub>in</sub> = AC Grounded	-0.5	0	0.5	V
T <sub>DEL</sub>	Analog output delay time			2		µs
<b>General</b>						
e <sub>NO</sub>	Output noise	BW=20Hz to 20kHz A-Weighted, all gain = 0dB		12	30	µV
		BW=20Hz - 20kHz A-Weighted, Output muted		6	25	µV
S/N	Signal to noise ratio	all gain = 0dB, A-weighted; V <sub>o</sub> = 2V <sub>RMS</sub>		104		dB
D	Distortion	V <sub>IN</sub> = 1V <sub>RMS</sub> ; all stages 0dB		0.01	0.2	%
S <sub>C</sub>	Channel separation left/right		80	90		dB

1. When DC offset detector is not used, the impedance of mono single-ended input is 50kΩ instead of 100kΩ
2. Minimun, typical and maximum are calculate in according to simulation result. Functionality is guaranteed by measuring a directly correlated parameter.

## 4 Description

### 4.1 Input stages

The input stage (Main source and 2<sup>nd</sup> source) is configurable to adapt to different application. There are 7 different configurations which provide different input structure and different number of input sources as shown below.

- 4 x QD,
- 2 x QD + 3 x SE,
- 1 x QD + 5 x SE,
- 1 x QD + 3 x SE + 2 x MD,
- 3 x QD + 1 x FD,
- 3 x QD + 2 x SE,
- 1 x QD + 2 x SE + 1 x FD + 1 x MD,
- 1 x QD + 3 x SE + 1 x FD

*Note:* QD = Quasi-Differential, SE = Single-ended input, FD = Full Differential, MD = mono Differential

The configuration of the input stage is controlled by 'Input Configuration' bits in I<sup>2</sup>C control table (Byte0 Bit5~Bit7). The table below shows the configuration of input pins in different configurations.

**Table 6. Input pin configuration**

Pin	Pin name	Configuration bits (Byte0 Bit7~Bit5)															
		"000"		"001"		"010"		"011"		"100"		"101"		"110"		"111"	
		CFG0	CFG1	CFG2	CFG3	CFG4	CFG5	CFG6	CFG7	CFG8	CFG9	CFG10	CFG11	CFG12	CFG13	CFG14	CFG15
1	QD1L_SE1L_MD3+	QD1L	IN0	SE1L	IN0	SE1L	IN0	SE1L	IN0	QD1L	IN0	QD1L	IN0	MD3+	IN7	SE1L	IN0
2	QD1R_SE1R_MD3-	QD1R		SE1R		SE1R		SE1R		QD1R		QD1R		MD3-		SE1R	
3	QD1G_SE2L	QD1G	IN4	SE2L	IN4	SE2L	IN4	SE2L	IN4	QD1G	IN4	QD1G	IN4	SE2L	IN4	SE2L	IN4
4	QD2G_SE2R	QD2G		SE2R		SE2R		SE2R		QD2G		QD2G		SE2R		SE2R	
5	QD2L_SE3L	QD2L	IN1	SE3L	IN1	SE3L	IN1	SE3L	IN1	QD2L	IN1	QD2L	IN1	SE3L	IN1	SE3L	IN1
6	QD2R_SE3R	QD2R		SE3R		SE3R		SE3R		QD2R		QD2R		SE3R		SE3R	
7	QD3L	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2
8	QD3G	QD3G		QD3G		QD3G		QD3G		QD3G		QD3G		QD3G		QD3G	
9	QD3R	QD3R	IN3	QD3R	IN3	QD3R	IN3	QD3R	IN3	QD3R	IN3	QD3R	IN3	QD3R	IN3	QD3R	IN3
10	QD4L_FD4+_SE4L_MD1+	QD4L		QD4L		SE4L		IN5		MD1+		IN3		FD4L+		IN3	
11	QD4G_FD4L_SE4R_MD1-	QD4G	IN3	QD4G	IN3	SE4R	IN6	MD1-	IN3	FD4L-	IN6	SE4R	IN6	FD4L-	IN6	FD4L-	IN6
12	QD4G_FD4R_SE5L_MD2-	QD4G		QD4G		SE5L		IN6		MD2-		IN3		FD4R-		IN6	
13	QD4R_FD4R+_SE5R_MD2+	QD4R	IN3	QD4R	IN3	SE5R	IN6	MD2+	IN3	FD4R+	IN6	SE5R	IN6	FD4R+	IN6	FD4R+	IN6

With different input configuration, the input source can be selected with input selector (Byte0/1 Bit0~Bit2). The following matrix defines the selector configuration of different input sources dependant on the configuration bits.

**Table 7. Selector configuration matrix**

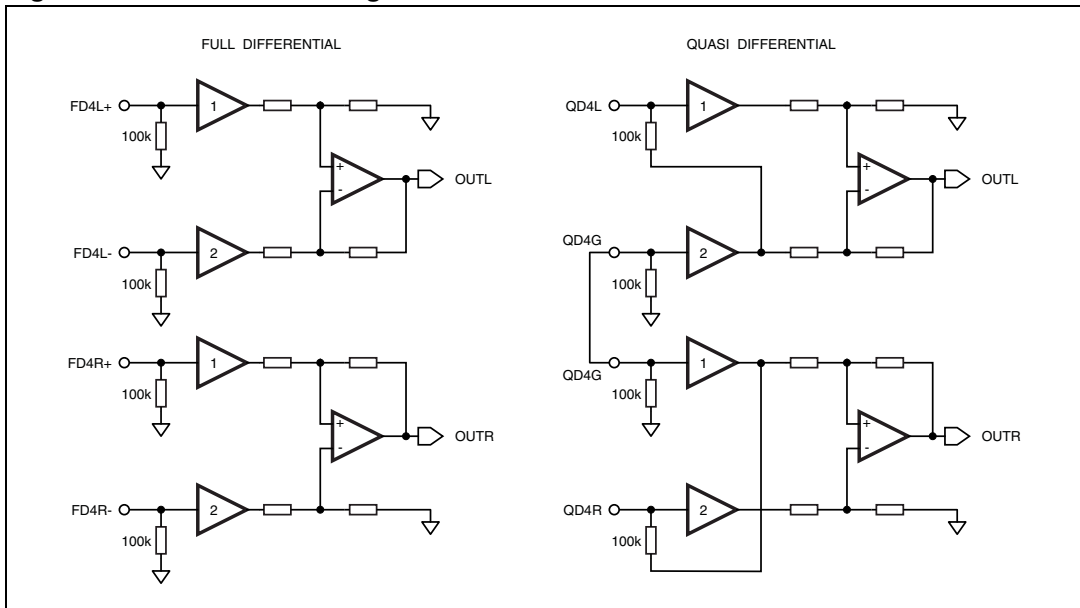
Selector Bits (Byte0/1 Bit2~Bit0)	000	001	010	011	100	101	110	111
	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
CFG0	QD1	QD2	QD3	QD4	NA	NA	NA	NA
CFG1	SE1	SE3	QD3	QD4	SE2	NA	NA	NA
CFG2	SE1	SE3	QD3	NA	SE2	SE4	SE5	NA
CFG3	SE1	SE3	QD3	MD1/2	SE2	NA	NA	NA
CFG4	QD1	QD2	QD3	FD	NA	NA	NA	NA
CFG5	QD1	QD2	QD3	NA	NA	SE4	SE5	NA
CFG6	NA	SE3	QD3	FD	SE2	NA	NA	MD3
CFG7	SE1	SE3	QD3	FD	SE2	NA	NA	NA

*Note:* In each configuration, only the green cells are allowed. The red cells is not allowed. MD1/MD2 selection is defined by extra bit – ‘MD1/2 selection’ in I<sup>2</sup>C control table (Bit3 of Byte0/1).

The input stage can be configured to 0dB or 3dB gain with I<sup>2</sup>C bus. The 0dB configuration allows up to 2V<sub>rms</sub> input signal level, while with 3dB gain, the internal signal will start to clip when input signal level is higher than 1.414V<sub>rms</sub>.

The Pin10~Pin13 can be configured as full differential input stage or quasi-differential input. When it is configured as quasi-differential input, both Pin11 and Pin12 are used as the QD common input pins. These two pins must be connected together externally in application. In this case the input impedance of QD4 common is reduced to 50kΩ (half of QD4 left and right input). The diagram below shows both QD and FD configuration of QD4/FD4.

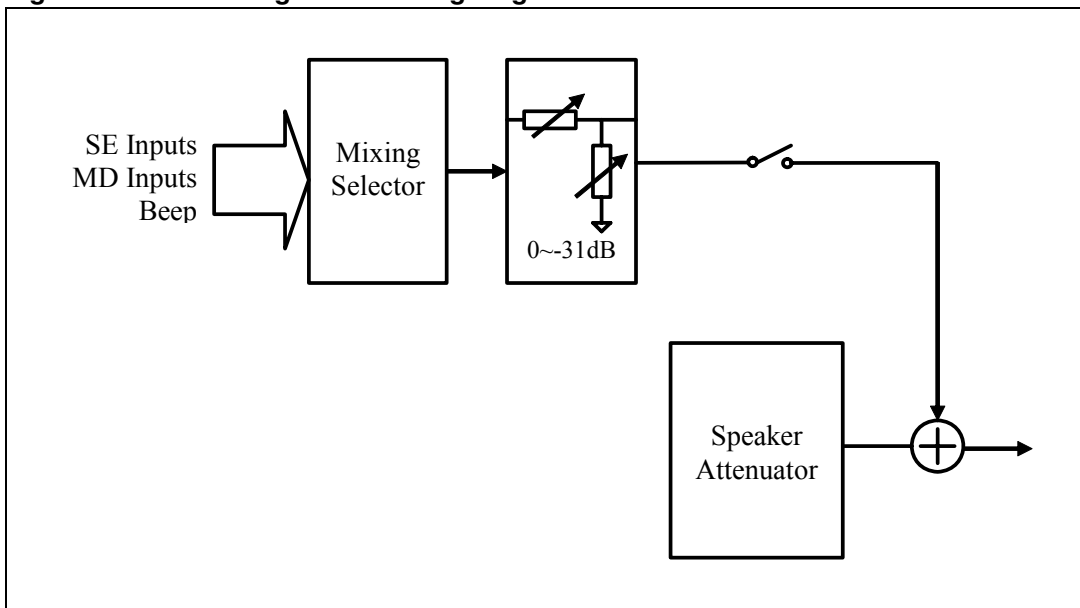
**Figure 3. QD and FD configuration of QD4/FD4**



## 4.2 Mixing

The device provides mixing function which allows the mixing source mixed into front and rear speaker output independently. The mixing source can be any single-ended input, mono-differential input or beep input (Mono single-ended input when DC offset detector is not used). In order to adjust the level of mixing signal, the mixing selector is followed with a 0dB~-31dB attenuator. The maximum mixing input signal level is 1.6Vrms for single-ended input and mono-differential input. For beep input, the maximum input signal level is about 1.4Vrms. The block diagram of the mixing function is shown below.

**Figure 4. Block diagram of mixing stage**



Since the input stage of this device has different configurations, the corresponding sources for mixing selector are also different according to the configurations. The following table defines the available sources for mixing under different configurations.

**Table 8. Available sources for mixing**

Mix selector bits (Byte2 Bit2~Bit0)	000	001	010	011	100	101	110	111
	MixIN0	MixIN1	MixIN2	MixIN3	MixIN4	MixIN5	MixIN6	MixIN7
CFG0	NA	NA	NA	NA	NA	NA	Beep	Mute
CFG1	SE1	SE2	SE3	NA	NA	NA	Beep	Mute
CFG2	SE1	SE2	SE3	SE4	SE5	NA	Beep	Mute
CFG3	SE1	SE2	SE3	MD1	NA	MD2	Beep	Mute
CFG4	NA	NA	NA	NA	NA	NA	Beep	Mute
CFG5	NA	NA	NA	SE4	SE5	NA	Beep	Mute
CFG6	MD3	SE2	SE3	NA	NA	NA	Beep	Mute
CFG7	SE1	SE2	SE3	NA	NA	NA	Beep	Mute

*Note:* Only green cells are allowed mixing input. The red cells are not allowed. The beep input is available only when DC offset detector function is not used.

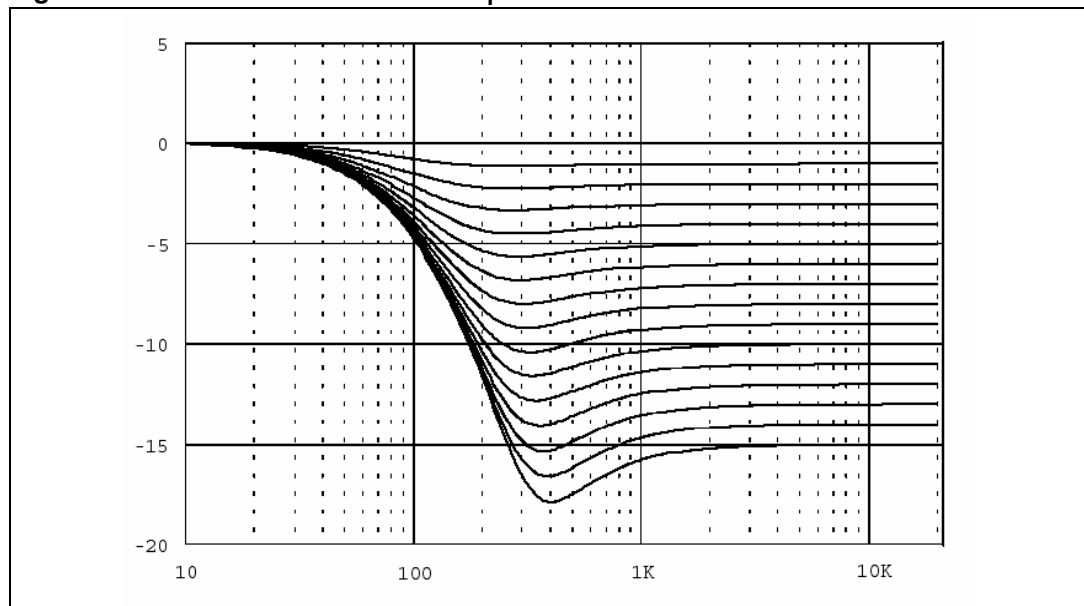
### 4.3 Loudness

There are four parameters programmable in the loudness stage:

#### 4.3.1 Loudness attenuation

Figure 5 shows the attenuation as a function of frequency at  $f_p = 400\text{Hz}$

**Figure 5. Loudness attenuation @  $f_p = 400\text{Hz}$ .**

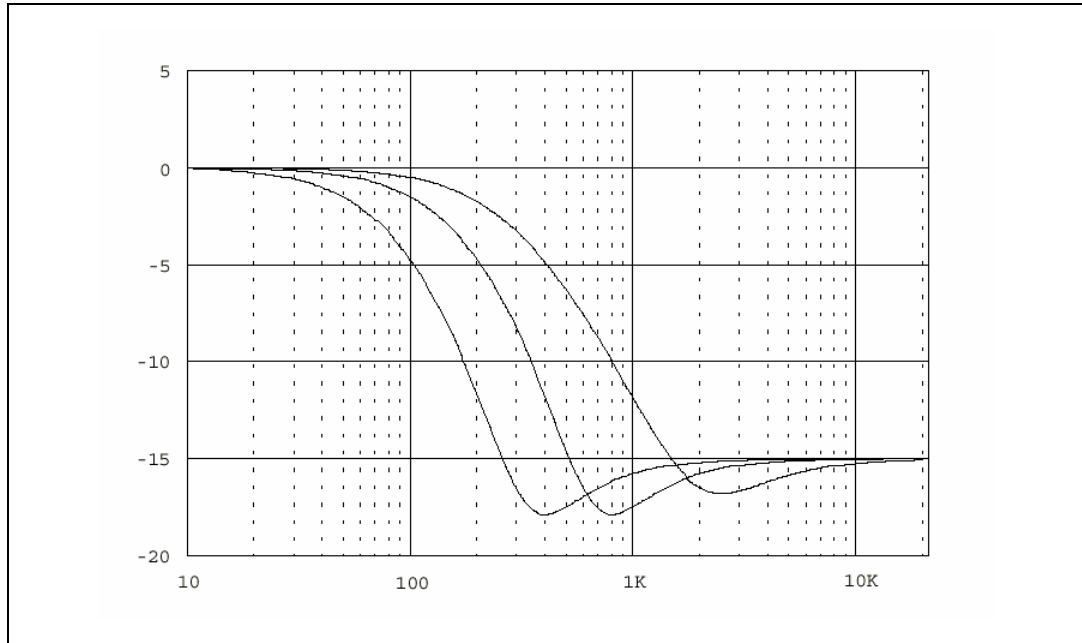




### 4.3.2 Peak frequency

Figure 6 shows the four possible peak-frequencies at 400, 800 and 2400Hz

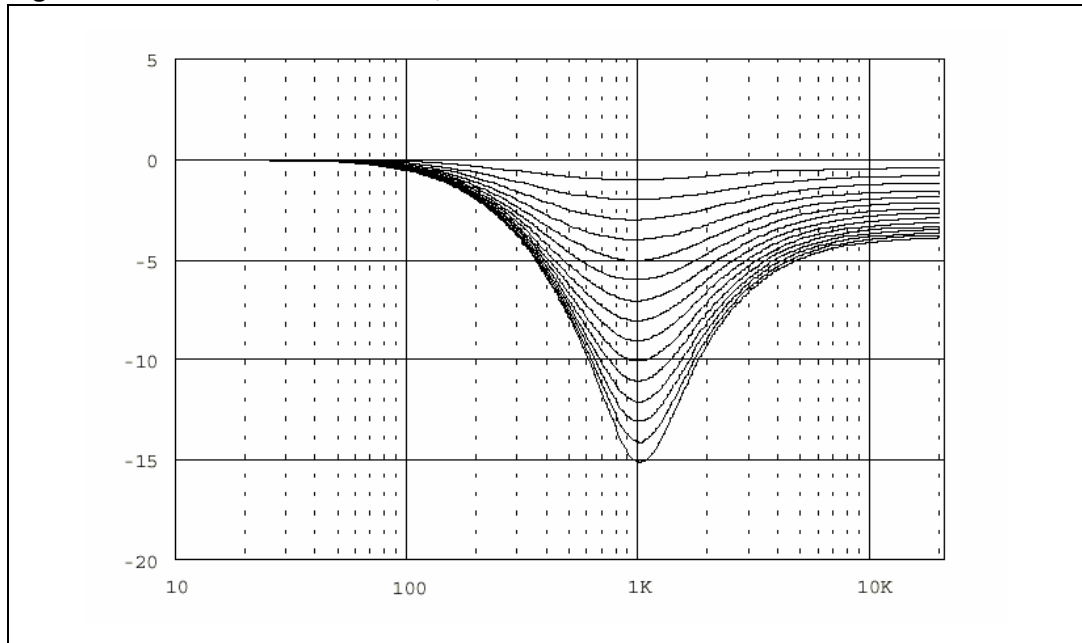
Figure 6. Loudness center frequencies @ Attn. = 15dB.



### 4.3.3 High frequency boost

Figure 7 shows the different Loudness shapes in low & high frequency boost.

Figure 7. Loudness attenuation, fc=2.4kHz



#### 4.3.4 Flat mode

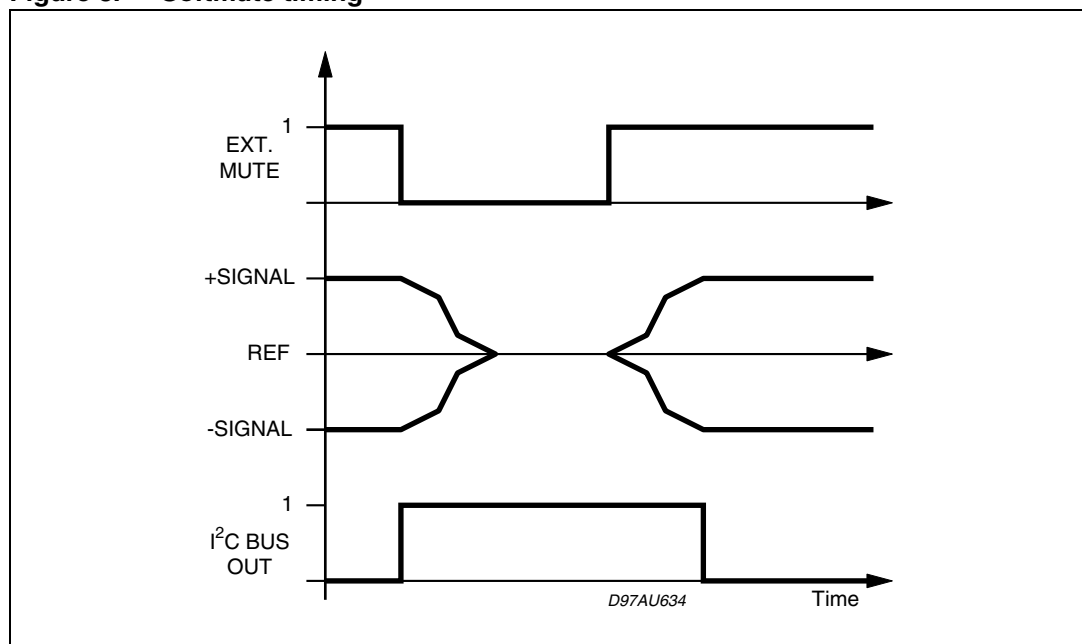
In flat mode the loudness stage works as a 0dB to -15dB attenuator.

### 4.4 SoftMute

The digitally controlled SoftMute stage allows muting/demuting the signal with a I<sup>2</sup>C-bus programmable slope. The mute process can either be activated by the SoftMute pin or by the I<sup>2</sup>C-bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see [Figure 8](#)).

For timing purposes the Bit0 of the I<sup>2</sup>C-bus output register is set to 1 from the start of muting until the end of demuting.

**Figure 8. Softmute timing**



*Note:* A started Mute action is always terminated and could not be interrupted by a change of the mute signal

#### 4.5 SoftStep volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC Offset before the volume-stage or the sudden change of the envelope of the audio signal. With the SoftStep feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5ms or 10ms. The softstep control is described in detail in [Chapter 4.10](#).

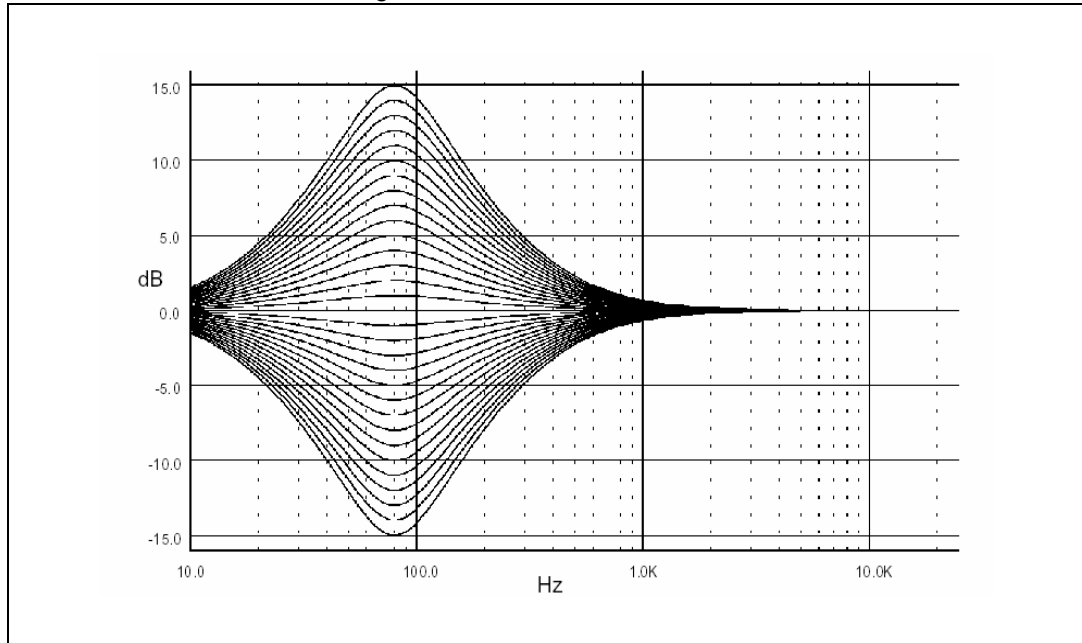
#### 4.6 Bass

There are four parameters programmable in the bass stage:

### 4.6.1 Bass attenuation

Figure 9 shows the attenuation as a function of frequency at a center frequency of 80Hz.

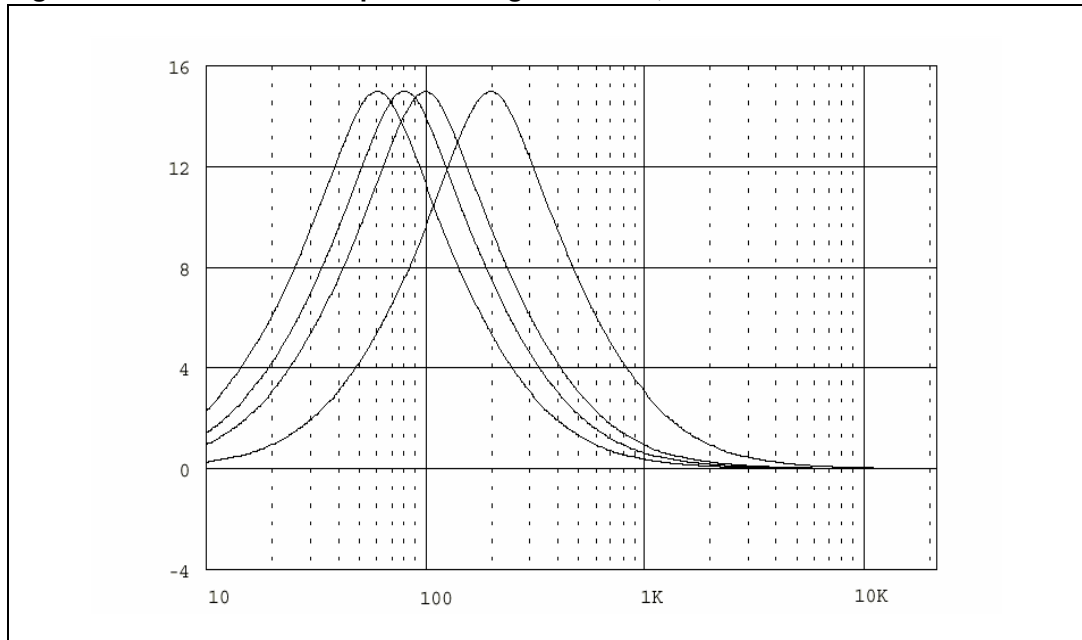
Figure 9. Bass Control @  $f_c = 80\text{Hz}$ ,  $Q = 1$



### 4.6.2 Bass center frequency

Figure 10 shows the four possible center frequencies 60, 80, 100 and 200Hz.

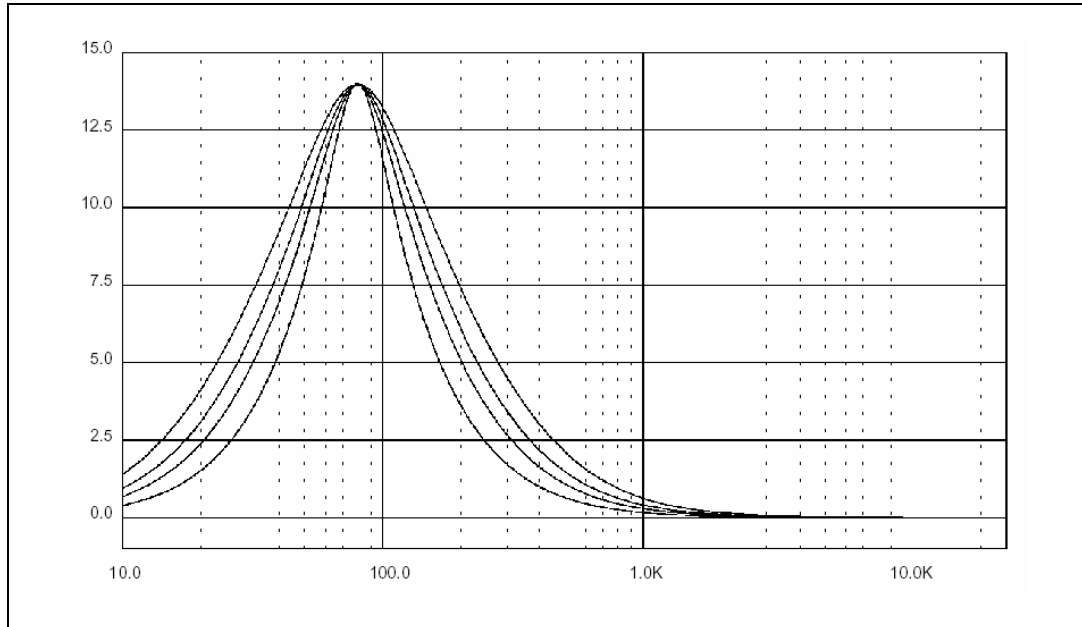
Figure 10. Bass center frequencies @ gain = 14dB,  $Q = 1$



### 4.6.3 Bass quality factors

Figure 11 shows the four possible quality factors 1, 1.25, 1.5 and 2.

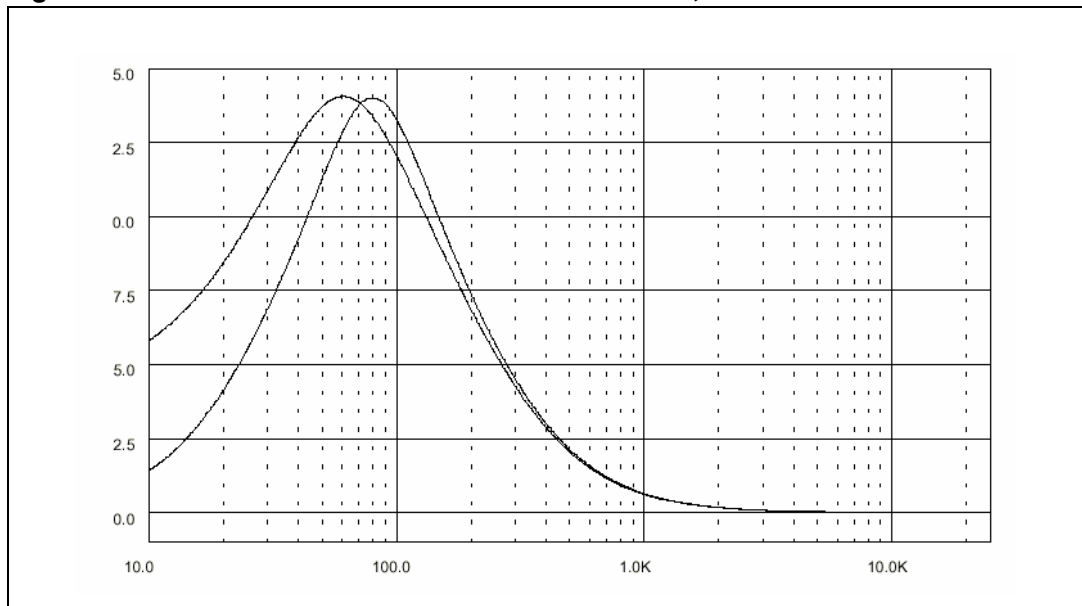
Figure 11. Bass quality factors @ gain = 14dB, fC = 80Hz



### 4.6.4 DC mode

In this mode the DC gain is increased by 4.4dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.

Figure 12. Bass normal and DC mode @ Gain = 14dB, fc = 80Hz



The center frequency, Q and DC-mode can be set fully independently.

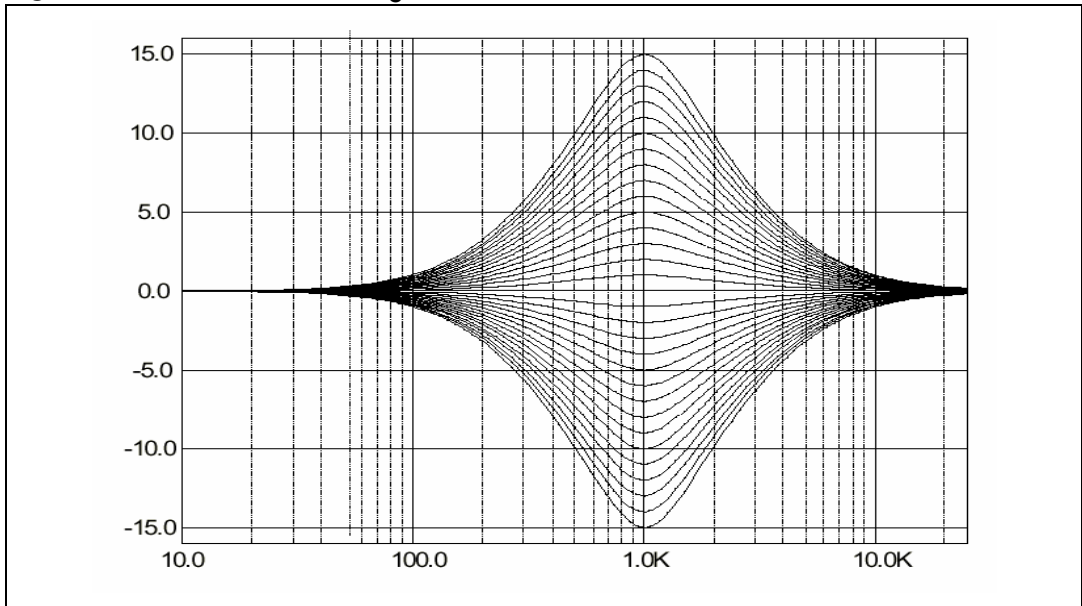
## 4.7 Middle

There are three parameters programmable in the middle stage:

### 4.7.1 Middle attenuation

*Figure 13* shows the attenuation as a function of frequency at a center frequency of 1kHz.

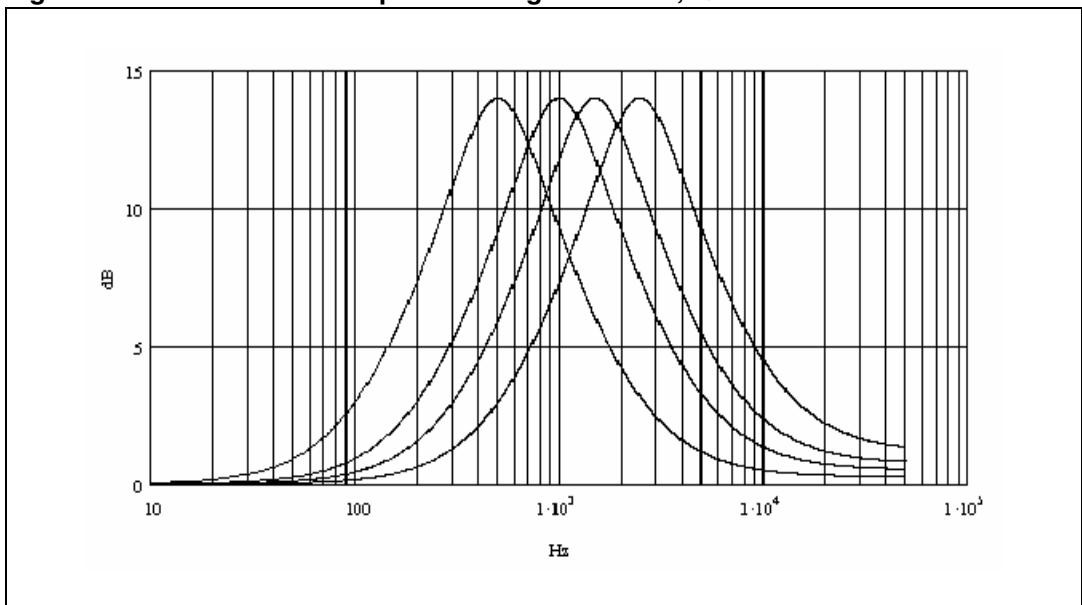
**Figure 13. Middle control @  $f_C = 1$  kHz,  $Q = 1$**



### 4.7.2 Middle center frequency

*Figure 14* shows the four possible center frequencies 500Hz, 1kHz, 1.5kHz and 2.5kHz.

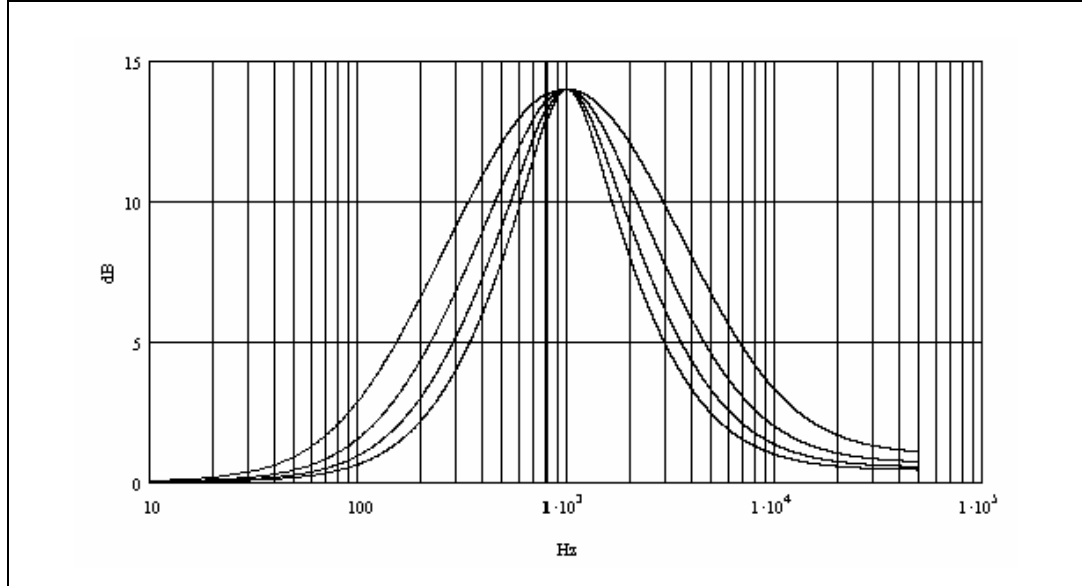
**Figure 14. Middle center frequencies @ gain = 14dB,  $Q = 1$**



### 4.7.3 Middle quality factors

Figure 15 shows the four possible quality factors 0.5, 0.75, 1 and 1.25.

Figure 15. Middle quality factors @ gain = 14dB,  $f_c = 1\text{kHz}$



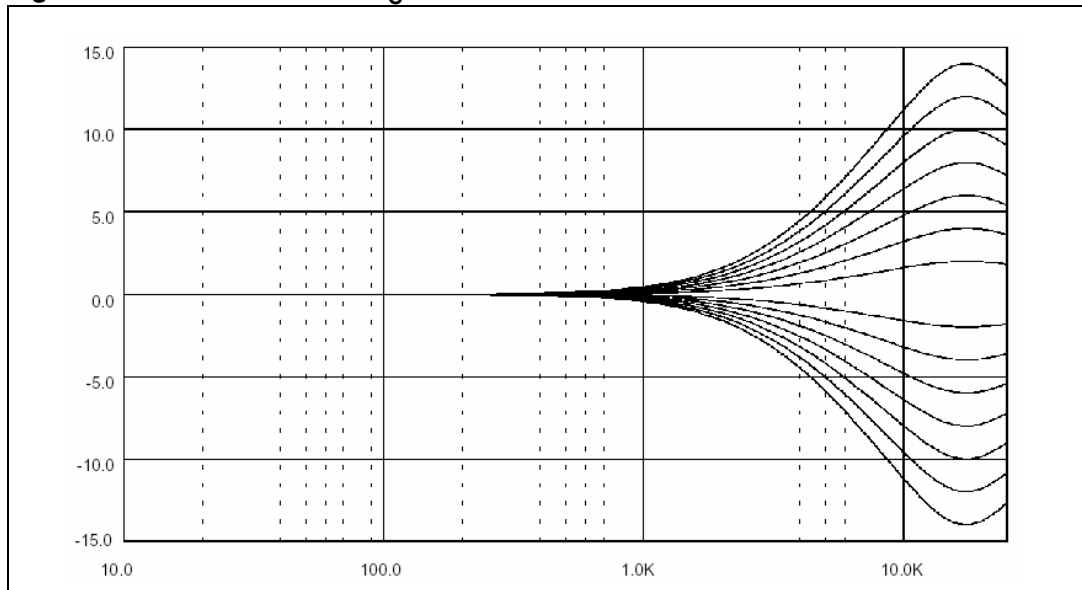
## 4.8 Treble

There are two parameters programmable in the treble stage:

### 4.8.1 Treble attenuation

Figure 16 shows the attenuation as a function of frequency at a center frequency of 17.5kHz

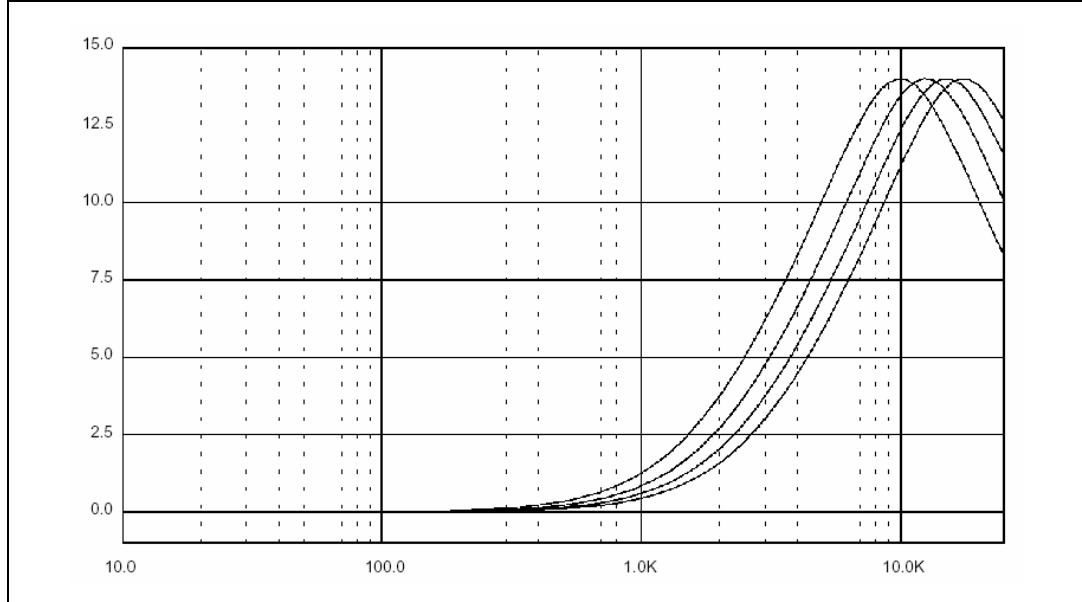
Figure 16. Treble Control @  $f_c = 17.5\text{kHz}$ .



### 4.8.2 Treble center frequency

Figure 17 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5kHz.

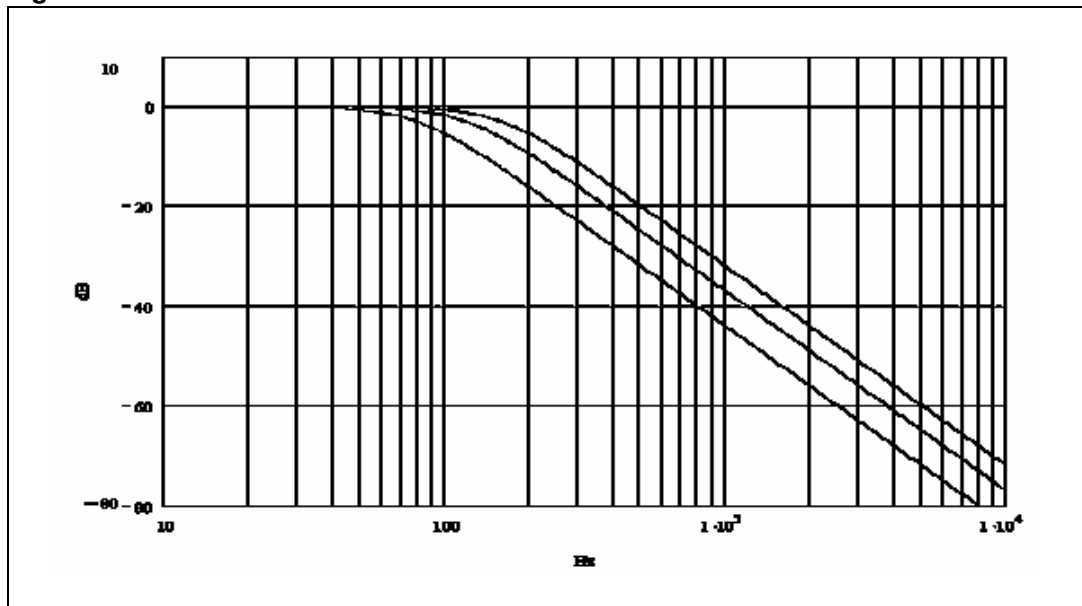
Figure 17. Treble center frequencies @ gain = 14dB



### 4.9 Subwoofer Filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (80 / 120 / 160Hz). The output phase can be selected between 0deg and 180deg. The input of subwoofer takes signal from bass filter output or output of input mux.

Figure 18. Subwoofer control



## 4.10 Softstep control

In this device, the softstep function is available for volume, speaker, loudness, treble, middle and bass block. With softstep function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the softstep function is controlled by softstep on/off control bit in the control table. The softstep transient time selection (5ms or 10ms) is common for all blocks and it is controlled by softstep time control bit. The softstep operation of all blocks has a common centralized control. In this case, a new softstep operation can not be started before the completion previous softstep.

There are two different modes to activate the softstep operation. The softstep operation can be started right after I<sup>2</sup>C data sending, or the softstep can be activated in parallel after data sending of several different blocks. The two modes are controlled by the 'act bit' (it is normally bit7 of the byte.) of each byte. When act bit is '0', which means action, the softstep is activated right after the data byte is sent. When the act bit is '1', which means wait, the block goes to wait for softstep status. In this case, the block will wait for some other block to activate the operation. The softstep operation of all blocks in wait status will be done together with the block which activate the softstep. With this mode, all specific blocks can do the softstep in parallel. This avoids waiting when the softstep is operated one by one.

Chip Addr	Sub Addr	0xxxxxxx
-----------	----------	----------

↑ Softstep start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	.....	0xxxxxxx
-----------	----------	----------	----------	-------	----------

↑ Softstep start here for all

1. It is not allowed to cross 0dB with softstep directly. From plus gain to minus gain, it must go to +0dB first, then destination. From minus gain to plus gain, it must go to -0dB first, and then destination.
2. When one block is in 'wait for softstep' status, it is not allowed to send data to this block again before its softstep is completed.
3. To know if there is a softstep in operation, it is possible to monitor the 'busy' signal by I<sup>2</sup>C transmission mode ([Section 5.1.2](#)). When softstep is busy (busy=0), it is better to wait before sending new data until it is free (busy=1).



## 4.11 DC offset detector and level meter option

This device provide DC offset detector function and level meter function option. In one specific application, only one of the function can be used. The configuration of the function is controlled by I<sup>2</sup>C bus (Byte3 Bit7).

When the device uses DC offset detector function, Pin22, Pin27 and Pin28 are used as WinTC, DCErr and WinIN for DC offset detector. When it is configured as level meter, DCErr becomes level meter output. In the mean time, WinIN is used as beep input (Mono single-ended input for mixing), and WinTC becomes a reference voltage output (4V external DC voltage or 3.3V internal reference voltage).

**Caution:** DC offset detector and level meter / Vref output / Beep / (mono single sided input) can not be used at the same time.

## 4.12 DC offset detector

Using the DC offset detection circuit ([Figure 19](#)) an offset voltage difference between the audio power amplifier and the APR's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the APR. The WinIn-input has an internal pull-up resistor connected to 5.5Volts. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin are implemented, with external capacitors introducing the same delay  $\tau = 7.5k\Omega * C_{ext}$  as the AC-coupling between the APR and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

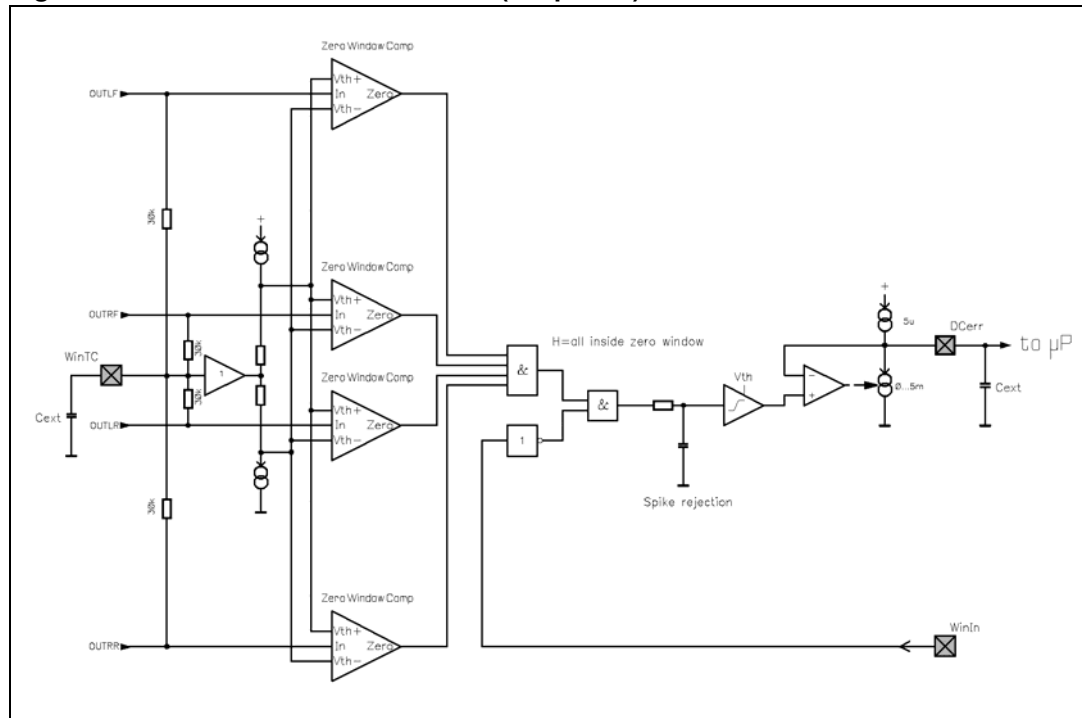
For electrical characteristics see [Chapter 3 on page 9](#).

A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

- a) Front and rear outputs are inside zero crossing windows.
- b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

Figure 19. DC offset detection circuit (simplified)



### 4.13 Level meter

In case of not using DC offset detector, the three pins used for this function can be configured as other functions. Pin27 (DC\_Err / LMOUT) then becomes the level meter output. The level meter block takes signal after main input selector and mix signal into mono, then rectify the signal and detect the peak of the signal. The output stage of level meter removes the DC voltage of the signal and the output voltage level shows exactly the  $V_{peak}$  of signal. Since the discharge time constant of the level meter is quite slow, it is necessary to reset level meter regularly (with I<sup>2</sup>C bus control Byte3 Bit6) to get correct peak information of the signal.

### 4.14 Output gain control

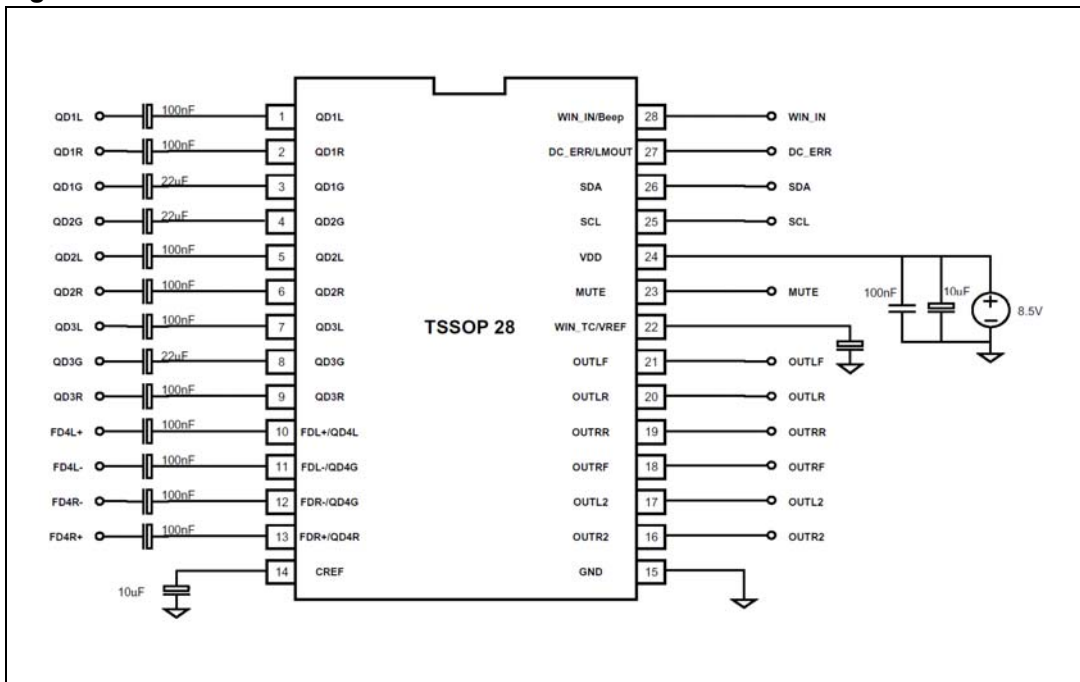
The output stage of the device can provide a option to have additional 1dB gain in order to boost the maximum output level to 2.2V<sub>rms</sub> with maximum 1% distortion.

### 4.15 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I<sup>2</sup>C subaddress byte and bit D0 of the testing-audioprocessor byte, several internal signals are available at the QD1L pin. In this mode, the input resistance of 100kOhm is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

### 4.16 Test circuit (3 x QD + 1 x FD + DC offset detector)

Figure 20. Test circuit



## 5 I<sup>2</sup>C Bus specification

### 5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 500kbits/s
- 3.3V logic compatible

#### 5.1.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P
---	---	---	---	---	---	---	---	-----	-----	----	---	----	----	----	----	----	----	-----	------	-----	---

S = Start

R/W = "0" -> Receive Mode (Chip can be programmed by μP)

"1" -> Transmission Mode (Data could be received by μP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

#### 5.1.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	X	BZ	SM	ACK	P
---	---	---	---	---	---	---	---	-----	-----	---	---	---	---	---	---	---	----	----	-----	---

SM = Soft mute activated for main channel

BZ = Softstep Busy ('0' = Busy)

X = Not Used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

#### 5.1.3 Reset condition

A Power-On-Reset is invoked if the supply voltage is below than 3.5V. After that the registers are initialized to the default data written in following tables.

Table 9. Subaddress (receive mode)

MSB								LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0		
0								Testing Mode	
1								Off	
	x							On	
								Not Used	
								Auto Increment Mode	
		0						Off	
		1						On	
			0	0	0	0	0	Input Configuration / Main Source Selector	
			0	0	0	0	1	2 <sup>nd</sup> Source Selector / Direct Path	
			0	0	0	1	0	Mixing Source / Mixing Gain	
			0	0	0	1	1	Mix Control / Level Meter / DC Offset Detector Config	
			0	0	1	0	0	Soft Mute / Others	
			0	0	1	0	1	Soft Step I	
			0	0	1	1	0	Soft Step II / DC-detector	
			0	0	1	1	1	Loudness	
			0	1	0	0	0	Volume / Output Gain	
			0	1	0	0	1	Treble	
			0	1	0	1	0	Middle	
			0	1	0	1	1	Bass	
			0	1	1	0	0	Subwoofer / Middle / Bass	
			0	1	1	0	1	Speaker Attenuator Left Front	
			0	1	1	1	0	Speaker Attenuator Right Front	
			0	1	1	1	1	Speaker Attenuator Left Rear	
			1	0	0	0	0	Speaker Attenuator Right Rear	
			1	0	0	0	1	Subwoofer Attenuator Left	
			1	0	0	1	0	Subwoofer Attenuator Right	
			1	0	0	1	1	Testing Audio Processor 1	
			1	0	1	0	0	Testing Audio Processor 2	

## 5.2 Data byte specification

The default power on status of the registers is written with underline.

**Table 10. Input configuration / main selector (0)**

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	Main source selector
					0	0	1	IN0
					0	1	0	<u>IN1</u>
					0	1	1	IN2
					1	0	0	IN3
					1	0	1	IN4
					1	1	0	IN5
					1	1	1	IN6
				0				MD1/2 configuration for main selector
				1				MD1
								<u>MD2</u>
			0					Main source input gain select
			1					0dB
								<u>3dB</u>
0	0	0						Input configuration
0	0	1						CFG0
0	1	0						CFG1
0	1	1						CFG2
1	0	0						CFG3
1	0	1						CFG4
1	1	0						CFG5
1	1	1						CFG6
1	1	1						<u>CFG7</u>

**Note:** For detailed input source and input stage configuration, please refer to [Section 4.1](#).

Table 11. 2<sup>nd</sup> Source selector / direct path (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	2 <sup>nd</sup> Source Selector IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7
				0 1				MD1/2 Configuration for 2 <sup>nd</sup> Selector MD1 MD2
			0 1					2 <sup>nd</sup> Source Input Gain Select 0dB 3dB
		0 1						QD2 Bypass (Front) on Off
	0 1							QD3 Bypass (Rear) on Off
0 1								QD4 Bypass (Subwoofer) on Off

**Note:** For detailed input source and input stage configuration, please refer to [Section 4.1](#).  
To active QD3 Bypass (Rear) function, it needs to set Byte3\_D4 to "Direct Path / 2<sup>nd</sup> Source" also.

Table 12. Mixing source / mixing gain (2)

MSB					LSB			Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	Mixing Source Selector
					0	0	1	IN0
					0	1	0	IN1
					0	1	1	IN2
					1	0	0	IN3
					1	0	1	IN4
					1	1	0	IN5
					1	1	1	IN6
					1	1	1	IN7
								Mixing Attenuator
0	0	0	0	0				0dB
0	0	0	0	1				-1dB
0	0	0	1	0				-2dB
0	0	0	1	1				-3dB
0	0	1	0	0				-4dB
0	0	1	0	1				-5dB
0	0	1	1	0				-6dB
0	0	1	1	1				-7dB
0	1	0	0	0				-8dB
0	1	0	0	1				-9dB
0	1	0	1	0				-10dB
0	1	0	1	1				-11dB
0	1	1	0	0				-12dB
0	1	1	0	1				-13dB
0	1	1	1	0				-14dB
0	1	1	1	1				-15dB
1	0	0	0	0				-16dB
1	0	0	0	1				-17dB
1	0	0	1	0				-18dB
1	0	0	1	1				-19dB
1	0	1	0	0				-20dB
1	0	1	0	1				-21dB
1	0	1	1	0				-22dB
1	0	1	1	1				-23dB
1	1	0	0	0				-24dB
1	1	0	0	1				-25dB
1	1	0	1	0				-26dB
1	1	0	1	1				-27dB
1	1	1	0	0				-28dB
1	1	1	0	1				-29dB
1	1	1	1	0				-30dB
1	1	1	1	1				-31dB



Table 13. Mix control / level meter / dc offset detector configure (3)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Mix To Front Left On <u>Off</u>
						0 1		Mix To Front Right On <u>Off</u>
					0 1			Mix To Rear Left On <u>Off</u>
				0 1				Mix To Rear Right On <u>Off</u>
			0 1					Rear Speaker Input Configuration Direct Path / 2 <sup>nd</sup> Source <u>Main Signal</u>
		0 1						Reference Output Select Internal Vref (3.3V) <u>External Vref (4V)</u>
	0 1							Level Meter Reset Normal <u>Reset</u>
0 1								DC Offset Detector / Level Meter Config Level Meter <u>DC Offset Detector</u>

Table 14. Soft mute / others (4)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Soft Mute On <u>Off</u>
						0 1		Pin Influence for Mute <u>Pin and IIC</u> IIC
				0 0 1 1	0 1 0 1			Soft Mute Time 0.48ms 0.96ms 7.68ms 15.36ms
			0 1					Subwoofer Input Configuration Input Mux <u>Bass Output</u>
		0 1						Subwoofer Enable (OUTL3 & OUTF3) On <u>Off</u>
	0 1							Fast Charge On <u>Off</u>
0 1								Anti-Alias Filter On <u>Off (bypass)</u>

Table 15. SoftStep I (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Loudness Soft Step On <u>Off</u>
						0 1		Volume Soft Step On <u>Off</u>
					0 1			Treble Soft Step On <u>Off</u>
				0 1				Middle Soft Step On <u>Off</u>
			0 1					Bass Soft Step On <u>Off</u>
		0 1						Speaker LF Soft Step On <u>Off</u>
	0 1							Speaker RF Soft Step On <u>Off</u>
0 1								Speaker LR Soft Step On <u>Off</u>

Table 16. SoftStep II / DC detector (6)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Speaker RR Soft Step on <u>off</u>
						0 1		Subwoofer Left Soft Step on <u>off</u>
					0 1			Subwoofer Right Soft Step on <u>off</u>
				0 1				Soft Step Time 5ms <u>10ms</u>
		0 0 1	0 1 0					Zero-comparator Window size $\pm 100\text{mV}$ $\pm 75\text{mV}$ $\pm 50\text{mV}$
0 0 1 1	0 1 0 1							Spike rejection time constant 11 $\mu\text{s}$ 22 $\mu\text{s}$ 33 $\mu\text{s}$ <u>44 <math>\mu\text{s}</math></u>

Table 17. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	Attenuation 0dB
				0	0	0	1	-1dB
				:	:	:	:	:
				1	1	1	0	<u>-14dB</u>
				1	1	1	1	-15dB
		0	0					Center Frequency Flat
		0	1					400Hz
		1	0					800Hz
		1	1					<u>2400Hz</u>
	0							High Boost on
	1							off
0								Soft Step Action act
1								wait

Table 18. Volume / output gain (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			0	0	0	0	0	Gain/Attenuation -15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	<u>+1dB</u>
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
		x						Not used
	0							Output Gain 1dB
	1							<u>0dB</u>
0								Soft Step Action act
1								wait

Table 19. Treble filter (9)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
			0	0	0	0	0	Gain/Attenuation -15dB	
			0	0	0	0	1	-14dB	
			:	:	:	:	:	:	
			0	1	1	1	0	-1dB	
			0	1	1	1	1	0dB	
			1	1	1	1	1	0dB	
			1	1	1	1	0	<u>+1dB</u>	
			:	:	:	:	:	:	
			1	0	0	0	1	+14dB	
			1	0	0	0	0	+15dB	
	0	0						Treble Center Frequency 10.0kHz	
	0	1						12.5kHz	
	1	0						15.0kHz	
	1	1						<u>17.5kHz</u>	
0								Soft Step Action act	
1								<u>wait</u>	

Table 20. Middle filter (10)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
			0	0	0	0	0	Gain/Attenuation -15dB	
			0	0	0	0	1	-14dB	
			:	:	:	:	:	:	
			0	1	1	1	0	-1dB	
			0	1	1	1	1	0dB	
			1	1	1	1	1	0dB	
			1	1	1	1	0	<u>+1dB</u>	
			:	:	:	:	:	:	
			1	0	0	0	1	+14dB	
			1	0	0	0	0	+15dB	
	0	0						Middle Q Factor 0.5	
	0	1						0.75	
	1	0						1	
	1	1						<u>1.25</u>	
0								Soft Step Action act	
1								<u>wait</u>	

Table 21. Bass filter (11)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
			0	0	0	0	0	Gain/Attenuation -15dB	
			0	0	0	0	1	-14dB	
			:	:	:	:	:	:	
			0	1	1	1	0	-1dB	
			0	1	1	1	1	0dB	
			1	1	1	1	1	0dB	
			1	1	1	1	0	<u>+1dB</u>	
			:	:	:	:	:	:	
			1	0	0	0	1	+14dB	
			1	0	0	0	0	+15dB	
	0	0						Bass Q Factor 1.0	
	0	1						1.25	
	1	0						1.5	
	1	1						<u>2.0</u>	
0								Soft Step Action act	
1								<u>wait</u>	

Table 22. Subwoofer / middle / bass (12)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0	Subwoofer Cut-off Frequency flat	
						0	1	80Hz	
						1	0	<u>120Hz</u>	
						1	1	160Hz	
					0			Subwoofer Output Phase 180 deg	
					1			<u>0 deg</u>	
			0	0				Middle Center Frequency 500Hz	
			0	1				1000Hz	
			1	0				1500Hz	
			1	1				<u>2500Hz</u>	
	0	0						Bass Center Frequency 60Hz	
	0	1						80Hz	
	1	0						100Hz	
	1	1						<u>200Hz</u>	
0								Bass DC Mode on	
1								<u>off</u>	

**Table 23. Speaker attenuation (LF/RF/LR/RR) (13-16)**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	Gain/Attenuation
	0	0	0	0	0	0	1	0dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	0dB
	0	0	1	0	0	0	0	0dB
	0	0	1	0	0	0	1	-1dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78dB
	1	0	1	1	1	1	1	-79dB
	1	1	x	x	x	x	x	<u>mute</u>
0								Soft Step Action
1								act <u>wait</u>

**Table 24. Subwoofer attenuation (subwoofer L/subwoofer R) (17-18)**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	Gain/Attenuation
	0	0	0	0	0	0	1	+0dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+1dB
	0	0	1	0	0	0	0	+15dB
	0	0	1	0	0	0	1	-0dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-1dB
	1	0	1	1	1	1	1	-78dB
	1	0	1	1	1	1	1	-79dB
	1	1	x	x	x	x	x	<u>mute</u>
0								Soft Step Action
1								act <u>wait</u>



Table 25. Testing audio processor 1 (19)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Audio Processor Testing Mode <u>off</u> on
			0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1	0 0 0 1 1 0 0 0 0 0 1 1 1 1 1	0 0 1 1 0 0 1 0 1 1 0 1 0 1 1	0 1 0 1 0 0 1 0 1 1 0 1 0 0 0		Test Multiplexer at QD1L <sup>(1)</sup> DCDet Vth High DCDet Vth Low VolumeoutL IntZeroErr InGainL LoudoutL BassoutL MidoutL Ref5V5 VGB1.26 SMCLK TrebleoutL SSCLK Clock200k <u>REQ</u> SDCLK
		0 1						Clock Fast Mode <sup>(2)</sup> on <u>Off</u>
	0 1							Clock Source <sup>(2)</sup> external (at mute pin) <u>Internal (200kHz)</u>
x								Not Used

1. The control bit needs both I2C test mode on & sub-address test mode on.

2. The control bit does not depend on test mode.

Table 26. Testing audio processor 2 (20)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Test Architecture <sup>(1)</sup> <u>normal</u> Split
						0 1		Oscillator Clock <sup>(2)</sup> 400kHz 800kHz
					0 1			Softstep Curve <sup>(2)</sup> S-Curve Linear Curve
			0 0 1 1	0 1 0 1				Manual Set Busy Signal <sup>(1)</sup> Auto Auto 0 1
			0 0 1 1	0 1 0 1				Request for Clk Generator <sup>(1)</sup> Allow Allow Stopped Stopped
x	x	x						Not Used

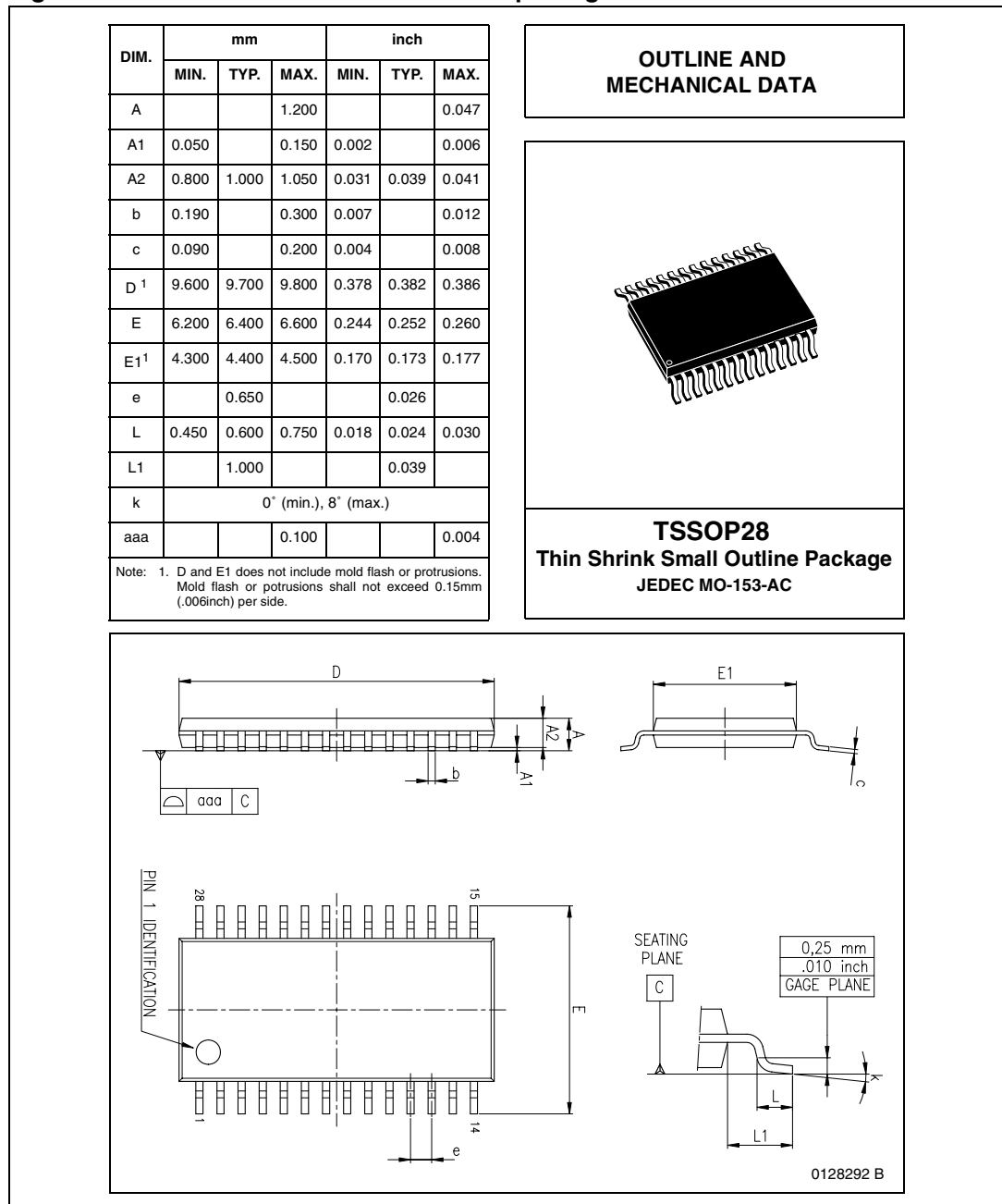
1. The control bit needs sub-address test mode on
2. The control bit does not depend on test mode.

## 6 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK<sup>®</sup> packages. ECOPACK<sup>®</sup> packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 21. TSSOP28 mechanical data and package dimensions**



## 7 Revision history

**Table 27. Document revision history**

Date	Revision	Changes
16-Jul-2007	1	Initial release.
7-Jan-2007	2	Added and updated the values on the <a href="#">Table 5: Electrical characteristics</a> . Document status promoted from preliminary data to datasheet.

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