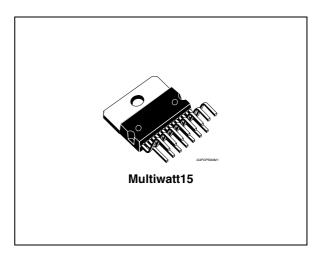


Dual bridge MOSFET power amplifier for 24 V systems

Datasheet - production data

Features

- Multipower BCD technology
- 24 V battery operation
- MOSFET output power stage
- High output power capability
 - 2 x 20 W/4 Ω @ 24 V, 1 kHz; 10 %
- Minimized external components
 - No decoupling capacitors
 - No bootstrap capacitor
 - No external compensation
 - Internally fixed gain
- Standby function
- Mute function
- Diagnostic pin for:
- clip detector (THD 2 %)
 - short circuit detection
 - thermal protection
- Output DC offset detection
- Protections:
 - 60 V load dump
 - Overrating chip temperature
 - Out short circuit protection (to GND, Vcc and across the load)
 - ESD



Description

The TDA7576B is a dual bridge power amplifier with MOSFET output power stages. It has been specifically designed for 24 V power supply systems making it compatible with truck/bus applications.

The feedback topology allows excellent distortion performances and the integrated buffer minimizes the need for external components. The fully complementary P-channel/N-channel output structure allows rail-to-rail output voltage swing minimizing saturation losses.

The TDA7576B integrates a DC offset detector, a clipping detector and a diagnostic output.

Table 1. Device summary

Order code	Package	Packing	
TDA7576B	Multiwatt15	Tube	

Contents TDA7576B

Contents

1	Bloc	k and application diagrams
2	Pins	description
3	Elec	trical specification
	3.1	Absolute maximum ratings 7
	3.2	Thermal data
	3.3	Electrical characteristics
	3.4	Electrical characteristics curves
4	Princ	ciple of operation
5	Powe	er dissipation computation13
6	Fund	ctional description14
	6.1	Diagnostics pins description
	6.2	Thermal protections
7	Pack	age information
8	Revi	sion history

TDA7576B List of tables

List of tables

Table 1.	Device summary
Table 2.	Pins information
	Absolute maximum ratings
Table 4.	Thermal data
Table 5.	Electrical characteristics
Table 6.	Document revision history

List of figures TDA7576B

List of figures

4/17

Figure 1.	Block diagram	5
Figure 2.	Application diagram	5
Figure 3.	Pins connection (top view)	6
Figure 4.	Audio section waveforms	9
Figure 5.	Quiescent current vs. supply voltage	9
Figure 6.	Output power vs. supply voltage ($R_L = 4 \Omega$)	9
Figure 7.	Distortion vs. output power ($R_L = 4 \Omega$)	10
Figure 8.	Crosstalk vs. frequency	10
Figure 9.	Total power dissipation and efficiency vs. Po (RL = 4Ω)	10
Figure 10.	Power dissipation vs. average Po (audio program simulation, 4Ω)	10
Figure 11.	Amplifier structure	11
Figure 12.	Thermal protection diagram	14
Figure 12	Multiwatt 15 (vortical) mochanical data and package dimensions	15

1 Block and application diagrams

Figure 1. Block diagram

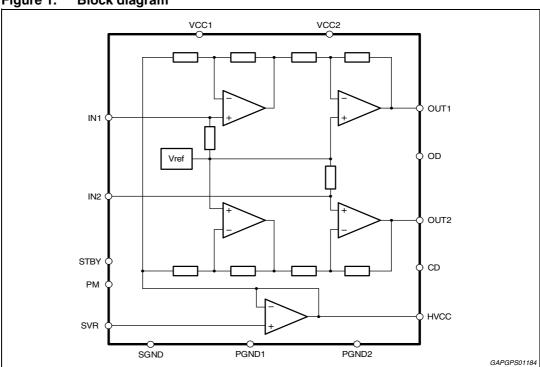
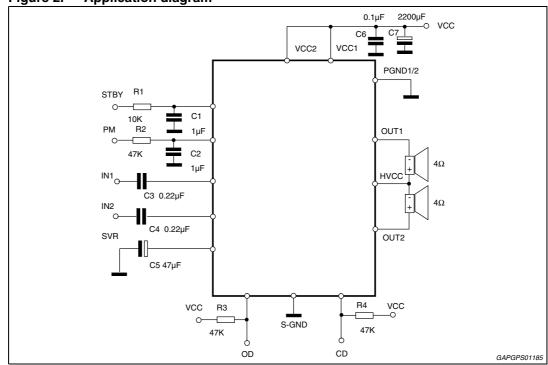


Figure 2. Application diagram



Pins description TDA7576B

2 Pins description

Figure 3. Pins connection (top view)

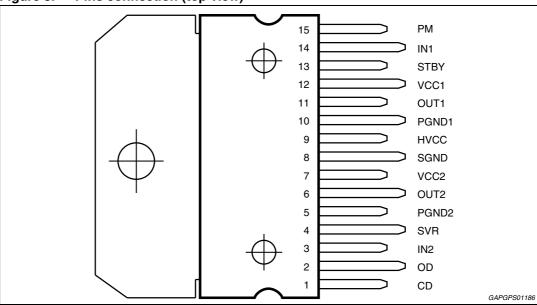


Table 2. Pins information

	· ····· ······························			
Pin number	Pin name	Description	Туре	Max. applicable voltage
1	CD	Clip Detector	Open collector output	-0.3/V _S
2	OD	Offset Detector	Open collector output	-0.3/V _S
3	IN2	Left channel input	Input	-0.3/5 V
4	SVR	SVR	Output	-0.3/20 V
5	PGND2	Power ground 2	Ground	-0.3/0.3
6	OUT2	Left channel output	Output	N.A.
7	VCC2	Supply voltage 2	Supply	-0.3/V _S
8	SGND	Signal ground	Ground	-0.3/0.3
9	HVCC	Half supply voltage buffer	Output	N.A.
10	PGND1	Power ground 1	Ground	-0.3/0.3
11	OUT1	Right channel output	Output	N.A.
12	VCC1	Supply voltage 1	Supply	-0.3/V _S
13	STBY	STBY pin	Input	-0.3/V _S
14	IN1	Right channel input	Input	-0.3/5 V
15	PM	Play/Mute pin	Input	-0.3/5 V

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _S	Operating supply voltage	32	V
V _{SPK}	Peak supply voltage (t = 50 ms) not operating	60	V
V _{DCS}	Not operating max. DC supply voltage	36	V
PGND, SGND	Ground pins	-0.3 to 0.3	V
V _{CC}	Supply voltage	-0.3 to V _s	V
SVR	Supply voltage rejection filter	-0.3 to 20	V
IN1, IN2	Inputs	-0.3 to 5	V
OD, CD	Offset detector, clip detector pins	-0.3 to V _s	V
PM	Play-mute pin	-0.3 to 5	V
P _{tot} ⁽¹⁾	Power dissipation at T _{case} = 85 °C	85	W
T _{stg} , T _j	Storage and junction temperature range	-40 to 150	°C

^{1.} Refer to Section 5 for detailed description of this value.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal resistance junction-to-case Max.	2	°C/W

3.3 Electrical characteristics

Refer to the test circuit; V_S = 28 V; R_L = 4 Ω , T_{amb} = 25 °C, f = 1 kHz, R_g = 0, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
General						
V _S	Supply voltage	-	8	-	32	V
Iq	Total quiescent current	$R_L = \infty$	-	90	130	mA
I _{ST-BY}	Standby current consumption	0 < V _{ST_BY} < 1.2 V	-	-	10	μΑ
R _{IN}	Input impedance	-	50	55	-	kΩ

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit		
V _{OS}	Offset voltage	-	-100	-	+100	mV		
V _{dth}	Dump threshold	-	36	37.5	39	V		
I _D	Dump current	V _S = 60 V	-	18	40	mA		
Audio sect	ion							
		THD = 1 %	20	22	-			
P _o	Output power	THD = 10 %	25	28	-	W		
P _{o max.}	Max. output power ⁽¹⁾	-	43	45	-	W		
THD	Distortion	P _o = 4 W; f = 1 kHz	-	0.05	0.1	%		
СТ	Cross talk	f = 1 kHz; P ₀ = 4 W f = 10 kHz; P ₀ = 4 W	50 45	65 60	-	dB dB		
G _v	Voltage gain		25	26	27	dB		
E _{NO}	Output noise voltage ⁽²⁾	Amplifier in Mute	-	60	100	μV		
SVR	Supply voltage rejection	f = 1 kHz; V _R = 1 Vpk	-	50	-	dB		
Standby								
V _{SB IN}	Standby input threshold voltage	-	-	-	1.2	V		
V _{SB OUT}	Standby output threshold voltage	-	2.6	-	-	V		
ASB	Standby attenuation	-	90	110	-	dB		
I _{PIN}	Standby pin current	Play mode	-1	-	1	μΑ		
Mute pin								
A _M	Mute attenuation	-	90	100	-	dB		
V _{M IN}	Mute input threshold voltage	(Amp: Mute)	-	-	1.2	٧		
V _{M OUT}	Mute output threshold voltage	(Amp: Play)	2.6	-	-	V		
V _{AM in}	V _S automute threshold	Amp: play, attenuation = -3 dB V _{out} = 2 Vrms; f = 1 kHz	6.7	7.25	8	V		
Clipping detector ⁽³⁾								
CD _{THD}	Clipping detector THD level	10 V < V _s < 32 V	-	2	-	%		
CD _{SAT}	Clipping detector saturation voltage	10 V < V _s < 32 V; Cd; On; I _{CD} = 1 mA	-	-	0.2	V		
Offset detector								
O _D	Offset detector	Power amp. in play AC input = 0	±1	±2	±3	V		
V _{OFF_SAT}	Offset detector saturation voltage	V_o - V_{hvcc} > 3 V, I_{OD} = 1 mA	-	-	0.2	V		

^{1.} Square wave input.

^{2. 22} Hz to 22 kHz.

^{3.} Clip detector not guaranteed for $V_s < 10 \text{ V}$.

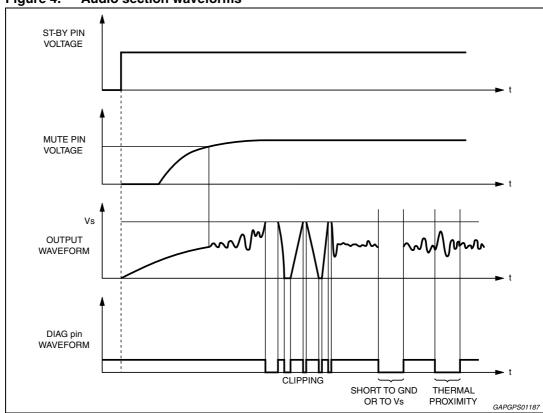


Figure 4. Audio section waveforms

3.4 Electrical characteristics curves

Figure 5. Quiescent current vs. supply voltage

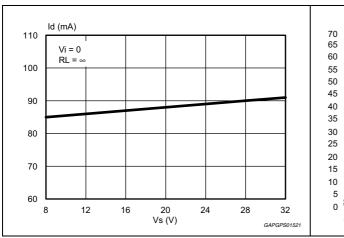


Figure 6. Output power vs. supply voltage ($R_L = 4 \Omega$)

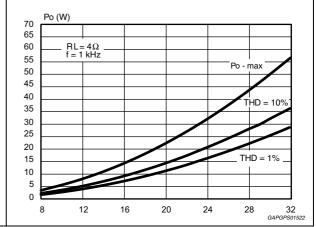
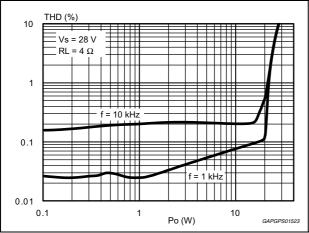


Figure 7. Distortion vs. output power $(R_L = 4 \Omega)$

Figure 8. Crosstalk vs. frequency



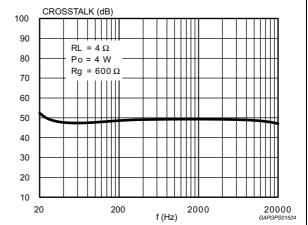
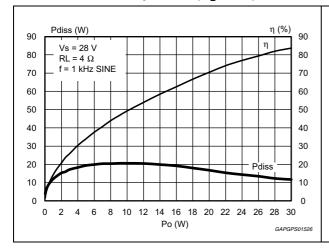
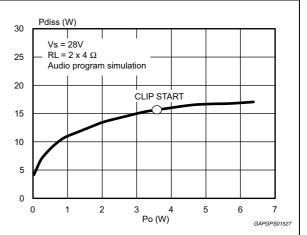


Figure 9. Total power dissipation and efficiency vs. Po $(R_1 = 4 \Omega)$

Figure 10. Power dissipation vs. average Po (audio program simulation, 4 Ω)



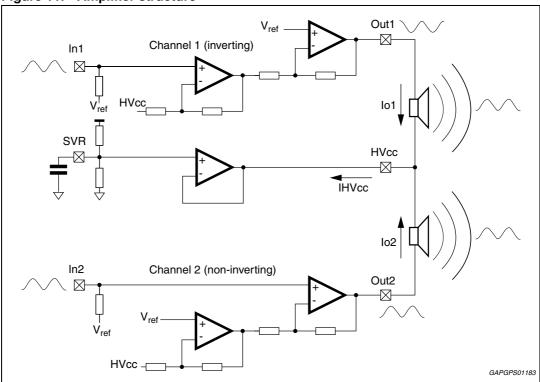


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4 Principle of operation

The TDA7576B is an innovative stereo audio amplifier meant for 24 V battery vehicles. The amplifier works in a single-ended configuration without the large decoupling capacitors on the outputs normally required by the s.e. topology. Its principle of operation is depicted in *Figure 11*.

Figure 11. Amplifier structure



Channel 1 is electrically inverting its input signal whereas channel 2 is not; if the speakers are connected with the positive pole of speaker 2 connected to Out2 and the negative pole of speaker 1 connected to Out1, then the two channels both behave as non-inverting. Speaker 1 and speaker 2 have one terminal in common and further connected to a half Vcc (HVCC) buffer.

If the signals at In1 and In2 are identical, then the voltage at Out1 and Out2 is identical in magnitude but inverted (Out1 = -Out2), and the current flowing through speaker 1 is all coming from speaker 2, with no current going into the HVCC buffer. If the signal at In1 is not identical to that at In2, then the signal at the two outputs will not be identical either, and some current will flow into or out of the HVCC buffer, keeping the voltage at HVCC constant.

This structure allows therefore the amplifier to operate in a single-ended configuration with no need for decoupling capacitors.

Mathematically this can be expressed as:

$$V_{L1} = -G * Vin1$$

$$V_{L2} = +G * Vin2$$

$$I_{HVCC} = Io1 + Io2 = V_{L1}/RL + V_{L2}/RL = G (Vin2 - Vin1) / R_L$$

where $V_{L1,2}$ is the voltage across speaker 1 or 2, G is the gain of the amplifiers and RL is the load resistance (supposed identical for the two speakers).

In the common practice the two channels of the amplifier are used for the left and the right audio parts of the stereo signal, and therefore the two outputs are not identical. This means that it is never mathematically true that all the current into one speaker comes from the other speaker, so the HVcc buffer will always have to provide a certain amount of difference current.

Apart from the fact that the left and the right audio channels are not identical unless the program is monophonic, other reasons why the HVcc buffer has to provide current are: imbalance in the level of the L and the R channel, equalization-induced delay in one channel compared to the other.

The current provided by the HVCC buffer leads to non-negligible power dissipation inside the IC: this should be added to power dissipation the output stages 1 and 2. It is necessary to keep this additional dissipation in mind when dimensioning the car-radio heat sink.

5 Power dissipation computation

The instantaneous power dissipated by each output stage is given by the formula below:

$$P_{D1,2}(t) = 1/R_L |V_{L1,2}(t)| (Vcc/2 - |V_{L1,2}(t)|)$$

with $V_{L1,2}(t)$ being the output signal on each of the two channels $(V_{L1,2}(t) = G * V_{in1,2}(t))$.

If the two input signals are not identical, as seen in *Section 4* a current IHVcc flows into or out of the half Vcc buffer; this current causes dissipation within the HVcc buffer given by:

$$\mathsf{P}_{\mathsf{DHVCC}}(\mathsf{t}) = \mathsf{Vcc}/(2\mathsf{R}_\mathsf{L}) \mid \mathsf{V}_{\mathsf{L2}}(\mathsf{t}) - \mathsf{V}_{\mathsf{L1}}(\mathsf{t}) \mid$$

which is obviously 0 when the two channels have identical signals.

The total instantaneous power dissipation inside the TDA7576B is therefore given by:

$$P_{dtot}(t) = P_{D1}(t) + P_{D2}(t) + P_{DHVCC}(t).$$

The dimensioning of the heat sink of the system must take into consideration these three components.

For more details on power dissipation and recommendations on heat-sink characteristics computation, please refer to the complete application note related to this subject.

6 Functional description

6.1 Diagnostics pins description

TDA7576B includes an offset detector pin and a clip detector and diagnostic pin.

DC offset detector is intended to avoid that an anomalous DC offset on the inputs of the amplifier may be multiplied by the gain and result in a dangerous large offset on the outputs. This may lead to speakers damage due to overheating.

The feature works with the amplifier unmuted and no signal at the inputs.

Moreover there is a pin named CD/Diag: the behavior of this pin is showed on Figure 4.

Whenever a failure condition (between thermal warning, output waveform clipping, short circuit to GND or V_{CC}) is verified by the IC the level of this pin goes true (low).

6.2 Thermal protections

Thermal protection function is triggered when junction temperature rises above the normal operating range, thus avoiding chip damaging.

For behavior description, refer to *Figure 4* and *12*. When temperature is reaching thermal warning (T_w = typ 140 °C) the CD/Diag pin is driven low. Thermal foldback begins limiting the audio input to the amplifier stage, this effectively limits the output power capability of the device thus reducing the temperature to acceptable levels without totally interrupting the operation of the device. Thermal mute is temperature when -6 dB output attenuation is reached (typical T_m = 160 °C).

The output power will decrease to the point at which thermal equilibrium is reached. Thermal equilibrium will be reached when the reduction in output power reduces the dissipated power such that the die temperature falls below the thermal foldback threshold.

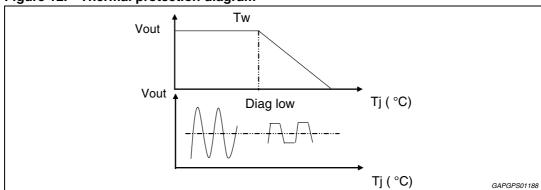


Figure 12. Thermal protection diagram

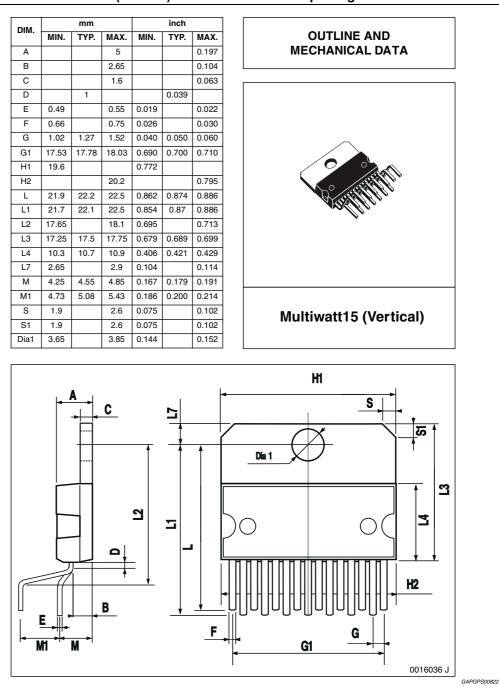
TDA7576B Package information

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

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Figure 13. Multiwatt 15 (vertical) mechanical data and package dimensions



Revision history TDA7576B

8 Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Sep-2012	1	Initial release.
05-Oct-2012 2		Updated Section 1: Block and application diagrams. Updated Section 2: Pins description.
18-Sep-2013	3	Updated Disclaimer.

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