

Car radio multimedia signal processor (CMSP)

Features

- 6-channel multimedia approach
- Fully integrated tone control with notch filter
- 7-band spectrum analyzer

Inputs

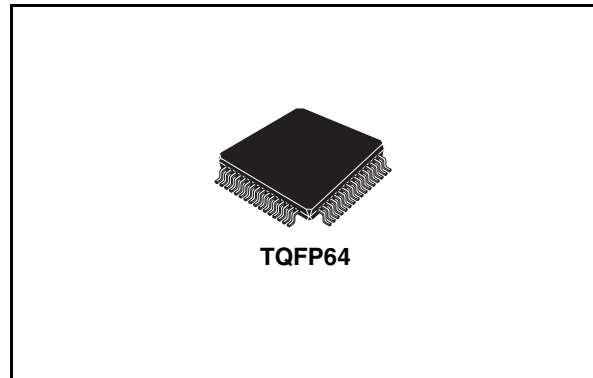
- Three independent signal paths
- Eight single-ended inputs
- Two quasi-differential inputs
- Optional full-differential input
- Level adjust gain-stages
- Independent soft-mute and direct-mute

Outputs

- Three independent signal paths
- Six output channels with soft-step volume
- Output level up to 4VRMS
- Independent soft-mute and direct-mute
- Flexible phone/navigation interrupts
- High-pass & subwoofer low-pass filters

Digital control

- Selectable SPI- or I²C-bus interface



Description

The TDA7415CB is the first 6-channel multimedia approach in the car-radio signal processor (CSP) family. It features full software programmability of three independent sections. The signal processor combines a three band audio tone control with an additional notch filter, high/low pass filters for subwoofer support and a spectrum-analyzer with the absence of any external components for the internal filters. Versatile input/output stages and an extended signal routing scheme provide all the flexibility that is needed to serve modern 6-channel applications such as required by DVD technology.

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
TDA7415CB	-40 to 85	TQFP64 (10x10x1.4mm)	Tray

Contents

- 1 Block diagram 6**
- 2 Pin description 7**
 - 2.1 ESD: 7
 - 2.2 Thermal data 7
 - 2.3 Pin assignment 7
 - 2.4 Pin function 8
- 3 Features 10**
- 4 Electrical specification 11**
 - 4.1 Supply 11
 - 4.2 Absolute maximum ratings 11
 - 4.3 Electrical characteristics 11
 - 4.3.1 Input section 11
 - 4.3.2 Main signal processing path 13
 - 4.3.3 Output section 15
 - 4.3.4 General 16
 - 4.3.5 Bus & control inputs 16
 - 4.3.6 DC Offset Detector 17
- 5 Description of the audio processor 18**
 - 5.1 Input section 18
 - 5.2 Main signal processing path 19
 - 5.2.1 Bass filter 19
 - 5.2.2 Mid filter 21
 - 5.2.3 Treble filter 23
 - 5.2.4 Room EQ filter 24
 - 5.3 Output path 26
 - 5.3.1 High pass filter 27
 - 5.3.2 Low pass (subwoofer) filter 27
 - 5.3.3 Line driver output stage (presenting the reference concept) 28
 - 5.3.4 Soft mute 28

5.4	Spectrum analyzer	29
5.5	DC offset detector	31
6	Digital interface	32
6.1	Interface in SPI -mode	32
6.2	I2C bus interface description	33
7	Programming	35
7.1	Data byte specification	36
8	Application information	47
9	Package information	48
10	Revision history	49

List of tables

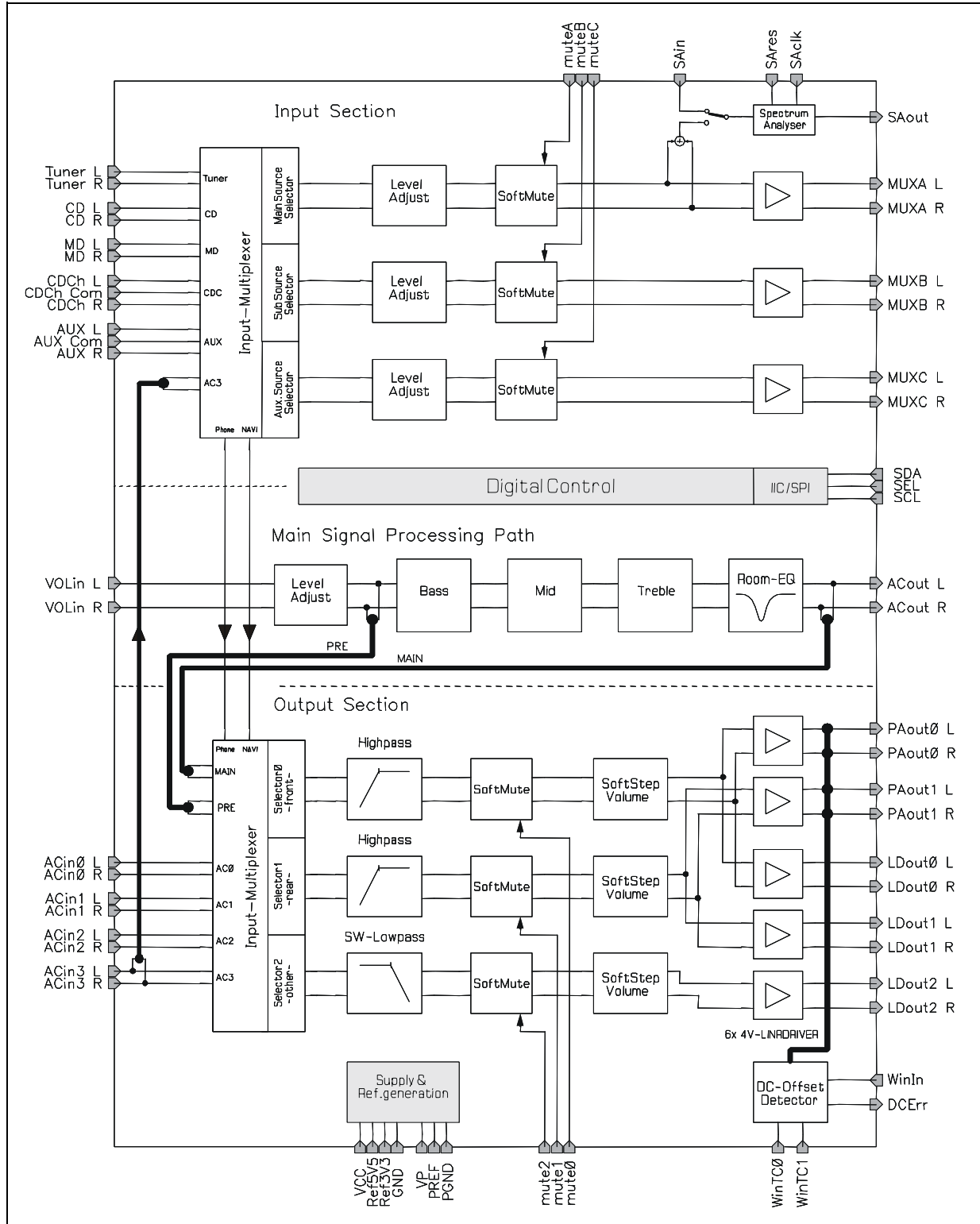
Table 1.	Device summary	1
Table 2.	Thermal data.	7
Table 3.	Pin description	8
Table 4.	Supply.	11
Table 5.	Absolute maximum ratings	11
Table 6.	Input section	11
Table 7.	Main signal processing path	13
Table 8.	Output section.	15
Table 9.	General.	16
Table 10.	Bus & control inputs	16
Table 11.	DC offset detector.	17
Table 12.	Interface in SPI -mode	33
Table 13.	Subaddress allocation (receive mode)	35
Table 14.	Main signal path input (addr. 00)	36
Table 15.	Main signal path, bass-filter (addr. 01)	36
Table 16.	Main signal path, bass-filter (addr. 02)	37
Table 17.	Main signal path, mid-filter (addr. 03)	37
Table 18.	Main signal path, treble-filter (addr. 04)	38
Table 19.	Main signal path, room-EQ (addr. 05)	38
Table 20.	Input section, signal paths A-C (addr. 06-08)	39
Table 21.	Input section; other settings (addr. 09)	39
Table 22.	Output section, signal path 0 (addr. 10)	40
Table 23.	Output section, signal path 1 and 2 (addr. 11)	40
Table 24.	Output section, high-pass filters (addr. 12)	41
Table 25.	Output section, volume 0L, 0R, 1L, 1R, 2L, 2R (addr. 13-16, 18, 19)	42
Table 26.	Output section, subwoofer low-pass filter (addr. 17)	43
Table 27.	Output section, bus-mutes (addr. 20)	43
Table 28.	DC-detector and other output section settings (addr. 21)	44
Table 29.	Soft-mute and soft-step fader time (addr. 22)	45
Table 30.	Spectrum analyzer settings (addr. 23)	45
Table 31.	Testing * (addr. 31)	46
Table 32.	Document revision history	49

List of figures

Figure 1.	Block diagram	6
Figure 2.	Pin connection (top view)	7
Figure 3.	Signal-flow input-section (the following soft-mute and output buffer are not shown)	18
Figure 4.	Bass control range; $f_C= 60\text{Hz}$, $Q= 1.0$	19
Figure 5.	Bass center frequencies; gain= 15dB, $Q= 1.0$	20
Figure 6.	Bass filter quality factors; $f_C= 60\text{Hz}$, gain= 15dB.	20
Figure 7.	Bass DC-mode frequency responses; gain= 15dB, $Q= 1.5$	21
Figure 8.	Mid control range; $f_C= 1\text{kHz}$, $Q= 1.0$	21
Figure 9.	Mid center frequencies; gain= 15dB, $Q= 1.0$	22
Figure 10.	Mid filter quality factors; $f_C= 1\text{kHz}$, gain= 15dB	22
Figure 11.	Treble control range; $f_C= 12.5\text{kHz}$, $Q= 1.0$	23
Figure 12.	Treble center frequencies; gain= 15dB, $Q= 1.0$	23
Figure 13.	Room-EQ control range; $f_C= 200\text{Hz}$, $Q= 1.0$	24
Figure 14.	Room-EQ notch frequencies; attenuation= -7dB, $Q= 1.0$	24
Figure 15.	Room-EQ notch filter quality factors; $f_C= 200\text{Hz}$, attenuation= 7dB.	25
Figure 16.	Signal flow output section	26
Figure 17.	High-pass corner frequencies; $Q= 0.707$	27
Figure 18.	Low-pass corner frequencies; $Q= 0.707$	27
Figure 19.	Line-driver output with reference generation scheme	28
Figure 20.	Soft-mute signal envelope versus time	29
Figure 21.	Spectrum analyzer block diagram	30
Figure 22.	Read cycle timing diagram	30
Figure 23.	DC-offset detection circuit (simplified)	31
Figure 24.	Switching characteristics (SPI-mode):	32
Figure 25.	Interface in SPI -mode diagram	32
Figure 26.	I ² C bus interface diagram	33
Figure 27.	Typical application connections diagram	47
Figure 28.	TQFP64 mechanical data and package dimensions	48

1 Block diagram

Figure 1. Block diagram



2 Pin description

2.1 ESD:

All pins are protected against ESD according to the MIL883 standard.

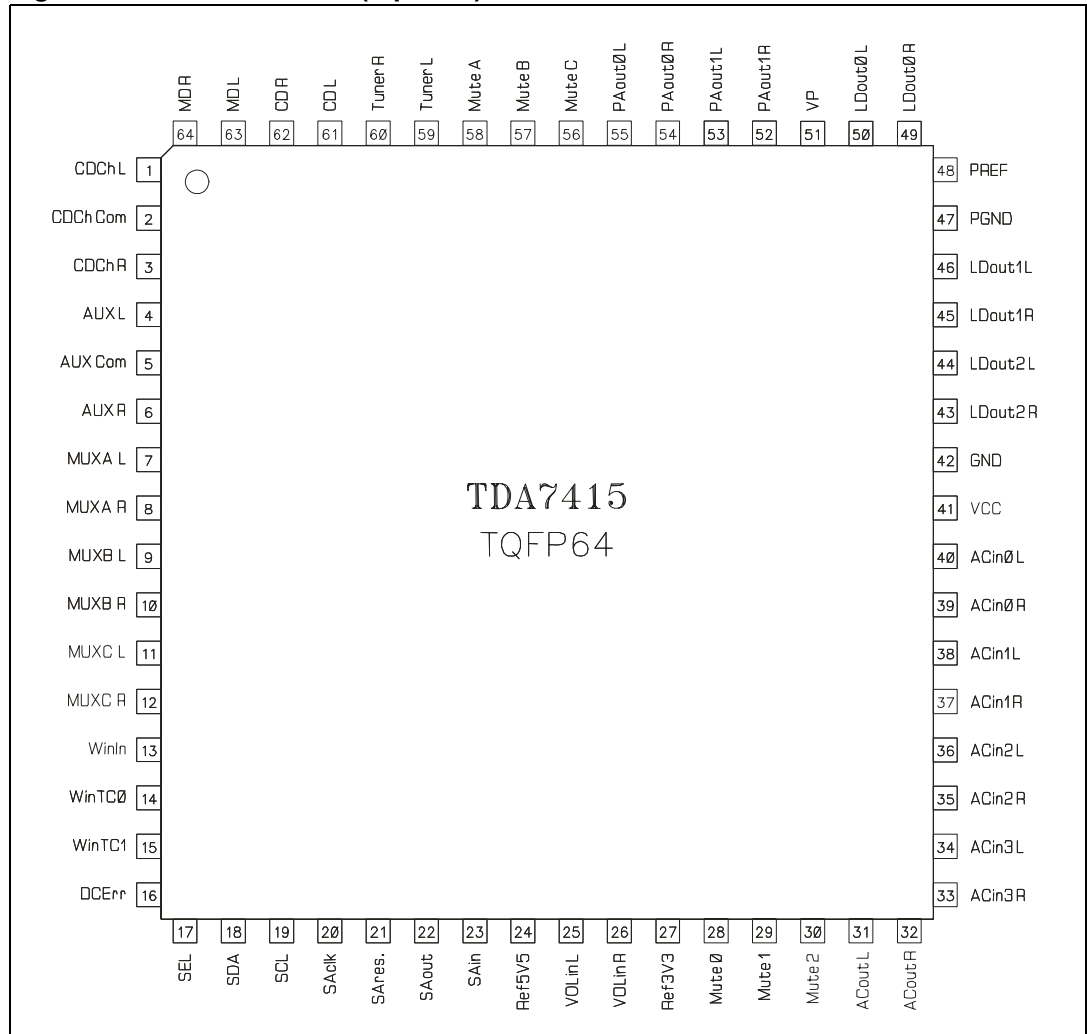
2.2 Thermal data

Table 2. Thermal data

Symbol	Description	Value	Unit
$R_{th\ j-pins}$	Thermal resistance junction-pins	50	°C/W

2.3 Pin assignment

Figure 2. Pin connection (top view)



2.4 Pin function

Table 3. Pin description

PIN	Direction (1)	Name	Description
1	I	CDCh L	CD-changer input, pseudo differential, left channel
2	I	CDCh Common	CD-changer input, pseudo differential common
3	I	CDCh R	CD-changer input, pseudo differential, right channel
4	I	AUX L	Aux./Navigation input, pseudo differential, left channel
5	I	AUX Common	Aux./Navigation input, pseudo differential common
6	I	AUX R	Aux./Navigation input, pseudo differential, right channel
7	O	MUXA L	IN-Section, signal path A output (Main), left channel
8	O	MUXA R	IN-Section, signal path A output (Main), right channel
9	O	MUXB L	IN-Section, signal path B output (Sub), left channel
10	O	MUXB R	IN-Section, signal path B output (Sub), right channel
11	O	MUXC L	IN-Section, signal path C output (Aux.), left channel
12	O	MUXC R	IN-Section, signal path C output (Aux.), right channel
13	I	WinIn	Zero-window Sense input (from power-amp)
14	P	WinTC0	Zero-window comparator 0 time constant
15	P	WinTC1	Zero-window comparator 1 time constant
16	O	DCErr	DC-detector Error output
17	I	SEL	Interface-select; SPI: receive enable
18	I / OC	SDA	I ² C/SPI-bus serial data input/output
19	I	SCL	I ² C/SPI-bus serial clock input
20	I	SAclk	Spectrum analyzer clock input
21	I	SAres.	Spectrum analyzer reset
22	O	SAout	Spectrum analyzer analog voltage output
23	I	SAin	Spectrum analyzer external input
24	P	Ref5V5	5.5V-reference decoupling pin, connects to external capacitor
25	I	Volln L	Main signal path input, left channel
26	I	Volln R	Main signal path input, right channel
27	P	Ref3V3	3.3V-reference decoupling pin, connects to external capacitor
28	I	Mute0	OUT-section, signal path 0 (front) direct mute
29	I	Mute1	OUT-section, signal path 1 (rear) direct mute
30	I	Mute2	OUT-section, signal path 2 (other) direct mute
31	O	ACout L	Main signal path output, left channel

Table 3. Pin description (continued)

PIN	Direction (1)	Name	Description
32	O	ACout R	Main signal path output, right channel
33	I	ACin3 R	OUT-section, AC-coupled input 3, right channel
34	I	ACin3 L	OUT-section, AC-coupled input 3, left channel
35	I	ACin2 R	OUT-section, AC-coupled input 2, right channel
36	I	ACin2 L	OUT-section, AC-coupled input 2, left channel
37	I	ACin1 R	OUT-section, AC-coupled input 1, right channel
38	I	ACin1 L	OUT-section, AC-coupled input 1, left channel
39	I	ACin0 R	OUT-section, AC-coupled input 0, right channel
40	I	ACin0 L	OUT-section, AC-coupled input 0, left channel
41	S	VCC	Device supply pin
42	S	GND	Device ground pin
43	O	LDout2 R	Line-driver output, signal path 2 (other), right channel
44	O	LDout2 L	Line-driver output, signal path 2 (other), left channel
45	O	LDout1 R	Line-driver output, signal path 1 (rear), right channel
46	O	LDout1 L	Line-driver output, signal path 1 (rear), left channel
47	S	PGND	Device ground pin (dual supply), connects to system ground
48	P	PREF	Line-driver-reference decoupling pin, connects to external capacitor
49	O	LDout0 R	Line-driver output, signal path 0 (front), right channel
50	O	LDout0 L	Line-driver output, signal path 0 (front), left channel
51	S	VP	Device supply pin (dual supply), Output section
52	O	PAout1 R	Out-section rear output, right channel
53	O	PAout1 L	Out-section rear output, left channel
54	O	PAout0 R	Out-section front output, right channel
55	O	PAout0 L	Out-section front output, left channel
56	I	Mute C	IN-section, signal path 2 (Aux.) direct mute
57	I	Mute B	IN-section, signal path 1 (Sub) direct mute
58	I	Mute A	IN-section, signal path 0 (Main) direct mute
59	I	Tuner L	Tuner input, left channel
60	I	Tuner R	Tuner input, right channel
61	I	CD L	CD input, left channel
62	I	CD R	CD input, right channel
63	I	MD L	Minidisk (mono-differential Phone+) input, left channel
64	I	MD R	Minidisk (mono-differential Phone-) input, right channel

1. I= input, O= output, OC =open collector, P= passive external component, S= supply

3 Features

The TDA7415CB is composed of four major building blocks. - The IN-section, the spectrum-analyzer, the main signal processing path and the OUT-section; Individually featuring:

IN-section

- Three independent signal-paths (front, rear and auxiliary) with independent soft-mute.
- Six stereo inputs; 3 single ended; 1 single ended or full differential mono; 2 quasi-differential.
- $\pm 15\text{dB}$ level-adjust with 1dB steps.
- Pin-accessible and/or I²C/SPI-controlled soft-mute (direct mute) for each signal path.

Spectrum-analyzer

- 7-band, fully integrated 2nd-order band-pass filters with programmable filter quality for different visual behavior.
- Dedicated one or two-wire serial port for analog data-readout.
- Analog output voltage 3,3V- μP compatible.

Main signal processing path

- $\pm 15\text{dB}$ level-adjust with 1dB steps.
- Fully integrated bass-, middle- and treble-tone control. All filters offer 2nd-order frequency response with programmable filter quality and center frequency.
- Room-acoustics notch filter (Room-EQ) allows the suppression of primary car-body resonance.

OUT-section

- Three independent signal-paths (front, rear and others) with individual soft-mute.
- Four AC-coupled, single ended stereo inputs.
- Pin-accessible soft-mute (direct mute), for each signal path.
- I²C/SPI-controlled soft-mute, independent for all six (mono) channels
- Main signal path monitor-select (pre/post tone control).
- L/R-channel independent phone, navigation or phone/navigation-mix signal interrupts for front signal path; L/R-channel independent phone or navigation interrupts for rear- and others-path.
- 2nd-order frequency response high-pass filters for front- and rear-signal path.
- 2nd-order frequency response subwoofer low-pass filter for others-signal path.
- Soft-step volume with 79 to 25dB range for each signal path.
- Four dedicated outputs for an internal (on-board) power amplifier.
- Six 4V_{RMS} line-driver outputs for an external (remote) power amplifier.
- Offset voltage detection circuit for on-board power amplifier failure diagnosis.

4 Electrical specification

4.1 Supply

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7.5	8.5	9.5	V
V_P	Supply Current (Line Driver)		7.5	12	13	V
I_{total}	Total Supply Current	$V_{CC} = 8.5V$; $V_P = 12V$		45		mA
SVRR	Ripple Rejection @ 1kHz	Audio Processor (all Filters flat)		60		dB

4.2 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Operating Supply Voltage	10	V
V_P	Operating Supply Voltage	13	V
T_{amb}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

4.3 Electrical characteristics

4.3.1 Input section

$V_{CC} = 8.0V$; $V_P = 12.0V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; $f = 1kHz$; unless otherwise specified.

Table 6. Input section

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
R_{in}	Input Impedance	Single-ended inputs	70	100	130	$k\Omega$
		Differential inputs	70	100	130	$k\Omega$
		MD-input, differential mode	35	56	65	$k\Omega$
V_{CL}	Input Clipping Level (THD $\leq 0.1\%$)	Single ended inputs	1.4	1.5		V_{RMS}
		Differential inputs; ⁽¹⁾	2.0	2.2		V_{RMS}
CMRR	Common Mode Rejection Ratio Differential inputs (CD, AUX.)	$V_{CM} = 1V_{RMS}$ @ 1kHz	40	70		dB
		$V_{CM} = 1V_{RMS}$ @ 10kHz	40	60		dB

Table 6. Input section (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
CMRR _{MD}	Common Mode Rejection Ratio	V _{CM} = 1V _{RMS} @ 1kHz	40	66		dB
	Mono differential input (MD)	V _{CM} = 1V _{RMS} @ 10kHz	40	56		dB
S _{IN}	Input Separation		80	100		dB
G _{IN MIN}	Min. Input Gain	input to output, ⁽¹⁾	-16	-15	-14	dB
G _{IN MAX}	Max. Input Gain		14	15	16	dB
G _{STEP}	Gain-adjust Step Resolution		0.5	1	1.5	dB
V _{DC}	DC-Offset Steps	Adjacent Gain Steps		0.5	6	mV
		G _{MIN} to G _{MAX}		5	35	mV
ATT _{MUTE}	Mute Attenuation		80	100		dB
t _{SMC}	Soft-mute completion time, ramp-up or -down	T1	0.1	0.24	0.4	ms
		T2	0.25	0.48	0.75	ms
		T3	7	10.2	13	ms
		T4	16	20.4	26	ms
V _{NO}	Output-noise, MUX-Outputs	20Hz - 20kHz; all flat, 0dB		8	15	μV
V _{OUT,max}	Maximum output level	R _{LOAD} ≥ 2kΩ; THD ≤ 0.1%	1.4	1.5		V _{RMS}
R _L	Output load resistance	THD ≤ 0.1%	1.0			kΩ
C _L	Output load capacitance				10	nF
R _{OUT}	Output impedance			24	100	Ω
V _{DC}	DC voltage level		3.1	3.3	3.5	V
Spectrum Analyzer (see figure 21)						
R _{in}	Input impedance		70	100	130	kΩ
V _{SAin}	Max. Input level, SAin-pin	3.3V full scale at SAout-pin		1.0		V _{RMS}
V _{SAout}	Output Voltage Range	R _{LOAD} ≥ 1MΩ; V _{SAin} ≤ 1V _{RMS}	0	-	3.3	V
f _{C1}	Center Frequency, band 1 ⁽²⁾		55	62	69	Hz
f _{C2}	Center Frequency, band 2 ⁽²⁾		141	157	173	Hz
f _{C3}	Center Frequency, band 3 ⁽²⁾		356	396	436	Hz
f _{C4}	Center Frequency, band 4 ⁽²⁾		0.9	1	1.1	kHz
f _{C5}	Center Frequency, band 5 ⁽²⁾		2.26	2.51	2.76	kHz
f _{C6}	Center Frequency, band 6 ⁽²⁾		5.70	6.34	6.98	kHz
f _{C7}	Center Frequency, band 7 ⁽²⁾		14.4	16.0	17.6	kHz
Q _f	Filter Quality Factor ⁽²⁾	Q ₁	1.40	1.75	2.10	
		Q ₂	2.80	3.5	4.20	
f _{SAclk}	Read-out clock frequency		1		100	kHz
t _{SAdel}	Analog output delay time	C _{Load} at SAout-pin ≤ 100pF		1	2	μs

Table 6. Input section (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
t_{repeat}	Read-out cycle repeat time	Recommended refresh rate	50			ms
t_{intres}	Internal reset time	Auto-reset mode enabled	3	4	5	ms
t_{SAres}	Reset pulse width	Auto-reset mode disabled	500			ns

1. All differential inputs or differential configurations have -3dB input gain.

4.3.2 Main signal processing path

Table 7. Main signal processing path

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
R_{in}	Input Impedance		35	50	65	k Ω
V_{CL}	Input Clipping Level	THD \leq 0.1%	1.4	1.5		V_{RMS}
$G_{IN MIN}$	Min. Input Gain	input to output; all filters flat	-16	-15	-14	dB
$G_{IN MAX}$	Max. Input Gain		14	+15	16	dB
G_{STEP}	Gain-adjust Step Resolution			1		dB
V_{DC}	DC-Offset Steps	Adjacent Gain Steps		0.5	6	mV
		G_{MIN} to G_{MAX}		5	30	mV
$V_{OUT,max}$	Maximum output level	$R_{LOAD} \geq 2k\Omega$; THD \leq 0.1%	1.4	1.5		V_{RMS}
R_L	Output load resistance	THD \leq 0.1%	1.0			k Ω
C_{OUT}	Output load capacitance				10	nF
R_{OUT}	Output impedance			24	36	Ω
V_{DC}	DC voltage level		3.1	3.3	3.5	V
Bass Control						
G_{RANGE}	Gain Control Range		± 13	± 15	± 17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
f_C	Center Frequency ⁽¹⁾	f_{C0}	30	40	50	Hz
		f_{C1}	40	50	50	Hz
		f_{C2}	50	60	70	Hz
		f_{C3}	60	70	90	Hz
		f_{C4}	60	80	100	Hz
		f_{C5}	80	100	120	Hz
		f_{C6}	100	120	140	Hz
		f_{C7}	120	150	170	Hz

Table 7. Main signal processing path (continued)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
Q _{BASS}	Quality Factor ⁽¹⁾	Q ₁	0.9	1	1.1	-
		Q ₂	1.13	1.25	1.38	-
		Q ₃	1.35	1.5	1.65	-
		Q ₄	1.8	2	2.2	-
DC _{GAIN}	Bass DC-Gain	DC-mode= off	-1	0	1	dB
		DC-mode= on	3.5	4.4	5.5	dB
MID control						
G _{RANGE}	Gain Control Range		±13	±15	±17	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
f _C	Center Frequency ⁽²⁾	f _{C1}	450	500	550	Hz
		f _{C2}	0.9	1	1.1	kHz
		f _{C3}	1.35	1.5	1.65	kHz
		f _{C4}	1.8	2	2.2	kHz
Q _{MID}	Quality Factor ⁽²⁾	Q ₁	0.5	1	1.1	
		Q ₂	1.8	2	2.2	
Treble Control						
G _{RANGE}	Gain Control Range		±13	±15	±17	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
f _C	Center Frequency ⁽¹⁾	f _{C1}	6.4	10	13.6	kHz
		f _{C2}	8.0	12.5	17	kHz
		f _{C3}	9.6	15	20.4	kHz
		f _{C4}	11.2	17.5	23.8	kHz
ROOM-EQ (Acoustics Notch-filter)						
G _{RANGE}	Gain Control Range			-0...9		dB
A _{STEP}	Step Resolution	Non-uniform, see description	1	-	2	dB
f _C	Notch Frequency ⁽¹⁾	f _{N1}	162	180	198	Hz
		f _{N2}	180	200	220	kHz
		f _{N3}	198	220	242	kHz
		f _{N4}	216	240	264	kHz
Q _{EQ}	Quality Factor ⁽¹⁾	Q ₁	0.9	1	1.1	
		Q ₂	1.8	2	2.2	

1. Min and Max values are calculated according to simulation results; Functionality is guaranteed by measuring a directly correlated parameter

4.3.3 Output section

$V_{CC} = 8.0V$; $V_P = 12.0V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; $f = 1kHz$; unless otherwise specified

Table 8. Output section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{in}	Input Impedance	AC0...3 inputs	35	50	65	$k\Omega$
V_{CL}	Input Clipping Level	THD $\leq 0.1\%$	1.4	1.5		V_{RMS}
ATT_{MUTE}	Mute Attenuation		80	100		dB
t_{SMC}	Soft-mute completion time, ramp-up or -down	T1		0.24		ms
		T2		0.48		ms
		T3		10.2		ms
		T4		5.1		ms
Volume (Soft-step)						
G_{MAX}	Max. Gain			25		dB
A_{MAX}	Max. Attenuation		-82	-79	-76	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	G= -20 to +20dB	-1.25	0	+1.25	dB
		G= -20 to -60dB	-3	0	3	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV
		From 0dB to G_{MIN}		0.5	5	mV
High Pass						
f_C	Center Frequency ⁽¹⁾	f_{C0}	34	40	46	Hz
		f_{C1}	52	60	68	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	108	120	132	Hz
		f_{C5}	135	150	165	Hz
		f_{C6}	162	180	198	Hz
		f_{C7}	198	220	242	Hz
Q_{HP}	Quality Factor ⁽²⁾	Butterworth characteristics	0.665	0.707	0.750	-
Subwoofer Low Pass						
f_C	Center Frequency ⁽²⁾	f_{C0}	44	50	56	Hz
		f_{C1}	54	60	66	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	108	120	132	Hz
Q_{HP}	Quality Factor ⁽²⁾	Butterworth characteristics	0.665	0.707	0.750	-
Audio Outputs						
$V_{PA,max}$	Max. output level; PA-outputs	$R_{LOAD} \geq 2k\Omega$; THD $\leq 0.1\%$	1.88	2		V_{RMS}

Table 8. Output section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{LD,max}	Max. output level; LD-outputs	as above; V _{CC} = 8.0V	2.20	2.75		V _{RMS}
		as above; V _P = 12V	3.75	4		V _{RMS}
R _L	Output load resistance	THD ≤ 0.1%; all outputs	1.0			kΩ
C _L	Output load capacitance	All outputs			10	nF
R _{OUT}	Output impedance	All outputs		24	100	Ω
V _{DC}	DC voltage level	PA-outputs	3.8	4.0	4.2	V
		LD-outputs	V _P / 2 -200mV	V _P / 2	V _P / 2 +200mV	V

1. All differential inputs or differential configurations have -3dB input gain.
2. Min and Max values are calculated according to simulation results; Functionality is guaranteed by measuring a directly correlated parameter

4.3.4 General

Table 9. General

Symbol	Parameter	Test Conditions / remark	Min.	Typ.	Max.	Unit
V _{NO}	Output Noise	BW = 20Hz to 20KHz output mode		10	15	μV
		unweighted all flat, 0dB		12	20	μV
S/N	Signal to Noise Ratio	all flat, 0dB; V _O = 1.5V _{RMS}		110		dB
		All tone filters +10dB; A-weighted; V _O = 1.5V _{RMS}		84		dB
d	Distortion	V _{OUT} = 1V _{RMS} ; all stages 0dB		0.01	0.1	%
		All tone filters +10dB; A-weighted; V _O = 1.5V _{RMS}		0.05	0.1	%
S _C	Channel Separation L/R		80	100		dB
E _T	Total Tracking Error	A _V = 0 to -20dB		0	1	dB
		A _V = -20 to -60dB		0	2	dB
V _{POR}	Internal POR Voltage				3.4	V

4.3.5 Bus & control inputs

Table 10. Bus & control inputs
(I²C/SPI, spectrum analyzer, direct-mute, offset detector)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
V _{IL}	Input Low Voltage	SDA-, SCL-, SEL-, WinIn-pin		0.8	0.7	V
V _{IH}	Input High Voltage		2.5	2.4		V
V _{TH}	Input threshold voltage	SAres-, SAclk-, all Mute-pins		1.5		V
V _{TH}	Input threshold hysteresis			100		mV

Table 10. Bus & control inputs (continued)
(I²C/SPI, spectrum analyzer, direct-mute, offset detector)

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
I _{IN}	Input Current	V _{IN} = 0.4V; SDA-, SCL-pin	-5		5	μA
V _{TH,SPI}	SPI-mode threshold voltage	(1)			5.5	V
V _{O,ACK}	SDA-Acknowledge Output Volt.	I _O = 1.6mA			0.4	V
R _{PULLUP}	Pull-up resistance	WinIn-pin	30	50	70	kΩ
I _{PULLUP}	Pull-up current	V _{IN} = 0V, all Mute-pins	50	100	150	μA
f _{SCKmax}	Maximum clock speed	SPI-mode			2000	kbit/s
		I ² C-mode			800	kbit/s

1. pull-up is needed for I²C Mute

4.3.6 DC Offset Detector

Table 11. DC offset detector

Symbol	Parameter	Test conditions / remark	Min.	Typ.	Max.	Unit
V _{th}	Zero Comp. Window Size	V1		±25		mV
		V2		±50		mV
		V3		±75		mV
		V4		±100		mV
τ _{sp}	Max. Rejected Spike Length	τ1		7.5		μs
		τ2		15		μs
		τ3		22.5		μs
		τ4		30		μs
I _{Err,charge}	DCErr charge current		1	5	10	μA
I _{Err,discharge}	DCErr discharge current		2.5	5	7.5	mA
V _{OutH}	DCErr high voltage		2.5	3.3		V
V _{OutL}	DCErr low voltage			150	300	mV

5 Description of the audio processor

As can be seen from the block diagram in *Figure 1*, the Audio processor is composed of three building blocks. - The INPUT-Section, the MAIN-SIGNAL-PROCESSING-path and the OUTPUT-Section.

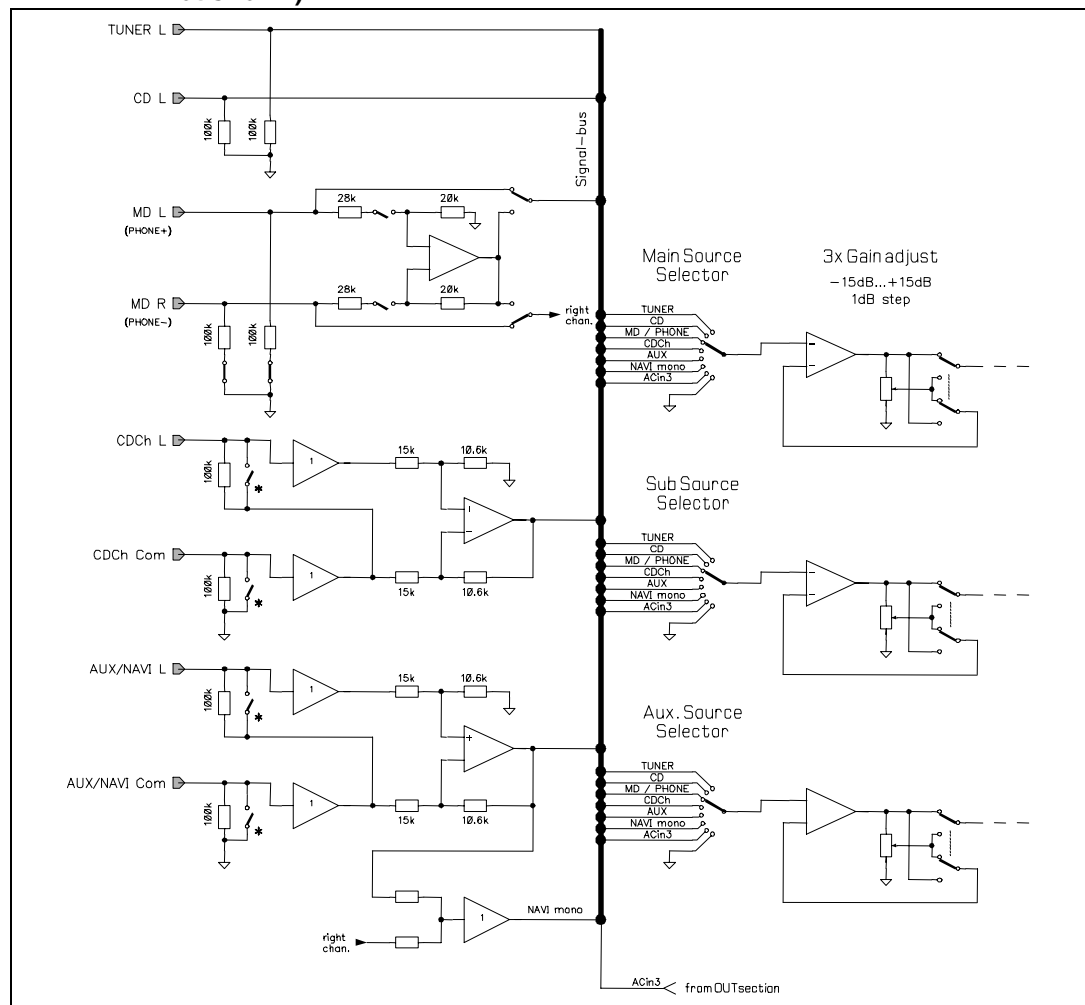
This chapter will give more insight into the different blocks and describe their function.

5.1 Input section

The Input-Section of the TDA7415CB incorporates three independent stereo signal paths, where each can connect to a variety of inputs and the AC3 input from the Output-section for monitoring purposes. For simplicity only the left inputs are shown.

After selection by the Main-, Sub-, and/or Auxiliary-source selector, the signal passes a gain-adjust amplifier, a soft-mute stage and finally a buffer before it is output at the device output-pins. The soft-mute circuit will be described later.

Figure 3. Signal-flow input-section (the following soft-mute and output buffer are not shown)



The CD-Changer- and Auxiliary/Navigation-inputs are quasi-differential inputs, where the 'out-of-phase' or ground signals of both channels share one common input. The Minidisk-input (MD) may be reconfigured for a true mono differential input as required by many phone units. Please note that all differential inputs dampen the signal by 3dB.

Additionally, each differential input-pin features a 'fast charge'-switch (*) allowing quickly charging external, large coupling capacitors upon power-on of the device. For normal operation, these switches **need to be released** by programming the corresponding bit.

For programming of the Input-section, see the programming chapter

5.2 Main signal processing path

The main-signal-processing path incorporates a classical three-band tone control (bass, mid and treble) that is preceded by a gain-adjust amplifier and completed by a dedicated room acoustics notch-filter (Room-EQ, see figure 1) that allows defeating the main car-body resonance.

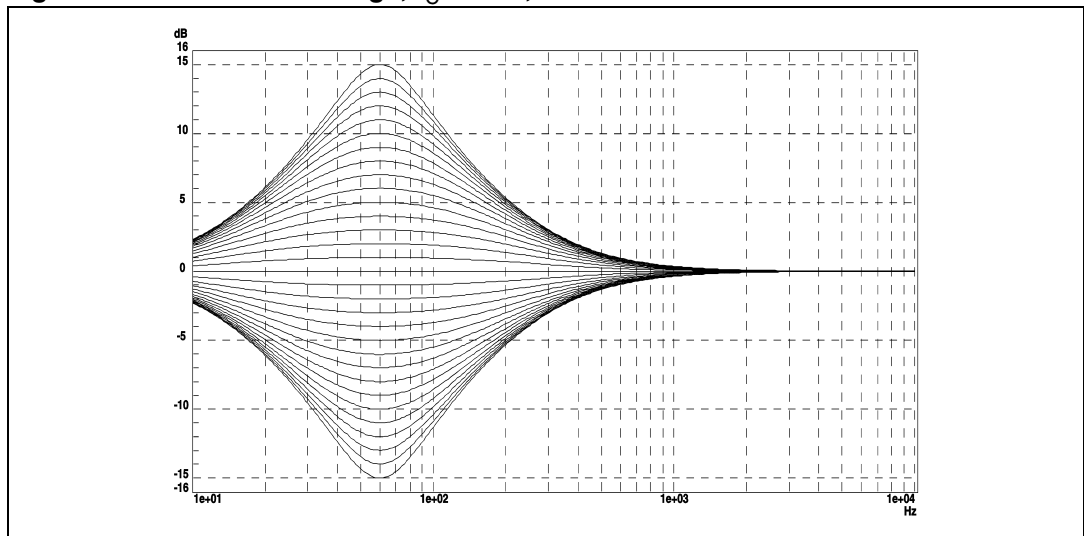
Hereafter, the filters composing the tone control and room-EQ will be presented.

5.2.1 Bass filter

There are four parameters programmable in the bass-filter stage.

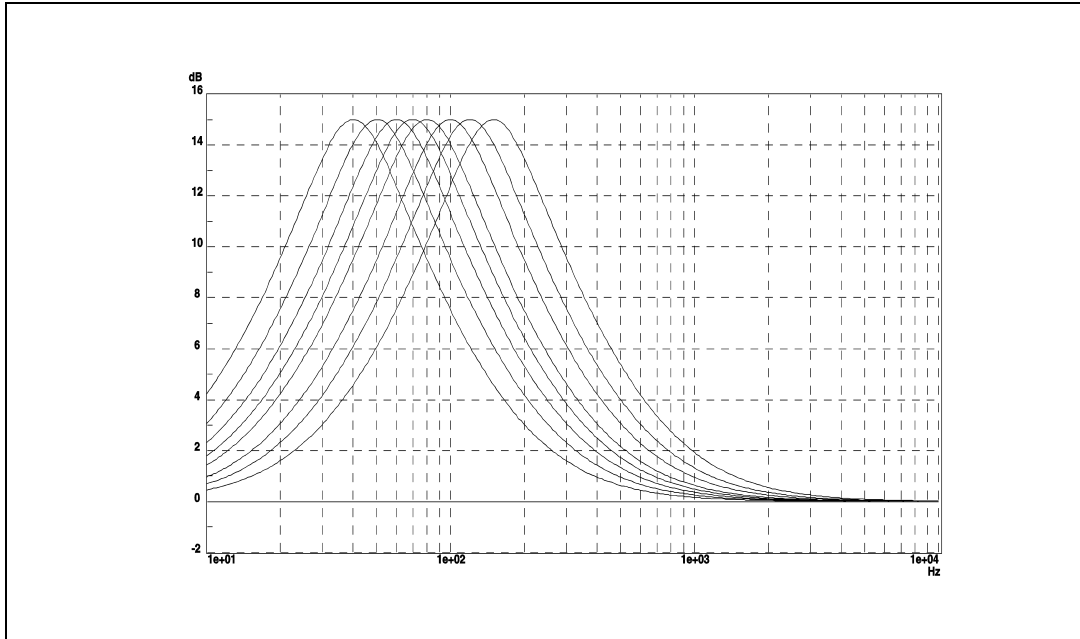
1. **Control Range:** *Figure 4* shows the control range in the frequency domain at 60Hz center frequency.

Figure 4. Bass control range; $f_C = 60\text{Hz}$, $Q = 1.0$



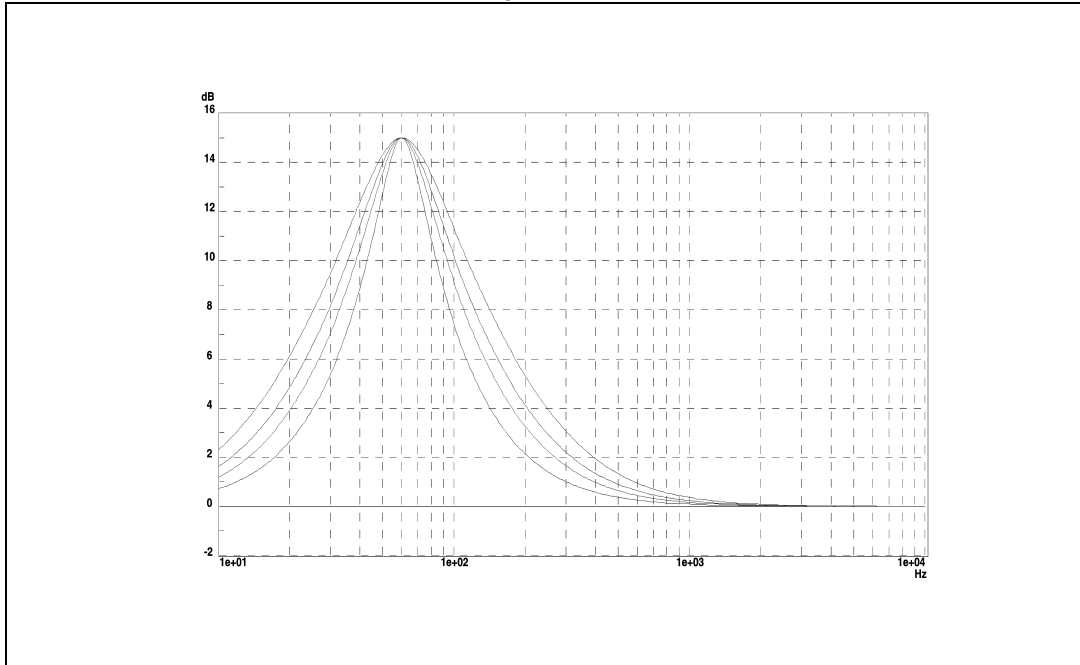
- 2. **Center frequency:** *Figure 5* shows all the selectable center frequencies at a gain of 15dB

Figure 5. Bass center frequencies; gain= 15dB, Q= 1.0



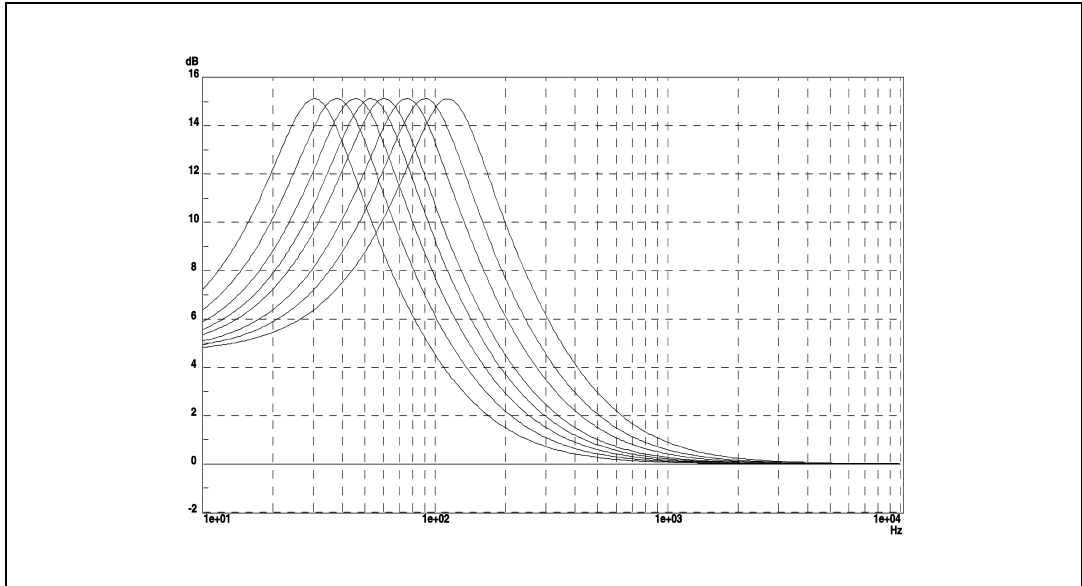
- 3. **Quality Factor:** *Figure 6* shows the four selectable filter quality factors at a gain of 15dB

Figure 6. Bass filter quality factors; $f_c= 60\text{Hz}$, gain= 15dB.



4. **DC-mode:** *Figure 7* shows the effect of the DC-mode at a filter gain of 15dB. In this mode the DC-gain is increased by 4.4dB. In addition the programmed center frequencies and quality factors are decreased by 25%, which realizes alternative frequency responses.

Figure 7. Bass DC-mode frequency responses; gain= 15dB, Q= 1.5

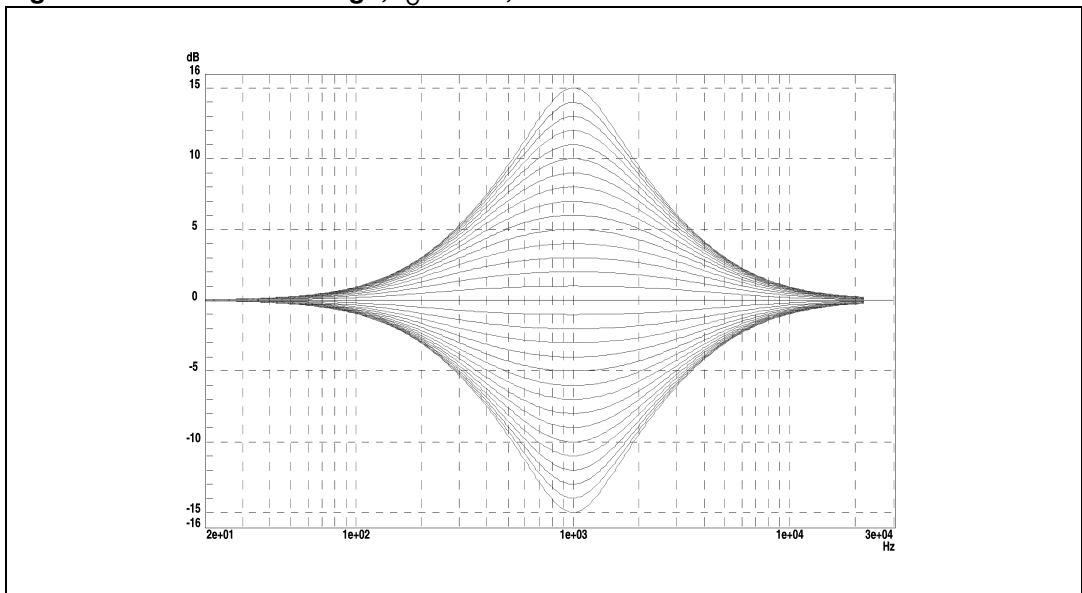


5.2.2 Mid filter

There are three parameters programmable in the mid-filter stage.

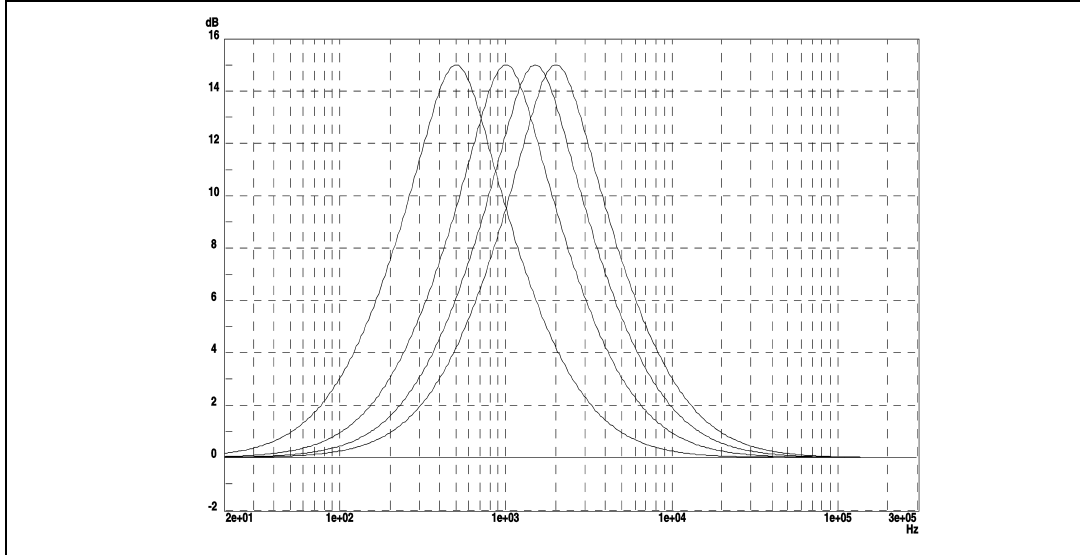
1. **Control Range:** *Figure 8* shows the control range in the frequency domain at 1kHz center frequency.

Figure 8. Mid control range; $f_C= 1\text{kHz}$, $Q= 1.0$



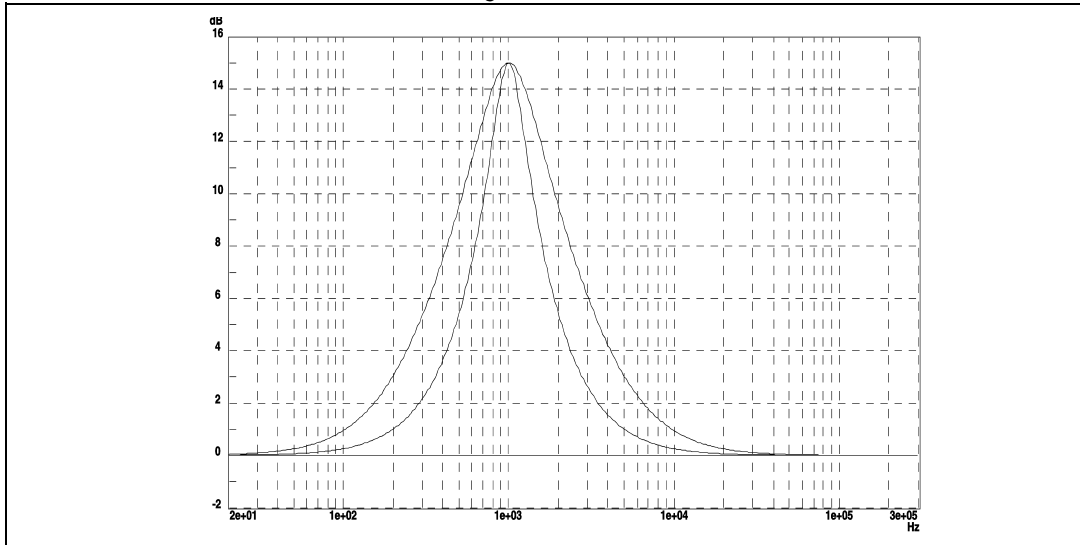
- 2. **Center frequency:** *Figure 9* shows the four selectable center frequencies at a gain of 15dB.

Figure 9. Mid center frequencies; gain= 15dB, Q= 1.0



- 3. **Quality Factor:** *Figure 10* shows the two selectable filter quality factors at a gain of 15dB.

Figure 10. Mid filter quality factors; f_c = 1kHz, gain= 15dB

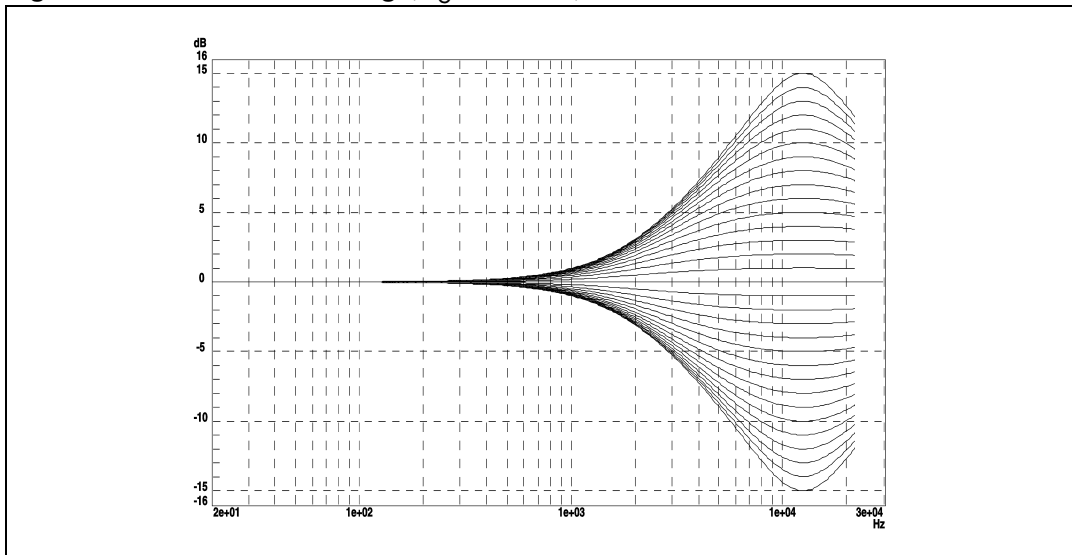


5.2.3 Treble filter

There are two parameters programmable in the treble-filter stage.

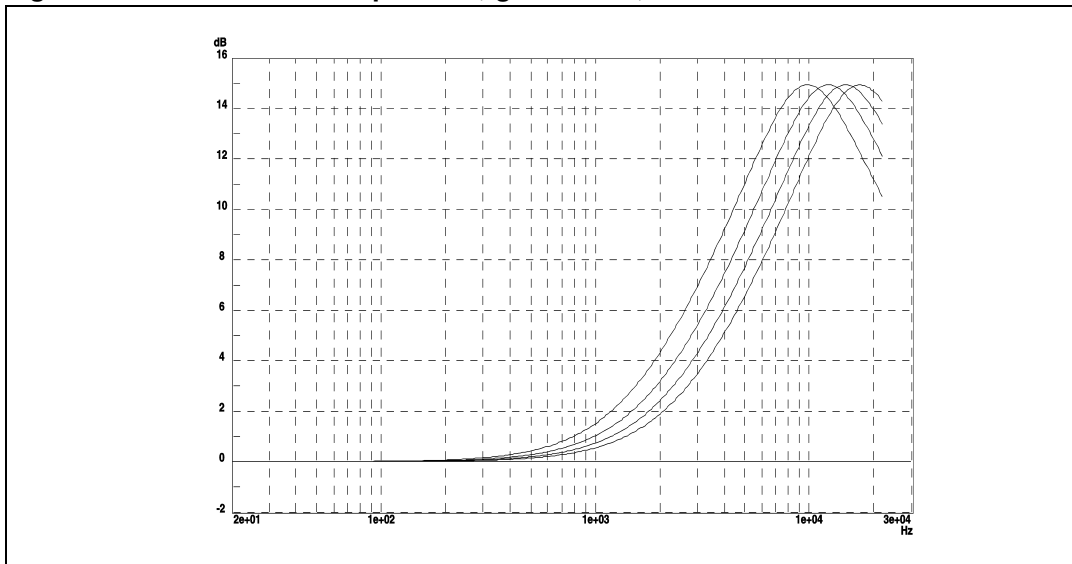
1. **Control Range:** *Figure 11* shows the control range in the frequency domain at 12.5kHz center frequency.

Figure 11. Treble control range; $f_C = 12.5\text{kHz}$, $Q = 1.0$



2. **Center frequency:** *Figure 12* shows the four selectable center frequencies at a gain of 15dB

Figure 12. Treble center frequencies; gain= 15dB, $Q = 1.0$

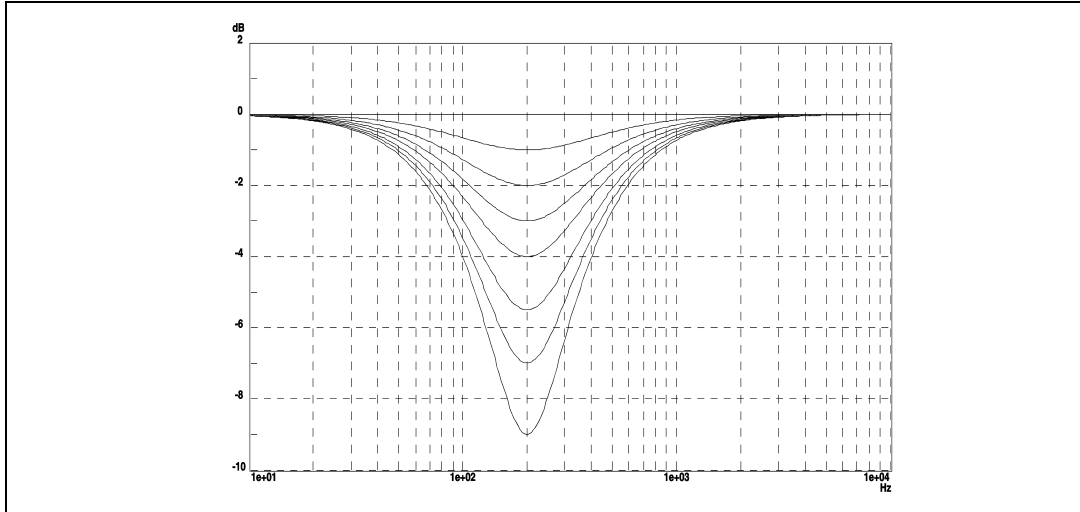


5.2.4 Room EQ filter

There are three parameters programmable in the room-EQ stage.

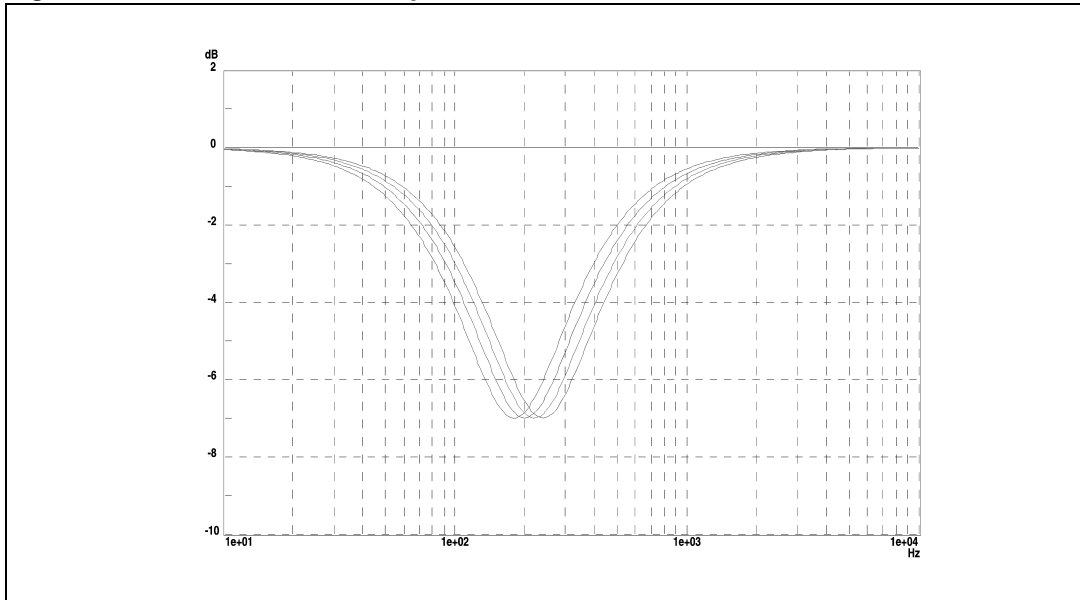
1. **Control Range:** *Figure 13* shows the control range in the frequency domain at 200Hz center frequency. The filter has intentional non-uniform attenuation steps. These are 1dB, 2dB, 3dB, 4dB, 5.5dB, 7dB and 9dB.

Figure 13. Room-EQ control range; $f_C= 200\text{Hz}$, $Q= 1.0$



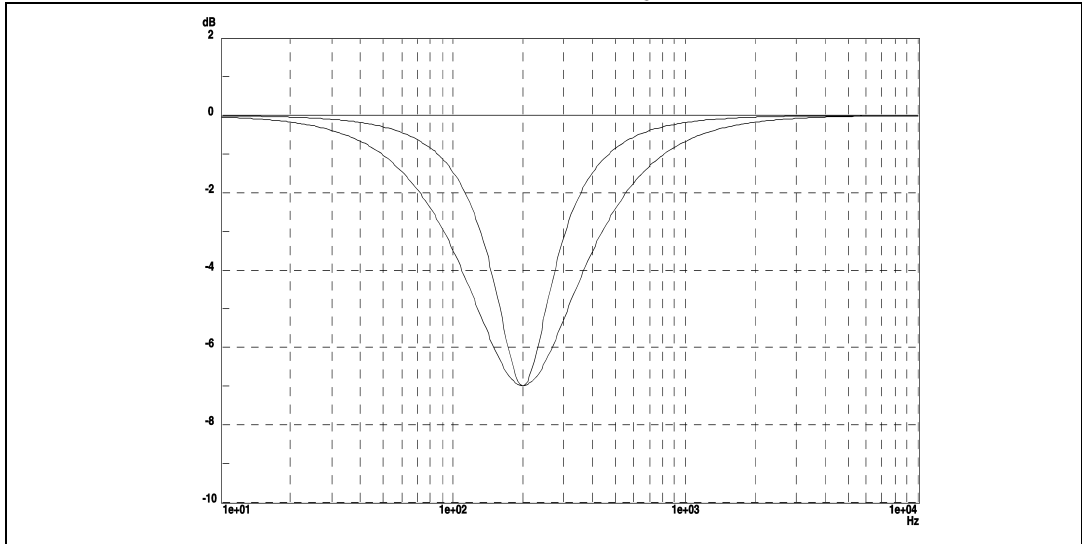
2. **Notch frequency:** *Figure 14* shows the four selectable notch frequencies at a gain of 15dB

Figure 14. Room-EQ notch frequencies; attenuation= -7dB, $Q= 1.0$.



3. **Quality Factor:** *Figure 15* shows the two selectable filter quality factors at a gain of 15dB

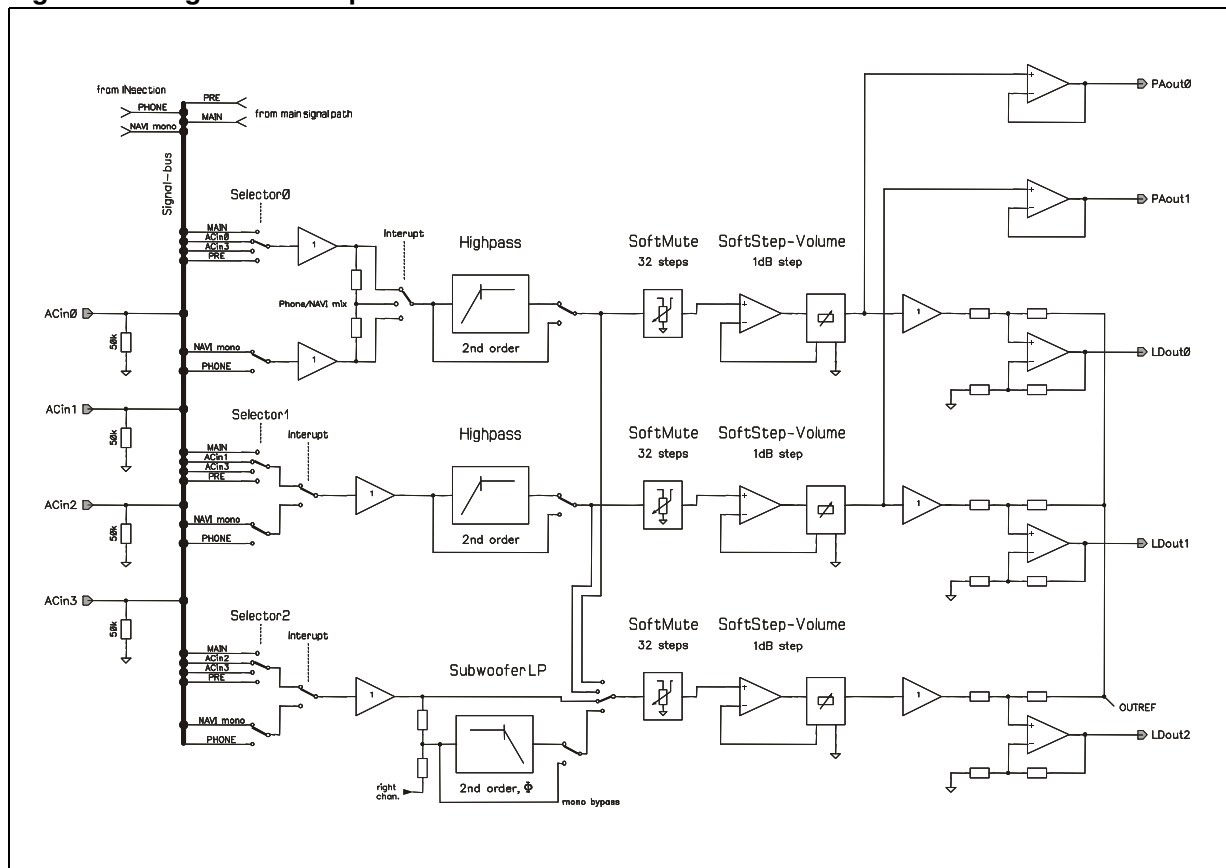
Figure 15. Room-EQ notch filter quality factors; $f_C=200\text{Hz}$, attenuation= 7dB.



5.3 Output path

As the Input-Section, the Output-Section of the TDA7415CB incorporates also three independent stereo signal paths, where each can connect to two out of four AC-coupled, single-ended inputs and to some dedicated signals originating from the input-section and/or main-signal-path. For simplicity only one channel is shown in *Figure 16*. Interruption switches follow the input selectors that can quickly toggle to the phone-, navigation-, or phone/navigation-mix signal independently for each signal path and single L/R-channel. The pre-selection of the interrupt source is common for all signal paths.

Figure 16. Signal flow output section



Signal path 0 and 1 (front and rear) may optionally enter high-pass filters whereas signal path 2 (other) can be low-pass filtered for subwoofer applications. Anti-radiation filters are integrated for all signal paths but there are no anti-alias filters present at the inputs, since for most signal sources it is unlikely to introduce significant high frequency energy. However, if present, the system designer must take care to filter out high frequency components by means of an external RC-low-pass filter located at the AC-input pins. Soft-mute stages and a soft-step volume, that offer fast and click-less muting and/or volume changing follow all three filters. The soft mute circuit will be described later.

Five stereo pairs of output buffers finally complete the Output-section: Signal-path 2 exclusively feeds a line driver output that is capable of $4V_{RMS}$ output level as required by external (remote) power amplifiers. The other signal-paths 1 & 2 feature both, a line driver output and a dedicated internal (on board) power amplifier output with 3dB fixed gain. To maximize the line-driver output swing, when the dual-supply option ($V_{CC} = 9V, V_P = 12V$) is

not needed or available, the line-driver output stages may be programmed for lower gain, still delivering $2.75V_{RMS}$.

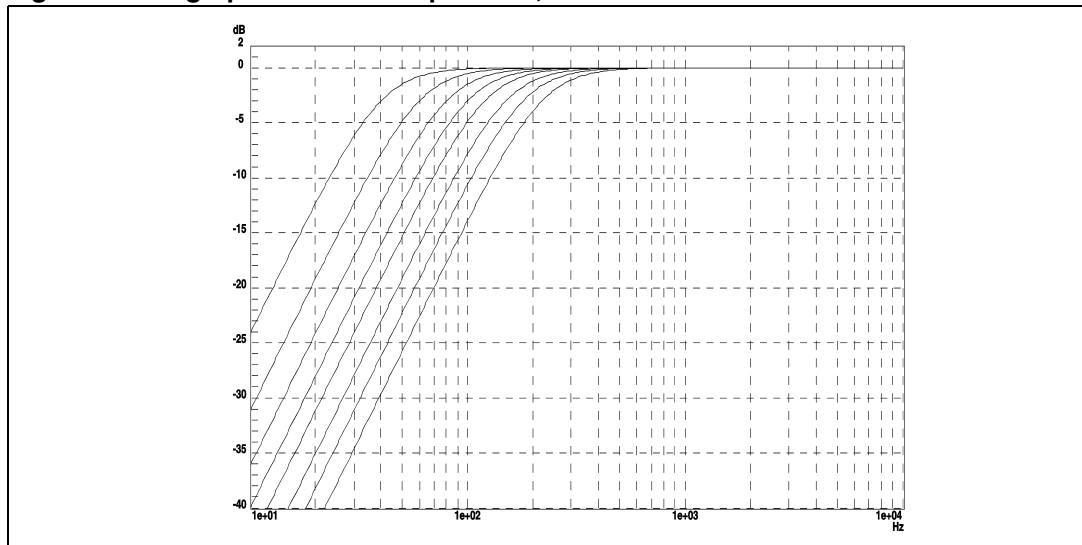
For programming of the Output-section, see the programming chapter

Hereafter, the different circuits composing the Output-section will be presented.

5.3.1 High pass filter

1. **Corner frequency:** *Figure 17* shows all the selectable corner frequencies for the high-pass filter

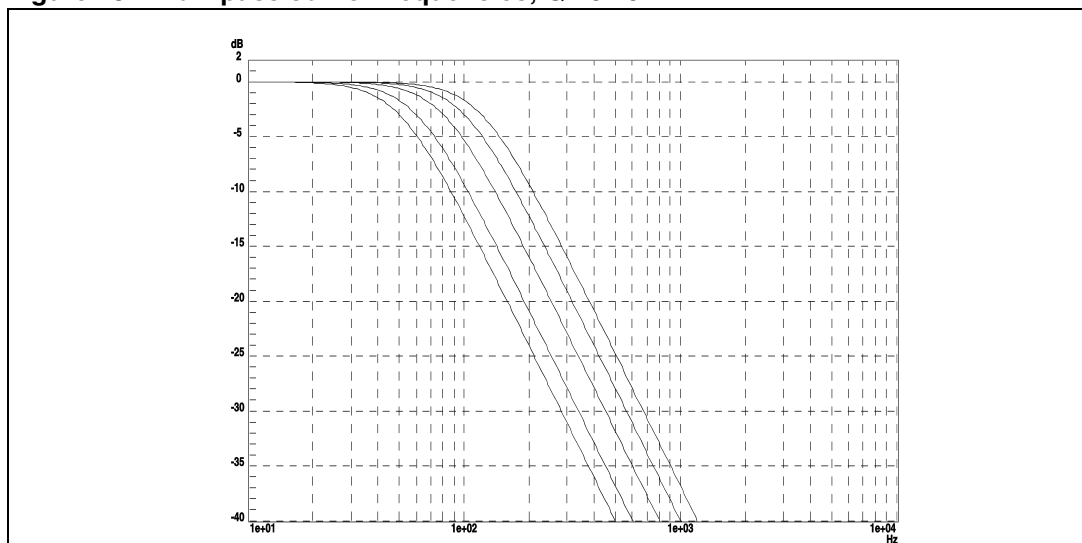
Figure 17. High-pass corner frequencies; Q= 0.707



5.3.2 Low pass (subwoofer) filter

1. **Corner frequency:** *Figure 18* shows all the selectable corner frequencies for the low-pass filter.

Figure 18. Low-pass corner frequencies; Q= 0.707

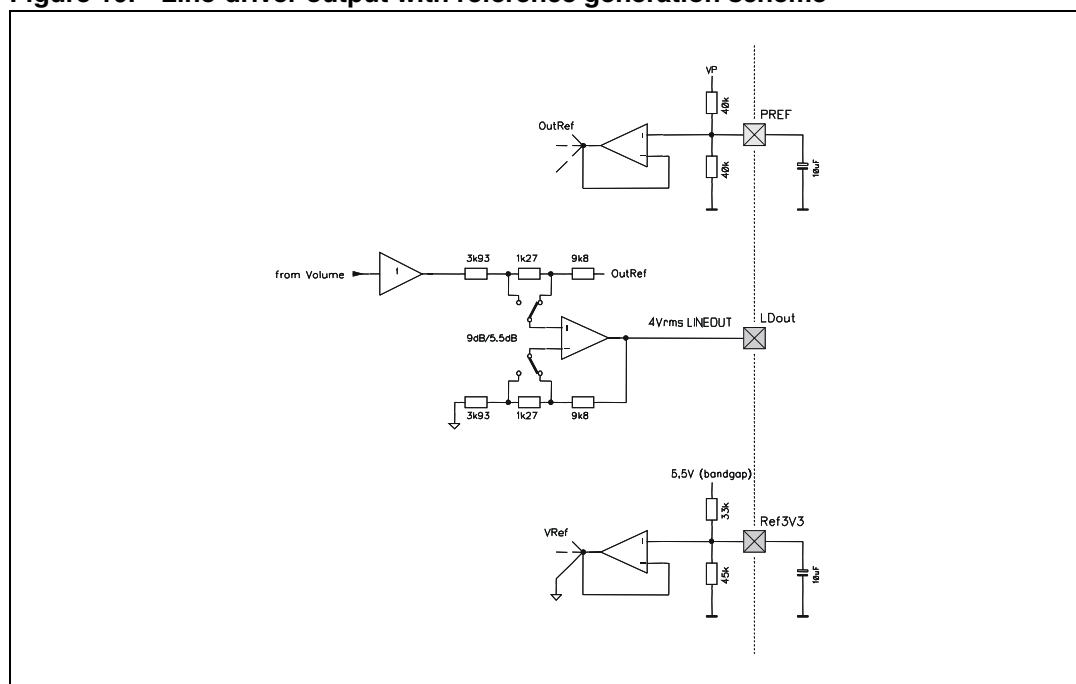


Remark: Both filters offer a 'Butterworth' roll-off response

5.3.3 Line driver output stage (presenting the reference concept)

In order to adapt to two different supply-voltages for the dual-supply option, while maintaining the highest possible output swing when only a single supply is available, the line-driver output was realized as differential amplifier biased around the two device references PRef and Vref3V3 (see [Figure 19](#)). The output DC-voltage precisely tracks the DC-voltage present at the PRef-pin that is half the VP-supply. However, forcing the PRef pin to any desired value could alter this DC-voltage, neglected the remaining output swing.

Figure 19. Line-driver output with reference generation scheme



In a dual-supply application ($V_{CC} = 8.5V$, $V_P = 12V$) the output gain should be set to 9dB to obtain a 4VRMS output level. For a single-supply application ($V_{CC} = V_P = 8.5V$) there is still an output level of $2.75V_{RMS}$ obtainable. Consequently, to avoid clipping in the output stages the gain needs to be reduced to 5.5dB. For the programming of the output gain, see the programming chapter.

Proper power sequencing is no critical issue for the TDA7415. However, it is recommended that both supply-voltages should follow each other within one diode forward-drop (<1V) before reaching their final value.

5.3.4 Soft mute

As can be seen from the block-diagram in figure 1, there are 6 soft-mute circuits placed inside the TDA7415CB: Three each, in both the Input-section and the Output-section that serve the independent signal-paths. A soft-mute can either be achieved by pulling one of the

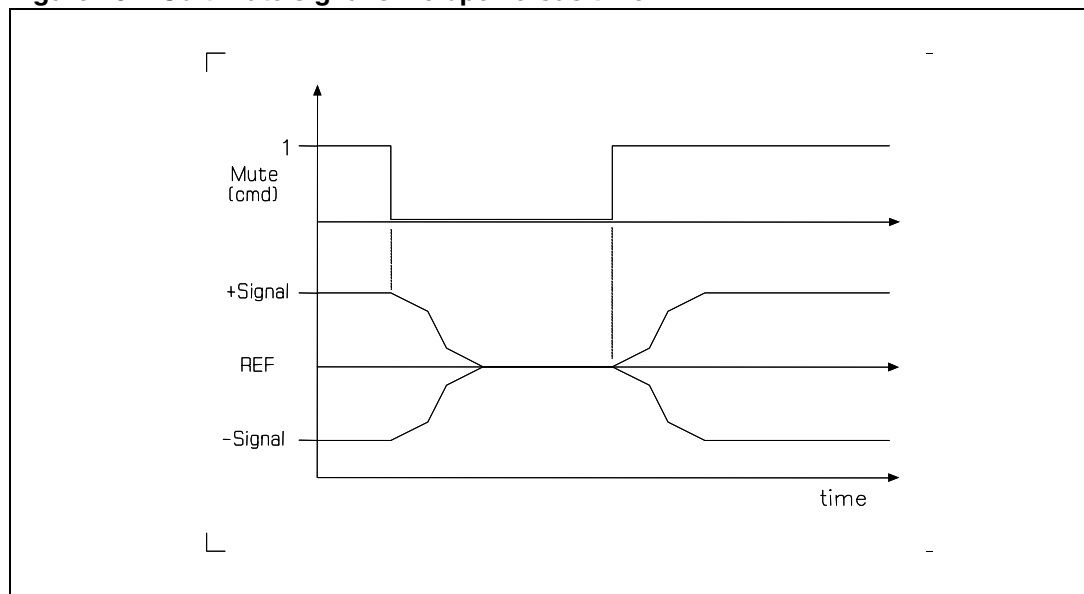
six soft-mute pins low (hardware-mute) or by assessing the corresponding programming bits (software-mute).

For the In-section, a soft-mute is always stereo for each of the three signal-paths and the bus-triggered mute exactly corresponds to the pin-triggered mute, with the exception that the later is inherently faster in response. This behavior is also true for the Out-section, but here the bus-triggered mute is independent for all six single L/R-channels.

All mute-pins have internal pull-ups connected to a 3,3Volts reference that allow the connection to either a 3,3V- or a 5V-microprocessor. Reverse flowing currents are limited to 100 μ A, so that the mute-pins may be driven by both, open-drain or push-pull outputs.

The envelope slope of the soft-mute was realized in a special S-shaped curve to soften the mute transitions in the critical regions (see [Figure 20](#)). The completion time for full mute / no mute is programmable by I²C/SPI-bus in four different values.

Figure 20. Soft-mute signal envelope versus time



Note: A triggered mute is always completed and cannot be interrupted by a change of the initial mute condition.

For the programming of the soft-mute, see the programming chapter.

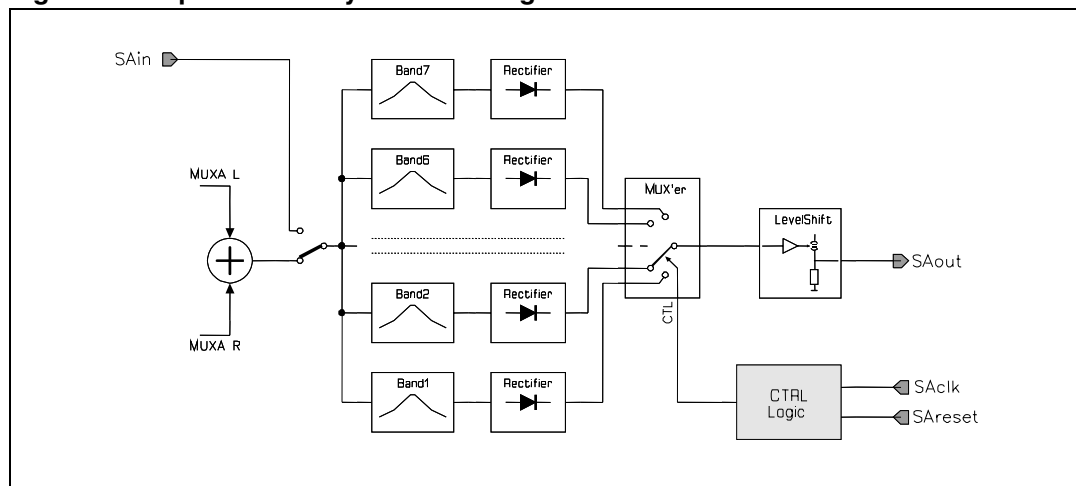
5.4 Spectrum analyzer

A fully integrated seven-band spectrum analyzer is present in the TDA7415CB ([Figure 21](#)).

The spectrum analyzer consists of seven band pass filters followed by rectifiers with sample capacitors that store the maximum peak signal level for each band since the last read cycle. This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog input-port of a microprocessor, the output voltage at this pin is referred to device ground. Since the output voltage follows the peak level linearly, the microprocessor should take care for a logarithmic conversion (e.g. logarithmic look-up table).

The spectrum analyzer's input signal is either the mono-sum of the stereo MUXA-output or alternatively a signal input at the SAin-pin. In order to have some influence on the visual behavior in a given application the filter quality for all band-pass filters may be programmed for two different qualities, with the higher filter quality creating a faster, more differentiating optical response. If the spectrum analyzer is disabled both, the SAres- and the SAclock-pin should be tied to ground.

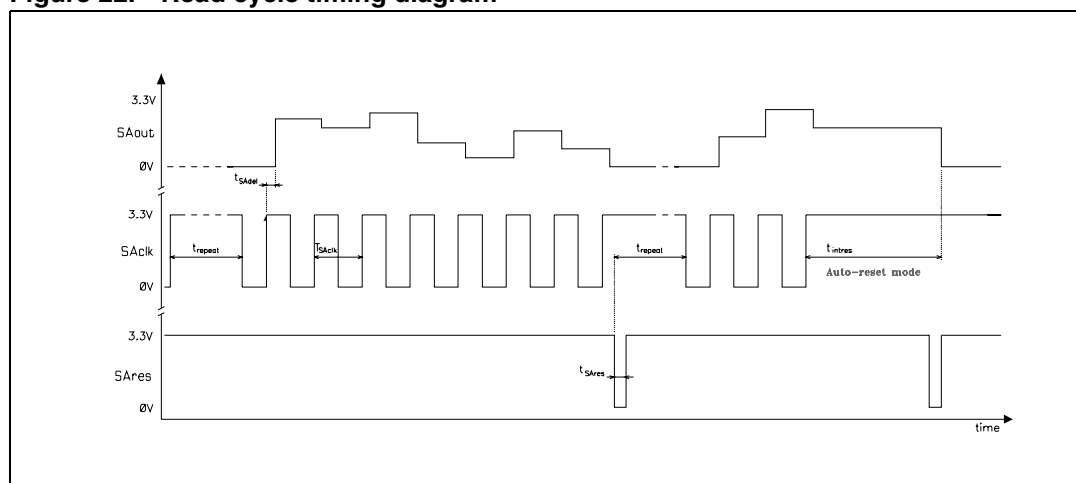
Figure 21. Spectrum analyzer block diagram



The microprocessor starts a read cycle with a negative going clock edge at the SAclock input. On the following positive clock edges, the stored peak signal level of the band pass filters is subsequently switched to SAout. Each analog output value is valid after the time $t_{SA\text{del}}$. A reset of the sample capacitors is triggered by either pulling the SAres-pin low any time or by setting-up the spectrum-analyzer for Auto-reset mode. Although not shown in [Figure 22](#), for the Auto-reset mode a reset is generated whenever SAclock remains high for the time t_{intres} .

Note that a proper auto-reset requires the clock signal SAclock to be held at high potential and that the reset is not repetitive. Once a reset was triggered, a new read-out cycle should not be initiated before the time t_{repeat} has passed. This allows sufficient settling of the filters. [Figure 22](#) illustrates the read cycle timing of the spectrum analyzer.

Figure 22. Read cycle timing diagram



5.5 DC offset detector

Using the DC offset detection circuit (figure 22) an offset voltage difference between the audio power amplifier and the TDA7415CB's PA-outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the TDA7415CB. The WinIn-input has an internal pull-up resistor connected to 5,5Volts. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC0/1-pins are implemented, with external capacitors introducing the same delay $\tau = 5k\Omega * C_{ext}$ as the AC-coupling between the TDA7415 and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

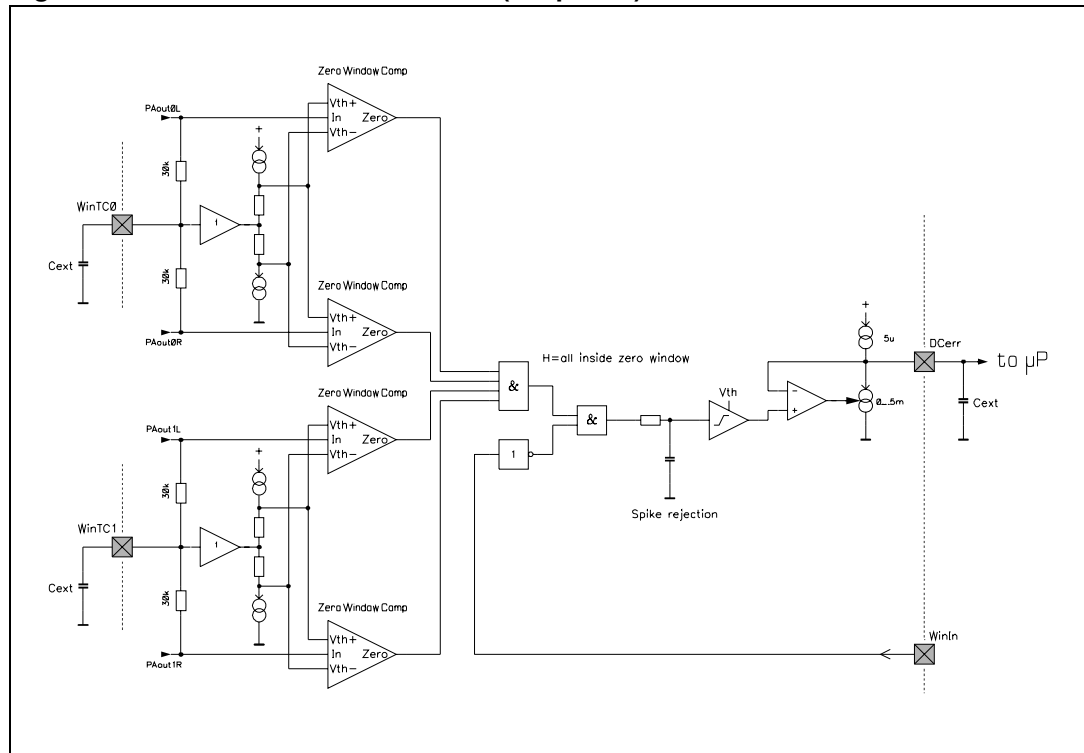
For electrical characteristics see page 8.

A low-active DC-offset error signal appears at the DCerr output if the next conditions are both true:

- a) All PA-outputs (front and rear) are inside zero crossing windows.
- b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication. The fast mode has to be turned off by a manual release of the fast-charge

Figure 23. DC-offset detection circuit (simplified)



6 Digital interface

The TDA7415CB digital interface supports two different protocols: SPI and I²C. To select the I²C-mode the SEL-pin has to be tied to the system supply by means of a 68k -resistor. If the voltage at the SEL-pin falls below 5.5V, the interface switches to SPI-mode. Consequently, the interface is able to work with a microprocessor either supplied by a 3.3V or a 5V power supply. The SPI-mode has to be set and remain static before the device leaves the reset state caused by power-on reset (POR).

For details of both protocols refer to the programming section.

6.1 Interface in SPI -mode

- Interface protocol

The SPI interface protocol comprises:

- A sub-address (SAx) and

A sequence of n data bytes (Dy); each consisting of 8 bits.

A negative going edge at SEL enables the interface receiving data. The interface accepts both a positive (Cpol=1, Cpha=1; SPI-mode 0) as well as a negative (Cpol=0, Cpha=0; SPI-mode 3) clocking scheme. However, the data transmitted has to be valid on the **rising edges** of the serial clock SCL.

Figure 24. Switching characteristics (SPI-mode):

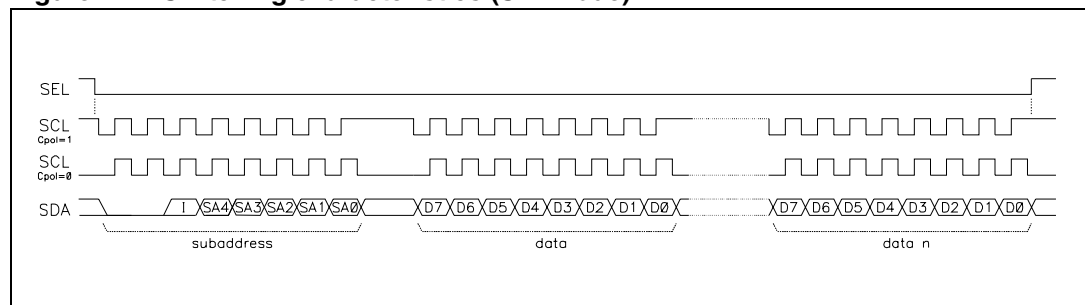


Figure 25. Interface in SPI -mode diagram

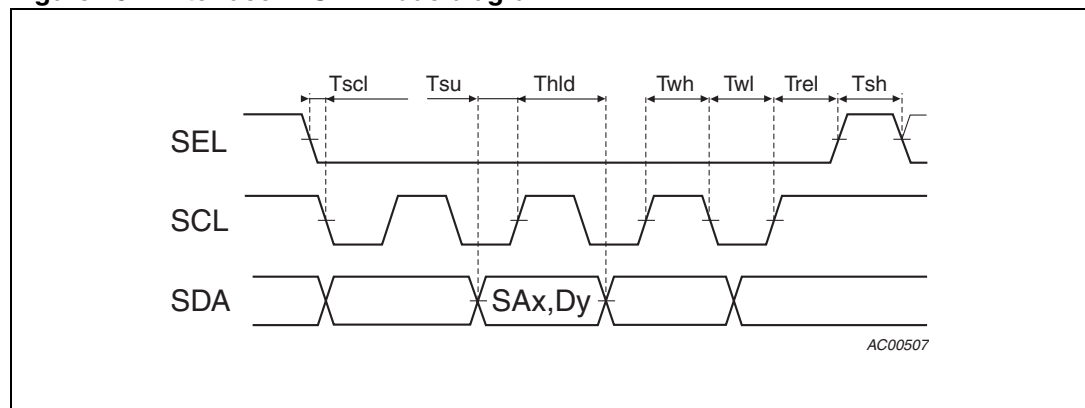


Table 12. Interface in SPI -mode

Symbol	Parameter	Min	Typ	Max	Units
f _{SCLK}	Serial input clock frequency (SCL)	0,00	-	4	MHz
T _{su}	Serial data setup time	40,00	-	-	ns
T _{hld}	Serial data hold time	40,00	-	-	ns
T _{wh}	Serial clock high time width	100,00	-	-	ns
T _{wl}	Serial clock low time width	100,00	-	-	ns
T _{scl}	Select (SEL) to clock (SCL) falling setup time	200,00	-	-	ns
T _{rel}	Clock (SCL) to select (SEL) rising release time	200,00	-	-	ns
t _r	Data rise time	-	-	2,00	μs
t _f	Data fall time	-	-	2,00	μs
T _{sh}	Chip select high time	200,00	-	-	μs

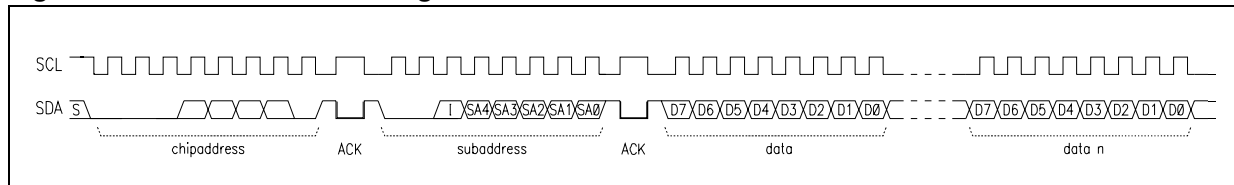
6.2 I²C bus interface description

- Interface Protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 26. I²C bus interface diagram



S = Start

ACK = Acknowledge

Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled which is also true for the SPI mode.

Chip-address

For the TDA7415CB the chip address is **\$8C** (10001100).

Reset condition

A power-on reset (POR) is generated whenever the supply voltage falls below 4.5V. After that, the following data is written automatically into all sub-address registers:

MSB							LSB
1	1	1	1	1	1	1	0

The programming after POR is marked bold face / underlined in the programming tables.

7 Programming

Table 13. Subaddress allocation (receive mode)

MSB							LSB	DESCRIPTION	Byte (dec)
I ₂	I ₁	I ₀	A ₄	A ₃	A ₂	A ₁	A ₀		
0								Unassigned	
	0 1							Test Mode off on	
		0 1						Auto Increment Mode off on	
			0	0	0	0	0	Main signal path input gain adjust	0
			0	0	0	0	1	Main signal path Bass-filter settings I	1
			0	0	0	1	0	Main signal path Bass-filter settings II	2
			0	0	0	1	1	Main signal path Mid-filter settings	3
			0	0	1	0	0	Main signal path Treble-filter settings	4
			0	0	1	0	1	Main signal path Room-EQ settings	5
			0	0	1	1	0	Input section, path A input select & gain adjust	6
			0	0	1	1	1	Input section, path B input select & gain adjust	7
			0	1	0	0	0	Input section, path C input select & gain adjust	8
			0	1	0	0	1	Global Input section settings; Bus contr. mutes	9
			0	1	0	1	0	Output section, path 0 input select & interrupt	10
			0	1	0	1	1	Output section, path 1&2 input select & interrupt	11
			0	1	1	0	0	f _C -select high-pass filter signal path 0&1	12
			0	1	1	0	1	Output section, path 0 left channel Volume	13
			0	1	1	1	0	Output section, path 0 right channel Volume	14
			0	1	1	1	1	Output section, path 1 left channel Volume	15
			1	0	0	0	0	Output section, path 1 right channel Volume	16
			1	0	0	0	1	f _C -select subwoofer filter, path 2 monitor select	17
			1	0	0	1	0	Output section, path 2 left channel Volume	18
			1	0	0	1	1	Output section, path 2 right channel Volume	19
			1	0	1	0	0	Output section, Bus-controlled mutes	20
			1	0	1	0	1	Dc-detector settings; PA-mutes; Linedriver gain	21
			1	0	1	1	0	Softstep & Softmute fade-times	22
			1	0	1	1	1	Spectrum-analyzer settings	23
			1	1	0	0	0	-----	24
			Unassigned	
			1	1	1	1	0	-----	30
			1	1	1	1	1	Test multiplexer; device clocking	31

7.1 Data byte specification

The status after power-on reset is marked bold face / underlined in the programming tables.

Table 14. Main signal path input (addr. 00)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
			0	0	0	0	0	Input gain adjust level
			0	0	0	0	1	-15dB
			0	:	:	:	:	...
			0	1	1	1	0	-1dB
			0	1	1	1	1	-0dB
			1	1	1	1	1	+0dB
			1	1	1	1	0	+1dB
			1	:	:	:	:	...
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
1	1	1						Unused , do not alter

Table 15. Main signal path, bass-filter (addr. 01)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				0	0	0	0	Level
				0	0	0	1	0dB
				:	:	:	:	1dB
				1	1	1	0	:
				1	1	1	1	14dB
								15dB
			0					Boost / Cut
			1					Boost
								Cut
		0						Soft-step
		1						On
								Off
0	0							Quality factor
0	1							1.00
1	0							1.25
1	1							1.50
								2.00

Table 16. Main signal path, bass-filter (addr. 02)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				1	1	1	0	Unused, do not alter
	0	0	0					Center frequency 150Hz
	0	0	1					120Hz
	0	1	0					100Hz
	0	1	1					80Hz
	1	0	0					70Hz
	1	0	1					60Hz
	1	1	0					50Hz
	1	1	1					40Hz
0								DC-mode
1								Off
								On

Table 17. Main signal path, mid-filter (addr. 03)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				0	0	0	0	Level 15dB
				0	0	0	1	14dB
				:	:	:	:	:
				1	1	1	0	1dB
				1	1	1	1	0dB
			0					Boost / Cut
			1					Cut
								Boost
	0	0						Center frequency 500Hz
	0	1						1.0kHz
	1	0						1.5kHz
	1	1						2.0kHz
0								Quality factor 1.0
1								2.0

Table 18. Main signal path, treble-filter (addr. 04)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				0	0	0	0	Level 15dB	
				0	0	0	1	14dB	
				:	:	:	:	:	
				1	1	1	0	1dB	
				1	1	1	1	0dB	
			0					Boost / Cut Cut	
			1					Boost	
	0	0						Center frequency 10kHz	
	0	1						12.5kHz	
	1	0						15kHz	
	1	1						17.5KHz	
1								Unused , do not alter	

Table 19. Main signal path, room-EQ (addr. 05)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
						1	0	Unused , do not alter	
			0	0	0			Attenuation level 9dB	
			0	0	1			7dB	
			0	1	0			5.5dB	
			0	1	1			4dB	
			1	0	0			3dB	
			1	0	1			2dB	
			1	1	0			1dB	
			1	1	1			0dB	
	0	0						Center frequency 240Hz	
	0	1						220Hz	
	1	0						200Hz	
	1	1						180Hz	
0								Quality factor 1.0	
1								2.0	

Table 20. Input section, signal paths A-C (addr. 06-08)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
			0	0	0	0	0	Input gain adjust level -15dB	
			0	0	0	0	1	-14dB	
			0	:	:	:	:	...	
			0	1	1	1	0	-1dB	
			0	1	1	1	1	-0dB	
			1	1	1	1	1	+0dB	
			1	1	1	1	0	<u>+1dB</u>	
			1	:	:	:	:	...	
			1	0	0	0	1	+14dB	
			1	0	0	0	0	+15dB	
0	0	0						Input select Tuner	
0	0	1						CD	
0	1	0						MD / Phone	
0	1	1						CD-Changer (quasi-differential)	
1	0	0						AUX./Navigation (quasi-differential)	
1	0	1						Navigation (mono-Mix)	
1	1	0						AC3in-monitor (from OUT-section)	
1	1	1						Full mute	

Table 21. Input section; other settings (addr. 09)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
							0	Unused , do not alter	
						0		Soft-mute, signal path A No mute	
						1		Mute	
					0			Soft-mute, signal path B No mute	
					1			Mute	
				0				Soft-mute, signal path C No mute	
				1				Mute	
		1	1					Unused , do not alter	
	0							MD-mode Single ended, stereo (e.g. Minidisk)	
	1							<u>Full differential, mono</u> (e.g. external Phone)	
0								Fast-charge (quasi-differential inputs) Release	
1								Engage	

Table 22. Output section, signal path 0 (addr. 10)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
						0	0	Input select Main signal path Output select	
						0	1	AC0in	
						1	0	AC3in	
						1	1	Main signal path PRE-Tone select	
				0	0			Interrupts select, right channel Not allowed	
				0	1			Interrupt enable	
				1	0			Interrupt, 50% signal mix	
				1	1			<u>Interrupt bypass</u> , normal operation	
		0	0					Interrupts select, left channel Not allowed	
		0	1					Interrupt enable	
		1	0					Interrupt, 50% signal mix	
		1	1					<u>Interrupt bypass</u> , normal operation	
	1							Unused , do not alter	
0								Interrupt Pre-select (common for all paths) Navigation	
1								Phone	

Table 23. Output section, signal path 1 and 2 (addr. 11)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
						0	0	Input select signal path1 Main signal path Output select	
						0	1	AC1in	
						1	0	AC3in	
						1	1	Main signal path PRE-Tone select	
					0			Interrupts select, right channel signal path 1 Interrupt enable	
					1			<u>Interrupt bypass</u> , normal operation	
				0				Interrupts select, left channel signal path 1 Interrupt enable	
				1				<u>Interrupt bypass</u> , normal operation	
		0	0					Input select signal path2 Main signal path Output select	
		0	1					AC2in	
		1	0					AC3in	
		1	1					Main signal path PRE-Tone select	
	0							Interrupts select, right channel signal path 2 Interrupt enable	
	1							<u>Interrupt bypass</u> , normal operation	
0								Interrupts select, left channel signal path 2 Interrupt enable	
1								<u>Interrupt bypass</u> , normal operation	

Table 24. Output section, high-pass filters (addr. 12)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
					0	0	0	Corner frequency , High-pass signal path 0 40Hz 60Hz 80Hz 100Hz 120Hz 150Hz 180Hz 220Hz
					0	0	1	
					0	1	0	
					0	1	1	
					1	0	0	
					1	0	1	
					1	1	0	
					1	1	1	
				0				Bypass , High-pass signal path 0 Filter bypass Filter insert
				1				
	0	0	0					Corner frequency , High-pass signal path 1 40Hz 60Hz 80Hz 100Hz 120Hz 150Hz 180Hz 220Hz
	0	0	1					
	0	1	0					
	0	1	1					
	1	0	0					
	1	0	1					
	1	1	0					
	1	1	1					
0								Bypass , High-pass signal path 1 Filter bypass Filter insert
1								

Table 25. Output section, volume 0L, 0R, 1L, 1R, 2L, 2R (addr. 13-16, 18, 19)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
								Volume level	
	0	0	0	1	:	:	:	Not allowed	
				1	0	0	1	+25dB	
				1	0	0	0	+24dB	
	0	0	0	:	:	:	:	...	
				0	0	0	1	+17dB	
				0	0	0	0	+16dB	
				1	1	1	1	+15dB	
	0	0	1	1	1	1	0	+14dB	
				:	:	:	:	...	
				0	0	0	1	+1dB	
				0	0	0	0	+0dB	
				0	0	0	0	-0dB	
	0	1	0	0	0	0	1	-1dB	
				:	:	:	:	...	
				1	1	1	0	-14dB	
				1	1	1	1	-15dB	
				0	0	0	0	-16dB	
	0	1	1	0	0	0	1	-17dB	
				:	:	:	:	...	
				1	1	1	0	-30dB	
				1	1	1	1	-31dB	
				0	0	0	0	-32dB	
	1	0	0	0	0	0	1	-33dB	
				:	:	:	:	...	
				1	1	1	0	-46dB	
				1	1	1	1	-47dB	
				0	0	0	0	-48dB	
	1	0	1	0	0	0	1	-49dB	
				:	:	:	:	...	
				1	1	1	0	-62dB	
				1	1	1	1	-63dB	
				0	0	0	0	-64dB	
	1	1	0	0	0	0	1	-65dB	
				:	:	:	:	...	
				1	1	1	0	-78dB	
				1	1	1	1	-79dB	
	1	1	1	X	X	X	X	Mute	
0								Soft-step	
1								On	
								Off	

Table 26. Output section, subwoofer low-pass filter (addr. 17)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
							0	Unused , do not alter
				X	0	0		Monitor select Signal path 0 (before Soft-mute)
				X	0	1		Signal path 1 (before Soft-mute)
				0	1	0		Low-pass filter (Subwoofer enable)
				1	1	0		Mono-sum bypass
				X	1	1		Stereo bypass (direct through)
	0	0	0					Corner frequency 120Hz
	0	0	1					100Hz
	0	1	0					80Hz
	0	1	1					60Hz
	1	X	X					50Hz
	1	1	1					50Hz
0								Phase No shift
1								Inverted

Table 27. Output section, bus-mutes (addr. 20)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
							0	Unused , do not alter
						0		Soft-mute, right channel signal path 0 No mute
						1		Mute
					0			Soft-mute, left channel signal path 0 No mute
					1			Mute
				0				Soft-mute, right channel signal path 1 No mute
				1				Mute
			0					Soft-mute, left channel signal path 1 No mute
			1					Mute
		0						Soft-mute, right channel signal path 2 No mute
		1						Mute
	0							Soft-mute, left channel signal path 2 No mute
	1							Mute
1								Unused , do not alter

Table 28. DC-detector and other output section settings (addr. 21)

MSB							LSB	FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
							0 1	Line drivers gain 9dB 5.5dB
						0 1		PAout0 (front) mute No mute Mute
					0 1			PAout1 (rear) mute No mute Mute
				0 1				DCErrror output behavior Forced high level by mute; ⁽¹⁾ Normal operation, see description Chapter 5.5 .
		0 0 1 1	0 1 0 1					Zero-comparator Window size ± 100mV ± 75mV ± 50mV ± 25mV
0 0 1 1	0 1 0 1							Spike rejection time constant 11µs 22µs 33µs 44µs

1. DCErrror output high for OUTsection signal paths 1&2 muted or all PAout muted

Table 29. Soft-mute and soft-step fader time (addr. 22)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				1	1	1	0	Unused , do not alter	
				0				Input selection procedure Soft-mute completion time programmed according to bits D6 and D7 Soft-mute completion time fixed to 0.5ms	
		0	0					Soft-step completion time 0.32ms	
		0	1					0.64ms	
		1	0					1.28ms	
		1	1					2.56ms	
0	0							Soft-mute completion time 0.25ms	
0	1							0.5ms	
1	0							10ms	
1	1							5ms	

Table 30. Spectrum analyzer settings (addr. 23)

MSB							LSB		FUNCTION
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
							0	Run/stop (internal clocking) Stop	
							1	Run	
						0		Filter quality High	
						1		Low	
					0			Reset mode SAres-pin triggered reset	
					1			Auto-reset mode	
				0				Source select Mono-sum of MUXA-outputs	
				1				SAin-pin	
1	1	1	1					Unused , do not alter	

Table 31. Testing * (addr. 31)

MSB							LSB		FUNCTION	
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
								0	Device clock Enable internal clock generation	
								1	Allow external clocking in <i>fast-mode</i>	
				1	1	1			Unused , do not alter	
									Test selector	
	0	0	0						TUNER L out: DCDet., lower TC-Vth Spec.Anal. 60Hz-bandpass Spec.Anal. 160Hz-bandpass Spec.Anal. 400Hz-bandpass Spec.Anal. 1kHz-bandpass Spec.Anal. 2,5kHz-bandpass Spec.Anal. 6,3kHz-bandpass Spec.Anal. 16kHz-bandpass	TUNER R out: DCDet., upper TC-Vth 5,5V CMOS-supply DCDet., time constant 200kHz reference clock actual Soft-Mute clock actual Soft-Step clock SC-reference, left chan. DC-Offset monitor point
	0	0	1							
	0	1	0							
	0	1	1							
	1	0	0							
	1	0	1							
	1	1	0							
	1	1	1							
0									Test mode Enabled *	
1									Disabled	

Successfully entering the test-mode requires to set bit D6 of the sub address (test mode-bit) to "1". In test-mode, the TUNER L&R inputs are reconfigured as output for the selected test signals

Note: This byte is used for testing and/or evaluation purposes only and must not be set to other values than the default "11111110" in the application.

8 Application information

Figure 27. Typical application connections diagram

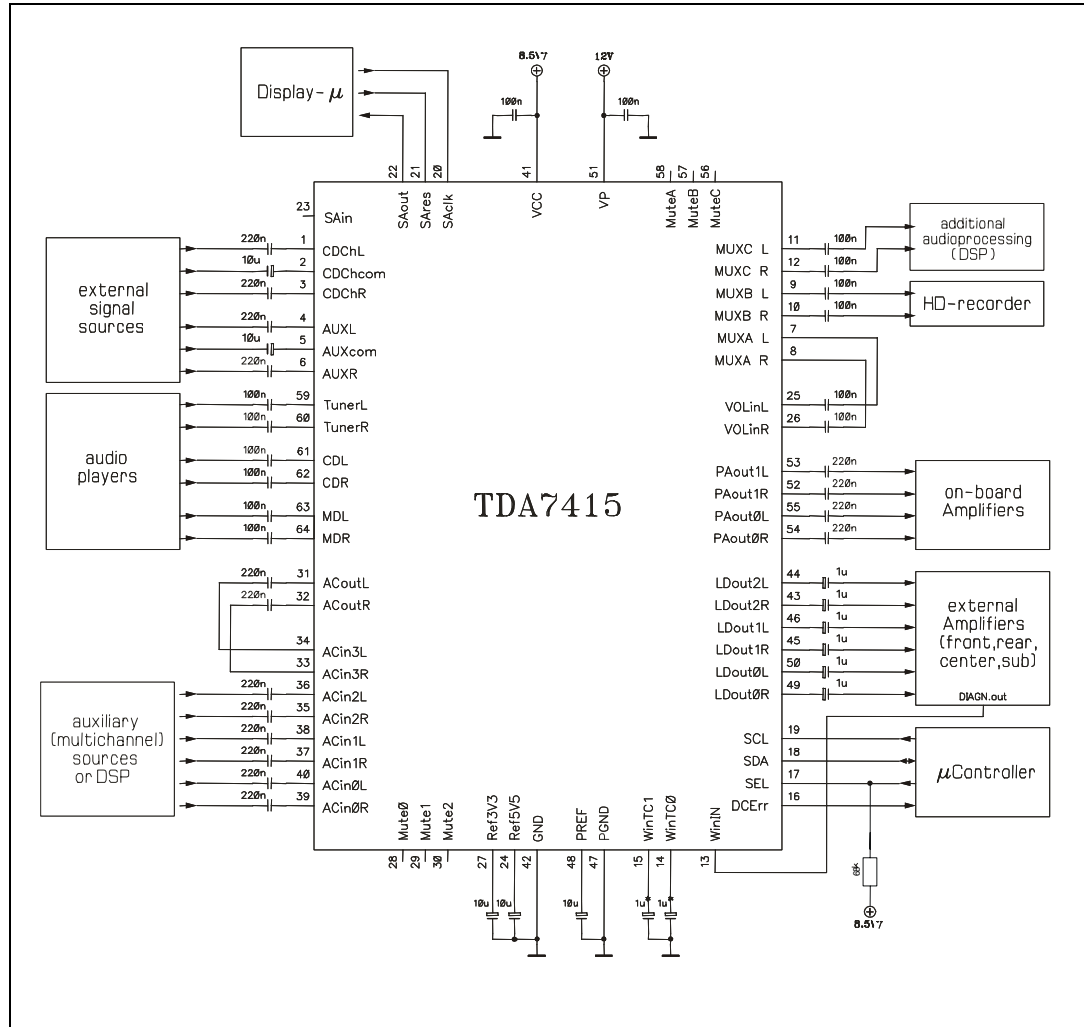


Figure 27 shows a proposal for a typical application. - However, the figure only represents one possible interconnection scheme with other devices (The shaded blocks could represent a complex digital sound reproducing/processing system). For simplicity, this proposal assumes the system designer not to take advantage from the direct muting feature and therefore let the corresponding Mute-pins floating.

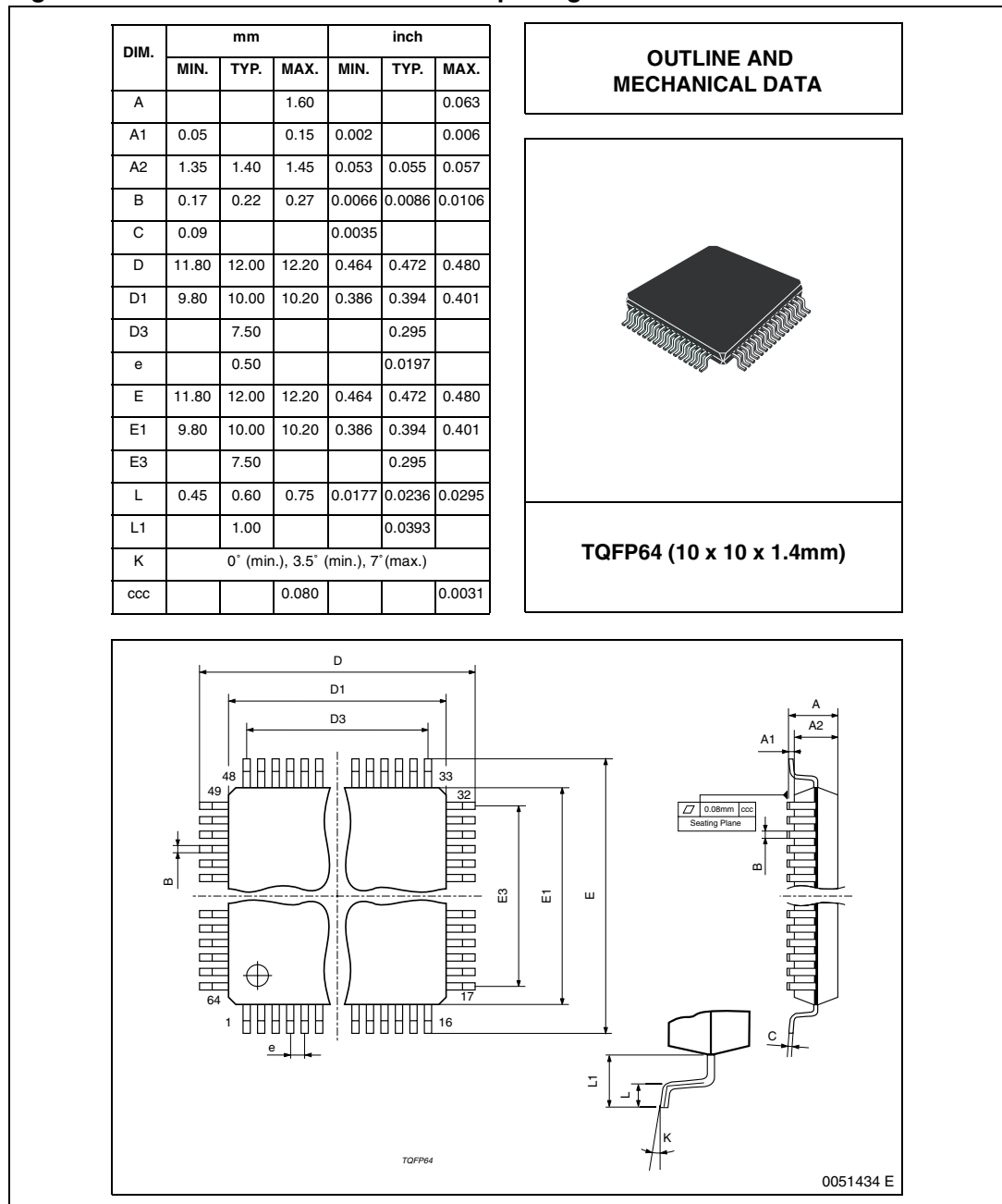
All capacitor values are suggestions with their dimensioning still being dependant on girdling impedances. This is especially true for the capacitors located at the WinTC-pins as can be read in chapter 6.5. **In case the DC-detector function is not assessed in the application it is recommended to short both the WinTC-pins 14 and 15 to device-ground.**

9 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 28. TQFP64 mechanical data and package dimensions



10 Revision history

Table 32. Document revision history

Date	Revision	Changes
26-Oct-2007	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com