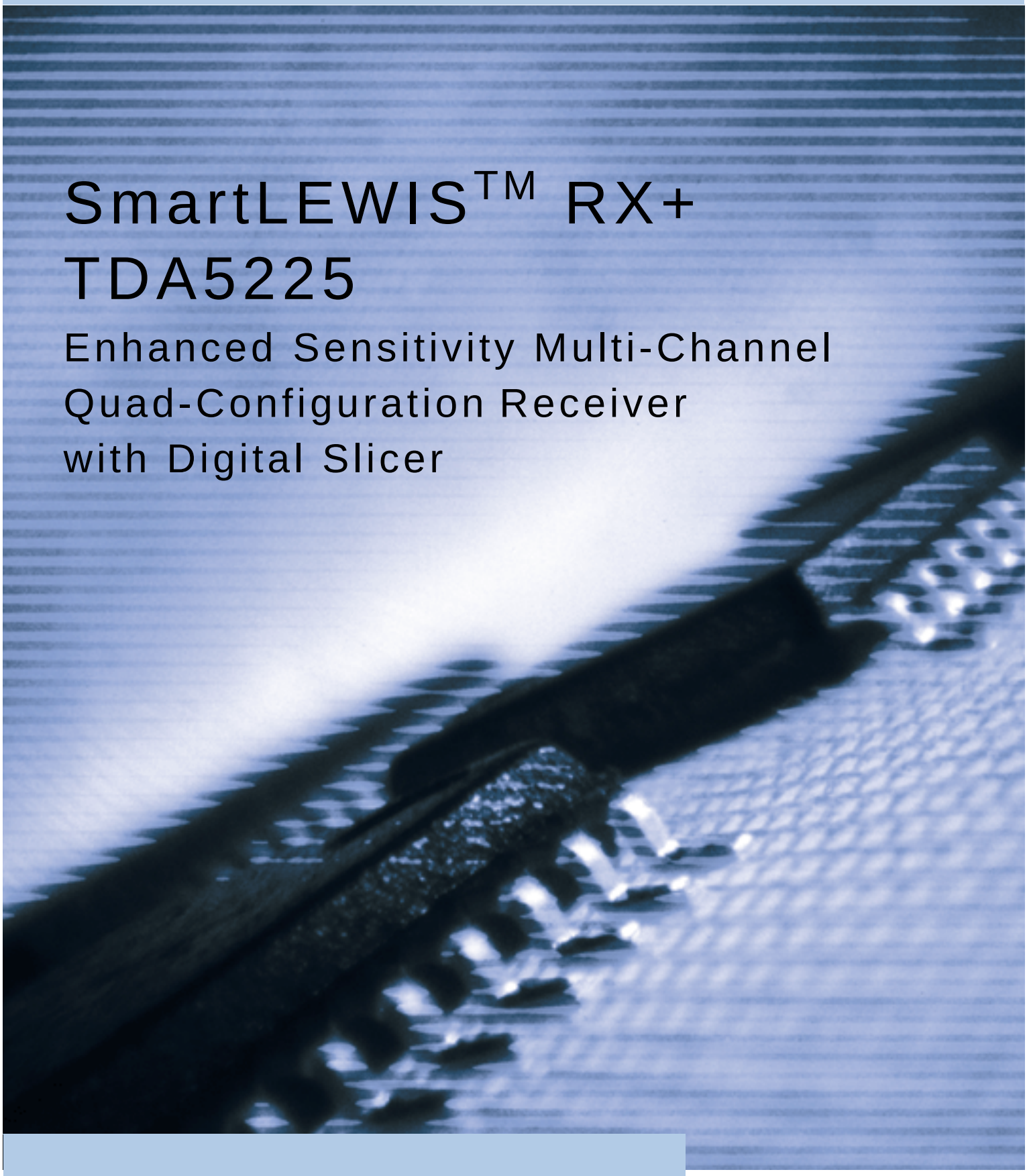

SmartLEWIS™ RX+ TDA5225

Enhanced Sensitivity Multi-Channel Quad-Configuration Receiver with Digital Slicer

Wireless Control

Never stop thinking.

Edition February 19, 2010

Published by Infineon Technologies AG,
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TDA5225

Revision Number:	**010**	
Revision History:	**2010-02-19**	V1.0
Previous Version:	TDA5225_v0.2	

Page	Subjects (major changes since last revision)
Page 26	Update of Figure 9
Page 28	Update of Figure 10
Page 30	AFC limitation added
Page 32	AGC setting proposal added
Page 33	New Section 2.4.6.5 ADC added
Page 34	Additional information on RSSIPRX register inserted
Page 40	Update of Figure 19
Page 41	Update of Figure 20
Page 45	Additional hint on clock and data recovery algorithm of the user software inserted
Page 49	Limitation for ISx readout and Burst-read function added
Page 51	Limitation for Burst-read function added
Page 77	Additional hints added
Page 79	Adaption of Section 4.1
Page 82	New item C7 added
Page 90 f	Comments added for items I6, I7, I8, I9, J11, J12
Page 90	Item J1 updated
Page 95	BOM components C7, C8, L1, R2 and R3 updated

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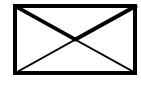

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1 Product Description

1.1 Overview

The IC is a low power ASK/FSK Receiver for the frequency bands 300-320, 425-450, 863-870 and 902-928 MHz.

The chip offers a very high level of integration and needs only a few external components.

The device is qualified to automotive quality standards and operates between -40 and +105°C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

The receiver is realized as a double down conversion super-heterodyne/low-IF architecture each with image rejection. A fully integrated Sigma-Delta Fractional-N PLL Synthesizer allows for high-resolution frequency generation and uses a crystal oscillator as the reference. The on-chip temperature sensor may be utilized for temperature drift compensation via the crystal oscillator.

The high performance down converter is the key element for the exceptional sensitivity performance of the device which take it close to the theoretical top-performance limits. It demodulates the received ASK or FSK data stream independently which can then be accessed via separate pins. The RSSI output signal is converted to the digital domain with an ADC. All these signals are accessible via the 4-wire SPI interface bus. Up to 4 pre-configured telegram parameters can be stored into the device offering independent pre-processing of the received data to an extent not available till now. The down converter can be also configured in single-conversion mode at moderately reduced selectivity performance but at the advantage of omitting the IF ceramic filter.

1.2 Features

- Enhanced sensitivity receiver
- Multi-band/Multi-Channel (300-320, 425-450, 863-870 and 902-928 MHz)
- One crystal frequency for all supported frequency bands
- 21-bit Sigma-Delta Fractional-N PLL synthesizer with high resolution of 10.5 Hz
- Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources
- Up to 12 different frequency channels are supported with 10.5 Hz resolution each
- Ultrafast Wake-up on RSSI
- Selectable IF filter bandwidth and optional external filters possible
- Double down conversion image reject mixer
- ASK and FSK capability
- Automatic Frequency Control (AFC) for carrier frequency offset compensation
- NRZ data processing capability
- Sliced data output
- RSSI peak detectors
- Wake-up generator and polling timer unit
- Unique 32-bit serial number
- On-chip temperature sensor
- Integrated timer usable for external watch unit
- Integrated 4-wire SPI interface bus
- Supply voltage range 3.0 Volts to 3.6 Volts or 4.5 Volts to 5.5 Volts
- Operating temperature range -40 to +105°C
- ESD protection +/- 2 kV on all pins
- Package PG-TSSOP-28

1.3 Applications

- Remote keyless entry systems
- Remote start applications
- Tire pressure monitoring
- Short range radio data transmission
- Remote control units
- Cordless alarm systems
- Remote metering

2 Functional Description

2.1 Pin Configuration

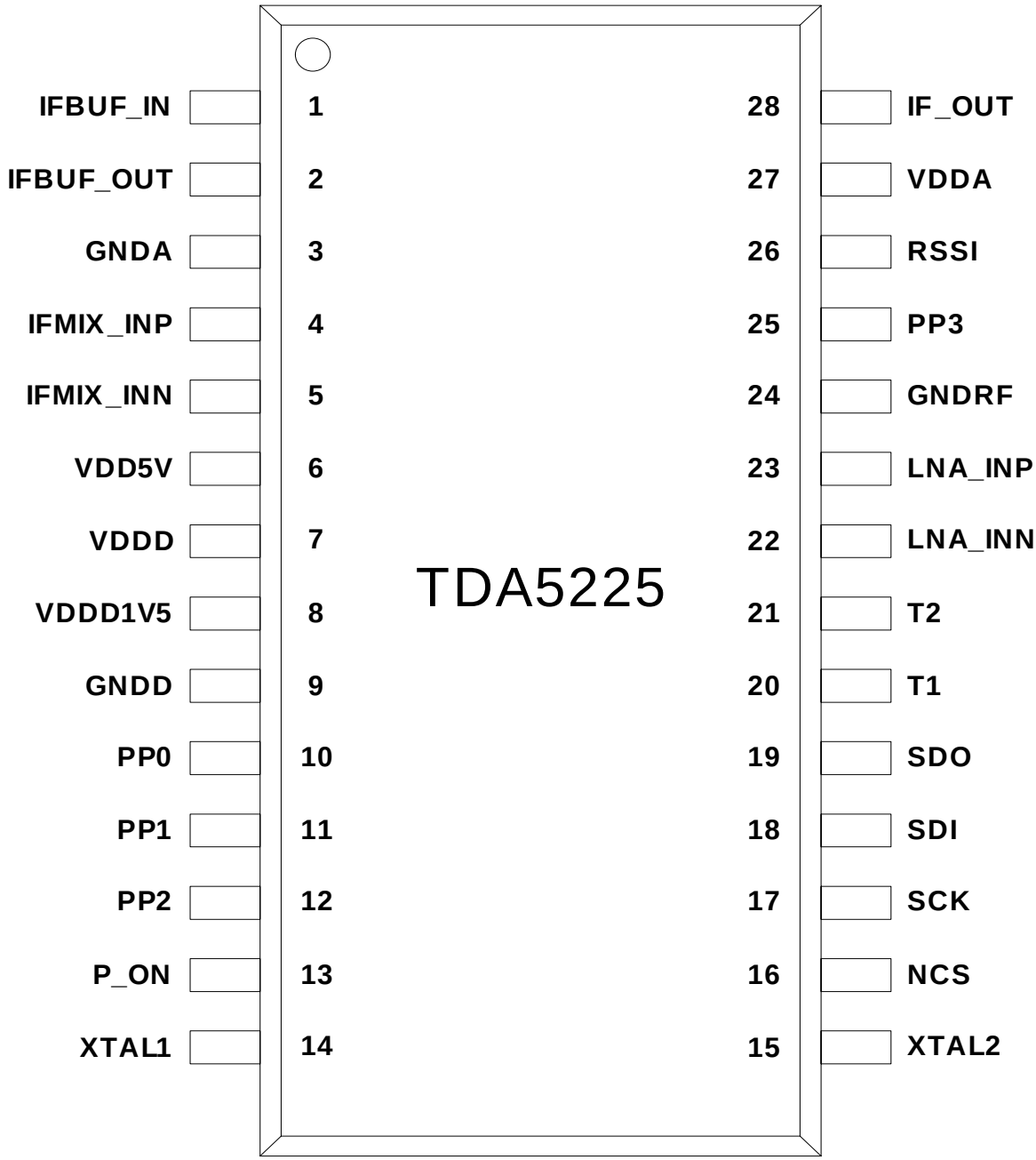
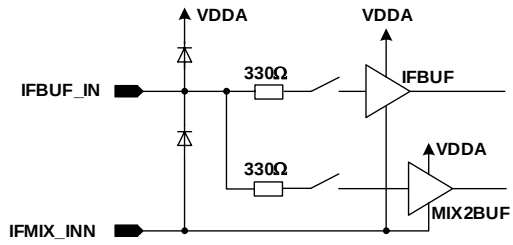
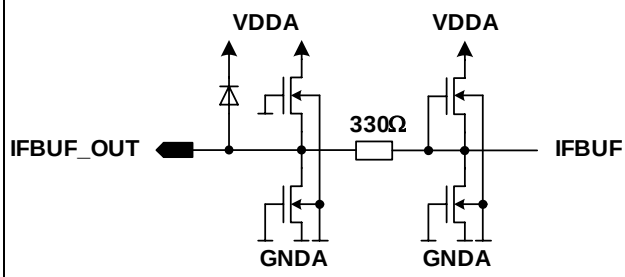
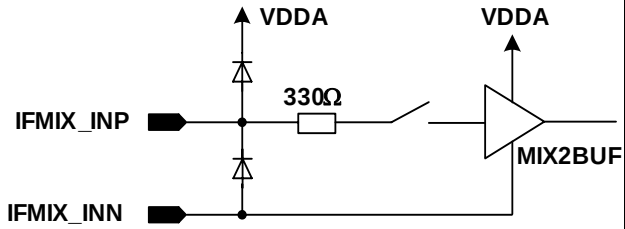
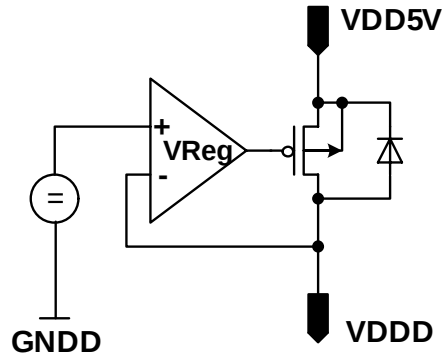
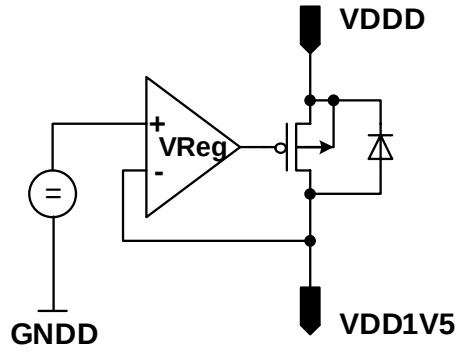
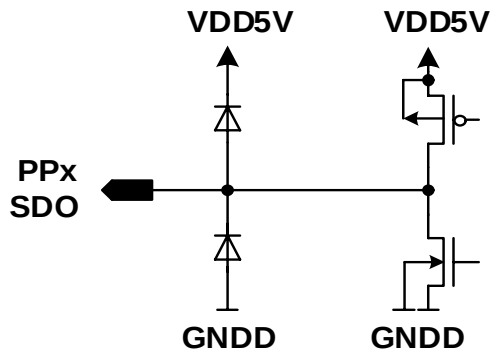


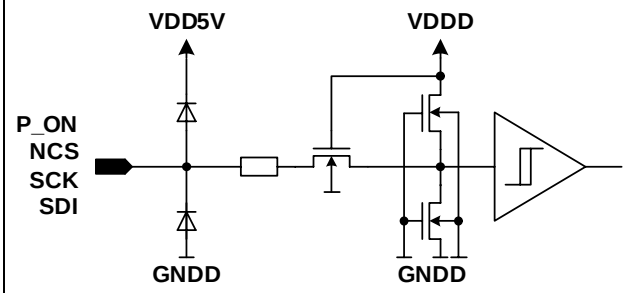
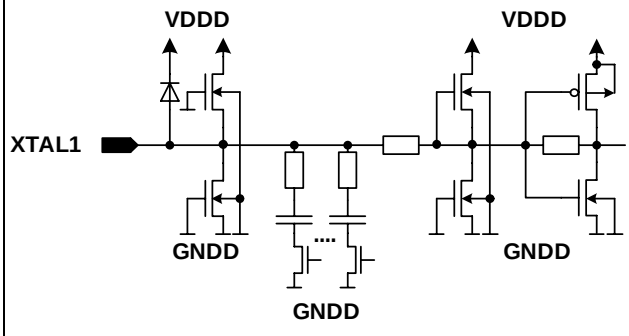
Figure 1 Pin-out

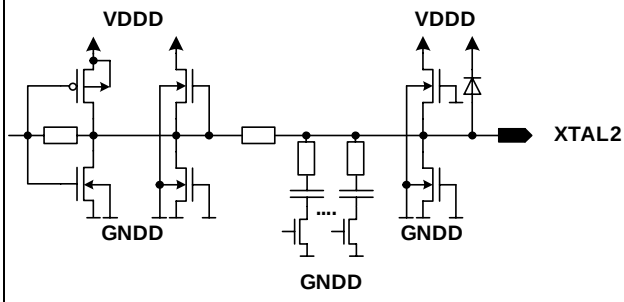
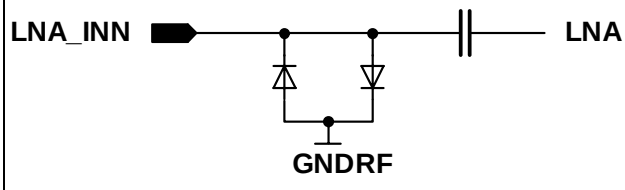
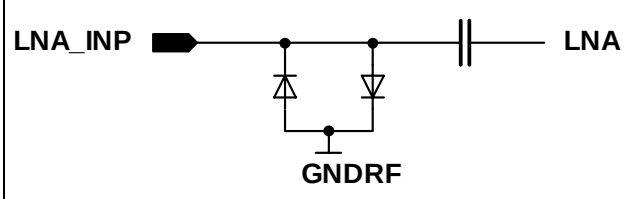
2.2 Pin Definition and Pin Functionality

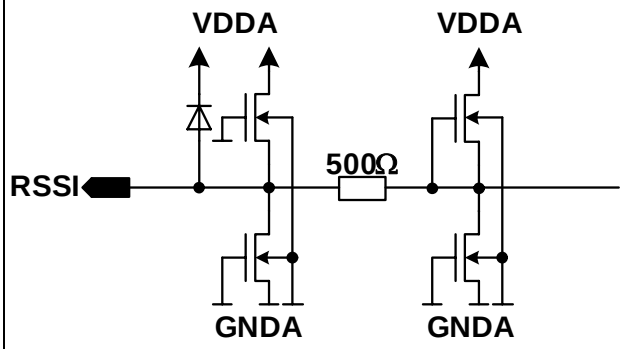
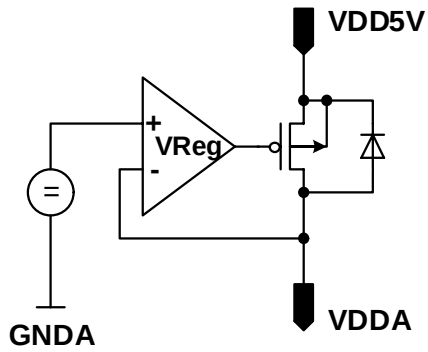
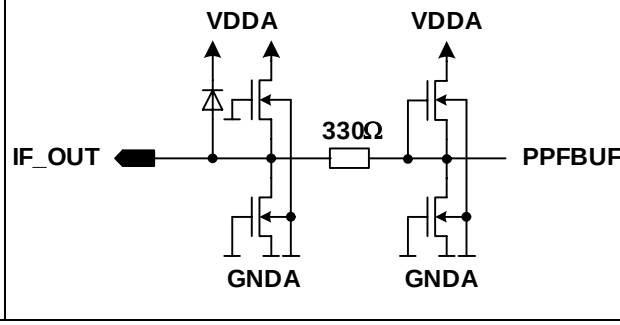
Table 1 Pin Definition and Function

Pin No.	Pad name	Equivalent I/O Schematic	Function
1	IFBUF_IN		Analog input IF Buffer input Note: Input is biased at VDDA/2
2	IFBUF_OUT		Analog output IF Buffer output
3	GNDA		Analog ground
4	IFMIX_INP		Analog input + IF mixer input Note: Input is biased at VDDA/2
5	IFMIX_INN	see schematic of Pin 1 and 4	Analog input. - IF mixer input
6	VDD5V		Analog input 5 Volt supply input

Pin No.	Pad name	Equivalent I/O Schematic	Function
7	VDDD		Analog input digital supply input
8	VDDD1V5		Analog output 1.5 Volt voltage regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR (Special Function Register), default = CLK_OUT

Pin No.	Pad name	Equivalent I/O Schematic	Function
11	PP1	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = DATA
12	PP2	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = NINT
13	P_ON		Digital input power-on reset
14	XTAL1		Analog input crystal oscillator input

Pin No.	Pad name	Equivalent I/O Schematic	Function
15	XTAL2		Analog output crystal oscillator output
16	NCS	see schematic of Pin 13	Digital input SPI enable
17	SCK	see schematic of Pin 13	Digital input SPI clock
18	SDI	see schematic of Pin 13	Digital input SPI data in
19	SDO	see schematic of Pin 10	Digital output SPI data out
20	T1		Digital input, connect to Digital Ground
21	T2		Digital input, connect to Digital Ground
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input + RF input
24	GNDRF		RF analog ground

Pin No.	Pad name	Equivalent I/O Schematic	Function
25	PP3	see schematic of Pin 10	Digital output RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = RX_RUN
26	RSSI		Analog output analog RSSI output/ analog test pin ANA_TST
27	VDDA		Analog input Analog supply
28	IF_OUT		Analog output IF output

2.3 Functional Block Diagram

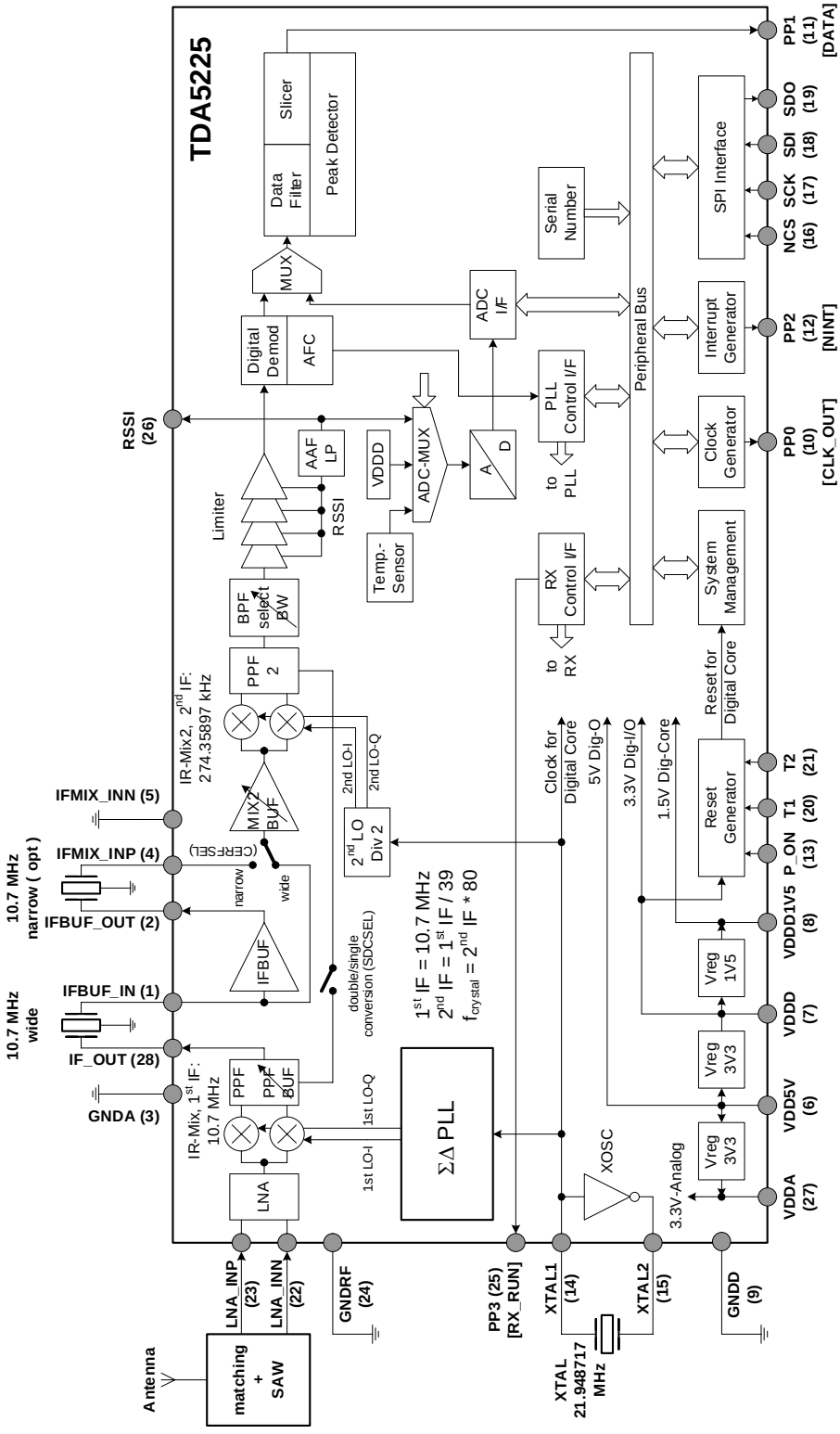


Figure 2 TDA5225 Block Diagram[1)]

1) The function on each PPx port pin can be programmed via SFR (see also **Table 1**). Default values are given in squared brackets in **Figure 2**.

2.4 Functional Block Description

2.4.1 Architecture Overview

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 425-450 MHz, 863-870 MHz, 902-928 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications.
For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

For Multi-Channel systems where even higher channel separation is required, up to two (switchable) external ceramic (CER) filters can be used to improve the selectivity.
An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution.
The harmonic suppressed limiter output signal feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer.
A digital receiver, which comprises RSSI peak detectors, a matched data filter and a data slicer, decodes the received ASK or FSK data stream. The received data signal is accessible via one of the port pins.
The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2^{nd} local oscillator signal. To accelerate the start up time of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

2.4.2 Block Overview

The TDA5225 is separated into the following main blocks:

- **RF / IF Receiver**
- **Crystal Oscillator and Clock Divider**
- **Sigma-Delta Fractional-N PLL Synthesizer**
- **ASK / FSK Demodulator incl. AFC, AGC and ADC**
- **RSSI Peak Detector**
- **Digital Baseband Receiver**
- **Power Supply Circuitry**
- **System Interface**
- **System Management Unit**

2.4.3 RF/IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two low-side injected I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter (optionally by two, decoupled by a buffer amplifier). For moderate or low cost applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency. The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps. For a frequency offset of -150 kHz to -120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configurable via PPCFG2 register.

The frequency relations are calculated with the following formulas:

$$f_{IF1} = 10.7MHz$$

$$f_{IF2} = \frac{f_{IF1}}{39}$$

$$f_{crystal} = f_{IF2} \times 80$$

$$f_{LO2} = \frac{f_{crystal}}{2}$$

$$f_{LO1} = f_{crystal} \times NF_{divider}$$

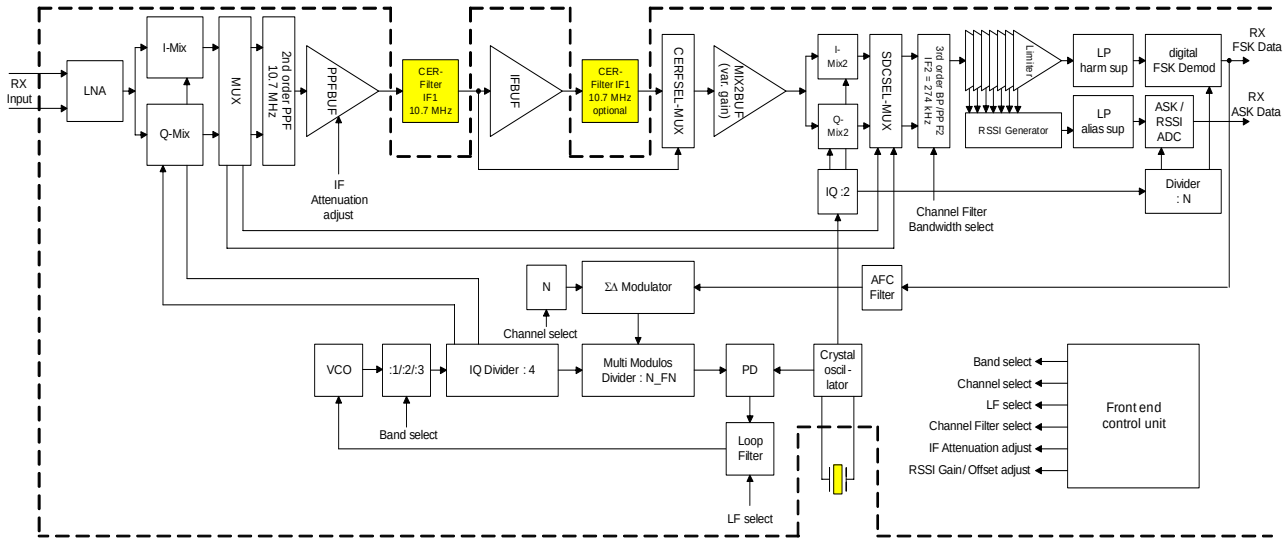


Figure 3 Block Diagram RF Section

The front end of the receiver comprises an LNA, an image reject mixer and a digitally gain controlled buffer amplifier. This buffer amplifier allows the production spread of the on-chip signal strip, of external matching circuitry and RF SAW and ceramic IF filters to be trimmed. The second image reject mixer down converts the first IF to the second IF.

The bandpass filter follows the subsequent formula:

$$f_{center} = \sqrt{f_{corner,\,low} \times f_{corner,\,high}}$$

Therefore asymmetric corner frequencies can be observed. The use of AFC results in more symmetry.
A multi-stage bandpass limiter at a center frequency of 274 kHz completes the receiver chain. The -3dB corner frequencies of the bandpass limiter are typically at 75 kHz and at 520 kHz.
An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC.
The limiter output signal is connected to a digital FSK demodulator.
The immunity against strong interference frequencies (so called blockers) is determined by the available filter bandwidth, the filter order and the 3rd order intercept point of the front end stages. For Single-Channel applications with moderate requirements to the selectivity the performance of the on-chip 3rd order bandpass polyphase filter might be sufficient. In this case no external filters are necessary and a single down conversion architecture can be used, which converts the input signal frequency directly to the 2nd IF frequency of 274 kHz.

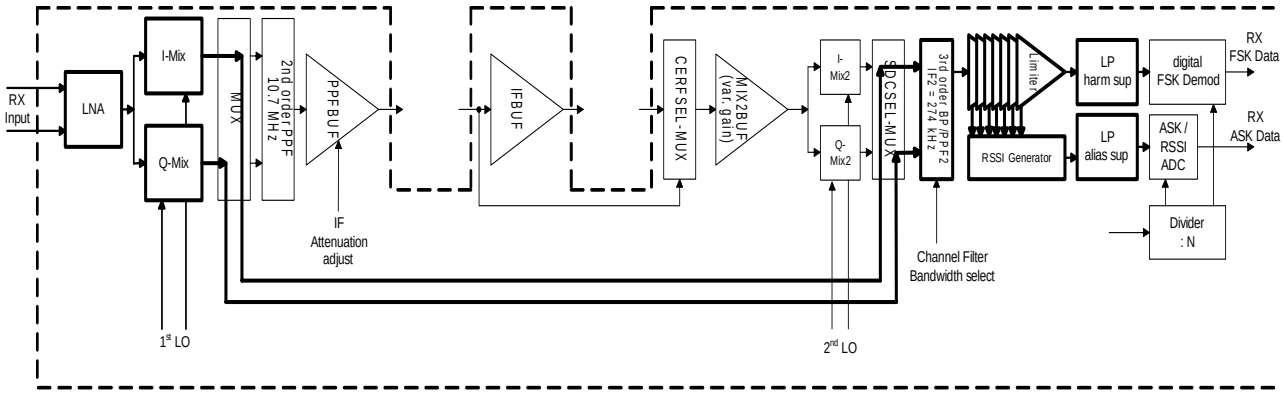


Figure 4 Single Down Conversion (SDC, no external filters required)

For Multi-Channel applications or systems which demand higher selectivity the double down conversion scheme together with one or two external CER filters can be selected. The order of such ceramic filters is in a range of 3, so the selectivity is further improved and a better channel separation is guaranteed.

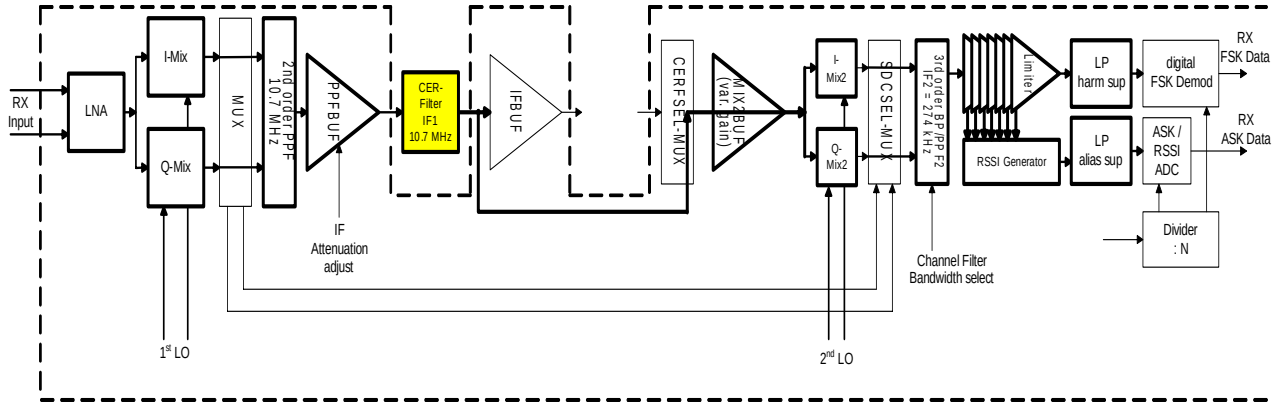


Figure 5 Double Down Conversion (DDC) with one external filter

For applications which demand very high selectivity and/or channel separation even two CER filters may be used. Also in applications where one channel requires a wider bandwidth than the other (e.g. TPMS and RKE) the second filter can be by-passed.

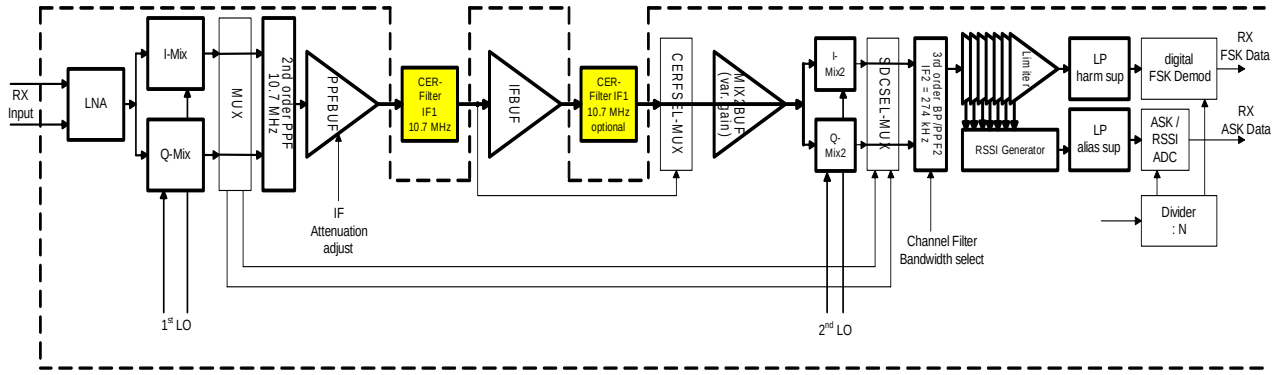


Figure 6 Double Down Conversion (DDC) with two external filters

2.4.4 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator which operates together with the crystal in parallel resonance mode. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly detuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration registers XTALCALx. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the desired value. The SFR control bit XTALHPMS can be used to activate the High Precision Mode also during SLEEP Mode.

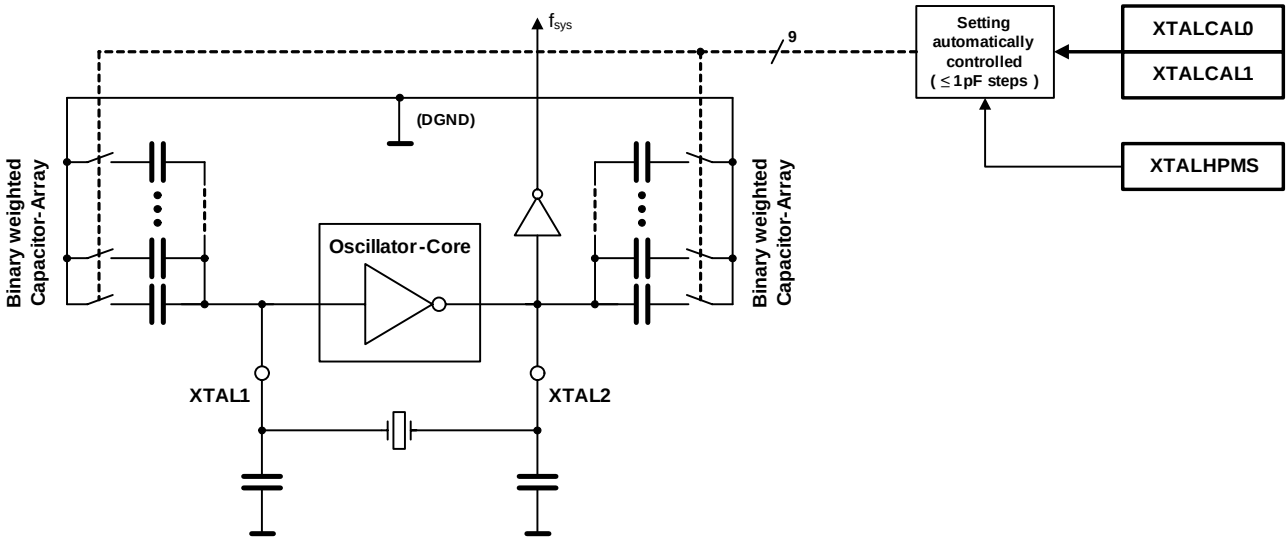


Figure 7 Crystal Oscillator

Recommended Trimming Procedure

- Set the registers XTALCAL0 and XTALCAL1 to the expected nominal values
- Set the TDA5225 to Run Mode Slave
- Wait for 0.5ms minimum
- Trim the oscillator by increasing and decreasing the values of XTALCAL0/1
- Register changes larger than 1 pF are automatically handled by the TDA5225 in 1 pF steps
- After the Oscillator is trimmed, the TDA5225 can be set to SLEEP mode and keeps these values during SLEEP mode
- Add the settings of XTALCAL0/1 to the configuration. It must be set after every power up or brownout!

Using the High Precision Mode

As discussed earlier, the TDA5225 allows the crystal oscillator to be trimmed by the use of internal trim capacitors. It is also possible to use the trim functionality to compensate temperature drift of crystals.

During Run Mode (always when the receiver is active) the capacitors are automatically connected and the oscillator is working in the High Precision Mode.

On entering SLEEP Mode, the capacitors are automatically disconnected to save power.

If the High Precision Mode is also required for SLEEP Mode, the automatic disconnection of trim capacitors can be avoided by setting XTALHPMS to 1 (enable XTAL High Precision Mode during SLEEP Mode).

External Clock Generation Unit

A built in programmable frequency divider can be used to generate an external clock source out of the crystal reference. The 20 bit wide division factor is stored in the registers CLKOUT0, CLKOUT1 and CLKOUT2. The minimum value of the programmable frequency divider is 2. This programmable divider is followed by an additional divider by 2, which generates a 50% duty cycle of the CLK_OUT signal. So the maximum frequency at the CLK_OUT signal is the crystal frequency divided by 4. The minimum CLK_OUT frequency is the crystal frequency divided by 2^{21}.

To save power, this programmable clock signal can be disabled by the SFR control bit CLKOUTEN. In this case the external clock signal is set to low.

The resulting CLK_OUT frequency can be calculated by:

$$f_{CLKOUT} = \frac{f_{sys}}{2 \cdot divisionfactor}$$

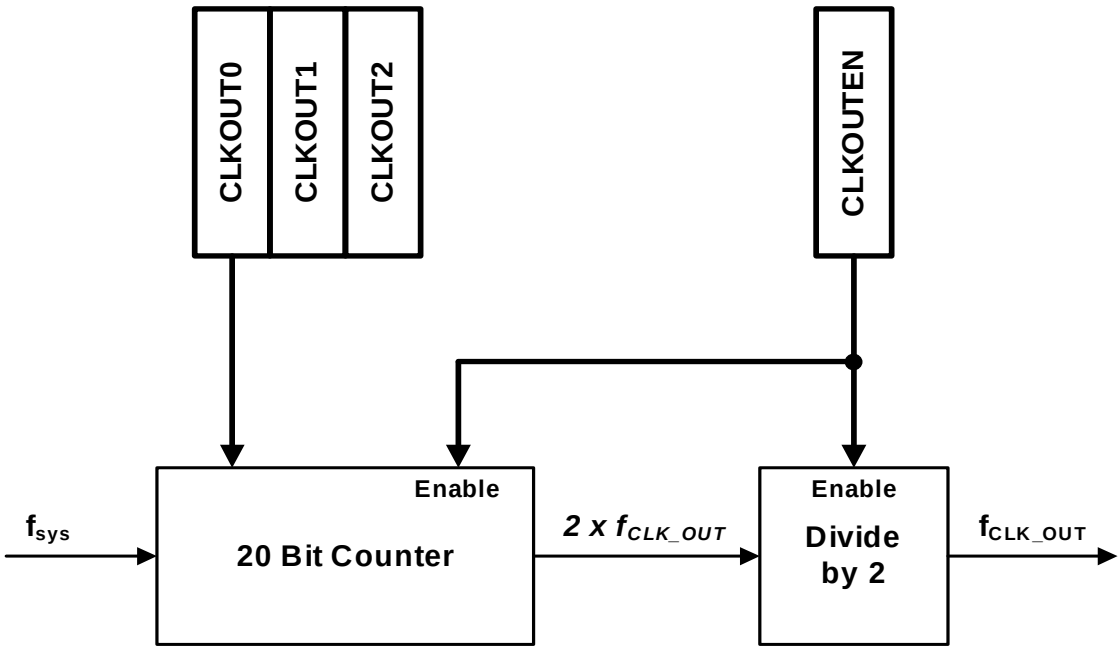


Figure 8 External Clock Generation Unit

The maximum CLK_OUT frequency is limited by the driver capability of the PPx pin and depends on the external load connected to this pin. Please be aware that large loads and/or high clock frequencies at this pin may interfere with the receiver and reduce performance.

After Reset the PPx pin is activated and the division factor is initialized to 11 (equals f_{CLK_OUT} = 998 kHz).

A clock output frequency higher than 1 MHz is not supported.

For high sensitivity applications, the use of the external clock generation unit is not recommended.

2.4.5 Sigma-Delta Fractional-N PLL Block

The Sigma-Delta Fractional-N PLL is fully integrated on chip. The ***V****oltage* ***C****ontrolled* ***O****scillator* (VCO) with on-chip LC-tank runs at approximately 3.6 GHz and is first divided with a band select divider by 1, 2 or 3 and then with an I/Q-divider by 4 which provides an orthogonal local oscillator signal for the first image reject mixer with the necessary high accuracy.
The multi-modulus divider determines the channel selection and is controlled by a 3rd order Sigma-Delta Modulator (*SDM*). A type IV phase detector, a charge pump with programmable current and an on-chip loop filter closes the phase locked loop.

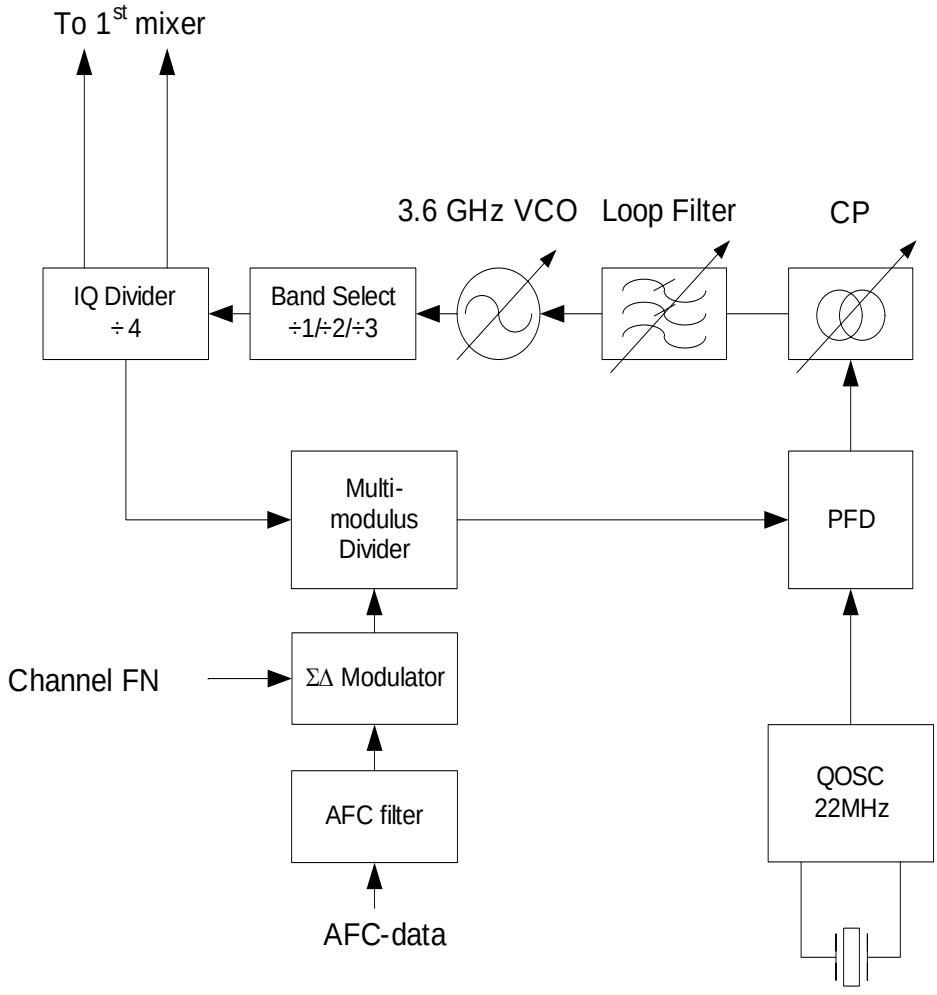


Figure 9 Synthesizer Block Diagram

When defining a Multi-Channel system, the correct selection of channel spacing is extremely important. A general rule is not possible, but following must be considered:

• If an additional SAW filter is used, all channels including their tolerances have to be inside the SAW filter bandwidth.

• The distance between channels must be high enough, that no overlapping can occur. Strong input signals may still appear as recognizable input signal in the neighboring channel because of the limited suppression of IF Filters. Example: a typical 330kHz IF filter has at 10.3 MHz (10.7 MHz - 0.4 MHz) only 30 dB suppression. A -70 dBm input signal appears like a -100 dBm signal, which is inside the receiver sensitivity. In critical cases the use of two IF filters must be considered. See also **Chapter 2.4.3 RF/IF Receiver**.

2.4.5.1 PLL Dividers

The divider chain consists of a band select divider 1/2/3, an I/Q-divider by 4 which provides an orthogonal 1st local oscillator signal for the first image reject mixer with the necessary high accuracy and a multi-modulus divider controlled by the Sigma-Delta Modulator. With the band select divider, the wanted frequency band is selected. Divide by 1 selects the 915 MHz and 868 MHz band, divide by 2 selects the 434 MHz band and divide by 3 selects the 315 MHz band. The ISM band selection is done via bit group BANDSEL in x_PLLINTC1 register.

2.4.5.2 Digital Modulator

The 3rd order ***Sigma-Delta Modulator (SDM)*** has a 22 bit wide input word, however the LSB is always high, and is clocked by the XTAL oscillator. This determines the achievable frequency resolution.

The ***Automatic Frequency Control Unit*** filters the actual frequency offset from the FSK demodulator data and calculates the necessary correction of the divider factor to achieve the nominal IF center frequency.

2.4.6 ASK and FSK Demodulator

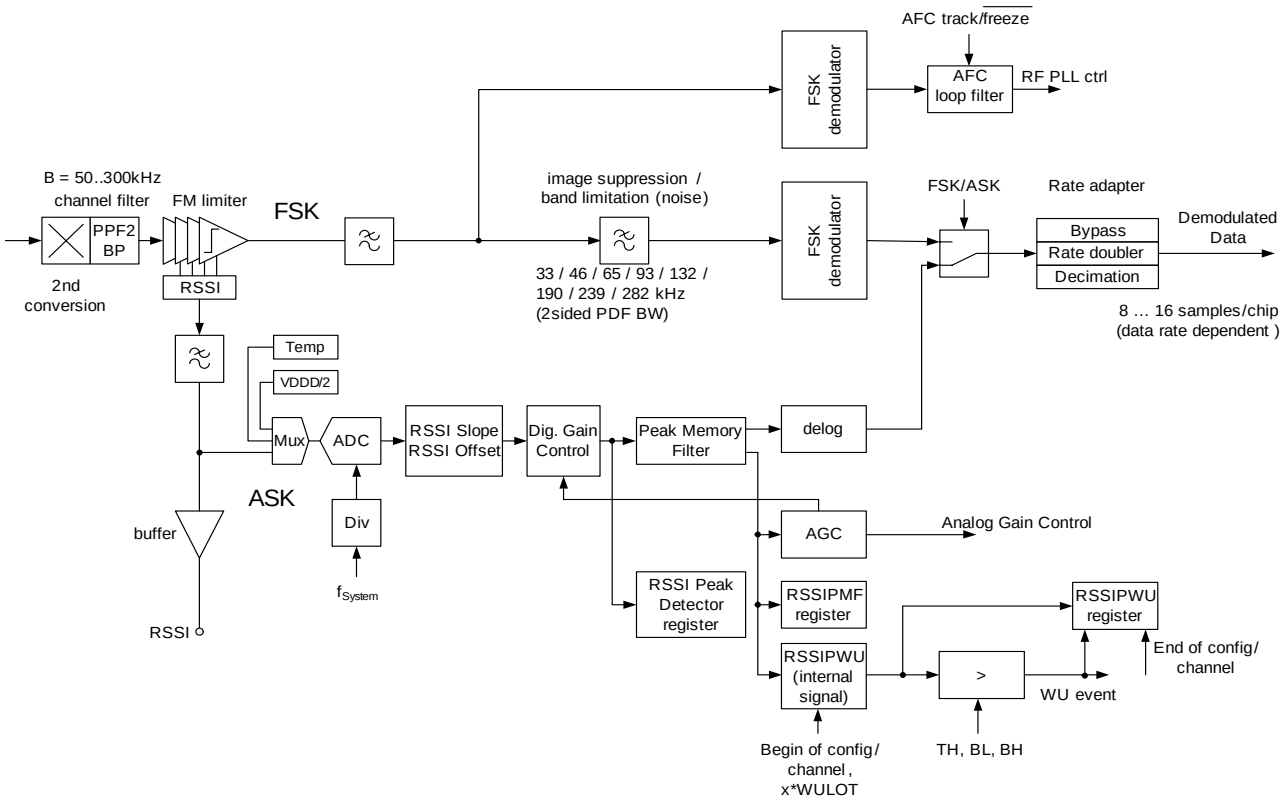


Figure 10 Functional Block Diagram ASK/FSK Demodulator

The IC comprises two separate demodulators for ASK and FSK.
After combining FSK and ASK data path, a sampling rate adaptation follows to meet an output oversampling between 8 and 16 samples per chip. Finally, an oversampling of 8 samples per chip can be achieved using a fractional sample rate converter (SRC) with linear interpolation (for further details see **Figure 15**).

2.4.6.1 ASK Demodulator

The RSSI generator delivers a DC signal proportional to the applied input power at a logarithmic scale (dBm) and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC. For the AM demodulation a signal proportional to the linear power is required. Therefore a conversion from logarithmic scale to linear scale is necessary. This is done in the digital domain by a nonlinear filter together with an exponential function. The analog RSSI signal after the anti-aliasing filter is available at the RSSI pin via a buffer amplifier. To enable this buffer the SFR control bit RSSIMONEN must be set. The anti-aliasing filter can be by-passed for visualization on the RSSI pin (see AAFBYP control bit).

2.4.6.2 FSK Demodulator

The limiter output signal, which has a constant amplitude over a wide range of the input signal, feeds the FSK demodulator. There is a configurable lowpass filter in front of the FSK demodulation to suppress the down conversion image and noise/limiter harmonics (FSK Pre-Demodulation Filter, PDF). This is realized as a 3rd order digital filter. The sampling rate after FSK demodulation is fixed and independent from the target data rate.

2.4.6.3 Automatic Frequency Control Unit (AFC)

In front of the image suppression filter a second FSK demodulator is used to derive the control signal for the **Automatic Frequency Control Unit**, which is actually the DC value of the FSK demodulated signal. This makes the AFC loop independent from signal path filtering and allow so a wider frequency capture range of the AFC. The derivation of the AFC control signal is preferably done during the DC free preamble and is then frozen for the rest of the datagram.

Since the digital FSK demodulator determines the exact frequency offset between the received input frequency and the programmed input center frequency of the receiver, this offset can be corrected through the sigma delta control of the PLL. As shown in **Figure 10**, for AFC purposes a parallel demodulation path is implemented. This path does not contain the digital low pass filter (PDF, Pre-Demodulation Filter). The entire IF bandwidth, filtered by the analog bandpass filter only, is processed by the AFC demodulator.

There are two options for the active time of the AFC loop:

- 1. always on
- 2. active for a programmable time relative to a signal identification event

In the latter case the AFC can either be started or frozen relative to the signal identification. After the active time the offset for the sigma-delta PLL (SD PLL) is frozen.

The programming of the active time is especially necessary in case the expected frame structure contains a gap (noise) between wake-up and payload in order to avoid the AFC from drifting.

AFC works both for FSK and ASK. In the latter case the AFC loop only regulates during ASK data = high.

The maximum frequency offset generated by the AFC can be limited by means of the x_AFCLIMIT register. This limit can be used to avoid the AFC from drifting in the presence of interferers or when no RF input signal is available (AFC wander). A maximum AFC limit of 42 kHz is recommended. AFC wandering needs to be kept in mind especially when using Run Mode Slave.

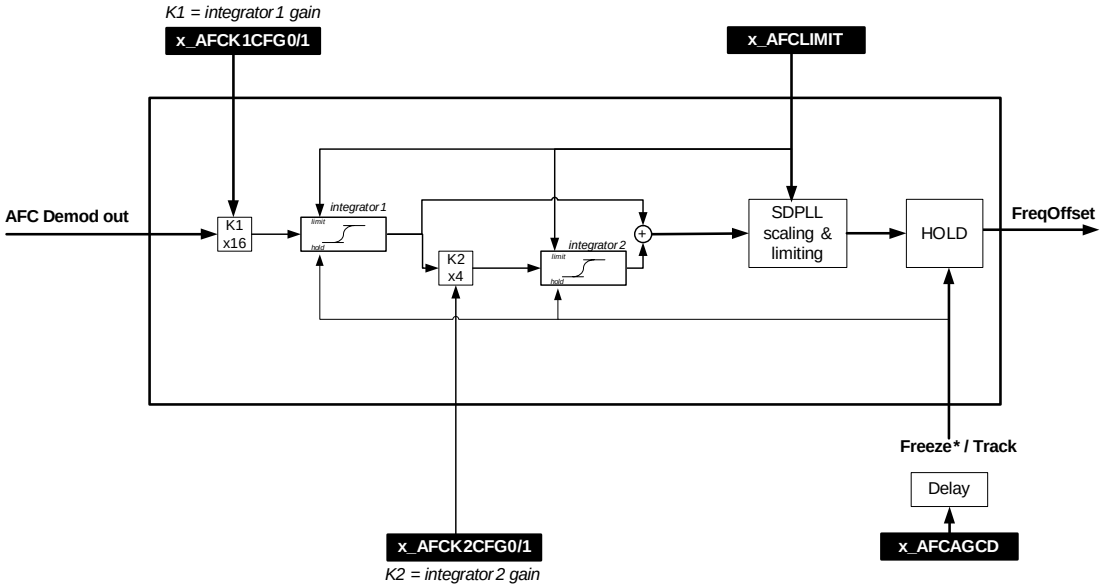


Figure 11 AFC Loop Filter (I-PI Filtering and Mapping)

The bandwidth (and thus settling time) of the loop is programmed by means of the integrator gain coefficients K1 and K2 (x_AFCK1CFG and x_AFCK2CFG register).

K1 mainly determines the bandwidth. K2 influences the dynamics/damping (overshoot) - smaller K2 means smaller overshoot, but slower dynamics. The bandwidth of the AFC loop is approximately 1.3*K1.

To avoid residual FM, limiting the AFC BW to 1/20 ~ 1/40 of the bit rate is suggested, therefore K1 must be set to approximately 1/50 ~ 1/100 of the bit rate. For most applications K2 can be set equal to K1 (overshoot is then <25%).

When very fast settling is necessary K1 and K2 can be increased up to bit rate/10, however, in this case approximately 1dB sensitivity loss is to be expected due to the AFC counteracting the input FSK signal.

AFC limitation at Local Oscillator (LO) frequencies at multiples of reference frequency (f_xtal). When AFC is activated and AFC drives the wanted LO frequency over the integer limit of Sigma Delta (SD) modulator, the SD modulator stucks at frac=1.0 or frac=0.0 due to saturation. So when AFC can change the integer value for the LO (register x_PLLINTCy) within the frequency range LO-frequency +/- AFC-limit, a change of the LO injection side or a smaller AFC-limit is recommended.

The frequency offset found by AFC (AFC loop filter output) can be readout via register AFCOFFSET, when AFC is activated. The value is in signed representation and has a frequency resolution of 2.68 kHz/digit. The output can be limited by the x_AFCLIMIT register.

2.4.6.4 Digital Automatic Gain Control Unit (AGC)

Automatic Gain Control (AGC) is necessary mainly because of the limited dynamic range of the on-chip bandpass filter (BPF). The dynamic range reduces to less than 60dB in case of minimum BPF bandwidth.

AGC is used to cover the following cases:

1. ASK demodulation at large input signals
2. RSSI reading at large input signals
3. Improve IIP3 performance in either FSK or ASK mode

The 1st IF buffer (PPFBUF, see **Figure 3**) can be fine tuned "manually" by means of 4 bits thus optimizing the overall gain to the application (attenuation of 0dB to -12dB by means of IFATT0 to IFATT15 in DDC mode; SDC mode has lower IFATT range). This buffer allows the production spread of external components to be trimmed.

The gain of the 2nd IF path is set to three different values by means of an AGC algorithm. Depending on whether the receiver is used in single down conversion or in double down conversion mode the gain control in the 2nd IF path is either after the 2nd poly-phase network or in front of the 2nd mixer.

The AGC action is illustrated in the RSSI curve below:

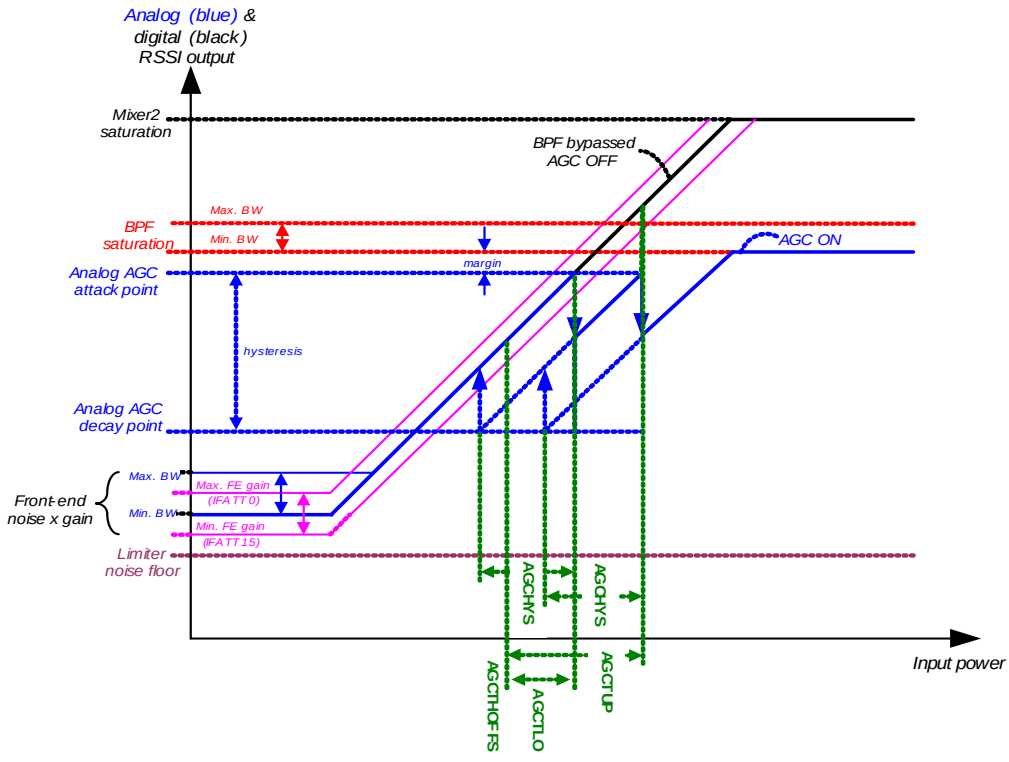


Figure 12 Analog RSSI output curve with AGC action ON (blue) vs. OFF (black)

Digital RSSI, AGC and Delog:

In order to match the analog RSSI signal to the **digital RSSI** output a correction is necessary. It adds an offset (RSSIOFFS) and modifies the slope (RSSISLOPE) such that standardized AGC levels and an appropriate DELOG table can be applied.

Upon entering the **AGC unit** the digital RSSI signal is passed through a Peak Memory Filter (PMF). This filter has programmable up and down integration time constants (PMFUP, PMFDN) to set attack respectively decay time. The integration time for decay time must be significantly longer than the attack time in order to avoid the AGC interfering with the ASK modulation.

The integrator is followed by two digital Schmitt triggers with programmable thresholds (AGCTLO; AGCTUP) - one Schmitt trigger for each of the two attack thresholds (two digital AGC switching points). The hysteresis of the Schmitt triggers is programmable (AGCHYS) and sets the decay threshold. The Schmitt triggers control both the analog gain as well as the corresponding (programmable) digital gain correction (DGC).

The difference ("error") signal in the PMF is actually a normalized version of the modulation. This signal is then used as input for the **DELOG** table.

AGC threshold programming

The SFR description for the AGC thresholds are in dBs. The first value to set is the AGC threshold offset in AGCTHOFFS.

This value is the offset relative to 0 input (no noise, no signal), which for the default setting of gain, and assuming typical insertion loss of matching network and ceramic filter, can be extrapolated to be approximately -143dBm.

In this case the default setting of the AGCTHOFFS of 63.9dB corresponds to an input power of approximately -79dBm (= -143dBm + 63.9dB).

The low (digital) AGC threshold is then -79 + 12.8dB (default AGCTLO) = -66dBm and the upper (digital) AGC threshold is -79 + 25.6 (default AGCTUP) = -53dBm.

Therefore a margin of about 6dB is indicated before a degradation of the linearity of the 2^{nd} IF can be observed when using the 50kHz BPF or even about 16dB when using the 300kHz BPF.

The input power level at which the AGC switches back to maximum gain is -66dBm - 21.3dB (default AGCHYS) = -87dBm. This provides enough margin against the minimum sensitivity.

When AGC is activated, RSSI is untrimmed, IFATT <= 5.6dB and the same RSSI offset should be applied for all bandpass filter settings, then the settings in **Table 2** can be applied, where a small reduction of the RSSI input range can be observed.

Table 2 AGC Settings 1

AGC Threshold Hysteresis = 21.3 dB					
AGC Digital RSSI Gain Correction = 15.5 dB					
BPF	**RSSI Offset Compensation (untrimmed) 1)**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**	**RSSI Input Range Reduction**
300 kHz	32	63.9 dB	8	4	5 dB
200 kHz	32	63.9 dB	6	2	5 dB
125 kHz	32	63.9 dB	5	0	5 dB
80 kHz	32	51.1 dB	11	6	2.8 dB
50 kHz	32	51.1 dB	9	5	0 dB

1) Note: This value needs to be used for calculating the register value

For the full RSSI input range, the values in **Table 3** can be applied.

Table 3 AGC Settings 2

AGC Threshold Hysteresis = 21.3 dB				
AGC Digital RSSI Gain Correction = 15.5 dB				
BPF	**RSSI Offset Compensation (untrimmed) 1)**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**
300 kHz	-18	63.9 dB	5	1
200 kHz	-18	51.1 dB	11	7
125 kHz	-18	51.1 dB	10	5
80 kHz	4	51.1 dB	9	5
50 kHz	32	51.1 dB	9	5

1) Note: This value needs to be used for calculating the register value

Attack and Decay coefficients PMF-UP & PMF-DOWN:

The settling time of the loop is determined by means of the integrator gain coefficients PMFUP and PMFDN, which need to be calculated from the wanted attack and decay times.

The ADC is running at a fixed sampling frequency of 274kHz. Therefore the integrator is integrating with PMFUP*274k per second, i.e. time constant is 1/(PMFUP*274k). The attack times are typically 16 times faster than the decay times.

Typical calculation of the coefficients by means of an example:

- PMFUP = 2^-round(ln(AttTime / BitRate * 274kHz) / ln(2))
- PMFDN = 2^-round(ln(DecTime / BitRate * 274kHz) / ln(2)) / PMFUP

where AttTime, DecTime = attack, decay time in number of bits

Note: PMFDN = overall_PMFDN / PMFUP

Example:

BitRate = 2kbps

AttTime = 0.1 bits

=> PMFUP = 2^-round(ln(0.1bit/2kbps*274kHz)/ln(2)) = 2^-round(3.8) = 2^-4

DecTime = 2 bits

=> PMFDN = 2^-round(ln(2bit/2kbps*274kHz)/ln(2))/PMFUP = 2^-round(8.1)/2^-4 = 2^-4

Note: In case of ASK with large modulation index the attack time (PMFUP) can be up to a factor 2 slower due to the fact that the ASK signal has a duty cycle of 50% - during the ASK low duration the integrator is actually slightly discharged due to the decay set by PMFDN.

The AGC start and freeze times are programmable. The same conditions can be used as in the corresponding AFC section above. They will however, be programmed in separate SFR registers.

2.4.6.5 Analog to Digital Converter (ADC)

In front of the AD converter there is a multiplexer so that also temperature and VDDD can be measured (see **Figure 10**).

The default value of the ADC-MUX is RSSI (register ADCINSEL: 000 for RSSI; 001 for Temperature; 010 for VDDD/2).

After switching ADC-MUX to a value other than RSSI in SLEEP Mode, the internal references are activated and this ADC start-up lasts 100µs. So after this ADC start-up time the readout measurements may begin. The chip stays in this mode until reconfiguration of register ADCINSEL to setting RSSI. However, it is recommended to measure temperature during SLEEP mode (This is also valid for VDDD).

Readout of the 10-bit ADC has to be done via ADCRESH register (the lower 2 bits in ADCRESL register can be inconsistent and should not be used).

Typical the ADC refresh rate is 3.7 µs. Time duration between two ADC readouts has to be at least 3.7 µs, so this is already achieved due to the maximum SPI rate (16 bit for SPI command and address last 8µs at an SPI rate of 2MBit/s). The EOC bit (end of conversion) indicates a successful conversion additionally. Repetition of the readout measurement for several times is for averaging purpose.

The input voltage of the ADC is in the range of 1 .. 2 V. Therefore VDDD/2 (= 1.65 V typical) is used to monitor VDDD.

Further details on the measurement and calibration procedure for temperature and VDDD can be taken from the corresponding application note.

2.4.7 RSSI Peak Detector

The IC possesses digital RSSI peak level detectors. The RSSI level is averaged over 4 samples before it is fed to the peak detectors. This prevents the evaluated peak values to be dominated by single noise peaks.

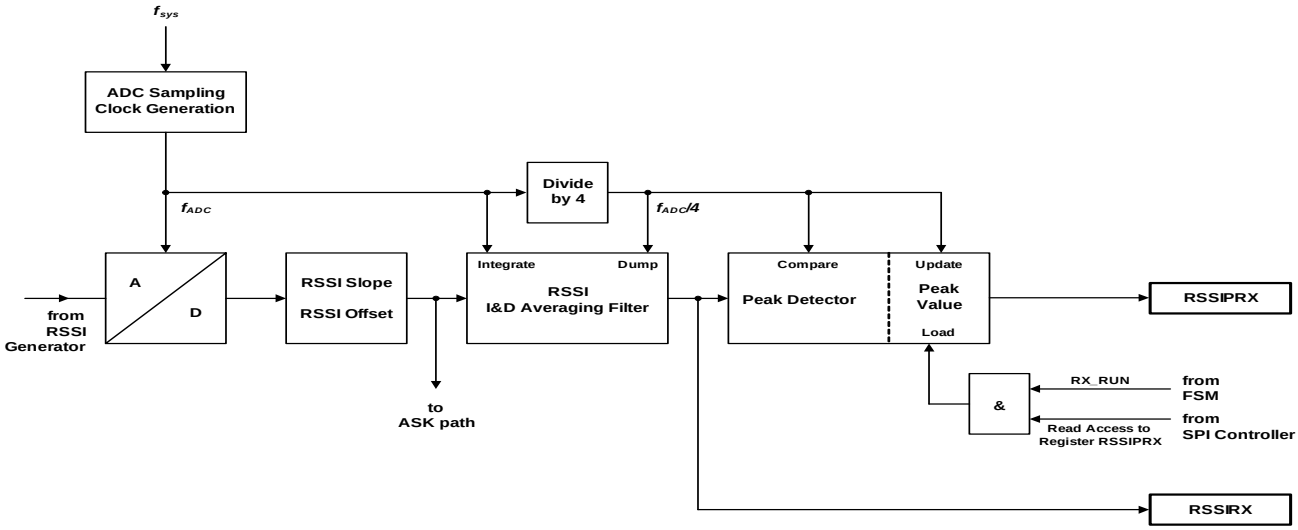


Figure 13 Peak Detector Unit

Peak Detector is used to measure RSSI independent of a data transfer and to digitally trim RSSI. It is read via SFR RSSIPRX.

Observation of the RSSI signal is active whenever the RX_RUN signal is high. The RSSIPRX register is refreshed and the Peak Detector is reset after every read access to RSSIPRX.

It may be required to read RSSIPRX twice to obtain the required result. This is because, for example, during a trim procedure in which the input signal power is reduced, after reading RSSIPRX, the peak detector will still hold the higher RSSI level. After reading RSSIPRX the lower RSSI level is loaded into the Peak Detector and can be read by reading RSSIPRX again.

Register RSSIPRX should not be read-out faster than 41µs in case AGC is ON (as register value would not represent the actual, but a lower value).

When the RX_RUN signal is inactive, a read access has no influence to the peak detector value. The register RSSIPRX is reset to 0 at power up reset.

Peak Detector Wake-Up RSSIPWU (see **Figure 10**) is used to measure the input signal power during Wake-Up search. The internal signal RSSIPWU gets initialized to 0 at start of the first observation time window at the beginning of each configuration/channel. The peak value of this signal is tracked during Wake-Up search.

In case of a Wake-Up, the actual peak value is written in the RSSIPWU register. Even in case no Wake-Up occurred, actual peak value is written in the RSSIPWU register at the end of the actual configuration/channel of the Self Polling period. So if no Wake-Up occurred, then the RSSIPWU register contains the peak value of the last configuration/channel of the Self Polling period, even in a Multi-Configuration/Multi-Channel setup. This functionality can be used to track RSSI during unsuccessful Wake-Up search due to no input signal or due to blocking RSSI detection.

For further details please refer to **Chapter 2.4.8.2 Wake-Up Generator** and **Chapter 2.6.2 Polling Timer Unit**.

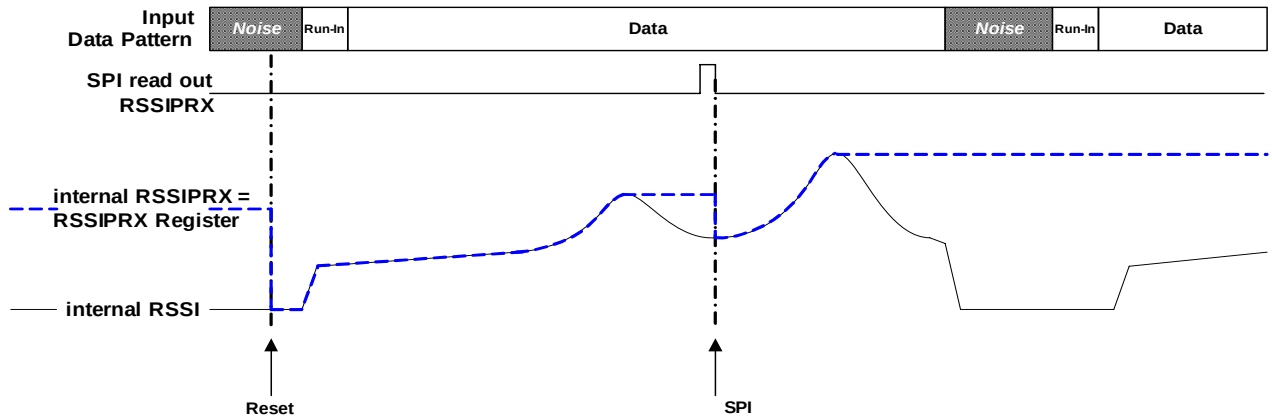


Figure 14 Peak Detector Behavior

Recommended Digital Trimming Procedure

- Download configuration file (Run Mode Slave; RSSISLOPE, RSSIOFFS set to default, i.e. RSSISLOPE=1, RSSIOFFS=0)
- Turn off AGC (AGCSTART=0) and set gain to AGCGAIN=0
- Apply P_{IN1} = -85 dBm RF input signal
- Read RSSIRX eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM1
- Apply P_{IN2} = -65 dBm RF input signal
- Read RSSIRX eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM2
- Calculate measured RSSI slope SLOPEM=(RSSIM2-RSSIM1)/(P_{IN2}-P_{IN1})
- Adjust RSSISLOPE for required RSSI slope SLOPER as follows: RSSISLOPE=SLOPER/SLOPEM
- Adjust RSSIOFFS for required value RSSIR2 at P_{IN2} as follows: RSSIOFFS=(RSSIR2-RSSIM2)+(SLOPEM-SLOPER)*P_{IN2}
- The new values for RSSISLOPE and RSSIOFFS have to be added to the configuration!

Notes:

1. The upper RF input level must stay well below the saturation level of the receiver (see **Chapter 2.4.6.4 Digital Automatic Gain Control Unit (AGC)**)
2. The lower RF input level must stay well above the noise level of the receiver
3. If IF Attenuation is trimmed, this has to be done before trimming of RSSI
4. If RSSI needs to be trimmed in a higher input power range the AGCGAIN must be set accordingly

2.4.8 Digital Baseband (DBB) Receiver

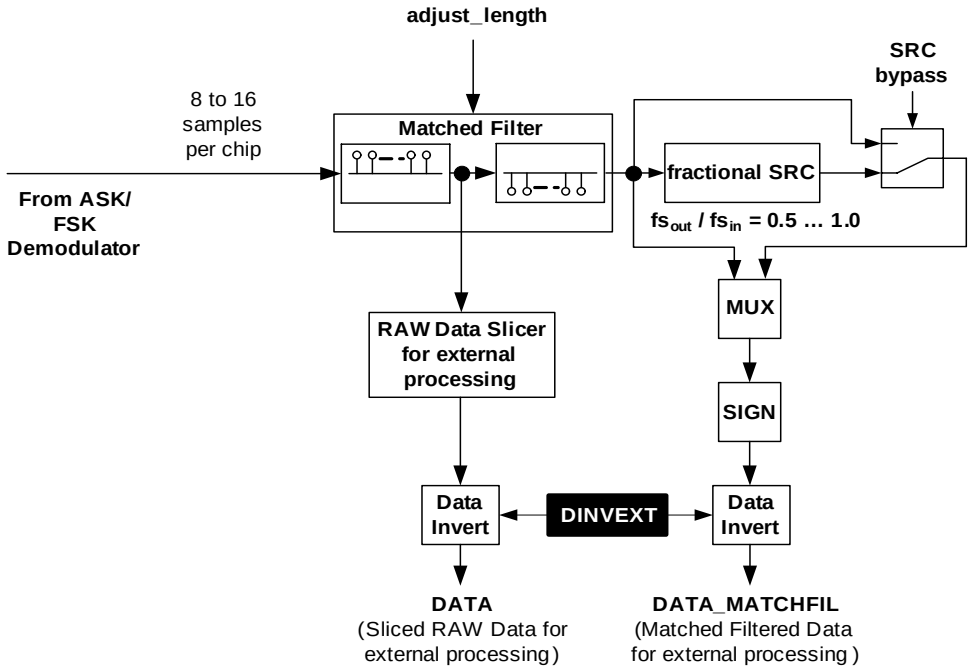


Figure 15 Functional Block Diagram Digital Baseband Receiver

The digital baseband receiver comprises a matched data filter and a data slicer. The received data signal is accessible via one of the port pins.

2.4.8.1 Data Filter

The data filter is a matched filter (*MF*). The frequency response of a matched filter has ideally the same shape as the power spectral density (*PSD*) of the originally transmitted signal, therefore the signal-to-noise ratio (*SNR*) at the output of the matched filter becomes maximum. The input sampling rate of the baseband receiver has to be

between 8 and 16 samples per chip. The oversampling factor within this range is depending on the data rate (see **Figure 10**). The MF has to be adjusted accordingly to this oversampling. After the MF a fractional sample rate converter (SRC) is applied using linear interpolation. Depending on the data rate decimation is adjusted within the range 1...2. Finally, at the output of the fractional SRC the sampling rate is adjusted to 8 samples per chip for further processing.

2.4.8.2 Wake-Up Generator

A wake-up generation unit is used only in the Self Polling Mode for the detection of exceeding a predefined level for RSSI, which then leads to a wake-up and to a change to Run Mode Self Polling.

A configurable observation time for Wake-up on RSSI can be set in the x_WULOT register. The Wake-up on RSSI criterion can be handled very quickly for FSK modulation, while in case of ASK the nature of this modulation type has to be kept in mind.

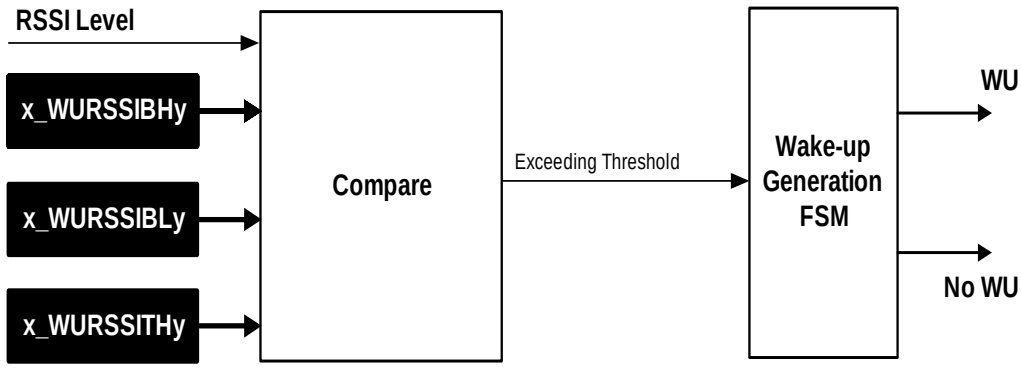


Figure 16 Wake-Up Generation Unit

The threshold x_WURSSITHy is used to decide whether the actual signal is a wanted signal or just noise. Any kind of interfering RSSI level can be blocked by using an RSSI blocking window. This window is determined by the thresholds x_WURSSIBLy and x_WURSSIBHy, where y represents the actual RF channel. These two thresholds can be evaluated during normal operation of the application to handle the actual interferer environment.

The blocking window can be disabled by setting x_WURSSIBHy to the minimum value and x_WURSSIBLy to the maximum value.

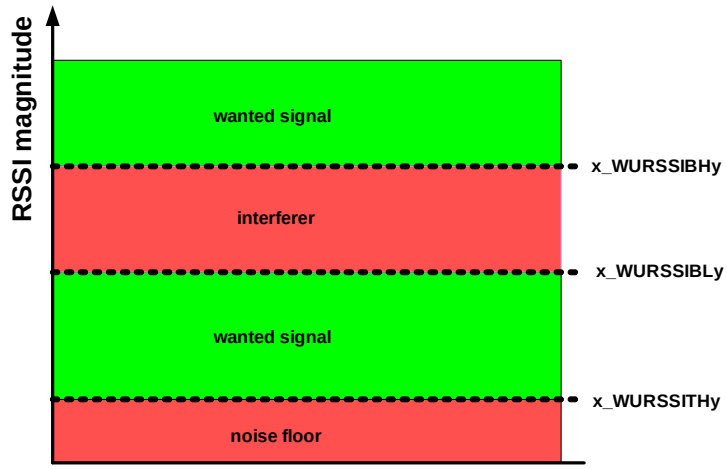


Figure 17 RSSI Blocking Thresholds

Threshold evaluation procedure

A statistical noise floor evaluation using read register RSSIPMF (RMS operation) leads to the threshold x_WURSSITHy. The interferer thresholds x_WURSSIBLy and x_WURSSIBHy are disabled when they are set to their default values.

For evaluation of the interferer thresholds, either use register RSSIPMF for RMS operation or during SPM and WU (Wake-Up) on RSSI use register RSSIPWU to statistically evaluate the interferer band. Finally the thresholds x_WURSSIBLy and x_WURSSIBHy can be set. Further details can be seen in **Figure 10**, **Chapter 2.4.7 RSSI Peak Detector** and **Chapter 2.6.2.2 Constant On-Off Time (COO)**.

NOTE: If e.g. an interferer ends/starts too close after/to the beginning/end of the observation time, then a decision level error can arise. This is due to the filter dynamics (settling time). Further, for interferer thresholds evaluation in SPM this changes interferer statistics. Several interferer measurements are recommended to suppress this, what makes sense anyway for a better distribution.

2.4.9 Power Supply Circuitry

The chip may be operated within a 5 Volts or a 3.3 Volts environment.

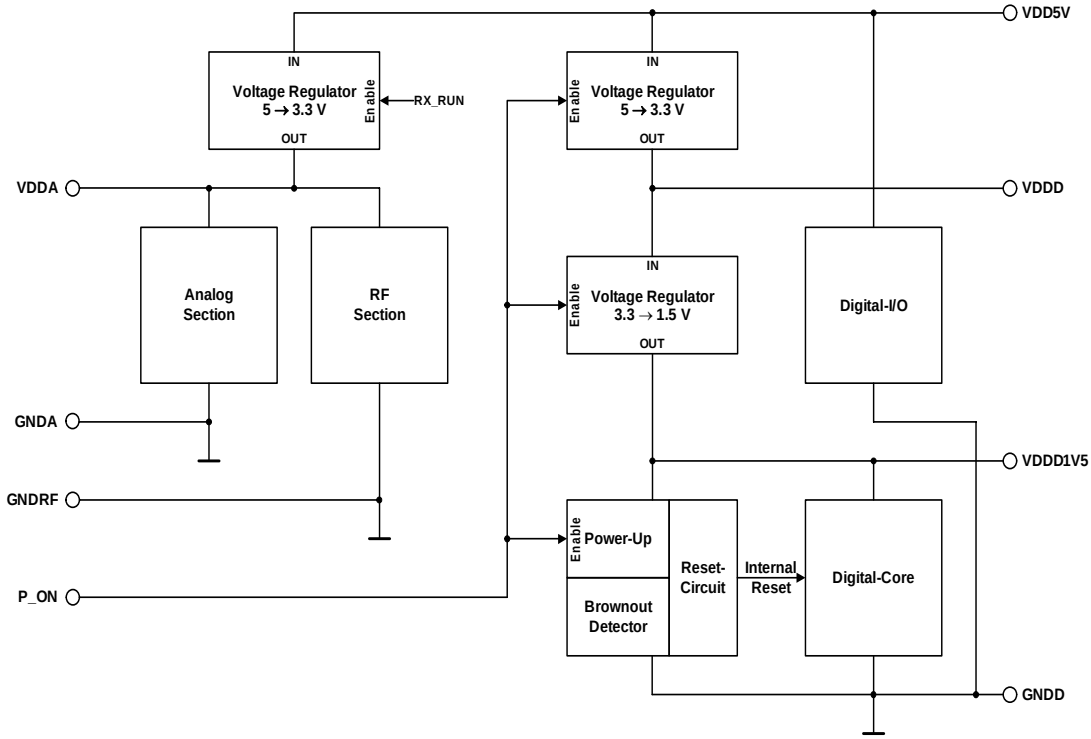


Figure 18 Power Supply

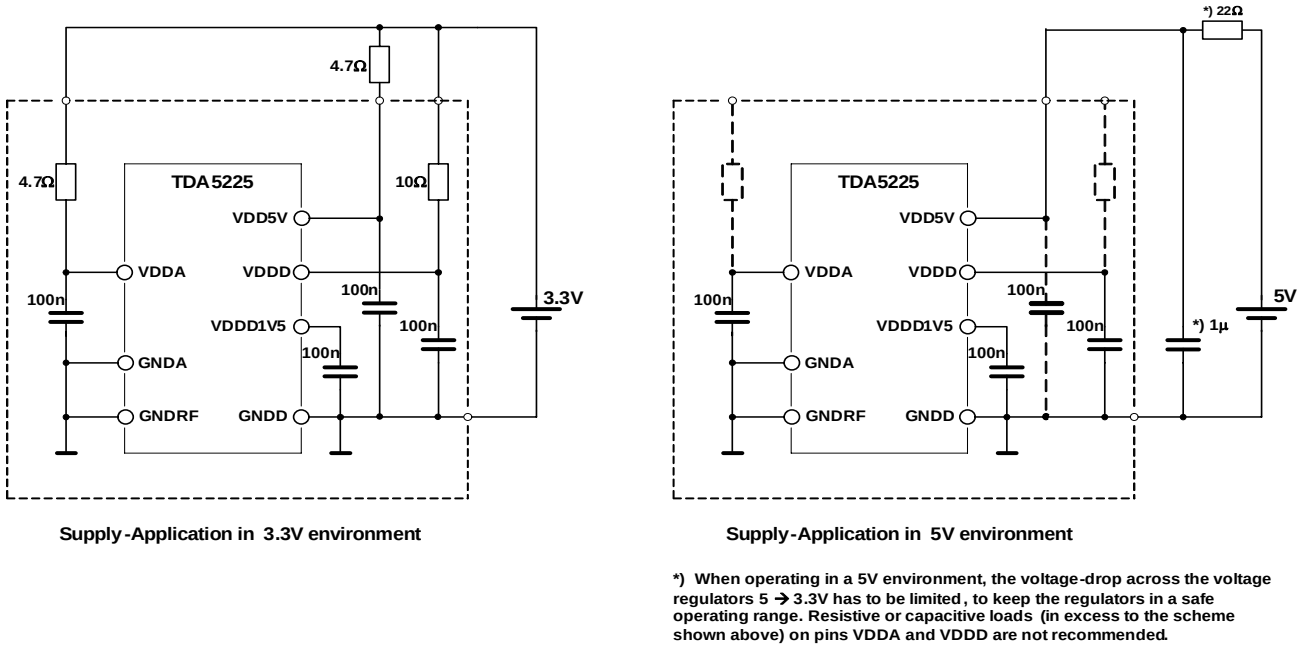
For operation within a 5 Volts environment (supply voltage range 1), the chip is supplied via the VDD5V pin. In this configuration the digital I/O pads are supplied via VDD5V and a 5 V to 3.3 V voltage regulator supplies the analog/RF section (only active in Run Modes).
When operating within a 3.3 Volts environment (supply voltage range 2), the VDD5V, VDDA and VDDD pins must be supplied. The 5 V to 3.3 V voltage regulators are inactive in this configuration.

The internal digital core is supplied by an additional 3.3 V to 1.5 V regulator.

The regulators for the digital section are controlled by the signal at P_ON (Power On) pin. A low signal at P_ON disables all regulators and set the IC in Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF section is active.

To provide data integrity within the digital units, a brownout detector monitors the digital supply. In case a voltage drop of VDDD below approximately 2.45 V is detected a RESET will be initiated.

A typical power supply application for a 3.3 Volts and a 5 Volts environment is shown in the figure below.



Supply-Application in 3.3V environment

Supply-Application in 5V environment

*) When operating in a 5V environment, the voltage-drop across the voltage regulators 5 → 3.3V has to be limited, to keep the regulators in a safe operating range. Resistive or capacitive loads (in excess to the scheme shown above) on pins VDDA and VDDD are not recommended.

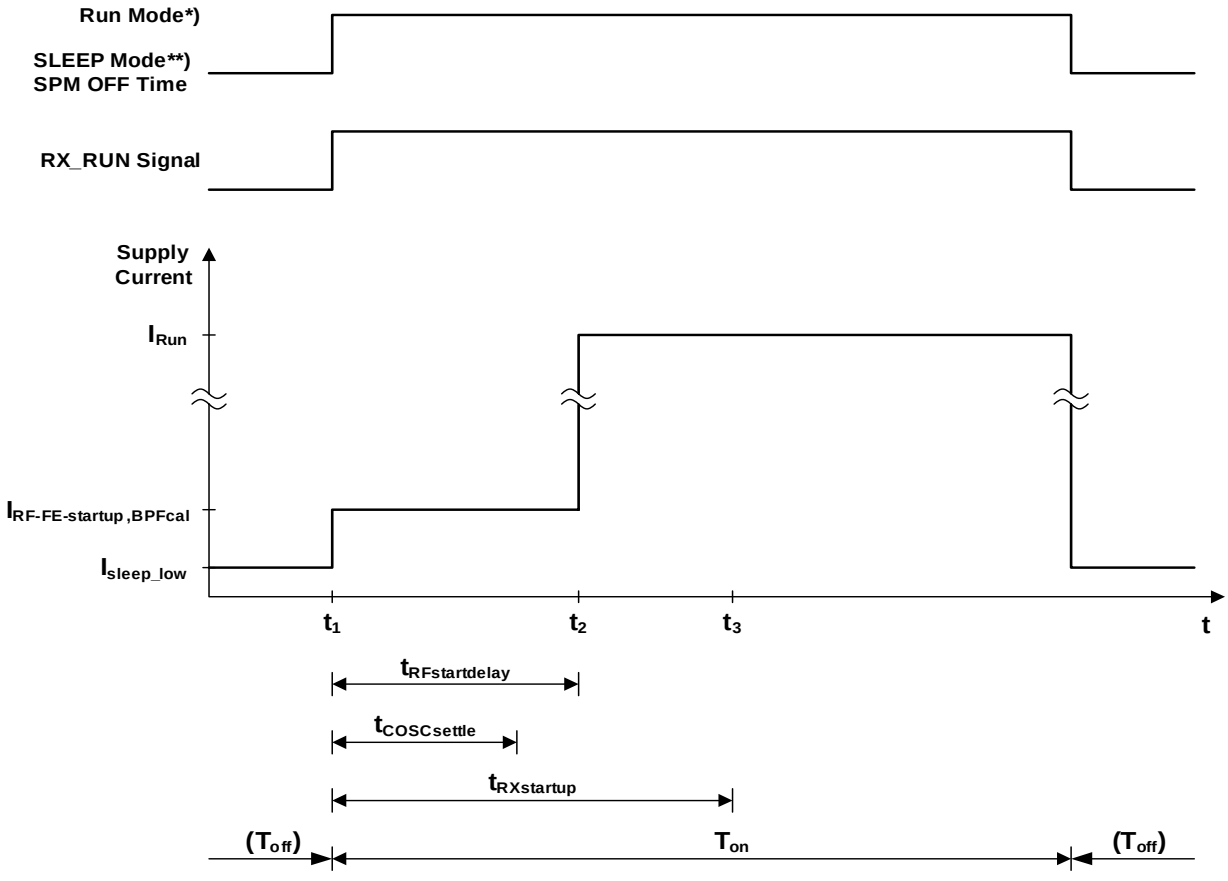
Figure 19 3.3 Volts and 5 Volts Applications

2.4.9.1 Supply Current

In SLEEP Mode, the Master Control Unit switches the crystal oscillator into Low Power Mode (all internal load capacitors are disconnected) to minimize power consumption. This is also valid for Self Polling Mode during Off time (SPM_OFF).

Whenever the chip leaves the SLEEP Mode/SPM_OFF (t_1), the crystal oscillator resumes operation in High Precision Mode and requires $t_{COSCsettle}$ to settle at the trimmed frequency. At t_2 the analog signal path (RF and IF section) and the RF PLL are activated. At t_3 the chip is ready to receive data. The chip requires $t_{RXstartup}$ when leaving SLEEP Mode/SPM_OFF until the receiver is ready to receive data.

A transient supply current peak may occur at t_1, depending on the selected trimming capacitance. The average supply current drawn during $t_{RFstartdelay}$ is $I_{RF\text{-}FE\text{-}startup,BPFcal}$.



*) Run Mode covers the global chip states Run Mode Slave/ Receiver active in Self Polling Mode/ Run Mode Self Polling
**) I_{sleep_low} is valid in the chip states SLEEP / Off time during Self Polling Mode

Figure 20 Supply Current Ramp Up/Down

If the IF buffer amplifier or the clock generation feature (PPx pin active) are enabled, the respective currents must be added.

2.4.9.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A LOW at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high transition at P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

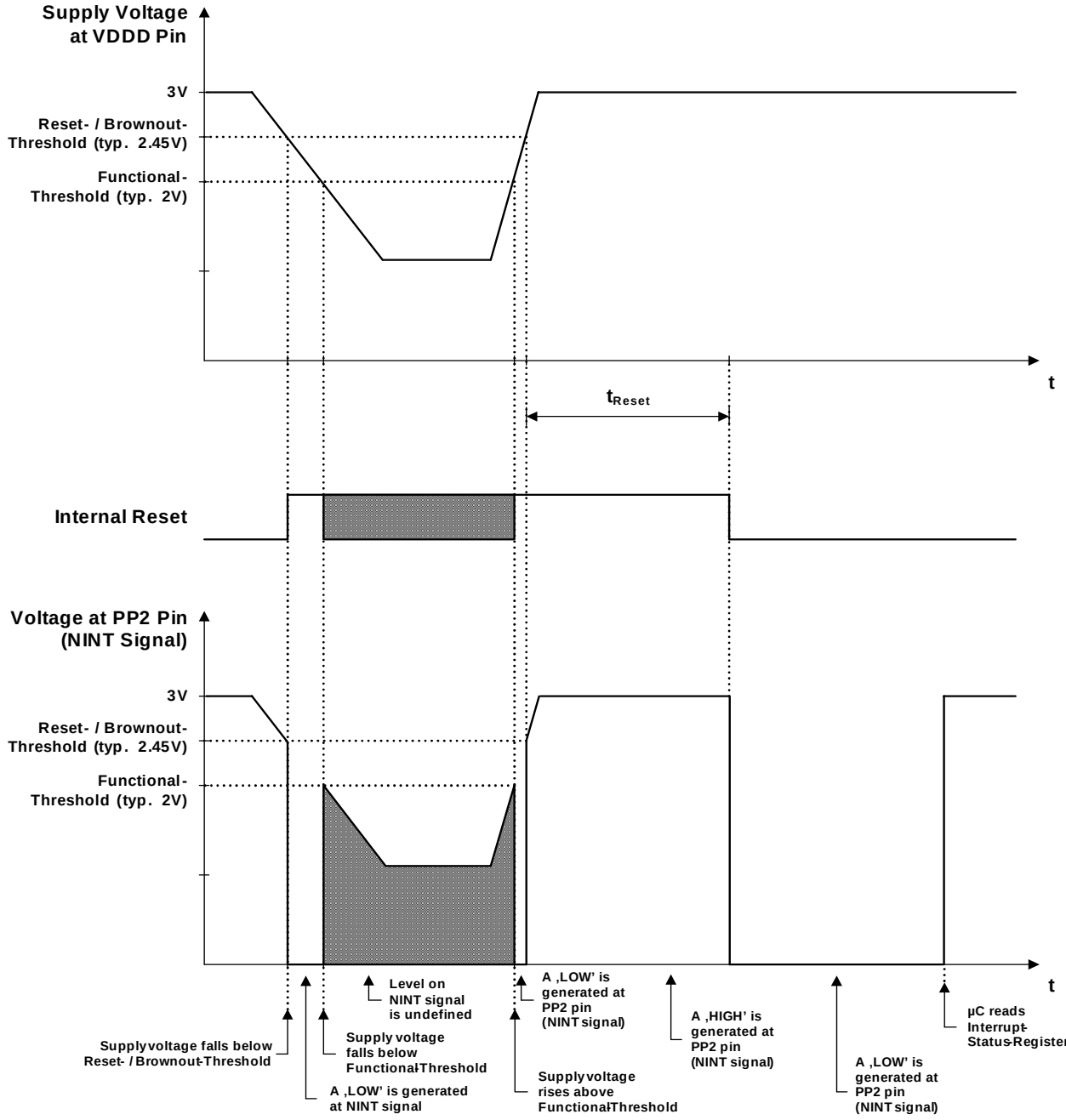


Figure 21 Reset Behavior

A second source that can trigger a reset is a brownout event. Whenever the integrated brownout detector measures a voltage drop below the brownout threshold on the digital

supply, the integrity of the stored data and configuration can no longer be guaranteed; thus a reset is generated. While the supply voltage stays between the brownout and the functional threshold of the chip, the NINT signal is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins are undefined.

When the supply voltage raises above the brownout threshold, the IC generates a high pulse at NINT and remains in the reset state for the duration of the reset time. When the IC leaves the reset state, the Interrupt Status registers (IS0 and IS1) are set to 0xFF and the NINT signal is forced to low. Now, the IC starts operation in the SLEEP Mode, ready to receive commands via the SPI interface. The NINT signal will go high, when one of the Interrupt Status registers is read for the first time.

2.5 System Interface

In all applications, the TDA5225 receiver IC is attached to an external microcontroller. This so-called Application Controller executes a firmware which governs the TDA5225 by reading data from the receiver when data has been received on the RF channel and by configuring the receiver device. The TDA5225 features an easy to use System Interface, which is described in this chapter.

The TDA5225 supports the so-called Transparent Mode, which provides a rather rudimentary interface by which the incoming RF signal is demodulated and the corresponding data is made available to the Application Controller. The usage of the Transparent Mode will be described in **Chapter 2.5.1.2**.

2.5.1 Interfacing to the TDA5225

The TDA5225 is interfacing with an application by three logical interfaces, see **Figure 22**. The RF/IF interface handles the reception of RF signals and is responsible for the demodulation. Its physical implementation has been described in **Chapter 2.4.3** and **Chapter 2.4.8**, respectively. The other two logical interfaces establish the connection to the Application Controller.

For the sake of clarity, the communication between the TDA5225 and the Application Controller is split into **control flow** and **data flow**. This separation leads to an independent definition of the data interface and the control interface, respectively.

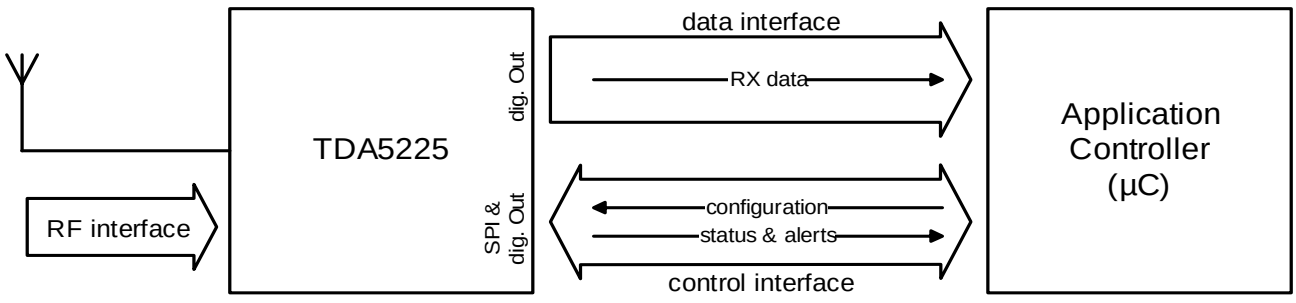


Figure 22 Logical and electrical System Interfaces of the TDA5225

2.5.1.1 Control Interface

The control interface is used in order to configure the TDA5225 after start-up or to re-configure it during run-time, as well as to properly react on changes in the status of the receiver in the Application Controller's firmware. The control interface offers a bi-directional communication link by which

- **configuration data** is sent from the Application Controller to the TDA5225,
- the receiver provides **status information** (e.g. information about the source of a received data stream, by reading out the interrupt status registers) as response to a request it has received from the Application Controller, and
- the TDA5225 autonomously **alerts** the Application Controller that a certain, configurable event has occurred (e.g. that a received signal is above a certain power level).

Configuration and status information are sent via the 4-wire SPI interface as described in **Chapter 2.5.4**. The configuration data determines the behavior of the receiver, which comprises

- scheduling the inactive power-saving phases as well as the active receive phases,
- selecting the properties of the RF/IF interface configuration (e.g. carrier frequency selection, filter settings),
- configuring the properties of a received message (e.g. if the received signal strength is above a certain configurable RSSI threshold level).

Note that the TDA5225 receiver IC supports reception of multiple configuration sets on multiple channels in a time-based manner without reconfiguration. Thus, the RF/IF interface as well as the message properties support alternative settings, which can be activated autonomously by the receiver as part of the scheduling process.

In contrast to the high-level interface used for communicating configuration instructions and status information, alerts are emitted by the receiver on a digital output pin that may trigger external interrupts in the Application Controller. Note that the alerting conditions as well as the polarity of the output pin are configurable, see **Chapter 2.5.3**.

2.5.1.2 Data Interface

The data interface between the Application Controller and the TDA5225 receiver IC is used for the transport of the received data, see **Figure 22**. The features of the data interface depend on the selected mode of operation.

There are two possible receive modes:

- Transparent Mode - Matched Filter (TMMF)
- Transparent Mode - Raw Data Slicer (TMRDS)

Access points for these receive modes can be seen in **Figure 15**.

Transparent Mode - Matched Filter (TMMF)

The received data after the Matched Filter (Two-Chip Matched Filter) with an additional SIGN function is provided via the DATA_MATCHFIL signal (PPx pin). In this mode sensitivity measurements with ideal data clock can be performed very simple. For further details see the block diagram in **Figure 15**.

Sensitivity in this transparent mode is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

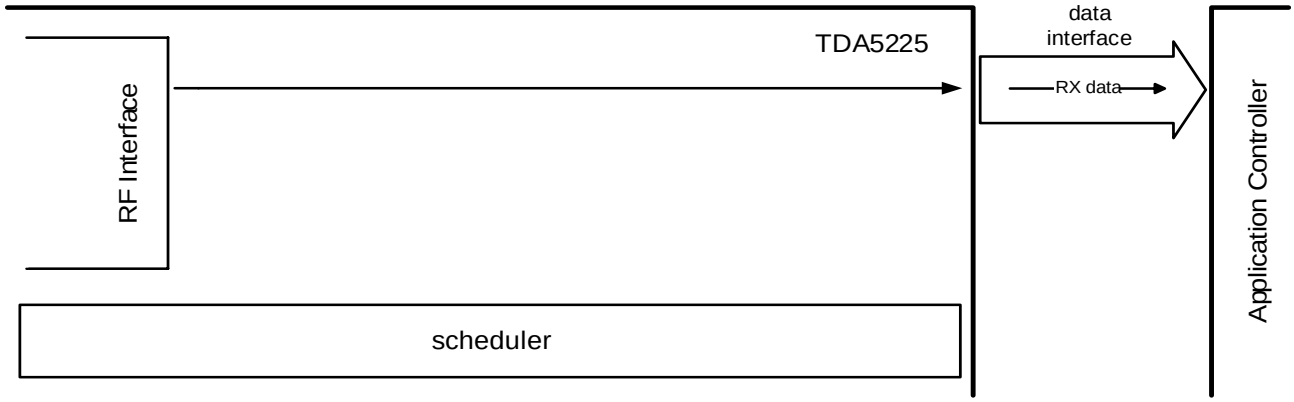


Figure 23 Data interface for the Transparent Mode

Transparent Mode - Raw Data Slicer (TMRDS)

This mode supports processing of data even without bi-phase encoding (e.g. NRZ encoding) by providing the received data via the One-Chip Matched Filter on the DATA signal (PPx pin). See more details in the block diagram in **Figure 15**.

Sensitivity in this transparent mode is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

The data interface can be seen from **Figure 23**.

Self Polling capabilities are possible as well, so Constant On-Off Mode and Wake-up on RSSI can be used. See also example for Configuration B in **Figure 24**. The needed On time (latency through TDA5225) is configured in the corresponding On time registers of the chip. The interrupt for Wake-Up Config B (WUB) is enabled and suitable RSSI thresholds are set.

If the RSSI signal is in a valid threshold area, the TDA5225 changes to Run Mode Self Polling and an interrupt can be signaled to the Application Controller.

In case the RSSI signal is outside the valid threshold area, the chip stays in Self Polling Mode and the external controller gets no interrupt (as the desired RSSI level is not reached).

When the actual processed configuration is the last configuration before the Off time, then the next programmed channel within the polling cycle would be the sequence of the Off time.

When data is available and the RSSI is within a valid threshold area, an interrupt is generated (NINT). So the Application Controller can process the data and decide about valid data.

In case the controller decides that wrong data was sent, the microcontroller can send the register command "EXTTOTIM" (see **Figure 43** and EXTPCMD register).

When the microcontroller detects valid data, then the controller can send the register command "EXTEOM found" (see **Figure 43** and EXTPCMD register) after completing the data reception.

The functionality described above can also be used for the receive mode TMMF, where the external microcontroller takes on responsibility for further data processing.

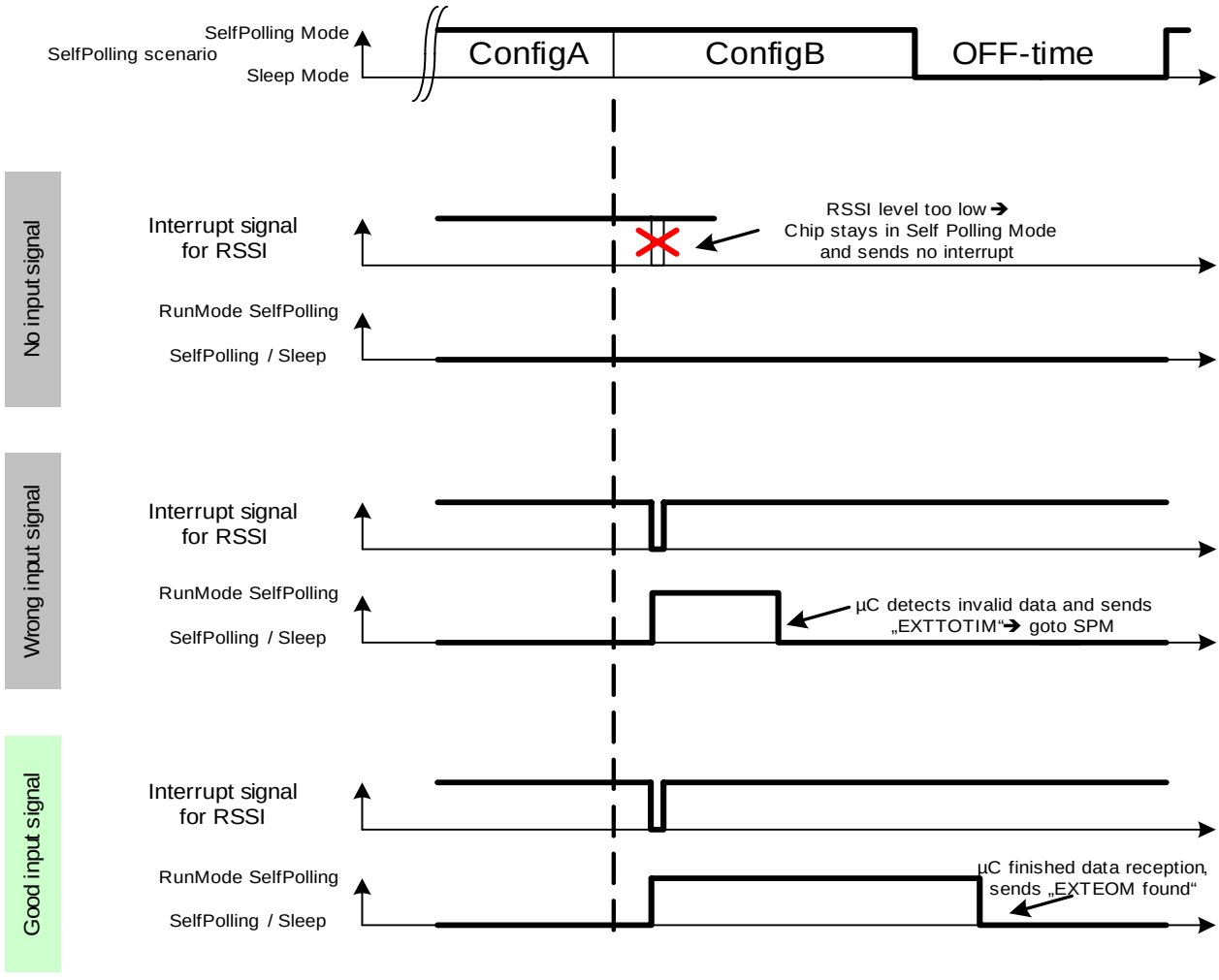


Figure 24 External Data Processing

2.5.2 Digital Output Pins

As long as the P_ON pin is high, all digital output pins operate as described. If the P_ON pin is low, all digital output pins are switched to high impedance mode.

The digital outputs PP0, PP1, PP2 and PP3 are configurable, where each of the signals CLK_OUT, RX_RUN, NINT, a LOW level (GND) and a HIGH level, DATA and DATA_MATCHFIL can be routed to any of the four output pins. There is only one exception, CLK_OUT is not available on PP3. The default configuration for these four output pins can be seen in **Table 1**.

Each port pin can be inverted by usage of PPCFG2 register.

The RX_RUN signal is active high for all Configurations by default. It can be deactivated for every Configuration separately. Every PPx can be configured with an individual RX_RUN setup. This can be set in RXRUNCFG0 and RXRUNCFG1 registers.

Interfacing to 3.3V Logic:

The TDA5225 is able to interface directly to a 3.3V logic, when chip is operated in 3.3V environment.

Interfacing to 5V Logic:

The TDA5225 is able to interface directly to a 5V logic, when chip is operated in 5V environment.

EMC Reduction of Digital I/Os:

Because electromagnetic distortion generated by digital I/Os may interfere with the high sensitivity radio receiver, it is recommended that all inputs are filtered by adding an RC low pass circuit.

2.5.3 Interrupt Generation Unit

The TDA5225 is able to signal interrupts (NINT signal) to the external Application Controller on one of the PPx port pins (for further details see **Chapter 2.5.2 Digital Output Pins**). The Interrupt Generation Unit receives all possible interrupts and sets the NINT signal based on the configuration of the Interrupt Mask registers (IM0 and IM1). The Interrupt Status registers (IS0 and IS1) are set from the Interrupt Generation Unit, depending on which interrupt occurred. The polarity of the interrupt can be changed in the PPCFG2 register. Please note that during power up and brownout reset, the polarity of NINT signal is always as described in **Chapter 2.4.9.2 Chip Reset**.

A Reset event has the highest priority. It sets all bits in the Status registers to “1” and sets the interrupt signal to “0”. The first interrupt after the Reset event will clear the Status registers and will set the interrupt signal to “1”, even if this interrupt is masked.

An WU interrupt clears the complementary flags for WU.

The Interrupt Status register is always cleared after read out via SPI.

It is not possible to disable the Power On Reset Indicator Interrupt using the Interrupt Mask registers.

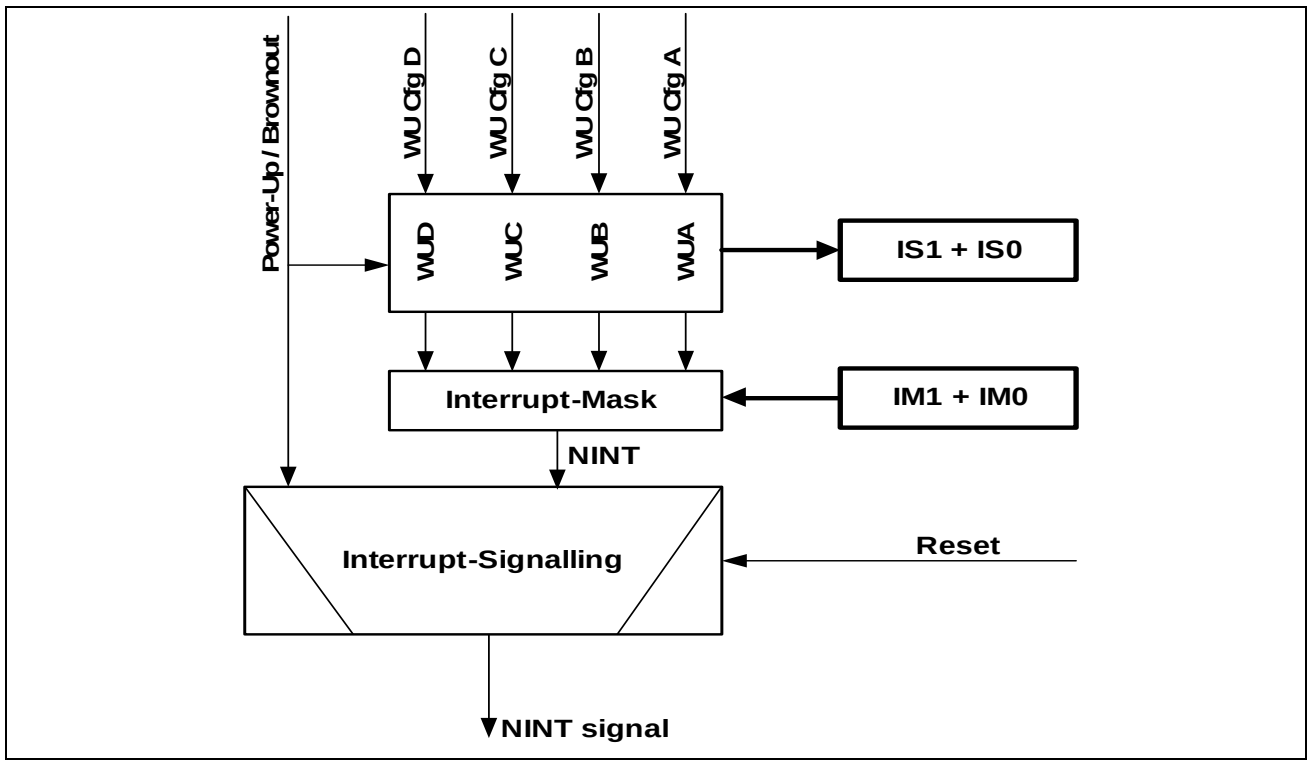


Figure 25 Interrupt Generation Unit

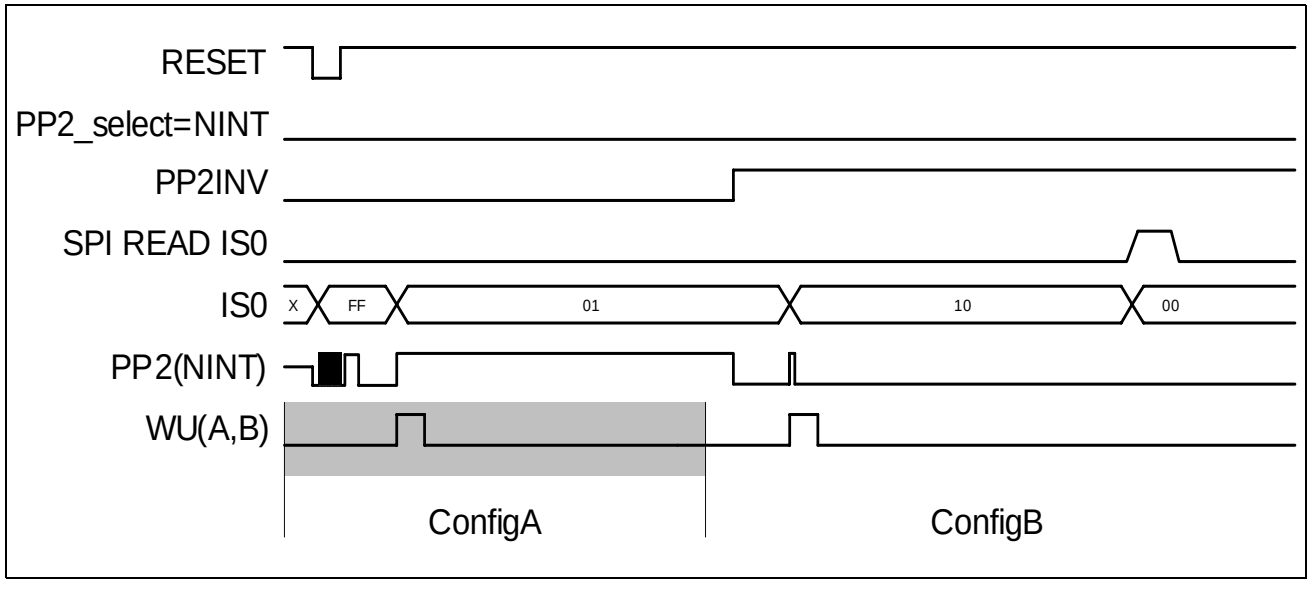


Figure 26 Interrupt Generation Waveform (Example for Configuration A+B)

The following handling mechanism for read-clear registers was chosen due to implementation of the Burst Read command:

- the current Interrupt Status (ISx) register 8-bit content is **latched** into the SPI shift register after the last address bit is clocked-in (**point A** in **Figure 27**)
- the IS register is then **cleared** after last IS register bit is clocked out of the SPI interface (**point B** in **Figure 27**)

Consequence: any interrupt event occurring in the window-time between points A and B is cleared at point B and not stored/shown in an later readout of ISx.

(However: NINT signal is toggling in any case, if occurring interrupt is not masked in IMx register)

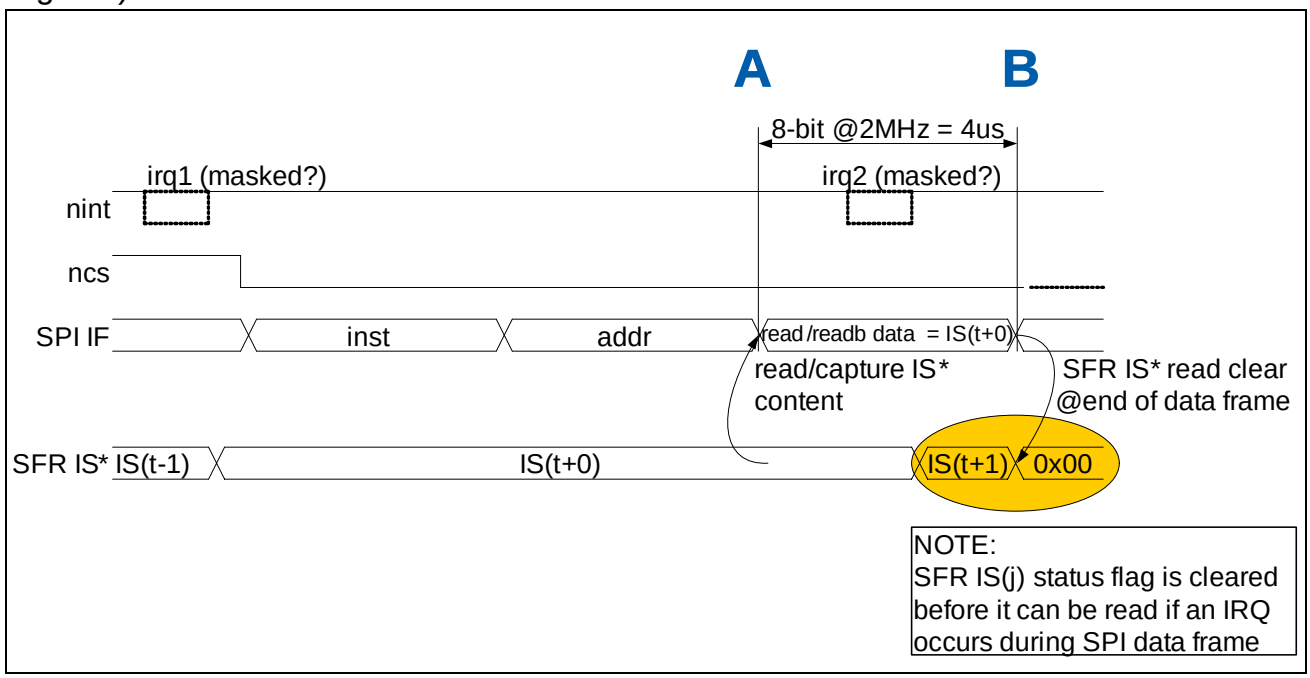


Figure 27 ISx Readout Set Clear Collision

Please see also the **IMPORTANT NOTE** in the Burst Read section !

2.5.4 Digital Control (4-wire SPI Bus)

The control interface used for device control is a 4-wire SPI interface.

- *NCS* - select input, active low
- *SDI* - data input
- *SDO* - data output
- SCK - clock input: Data bits on *SDI* are read in at rising *SCK* edges and written out on *SDO* at falling *SCK* edges.

Level definition:
logic 0 = low voltage level
logic 1 = high voltage level

Note for non-Burst modes: It is possible to send multiple frames while the device is selected. It is also possible to change the access mode while the device is selected by sending a different instruction.

Note: In all bus transfers MSB is sent first.

To **read from the device**, the SPI master has to select the SPI slave unit first. Therefore, the master must set the *NCS* line to low. After this, the instruction byte and the address byte are shifted in on *SDI* and stored in the internal instruction and address register. The data byte at this address is then shifted out on *SDO*. After completing the read operation, the master sets the *NCS* line to high.

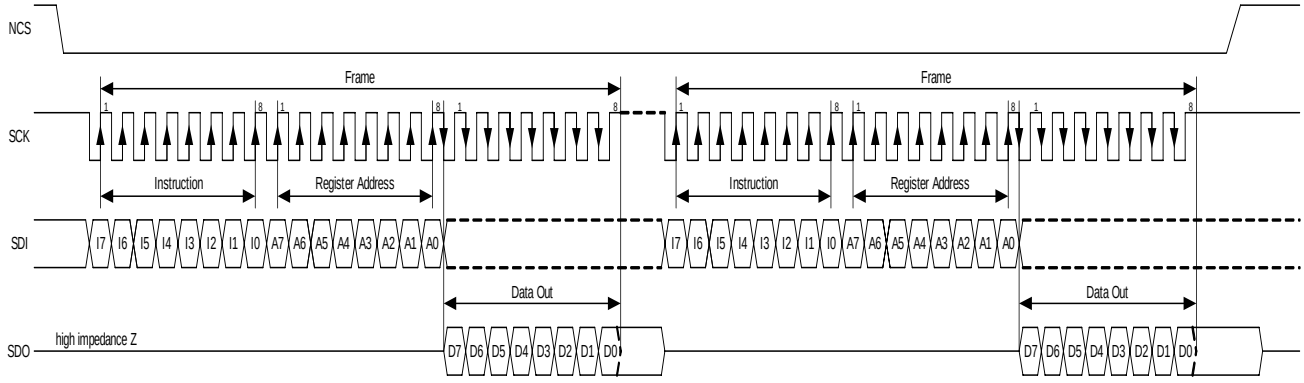


Figure 28 Read Register

To **read from the device in Burst mode**, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first), the slave unit will respond by transferring the register contents beginning from the given start address (MSB first). Driving the NCS line to high will end the Burst frame.

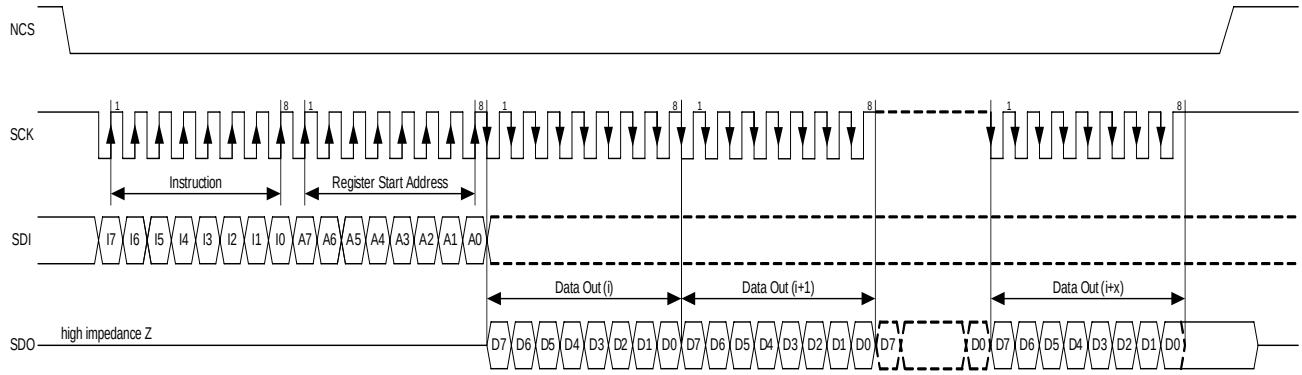


Figure 29 Burst Read Registers

IMPORTANT NOTE - for being upwards compatible with further versions of the product, we give following strong recommendation:

For read-clear registers at address (N), no read-burst access stopping at address (N-1) is allowed, because read-clear register will be cleared without being read out. Use single read command to read out the register at address (N-1) or extend the burst read to include the read-clear register at address (N).

To **write to the device,** the SPI master has to select the SPI slave unit first. Therefore, the master must set the *NCS* line to low. After this, the instruction byte and the address byte are shifted in on *SDI* and stored in the internal instruction and address register. The following data byte is then stored at this address.
After completing the writing operation, the master sets the *NCS* line to high.

Additionally the received address byte is stored into the register *SPIAT* and the received data byte is stored into the register *SPIDT*. These two **trace registers** are readable.

Therefore, an external controller is able to check the correct address and data transmission by reading out these two registers after each write instruction. The trace

registers are updated at every write instruction, so only the last transmission can be checked by a read out of these two registers.

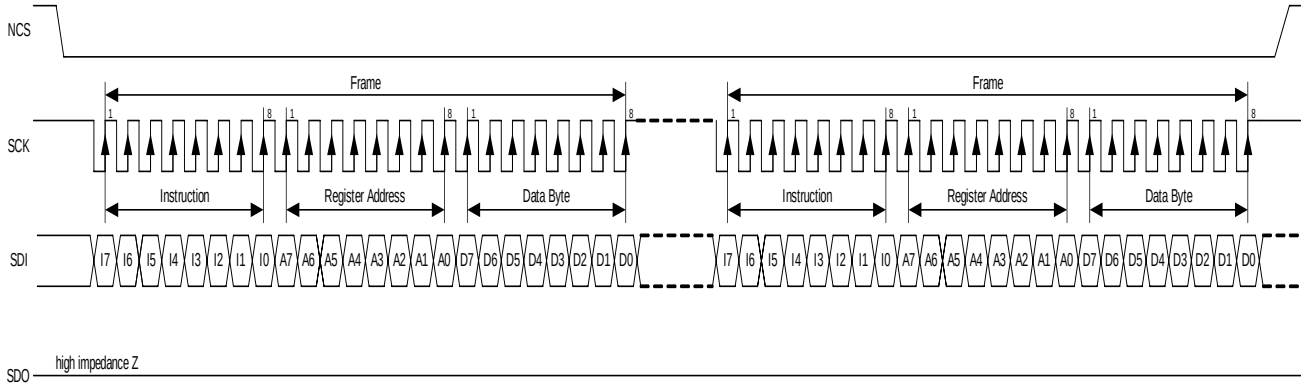


Figure 30 Write Register

To **write to the device in Burst mode**, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first) the successive data bytes will be stored into the automatically addressed registers.

To verify the SPI Burst Write transfer, the current address (start address, start address + 1, etc.) is stored in register SPIAT and the current data field of the frame is stored in register SPIDT. At the end of the Burst Write frame the latest address as well as the latest data field can be read out to verify the transfer. Note that some error in one of the intermediate data bytes can not be detected by reading SPIDT.

Driving the NCS line to high will end the Burst frame.

A single SPI Burst Write command can be applied very efficiently for data transfer either within a register block of configuration dependent registers or within the block of configuration independent registers.

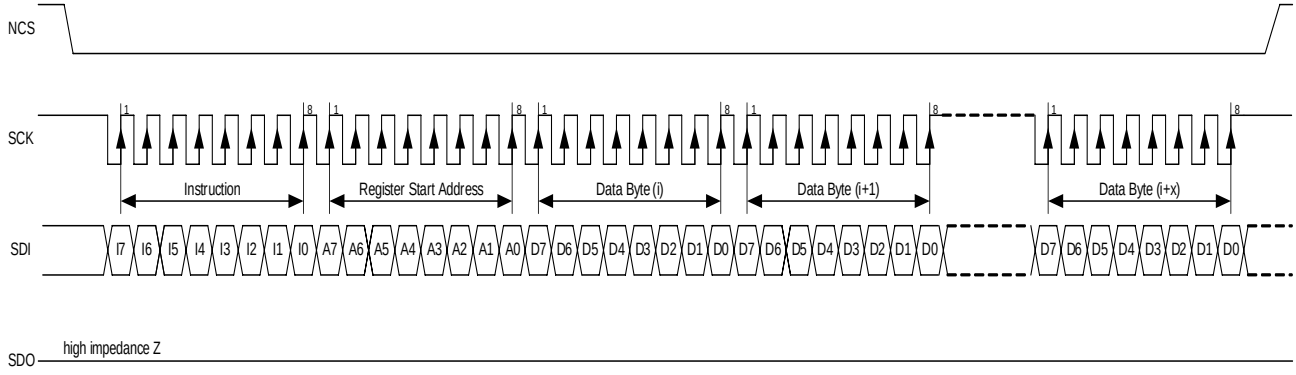


Figure 31 Burst Write Registers

The SPI also includes a safety feature by which the **checksum is calculated** with an XOR operation from the address and the data when writing SFR registers. The checksum is in fact an XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is automatically written in the SPICHKSUM register and can be compared with the expected value. After the SPICHKSUM register is read, its value is cleared.

In case of an SPI Burst Write frame, a checksum is calculated from the SPI start address and consecutive data fields.

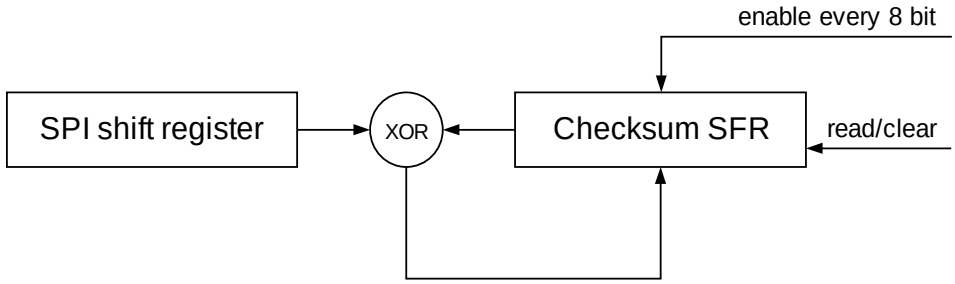


Figure 32 SPI Checksum Generation

Table 4 Instruction Set

Instruction	Description	Instruction Format
WR	Write to chip	0000 0010
RD	Read from chip	0000 0011
WRB	Write to chip in Burst mode	0000 0001
RDB	Read from chip in Burst mode	0000 0101

2.5.4.1 Timing Diagrams

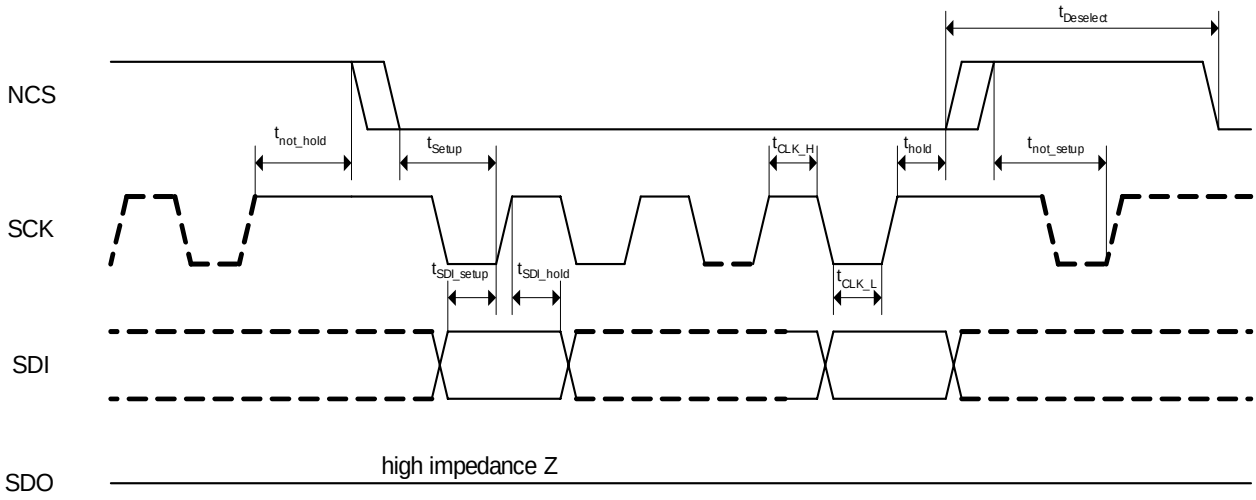


Figure 33 Serial Input Timing

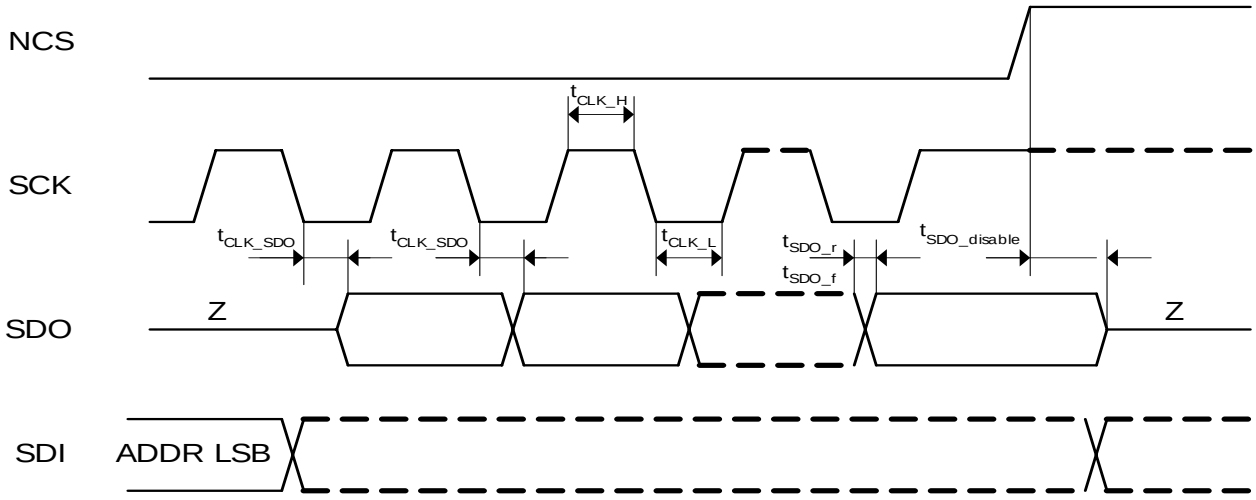


Figure 34 Serial Output Timing

Table 5 SPI Bus Timing Parameter

Symbol	Parameter
f_{clock}	Clock frequency
t_{CLK_H}	Clock High time
t_{CLK_L}	Clock Low time
t_{setup}	Active setup time
t_{not_setup}	Not active setup time
t_{hold}	Active hold time
t_{not_hold}	Not active hold time
$t_{Deselect}$	Deselect time
t_{SDI_setup}	SDI setup time
t_{SDI_hold}	SDI hold time
t_{CLK_SDO}	Clock low to SDO valid
t_{SDO_r}	SDO rise time
t_{SDO_f}	SDO fall time
$t_{SDO\_disable}$	SDO disable time

2.5.5 Chip Serial Number

Every device contains a unique, preprogrammed 32-bit wide serial number. This number can be read out from SN3, SN2, SN1 and SN0 registers via the SPI interface. The TDA5225 always has SN0.6 set to 0 and SN0.5 set to 1.

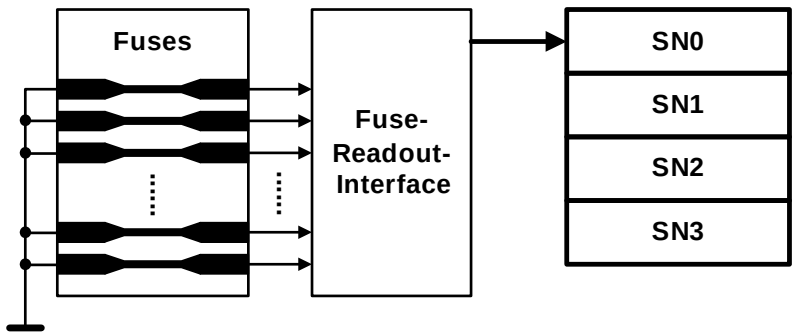


Figure 35 Chip Serial Number

2.6 System Management Unit (SMU)

The System Management Unit consists of two main units:

- **Master Control Unit**, where the various operating modes can be configured.
- **Polling Timer Unit**, where the receiver's On and Off times and modes are defined. The Polling Timer Unit is only working in the Self Polling Mode.

2.6.1 Master Control Unit (MCU)

2.6.1.1 Overview

The Master Control Unit controls the operation modes and the global states.

The transparent data stream can be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

The following operation modes and the behavior of the Master Control Unit are fully automatic and only influenced by SFR settings and by incoming RF data streams.

The TDA5225 has two major operation modes, which are switched by SFR bit MSEL.

In **Slave Mode** the device is controlled via SPI by the external microcontroller. This mode supports:

- **Run Mode Slave (RMS)**, where the receiver is continuously active
- **SLEEP Mode**, where the receiver is switched off for power saving. This mode can also be used to change register settings
- **HOLD Mode**, allows register settings to be changed. The change to HOLD Mode and back to RMS is faster than changing to SLEEP Mode and back to RMS.

In Slave Mode, switching between configurations and channels, as well as between Run and SLEEP Mode must be initiated by the microcontroller.

In **Self Polling Mode,** TDA5225 autonomously polls for incoming RF signals. The receiver switches automatically between up to four configurations (Configuration A, B, C and D) and up to 3 channels per configuration (Further information can be found in **Chapter 2.6.2**).

Between the RF signal scans, the receiver is automatically switched to Low Power Mode for reducing the average power consumption. If an incoming signal fulfills the selected wake-up criterion an interrupt can be generated and Run Mode Self Polling will be entered.

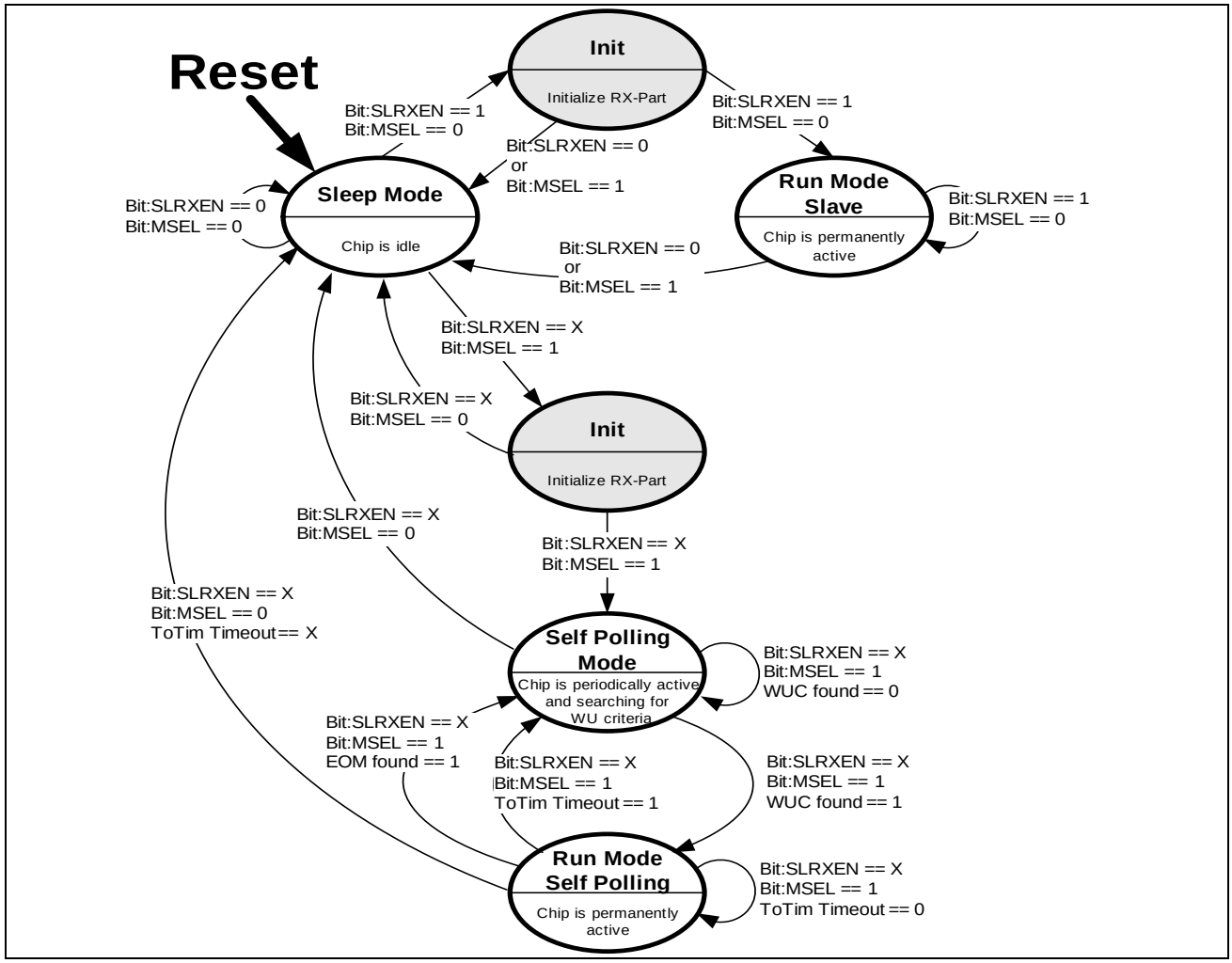


Figure 36 Global State Diagram

2.6.1.2 Run Mode Slave (RMS)

In Run Mode Slave, the receiver is able to continuously scan for incoming data streams. Detection and validation of a wake-up criterion are not performed.

The transparent data stream can be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

Run Mode Slave is entered by setting SFR CMC0 bits MSEL to 0 and SLRXEN to 1.

Configurations are switched via SFR bit group MCS in the CMC0 register. The RF channel in use can be selected in the x_CHCFG register, the frequency selection is defined by SFRs x_PLLINTCy, x_PLLFRAC0Cy, x_PLLFRAC1Cy, x_PLLFRAC2Cy, where x = A, B, C or D and y = 1, 2 or 3.

The configuration may be changed only in SLEEP or in HOLD Mode before returning to the previously selected operation mode. This is necessary to restart the state machine

with defined settings at a defined state. Otherwise the state machine may hang up. Reconfigurations in HOLD Mode are faster, because there is no Start-Up sequence.

The following flowchart and explanation show and help to understand the internal behavior of the Finite State Machine (FSM) in Run Mode Slave.

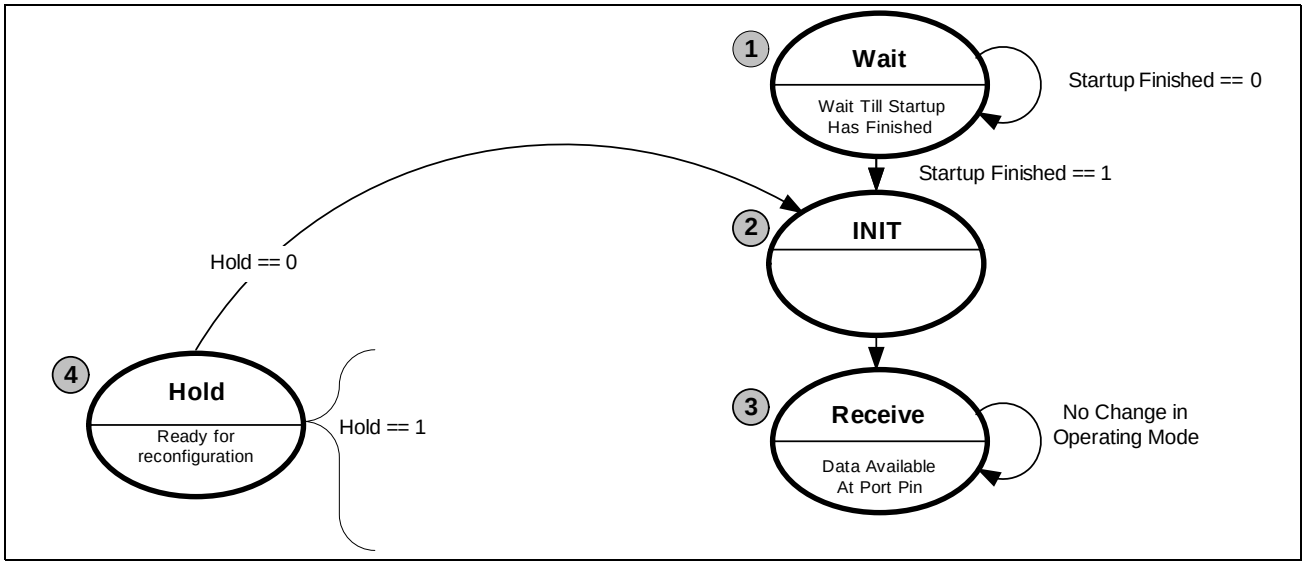


Figure 37 Run Mode Slave

2.6.1.3 HOLD Mode

This state (item 4 in **Figure 37**) is used for fast reconfiguration of the chip in Run Mode Slave. HOLD state can be reached after the Start-Up Sequencer and Initialization of the chip have been completed and the chip is working in state 3. To reconfigure the chip the SFR control bit HOLD must be set. After reconfiguration in this state the SFR control bit HOLD must be cleared again. After leaving the HOLD state, the INIT state is entered and the receiver can work with the new settings. Be aware that the time between changing the configuration and reinitialization of the chip has to be at least 40us. Take note that one SPI command for clearing the SFR control bit HOLD needs 24 bits or 12µs at an SPI data rate of 2.0Mbit/s. The remaining 28µs must be guaranteed by the application.

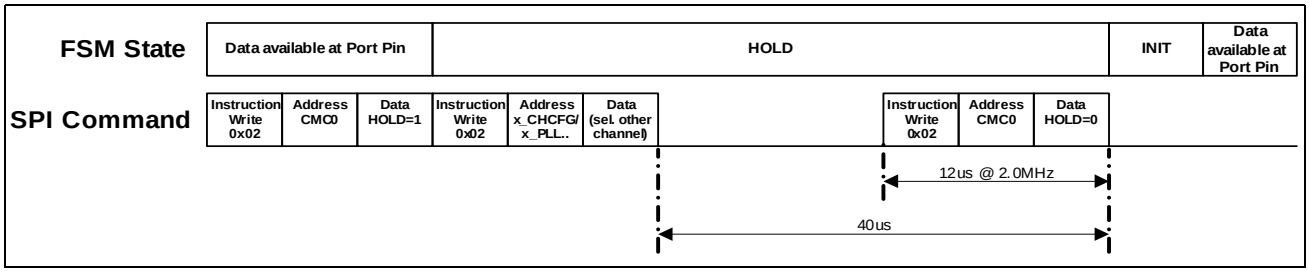


Figure 38 HOLD State Behavior (INITPLLHOLD disabled)

In case of large frequency steps, an additional VAC routine (VCO Automatic Calibration) has to be activated when recovering from HOLD Mode (INITPLLHOLD bit). The maximum allowed frequency step in HOLD Mode without activation of VAC routine is depending on the selected frequency band. The limits are +/- 1 MHz for the 315 MHz band, +/- 1.5 MHz for the 434 MHz band and +/- 3 MHz for the 868/915 MHz band.

When this additional VAC routine is enabled, the TDA5225 starts initialization of the Digital Receiver block after release from HOLD and an additional Channel Hop time.

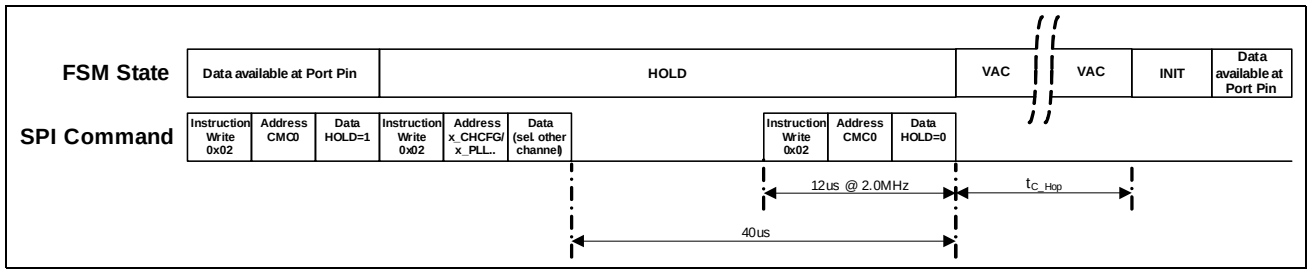


Figure 39 HOLD State Behavior (INITPLLHOLD enabled)

HOLD Mode is only available in Run Mode Slave. Configuration changes in Self Polling Mode have to be done by switching to SLEEP Mode and returning to Self Polling Mode after reconfiguration.

2.6.1.4 SLEEP Mode

The SLEEP Mode is a power save mode. The complete RF part is switched off and the oscillator is in Low Power Mode. As in HOLD Mode, the chip can be reconfigured. When switching from SLEEP to Run Mode Slave, the state machine starts with the internal Start-Up Sequence.

2.6.1.5 Self Polling Mode (SPM)

In Self Polling Mode TDA5225 autonomously polls for incoming RF wake-up data streams. At that time there is no processing load on the host microcontroller. When a wake-up criterion has been found, an interrupt can be generated and the TDA5225 mode will be changed to Run Mode Self Polling.

A general overview on a typically transmitted protocol and the behaviour of the TDA5225 is given in **Figure 40**.

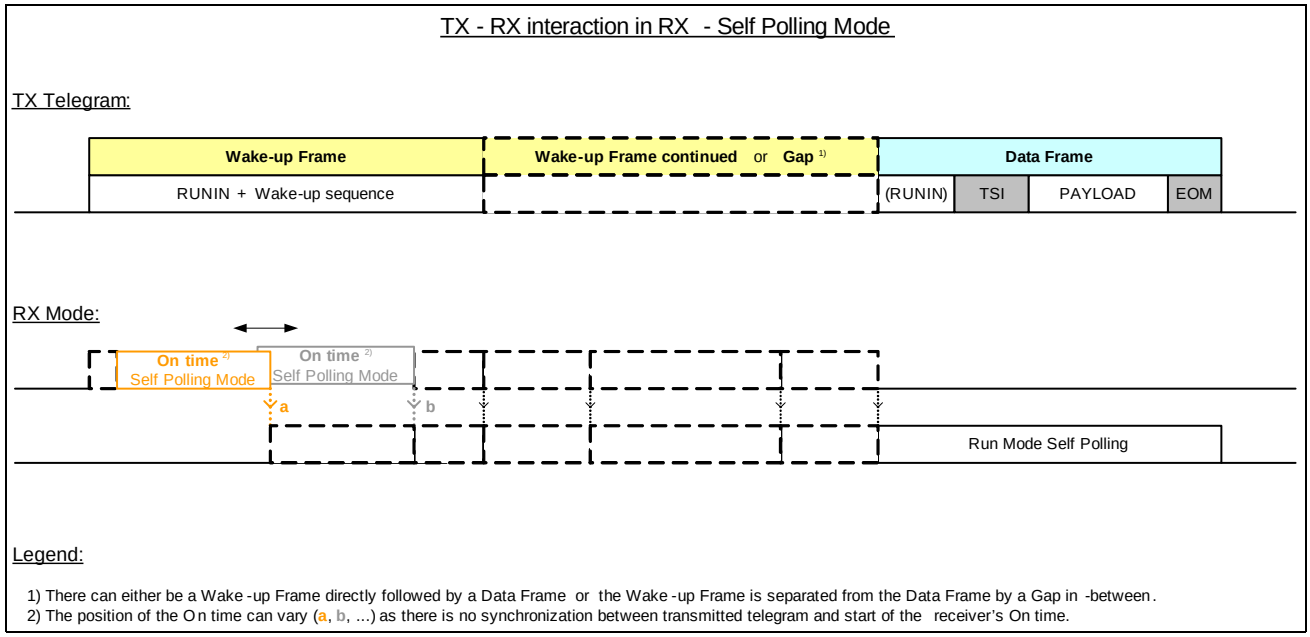


Figure 40 SPM - TX-RX Interaction

The transparent data stream can be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

Self Polling Mode is entered by setting the MSEL register bit to 1.

Configuration changes are allowed only by switching to SLEEP Mode, and returning to Self Polling Mode after reconfiguration.

The **Polling Timer Unit** controls the timing for scanning (On time) and sleeping (Off time, SPM_OFF). Up to four independent configuration sets (A, B, C and D) can automatically be processed, thus enabling scanning from different transmit sources. Additionally, up to 3 different frequency channels within each configuration may be scanned to support Multi-Channel applications. See also **Chapter 2.6.2 Polling Timer Unit**. So a total number of up to 12 different frequency channels is supported.

The **Wake-Up Generation Unit** identifies, whether an incoming data stream matches the configurable wake-up criterion.

After fulfillment of the wake-up criterion, modulation can be switched automatically.

See also **Chapter 2.6.1.6 Automatic Modulation Switching** and **Chapter 2.5.1.2 Data Interface** (in Subsection TMRDS).

The following state diagrams and explanations help to illustrate the behavior during Self Polling Mode. First there is a search for a wake-up criterion according to Configuration A on up to three different channels. Then, there is an optional search for a wake-up criterion according to Configuration B, C and D, again including up to 3 channels.

In applications using only Single-Configuration, settings are always taken from Configuration A.

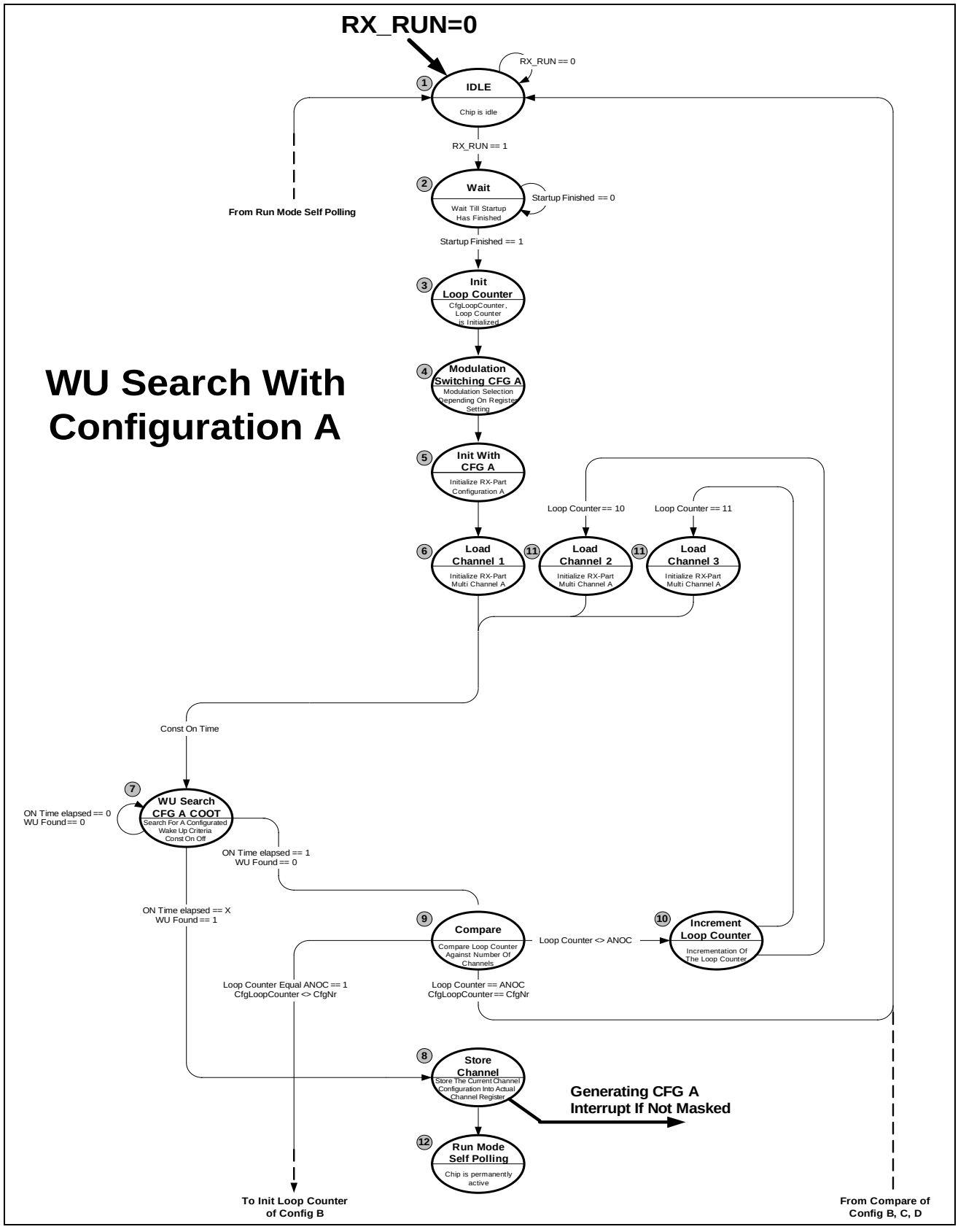


Figure 41 Wake-up Search with Configuration A

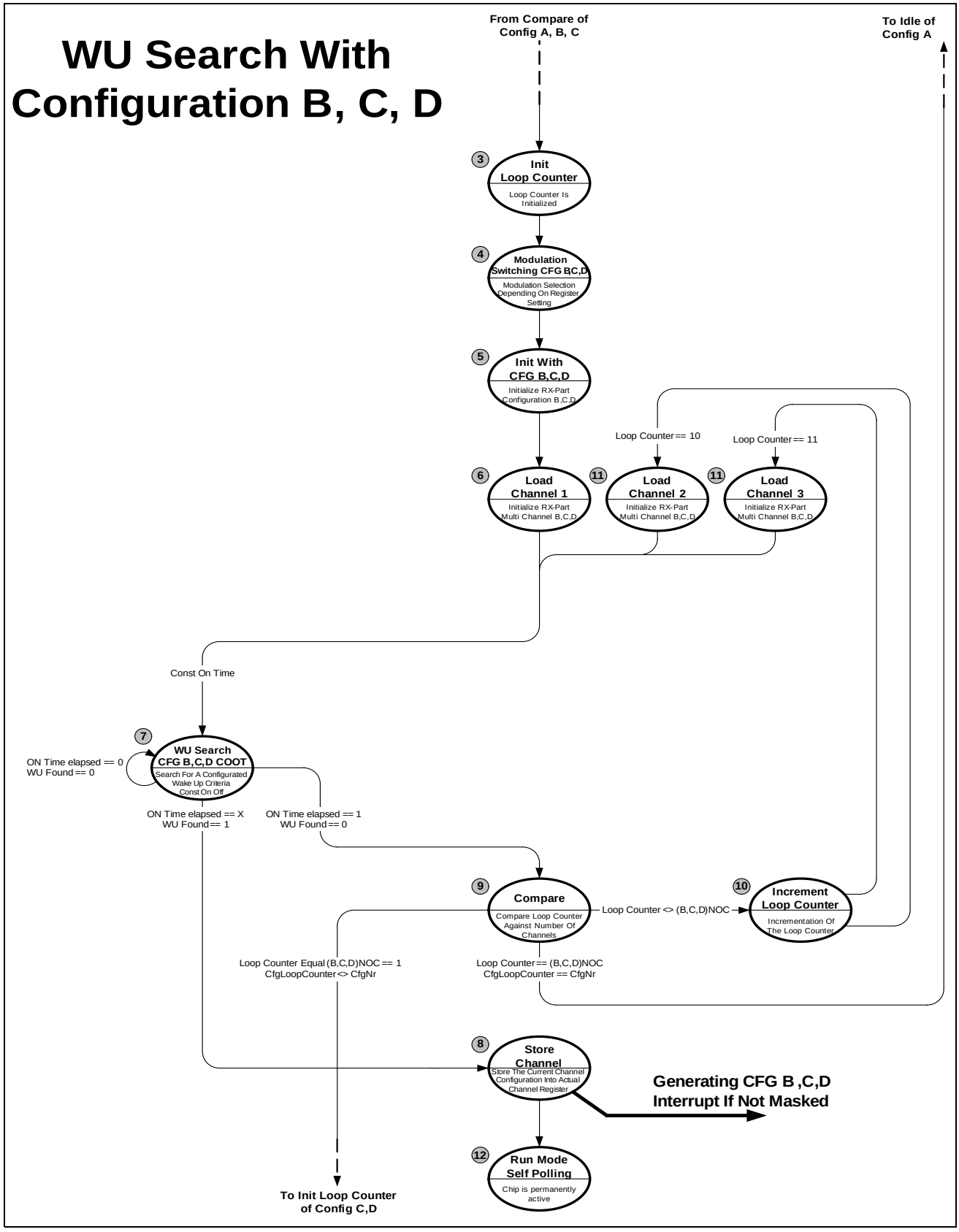


Figure 42 Wake-up Search with Configuration B, C, D

2.6.1.6 Automatic Modulation Switching

In **Self Polling Mode**, the chip is able to automatically change the type of modulation after a **wake-up** criterion was fulfilled in a received data stream. The type of modulation used in the different operational modes is selected by the SFR control bit MT.

2.6.1.7 Multi-Channel in Self Polling Mode

As previously mentioned, in Self Polling Mode the TDA5225 allows RF scans on up to three RF channels per configuration, this can be defined in the x_CHCFG register. Channel frequencies are defined in registers x_PLLINTCy, x_PLLFRAC0Cy, x_PLLFRAC1Cy, x_PLLFRAC2Cy, where x = A, B, C or D and y = 1, 2 or 3.

The channel number at which a wake-up criterion has been found is available in register RFPLLACC. See also **Chapter 2.4.5 Sigma-Delta Fractional-N PLL Block**.

2.6.1.8 Run Mode Self Polling (RMSP)

Wake-Up criterion fulfillment in Self Polling Mode for RSSI leads to a change to **Run Mode Self Polling** and a transparent data stream can be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

Modulation switching is performed automatically, depending on register settings (see **Chapter 2.6.1.6 Automatic Modulation Switching**)

Depending on interrupt masking, the host microcontroller is alerted when the level criterion RSSI is fulfilled. See also **Chapter 2.5.3 Interrupt Generation Unit**

Run Mode Self Polling is left, when the timeout timer command “EXTTOTIM” is sent by the Application Controller, or when an “EXTEOM found” command is sent by the microcontroller and the SFR bit EOM2SPM is activated, or when the operating mode is switched to SLEEP or Run Mode Slave by the host microcontroller.

When the TDA5225 gets the “EXTTOTIM” command, the receiver proceeds with Self Polling Mode and with searching for a suitable wake-up criterion on the next programmed channel (either next RF channel or next configuration, depending on the selected mode - Multi-Configuration or Multi-Channel or a mix of both) or a search for a wake-up criterion in Configuration A is initiated.

As long as the chip is in Run Mode Self Polling, the transparent data stream can be processed externally by the Application Controller.

After an EOM was found, the information about the RF channel and the configuration of the actual payload data is saved in the RFPLLACC register.

After receiving the “EXTEOM found” command the TDA5225 can either proceed with a search for a wake-up criterion in the next configuration or a search for wake-up in

Configuration A can follow or the TDA5225 can proceed receiving another (redundant) payload data frame within the same configuration.

The transparent data stream has to be processed externally by the Application Controller. Therefore the external controller needs the possibility to send following commands (see **Figure 43** and EXTPCMD register as well):

- EXTTOTIM: So the TDA5225 can proceed with Self Polling Mode (either with the next programmed channel or with Configuration A).
- EXTEOM found: In this case the TDA5225 can either proceed with Self Polling Mode (either with the next configuration or with Configuration A) or stay in Run Mode Self Polling.

When the actual processed configuration is right before the Off time and the Application Controller sends one of the above mentioned commands, then the TDA5225 can proceed with the Off time (in case next configuration is selected).

In Constant On-Off Time Mode the Polling Timer is always initialized after a TOTIM or EOM event. This means a new On period is always started.

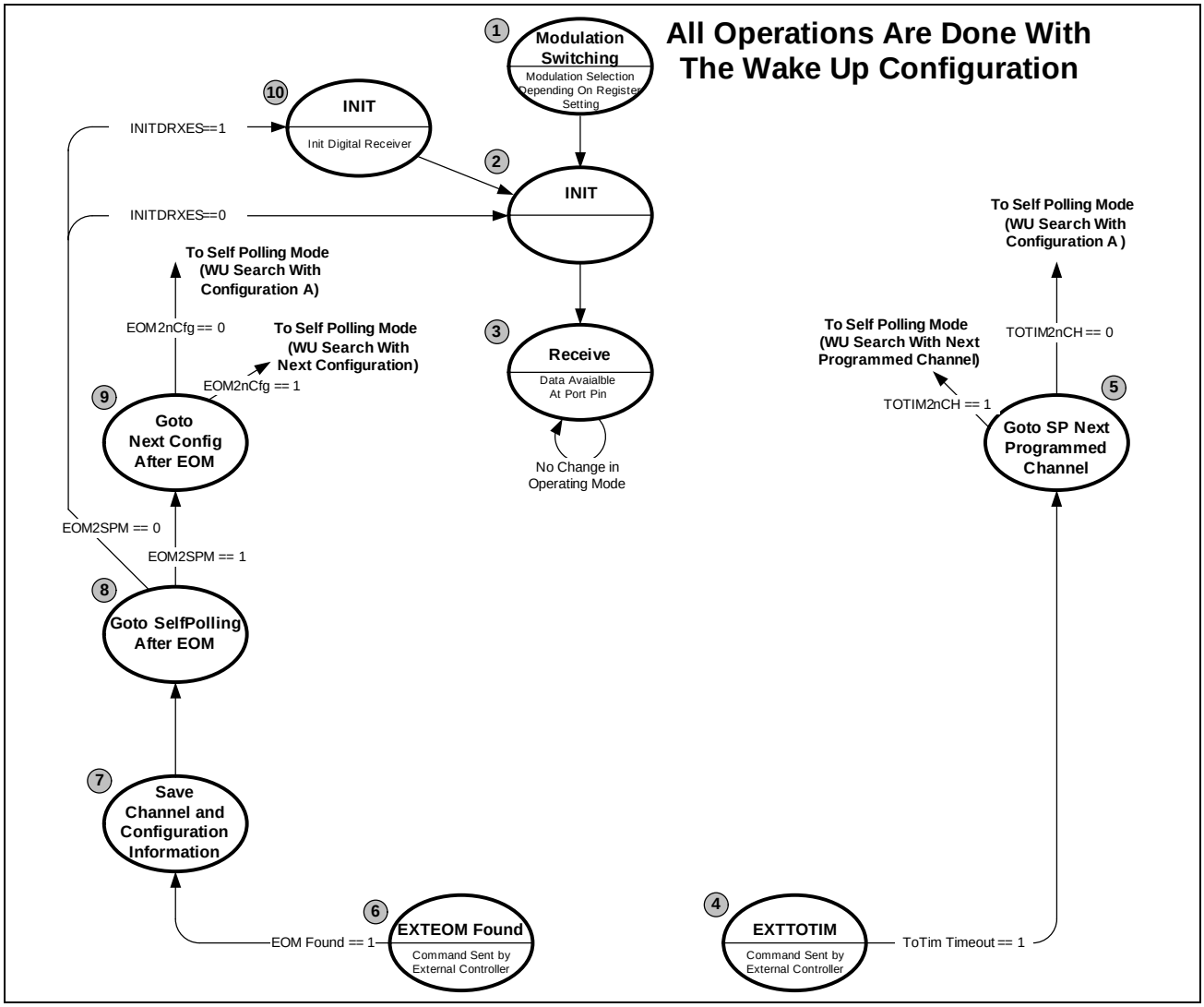


Figure 43 Run Mode Self Polling

2.6.2 Polling Timer Unit

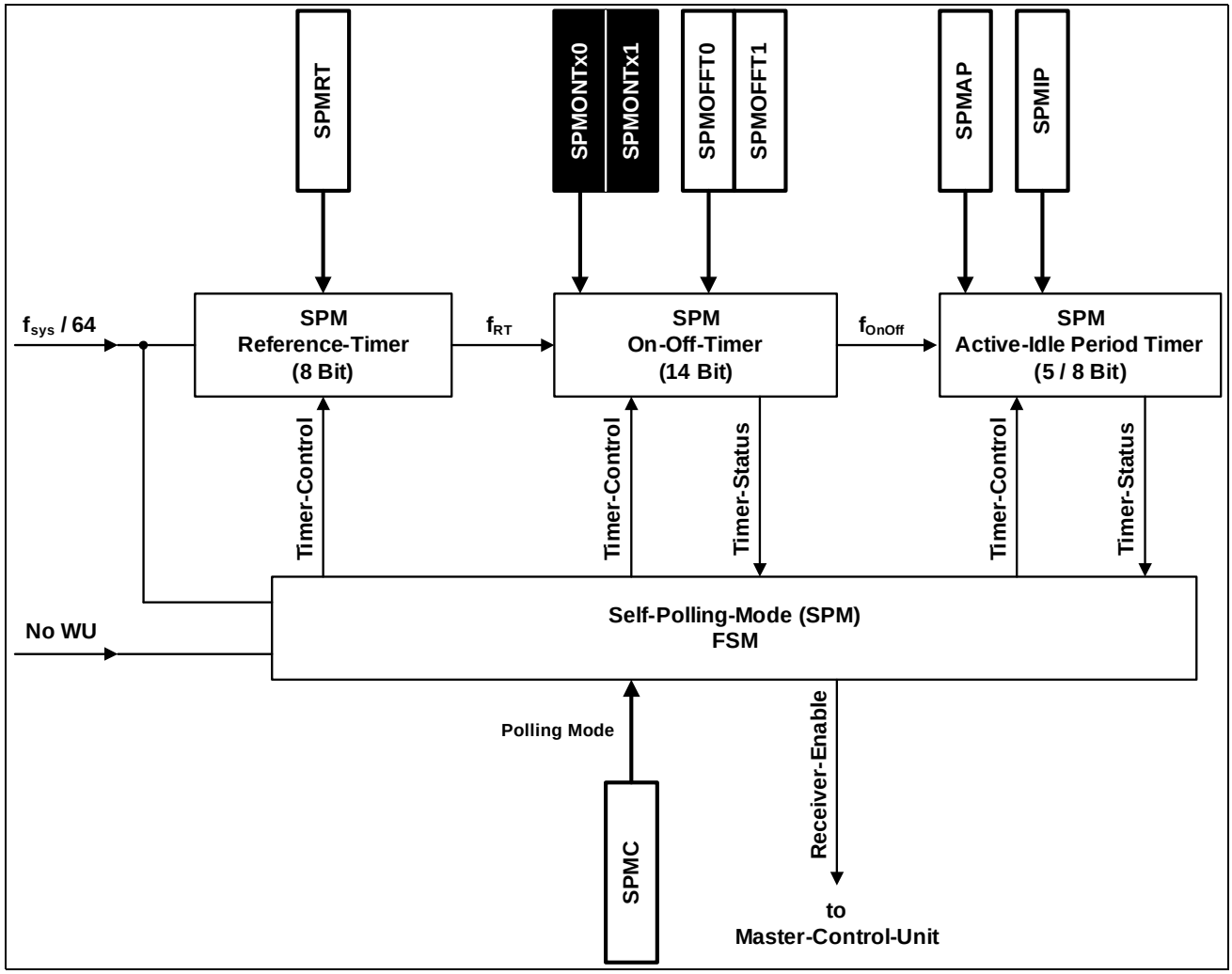


Figure 44 Polling Timer Unit

The Polling Timer Unit consists of a Counter Stage and a Control FSM (Finite State Machine).

The Counter Stage is divided into three sub-modules.

The **Reference Timer** is used to divide the state machine clock (f_{sys}/64) into the slower clock required for the SPM timers.

The **On-Off Timer** and the **Active Idle Period Timer** are used to generate the polling signal. The entire unit is controlled by the SPM FSM.

The TDA5225 is able to handle up to four different sets of configurations automatically. However, the example and figure in this subsection only show up to two configuration sets for the sake of clarity.

2.6.2.1 Self Polling Mode

An actual value for RSSI exceeding a certain adjustable threshold forces the TDA5225 into Run Mode Self Polling.

The timing resolution is defined by the Reference Timer, which scales the incoming frequency (f_{sys}/64) corresponding to the value, which is defined in the Self Polling Mode Reference Timer (SPMRT) register. Changing values of SPMRT helps to fit the final On-Off timing to the calculated ideal timing.

2.6.2.2 Constant On-Off Time (COO)

In this mode there is a constant On and a constant Off time. Therefore also the resulting master period time is constant. The On and Off time are set in the SPMONTA0, SPMONTA1, SPMONTB0, SPMONTB1, SPMONTC0, SPMONTC1, SPMONTD0, SPMONTD1, SPMOFFT0 and SPMOFFT1 registers. The On time configuration is done separately for Configuration A, B, C and D.

When **Single-Configuration** is selected then only Configuration A is used. The number of RF channels is defined in the A_CHCFG register (**Single-Channel** or **Multi-Channel** Mode).

Multi-Configuration Mode allows reception of up to 4 different transmit sources. The corresponding RF channels can be defined in the A_CHCFG, B_CHCFG, C_CHCFG and D_CHCFG registers. In the case of Multi-Channel or combination of Multi-Channel and Multi-Configuration Mode, the configured On time is used for each RF channel in a configuration. The diagram below shows possible scenarios.

All receive modes described in **Chapter 2.5.1.2 Data Interface** can be used.

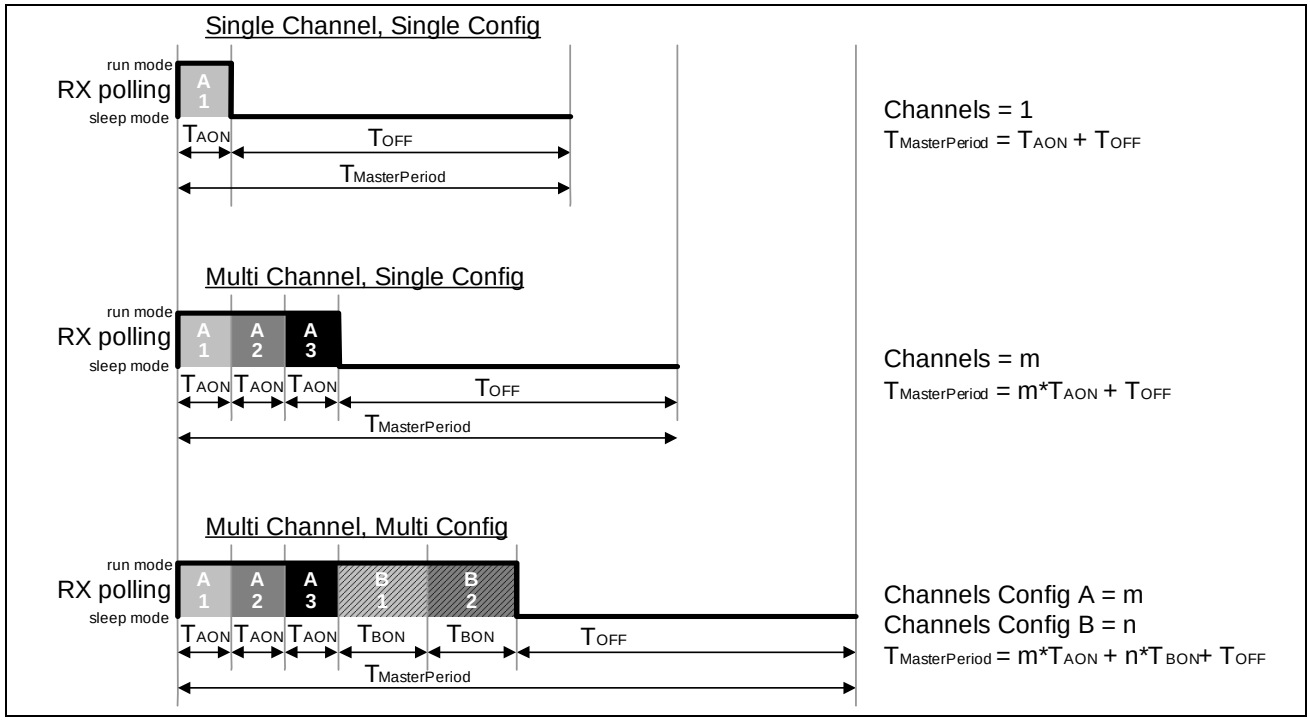


Figure 45 Constant On-Off Time

Calculation of the On time:

The On time for each channel must be long enough to ensure proper detection of a specified wake-up criterion. Therefore the On time depends on the wake-up pattern. It has to include transmitter data rate tolerances.

T_{ON} also must include the relevant start-up times. In case of the first channel after T_{OFF}, this is the Receiver Start-Up Time. In case of following channels (RF Receiver is already on, there is only a change of the channel or the configuration), e.g. if Configuration B is used, this is the Channel Hop Latency Time.

Calculation of the Off time:

The longer the Off time, the lower the average power consumption in Self Polling Mode. On the other hand, the Off time has to be short enough that no transmitted wake-up pattern is missed. Therefore the Off time depends mainly on the duration of the expected wake-up pattern.

If there are further channels scanned, T_{OFF} has to be reduced by the related additional On times.

For basic timing of WU on RSSI in COO mode, please see **Figure 46**.

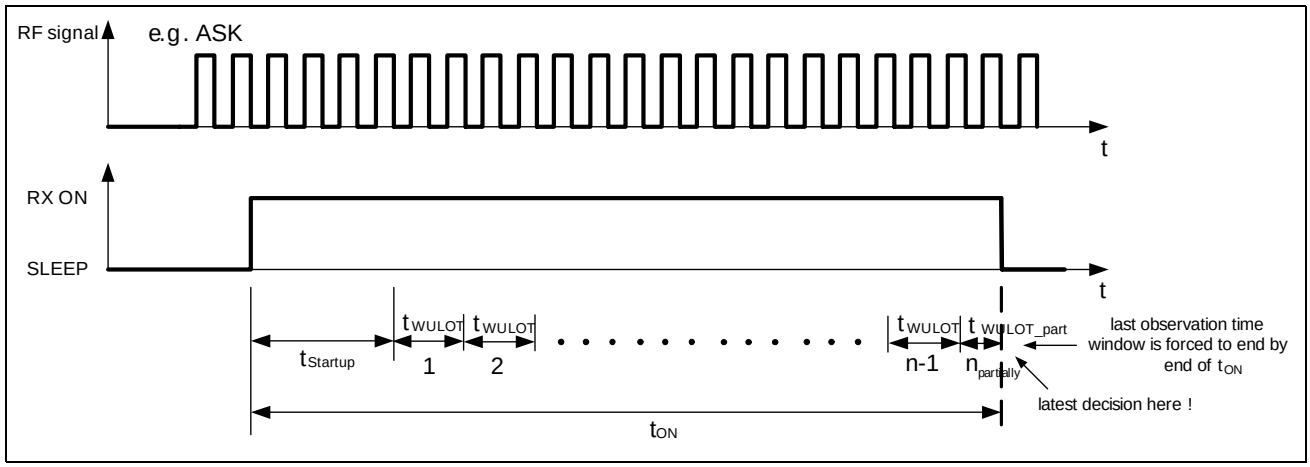


Figure 46 COO Polling in WU on RSSI Mode

Always check at the end of the current observation time window, if there is a WU (Wake-Up) event or NOT. This means, in algorithmic description (see also **Figure 10**, **Chapter 2.4.7 RSSI Peak Detector** and **Chapter 2.4.8.2 Wake-Up Generator**):

if (RSSIPWU_value > x_WURSSITHy) and (RSSIPWU_value > x_WURSSIBHy)

then WU

else NOT

Here, ‘NOT‘ means to keep on evaluating and move on to the next observation time window, also keep on peak value tracking of RSSIPWU signal. Keep on walking through the observation time windows until there is a WU event from the algorithm above or finally decide at the end of the On time with the following algorithm:

if (RSSIPWU_value > x_WURSSITHy) and (RSSIPWU_value < x_WURSSIBLy or RSSIPWU_value > x_WURSSIBHy)

then WU

else NOT

If there is a WU event at the end of an observation time window while walking through the observation time windows, freeze/hold this decision/peak value in register RSSIPWU for optional read out and switch to run mode self polling.

2.6.2.3 Active Idle Period Selection

This mode is used to deactivate some polling periods and can additionally be applied to the above mentioned Polling Mode.

Normally, polling starts again after the $T_{MasterPeriod}$. With this Active Idle Period selection some of the polling periods can be deactivated, independent from the Polling Mode. The active and the idle sequence is set with the SPMAP and the SPMIP registers. The values of these registers determine the factor M and N.

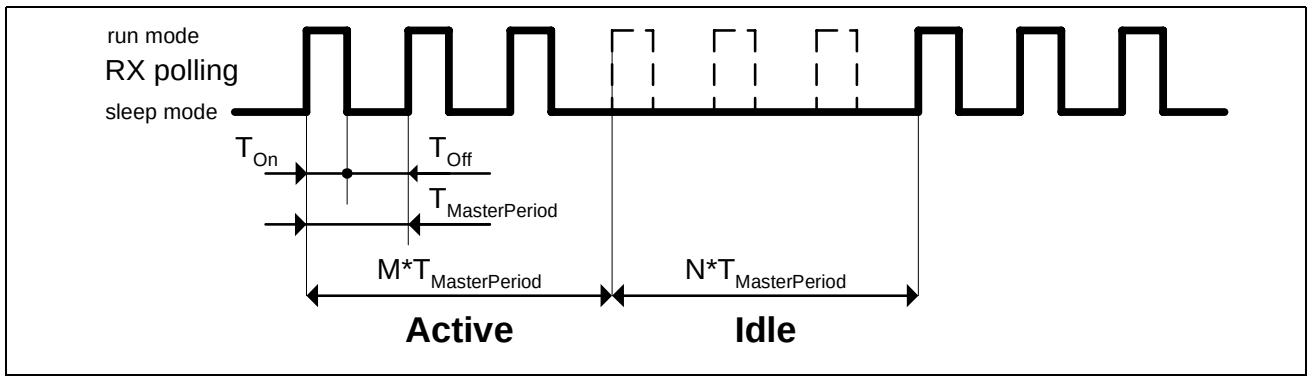


Figure 47 Active Idle Period

2.7 Definitions

2.7.1 Definition of Bit Rate

The definition for the bit rate in the following description is:

$$\text{bitrate} = \frac{\text{symbols}}{\text{s}}$$

If a symbol contains n chips (for Manchester n=2; for NRZ n=1) the chip rate is n times the bit rate:

$$\text{chiprate} = \text{n} \times \text{bitrate}$$

2.7.2 Definition of Manchester Duty Cycle

Several different definitions for the Manchester duty cycle *(MDC)* are in place. To avoid wrong interpretation some of the definitions are given below.

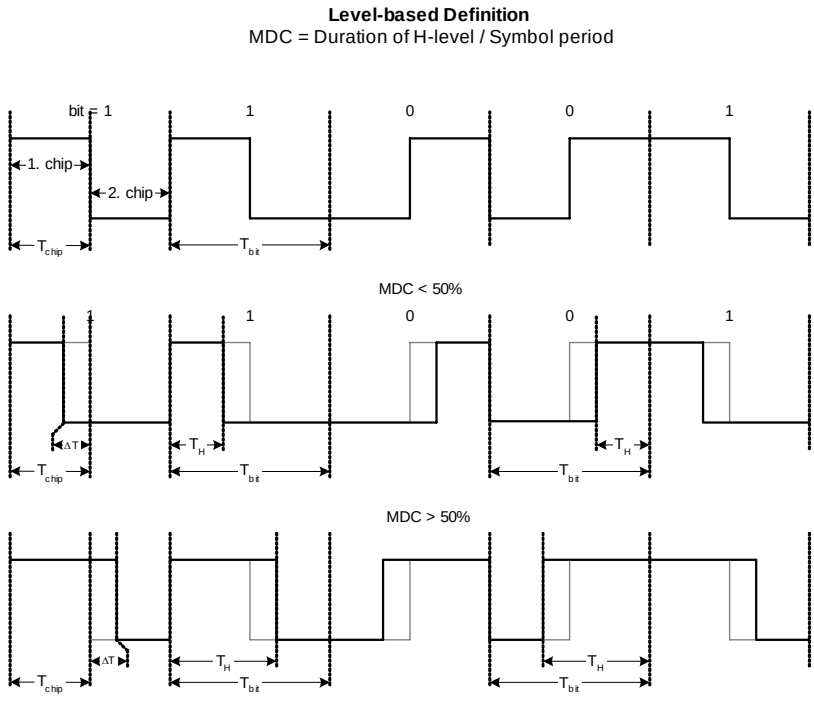


Figure 48 Definition A: Level-based definition

This definition determinates the duty cycle to be the ratio of the high pulse width and the ideal symbol period. The DC content is constant and directly proportional to the specified duty cycle.
For $\Delta T > 0$ the high period is longer than the chip-period and for $\Delta T < 0$ the high period is shorter than the chip-period.

Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_A = \frac{T_H}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}}$$

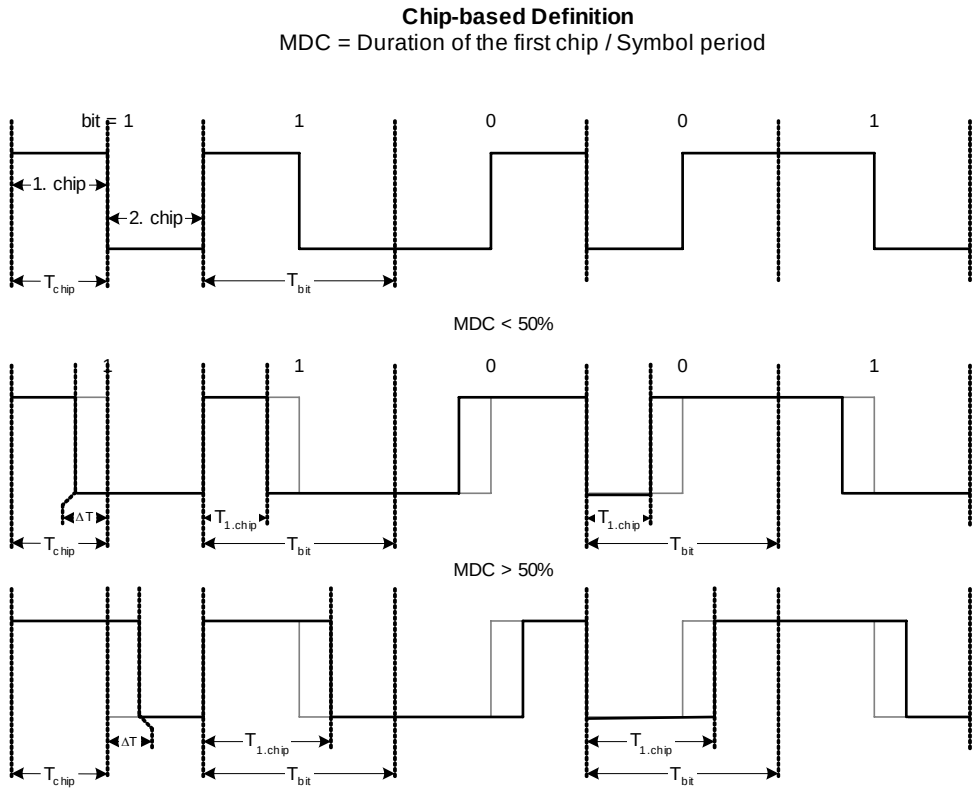


Figure 49 Definition B: Chip-based definition

This definition determinates the duty cycle to be the ratio of the first symbol chip and the ideal symbol period independently of the information bit content. The DC content depends on the information bit and it is balanced only if the message itself is balanced. For $\Delta T > 0$ the first chip-period is longer than the ideal chip-period and for $\Delta T < 0$ the first chip-period is shorter than the ideal chip-period.

Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_B = \frac{T_{1.chip}}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}}$$

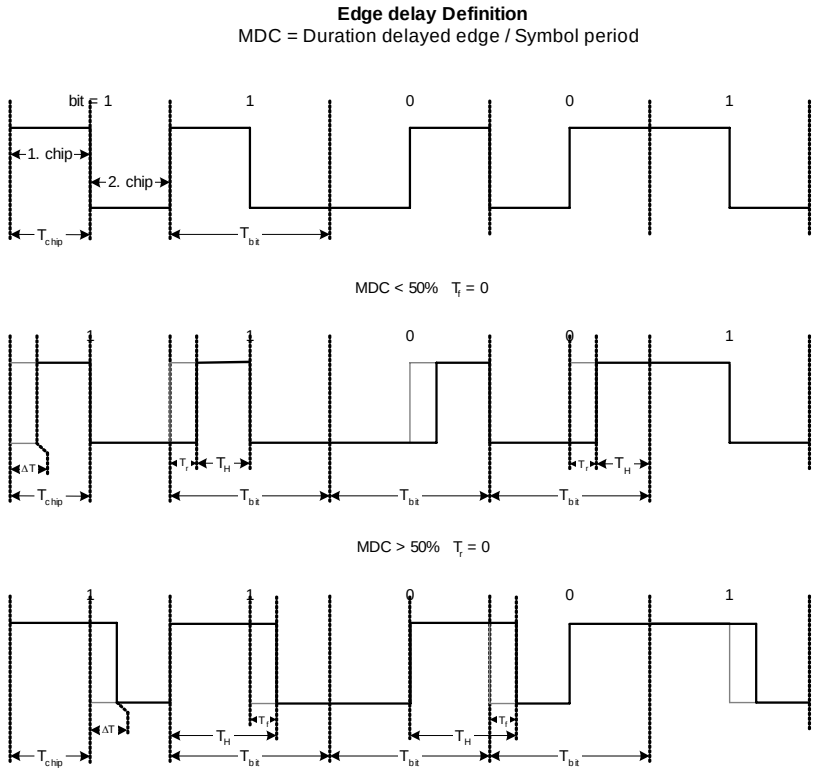


Figure 50 Definition C: Edge delay definition

This definition determinates the duty cycle to be the ratio of the duration of the delayed high-chip and the ideal symbol period independently of the information bit content. The position of the high-chip is determined by the delayed rising edge and/or the delayed falling edge. For $\Delta T = T_{fall} - T_{rise}$ the Manchester duty cycle is calculated to

$$MDC_C = \frac{T_{delayedHighchip}}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}} = \frac{T_{chip} + T_{fall} - T_{rise}}{T_{bit}}$$

Independent on the bit content, the same type of edge (rising edge and/or falling edge) is shifted.

2.7.3 Definition of Power Level

The reference plane for the power level is the input of the receiver board. This means, the power level at this point (P_r) is corrected for all offsets in the signal path (e.g. attenuation of cables, power combiners etc.).

The specification value of power levels in terms of sensitivity is related to the peak power of P_r in case of On-Off Keying (OOK). This is noted by the unit dBm peak.

Specification value of power levels is related to a Manchester encoded signal with a Manchester duty cycle of 50% in case of ASK modulation.

An RF signal generator usually displays the level of the unmodulated carrier ($P_{carrier}$). This has following consequences for the different modulation types:

Table 6 Power Level

Modulation scheme	Realization with RF signal generator	Power level specification value
ASK	AM 100%	$P_r = P_{carrier} + 6dB$
ASK	Pulse modulation (=OOK)	$P_r = P_{carrier}$
FSK	FM with deviation Δf: $f_1 = f_{carrier} - \Delta f$ $f_2 = f_{carrier} + \Delta f$	$P_r = P_{carrier}$

For power levels in sensitivity parameters given as average power, this is noted by the unit dBm. Peak power can be calculated by adding 3 dB to the average power level in case of ASK modulation and a Manchester duty cycle of 50%.

2.7.4 Symbols of SFR Registers and Control Bits

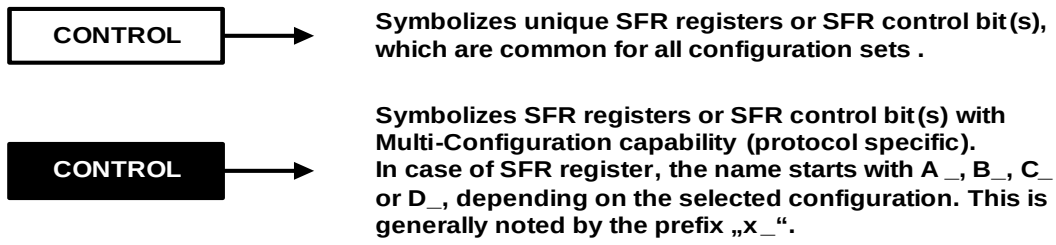


Figure 51 SFR Symbols

2.8 Digital Control (SFR Registers)

2.8.1 SFR Address Paging

An SPI instruction allows a maximum address space of 8 bit. The address space for supporting more than one configuration set is exceeding this 8 bit address room. Therefore a page switch is introduced, which can be applied via register SFRPAGE (see **Figure 52**).

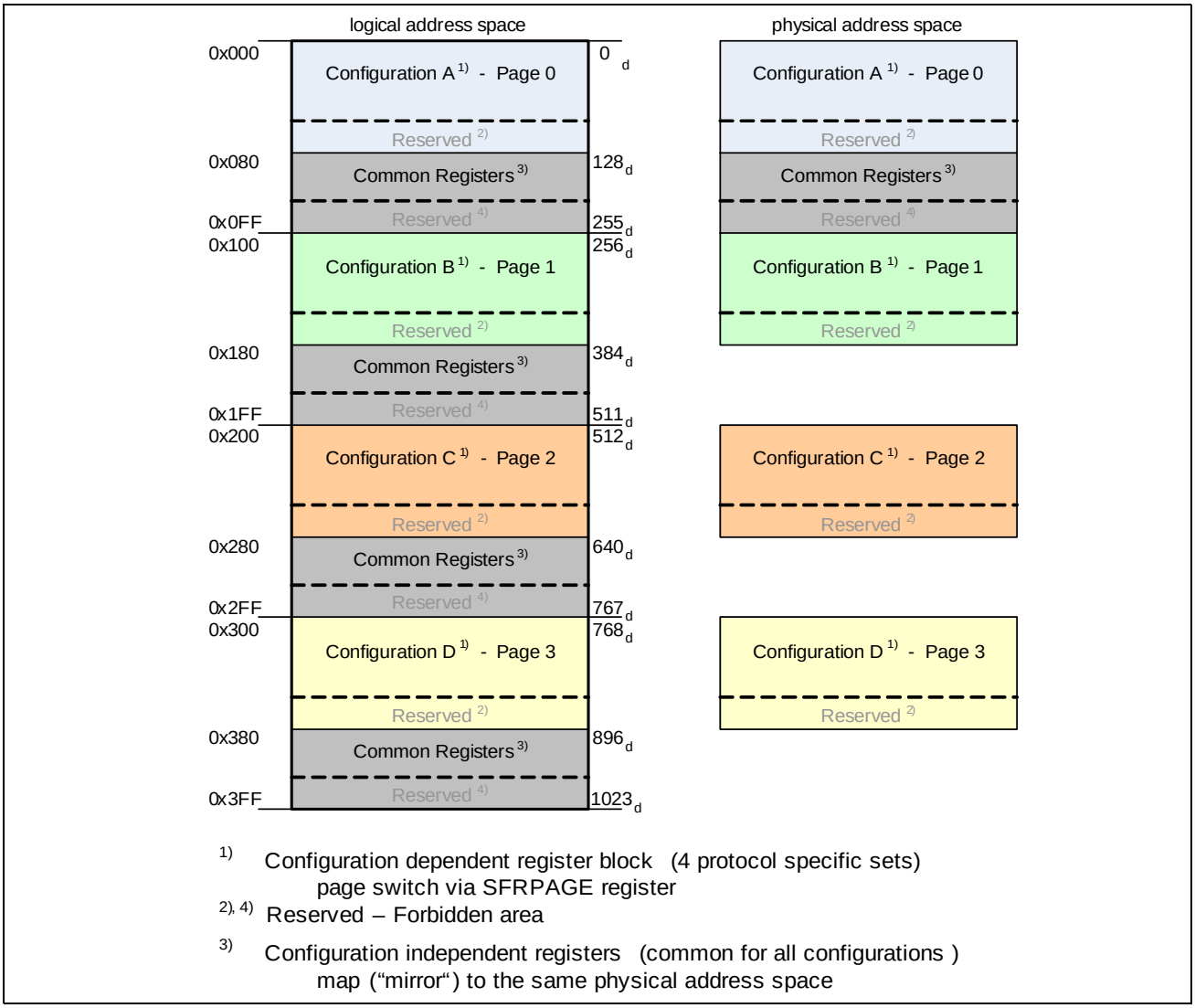


Figure 52 SFR Address Paging

2.8.2 SFR Register List and Detailed SFR Description

The register list is attached in the Appendix at the end of the document.

Registers for Configurations B, C and D are equivalent and not shown in detail.

All registers with prefix “A_” are related to Configuration A. All these registers are also available for Configuration B, C and D having the prefix “B_”, “C_” and “D_”.

3 Applications

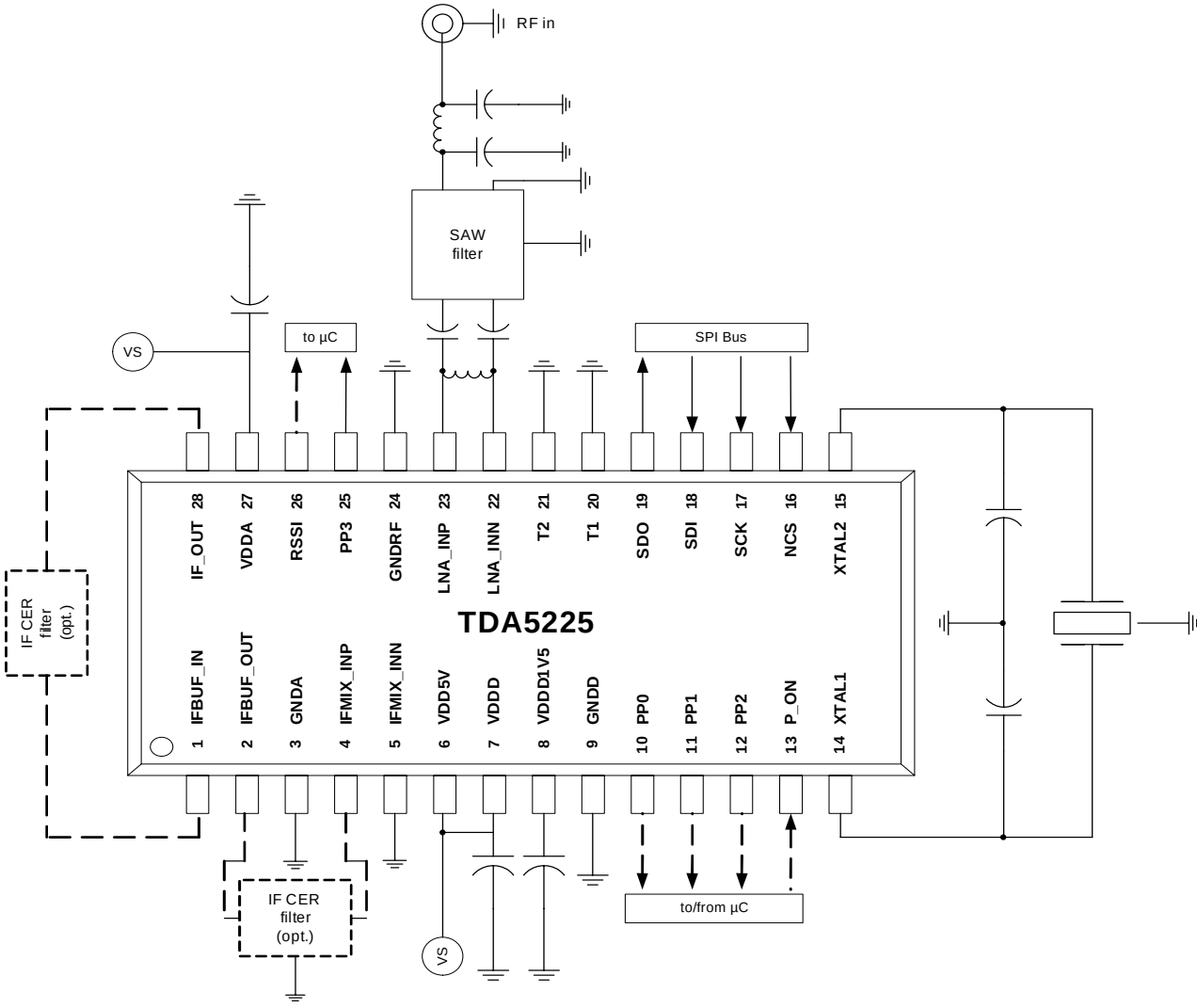


Figure 53 Typical Application Schematic

Note: As a good practice in any RF design, shielding around sensitive nodes can improve the EMC performance of the application.

For achieving the best sensitivity results the following has to be kept in mind. Every digital system generates certain frequencies (f_{SRC}, e.g. the crystal frequency or a microcontroller clock) and harmonics (N * f_{SRC}) of it, which can act as interferer (EMI source) and therefore sensitivity can be reduced.

There are two different cases, which need to be checked for the desired receive channel(s):

Elimination of in-band EMI mixing with (2*M + 1) * f_{LO}, where M > 0:

A square wave is used as LO (Local Oscillator) for the switching-type mixer, which also has odd harmonics. When the harmonics of the EMI source are exactly the IF frequency away from the harmonics of the LO, these spurs will be down-converted to the IF frequency and act as a co-channel interferer within the receiver's channel bandwidth mainly in the 315 MHz band.

In this case a change of the LO injection side (high side or low side injection) can be applied.

Example (Low Side LO-injection):

Wanted channel f_{RF} = 314.233MHz ==> f_{LO} = 303.533MHz ==> 3*f_{LO} = 910.599MHz

f_{XOSC} = 21.948717 MHz ==> 41 * f_{XOSC} = 899.8974 MHz

Resulting IF = 910.599 - 899.8974 MHz = 10.702 MHz ==> co-channel interferer within the receiver's channel bandwidth ==> change LO injection side

Example (High Side LO-injection):

Wanted channel f_{RF} = 314.233 MHz ==> f_{LO} = 324.933 MHz ==> 3*f_{LO} = 974.799 MHz

f_{XOSC} = 21.948717 MHz ==> 44 * f_{XOSC} = 965.744 MHz; 45 * f_{XOSC} = 987.692 MHz

==> both XOSC harmonics are not generating a co-channel interferer at 10.7 MHz

A final sensitivity measurement on the application hardware is recommended.

Elimination of in-band EMI mixing with 1 * f_{LO}:

Assuming a harmonic (N * f_{SRC}) is falling within the BW of the wanted channel and has an impact on the sensitivity there. In this case another XTAL frequency shall be selected, e.g. 10 kHz away

$$| N * f_{SRC} - f_{LocalOscillator} | < BW_{Channel}$$

Example (e.g. EMI source TDA5225 XOSC):

f_{XOSC} = 21.948717 MHz ==> 42 * f_{XOSC} = 921.846114 MHz

For further details please refer to the corresponding application note or to the latest configuration software.

3.1 Configuration Example

Please see configuration files supplied with the Explorer tool.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 7 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
A1	Supply Voltage at VDD5V pin	V_{smax}	-0.3	+6	V	
A2	Supply Voltage at VDDD, VDDA pin	V_{smax}	-0.3	+4	V	
A3	Voltage between VDD5V vs VDDD and VDD5V vs VDDA	V_{smax}	-0.3	+4	V	
A4	Junction Temperature	T_j	-40	+125	°C	
A5	Storage Temperature	T_s	-40	+150	°C	
A6	Thermal resistance junction to air	$R_{th(ja)}$		140	K/W	
A7	Total power dissipation at T_{amb} = 105°C	P_{tot}		100	mW	
A8	ESD HBM integrity	V_{HBMRF}	-2	2	KV	According to ESD Standard JEDEC EIA / JESD22-A114-B
A9	ESD SDM integrity (All pins except corner pins)	V_{SDM}	-500	500	V	
A10	ESD SDM integrity (All corner pins)	V_{SDM}	-750	750	V	
A11	Latch up	I_{LU}	100		mA	AEC-Q100 (transient current)
A12	Maximum input voltage at digital input pins	V_{inmax}	-0.3	V_{DD5V}+0.5 or 6.0	V	whichever is lower
A13	Maximum current into digital input and output pins	I_{IOmax}		4	mA	

4.1.2 Operating Range

Table 8 Supply Operating Range and Ambient Temperature

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
B1	Supply voltage at pin VDD5V	V_{DD5V}	4.5	5.5	V	Supply voltage range 1
B2	Supply voltage at pin VDD5V=VDDD=VDDA	V_{DD3V3}	3.0	3.6	V	Supply voltage range 2
B3	Ambient temperature	T_{amb}	-40	105	°C	

4.1.3 AC/DC Characteristics

Supply voltage VDD5V = 4.5 to 5.5 Volt or VDD5V = VDDA = VDDD = 3.0 to 3.6 Volt
Ambient temperature T_{amb} = -40...105°C; T_{amb} = +25°C and VDD5V = 5.0V or VDD5V = VDDA = VDDD = 3.3V for typical parameters, unless otherwise specified.

■ not subject to production test - verified by characterization/design

Table 9 AC/DC Characteristics

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
General DC Characteristics								
C1.1	Supply Current in Run Mode and Double Down Conversion Mode	$I_{Run, Double}$		12	15	mA	ASK or FSK mode P_{in} < -50dBm	
C1.2	Supply Current in Run Mode and Single Down Conversion Mode	$I_{Run, Single}$		10.5	14	mA	ASK or FSK mode P_{in} < -50dBm	
C2	Supply current in Sleep Mode	I_{sleep_low}					crystal oscillator in Low Power Mode; clock generator off; valid for SLEEP Mode and during SPM Off time	
	T_{amb} = 25 °C			40	50	µA		
	T_{amb} = 85 °C			60	110	µA		■
	T_{amb} = 105 °C			90	160	µA		■
C3	Supply current in Sleep Mode	I_{sleep_high}		115	350	µA	crystal oscillator in High Precision Mode C_{load} = 25 pF; clock generator off; valid for SLEEP Mode and during SPM Off time	
C4	Supply current in Power Down Mode	I_{PDN}						
	T_{amb} = 25 °C			0.8	1.5	µA		
	T_{amb} = 85 °C			3.7	13	µA		■
	T_{amb} = 105 °C			9.0	27	µA		■
C5	Supply current clock generator	I_{clock}		23	27	µA	$f_{clockout}$ = 1 kHz C_{load} = 10 pF	■
C6	Supply current IF-Buffer	I_{Buffer}		0.5	0.7	mA	f_{IF_1} = 10.7 MHz R_{load} = 330 Ω no AC signal	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
C7	Supply current during RF-FE startup / BPF calibration	$I_{RF\text{-}FE\text{-}startup,BPFcal}$		2.2	2.9	mA		■
C8	Brownout detector threshold	V_{BOR}	2.3	2.45	2.6	V		
C9	Receiver reset time	t_{Reset}	1.0		3.0	ms	Note: No SPI communication is allowed before XOSC start-up is finished and chip reset is already finished	
C10	Receiver startup time	$t_{RXstartup}$	455	455	455	µs	Time to startup RF frontend (comprises time required to switch crystal oscillator from Low Power Mode to High Precision Mode	■
C11	RF Channel Hop Latency Time and Configuration (Hop) Change Latency Time (e.g. Cfg A to Cfg B)	t_{C_Hop}	111	111	111	µs	Time to switch RF PLL between different RF Channels (does not include settling of Data Clock Recovery) and time to change Configuration	■
C12	RF Frontend startup delay	$t_{RFstartdelay}$	350	350	350	µs	Delay of startup of RF frontend	■
C13	P_ON pulse width	t_{P_ON}	15			µs	Minimal pulse width to reset the chip	■
C14	NINT pulse length	t_{NINT_Pulse}		12		µs	Pulse width of interrupt	■
C15	Accuracy of Temperature Sensor						Valid for temperature range -40°C .. +105°C; using upper 8 ADC bits (ADCRESH)	
C15.1	uncalibrated	$T_{Error, uncal}$			+/- 23	°C	uncalibrated (3 sigma) value	■
C15.2	calibrated	$T_{Error, cal}$			+/- 4.5	°C	after 1-point calibration at room temperature (3 sigma)	■
C16	Accuracy of VDDD readout						Valid for temperature range -40°C .. +105°C; using upper 8 ADC bits (ADCRESH)	
C16.1	uncalibrated	$V_{DDD, Error, uncal}$			+/- 200	mV	uncalibrated (3 sigma) value	■
C16.2	calibrated	$V_{DDD, Error, cal}$			+/- 25	mV	after 1-point calibration at room temperature (3 sigma)	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
General RF Characteristics (overall)								
D1	Frequency							
	Range 1	f_{band_1}	300		320	MHz	1st Local Oscillator Low Side LO-injection and High Side LO-injection allowed; See also **Chapter 3**	
	Range 2	f_{band_2}	425		450	MHz		
	Range 3	f_{band_3}	863		870	MHz		
	Range 4	f_{band_4}	902		928	MHz		
D2	Frequency step of Sigma-Delta PLL	f_{step}	10.5			Hz	$f_{step} = f_{XTAL} / 2^{21}$	■
D3	ASK Demodulation							
	Data Rate	R_{data}	0.5		40	kchip/s		■
	Data rate tol.	R_{data_tol}	-10		+10	%		■
	Modulation index	m_{ASK}	50		100	%	ASK	■
		m_{OOK}	99		100	%	ON-OFF keying	■
D4	FSK Demodulation							
	Data Rate	R_{data}	0.5		112	kchip/s	including tolerance	■
	Data rate tol.	R_{data_tol}	-10		+10	%		■
	Frequency deviation	Δf	1		64	kHz	frequency deviation zero-peak	■
	Modulation index	m_{FSK}	1.0				m = frequency_deviation$_{zero\text{-}peak}$ / maximum_occuring_data_frequency; m >= 1.25 is recommended at small frequency deviation	■
D5	Decoding schemes							
			Manchester, differential Manchester, Bi-phase Mark / Bi-phase Space					
	Duty cycle ASK	T_{chip}/T_{data}	35		55	%	see **Chapter 2.7.2** Definition C	■
	Duty cycle FSK	T_{chip}/T_{data}	45		55	%	see **Chapter 2.7.2** Definition B	■
D6	Overall noise figure						RF input matched to 50 Ω @ T_{amb} = 25 °C	
	Noise figure	NF		6	8	dB		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D7	BER Sensitivity (FSK)						BER = $2*10^{-3}$	
		Manchester coding; for additional test conditions see right after this table					RF input matched to 50 Ω @ T_{amb} = 25 °C; Single-Ended Matching without SAW; Insertion loss of input matching network = 1dB; Receive Mode = TMMF (sampled with ideal data clock); Double Down Conversion	
D7.1	Data Rate 2 kBit/s; Δf = 10 kHz	$SFSK1_{BER}$		-119	-116	dBm	2nd IF BW = 50 kHz PDF = 33 kHz, AFC off, IFATT=0	■
D7.2	Data Rate 10 kBit/s; Δf = 14 kHz	$SFSK2_{BER}$		-114	-111	dBm	2nd IF BW = 50 kHz PDF = 65 kHz, AFC off, IFATT=0	■
D7.3	Data Rate 10 kBit/s; Δf = 50 kHz	$SFSK3_{BER}$		-112	-109	dBm	2nd IF BW = 125 kHz PDF = 132 kHz, AFC off, IFATT=0	■
D7.4	Data Rate 50 kBit/s; Δf = 50 kHz	$SFSK4_{BER}$		-105	-102	dBm	2nd IF BW = 300 kHz PDF = 239 kHz, AFC off, IFATT=0	■
D7.5	Data Rate 2 kBit/s; Δf = 10 kHz	$SFSK5_{BER}$		-110	-107	dBm	2nd IF BW = 300 kHz PDF = 282kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
D7.6	Data Rate 10 kBit/s; Δf = 14 kHz	$SFSK6_{BER}$		-106	-103	dBm	2nd IF BW = 300 kHz PDF = 282kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
D7.7	Data Rate 10 kBit/s; Δf = 50 kHz	$SFSK7_{BER}$		-110	-107	dBm	2nd IF BW = 300 kHz PDF = 282kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D8	BER Sensitivity (OOK)						BER = $2*10^{-3}$ RF input matched to 50 Ω @ T_{amb} = 25 °C, peak power level (see **Chapter 2.7.3**); Single-Ended Matching without SAW; Insertion loss of input matching network = 1dB; Receive Mode = TMMF (sampled with ideal data clock); Double Down Conversion	
		Manchester coding; for additional test conditions see right after this table						
D8.1	Data Rate 0.5 kBit/s	$SASK1_{BER}$		-120	-117	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.2	Data Rate 2 kBit/s	$SASK2_{BER}$		-116	-113	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.3	Data Rate 10 kBit/s	$SASK3_{BER}$		-111	-108	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.4	Data Rate 16 kBit/s	$SASK4_{BER}$		-109	-106	dBm peak	m = 100%, IFATT=0 2nd IF BW = 80 kHz	■
D8.5	Data Rate 0.5 kBit/s	$SASK5_{BER}$		-115	-112	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.6	Data Rate 2 kBit/s	$SASK6_{BER}$		-112	-109	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.7	Data Rate 10 kBit/s	$SASK7_{BER}$		-106	-103	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.8	Data Rate 16 kBit/s	$SASK8_{BER}$		-104	-101	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D9.1	Sensitivity increase for Single Down Conversion mode	ΔS_{SDC}	0	0.5	1	dB		■
D9.2	Double Down Conversion sensitivity decrease for higher blocking performance (IFATT=0 => IFATT=7)	$\Delta S_{DDC,\ IFATT7}$		1	2	dB		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D9.3	Single Down Conversion sensitivity decrease for higher blocking performance (IFATT=4 => IFATT=7)	$\Delta S_{SDC, IFATT7}$		0.5	1	dB		■
D10.1	Sensitivity variation due to temperature (-40...+105°C)	ΔP_{in}			2	dB	relative to T_{amb} = 25 °C; temperature drift of crystal not considered	■
D10.2	Sensitivity variation due to frequency offset [1)]	ΔP_{in}			3	dB	AFC inactive; For Sensitivity Bandwidth see **Table 10**	■
D10.3	Sensitivity variation due to frequency offset	ΔP_{in}			3	dB	AFC active, slow AFC; For Sensitivity Bandwidth see **Table 10** and applied AFCLIMIT	■
D10.4	Sensitivity loss when AFC active at center frequency	ΔP_{in}			1	dB	AFC active; center frequency - no AFC wander (see **Chapter 2.4.6.3**)	■
D11	3rd order intercept IIP3	P_{IIP3}	-16	-14		dBm	input matched to 50 Ω; Insertion loss of input matching network = 1dB; IFATT = 7; valid for Single and Double Down Conversion Mode	■
D12	1 dB compression point CP1dB	P_{CP1dB}	-27	-25		dBm	input matched to 50 Ω; Insertion loss of input matching network = 1dB; IFATT = 7; valid for Single and Double Down Conversion Mode	■
D13	1st IF image rejection	d_{image1}	30	40		dB	1st IF = 10.7 MHz without front end SAW filter; valid for Double Down Conversion Mode	
D14	2nd IF image rejection	d_{image2}	30	34		dB	2nd IF = 274 kHz without 1st IF CER filter; valid for Single and Double Down Conversion Mode	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
RF Front End Characteristics (Unless otherwise noted, all values apply for the specified frequency ranges)								
E1	LNA input impedance							
E1.1	f_{RF} = 315 MHz	$R_{in\_p,diff}$		680		Ω	differential parallel equivalent input between LNA_INP and LNA_INN	■
		$C_{in\_p,diff}$		1.05		pF		■
E1.2	f_{RF} = 434MHz	$R_{in\_p,diff}$		570		Ω		■
		$C_{in\_p,diff}$		0.87		pF		■
E1.3	f_{RF} = 868MHz	$R_{in\_p,diff}$		550		Ω		■
		$C_{in\_p,diff}$		0.63		pF		■
E1.4	f_{RF} = 915MHz	$R_{in\_p,diff}$		540		Ω		■
		$C_{in\_p,diff}$		0.63		pF		■
E1.5	f_{RF} = 315 MHz	$R_{in\_p,\ SE}$		500		Ω	single-ended parallel equivalent input between LNA_INP and GNDRF / LNA_INN and GNDRF	■
		$C_{in\_p,\ SE}$		1.87		pF		■
E1.6	f_{RF} = 434MHz	$R_{in\_p,\ SE}$		400		Ω		■
		$C_{in\_p,\ SE}$		1.63		pF		■
E1.7	f_{RF} = 868MHz	$R_{in\_p,\ SE}$		322		Ω		■
		$C_{in\_p,\ SE}$		1.59		pF		■
E1.8	f_{RF} = 915MHz	$R_{in\_p,\ SE}$		312		Ω		■
		$C_{in\_p,\ SE}$		1.56		pF		■
E2	FE output impedance	R_{out_IF}	290	330	380	Ω	f_{IF} = 10.7 MHz	■
E3	FE voltage conversion gain	$AV_{FE,\ max}$	34	36	38	dB	min. IF attenuation (IFATT = 0); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	
E4	FE voltage conversion gain	AV_{FE_7}	29	31	33	dB	IF attenuation (IFATT = 7); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
E5	FE voltage conversion gain	$AV_{FE, min}$	22	24	26	dB	max. IF attenuation (IFATT = 15); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	
E6	FE voltage conversion gain step			0.8		dB	12dB / 15 = 0.8dB/step Double Down Conversion: 16 gain settings (4 bit) Single Down Conversion: 7 gain settings	■
E7	1^{st} Local Oscillator SSB Noise						closed loop	
E7.1	PLL loop Bandwidth	BW	100	150	200	kHz	BW and its tolerances	■
E7.2	f_{in_R1} = 315MHz	d_{SSB_LO}		-81	-76	dBc/Hz	@ f_{offset} = 1 kHz	■
				-85	-80		@ f_{offset} = 10 kHz	■
				-82	-77		@ f_{offset} = 100 kHz	■
				-120	-115		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.3	f_{in_R2} = 434MHz	d_{SSB_LO}		-78	-73	dBc/Hz	@ f_{offset} = 1 kHz	■
				-83	-78		@ f_{offset} = 10 kHz	■
				-82	-77		@ f_{offset} = 100 kHz	■
				-117	-112		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.4	f_{in_R3} = 868MHz	d_{SSB_LO}		-75	-70	dBc/Hz	@ f_{offset} = 1 kHz	■
				-79	-74		@ f_{offset} = 10 kHz	■
				-77	-72		@ f_{offset} = 100 kHz	■
				-114	-109		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.5	f_{in_R4} = 915MHz	d_{SSB_LO}		-71	-66	dBc/Hz	@ f_{offset} = 1 kHz	■
				-79	-74		@ f_{offset} = 10 kHz	■
				-77	-72		@ f_{offset} = 100 kHz	■
				-116	-111		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E8.1	Spurious emission < 1 GHz				-57	dBm		■
E8.2	Spurious emission > 1 GHz				-47	dBm		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
E9	Inband fractional spur		-40			dBc		■
E10	3dB Overall Analog Frontend Bandwidth	BW_{ANA}		230		kHz	LNA input to Limiter output, excluding external CER filter	■
1st IF Buffer Characteristics								
F1	Input impedance	R_{in_IF}	290	330	370	Ω	f_{IF} = 10...12 MHz	■
F2	Output impedance	R_{out_IF}	290	330	370	Ω	f_{IF} = 10...12 MHz	■
F3	Voltage gain	AV_{Buffer}	3	4	5	dB	f_{IF} = 10...12 MHz Z_{source} = 330 Ω Z_{load} = 330 Ω	
F4	Buffer switch isolation (CERFSEL)	$d_{isolation}$	60			dB	f_{IF} = 10...12 MHz see **Figure 6**	■
2nd IF Mixer, RSSI and Filter Characteristics								
G1	Mixer input impedance	R_{in_IF}	290	330	390	Ω	f_{IF} = 10...12 MHz	■
G6	RSSI						Related to RF input matched to 50 Ω	
G2.1	Dynamic range (Linearity +/- 2 dB)	DR_{RSSI}	-110		-30	dBm	applies for digital RSSI; AGC on	■
			-115		-60	dBm	applies for analog RSSI @ 50kHz BPF, AFGC off	■
			-110		-50	dBm	applies for analog RSSI @ 300kHz BPF, AFGC off	■
G2.2	Linearity	DR_{LIN}	-1		+1	dB	-95 dBm...-35 dBm; applies for digital RSSI	■
G2.3	Temperature drift within linear dynamic range	DR_{TEMP}	-2.5		+1.5	dB	-95 dBm...-35 dBm; applies for digital RSSI	■
G2.4	Output dynamic range	V_{RSSI+}	0.8		2.0	V		
G2.5	analog RSSI error, untrimmed	$DRSSI_{ana}$	-4		+2	dB	at RSSI pin	
G2.6	analog RSSI slope, untrimmed	dV_{RSSI}/ dV_{mix_in}	8	10	12	mV/dB	at RSSI pin; typical 600 mV/60 dB = 10 mV/dB	
G2.7	digital RSSI error, untrimmed	$DRSSI_{dig\_u}$	-4		+2	dB	RSSI register readout	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
G2.8	digital RSSI error, user trimmed via SFRs RSSISLOPE and RSSIOFFS	$DRSSI_{dig\_t}$	-1		+1	dB	RSSI register readout	■
G2.9	digital RSSI slope, untrimmed	dV_{RSSI}/dV_{mix_in}	2	2.5	3	LSB /dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1mV = 1 LSB (10-bit ADC) 8-bit readout: 4mV=1LSB	
G2.10	digital RSSI slope, user trimmed via SFRs RSSISLOPE and RSSIOFFS	dV_{RSSI}/dV_{mix_in}	2.35	2.5	2.65	LSB /dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1mV = 1 LSB (10-bit ADC) 8-bit readout: 4mV=1LSB	■
G2.11	Resistive load at RSSI pin	$R_{L,RSSImax}$	100			kΩ		■
G2.12	Capacitive load at RSSI pin	$C_{L,RSSI}$			20	pF		■
G3	2nd IF Filter (3rd order Bandpass Filter)							
G3.1	Center frequency	f_{center}	262	274	288	kHz	Asymmetric BPF corners: f_center=sqrt(f_{low} * f_{high}); Use AFC for more symmetry	
G3.2	-3 dB BW	BW_{-3dB}		50 80 125 200 300		kHz		■
G3.3	-3 dB BW tolerance	tol_BW_{-3dB}	-5		+5	%	For BW = 125, 200, 300 kHz	■
G3.4	-3 dB BW tolerance	tol_BW_{-3dB}	-6		+6	%	For BW = 50, 80 kHz	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Crystal Oscillator Characteristics								
H1	Frequency range	f_{XTAL}		21.948 717		MHz		
H2	Crystal parameters							
H2.1	Motional capacitance	C_1	3	6	10	fF		■
H2.2	Motional resistance	R_1		18	80	Ω		■
H2.3	Shunt capacitance	C_0		2	4	pF		■
H2.4	Load capacitance	C_{Load}		12		pF	nominal value	■
H2.5	Initial frequency tolerance	f_{XTAL_Tol}	-30		+30	ppm	oscillator untrimmed (trim capacitor default settings, usage of recommended crystal); not including crystal tolerances	■
H2.6	Frequency trimming range	Δf_{XTAL}	-50		+50	ppm	larger trimming range possible via SD PLL	
H2.7	Trimming step	Δf_{X_step}		1	4	ppm	see also step size of SD PLL	■
H3	Clock output frequency at PPx pin	f_{clock_out}	11		5.5M	Hz	10pF load	
H4	Crystal oscillator settling time (switching from Low Power to High Precision Mode)	$t_{COSCsettle}$	292	292	292	µs		■
H5	Start up time	t_{start_up}		0.45	1	ms	crystal type: NDK NX5032SD; See also BOM for ext. load caps; Note: No SPI communication is allowed before XOSC start-up is finished and chip reset is already finished	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Digital Inputs/Outputs Characteristics								
I1	High level input voltage	V_{In_High}	0.7* VDDD		VDD5V +0.1	V		
I2	High level input leakage current	I_{In_High}			5	µA		
I3	Low level input voltage (except P_ON pin)	V_{In_Low}	0		0.8	V		
I4	Low level input voltage (at P_ON pin)	$V_{In\_Low\_PON}$	0		0.5	V		
I5	Low level input leakage current	I_{In_Low}	-5			µA		
I6	High level output voltage 1	V_{Out_High1}	VDD5V -0.4		VDD5V	V	IOH=-500 µA, static driver capability; Normal Pad Mode (see register PPCFG2 and CMC0)	
I7	Low level output voltage 1	V_{Out_Low1}	0		0.4	V	IOL=500 µA, static driver capability; Normal Pad Mode (see register PPCFG2 and CMC0)	
I8	High level output voltage 2	V_{Out_High2}	VDD5V -0.8		VDD5V	V	IOH=-4 mA, static driver capability; High Power Pad Mode (see register PPCFG2 and CMC0)	
I9	Low level output voltage 2	V_{Out_Low2}	0		0.8	V	IOL=4 mA, static driver capability; High Power Pad Mode (see register PPCFG2 and CMC0)	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Timing SPI-Bus Characteristics								
J1	Clock frequency	f_{clock}			2.2	MHz	Note: A high SPI clock rate during data reception can reduce sensitivity	
J2	Clock High time	t_{CLK_H}	200			ns		■
J3	Clock Low time	t_{CLK_L}	200			ns		■
J4	Active setup time	t_{setup}	200			ns		■
J5	Not active setup time	t_{not_setup}	200			ns		■
J6	Active hold time	t_{hold}	200			ns		■
J7	Not active hold time	t_{not_hold}	200			ns		■
J8	Deselect time	$t_{Deselect}$	200			ns		■
J9	SDI setup time	t_{SDI_setup}	100			ns		■
J10	SDI hold time	t_{SDI_hold}	100			ns		■
J11	Clock low to SDO valid	t_{CLK_SDO}			145	ns	@ C_{load} = 80 pF High Power Pad not enabled (Normal Mode) (see register PPCFG2 and CMC0)	■
J12	Clock low to SDO valid	t_{CLK_SDO}			40	ns	@ C_{load} = 10 pF High Power Pad not enabled (Normal Mode) (see register PPCFG2 and CMC0)	
J13	SDO rise time	t_{SDO_r}			90	ns	@ C_{load} = 80 pF	■
J14	SDO fall time	t_{SDO_f}			90	ns	@ C_{load} = 80 pF	■
J15	SDO rise time	t_{SDO_r}			15	ns	@ C_{load} = 10 pF	■
J16	SDO fall time	t_{SDO_f}			15	ns	@ C_{load} = 10 pF	■
J17	SDO disable time	$t_{SDO\_disable}$			25	ns		■

1) Please note that the system bandwidth is smaller than the smallest bandwidth in the signal path.

Unless explicitly otherwise noted, the following test conditions apply to the given specification values in the items D7 and D8:

* Hardware: TDA5240 Platform Testboard V1.0
* Single-Ended Matching for 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz
* RF input matched to 50 Ω; Insertion loss of input matching network = 1dB
* Receive Frequency 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz; Lo-Side LO-Injection
* Reference Clock: XTAL=21.948717 MHz

* IF-Gain: Attenuation set to default value (IFATT = 7)
* Double Down Conversion
* 1 IF-Filter: Center=10.7MHz; BW=330kHz; Connected between IF_OUT and IFBUF_IN
* 2nd IF Filter BW: Depending on Data Rate and FSK Deviation
* Received Signal at zero Offset to IF Center Frequency
* RSSI trimmed
* FSK Pre-Demodulation Filter (PDF) BW: Depending on Data Rate and FSK Deviation
* No SPI-traffic during telegram reception, CLK_OUT disabled
* AFC and AGC are OFF, unless otherwise noted

BER sensitivity measurements use Receive Mode TMMF (sampled with ideal data clock)

* DRE ... Data Date Error of received telegram vs. adjusted Data Rate
* DC ... Duty Cycle
* BER ... Bit Error Rate (using a PRBS9 Pseudo-Random Binary Sequence)
  [BER = 1 - (number_of_correctly_received_bits / number_of_transmitted bits)]

Table 10 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 300 k PDF = 282 k	ASK	-	3 dB	230	230	230	230	230	-
			6 dB	280	280	280	280	280	-
	FSK	0.5 k	3 dB	160	150	-	-	-	-
			6 dB	230	220	-	-	-	-
		1 k	3 dB	140	160	-	-	-	-
			6 dB	220	230	-	-	-	-
		5 k	3 dB	120	130	150	140	-	-
			6 dB	200	210	220	220	-	-
		10 k	3 dB	120	120	140	140	150	-
			6 dB	180	190	210	210	210	-
		15 k	3 dB	-	-	130	140	150	-
			6 dB	-	-	200	200	210	-
		20 k	3 dB	110	-	130	130	140	-
			6 dB	160	-	190	190	190	-
		40 k	3 dB	-	-	-	120	-	-
			6 dB	-	-	-	160	-	-
		50 k	3 dB	110	110	110	110	100	100
			6 dB	140	140	140	140	140	140

Table 10 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 200 k PDF = 239 k	ASK	-	3 dB	180	180	180	180	180	-
			6 dB	220	220	220	220	220	-
	FSK	0.5 k	3 dB	140	140	-	-	-	-
			6 dB	190	190	-	-	-	-
		1 k	3 dB	130	130	-	-	-	-
			6 dB	180	190	-	-	-	-
		5 k	3 dB	100	120	130	130	-	-
			6 dB	160	170	180	180	-	-
		10 k	3 dB	100	100	120	120	140	-
			6 dB	140	150	170	170	170	-
		15 k	3 dB	-	-	110	110	120	-
			6 dB	-	-	150	150	160	-
		20 k	3 dB	90	-	100	100	110	-
			6 dB	130	-	140	150	150	-
		40 k	3 dB	-	-	-	90	-	-
			6 dB	-	-	-	120	-	-
		50 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-

Table 10 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 125 k PDF = 132 k	ASK	-	3 dB	120	120	120	120	120	-
			6 dB	150	150	150	150	150	-
	FSK	0.5 k	3 dB	100	100	-	-	-	-
			6 dB	120	120	-	-	-	-
		1 k	3 dB	90	100	-	-	-	-
			6 dB	120	120	-	-	-	-
		5 k	3 dB	70	80	80	90	-	-
			6 dB	100	110	110	110	-	-
		10 k	3 dB	70	70	80	80	80	-
			6 dB	90	100	100	100	100	-
		15 k	3 dB	-	-	70	80	80	-
			6 dB	-	-	90	90	100	-
		20 k	3 dB	60	-	70	70	70	-
			6 dB	80	-	90	90	90	-
		40 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-
		50 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-

4.2 Test Circuit - Evaluation Board v1.0

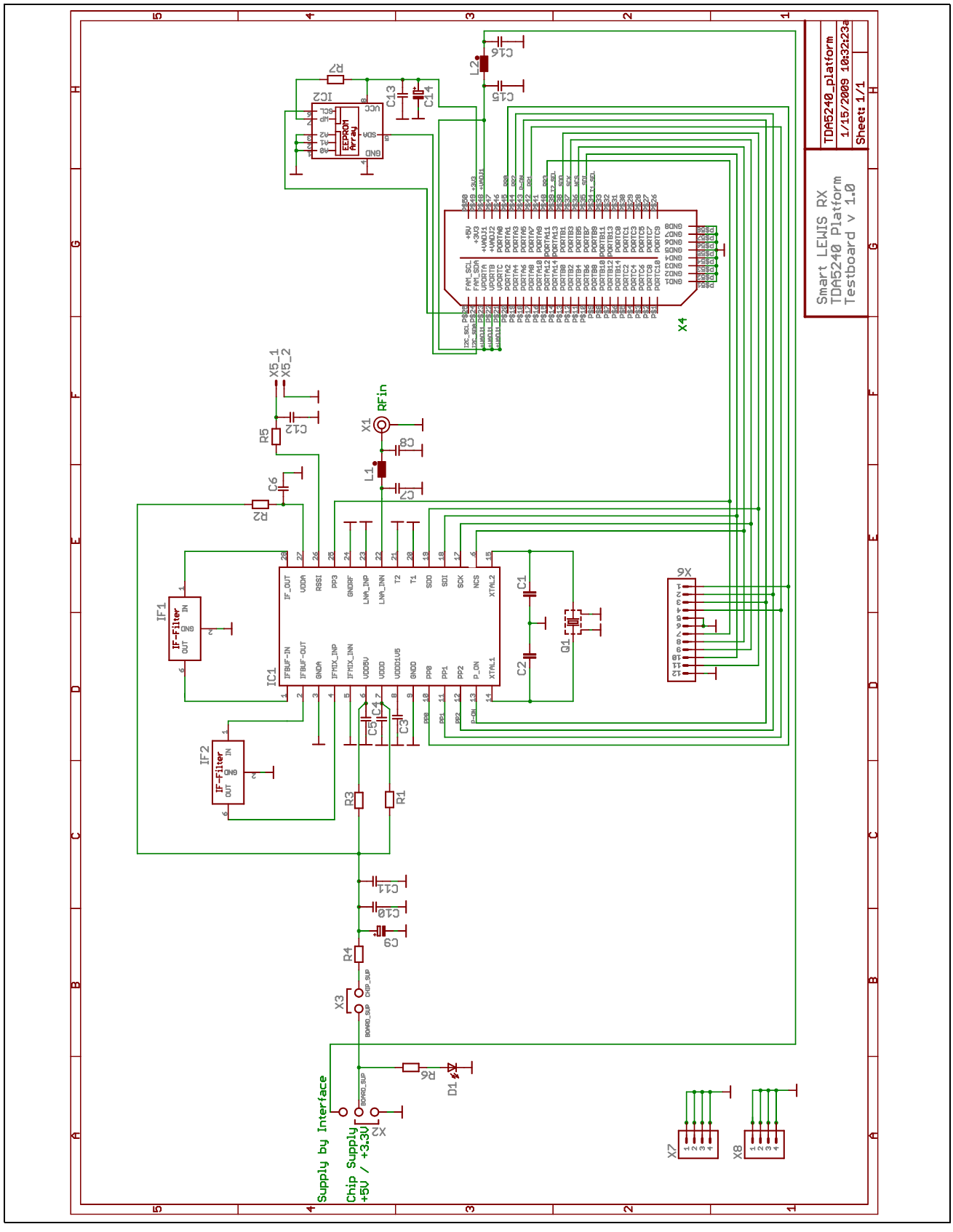


Figure 54 Test Circuit Schematic

4.3 Test Board Layout - Evaluation Board v1.0

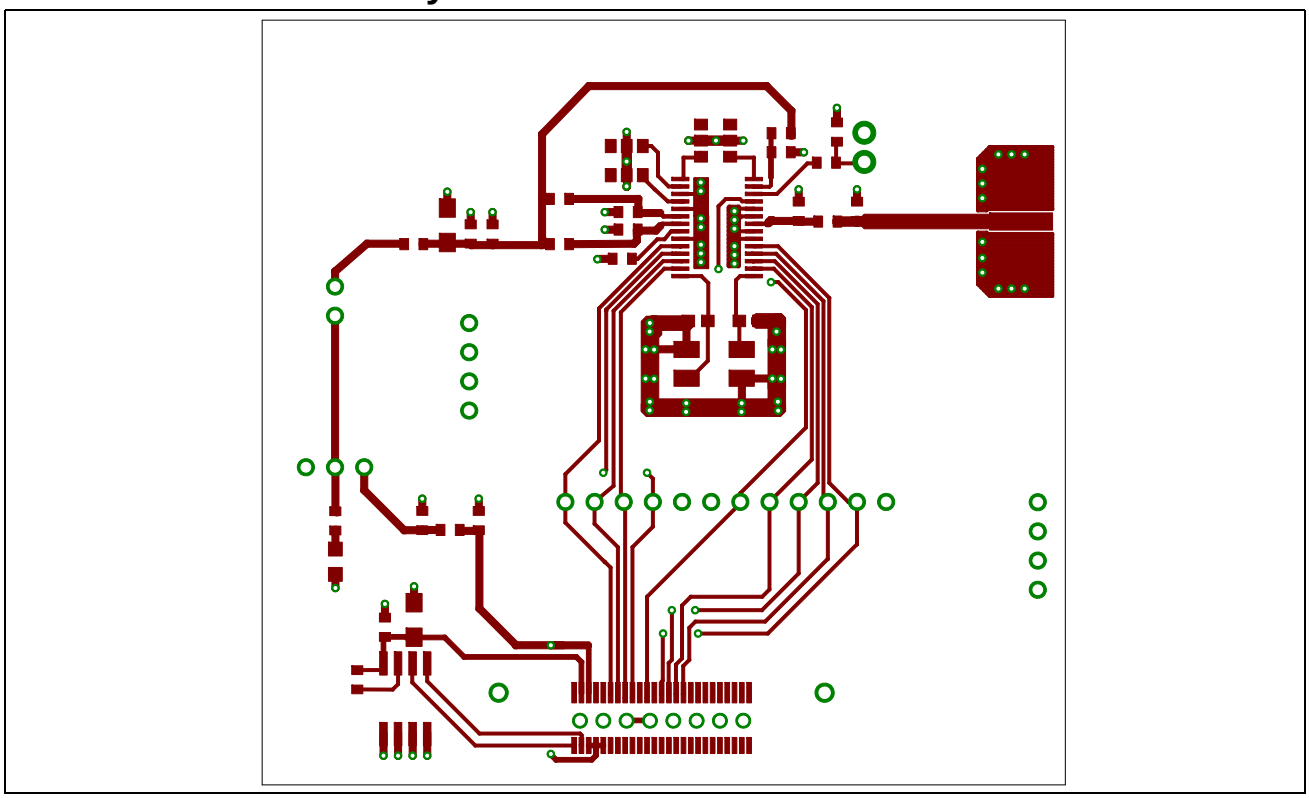


Figure 55 Test Board Layout, Top View

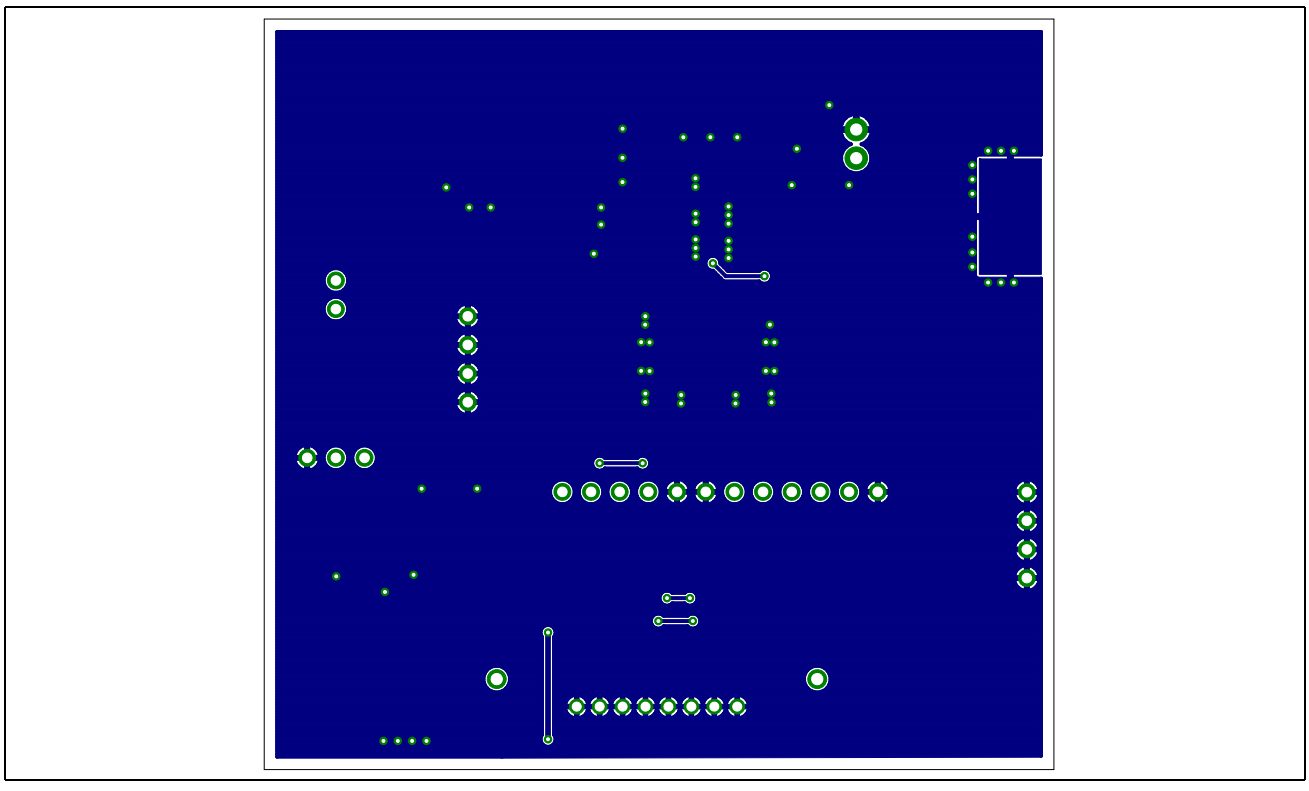


Figure 56 Test Board Layout, Bottom View

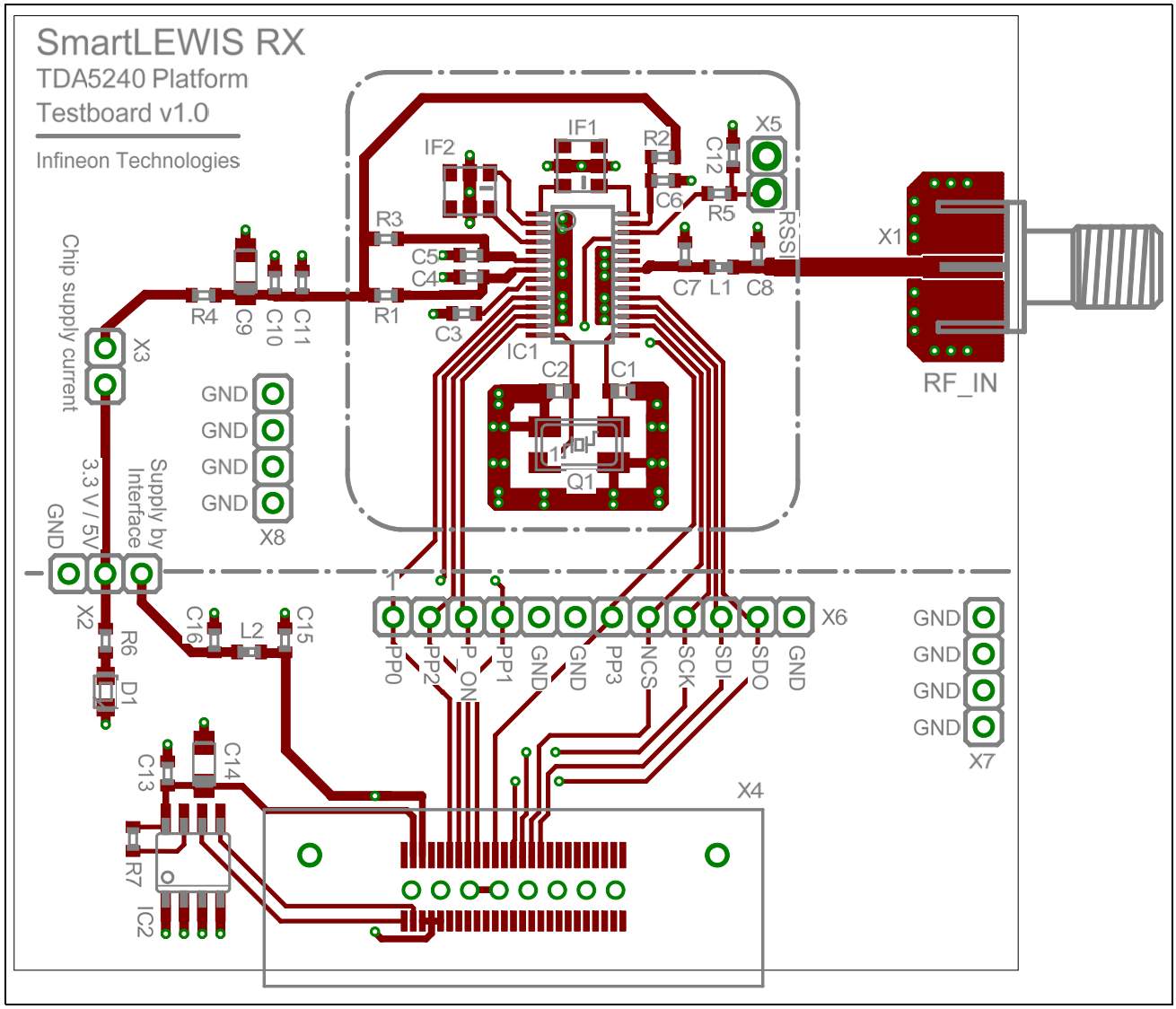


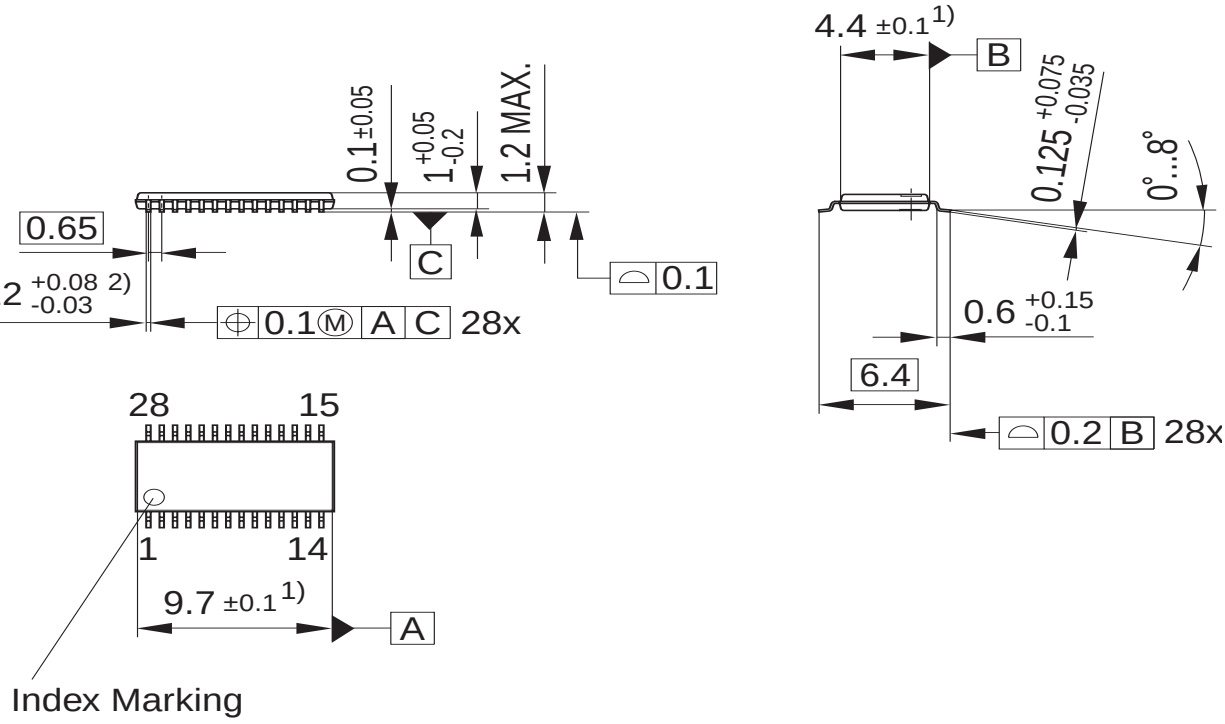
Figure 57 Test Board Layout, Component View

4.4 Bill of Materials

Pos	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark/Options (RF+supply variant)
1	IC1	TDA5225	PG-TSSOP-28			Infineon	
2	C1	3.9 pF	0603	C0G	+/- 0.1 pF		crystal oscillator load
3	C2	3.9 pF	0603	C0G	+/- 0.1 pF		crystal oscillator load
4	C3	100 nF	0603	X7R	+/- 10 %		
5	C4	100 nF	0603	X7R	+/- 10 %		
6	C5	100 nF / (1 µF)	0603	X7R / X5R	+/- 10 %		3.3V / (5 V environment)
7	C6	100 nF	0603	X7R	+/- 10 %		
8	C7	1 pF	0603	C0G	+/- 0.1 pF		matching for 315MHz
		0.5 pF	0603	C0G	+/- 0.1 pF		matching for 434MHz
		open	0603	C0G			matching for 868MHz
		1 pF	0603	C0G	+/- 0.1 pF		matching for 915MHz
9	C8	open	0603	C0G			matching for 315MHz
		open	0603	C0G			matching for 434MHz
		2.7 pF	0603	C0G	+/- 0.1 pF		matching for 868MHz
		5.1 pF	0603	C0G	+/- 0.1 pF		matching for 915MHz
10	C9	1 µF	SMC-A	Tantal	+/- 10%		polarized capacitor
11	C10	100 nF	0603	X7R	+/- 10%		
12	C11	10 nF	0603	X7R	+/- 10%		
13	L1	68 nH	0603		+/- 2%		matching for 315MHz
		39 nH	0603		+/- 2%		matching for 434MHz
		22 nH	0603		+/- 2%		matching for 868MHz
		15 nH	0603		+/- 2%		matching for 915MHz
14	R1	10 Ohm / (open)	0603		+/- 5%		3.3 V / (5 V environment)
15	R2	4.7 Ohm / (open)	0603		+/- 5%		3.3 V / (5 V environment)
16	R3	4.7 Ohm / (22 Ohm)	0603		+/- 5%		3.3 V / (5 V environment)
17	R4	0 Ohm	0603				
18	IF1	SFECF10 M7EA00				Murata	BW = 330 kHz
19	Q1	21.948717 MHz	NX5032SD	C0=1.7 pF C1=7 fF CL=12 pF		NDK (Frischer Electronic), EXS00A-CS01580	SMD crystal

Pos	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark/Options (RF+supply variant)
Interface / optional							
20	IC2	AT24C32 C-SH-B or AT24C512	SOIC8				EEPROM for board detection
21	C12	open	0603	X7R	+/- 10%		RSSI measurement low pass
22	C13	100 nF	0603	X7R	+/- 10%		
23	C14	1 µF	SMC-A	Tantal	+/- 10%		polarized capacitor
24	C15	10 nF	0603	X7R	+/- 10%		filter network on supply line
25	C16	10 nF	0603	X7R	+/- 10%		filter network on supply line
26	L2	0 Ohm	0603				no filter network on supply line
27	R5	open	0603				RSSI measurement low pass
28	R6	1 kOhm	0603				
29	R7	0 Ohm	0603				write protection for EEPROM
30	D1	LED		LS M676-P251-1			status indication LED
31	IF2	open				Murata	2nd IF filter is optional
32	X1	SMA socket					RF input
33	X2	3 pins					Board supply
34	X3	2 pins					Chip supply current (jumper closed)
35	X4	50 pins	SIB-QTS-025-01-X-D-RA			Samtec	Connector to PC/µC/Interface
36	X5	2 pins					RSSI measuring point
37	X6	12 pins					Interface line measuring point
38	X7	4 pins					GND
39	X8	4 pins					GND
40	Jumper 1	2 pins					Jumper for X3
41	Jumper 2	2 pins					Jumper for X2 - Supply by interface
Board material 1.5mm FR4 with 35µm copper on both sides							

5 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 58 PG-TSSOP-28 Package Outline (green package)

Table 11 Order Information

Type	Ordering Code	Package
TDA5225	SP000507672	PG-TSSOP-28

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”:**http://www.infineon.com/products**

SMD = Surface Mounted Device

Dimensions in mm

List of Tables

List of Figures

Appendix - Registers Chapter

Appendix - Registers Chapter

Register Overview

Table 1 Register Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Appendix - Registers Chapter, Register Description			
A_IF1	IF1 Register	016_H	122
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	122
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	123
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	123
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	124
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	124
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	124
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	125
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	125
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	126
A_WULOT	Wake-up on Level Observation Time Register	025_H	126
A_AFCLIMIT	AFC Limit Configuration Register	$02A_H$	127
A_AFCAGCD	AFC/AGC Freeze Delay Register	$02B_H$	127
A_AFCSFCFG	AFC Start/Freeze Configuration Register	$02C_H$	128
A_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$02D_H$	129
A_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$02E_H$	129
A_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$02F_H$	129
A_AFCK2CFG1	AFC Integrator 2 Gain Register 1	030_H	130
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	031_H	130
A_AGCSFCFG	AGC Start/Freeze Configuration Register	032_H	131
A_AGCCFG0	AGC Configuration Register 0	033_H	132
A_AGCCFG1	AGC Configuration Register 1	034_H	133
A_AGCTHR	AGC Threshold Register	035_H	133
A_DIGRXC	Digital Receiver Configuration Register	036_H	134
A_ISUPFCSEL	Image Supression Fc Selection Register	038_H	134
A_PDECF	Pre Decimation Factor Register	039_H	135
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03A_H$	135
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03B_H$	136

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_MFC	Matched Filter Control Register	$03C_H$	136
A_SRC	Sampe Rate Converter NCO Tune	$03D_H$	137
A_EXTSLC	Externel Data Slicer Configuration	$03E_H$	137
A_CHCFG	Channel Configuration Register	058_H	138
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	059_H	139
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$05A_H$	139
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$05B_H$	140
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$05C_H$	140
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$05D_H$	141
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$05E_H$	141
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$05F_H$	142
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	060_H	142
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	061_H	143
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	062_H	143
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	063_H	143
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	064_H	144
SFRPAGE	Special Function Register Page Register	080_H	144
PPCFG0	PP0 and PP1 Configuration Register	081_H	145
PPCFG1	PP2 and PP3 Configuration Register	082_H	146
PPCFG2	PPx Port Configuration Register	083_H	147
RXRUNCFG0	RX RUN Configuration Register 0	084_H	148
RXRUNCFG1	RX RUN Configuration Register 1	085_H	149
CLKOUT0	Clock Divider Register 0	086_H	150
CLKOUT1	Clock Divider Register 1	087_H	150
CLKOUT2	Clock Divider Register 2	088_H	151
RFC	RF Control Register	089_H	151
BPFCALCFG0	BPF Calibration Configuration Register 0	$08A_H$	152
BPFCALCFG1	BPF Calibration Configuration Register 1	$08B_H$	152
XTALCAL0	XTAL Coarse Calibration Register	$08C_H$	153
XTALCAL1	XTAL Fine Calibration Register	$08D_H$	153
RSSIMONC	RSSI Monitor Configuration Register	$08E_H$	154
ADCINSEL	ADC Input Selection Register	$08F_H$	155
RSSIOFFS	RSSI Offset Register	090_H	155
RSSISLOPE	RSSI Slope Register	091_H	156
IM0	Interrupt Mask Register 0	094_H	156
IM1	Interrupt Mask Register 1	095_H	157
SPMAP	Self Polling Mode Active Periods Register	096_H	157
SPMIP	Self Polling Mode Idle Periods Register	097_H	158

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
SPMC	Self Polling Mode Control Register	098_H	158
SPMRT	Self Polling Mode Reference Timer Register	099_H	159
SPMOFFT0	Self Polling Mode Off Time Register 0	$09A_H$	159
SPMOFFT1	Self Polling Mode Off Time Register 1	$09B_H$	160
SPMONTA0	Self Polling Mode On Time Config A Register 0	$09C_H$	160
SPMONTA1	Self Polling Mode On Time Config A Register 1	$09D_H$	161
SPMONTB0	Self Polling Mode On Time Config B Register 0	$09E_H$	161
SPMONTB1	Self Polling Mode On Time Config B Register 1	$09F_H$	162
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0A0_H$	162
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0A1_H$	163
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0A2_H$	163
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0A3_H$	164
EXTPCMD	External Processing Command Register	$0A4_H$	164
CMC1	Chip Mode Control Register 1	$0A5_H$	165
CMC0	Chip Mode Control Register 0	$0A6_H$	166
RSSIPWU	Wakeup Peak Detector Readout Register	$0A7_H$	167
IS0	Interrupt Status Register 0	$0A8_H$	167
IS1	Interrupt Status Register 1	$0A9_H$	168
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0AA_H$	169
RSSIPRX	RSSI Peak Detector Readout Register	$0AB_H$	169
ADCRESH	ADC Result High Byte Register	$0AE_H$	170
ADCRESL	ADC Result Low Byte Register	$0AF_H$	170
VACRES	VCO Autocalibration Result Readout Register	$0B0_H$	171
AFCOFFSET	AFC Offset Read Register	$0B1_H$	171
AGCGAINR	AGC Gain Readout Register	$0B2_H$	172
SPIAT	SPI Address Tracer Register	$0B3_H$	172
SPIDT	SPI Data Tracer Register	$0B4_H$	172
SPICHKSUM	SPI Checksum Register	$0B5_H$	173
SN0	Serial Number Register 0	$0B6_H$	173
SN1	Serial Number Register 1	$0B7_H$	174
SN2	Serial Number Register 2	$0B8_H$	174
SN3	Serial Number Register 3	$0B9_H$	174
RSSIRX	RSSI Readout Register	$0BA_H$	175
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0BB_H$	175
B_IF1	IF1 Register	116_H	
B_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$11B_H$	
B_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$11C_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
B_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$11D_H$	
B_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$11E_H$	
B_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$11F_H$	
B_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	120_H	
B_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	121_H	
B_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	122_H	
B_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	123_H	
B_WULOT	Wake-Up on Level Observation Time Register	125_H	
B_AFCLIMIT	AFC Limit Configuration Register	$12A_H$	
B_AFCAGCD	AFC/AGC Freeze Delay Register	$12B_H$	
B_AFCSFCFG	AFC Start/Freeze Configuration Register	$12C_H$	
B_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$12D_H$	
B_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$12E_H$	
B_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$12F_H$	
B_AFCK2CFG1	AFC Integrator 2 Gain Register 1	130_H	
B_PMFUDSF	Peak Memory Filter Up-Down Factor Register	131_H	
B_AGCSFCFG	AGC Start/Freeze Configuration Register	132_H	
B_AGCCFG0	AGC Configuration Register 0	133_H	
B_AGCCFG1	AGC Configuration Register 1	134_H	
B_AGCTHR	AGC Threshold Register	135_H	
B_DIGRXC	Digital Receiver Configuration Register	136_H	
B_ISUPFCSEL	Image Supression Fc Selection Register	138_H	
B_PDECF	Pre Decimation Factor Register	139_H	
B_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$13A_H$	
B_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$13B_H$	
B_MFC	Matched Filter Control Register	$13C_H$	
B_SRC	Sampe Rate Converter NCO Tune	$13D_H$	
B_EXTSLC	Externel Data Slicer Configuration	$13E_H$	
B_CHCFG	Channel Configuration Register	158_H	
B_PLLINTC1	PLL MMD Integer Value Register Channel 1	159_H	
B_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$15A_H$	
B_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$15B_H$	
B_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$15C_H$	
B_PLLINTC2	PLL MMD Integer Value Register Channel 2	$15D_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
B_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$15E_H$	
B_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$15F_H$	
B_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	160_H	
B_PLLINTC3	PLL MMD Integer Value Register Channel 3	161_H	
B_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	162_H	
B_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	163_H	
B_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	164_H	
C_IF1	IF1 Register	216_H	
C_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$21B_H$	
C_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$21C_H$	
C_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$21D_H$	
C_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$21E_H$	
C_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$21F_H$	
C_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	220_H	
C_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	221_H	
C_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	222_H	
C_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	223_H	
C_WULOT	Wake-Up on Level Observation Time Register	225_H	
C_AFCLIMIT	AFC Limit Configuration Register	$22A_H$	
C_AFCAGCD	AFC/AGC Freeze Delay Register	$22B_H$	
C_AFCSFCFG	AFC Start/Freeze Configuration Register	$22C_H$	
C_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$22D_H$	
C_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$22E_H$	
C_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$22F_H$	
C_AFCK2CFG1	AFC Integrator 2 Gain Register 1	230_H	
C_PMFUDSF	Peak Memory Filter Up-Down Factor Register	231_H	
C_AGCSFCFG	AGC Start/Freeze Configuration Register	232_H	
C_AGCCFG0	AGC Configuration Register 0	233_H	
C_AGCCFG1	AGC Configuration Register 1	234_H	
C_AGCTHR	AGC Threshold Register	235_H	
C_DIGRXC	Digital Receiver Configuration Register	236_H	
C_ISUPFCSEL	Image Supression Fc Selection Register	238_H	
C_PDECF	Pre Decimation Factor Register	239_H	
C_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$23A_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
C_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$23B_H$	
C_MFC	Matched Filter Control Register	$23C_H$	
C_SRC	Sampe Rate Converter NCO Tune	$23D_H$	
C_EXTSLC	Externel Data Slicer Configuration	$23E_H$	
C_CHCFG	Channel Configuration Register	258_H	
C_PLLINTC1	PLL MMD Integer Value Register Channel 1	259_H	
C_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$25A_H$	
C_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$25B_H$	
C_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$25C_H$	
C_PLLINTC2	PLL MMD Integer Value Register Channel 2	$25D_H$	
C_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$25E_H$	
C_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$25F_H$	
C_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	260_H	
C_PLLINTC3	PLL MMD Integer Value Register Channel 3	261_H	
C_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	262_H	
C_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	263_H	
C_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	264_H	
D_IF1	IF1 Register	316_H	
D_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$31B_H$	
D_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$31C_H$	
D_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$31D_H$	
D_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$31E_H$	
D_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$31F_H$	
D_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	320_H	
D_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	321_H	
D_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	322_H	
D_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	323_H	
D_WULOT	Wake-Up on Level Observation Time Register	325_H	
D_AFCLIMIT	AFC Limit Configuration Register	$32A_H$	
D_AFCAGCD	AFC/AGC Freeze Delay Register	$32B_H$	
D_AFCSFCFG	AFC Start/Freeze Configuration Register	$32C_H$	
D_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$32D_H$	
D_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$32E_H$	
D_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$32F_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
D_AFCK2CFG1	AFC Integrator 2 Gain Register 1	330_H	
D_PMFUDSF	Peak Memory Filter Up-Down Factor Register	331_H	
D_AGCSFCFG	AGC Start/Freeze Configuration Register	332_H	
D_AGCCFG0	AGC Configuration Register 0	333_H	
D_AGCCFG1	AGC Configuration Register 1	334_H	
D_AGCTHR	AGC Threshold Register	335_H	
D_DIGRXC	Digital Receiver Configuration Register	336_H	
D_ISUPFCSEL	Image Supression Fc Selection Register	338_H	
D_PDECF	Pre Decimation Factor Register	339_H	
D_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$33A_H$	
D_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$33B_H$	
D_MFC	Matched Filter Control Register	$33C_H$	
D_SRC	Sampe Rate Converter NCO Tune	$33D_H$	
D_EXTSLC	Externel Data Slicer Configuration	$33E_H$	
D_CHCFG	Channel Configuration Register	358_H	
D_PLLINTC1	PLL MMD Integer Value Register Channel 1	359_H	
D_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$35A_H$	
D_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$35B_H$	
D_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$35C_H$	
D_PLLINTC2	PLL MMD Integer Value Register Channel 2	$35D_H$	
D_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$35E_H$	
D_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$35F_H$	
D_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	360_H	
D_PLLINTC3	PLL MMD Integer Value Register Channel 3	361_H	
D_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	362_H	
D_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	363_H	
D_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	364_H	

Table 2 Register Overview and Reset Value

Register Short Name	Register Long Name	Offset Address	Reset Value
Appendix - Registers Chapter, Register Description			
A_IF1	IF1 Register	016_H	20_H
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	00_H
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	FF_H
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	00_H
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	FF_H
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	00_H
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	00_H
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	FF_H
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	00_H
A_WULOT	Wake-up on Level Observation Time Register	025_H	00_H
A_AFCLIMIT	AFC Limit Configuration Register	$02A_H$	02_H
A_AFCAGCD	AFC/AGC Freeze Delay Register	$02B_H$	00_H
A_AFCSFCFG	AFC Start/Freeze Configuration Register	$02C_H$	00_H
A_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$02D_H$	00_H
A_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$02E_H$	00_H
A_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$02F_H$	00_H
A_AFCK2CFG1	AFC Integrator 2 Gain Register 1	030_H	00_H
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	031_H	42_H
A_AGCSFCFG	AGC Start/Freeze Configuration Register	032_H	00_H
A_AGCCFG0	AGC Configuration Register 0	033_H	$2B_H$
A_AGCCFG1	AGC Configuration Register 1	034_H	03_H
A_AGCTHR	AGC Threshold Register	035_H	08_H
A_DIGRXC	Digital Receiver Configuration Register	036_H	40_H
A_ISUPFCSEL	Image Supression Fc Selection Register	038_H	07_H
A_PDECF	Pre Decimation Factor Register	039_H	00_H
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03A_H$	00_H
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03B_H$	20_H
A_MFC	Matched Filter Control Register	$03C_H$	07_H
A_SRC	Sampe Rate Converter NCO Tune	$03D_H$	00_H
A_EXTSLC	Externel Data Slicer Configuration	$03E_H$	02_H
A_CHCFG	Channel Configuration Register	058_H	44_H
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	059_H	93_H
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$05A_H$	$F3_H$
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$05B_H$	07_H
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$05C_H$	09_H
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$05D_H$	13_H
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$05E_H$	$F3_H$
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$05F_H$	07_H
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	060_H	09_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	061_H	13_H
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	062_H	$F3_H$
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	063_H	07_H
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	064_H	09_H
SFRPAGE	Special Function Register Page Register	080_H	00_H
PPCFG0	PP0 and PP1 Configuration Register	081_H	50_H
PPCFG1	PP2 and PP3 Configuration Register	082_H	12_H
PPCFG2	PPx Port Configuration Register	083_H	00_H
RXRUNCFG0	RX RUN Configuration Register 0	084_H	FF_H
RXRUNCFG1	RX RUN Configuration Register 1	085_H	FF_H
CLKOUT0	Clock Divider Register 0	086_H	$0B_H$
CLKOUT1	Clock Divider Register 1	087_H	00_H
CLKOUT2	Clock Divider Register 2	088_H	00_H
RFC	RF Control Register	089_H	07_H
BPFCALCFG0	BPF Calibration Configuration Register 0	$08A_H$	07_H
BPFCALCFG1	BPF Calibration Configuration Register 1	$08B_H$	04_H
XTALCAL0	XTAL Coarse Calibration Register	$08C_H$	10_H
XTALCAL1	XTAL Fine Calibration Register	$08D_H$	00_H
RSSIMONC	RSSI Monitor Configuration Register	$08E_H$	01_H
ADCINSEL	ADC Input Selection Register	$08F_H$	00_H
RSSIOFFS	RSSI Offset Register	090_H	80_H
RSSISLOPE	RSSI Slope Register	091_H	80_H
IM0	Interrupt Mask Register 0	094_H	00_H
IM1	Interrupt Mask Register 1	095_H	00_H
SPMAP	Self Polling Mode Active Periods Register	096_H	01_H
SPMIP	Self Polling Mode Idle Periods Register	097_H	01_H
SPMC	Self Polling Mode Control Register	098_H	00_H
SPMRT	Self Polling Mode Reference Timer Register	099_H	01_H
SPMOFFT0	Self Polling Mode Off Time Register 0	$09A_H$	01_H
SPMOFFT1	Self Polling Mode Off Time Register 1	$09B_H$	00_H
SPMONTA0	Self Polling Mode On Time Config A Register 0	$09C_H$	01_H
SPMONTA1	Self Polling Mode On Time Config A Register 1	$09D_H$	00_H
SPMONTB0	Self Polling Mode On Time Config B Register 0	$09E_H$	01_H
SPMONTB1	Self Polling Mode On Time Config B Register 1	$09F_H$	00_H
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0A0_H$	01_H
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0A1_H$	00_H
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0A2_H$	01_H
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0A3_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
EXTPCMD	External Processing Command Register	$0A4_H$	00_H
CMC1	Chip Mode Control Register 1	$0A5_H$	04_H
CMC0	Chip Mode Control Register 0	$0A6_H$	10_H
RSSIPWU	Wakeup Peak Detector Readout Register	$0A7_H$	00_H
IS0	Interrupt Status Register 0	$0A8_H$	FF_H
IS1	Interrupt Status Register 1	$0A9_H$	FF_H
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0AA_H$	00_H
RSSIPRX	RSSI Peak Detector Readout Register	$0AB_H$	00_H
ADCRESH	ADC Result High Byte Register	$0AE_H$	00_H
ADCRESL	ADC Result Low Byte Register	$0AF_H$	00_H
VACRES	VCO Autocalibration Result Readout Register	$0B0_H$	00_H
AFCOFFSET	AFC Offset Read Register	$0B1_H$	00_H
AGCGAINR	AGC Gain Readout Register	$0B2_H$	00_H
SPIAT	SPI Address Tracer Register	$0B3_H$	00_H
SPIDT	SPI Data Tracer Register	$0B4_H$	00_H
SPICHKSUM	SPI Checksum Register	$0B5_H$	00_H
SN0	Serial Number Register 0	$0B6_H$	00_H
SN1	Serial Number Register 1	$0B7_H$	00_H
SN2	Serial Number Register 2	$0B8_H$	00_H
SN3	Serial Number Register 3	$0B9_H$	00_H
RSSIRX	RSSI Readout Register	$0BA_H$	00_H
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0BB_H$	00_H
B_IF1	IF1 Register	116_H	20_H
B_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$11B_H$	00_H
B_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$11C_H$	FF_H
B_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$11D_H$	00_H
B_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$11E_H$	00_H
B_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$11F_H$	FF_H
B_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	120_H	00_H
B_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	121_H	00_H
B_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	122_H	FF_H
B_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	123_H	00_H
B_WULOT	Wake-Up on Level Observation Time Register	125_H	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
B_AFCLIMIT	AFC Limit Configuration Register	$12A_H$	02_H
B_AFCAGCD	AFC/AGC Freeze Delay Register	$12B_H$	00_H
B_AFCSFCFG	AFC Start/Freeze Configuration Register	$12C_H$	00_H
B_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$12D_H$	00_H
B_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$12E_H$	00_H
B_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$12F_H$	00_H
B_AFCK2CFG1	AFC Integrator 2 Gain Register 1	130_H	00_H
B_PMFUDSF	Peak Memory Filter Up-Down Factor Register	131_H	42_H
B_AGCSFCFG	AGC Start/Freeze Configuration Register	132_H	00_H
B_AGCCFG0	AGC Configuration Register 0	133_H	$2B_H$
B_AGCCFG1	AGC Configuration Register 1	134_H	03_H
B_AGCTHR	AGC Threshold Register	135_H	08_H
B_DIGRXC	Digital Receiver Configuration Register	136_H	40_H
B_ISUPFCSEL	Image Supression Fc Selection Register	138_H	07_H
B_PDECF	Pre Decimation Factor Register	139_H	00_H
B_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$13A_H$	00_H
B_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$13B_H$	20_H
B_MFC	Matched Filter Control Register	$13C_H$	07_H
B_SRC	Sampe Rate Converter NCO Tune	$13D_H$	00_H
B_EXTSLC	Externel Data Slicer Configuration	$13E_H$	02_H
B_CHCFG	Channel Configuration Register	158_H	44_H
B_PLLINTC1	PLL MMD Integer Value Register Channel 1	159_H	93_H
B_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$15A_H$	$F3_H$
B_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$15B_H$	07_H
B_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$15C_H$	09_H
B_PLLINTC2	PLL MMD Integer Value Register Channel 2	$15D_H$	13_H
B_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$15E_H$	$F3_H$
B_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$15F_H$	07_H
B_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	160_H	09_H
B_PLLINTC3	PLL MMD Integer Value Register Channel 3	161_H	13_H
B_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	162_H	$F3_H$
B_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	163_H	07_H
B_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	164_H	09_H
C_IF1	IF1 Register	216_H	20_H
C_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$21B_H$	00_H
C_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$21C_H$	FF_H
C_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$21D_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
C_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$21E_H$	00_H
C_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$21F_H$	FF_H
C_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	220_H	00_H
C_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	221_H	00_H
C_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	222_H	FF_H
C_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	223_H	00_H
C_WULOT	Wake-Up on Level Observation Time Register	225_H	00_H
C_AFCLIMIT	AFC Limit Configuration Register	$22A_H$	02_H
C_AFCAGCD	AFC/AGC Freeze Delay Register	$22B_H$	00_H
C_AFCSFCFG	AFC Start/Freeze Configuration Register	$22C_H$	00_H
C_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$22D_H$	00_H
C_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$22E_H$	00_H
C_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$22F_H$	00_H
C_AFCK2CFG1	AFC Integrator 2 Gain Register 1	230_H	00_H
C_PMFUDSF	Peak Memory Filter Up-Down Factor Register	231_H	42_H
C_AGCSFCFG	AGC Start/Freeze Configuration Register	232_H	00_H
C_AGCCFG0	AGC Configuration Register 0	233_H	$2B_H$
C_AGCCFG1	AGC Configuration Register 1	234_H	03_H
C_AGCTHR	AGC Threshold Register	235_H	08_H
C_DIGRXC	Digital Receiver Configuration Register	236_H	40_H
C_ISUPFCSEL	Image Supression Fc Selection Register	238_H	07_H
C_PDECF	Pre Decimation Factor Register	239_H	00_H
C_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$23A_H$	00_H
C_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$23B_H$	20_H
C_MFC	Matched Filter Control Register	$23C_H$	07_H
C_SRC	Sampe Rate Converter NCO Tune	$23D_H$	00_H
C_EXTSLC	Externel Data Slicer Configuration	$23E_H$	02_H
C_CHCFG	Channel Configuration Register	258_H	44_H
C_PLLINTC1	PLL MMD Integer Value Register Channel 1	259_H	93_H
C_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$25A_H$	$F3_H$
C_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$25B_H$	07_H
C_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$25C_H$	09_H
C_PLLINTC2	PLL MMD Integer Value Register Channel 2	$25D_H$	13_H
C_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$25E_H$	$F3_H$
C_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$25F_H$	07_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
C_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	260_H	09_H
C_PLLINTC3	PLL MMD Integer Value Register Channel 3	261_H	13_H
C_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	262_H	$F3_H$
C_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	263_H	07_H
C_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	264_H	09_H
D_IF1	IF1 Register	316_H	20_H
D_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$31B_H$	00_H
D_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$31C_H$	FF_H
D_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$31D_H$	00_H
D_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$31E_H$	00_H
D_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$31F_H$	FF_H
D_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	320_H	00_H
D_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	321_H	00_H
D_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	322_H	FF_H
D_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	323_H	00_H
D_WULOT	Wake-Up on Level Observation Time Register	325_H	00_H
D_AFCLIMIT	AFC Limit Configuration Register	$32A_H$	02_H
D_AFCAGCD	AFC/AGC Freeze Delay Register	$32B_H$	00_H
D_AFCSFCFG	AFC Start/Freeze Configuration Register	$32C_H$	00_H
D_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$32D_H$	00_H
D_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$32E_H$	00_H
D_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$32F_H$	00_H
D_AFCK2CFG1	AFC Integrator 2 Gain Register 1	330_H	00_H
D_PMFUDSF	Peak Memory Filter Up-Down Factor Register	331_H	42_H
D_AGCSFCFG	AGC Start/Freeze Configuration Register	332_H	00_H
D_AGCCFG0	AGC Configuration Register 0	333_H	$2B_H$
D_AGCCFG1	AGC Configuration Register 1	334_H	03_H
D_AGCTHR	AGC Threshold Register	335_H	08_H
D_DIGRXC	Digital Receiver Configuration Register	336_H	40_H
D_ISUPFCSEL	Image Supression Fc Selection Register	338_H	07_H
D_PDECF	Pre Decimation Factor Register	339_H	00_H
D_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$33A_H$	00_H
D_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$33B_H$	20_H
D_MFC	Matched Filter Control Register	$33C_H$	07_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
D_SRC	Sampe Rate Converter NCO Tune	$33D_H$	00_H
D_EXTSLC	Externel Data Slicer Configuration	$33E_H$	02_H
D_CHCFG	Channel Configuration Register	358_H	44_H
D_PLLINTC1	PLL MMD Integer Value Register Channel 1	359_H	93_H
D_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$35A_H$	$F3_H$
D_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$35B_H$	07_H
D_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$35C_H$	09_H
D_PLLINTC2	PLL MMD Integer Value Register Channel 2	$35D_H$	13_H
D_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$35E_H$	$F3_H$
D_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$35F_H$	07_H
D_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	360_H	09_H
D_PLLINTC3	PLL MMD Integer Value Register Channel 3	361_H	13_H
D_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	362_H	$F3_H$
D_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	363_H	07_H
D_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	364_H	09_H

Register Description

IF1 Register

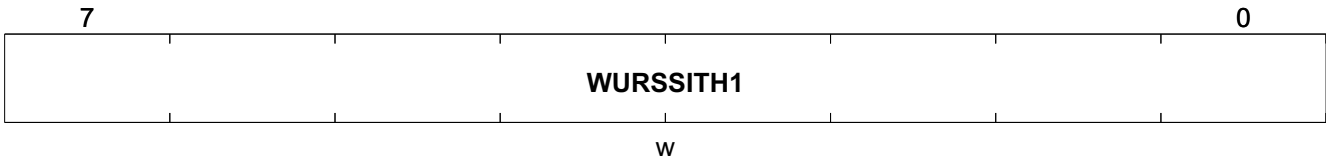
A_IF1	Offset	Reset Value
IF1 Register	016_H	20_H

7	6	5	3	2	1	0
UNUSED	SSBSEL	BPFBWSEL		SDCSEL	IFBUFEN	CERFSEL
-	w	w		w	w	w

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
SSBSEL	6	w	**RXRF Receive Side Band Select** 0_B RF = LO + IF1 (Lo-side LO-injection) 1_B RF = LO - IF1 (Hi-side LO-injection) Reset: 0_H
BPFBWSEL	5:3	w	**Band Pass Filter Bandwidth Selection** 000_B 50 kHz 001_B 80 kHz 010_B 125 kHz 011_B 200 kHz 100_B 300 kHz 101_B not used 110_B not used 111_B not used Reset: 4_H
SDCSEL	2	w	**Single / Double Conversion Selection** 0_B Double Conversion (10.7 MHz/274 kHz) 1_B Single Conversion (274 kHz) Reset: 0_H
IFBUFEN	1	w	**IF Buffer Enable** 0_B Disabled 1_B Enabled Reset: 0_H
CERFSEL	0	w	**Number of external Ceramic Filters** 0_B 1 Ceramic Filter 1_B 2 Ceramic Filters Reset: 0_H

RSSI Wake-Up Threshold for Channel 1 Register

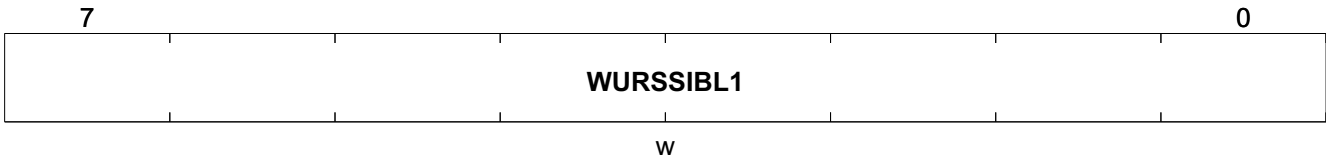
A_WURSSITH1	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	00_H



Field	Bits	Type	Description
WURSSITH1	7:0	w	**Wake Up on RSSI Threshold level for Channel 1** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 1 Register

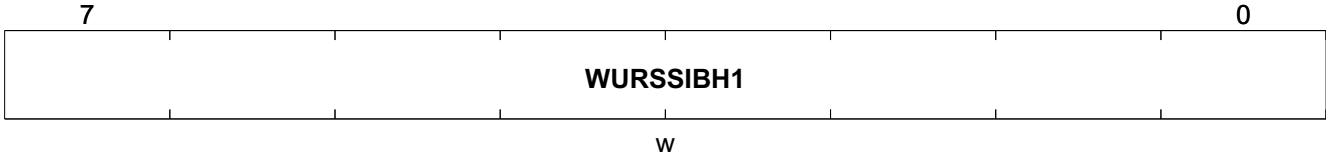
A_WURSSIBL1	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	FF_H



Field	Bits	Type	Description
WURSSIBL1	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 1** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 1 Register

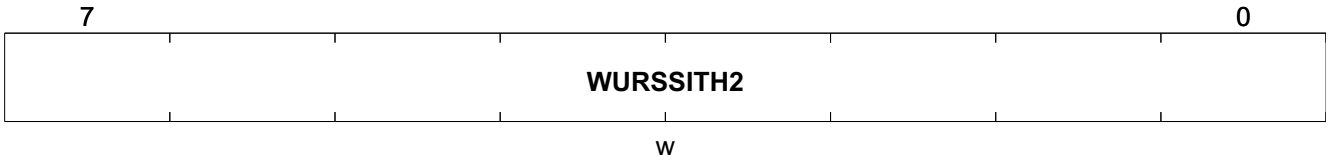
A_WURSSIBH1	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	00_H



Field	Bits	Type	Description
WURSSIBH1	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 1** Reset: 00_H

RSSI Wake-Up Threshold for Channel 2 Register

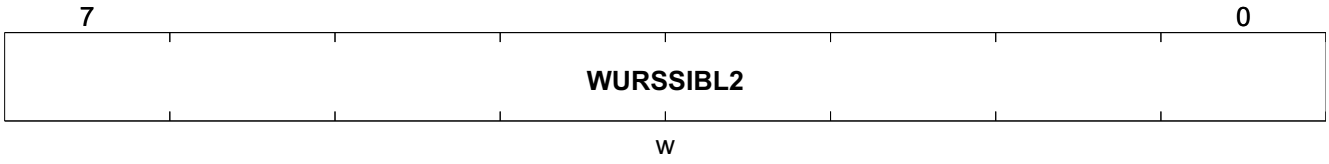
A_WURSSITH2	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 2 Register	**$01E_H$**	**00_H**



Field	Bits	Type	Description
WURSSITH2	7:0	w	**Wake Up on RSSI Threshold level for Channel 2** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 2 Register

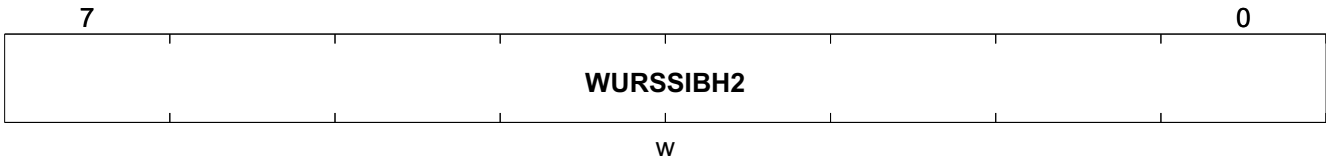
A_WURSSIBL2	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 2 Register	**$01F_H$**	**FF_H**



Field	Bits	Type	Description
WURSSIBL2	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 2** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 2 Register

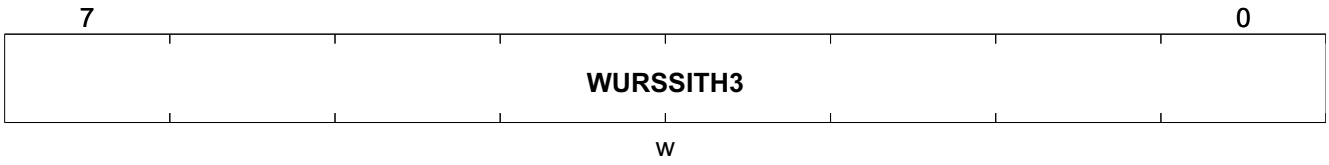
A_WURSSIBH2	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 2 Register	**020_H**	**00_H**



Field	Bits	Type	Description
WURSSIBH2	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 2** Reset: 00_H

RSSI Wake-Up Threshold for Channel 3 Register

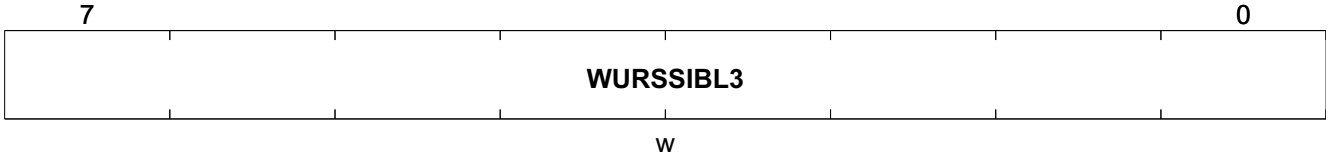
A_WURSSITH3	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 3 Register	**021_H**	**00_H**



Field	Bits	Type	Description
WURSSITH3	7:0	w	**Wake Up on RSSI Threshold level for Channel 3** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 3 Register

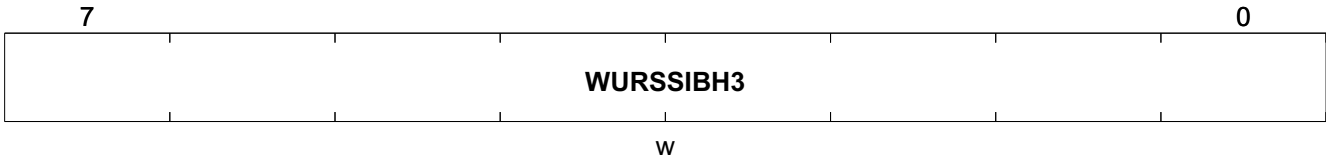
A_WURSSIBL3	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 3 Register	**022_H**	**FF_H**



Field	Bits	Type	Description
WURSSIBL3	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 3** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 3 Register

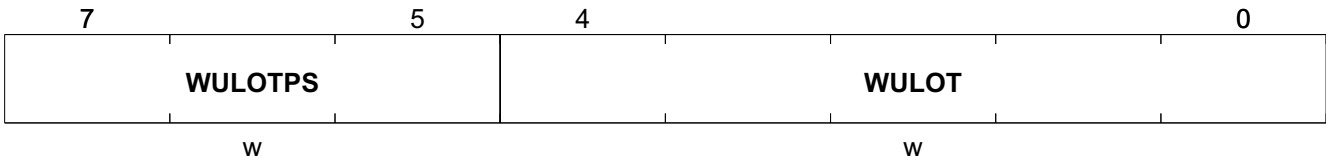
A_WURSSIBH3	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 3 Register	**023_H**	**00_H**



Field	Bits	Type	Description
WURSSIBH3	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 3** Reset: 00_H

Wake-up on Level Observation Time Register

A_WULOT	Offset	Reset Value
Wake-up on Level Observation Time Register	**025_H**	**00_H**

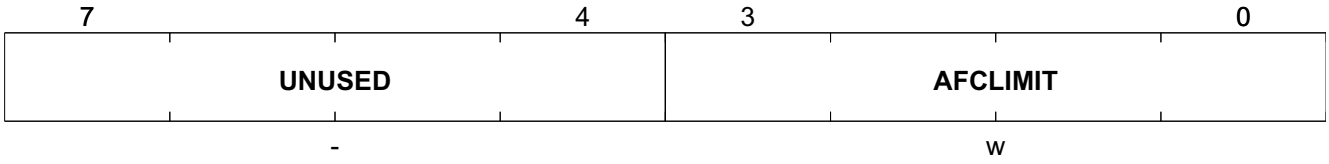


Field	Bits	Type	Description
WULOTPS	7:5	w	**Wake-Up Level Observation Time PreScaler** 000_B 4 001_B 8 010_B 16 011_B 32 100_B 64 101_B 128 110_B 256 111_B 512 Reset: 0_H

Field	Bits	Type	Description
WULOT	4:0	w	**Wake-Up Level Observation Time** Min. 01h : Twulot = 1 * WULOTPS * 64 / Fsys Max 1Fh : Twulot = 31 * WULOTPS * 64 / Fsys Value 00h : Twulot = 32 * WULOTPS * 64 / Fsys Reset: 00_H

AFC Limit Configuration Register

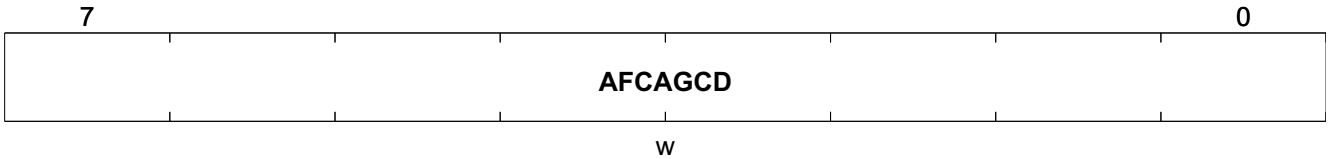
A_AFCLIMIT	Offset	Reset Value
AFC Limit Configuration Register	**$02A_H$**	**02_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCLIMIT	3:0	w	**AFC Frequency Offset Saturation Limit ==> 1...15 x 21.4 kHz** Min: 1h = +/- Fsys / 2^(22-12) Hz Max: Fh = +/- 15 * Fsys / 2^(22-12) Hz Reg. value 0h = 0 Hz - no AFC correction Reset: 2_H

AFC/AGC Freeze Delay Register

A_AFCAGCD	Offset	Reset Value
AFC/AGC Freeze Delay Register	**$02B_H$**	**00_H**



Field	Bits	Type	Description
AFCAGCD	7:0	w	**AFC/AGC Freeze Delay Counter Division Ratio** The base period for the delay counter is the 8-16 samples/chip (predecimation strobe) divided by 4 Reset: 00_H

AFC Start/Freeze Configuration Register

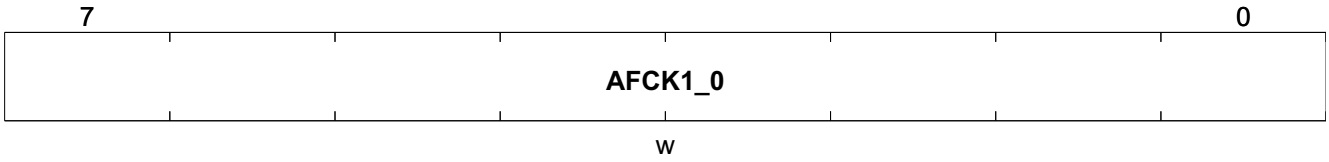
A_AFCSFCFG	Offset	Reset Value
AFC Start/Freeze Configuration Register	$02C_H$	00_H

7	6	5	4	2	1	0
UNUSED	AFCBLASK	AFCRESATCC	AFCFREEZE		AFCSTART	
-	w	w	w		w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
AFCBLASK	6	w	**AFC blocking during a low phase in the ASK signal** 0_B Disabled 1_B Enabled Reset: 0_H
AFCRESATCC	5	w	**Enable AFC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H
AFCFREEZE	4:2	w	**AFC Freeze Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 000_B Stay ON 001_B Freeze on RSSI Event + Delay (AFCAGCDEL) 010_B not used 011_B not used 100_B SPI Command - write to EXTPCMD.AFCMANF bit 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H
AFCSTART	1:0	w	**AFC Start Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B not used Reset: 0_H

AFC Integrator 1 Gain Register 0

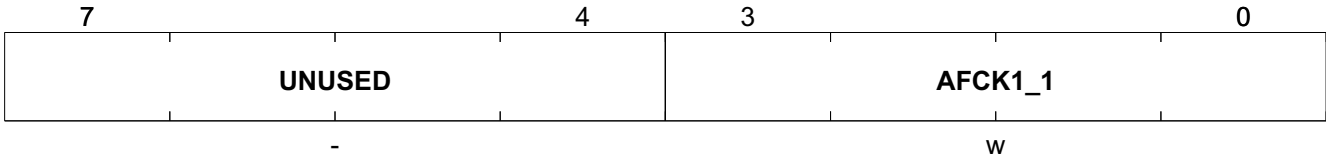
A_AFCK1CFG0	Offset	Reset Value
AFC Integrator 1 Gain Register 0	**$02D_H$**	**00_H**



Field	Bits	Type	Description
AFCK1_0	7:0	w	**AFC Filter coefficient K1, AFCK1(11:0) = AFCK1_1(MSB) & AFCK1_0(LSB)** Reset: 00_H

AFC Integrator 1 Gain Register 1

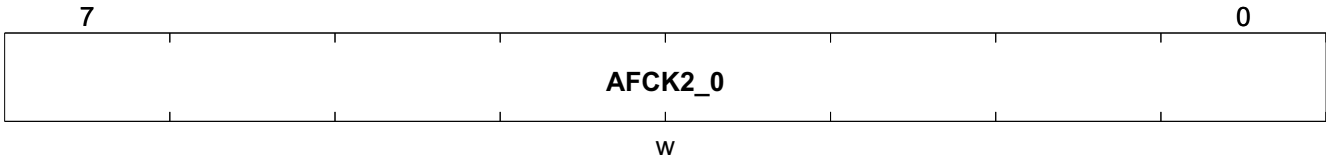
A_AFCK1CFG1	Offset	Reset Value
AFC Integrator 1 Gain Register 1	**$02E_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCK1_1	3:0	w	**AFC Filter coefficient K1, AFCK1(11:0) = AFCK1_1(MSB) & AFCK1_0(LSB)** Reset: 0_H

AFC Integrator 2 Gain Register 0

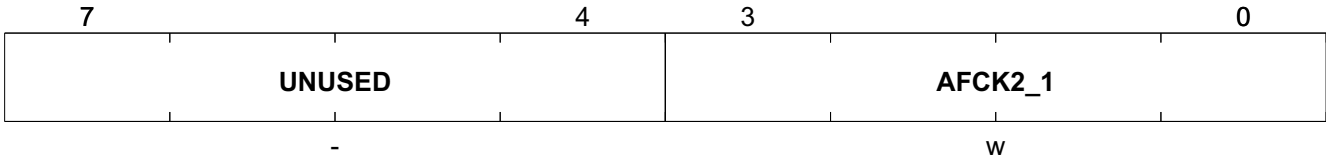
A_AFCK2CFG0	Offset	Reset Value
AFC Integrator 2 Gain Register 0	**$02F_H$**	**00_H**



Field	Bits	Type	Description
AFCK2_0	7:0	w	**AFC Filter coefficient K2, AFCK2(11:0) = AFCK2_1(MSB) & AFCK2_0(LSB)** Reset: 00_H

AFC Integrator 2 Gain Register 1

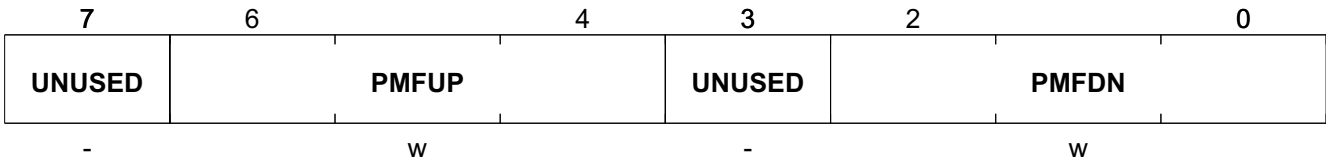
A_AFCK2CFG1	Offset	Reset Value
AFC Integrator 2 Gain Register 1	**030_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCK2_1	3:0	w	**AFC Filter coefficient K2, AFCK2(11:0) = AFCK2_1(MSB) & AFCK2_0(LSB)** Reset: 0_H

Peak Memory Filter Up-Down Factor Register

A_PMFUDSF	Offset	Reset Value
Peak Memory Filter Up-Down Factor Register	**031_H**	**42_H**

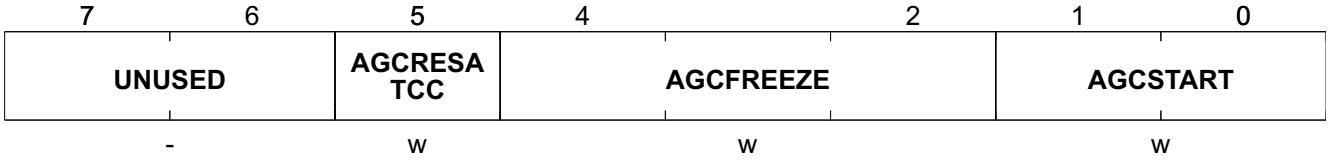


Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
PMFUP	6:4	w	**Peak Memory Filter Attack (Up) Factor** 000_B 2^-1 001_B 2^-2 010_B 2^-3 011_B 2^-4 100_B 2^-5 101_B 2^-6 110_B 2^-7 111_B 2^-8 Reset: 4_H
UNUSED	3	-	**UNUSED** Reset: 0_H
PMFDN	2:0	w	**Peak Memory Filter Decay (Down) Factor (additional to Attack Factor)** 000_B 2^-2 001_B 2^-3 010_B 2^-4 011_B 2^-5 100_B 2^-6 101_B 2^-7 110_B 2^-8 111_B 2^-9 Reset: 2_H

AGC Start/Freeze Configuration Register

A_AGCSFCFG	Offset	Reset Value
AGC Start/Freeze Configuration Register	**032_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
AGCRESATCC	5	w	**Enable AGC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
AGCFREEZE	4:2	w	**AGC Freeze Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 000_B Stay ON 001_B Freeze on RSSI Event + Delay (AFCAGCDEL) 010_B not used 011_B not used 100_B SPI Command - write to EXTPCMD.AGCMANF bit 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H
AGCSTART	1:0	w	**AGC Start Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B not used Reset: 0_H

AGC Configuration Register 0

A_AGCCFG0	Offset	Reset Value
AGC Configuration Register 0	**033_H**	**$2B_H$**

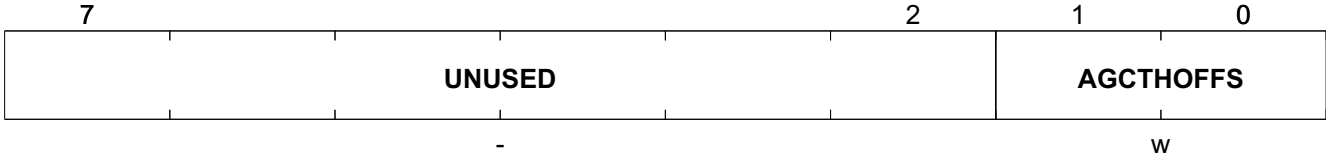
7	6	4	3	2	1	0
UNUSED	**AGCDGC**		**AGCHYS**		**AGCGAIN**	
-	w		w		w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
AGCDGC	6:4	w	**AGC Digital RSSI Gain Correction Tuning** 000_B 14.5 dB 001_B 15.0 dB 010_B 15.5 dB 011_B 16.0 dB 100_B 16.5 dB 101_B 17.0 dB 110_B 17.5 dB 111_B 18.0 dB Reset: 2_H

Field	Bits	Type	Description
AGCHYS	3:2	w	**AGC Threshold Hysteresis** 00_B 12.8 dB 01_B 17.1 dB 10_B 21.3 dB 11_B 25.6 dB Reset: 2_H
AGCGAIN	1:0	w	**AGC Gain Control** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B Automatic Reset: 3_H

AGC Configuration Register 1

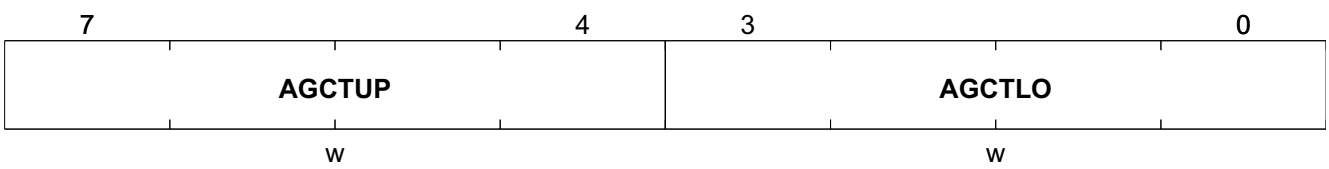
A_AGCCFG1	Offset	Reset Value
AGC Configuration Register 1	**034_H**	**03_H**



Field	Bits	Type	Description
UNUSED	7:2	-	**UNUSED** Reset: 00_H
AGCTHOFFS	1:0	w	**AGC Threshold Offset** 00_B 25.5 dB 01_B 38.3 dB 10_B 51.1 dB 11_B 63.9 dB Reset: 3_H

AGC Threshold Register

A_AGCTHR	Offset	Reset Value
AGC Threshold Register	**035_H**	**08_H**



Field	Bits	Type	Description
AGCTUP	7:4	w	**AGC Upper Attack Threshold [dB]** AGC Upper Threshold = A_AGCCFG1.AGCTHOFFS + 25.6 + AGCTUP*1.6 Reset: 0_H
AGCTLO	3:0	w	**AGC Lower Attack Threshold [dB]** AGC Lower Threshold = A_AGCCFG1.AGCTHOFFS + AGCTLO*1.6 Reset: 8_H

Digital Receiver Configuration Register

A_DIGRXC	Offset	Reset Value
Digital Receiver Configuration Register	**036_H**	**40_H**

7	6	3	2	1	0
INITDRXES	**UNUSED**		**DINVEXT**	**AAFBYP**	**AAFFCSEL**
w	w		w	w	w

Field	Bits	Type	Description
INITDRXES	7	w	**Init the Digital Receiver at EOM signal (e.g. for initialization of the Peak Memory Filter)** 0_B Disabled 1_B Enabled Reset: 0_H
UNUSED	6:3	w	**UNUSED** Reset: 8_H
DINVEXT	2	w	**Data Inversion of signal DATA and DATA_MATCHFIL for External Processing** 0_B Not inverted 1_B Inverted Reset: 0_H
AAFBYP	1	w	**Anti-Alliasing Filter Bypass for RSSI pin** 0_B Not bypassed 1_B Bypassed Reset: 0_H
AAFFCSEL	0	w	**Anti-Alliasing Filter Corner Frequency Select** 0_B 40 kHz 1_B 80 kHz Reset: 0_H

Image Supression Fc Selection Register

A_ISUPFCSEL **Offset** **Reset Value**

Image Supression Fc Selection Register **038_H** **07_H**

7	4	3	2	0
UNUSED		Res	FCSEL	
-			w	

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
FCSEL	2:0	w	**Image Supression Filter Corner Frequency Selection for FSK signal path** 000_B 33 kHz 001_B 46 kHz 010_B 65 kHz 011_B 93 kHz 100_B 132 kHz 101_B 190 kHz 110_B 239 kHz 111_B 282 kHz Reset: 7_H

Pre Decimation Factor Register

A_PDECF **Offset** **Reset Value**

Pre Decimation Factor Register **039_H** **00_H**

7	6	0
UNUSED	PREDECF	
-	w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
PREDECF	6:0	w	**Predecimation Filter Decimation Factor** Predecimation Factor = PREDECF + 1 Reset: 00_H

Pre Decimation Scaling Register FSK Mode

A_PDECSCFSK **Offset** **Reset Value**

Pre Decimation Scaling Register FSK Mode **$03A_H$** **00_H**

7	6	5	4	0
Res		INTPOLENF	PDSCALEF	
		w	w	

Field	Bits	Type	Description
INTPOLENF	5	w	**FSK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 0_H
PDSCALEF	4:0	w	**Predecimation Block Scaling Factor for FSK** Min 00h : 2^-10 Max 17h : 2^13 Reset: 00_H

Pre Decimation Scaling Register ASK Mode

A_PDECSCASK **Offset** **Reset Value**

Pre Decimation Scaling Register ASK Mode **$03B_H$** **20_H**

7	6	5	4	0
UNUSED	Res	INTPOLENA	PDSCALEA	
-		w	w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
INTPOLENA	5	w	**ASK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 1_H
PDSCALEA	4:0	w	**Predecimation Block Scaling Factor for ASK** Min 00h : 2^-10 Max 17h : 2^13 Reset: 00_H

Matched Filter Control Register

A_MFC **Offset** **Reset Value**

Matched Filter Control Register **$03C_H$** **07_H**

7	6	5	4	3	2	1	0
UNUSED				MFL			
-				w			

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
MFL	3:0	w	**Matched Filter Length** MF Length = MFL + 1 Reset: 7_H

Sampe Rate Converter NCO Tune

A_SRC **Offset** **Reset Value**

Sampe Rate Converter NCO Tune **$03D_H$** **00_H**

7	6	5	4	3	2	1	0
SRCNCO							
w							

Field	Bits	Type	Description
SRCNCO	7:0	w	**Sample Rate Converter NCO Tune** Min 00h : Fout = Fin Max FFh : Fout = Fin / 2 Reset: 00_H

Externel Data Slicer Configuration

A_EXTSLC **Offset** **Reset Value**

Externel Data Slicer Configuration **$03E_H$** **02_H**

7	6	5	4	3	2	1	0
UNUSED	Res		ESLCSCA		ESLCBW		
-			w		w		

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
ESLCSCA	4:3	w	**External Slicer BW Selection Scaling** 00_B 1/2 01_B 1/4 10_B 1/8 11_B 1/16 Reset: 0_H
ESLCBW	2:0	w	**External Slicer Manual BW Selection** 000_B 1/8 001_B 1/16 010_B 1/24 011_B 1/32 100_B 1/40 101_B 1/48 110_B n.u. 111_B n.u. Reset: 2_H

Channel Configuration Register

A_CHCFG	Offset	Reset Value
Channel Configuration Register	**058_H**	**44_H**

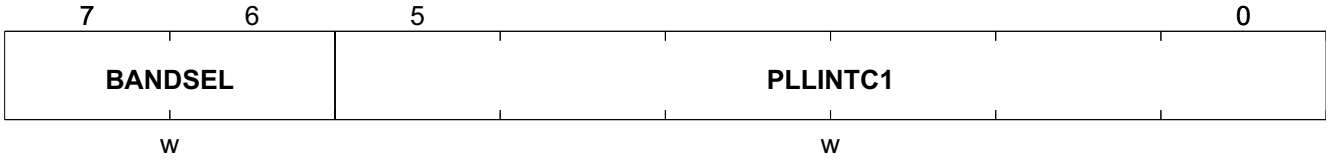
7	5	4	3	2	1	0
UNUSED		**EOM2SPM**	**NOC**		**MT**	
-		w	w		w	

Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 2_H
EOM2SPM	4	w	**Continue with Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Disabled - stay in Run Mode Self Polling (next Payload Frame is expected) 1_B Enabled - leave Run Mode Self Polling after EOM Reset: 0_H

Field	Bits	Type	Description
NOC	3:2	w	**Number of Channels (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B Channel 1 / Channel 1 01_B Channel 1 / Channel 1 10_B Channel 2 / Channel 1 + 2 11_B Channel 3 / Channel 1 + 2 + 3 Reset: 1_H
MT	1:0	w	**Modulation Type (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B ASK / ASK - ASK 01_B FSK / FSK - FSK 10_B ASK / FSK - ASK 11_B FSK / ASK - FSK Reset: 0_H

PLL MMD Integer Value Register Channel 1

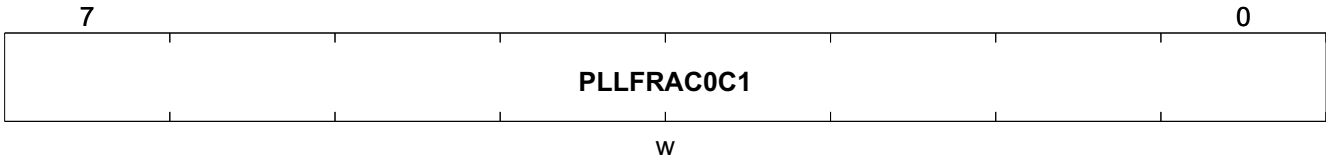
A_PLLINTC1	Offset	Reset Value
PLL MMD Integer Value Register Channel 1	**059_H**	**93_H**



Field	Bits	Type	Description
BANDSEL	7:6	w	**Frequency Band Selection** 00_B not used 01_B 915MHz/868MHz 10_B 434MHz 11_B 315MHz Reset: 2_H
PLLINTC1	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 1** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 1

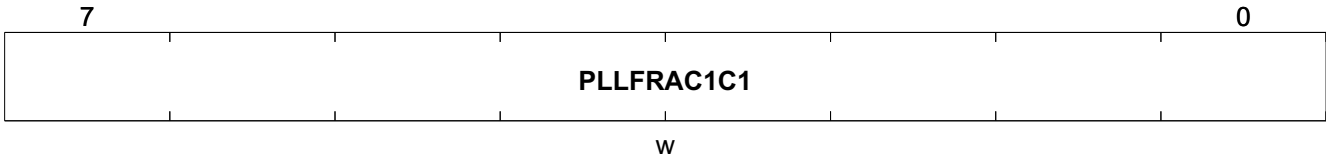
A_PLLFRAC0C1	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 1	**$05A_H$**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 1

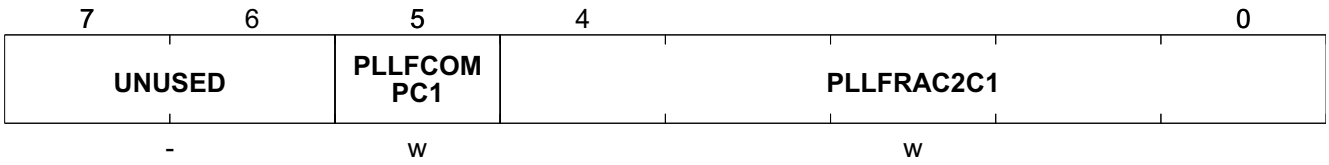
A_PLLFRAC1C1	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 1	**$05B_H$**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 1

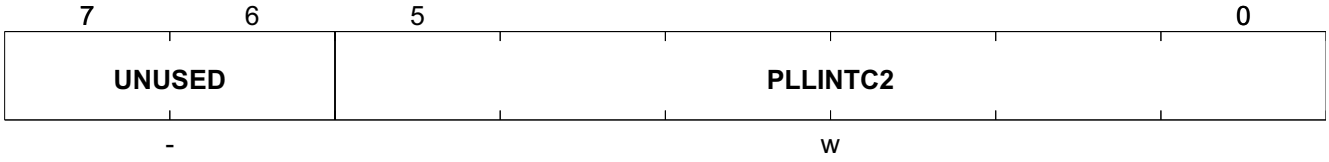
A_PLLFRAC2C1	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 1	**$05C_H$**	**09_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC1	5	w	**Fractional Spurii Compensation enable for Channel 1** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C1	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 2

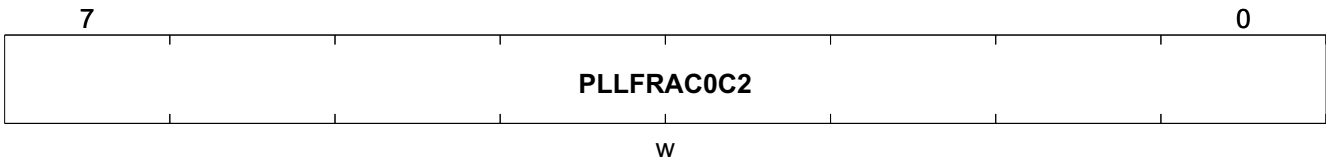
A_PLLINTC2	Offset	Reset Value
PLL MMD Integer Value Register Channel 2	**$05D_H$**	**13_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLINTC2	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 2** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 2

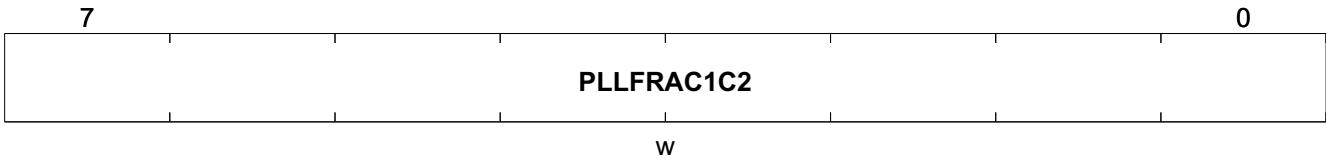
A_PLLFRAC0C2	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 2	**$05E_H$**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 2

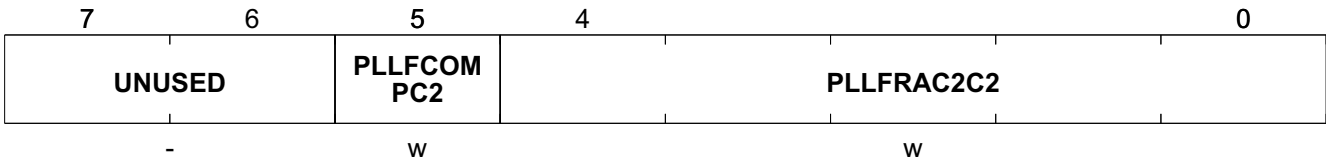
A_PLLFRAC1C2	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 2	**$05F_H$**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 2

A_PLLFRAC2C2	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 2	**060_H**	**09_H**

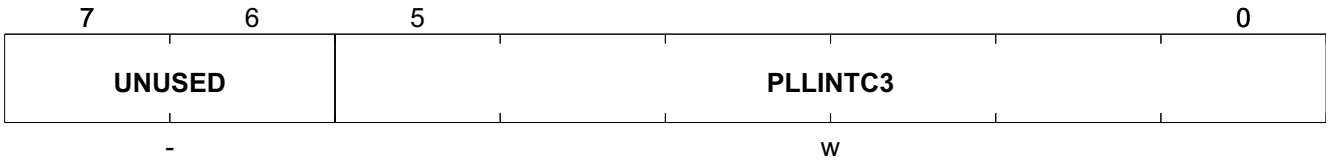


Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC2	5	w	**Fractional Spurii Compensation enable for Channel 2** 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
PLLFRAC2C2	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 3

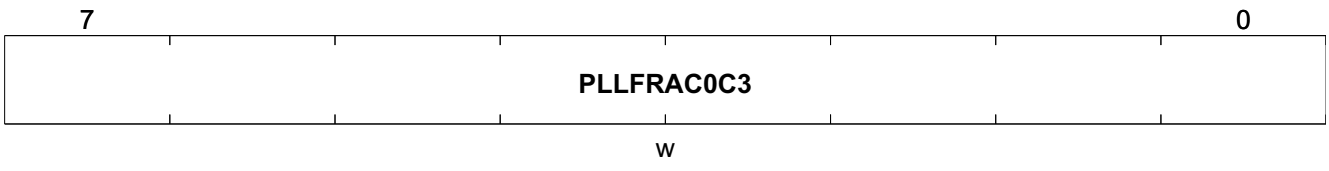
A_PLLINTC3	Offset	Reset Value
PLL MMD Integer Value Register Channel 3	**061_H**	**13_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLINTC3	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 3** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 3

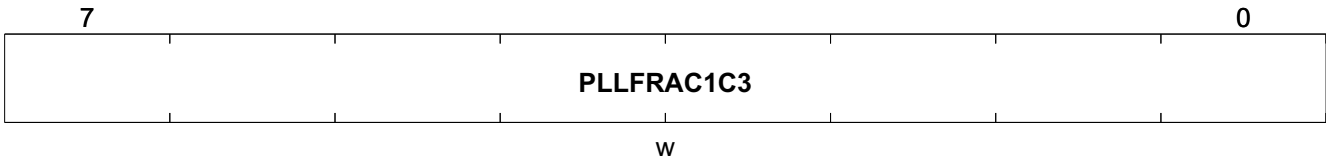
A_PLLFRAC0C3	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 3	**062_H**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 3

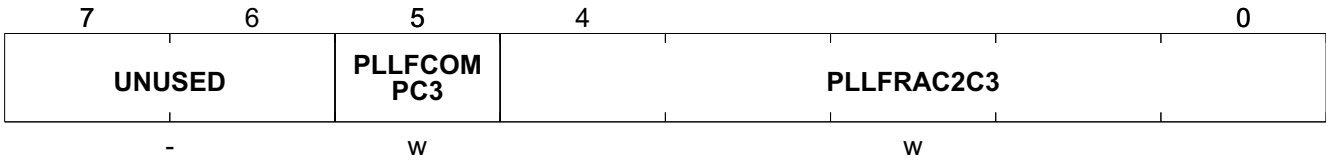
A_PLLFRAC1C3	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 3	063_H	07_H



Field	Bits	Type	Description
PLLFRAC1C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 3

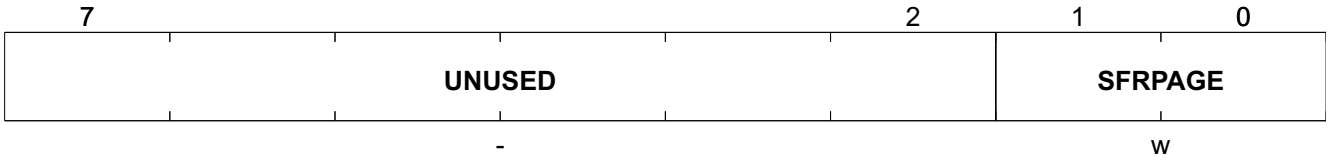
A_PLLFRAC2C3	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 3	064_H	09_H



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC3	5	w	**Fractional Spurii Compensation enable for Channel 3** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C3	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

Special Function Register Page Register

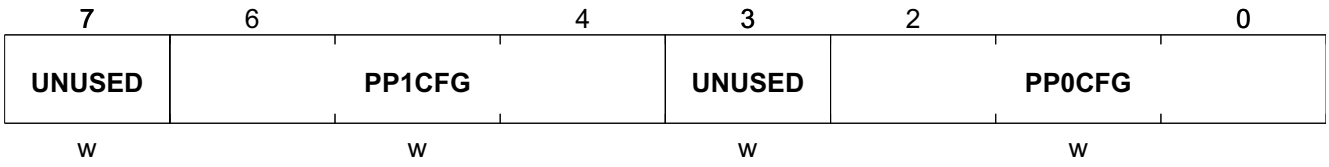
SFRPAGE	Offset	Reset Value
Special Function Register Page Register	080_H	00_H



Field	Bits	Type	Description
UNUSED	7:2	-	**UNUSED** Reset: 00_H
SFRPAGE	1:0	w	**Selection of Register Page File (Configuration A..D) for SPI communication** 00_B Page 0 (Config. A, start address: 000_H) 01_B Page 1 (Config. B, start address: 100_H) 10_B Page 2 (Config. C, start address: 200_H) 11_B Page 3 (Config. D, start address: 300_H) Reset: 0_H

PP0 and PP1 Configuration Register

PPCFG0	Offset	Reset Value
PP0 and PP1 Configuration Register	081_H	50_H



Field	Bits	Type	Description
UNUSED	7	w	**UNUSED** Reset: 0_H
PP1CFG	6:4	w	**Port Pin 1 Output Signal Selection** 000_B CLK_OUT 001_B RX_RUN 010_B NINT 011_B LOW 100_B HIGH 101_B DATA 110_B DATA_MATCHFIL 111_B n.u. Reset: 5_H

Field	Bits	Type	Description
UNUSED	3	w	**UNUSED** Reset: 0_H
PP0CFG	2:0	w	**Port Pin 0 Output Signal Selection** 000_B CLK_OUT 001_B RX_RUN 010_B NINT 011_B LOW 100_B HIGH 101_B DATA 110_B DATA_MATCHFIL 111_B n.u. Reset: 0_H

PP2 and PP3 Configuration Register

PPCFG1	Offset	Reset Value
PP2 and PP3 Configuration Register	**082_H**	**12_H**

7	6	4	3	2	0
UNUSED	**PP3CFG**		**UNUSED**	**PP2CFG**	
w	w		w	w	

Field	Bits	Type	Description
UNUSED	7	w	**UNUSED** Reset: 0_H
PP3CFG	6:4	w	**Port Pin 3 Output Signal Selection** 000_B n.u. 001_B RX_RUN 010_B NINT 011_B LOW 100_B HIGH 101_B DATA 110_B DATA_MATCHFIL 111_B n.u. Reset: 1_H
UNUSED	3	w	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
PP2CFG	2:0	w	**Port Pin 2 Output Signal Selection** 000_B CLK_OUT 001_B RX_RUN 010_B NINT 011_B LOW 100_B HIGH 101_B DATA 110_B DATA_MATCHFIL 111_B n.u. Reset: 2_H

PPx Port Configuration Register

PPCFG2	Offset	Reset Value
PPx Port Configuration Register	083_H	00_H

7	6	5	4	3	2	1	0
PP3HPPEN	PP2HPPEN	PP1HPPEN	PP0HPPEN	PP3INV	PP2INV	PP1INV	PP0INV
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PP3HPPEN	7	w	**PP3 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP2HPPEN	6	w	**PP2 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP1HPPEN	5	w	**PP1 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP0HPPEN	4	w	**PP0 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP3INV	3	w	**PP3 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H

Field	Bits	Type	Description
PP2INV	2	w	**PP2 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP1INV	1	w	**PP1 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP0INV	0	w	**PP0 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H

RX RUN Configuration Register 0

RXRUNCFG0	Offset	Reset Value
RX RUN Configuration Register 0	084_H	FF_H

7	6	5	4	3	2	1	0
RXRUNPP 1D	RXRUNPP 1C	RXRUNPP 1B	RXRUNPP 1A	RXRUNPP 0D	RXRUNPP 0C	RXRUNPP 0B	RXRUNPP 0A
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXRUNPP1D	7	w	**RXRUN Active Level on PP1 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1C	6	w	**RXRUN Active Level on PP1 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1B	5	w	**RXRUN Active Level on PP1 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1A	4	w	**RXRUN Active Level on PP1 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0D	3	w	**RXRUN Active Level on PP0 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H

Field	Bits	Type	Description
RXRUNPP0C	2	w	**RXRUN Active Level on PP0 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0B	1	w	**RXRUN Active Level on PP0 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0A	0	w	**RXRUN Active Level on PP0 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

RX RUN Configuration Register 1

RXRUNCFG1	Offset	Reset Value
RX RUN Configuration Register 1	085_H	FF_H

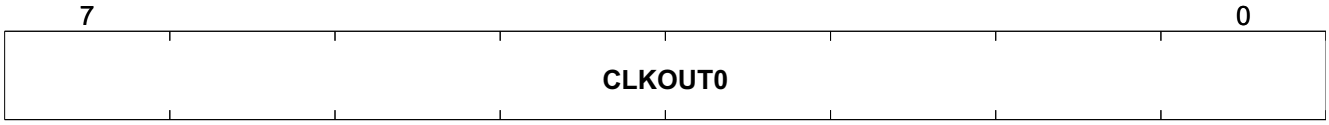
7	6	5	4	3	2	1	0
RXRUNPP 3D	RXRUNPP 3C	RXRUNPP 3B	RXRUNPP 3A	RXRUNPP 2D	RXRUNPP 2C	RXRUNPP 2B	RXRUNPP 2A
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXRUNPP3D	7	w	**RXRUN Active Level on PP3 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3C	6	w	**RXRUN Active Level on PP3 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3B	5	w	**RXRUN Active Level on PP3 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3A	4	w	**RXRUN Active Level on PP3 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2D	3	w	**RXRUN Active Level on PP2 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H

Field	Bits	Type	Description
RXRUNPP2C	2	w	**RXRUN Active Level on PP2 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2B	1	w	**RXRUN Active Level on PP2 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2A	0	w	**RXRUN Active Level on PP2 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

Clock Divider Register 0

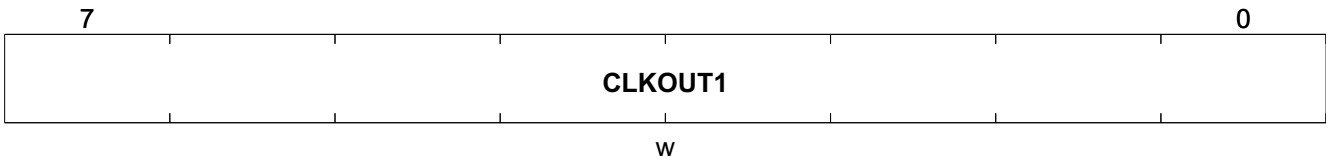
CLKOUT0	Offset	Reset Value
Clock Divider Register 0	**086_H**	**$0B_H$**



Field	Bits	Type	Description
CLKOUT0	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: $0B_H$

Clock Divider Register 1

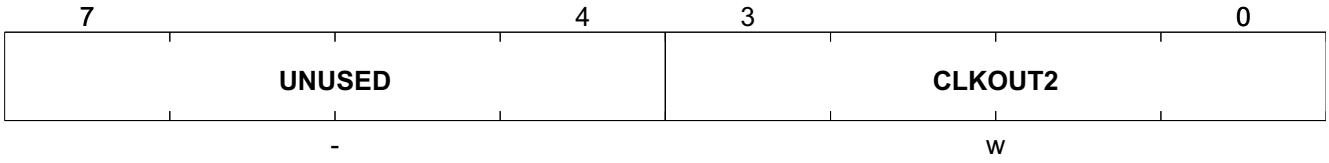
CLKOUT1	Offset	Reset Value
Clock Divider Register 1	**087_H**	**00_H**



Field	Bits	Type	Description
CLKOUT1	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 00_H

Clock Divider Register 2

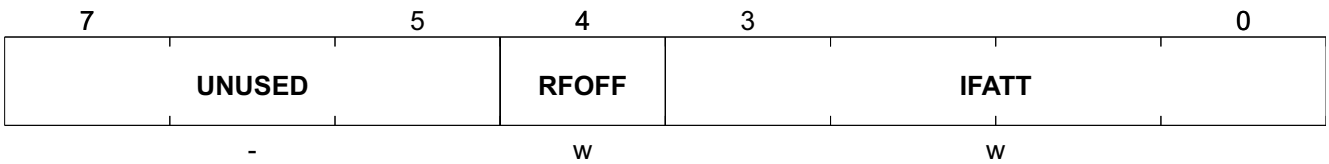
CLKOUT2	Offset	Reset Value
Clock Divider Register 2	**088_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
CLKOUT2	3:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 0_H

RF Control Register

RFC	Offset	Reset Value
RF Control Register	**089_H**	**07_H**

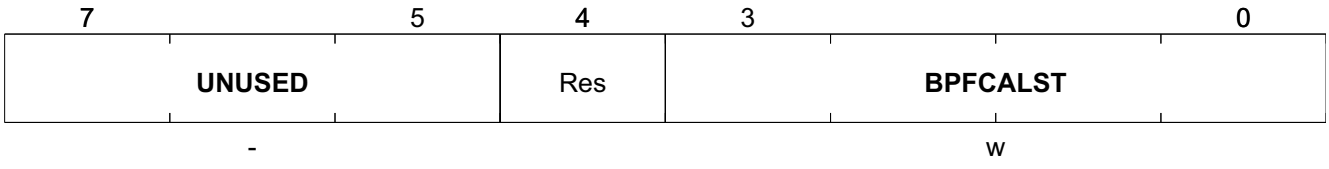


Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
RFOFF	4	w	**Switch off RF-path (for RSSI trimming)** 0_B RF path enabled 1_B RF path disabled Reset: 0_H
IFATT	3:0	w	**Adjust IF attenuation from LNA_IN to IF_OUT (Double-Down Conversion / Single-Down Conversion)** Used to trim out external component tolerances. 0000_B 0 dB / n.u. 0001_B 0.8 dB / n.u. 0010_B 1.6 dB / n.u. 0011_B 2.4 dB / n.u. 0100_B 3.2 dB / 0 dB 0101_B 4.0 dB / 0.8 dB 0110_B 4.8 dB / 1.6 dB 0111_B 5.6 dB / 2.4 dB 1000_B 6.4 dB / 3.2 dB 1001_B 7.2 dB / 4.0 dB 1010_B 8.0 dB / 4.8 dB 1011_B 8.8 dB / n.u. 1100_B 9.6 dB / n.u. 1101_B 10.4 dB / n.u. 1110_B 11.2 dB / n.u. 1111_B 12.0 dB / n.u. Reset: 7_H

BPF Calibration Configuration Register 0

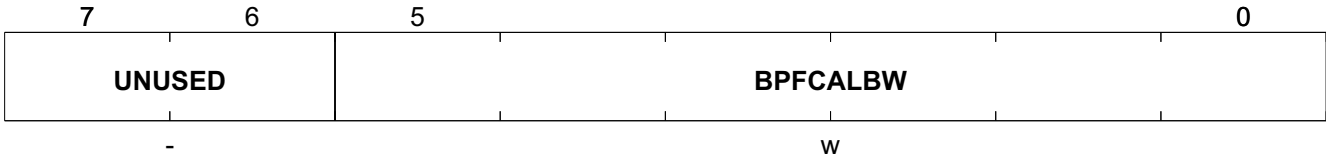
BPFCALCFG0	Offset	Reset Value
BPF Calibration Configuration Register 0	$08A_H$	07_H



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
BPFCALST	3:0	w	**BPF Calibration Time (use default = 07_H)** Min: 0h= Txtal * 80 * 7 * (0 + 4) Max: Fh= Txtal * 80 * 7 * (15 + 4) Reset: 7_H

BPF Calibration Configuration Register 1

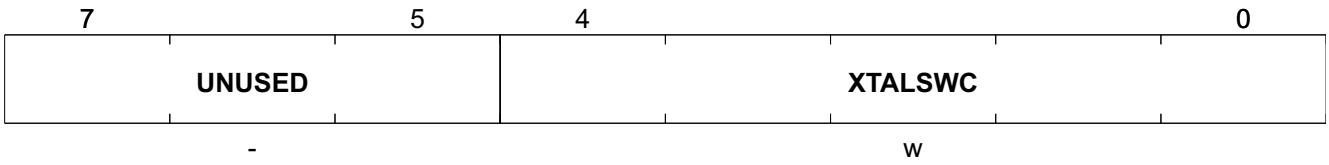
BPFCALCFG1	Offset	Reset Value
BPF Calibration Configuration Register 1	$08B_H$	04_H



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
BPFCALBW	5:0	w	**Band Pass Filter Bandwidth Selection during Calibration** 04_H - 50 kHz (=default) $0D_H$ - 80 kHz 16_H - 125 kHz $1F_H$ - 200 kHz 27_H - 300 kHz Reset: 04_H

XTAL Coarse Calibration Register

XTALCAL0	Offset	Reset Value
XTAL Coarse Calibration Register	$08C_H$	10_H



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
XTALSWC	4:0	w	**Xtal Trim Capacitor Value** Min 00h: 0pF Value 01h: 1pF Max 18h: 24pF higher values than 18h are automatically mapped to 24pF Reset: 10_H

XTAL Fine Calibration Register

XTALCAL1 **Offset** **Reset Value**

XTAL Fine Calibration Register **$08D_H$** **00_H**

7	6	5	4	3	2	1	0
UNUSED				XTALSWF3	XTALSWF2	XTALSWF1	XTALSWF0
-				w	w	w	w

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
XTALSWF3	3	w	**Connect 500 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF2	2	w	**Connect 250 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF1	1	w	**Connect 125 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF0	0	w	**Connect 62.5 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H

RSSI Monitor Configuration Register

RSSIMONC **Offset** **Reset Value**

RSSI Monitor Configuration Register **$08E_H$** **01_H**

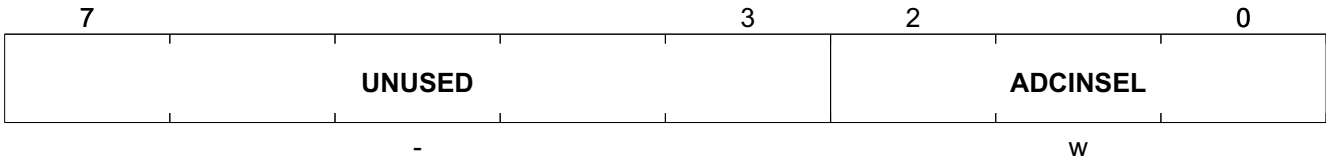
7	6	5	4	3	2	1	0
UNUSED					Res		RSSIMONEN
-							w

Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H

Field	Bits	Type	Description
RSSIMONEN	0	w	**Enable Buffer for RSSI pin** 0_B Disabled 1_B Enabled Reset: 1_H

ADC Input Selection Register

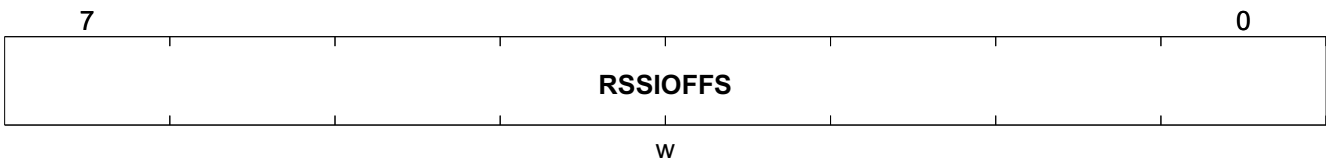
ADCINSEL	Offset	Reset Value
ADC Input Selection Register	**$08F_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
ADCINSEL	2:0	w	**ADC Input Selection** 000_B RSSI 001_B Temperature 010_B VDDD / 2 011_B n.u. 100_B n.u. 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H

RSSI Offset Register

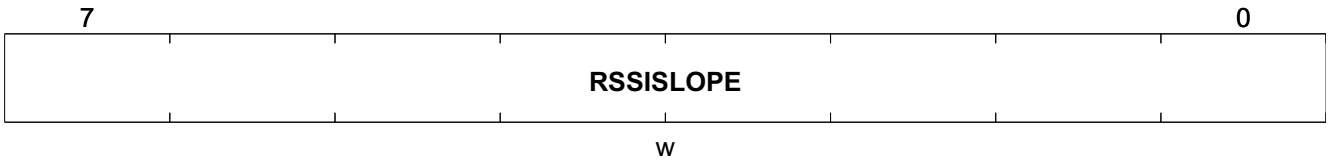
RSSIOFFS	Offset	Reset Value
RSSI Offset Register	**090_H**	**80_H**



Field	Bits	Type	Description
RSSIOFFS	7:0	w	**RSSI Offset Compensation Value** Min: 00h= -256 Max: FFh= 254 Reset: 80_H

RSSI Slope Register

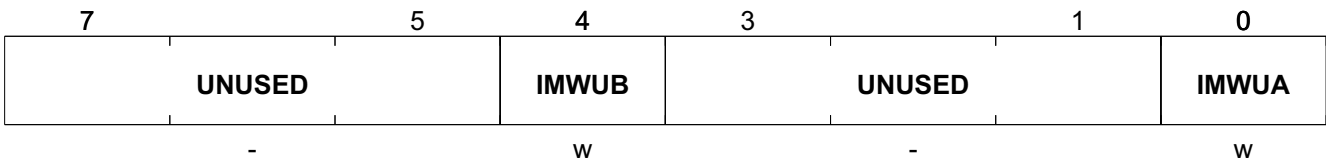
RSSISLOPE	Offset	Reset Value
RSSI Slope Register	**091_H**	**80_H**



Field	Bits	Type	Description
RSSISLOPE	7:0	w	**RSSI Slope Compensation Value (Multiplication Value)** Multiplication Factor = RSSISLOPE * 2^-7 Min: 00h= 0.0 Max: FFh= 1.992 Reset: 80_H

Interrupt Mask Register 0

IM0	Offset	Reset Value
Interrupt Mask Register 0	**094_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
IMWUB	4	w	**Mask Interrupt on "Wake-up" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
UNUSED	3:1	-	**UNUSED** Reset: 0_H
IMWUA	0	w	**Mask Interrupt on "Wake-up" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Interrupt Mask Register 1

IM1	Offset	Reset Value
Interrupt Mask Register 1	**095_H**	**00_H**

7	5	4	3	1	0
UNUSED		**IMWUD**	**UNUSED**		**IMWUC**
-		w	-		w

Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
IMWUD	4	w	**Mask Interrupt on "Wake-up" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
UNUSED	3:1	-	**UNUSED** Reset: 0_H
IMWUC	0	w	**Mask Interrupt on "Wake-up" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Self Polling Mode Active Periods Register

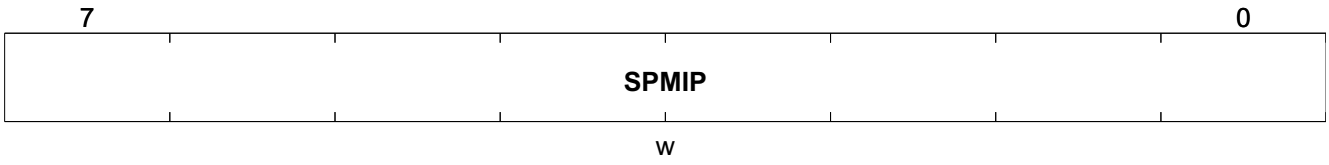
SPMAP	Offset	Reset Value
Self Polling Mode Active Periods Register	**096_H**	**01_H**

7	5	4	0
UNUSED		**SPMAP**	
-		w	

Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
SPMAP	4:0	w	**Self Polling Mode Active Periods value** Min: 01h = 1 (Master) Period Max: 1Fh = 31(Master) Periods Reg. value 00h = 32 (Master) Periods Reset: 01_H

Self Polling Mode Idle Periods Register

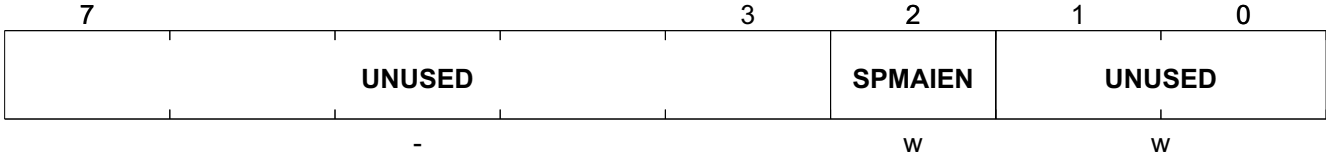
SPMIP	Offset	Reset Value
Self Polling Mode Idle Periods Register	**097_H**	**01_H**



Field	Bits	Type	Description
SPMIP	7:0	w	**Self Polling Mode Idle Periods value** Min: 01h = 1 (Master) Period Max: FFh = 255 (Master) Periods Reg. value 00h = 256 (Master) Periods Reset: 01_H

Self Polling Mode Control Register

SPMC	Offset	Reset Value
Self Polling Mode Control Register	**098_H**	**00_H**

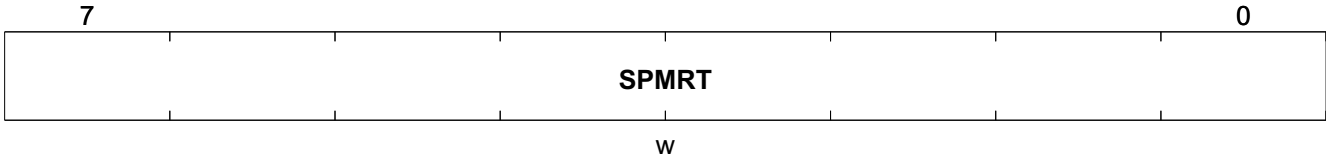


Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H

Field	Bits	Type	Description
SPMAIEN	2	w	**Self Polling Mode Active Idle Enable** 0_B Disabled 1_B Enabled Reset: 0_H
UNUSED	1:0	w	**UNUSED** Reset: 0_H

Self Polling Mode Reference Timer Register

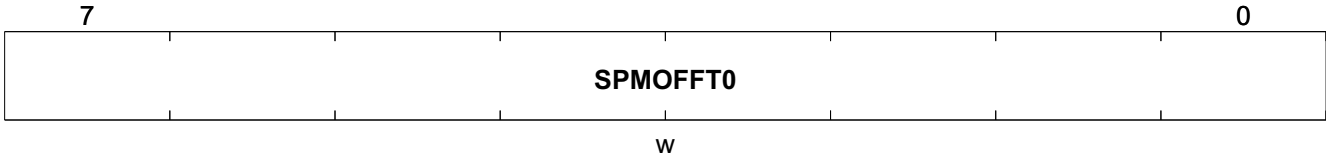
SPMRT	Offset	Reset Value
Self Polling Mode Reference Timer Register	**099_H**	**01_H**



Field	Bits	Type	Description
SPMRT	7:0	w	**Self Polling Mode Reference Timer value** The output of this timer is used as input for the On/Off Timer Incoming Periodic Time = 64 / fsys Output Periodic Time = TRT = (64 * SPMRT) / fsys Min: 01h = (64*1) / fsys Max: 00h = (64 * 256) / fsys Reset: 01_H

Self Polling Mode Off Time Register 0

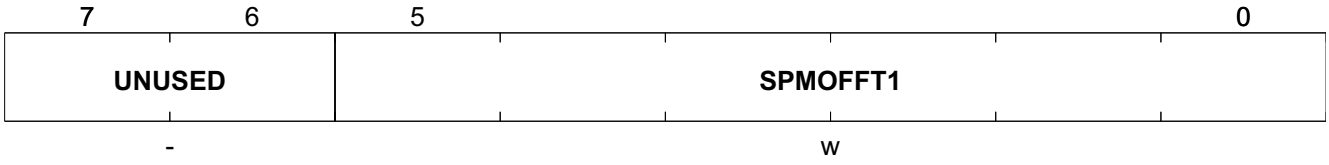
SPMOFFT0	Offset	Reset Value
Self Polling Mode Off Time Register 0	**$09A_H$**	**01_H**



Field	Bits	Type	Description
SPMOFFT0	7:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 01_H

Self Polling Mode Off Time Register 1

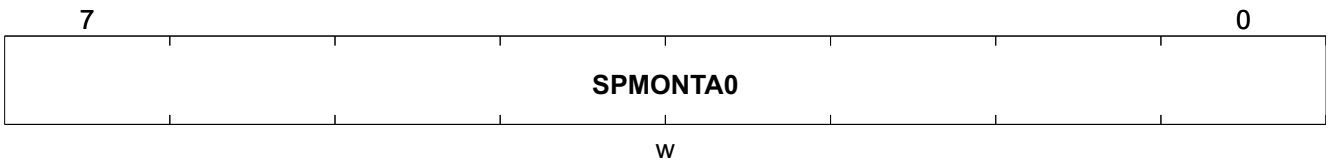
SPMOFFT1	Offset	Reset Value
Self Polling Mode Off Time Register 1	**$09B_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMOFFT1	5:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 00_H

Self Polling Mode On Time Config A Register 0

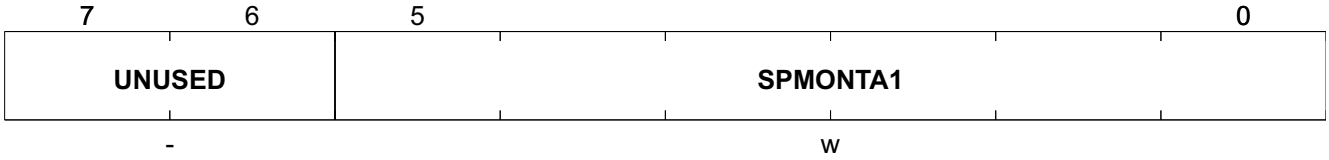
SPMONTA0	Offset	Reset Value
Self Polling Mode On Time Config A Register 0	**$09C_H$**	**01_H**



Field	Bits	Type	Description
SPMONTA0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config A Register 1

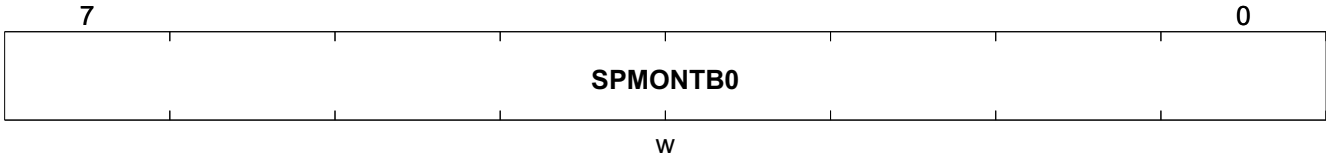
SPMONTA1	Offset	Reset Value
Self Polling Mode On Time Config A Register 1	**$09D_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTA1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config B Register 0

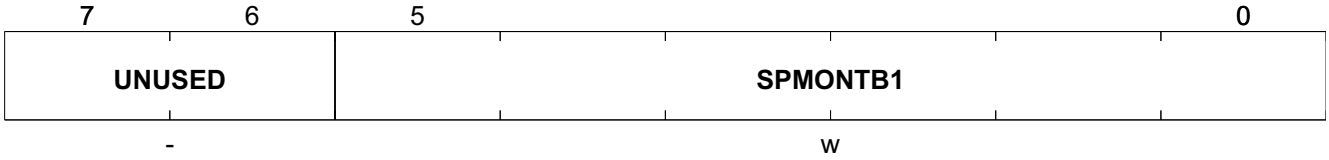
SPMONTB0	Offset	Reset Value
Self Polling Mode On Time Config B Register 0	**$09E_H$**	**01_H**



Field	Bits	Type	Description
SPMONTB0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config B Register 1

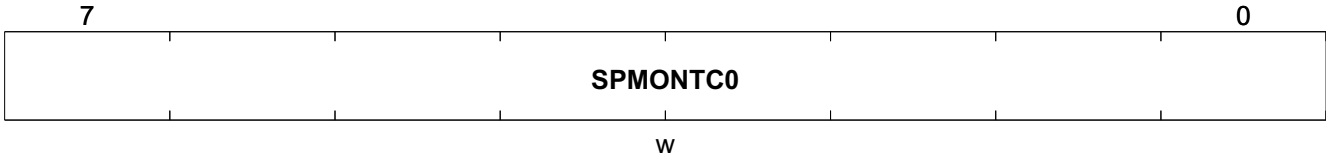
SPMONTB1	Offset	Reset Value
Self Polling Mode On Time Config B Register 1	**$09F_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTB1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config C Register 0

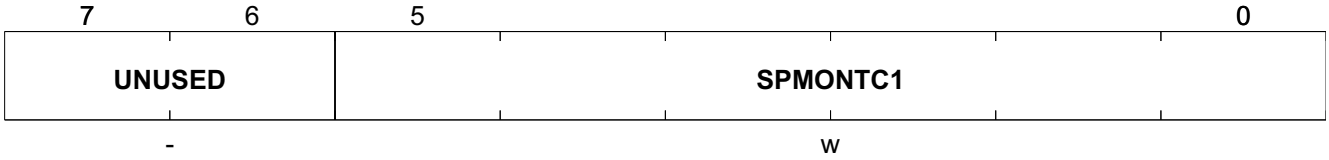
SPMONTC0	Offset	Reset Value
Self Polling Mode On Time Config C Register 0	**$0A0_H$**	**01_H**



Field	Bits	Type	Description
SPMONTC0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config C Register 1

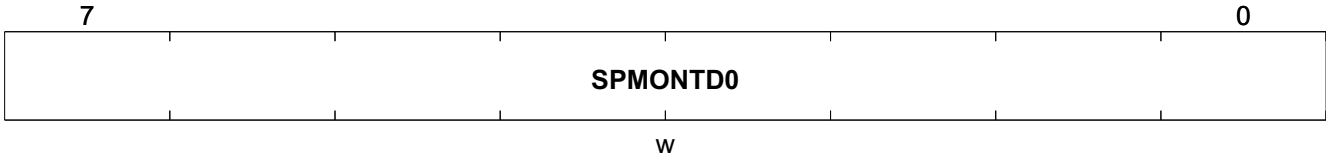
SPMONTC1	Offset	Reset Value
Self Polling Mode On Time Config C Register 1	**$0A1_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTC1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config D Register 0

SPMONTD0	Offset	Reset Value
Self Polling Mode On Time Config D Register 0	**$0A2_H$**	**01_H**



Field	Bits	Type	Description
SPMONTD0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config D Register 1

SPMONTD1	Offset	Reset Value
Self Polling Mode On Time Config D Register 1	**$0A3_H$**	**00_H**

7	6	5	0
UNUSED		SPMONTD1	
-		w	

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTD1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

External Processing Command Register

EXTPCMD	Offset	Reset Value
External Processing Command Register	**$0A4_H$**	**00_H**

7	6	4	3	2	1	0
Res	UNUSED		AGCMANF	AFCMANF	EXTTOTIM	EXTEOM
	-		wc	wc	wc	wc

Field	Bits	Type	Description
UNUSED	6:4	-	**UNUSED** Reset: 0_H
AGCMANF	3	wc	**AGC Manual Freeze** When *_AGCSFCFG.AGCFREEZE set to SPI Command, this bit sets the AGC to freeze mode 0_B Inactive 1_B Active Reset: 0_H
AFCMANF	2	wc	**AFC Manual Freeze** When *_AFCSFCFG.AFCFREEZE set to SPI Command, this bit sets the AFC to freeze mode 0_B Inactive 1_B Active Reset: 0_H
EXTTOTIM	1	wc	**Force TOTIM signal** 0_B no external TOTIM signal forced 1_B external TOTIM signal forced Reset: 0_H
EXTEOM	0	wc	**Force EOM signal** 0_B no external EOM signal forced 1_B external EOM signal forced Reset: 0_H

Chip Mode Control Register 1

CMC1	Offset	Reset Value
Chip Mode Control Register 1	**$0A5_H$**	**04_H**

7	6	5	4	3	1	0
UNUSED		**EOM2NCFG**	**TOTIM2NCH**	**UNUSED**		**XTALHPMS**
-		w	w	w		w

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
EOM2NCFG	5	w	**Continue with next Configuration in Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next Configuration in Self Polling Mode Reset: 0_H

Field	Bits	Type	Description
TOTIM2NCH	4	w	**Continue with next RF channel in Self Polling Mode after TOTIM detected in Run Mode Self Polling. In case of single RF channel application this means "continue with next Configuration" instead of "continue with next RF channel".** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next RF channel in Self Polling Mode Reset: 0_H
UNUSED	3:1	w	**UNUSED** Reset: 2_H
XTALHPMS	0	w	**XTAL High Precision Mode in Sleep Mode** 0_B Disabled 1_B Enabled Reset: 0_H

Chip Mode Control Register 0

CMC0	Offset	Reset Value
Chip Mode Control Register 0	$0A6_H$	10_H

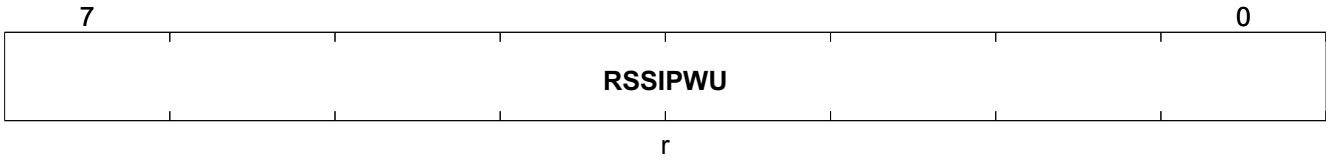
7	6	5	4	3	2	1	0
SDOHPPEN	INITPLLHOLD	HOLD	CLKOUTEN	MCS		SLRXEN	MSEL
w	w	w	w	w		w	w

Field	Bits	Type	Description
SDOHPPEN	7	w	**SDO High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
INITPLLHOLD	6	w	**Init PLL after coming from HOLD (when new channel programmed).** This requires an additional Channel Hop Time before initialization of the Digital Receiver. 0_B No init of PLL 1_B Init of PLL Reset: 0_H
HOLD	5	w	**Holds the chip in the Register Configuration state (only in Run Mode Slave)** 0_B Normal Operation 1_B Jump into the Register Config state Hold Reset: 0_H
CLKOUTEN	4	w	**CLK_OUT Enable** 0_B Disabled 1_B Enable programmable clock output Reset: 1_H

Field	Bits	Type	Description
MCS	3:2	w	**Multi Configuration Selection (Run Mode Slave / Self Polling Mode)** 00_B Config A / Config A 01_B Config B / Config A + B 10_B Config C / Config A + B + C 11_B Config D / Config A + B + C + D Reset: 0_H
SLRXEN	1	w	**Slave Receiver Enable** This Bit is only used in Operating Mode Run Mode Slave / Sleep Mode 0_B Receiver is in Sleep Mode 1_B Receiver is in Run Mode Slave Reset: 0_H
MSEL	0	w	**Operating Mode Selection** 0_B Run Mode Slave / Sleep Mode 1_B Self Polling Mode Reset: 0_H

Wakeup Peak Detector Readout Register

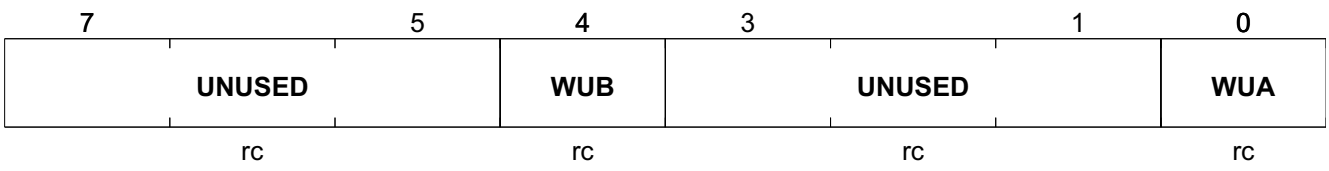
RSSIPWU	Offset	Reset Value
Wakeup Peak Detector Readout Register	**$0A7_H$**	**00_H**



Field	Bits	Type	Description
RSSIPWU	7:0	r	**Peak Detector Level at Wakeup** Set at every WU event and also set at the end of every configuration/channel cycle within a Self Polling period. Cleared at Reset only. Reset: 00_H

Interrupt Status Register 0

IS0	Offset	Reset Value
Interrupt Status Register 0	**$0A8_H$**	**FF_H**



Field	Bits	Type	Description
UNUSED	7:5	rc	**UNUSED** Reset: 7_H
WUB	4	rc	**Interrupt Request by "Wake Up" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
UNUSED	3:1	rc	**UNUSED** Reset: 7_H
WUA	0	rc	**Interrupt Request by "Wake Up" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Interrupt Status Register 1

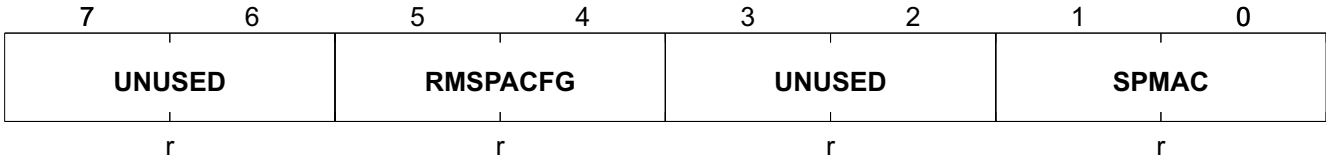
IS1	Offset	Reset Value
Interrupt Status Register 1	**$0A9_H$**	**FF_H**

7	5	4	3	1	0
UNUSED		**WUD**	**UNUSED**		**WUC**
rc		rc	rc		rc

Field	Bits	Type	Description
UNUSED	7:5	rc	**UNUSED** Reset: 7_H
WUD	4	rc	**Interrupt Request by "Wake Up" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
UNUSED	3:1	rc	**UNUSED** Reset: 7_H
WUC	0	rc	**Interrupt Request by "Wake Up" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

RF PLL Actual Channel and Configuration Register

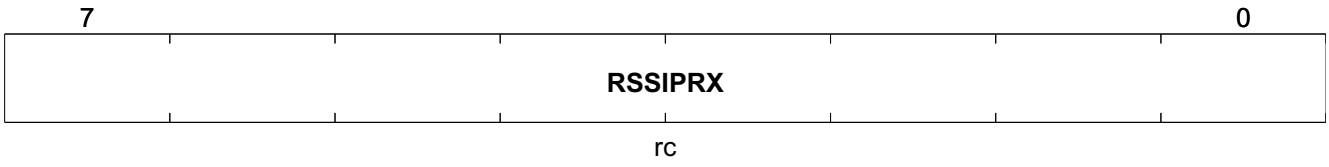
RFPLLACC	Offset	Reset Value
RF PLL Actual Channel and Configuration Register	$0AA_H$	00_H



Field	Bits	Type	Description
UNUSED	7:6	r	**UNUSED** Reset: 0_H
RMSPACFG	5:4	r	**RF PLL Run Mode Self Polling Actual Configuration** 00_B Configuration A 01_B Configuration B 10_B Configuration C 11_B Configuration D Reset: 0_H
UNUSED	3:2	r	**UNUSED** Reset: 0_H
SPMAC	1:0	r	**RF PLL Self Polling Mode Actual Channel** 00_B No Wake Up from any Channel was actually found 01_B Wake Up was found from Channel 1 10_B Wake Up was found from Channel 2 11_B Wake Up was found from Channel 3 Reset: 0_H

RSSI Peak Detector Readout Register

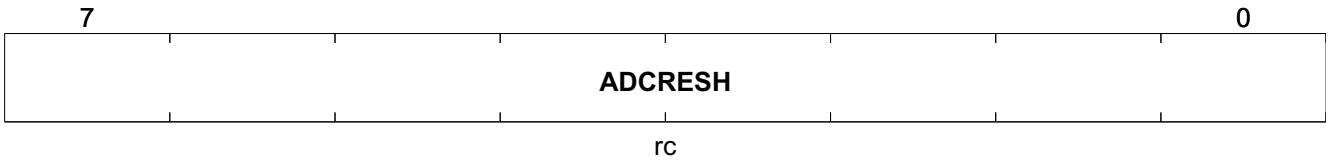
RSSIPRX	Offset	Reset Value
RSSI Peak Detector Readout Register	$0AB_H$	00_H



Field	Bits	Type	Description
RSSIPRX	7:0	rc	**RSSI Peak Level during Receiving** Tracking is active when Digital Receiver is enabled Set at higher peak levels than stored Cleared at Reset and SPI read out Reset: 00_H

ADC Result High Byte Register

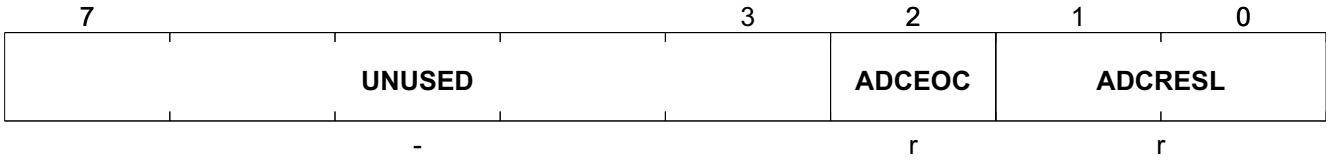
ADCRESH	Offset	Reset Value
ADC Result High Byte Register	**$0AE_H$**	**00_H**



Field	Bits	Type	Description
ADCRESH	7:0	rc	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** Note: RC for control signal generation only, no clear Reset: 00_H

ADC Result Low Byte Register

ADCRESL	Offset	Reset Value
ADC Result Low Byte Register	**$0AF_H$**	**00_H**

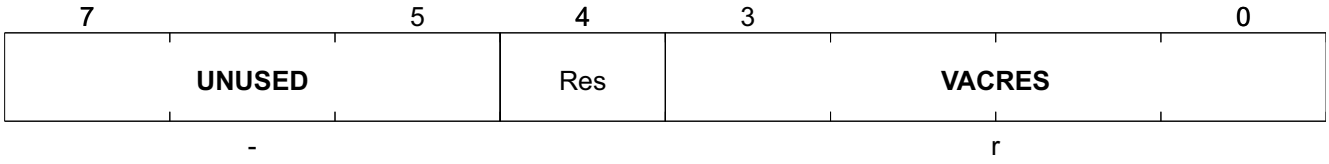


Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
ADCEOC	2	r	**ADC End of Conversion detected** 0_B not detected 1_B detected Reset: 0_H

Field	Bits	Type	Description
ADCRESL	1:0	r	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** The 2 LSBs of the ADC result are captured when the SFR register ADCRESH is readout. Reset: 0_H

VCO Autocalibration Result Readout Register

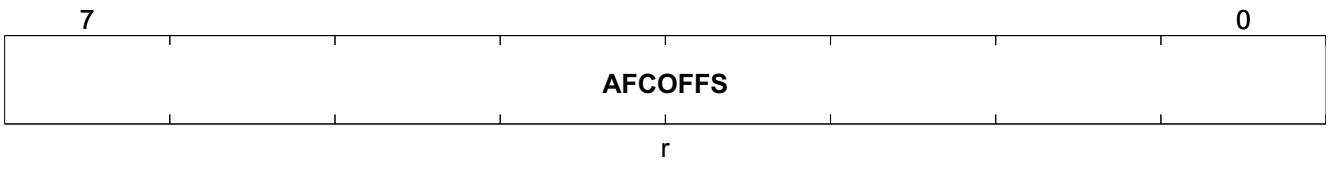
VACRES	Offset	Reset Value
VCO Autocalibration Result Readout Register	**$0B0_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
VACRES	3:0	r	**VCO Autocalibration Result** Returns the VCO range selected by VCO Autocalibration Reset: 0_H

AFC Offset Read Register

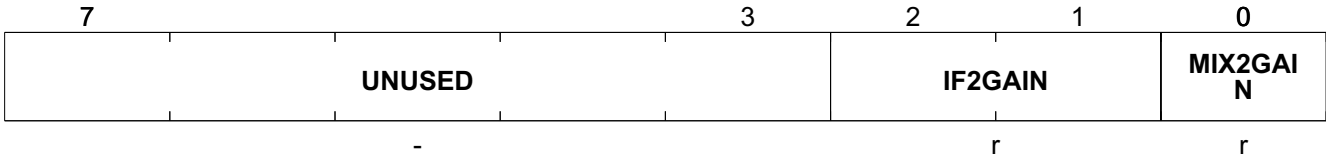
AFCOFFSET	Offset	Reset Value
AFC Offset Read Register	**$0B1_H$**	**00_H**



Field	Bits	Type	Description
AFCOFFS	7:0	r	**Readout of the Frequency Offset found by AFC (AFC loop filter output).** Value is in signed representation. Frequency resolution is 2.68 kHz/digit Output can be limited by x_AFCLIMIT register Update rate is 548 kHz Reset: 00_H

AGC Gain Readout Register

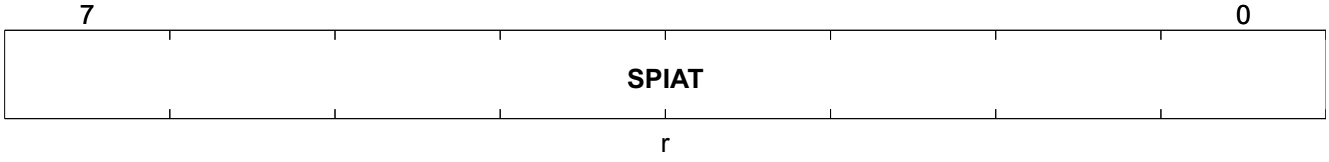
AGCGAINR	Offset	Reset Value
AGC Gain Readout Register	$0B2_H$	00_H



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
IF2GAIN	2:1	r	**AGC IF2 Gain Readout** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B n.u. Reset: 0_H
MIX2GAIN	0	r	**AGC MIX2 Gain Readout** 0_B 0 dB 1_B -15 dB Reset: 0_H

SPI Address Tracer Register

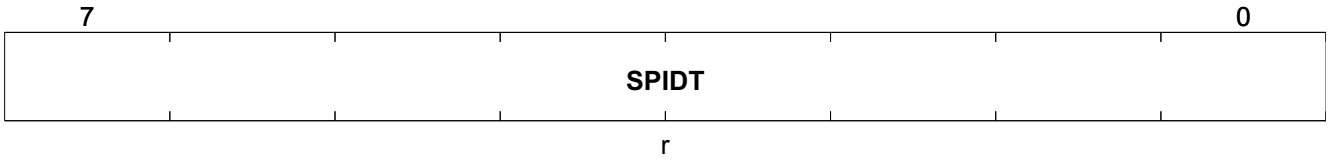
SPIAT	Offset	Reset Value
SPI Address Tracer Register	$0B3_H$	00_H



Field	Bits	Type	Description
SPIAT	7:0	r	**SPI Address Tracer, Readout of the last address of a SFR Register written by SPI** Reset: 00_H

SPI Data Tracer Register

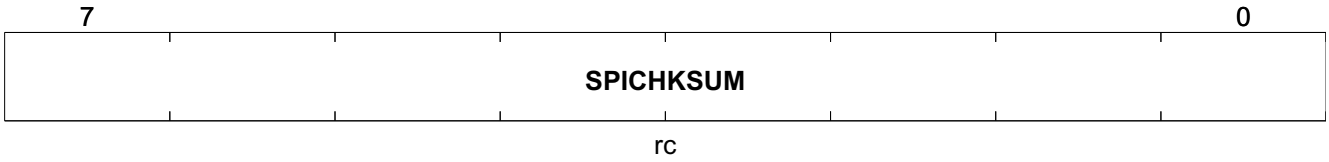
SPIDT | **Offset** | **Reset Value**
SPI Data Tracer Register | **0B4$_H$** | **00$_H$**



Field	Bits	Type	Description
SPIDT	7:0	r	**SPI Data Tracer, Readout of the last written data to a SFR Register by SPI** Reset: 00$_H$

SPI Checksum Register

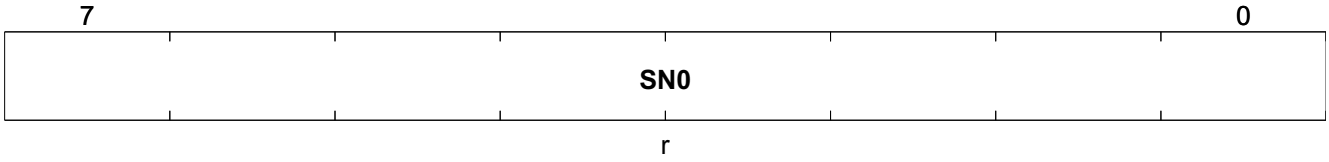
SPICHKSUM | **Offset** | **Reset Value**
SPI Checksum Register | **0B5$_H$** | **00$_H$**



Field	Bits	Type	Description
SPICHKSUM	7:0	rc	**SPI Checksum Readout** Reset: 00$_H$

Serial Number Register 0

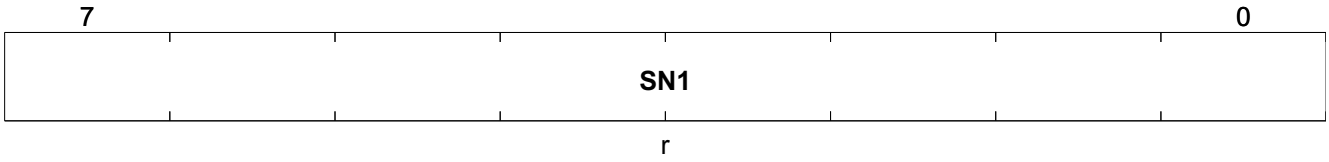
SN0 | **Offset** | **Reset Value**
Serial Number Register 0 | **0B6$_H$** | **00$_H$**



Field	Bits	Type	Description
SN0	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 1

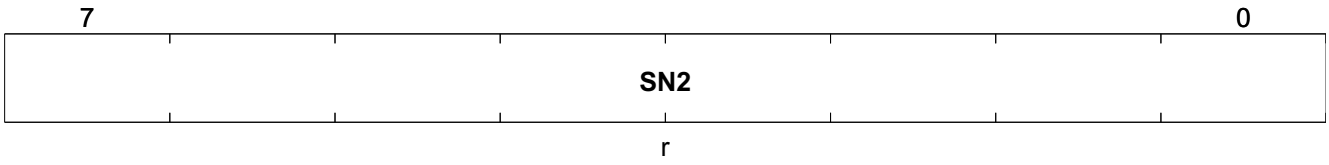
SN1	Offset	Reset Value
Serial Number Register 1	**$0B7_H$**	**00_H**



Field	Bits	Type	Description
SN1	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 2

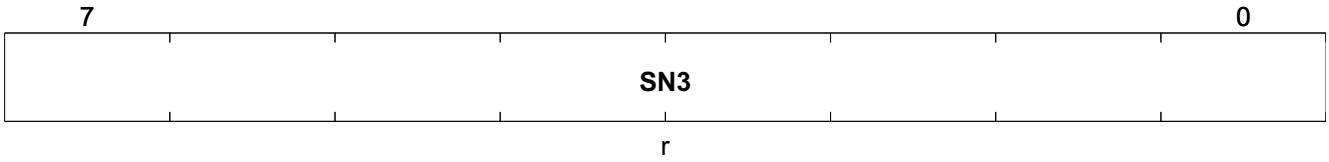
SN2	Offset	Reset Value
Serial Number Register 2	**$0B8_H$**	**00_H**



Field	Bits	Type	Description
SN2	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 3

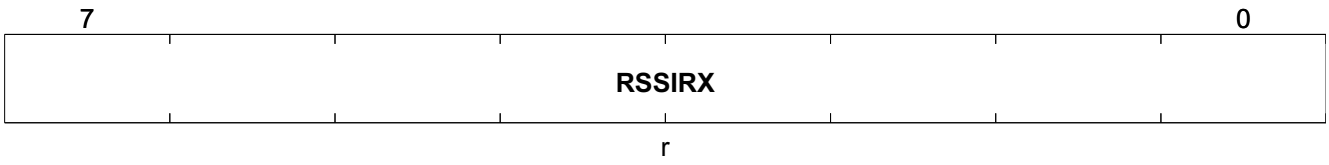
SN3	Offset	Reset Value
Serial Number Register 3	**$0B9_H$**	**00_H**



Field	Bits	Type	Description
SN3	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

RSSI Readout Register

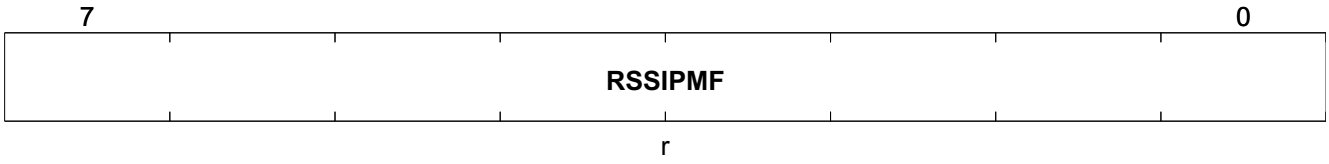
RSSIRX	Offset	Reset Value
RSSI Readout Register	**$0BA_H$**	**00_H**



Field	Bits	Type	Description
RSSIRX	7:0	r	**RSSI value after averaging over 4 samples** Reset: 00_H

RSSI Peak Memory Filter Readout Register

RSSIPMF	Offset	Reset Value
RSSI Peak Memory Filter Readout Register	**$0BB_H$**	**00_H**



Field	Bits	Type	Description
RSSIPMF	7:0	r	**RSSI Peak Memory Filter Level** Reset: 00_H

w w w . i n f i n e o n . c o m

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