TDA18218HN

DVB-T Silicon Tuner IC

Rev. 01 — 8 July 2009 Product data sheet

1. General description

The TDA18218HN is a Silicon Tuner IC designed for digital terrestrial (DVB-T) TV reception. The TDA18218HN integrates the overall tuning function, including selectivity and provides a low-IF output signal.

The TDA18218HN uses integrated IF filters to support 6 MHz, 7 MHz or 8 MHz channel bandwidths. The TDA18218HN requires only one single 16 MHz crystal for clock generation. A clock signal is available on crystal oscillator output pins (XTO_P / XTO_N) to synchronize the channel decoder.

The TDA18218HN is a low cost Silicon Tuner targeting digital terrestrial applications. The TDA18218HN matches the performance of the conventional can tuners. Additionally, the following benefits can be stated:

- Easy on-board integration
- Drastically reduces:
  - the size of the tuner function
  - the power consumption

2. Features

- Fully integrated IF selectivity; eliminating the need for external SAW filters
- Fully integrated oscillators with no external components
- Integrated wideband gain control
- Alignment free
- RF loop-through for easy implementation in the Set-Top Box (STB)
- Integrated die thermal sensor
- Single 3.3 V power supply
- Low power consumption (750 mW)
- Crystal oscillator output buffer (16 MHz) for single crystal applications
- I^2C-bus interface compatible with 3.3 V and 5 V microcontrollers
- Three Standby modes
- RoHS packaging

3. Applications

- DVB-T Set-Top Box (STB) and TV receiver
- System application optimization is described in the application note *AN0814*
- Driver application is described in the application note *AN0822*

4. Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option = 2 V (p - p); IF output load = 1 kΩ on each terminal

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	center of channel		174	-	864	MHz
NF_{tun}	tuner noise figure	normal mode; maximum gain		-	5	7	dB
φ_n	phase noise	worst case in the RF frequency range					
		10 kHz		-	–85	-	dBc/Hz
		100 kHz		-	–105	-	dBc/Hz
P	power dissipation			-	775	-	mW
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal		-	108	-	dBµV
α_{image}	image rejection	normal mode		-	65	-	dB
S_{dig}	digital sensitivity	DVB-T (64 QAM 2/3); BER = 2×10^{-4}	[1]	-	–82	-	dBm

[1] Measured with TDA10048 channel decoder.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18218HN	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

6. Block diagram

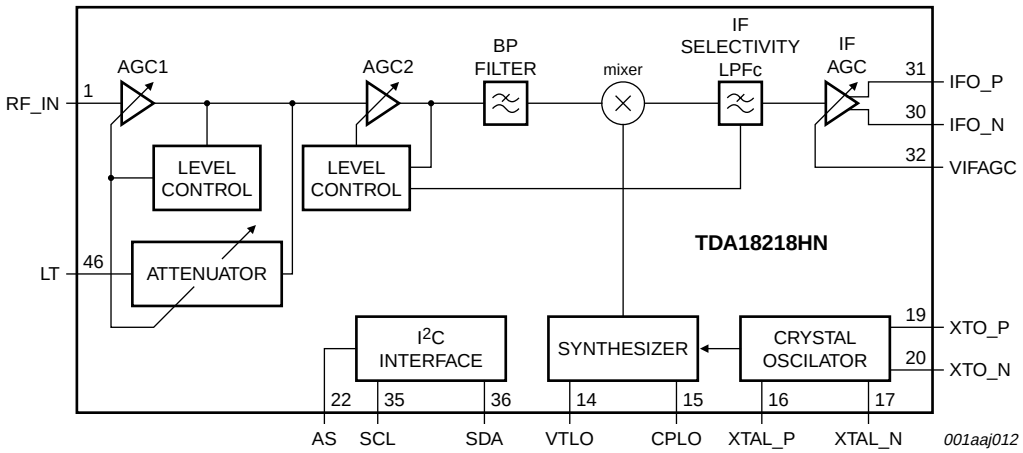


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

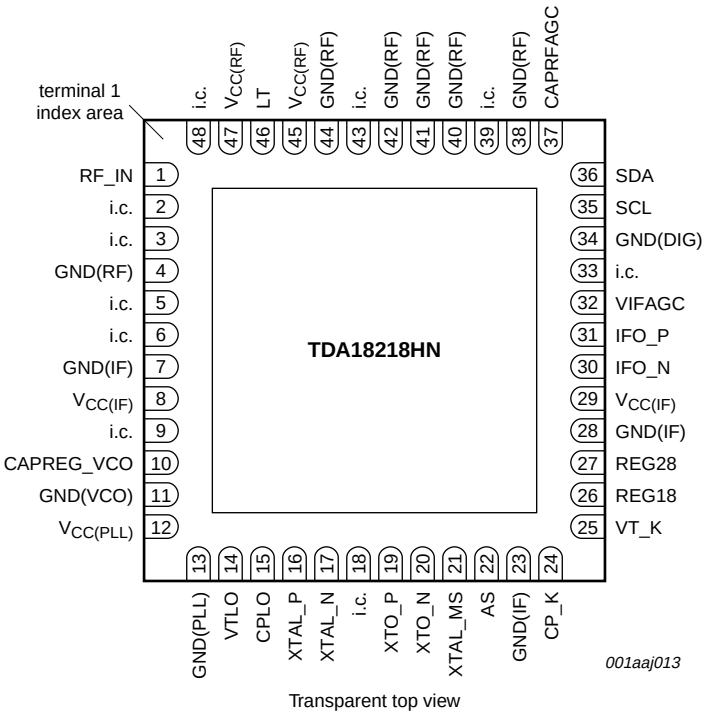


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
RF_IN	1	unbalanced RF input
i.c.	2	internally connected; leave open
i.c.	3	internally connected; leave open
GND(RF)	4	RF ground
i.c.	5	internally connected; leave open
i.c	6	internally connected; leave open
GND(IF)	7	IF ground
$V_{CC(IF)}$	8	IF supply voltage (3.3 V)
i.c.	9	internally connected; leave open
CAPREG_VCO	10	VCO supply decoupling
GND(VCO)	11	VCO ground
$V_{CC(PLL)}$	12	PLL supply voltage
GND(PLL)	13	PLL ground
VTLO	14	local oscillator (LO) tuning voltage input

Table 3. Pin description *...continued*

Symbol	Pin	Description
CPLO	15	charge pump of the LO synthesizer
XTAL_P	16	crystal oscillator input positive
XTAL_N	17	crystal oscillator input negative
i.c.	18	internally connected; leave open
XTO_P	19	crystal oscillator output buffer positive
XTO_N	20	crystal oscillator output buffer negative
XTAL_MS	21	XTAL out mode
AS	22	I^2C-bus address selection input
GND(IF)	23	IF ground
CP_K	24	charge pump of the calibration synthesizer
VT_K	25	tuning voltage of the calibration synthesizer
REG18	26	internal regulator decoupling
REG28	27	internal regulator decoupling
GND(IF)	28	IF ground
$V_{CC(IF)}$	29	IF supply voltage (3.3 V)
IFO_N	30	IF output negative
IFO_P	31	IF output positive
VIFAGC	32	IF gain control input
i.c.	33	internally connected; leave open
GND(DIG)	34	digital ground
SCL	35	I^2C-bus clock input
SDA	36	I^2C-bus data input and output
CAPRFAGC	37	RF AGC filtering
GND(RF)	38	RF ground
i.c.	39	internally connected; leave open
GND(RF)	40	RF ground
GND(RF)	41	RF ground
GND(RF)	42	RF ground
i.c.	43	internally connected; leave open
GND(RF)	44	RF ground
$V_{CC(RF)}$	45	RF supply voltage
LT	46	loop-through
$V_{CC(RF)}$	47	RF supply voltage
i.c.	48	internally connected; leave open

8. Functional description

The RF input signal is driven to a low-noise amplifier. It is then amplified and fed to the image rejection mixer. The mixer down-converts the RF signal to a low IF frequency, which depends on channel bandwidth (standard IF filters are implemented for 6 MHz, 7 MHz

and 8 MHz channel bandwidths). The TDA18218HN requires a single 16 MHz crystal for clock generation, a 16 MHz differential sine wave clock reference is available to drive a channel decoder.

8.1 AGC1 stage

The TDA18218HN embeds 2 different RF amplifiers with internal gain control.

The first stage, AGC1, behaves like a LNA (Low noise amplifier); its gain can take 4 different values (15 dB, 12 dB, 9 dB and 6 dB). Purpose of this amplifier is to ensure a low noise figure for the tuner.

In order to optimize noise and linearity performances an internal level detector selects the appropriate gain:

- If the signal level at the tuner is low, the gain is set to the maximum value (15 dB).
- If the signal level at the tuner input is high, the gain is set to the minimum value (6 dB).
- In between the gain is set to an intermediate value 12 dB or 9 dB.

The strategy of the level detection is a proprietary algorithm from NXP, managed by the driver.

It should be noted that:

1. The level detector measures the signal level within the complete RF frequency range, i.e. from 50 MHz to 870 MHz. Consequently, AGC1 gain is adapted to the complete RF power. If a strong signal is present at the tuner input, it will determine AGC1 gain (even if it is not the wanted signal). This concept prevents the tuner from overloading.
2. The level control is always operating.

8.2 AGC2 stage

The second stage, AGC2, is also an amplifier with a gain controlled thanks to a level detector.

The gain is controlled between –12 dB and +16.4 dB, it is adapted by steps of 0.2 dB.

It should be noted that:

1. The level control is always operating. Consequently, this amplifier is responsible for adapting the daily level changes.
2. The level detector measures the signal level within the complete RF frequency range (same as AGC1)

The strategy of the level detection is a proprietary algorithm from NXP, managed by the driver.

8.3 IF AGC

Finally, in order to adapt the tuner output level, a last amplifier is used (IF AGC). This amplifier delivers the appropriate level to the DVB-T channel decoder. The output level is therefore controlled thanks to the DC voltage applied on VIFAGC pin. This voltage is commonly delivered by the channel decoder.

It should be noted that the level control is always operating.

The strategy of the level detection has to be adapted for each type of channel decoder. It must be defined to satisfy ADC sampling (minimum level, ADC headroom).

All AGC amplifiers are controlled independently.

8.4 Power-down mode

The TDA18218HN can be programmed in Standby mode. The following blocks are turned off when programming a power-down:

- AGC2 and its level detector
- BP filter
- Mixer and VCO
- IF selectivity LPFc
- IF AGC

Remaining functions are:

- Loop-Through
- 16 MHz clock output (to drive a channel decoder)
- I^2C-bus Core (to wake-up the IC later on)

9. Control interface

9.1 I^2C-bus format, write and read mode

I^2C-bus uses two pins (SDA and SCL) to transfer information between devices connected to the bus. The SDA pin provides bidirectional data transfer. While the SCL pin provides the timing sequences. Data can be read and written as follows:

Write mode:

- Any register can be written to using its subaddress
- Any following (contiguous) registers can be written using the subaddress of the first register

Read mode:

- The read after Restart mode is not allowed. In addition, registers cannot be read using the subaddress of the register. However, registers can be read as follows:
  - from 00h to 16h
  - from 00h to 27h
  - from 00h to 3Ah
  - from 00h to any register subaddress, if MSB = 1 for the next register

Table 4. I²C-bus register map

Sub address	Register	Bit								Initial value (Hex)	POR (Hex)
		7 (MSB)	6	5	4	3	2	1	0 (LSB)		
	Address byte 1	1	1	0	0	0	MA[1:0]		R/W	-	-
	Address byte 2	0	0	AD[5:0]						-	-
00h	ID byte	1	ID[6:0]							C0[1]	C0
01h	Read byte 1	-	LO_Lock	CAL_Lock	-	TM_D[3:0]				88	80
02h	Read byte 2	-								00	00
03h	Read byte 3	AGC2[7:0]								8E	3C
04h	Read byte 4	AGC1[2]	-			LT[1:0]		AGC1[1:0]		03	00
05h	Read byte 5	-								00	00
06h	Read byte 6	-								00	00
07h	Main divider byte 1	-								D0	F0
08h	PSM byte 1	-								00	00
09h	Main divider byte 2	-								40	40
0Ah	Main divider byte 3	LO_Frac_0[31:24]								00	00
0Bh	Main divider byte 4	LO_Frac_1[23:16]								00	00
0Ch	Main divider byte 5	LO_Frac_2[15:12]				-				07	00
0Dh	Main divider byte 6	-								FF	01
0Eh	Main divider byte 7	-								84	84
0Fh	Main divider byte 8	-	Freq_prog_ Start	-						09	08
10h	Call divider byte 1	-								00	00
11h	Call divider byte 2	-								13	13
12h	Call divider byte 3	-								00	00

Table 4. I²C-bus register map *…continued*

Sub address	Register	Bit								Initial value (Hex)	POR (Hex)
		7 (MSB)	6	5	4	3	2	1	0 (LSB)		
13h	Call divider byte 4	-								00	00
14h	Call divider byte 5	-								01	01
15h	Call divider byte 6	-								84	84
16h	Call divider byte 7	-								09	09
17h	Power-down byte 1	-	pdLT	-		pdAGC1b	PD_RFAGC_Ifout	PD_LO_Synthe	SM	F0[2] B0[3]	B5
18h	Power-down byte 2	-	RFSW_MTO_LT_RFin	-			pdDETECT1	pdAGC2b	-	19[2] 59[3]	59
19h	XTOUT byte	-				XtOut[3:0]				0A	0A
1Ah	IF byte 1	-	IF_level[2:0]			-	BP_Filter[2:0]			8E	86
1Bh	IF byte 2	-						LP_Fc[1:0]		69	6A
1Ch	AGC2b byte	pulse_up_auto	pulse_up_width[1:0]		AGC_On	-				98	98
1Dh	PSM byte 2	TM_Range	TM_ON	-						01	C3
1Eh	PSM byte 3	-								00	00
1Fh	PSM byte 4	AGC1_Speed[1:0]		-			AGC1_aud_sel	AGC1_au_ptr[1:0]		58	58
20h	AGC1 byte 1	AGC2_RAM_sel[1:0]		AGC2_Gup_sel	AGC1_Gup_sel	Manual_LT	AGC1_aud[2:0]			10	00
21h	AGC1 byte 2	AGC2_Speed[1:0]		-	AGC1_Gud[4:0]					40	40
22h	AGC1 byte 3	-								8C	80
23h	AGC2 byte 1	-			AGC2_Gud[4:0]					00	00
24h	AGC2 byte 2	-								0C	0C
25h	Analog AGC byte	-				IFAGC_Top[3:0]				48	48
26h	RC byte	-								85	80
27h	RSSI byte	-								C9	8E

Table 4. I²C-bus register map *…continued*

Sub address	Register	Bit								Initial value (Hex)	POR (Hex)
		7 (MSB)	6	5	4	3	2	1	0 (LSB)		
28h	IR CAL byte 1	-								A7	F5
29h	IR CAL byte 2	-								00	30
2Ah	IR CAL byte 3	-								00	30
2Bh	IR CAL byte 4	-								00	00
2Ch	RF CAL byte 1	-								30	30
2Dh	RF CAL byte 2	-								81	80
2Eh	RF CAL byte 3	-								80	00
2Fh	RF CAL byte 4	-								00	00
30h	RF CAL byte 5	-								39	36
31h	RF CAL byte 6	-								00	00
32h	RF CAL byte 7	-								8A	8A
33h	RF CAL byte 8	-								00	00
34h	RF CAL byte 9	-								00	00
35h	RF CAL byte 10	-								00	00
36h	RF CAL RAM byte 1	-								00	00
37h	RF CAL RAM byte 2	-								00	00
38h	Margin byte	-								00	00
39h	Fmax byte 1	-								F6	F6
3Ah	Fmax byte 2	-								F6	F6

[1] See Section 9.2.1 “Device type address ID”.

[2] Case TDA18218HN is a device without LT.

[3] Case TDA18218HN is a device with LT.

9.2 I²C-bus address selection

The programmable module address bits MA[1:0] allow up to four tuners to be addressed in one system. Bits MA[1:0] are programmed by applying a specific voltage (V_{AS}) to pin AS. The relationship between the status of bits MA[1:0] and the voltage applied to pin AS is shown in Table 5.

Table 5. Address byte 1 bit descriptions

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	1 1000*	must be set to 1 1000
2 to 1	MA[1:0]	R/W		programmable address bit value set with V_{AS}
			00	V_{AS} = 0 V to 0.1 × V_{CC}
			01	V_{AS} = 0.2 × V_{CC} to 0.3 × V_{CC}
			10	V_{AS} = 0.4 × V_{CC} to 0.6 × V_{CC}
			11	V_{AS} = 0.9 × V_{CC} to V_{CC}
0	R/W	R/W	0	write mode
			1	read mode

Example: MA[1:0] = 00, R/W = 0, full module address = 1100 0000 (C0h).

Table 6. Address byte 2 bit descriptions

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 6	-	R/W	00*	must be set to 00
5 to 0	AD[5:0]	R/W	-	programmable address bits of the first programming byte

9.2.1 Device type address ID

Table 7. ID byte bit descriptions

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
00h	ID byte	7	-	R	1*	must be 1
		6 to 0	ID[6:0]	R	100 0000*	TDA18218HN device type address

9.3 Crystal buffer output

TDA18218HN embeds a Xtal oscillator and a buffer to drive another IC. The buffer can be configured through register XTOUT (I²C-bus sub address 19h). This buffer has been designed to be AC coupled. This output can be used in differential or sinusoidal mode (using XTO_N and XTO_P pins) or in asymmetrical or square mode (just leaving one pin open).

It should be noted that TDA18218HN specification refers to differential output with no load.

Table 8. Crystal buffer output register bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
19h	XTOUT byte	3 to 0	XtOut[3:0]	R/W		crystal buffer output
					0	XTAL off
					1	XTOUT off
					2	square wave 16 MHz
					7	sine wave 200 mV
					8	sine wave 400 mV
					9	sine wave 800 mV
					10	sine wave 1200 mV
					other	not applicable

9.4 Temperature sensor

Table 9. Temperature sensor bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
1Dh	PSM byte 2	6	TM_ON	W		temperature sensor on or off
					0	temperature sensor switched off
					1	temperature sensor switched on
		7	TM_Range	R/W		temperature range selection
					0	60 °C to 90 °C
					1	92 °C to 122 °C
01h	Read byte 1	3 to 0	TM_D[3:0]	R	-	die temperature[1]

[1] The die temperature can be read as shown in Table 10.

Table 10. Die temperature values

TM_D[3:0]	Temperature range selection (die temperature)	
	TM_RANGE = 0	TM_RANGE = 1
0000	60 °C	92 °C
0001	62 °C	94 °C
0010	66 °C	98 °C
0011	64 °C	96 °C
0100	74 °C	106 °C
0101	72 °C	104 °C
0110	68 °C	100 °C
0111	70 °C	102 °C
1000	90 °C	122 °C
1001	88 °C	120 °C
1010	84 °C	116 °C
1011	86 °C	118 °C
1100	76 °C	108 °C

Table 10. Die temperature values *…continued*

TM_D[3:0]	Temperature range selection (die temperature)	
	TM_RANGE = 0	TM_RANGE = 1
1101	78 °C	110 °C
1110	82 °C	114 °C
1111	80 °C	112 °C

9.5 Standby mode selection

Table 11. Standby mode selection

Mode	Power down byte 1 (address 17h)		
	SM (bit 0)	pdAGC1b (bit 3)	XTOUT
Device-off mode	1	1	see Table 8
Standby mode with loop-through and crystal oscillator on (default at POR), XTOUT 1200 mV	1	0	see Table 8
Standby mode with only crystal oscillator on	1	1	see Table 8

9.6 IF level

Refer to Table 21 “General characteristics for TV reception (RF input to IF output)”.

9.7 AGC and band-pass filters

Table 12. AGC and band-pass filter bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
03h	Read byte 3	7 to 0	AGC2[7:0]	R/W	-	AGC2 gain = 0.2 × (AGC2[7:0]) – 12 (dB) range = –12 dB to 16.4 dB
04h	Read byte 4	7 and 1 to 0	AGC1[2:0]	R/W		AGC1 gain range = 6 dB to 15 dB
					0	6 dB
					1	9 dB
					2	12 dB
					3	15 dB
1Ah	IF byte 1	2 to 0	BP_Filter[2:0]	W		band-pass filters
					3	filter 3 (174 MHz to 188 MHz)
					4	filter 4 (188 MHz to 253 MHz)
					5	filter 5 (253 MHz to 343 MHz)
					6	filter 6 (343 MHz to 870 MHz; bypass)
1Bh	IF byte 2	1 to 0	LP_Fc[1:0]	W		low-pass filter cut-off frequency
					0	6 MHz
					1	7 MHz
					2	8 MHz
1Ch	AGC2b byte	4	AGC_On	W		AGC1 and AGC2 clock on or off
					0	off
					1	on

9.8 RFin to LT path

Table 13. RFin to LT path bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
20h	AGC1 byte 1	3	Manual_LT	W		loop-through command
					0	sets LT attenuation depending on state of pin XTAL_MS; see Table 14
					1	sets LT attenuation manually; see Table 15
04h	Read byte 4	3 to 2	LT[1:0]	R/W	-	sets LT gain in range: –6 dB to –15 dB; see Table 15

Table 14. RFin to LT gain control modes

Bit Manual_LT	Pin XTAL_MS	AGC1 and LT attenuator gain modes
0	LOW	AGC1 gain fixed at 6 dB; LT gain set by LT[1:0]; see Table 15
0	HIGH	LT gain set automatically function of AGC1 gain; see Table 15
1	LOW	AGC1 gain fixed at gain set by AGC1[2:0]; LT gain set by LT[1:0]; see Table 15
1	HIGH	AGC1 gain set automatically; LT gain set by LT[1:0]; see Table 15

Table 15. Loop-through attenuator gain settings

LT[1]	LT[0]	Loop-through gain
0	0	–6 dB
0	1	–9 dB
1	0	–12 dB
1	1	–15 dB

9.9 PLL settings

Table 16. PLL bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	Main divider byte 3	7 to 0	LO_Frac_0[31:24]	R	-	LO frequency setting (kHz); in automatic mode
0Bh	Main divider byte 4	7 to 0	LO_Frac_1[23:16]			
0Ch	Main divider byte 5	7 to 4	LO_Frac_2[15:12]			
01h	Read byte 1	6	LO_Lock	R		LO lock flag
					0	PLL unlocked
					1	PLL locked
		5	CAL_Lock	R		calibration oscillator lock flag
					0	PLL unlocked
					1	PLL locked
0Fh	Main divider byte 8	6	Freq_prog_Start	W	1	launch automatic mode of PLL calculation (LO and calibration synthesizer); automatically reset to logic 0 (internally) when LO and calibration are completed

9.10 Power-down and switches

Table 17. Power-down and switches bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
17h	Power-down byte 1	6	pdLT	R/W		loop-through output switch
					0	closed
					1	open
		3	pdAGC1b			AGC1 power-down[1]
					0	LNA on
					1	LNA off
		2	PD_RFAGC_Ifout			mixer and IF stages power-down
					0	blocks on
					1	blocks off
		1	PD_LO_Synthe			LO synthesizer power-down
					0	PLL on
					1	PLL off
		0	SM			Standby mode; I^2C-bus interface, crystal oscillator and AGC1 are turned on
					0	normal
					1	standby
18h	Power-down byte 2	6	RFSW_MTO_LT_RFin	R/W		provides the RF signal to the loop-through[2]
					0	switch is open
					1	switch is closed
		2	pdDETECT1			AGC1 detector power-down
					0	detector on
					1	detector off
		1	pdAGC2b			AGC2 power-down[1]
					0	LNA on
					1	LNA off

[1] This setting controls the status of the Low Noise Amplifier (LNA).

[2] RFSW_MTO_LT_RFin = 0 in tuner applications with loop-through disabled.
RFSW_MTO_LT_RFin = 1 in tuner applications with loop-through enabled.

10. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.60	V

Table 18. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins SDA and SCL	–0.3	+5.5	V
		all other pins			
		V_{CC} < 3.3 V	–0.3	V_{CC} + 0.3	V
		V_{CC} > 3.3 V	–0.3	+3.6	V
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	+95	°C
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114 (human body model)	±2000	-	V
		EIA/JESD22-C101-C (FCDM) class III[1]	±200	-	V

[1] Class III: 200 V to 1000 V.

11. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	according to JEDEC specification 4L board with 16 thermal vias	-	29.9	-	K/W
T_{amb}	ambient temperature	-	0	-	+70	°C

12. Characteristics

Table 20. Loop-through characteristics (RF input to loop-through output)

T_{amb} = 25 °C, V_{CC} = 3.3 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{RF(lt)}$	loop-through RF frequency	center of channel		54	-	864	MHz
$\|s_{11}\|^2$	input return loss	75 Ω nominal impedance		-	–8	-	dB
$\|s_{22}\|^2$	output return loss	75 Ω nominal impedance		-	–8	-	dB
$G_{v(lt)}$	loop-through voltage gain	75 Ω load		-	–0.5	-	dB
ΔG_{lt}	loop-through gain variation	in the RF frequency range; 75 Ω load		-	2	4	dB
NF_{lt}	loop-through noise figure	maximum gain		-	6	-	dB
CSO_{lt}	loop-through composite second-order distortion		[1]	-	–51	-	dBc
CTB_{lt}	loop-through composite triple beat		[1]	-	–55	-	dBc
$\alpha_{isol(bp)}$	bypass isolation	from loop-through output to RF input		-	40	-	dB

[1] Channel loading assumptions: 129 channels at 75 dBµV.

Table 21. General characteristics for TV reception (RF input to IF output)

T_{amb} = 25 °C, V_{CC} = 3.3 V, IF output level option 2 V (p - p), IF output load = 1 kΩ on each pin; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.13	3.30	3.47	V
I_{CC}	supply current	normal mode	[1]	-	235[2]	270[3]	mA
		device-off mode		-	3	-	mA
		Standby mode with loop-through and crystal oscillator on (default at POR), XTOUT 1200 mV		-	60	-	mA
		Standby mode with only oscillator on		-	22	-	mA
P	power dissipation			-	775	-	mW
f_{RF}	RF frequency	center of channel		174	-	864	MHz
$f_{IF(nom)}$	nominal IF frequency	center of channel; for channel bandwidth					
		6 MHz		-	3	-	MHz
		7 MHz		-	3.5	-	MHz
		8 MHz		-	4	-	MHz
G_v	voltage gain	normal mode		70	76	-	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range	normal mode		-	63	-	dB
NF_{tun}	tuner noise figure	normal mode; maximum gain		-	5	7	dB
$V_{o(IF)dif(p-p)}$	peak-to-peak differential IF output voltage	IF_level[2:0] = 000		-	2	-	V
		IF_level[2:0] = 010		-	1	-	V
		IF_level[2:0] = 111		-	0.5	-	V
$Z_{o(IF)}$	IF output impedance	differential mode; magnitude value		-	100	-	Ω
$\Delta G_{AGC(IF)}$	IF AGC GAIN range	2 V (peak-to-peak) IF output voltage selection		-	30	-	dB
G_{tlt}	tilt gain	RF frequency range	[4]				
		6 MHz IF filter (1 MHz to 5.5 MHz)		-	-	4	dB
		7 MHz IF filter (1 MHz to 6.5 MHz)		-	-	4	dB
		8 MHz IF filter (1 MHz to 7.5 MHz)		-	-	4	dB
$f_{IF(stpb)lp}$	low-pass stop-band IF frequency	60 dB attenuation					
		6 MHz IF filter (1 MHz to 5.5 MHz)		-	12	-	MHz
		7 MHz IF filter (1 MHz to 6.5 MHz)		-	14	-	MHz
		8 MHz IF filter (1 MHz to 7.5 MHz)		-	16	-	MHz
α_{image}	image rejection	normal mode		-	65	-	dB
$t_{d(grp)}$	group delay time	normal mode					
		6 MHz IF filter (1 MHz to 5.5 MHz)		-	155	-	ns
		7 MHz IF filter (1 MHz to 6.5 MHz)		-	165	-	ns
		8 MHz IF filter (1 MHz to 7.5 MHz)		-	175	-	ns
φ_n	phase noise	worst case in the RF frequency range					
		10 kHz		-	–85	-	dBc/Hz
		100 kHz		-	–105	-	dBc/Hz
$t_{startup(tun)}$	tuner start-up time	at power-up		-	-	1	s

Table 21. General characteristics for TV reception (RF input to IF output) *…continued*

T_{amb} = 25 °C, V_{CC} = 3.3 V, IF output level option 2 V (p - p), IF output load = 1 kΩ on each pin; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{set}	setting time	channel change		-	-	60	ms
$f_{tun(step)}$	tuner frequency (step size)			-	1	-	kHz
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal		-	108	-	dBµV
S_{dig}	digital sensitivity	DVB-T (64 QAM 2/3); BER = 2×10^{-4}	[5]	-	–82	-	dBm

[1] XTAL buffer off.

[2] Measured at 3.3 V.

[3] Measured at 3.47 V.

[4] Difference defined between maximum and minimum over the IF bandwidth.

[5] Measured with TDA10048 channel decoder.

Table 22. Pin characteristics

T_{amb} = 25 °C, V_{CC} = 3.3 V; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IF AGC input: pin VIFAGC							
V_{AGC}	AGC voltage			0	-	V_{CC}	V
Z_i	input impedance		[1]	-	-	-	MΩ
dG_{AGC}/dV	rate of change of AGC gain with voltage			-	30	55	dB/V
Crystal oscillator							
f_{xtal}	crystal frequency			-	16	-	MHz
Z_i	input impedance	magnitude value; crystal specification: R_s = 150 Ω max; drive level < 100 µW		-	500	-	Ω
Crystal oscillator output buffer							
Square mode: only on XTO_N (XtOut[3:0] = 2)							
R_o	output resistance	16 MHz output frequency		-	90	-	Ω
$V_{o(p-p)}$	peak-to-peak output voltage	10 kΩ; 10 pF AC load; same load on XTO_P and XTO_N		-	0.6	-	V
SR_r	slew rate of rising signal	10 kΩ; 10 pF AC load		-	150	-	V/µs
SR_f	slew rate of falling signal	10 kΩ; 10 pF AC load		-	80	-	V/µs
Sinusoidal mode: on XTO_P and XTO_N (XtOut[3:0] = 8)							
R_o	output resistance	16 MHz output frequency		-	480	-	Ω
$V_{o(p-p)}$	peak-to-peak output voltage	10 kΩ; 10 pF AC load; same load on XTO_P and XTO_N		-	0.4	-	V
Digital levels I²C-bus	[2]						
Pin SCL							
V_{IL}	LOW-level input voltage	fixed input levels		-	-	1.5	V
		V_{DD} related input levels		-	-	$0.3 \times V_{CC}$	V
V_{IH}	HIGH-level input voltage	fixed input levels		3	-	-	V
		V_{DD} related input levels		$0.7 \times V_{CC}$	-	-	V

Table 22. Pin characteristics *…continued*

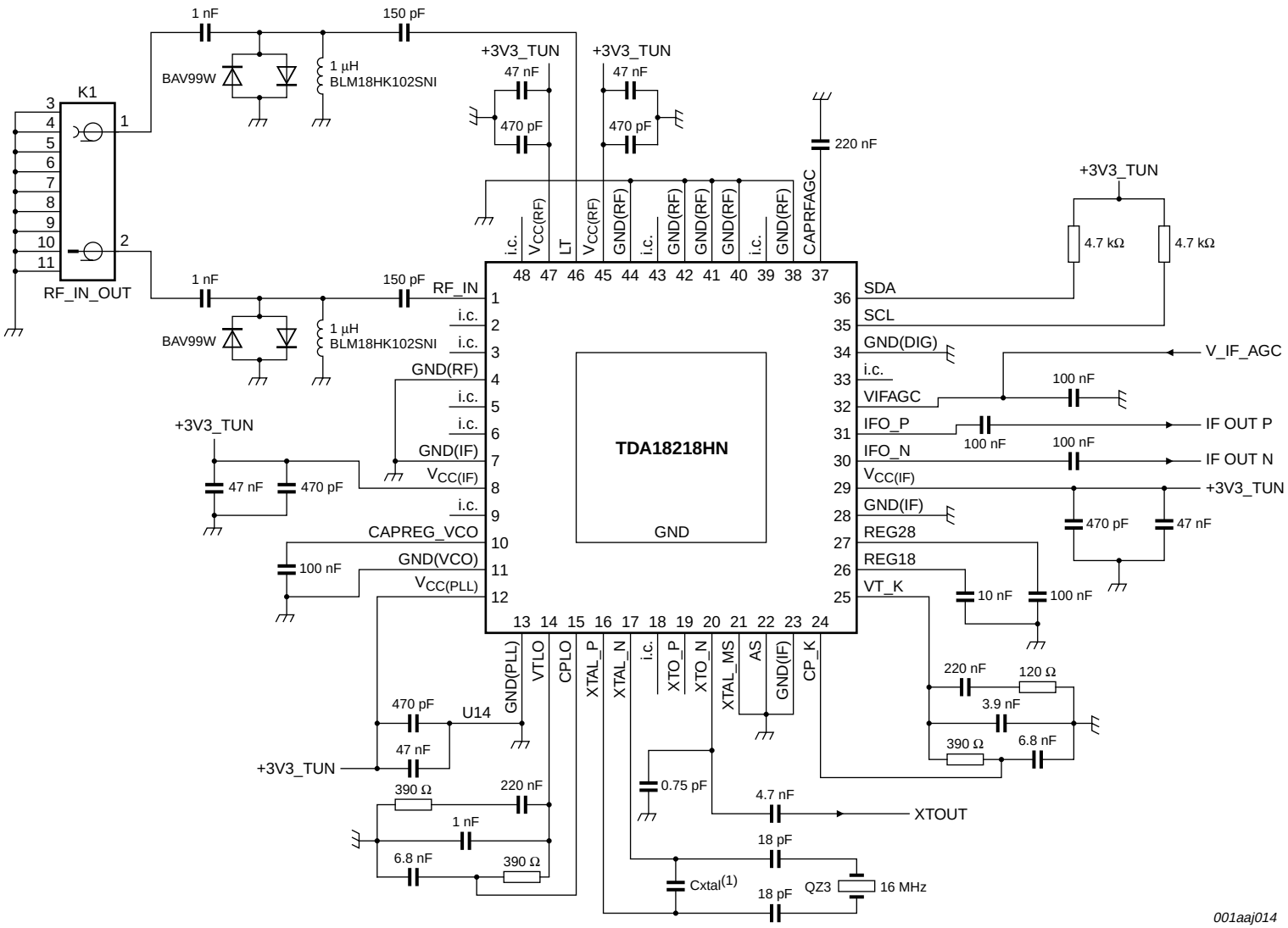
T_{amb} = 25 °C, V_{CC} = 3.3 V; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	400	kHz
pin SDA						
V_{OH}	HIGH-level output voltage	I_{SDA} = 3 mA (sink current)	-	-	0.4	V
V_{IL}	LOW-level input voltage	fixed input levels	-	-	1.5	V
		V_{DD} related input levels	-	-	$0.3 \times V_{CC}$	V
V_{IH}	HIGH-level input voltage	fixed input levels	3	-	-	V
		V_{DD} related input levels	$0.7 \times V_{CC}$	-	-	V

[1] Typical value is HIGH impedance input.

[2] Devices that use non-standard supply voltages, which do not conform to the intended I^2C-bus system levels, must relate their input levels to the supply voltage to which the pull-up resistors are connected.

13. Application information

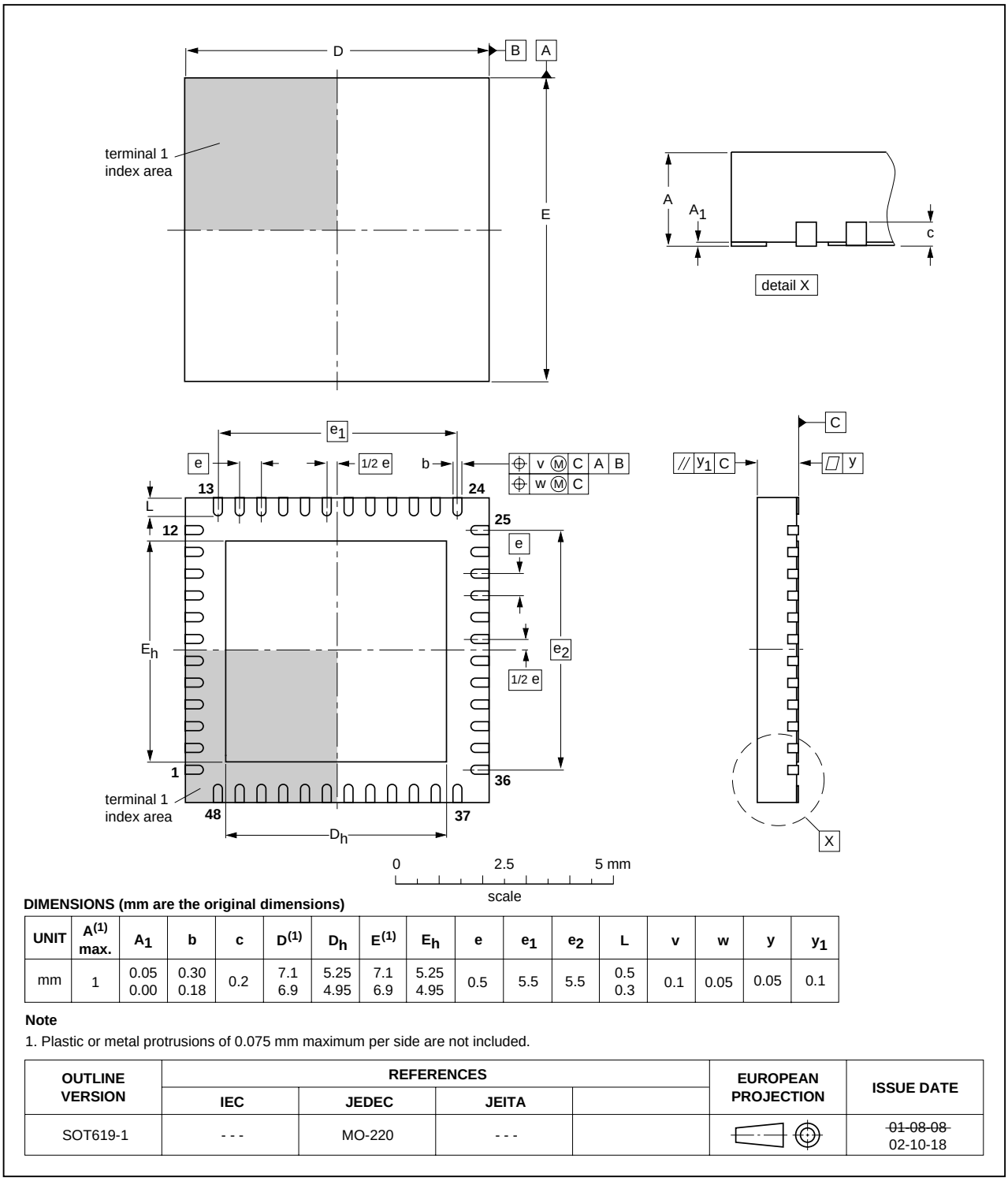


(1) Cxtal not connected for NDK; Cxtal = 1.5 pF for Siward.

Fig 3. Application diagram

14. Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.25 4.95	7.1 6.9	5.25 4.95	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 4. Package outline HVQFN48 - SOT619-1

15. Abbreviations

Table 23. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BER	Bit Error Rate
BP	Band-Pass
Cxtal	crystal Capacitor
DVB-T	Digital Video Broadcasting – Terrestrial
DVR	Digital Video Recorder
FCDM	Flow Control Decision Message
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LPFc	Low Pass Frequency cut
LO	Local Oscillator
LT	Loop-Through
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
POR	Power-On Reset
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
SAW	Surface Acoustic Wave
STB	Set-Top Box
TOP	Take-Over Point
VCO	Voltage Controlled Oscillator
XTAL	Crystal

16. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA18218HN_1	20090708	Product data sheet	-	-

17. Legal information

18. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Tables

21. Figures

22. Contents

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