TCAN1043x-Q1 Fault Protected CAN Transceiver with CAN FD

ADVANCE INFORMATION

1 Features

- AEC Q100: Qualified for Automotive Applications
- Meets the Requirements of the ISO11898-2 (2016)
- All Devices Support Classic CAN and 2 Mbps CAN FD (Flexible Data Rate) and "G" Options Support 5 Mbps
  - Short and Symmetrical Propagation Delay Times and Fast Loop Times for Enhanced Timing Margin
  - Higher Data Rates in Loaded CAN Networks
- V_{IO} Level Shifting Supports 2.8 V to 5.5 V
- Operating Modes
  - Normal Mode
  - Low Power Sleep Mode with INH Output and Local and Remote Wake up Request
- Ideal Passive Behavior When Unpowered
  - Bus and Logic Terminals are High Impedance (No Load to Operating Bus or Application)
  - Power Up or Down Glitch Free Operation
- Excellent EMC Performance
  - IEC 62228 – 2007 Compliant
  - SAE J2962-2 Compliant
- Protection Features
  - ESD Protection of Bus Terminals
    - HBM ESD Protection: ±10 kV
    - IEC ESD Protection up to ±8 kV
  - Bus Fault Protection: ±58 V (non-H variants) and ±70 V (H variants)
  - Undervoltage Protection on Supply Terminals
  - TXD Dominant Time Out (DTO)
  - Thermal Shutdown Protection
- Receiver Common Mode Input Voltage: ±30 V
- Typical Loop Delay: 110 ns
- Junction Temperatures from –55°C to 150°C
- Available in SOIC (14) Package and Leadless VSON (14) package (4.5 mm x 3.0 mm) with Improved Automated Optical Inspection (AOI) Capability

2 Applications

- 12 V and 24 V System Applications
- Automotive and Transportation
  - Body Control Module & Gateway
  - Head Unit
  - Radar
  - Telematics
  - Cluster
  - HMI & Display

3 Description

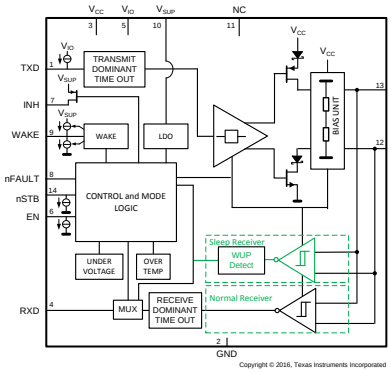
The TCAN1043xx-Q1 meets the specifications of the ISO11898–2 (2016) High Speed Controller Area Network (CAN) Physical Layer standard. The device is designed for use in CAN FD networks up to 2 megabit per second (Mbps). Devices with part numbers that include the suffix “G” are designed for data rates up to 5 Mbps. The device has a remote wake request feature via the CAN bus pins and a local wake request feature via the high voltage WAKE terminal. Additionally, the device has the ability to control the system power via the high voltage output INH terminal. The device includes many protection features providing device and CAN network robustness.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCAN1043x-Q1	SOIC (14)	8.95 mm × 3.91 mm
	VSON (14)	4.5 mm x 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

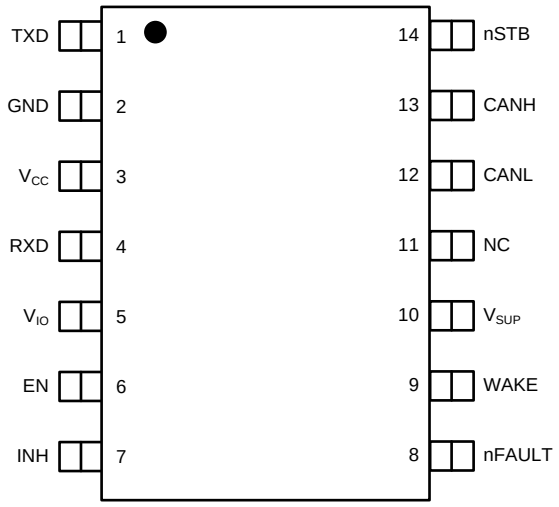
DATE	REVISION	NOTES
October 2017	*	Initial release.

5 Device Comparison Table

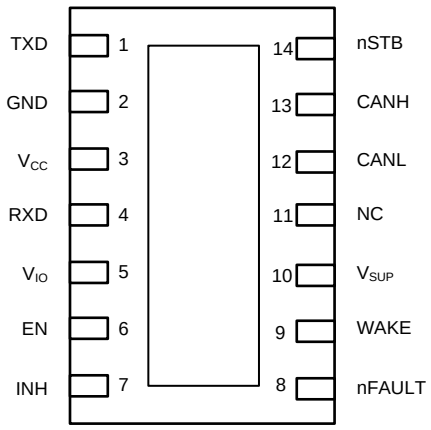
DEVICE NUMBER	BUS FAULT PROTECTION	MAXIMUM DATA RATE
TCAN1043-Q1	±58 V	2 Mbps
TCAN1043H-Q1	±70 V	2 Mbps
TCAN1043G-Q1	±58 V	5 Mbps
TCAN1043HG-Q1	±70 V	5 Mbps

6 Pin Configurations and Functions

D Package
14 Pin (SOIC)
Top View



DMT Package
14 Pin (VSON)
Top View



Pin Functions

PINS		TYPE	DESCRIPTION
NAME	NO		
TXD	1	Digital Input	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	GND	Ground connection
V_{CC}	3	Supply	5-V CAN bus supply voltage
RXD	4	Digital Output	CAN receive data output (LOW for dominant and HIGH for recessive bus states), tri-state™
V_{IO}	5	Supply	I/O supply voltage
EN	6	Digital Input	Mode control input, Enable Input, integrated pull down
INH	7	High Voltage Output	Inhibit Output, controls system voltage regulators and supplies
nFAULT	8	Digital Output	Fault Output, inverted logic
WAKE	9	High Voltage Input	Wake Input terminal, high voltage input
V_{SUP}	10	Supply	Reverse Blocked Battery supply input
NC	11	—	No Connect (Not Internally Connected)
CANL	12	Bus I/O	Low level CAN bus input/output line
CANH	13	Bus I/O	High level CAN bus Input/output line
nSTB	14	Digital Input	Mode control input, Standby input, integrated pull down

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7 Specifications

7.1 Absolute Maximum Ratings (1) (2)

			MIN	MAX	UNIT
V_{SUP}	Battery supply (reverse blocked) voltage range – standard versions		–0.3	58	V
	Battery supply (reverse blocked) voltage range – H versions		–0.3	70	
V_{CC}	5-V bus supply voltage range		–0.3	7	
V_{IO}	I/O Level Shifting Voltage Range		–0.3	7	
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices without the "H" suffix	–58	58	
	CAN Bus I/O voltage range (CANH, CANL)	Devices with the "H" suffix	–70	70	
$V_{(DIFF)}$	Max Differential voltage between CANH and CANL	Devices without the "H" suffix	–58	58	
		Devices with the "H" suffix	–70	70	
$V_{(Logic\_Input)}$	Logic input terminal voltage range		–0.3	7	
$V_{(Logic\_Output)}$	Logic output terminal voltage range		–0.3	7	
V_{INH}	INH output pin voltage range	Devices without the "H" suffix	–0.3	58 and $V_O \le V_{SUP} + 0.3$	
	INH output pin voltage range	H versions	–0.3	70 and $V_O \le V_{SUP} + 0.3$	
$V_{(WAKE)}$	WAKE input pin voltage range	Devices without the "H" suffix	–0.3	58 and $V_I \le V_{SUP} + 0.3$	
	WAKE input pin voltage range	H versions	–0.3	70 and $V_I \le V_{SUP} + 0.3$	
$I_{O(LOGIC)}$	Logic output current	RXD, and nFAULT		8	mA
$I_{O(INH)}$	INH output current			4	
$I_{O(WAKE)}$	Wake current if due to ground shifts $V_{(WAKE)} \le V_{(GND)} – 0.3$ V, thus the current into WAKE must be limited via an external serial resistor			3	
T_J	Operating virtual junction temperature range		–55	150	°C
T_A	Ambient temperature range		–55	125	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	V_{SUP}, INH	±4000	V
			All pins, except V_{SUP}, INH (1)	±6000	
			CAN bus terminals (CANH, CANL) (2)	±16000	
		Charged device model (CDM)	All terminals (3)	±750	
		Machine Model (MM)	All terminals (4)	±200	

(1) Tested in accordance to AEC-Q100-002.
(2) Test method based upon AEC-Q100-002, CAN bus terminals stressed with respect to each other and to GND.
(3) Tested in accordance to AEC-Q100-011.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115A.

7.3 ESD Ratings IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
			SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
			IEC 61000-4-2 (150 pF, 330 Ω) Unpowered Contact Discharge	±8000	
		V_{BAT} and WAKE		±6000	
	ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification (1)	CAN bus terminals (CANH, CANL) to GND, V_{SUP}, WAKE	Pulse 1	–100	
			Pulse 2	+75	
			Pulse 3a	–150	
			Pulse 3b	+100	
	ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND, V_{SUP}, WAKE	Direct Coupling Capacitor "Slow Transient Pulse" with 100 nF coupling capacitor - Powered	±85	

(1) ISO7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations will lead to different results.

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7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Battery supply (reverse blocked) voltage range	4.5		60	V
V_{CC}	5V Supply Voltage	4.5		5.5	V
	Supply voltage range – by char CAN functionality to support cold crank events	4		4.5	V
V_{IO}	I/O supply voltage	2.8		5.5	V
$I_{OH(ILOGIC)}$	Logic terminal HIGH level output current – RXD and nFAULT	–2			mA
$I_{OL(LOGIC)}$	Logic terminal LOW level output current – RXD and nFAULT			2	mA
$I_{O(INH)}$	INH output current			1	mA
$C_{(VCC)}$	V_{CC} supply capacitor		100		nF
$C_{(VIO)}$	V_{IO} supply capacitor		100		nF
$C_{(VSUP)}$	V_{SUP} supply capacitor		100		nF
T_A	Operational free-air temperature (see Thermal Information) - standard version	–40		125	°C
	Operational free-air temperature (see Thermal Information) - H version	–55		125	°C

7.5 Thermal Information

THERMAL METRIC[1]		TEST CONDITIONS	TCAN1043x-Q1	TCAN1043x-Q1	UNIT
			D (SOIC)	DMT (VSON)	
			14 Pins	14 Pins	
$R_{\theta JA}$	Junction-to-air thermal resistance	Low-K thermal resistance	–	–	°C/W
		High-K thermal resistance	78	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		34.7	10.8	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance		33.6	30.5	°C/W
$R_{\theta JC(BOT)}$	Junction-to-case (bottom) thermal resistance		–	1.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		5.7	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		34.3	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Dissipation Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, V_{IO} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_{L_RXD} = 15 pF.	TBD	mW
		V_{CC} = 5.5 V, V_{IO} = 5 V, T_J = 150°C, R_L = 60 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_{L_RXD} = 15 pF.	TBD	mW
T_{TSD}	Thermal shutdown temperature		170	°C
T_{TSD_HYS}	Thermal shutdown hysteresis		10	°C

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7.7 Electrical Characteristics

Over recommended operating conditions with T_A = –55°C to 150°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY CHARACTERISTICS							
I_{SUP}	Supply current	Normal, Silent, Go to Sleep	Normal, Silent, Go to Sleep		40	70	µA
		Standby Mode	Standby mode, V_{CC} > 4.5 V, V_{IO} > 2.8 V, $V_{(INH)} = V_{(WAKE)} = V_{SUP}$		15	45	
		Sleep Mode	Sleep mode, $V_{CC} = V_{IO} = V_{(INH)}$ = 0 V $V_{(WAKE)} = V_{SUP}$		15	30	
I_{CC}	Supply Current Normal Mode	Dominant	See Figure 8. TXD = 0 V, R_L = 60 Ω, C_L = open. Typical Bus Load.			70	mA
			See Figure 8. TXD = 0 V, R_L = 50 Ω, C_L = open. High Bus Load.			80	
		Dominant with bus fault	See Figure 8. TXD = 0 V, CANH = -25 V, R_L = open, C_L = open			180	
	Supply Current Normal Mode	Recessive	See Figure 8. TXD = V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open			5	mA
	Supply Current Silent and Go to Sleep Mode		See Figure 8. TXD = V_{IO}, R_L = 50 Ω, C_L = open			2.5	mA
	Supply current Standby Mode		See Figure 8. EN = L, NSTB = L			5	µA
	Sleep Mode		See Figure 8. EN = H or L, NSTB = L			5	
I_{IO}	I/O Supply Current	Normal Mode	RXD floating. TXD = 0 V (dominant) nSTB = V_{IO}, EN = V_{IO}			450	µA
		Normal, Silent or Go to Sleep Mode	RXD floating. TXD = V_{IO} recessive			5	
		Sleep Mode	NSTB = L			5	
UV_{SUP}	Undervoltage detection on V_{SUP} for protected mode			3.0		4.2	V
$V_{HYS(UVSUP)}$	Hysteresis voltage on UV_{SUP}				50		mV
UV_{VCC}	Rising undervoltage detection on V_{CC} for protected mode				4.1	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.5	3.9		
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for protected mode			1.3		2.75	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				80		mV
Driver Electrical Characteristics							
$V_{O(D)}$	Bus output voltage (dominant) - normal mode	CANH	See and Figure 20 and Figure 19. TXD = 0 V, Normal mode 50 ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	
$V_{O(R)}$	Bus output voltage (recessive)	CANH and CANL	See Figure 20 and Figure 19. TXD = V_{CC}, $V_{IO} = V_{CC}$, normal or silent , R_L = open (no load), R_{CM} = open	2	0.5 × V_{CC}	3	V
$V_{OD(D)}$	Differential output voltage (dominant)	CANH - CANL	See Figure 20 and Figure 19. TXD = 0 V, Normal mode, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	V
			See Figure 20 and Figure 19. TXD = 0 V, Normal mode, 45 Ω ≤ R_L ≤ 50 Ω, CL = open, R_{CM} = open	1.4		3	
			See Figure 20 and Figure 19. TXD = 0 V, Normal mode, R_L = 2240 Ω, C_L = open, R_{CM} = open	1.5		5	
			See Figure 20 and Figure 19. TXD = 0 V, Normal mode, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, R_{CM} = open (optional)	1.4		3.3	
$V_{OD(R)}$	Differential output voltage (recessive)	CANH - CANL	See Figure 20 and Figure 19. TXD = V_{CC}, normal or silent mode, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
			See Figure 20 and Figure 19. TXD = V_{CC}, normal or silent mode, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		See Figure 6 and Figure 29, normal mode, R_{TERM}/2 = 30Ω(split), C_{split} = 4.7nF, C_L = open, R_{CM} = open, TXD = 1MHz	0.9		1.1	V/V

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V. For dual supply devices V_{IO} = 3.3 V. R_L = 60 Ω.

ADVANCE INFORMATION

Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 150°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{SYM_DC}	Output symmetry (dominant or recessive)		See Figure 6 and Figure 21,normal or silent mode, R_L = 60 Ω, C_L = open, R_{CM} = open; $V_{SYM} = V_{CC} - V_{O(CANH)} - V_{O(CANL)}$	–400		400	mV
$I_{OS(DOM)}$	short circuit steady-state output current, Dominant		See Figure 20 and Figure 12 V_{CANH} = -5 V, CANL = open, TXD = 0 V	–100			mA
			See Figure 20 and Figure 12, V_{CANL} = 40 V, CANH = open, TXD = 0 V			100	
$I_{OS(REC)}$	Short circuit steady-state output current, Recessive		See Figure 20 and Figure 12, –27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = CANH = CANL, TXD = V_{IO}	–5		5	mA
$V_{O(STB)}$	Bus output voltage (Standby mode)	CANH	STB = V_{CC} or V_{IO}, R_L = open, R_{CM} = open	–0.1	0	0.1	V
		CANL		–0.1	0	1	
		CANH-CANL		–0.2	0	0.2	
Receiver Electrical Characteristics							
V_{CM}	Common Mode Range: Normal, and Silent modes		See Figure 7 and Table 5	-30		30	V
V_{IT}	Input threshold voltage, Normal mode and Silent modes		See Figure 7 and Table 5, V_{CM} ≤ ±20 V	500		900	mV
			See Figure 7 and Table 5, V_{CM} ≤ ±30 V	400		1000	
V_{HYS}	Hysteresis voltage for input threshold, Normal and Silent modes		See Figure 7 and Table 5		120		
$V_{IT(Sleep)}$	Input Threshold, standby mode		See and Table 5	400		1150	mV
V_{CM}	Common Mode Range: Standyby, Go-to-Sleep and Sleep modes		See Figure 7 and Table 5	-12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current		CANH = CANL = 5 V, V_{CC} to GND via 0 ohm or 47 kΩ resistor. V_{IO} = to GND via 0 Ω or 47 kΩ resistor. V_{SUP} = 0 V (47 kΩ case by characterization and design)			4.8	µA
C_I	Input capacitance to ground (CANH or CANL)		By Characterization and Design		24	30	pF
C_{ID}	Differential input capacitance		By Characterization and Design		12	15	
R_{ID}	Differential input resistance		TXD = V_{CC} = V_{IO}, Normal mode; -30 ≤ V_{CM} ≤ +30V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)			15		40	
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%		$V_{(CANH)}$ = $V_{(CANL)}$ = 5V	–2		2	%
R_{CBF}	Valid Differential load impedance range for bus fault circuitry		R_{CM} = R_L, C_L = open	45		70	Ω
TXD TERMINAL (CAN TRANSMIT DATA INPUT)							
V_{IH}	High level input voltage			0.7 V_{IO}			V
V_{IL}	Low level input voltage					0.3 V_{IO}	V
I_{IH}	High level input leakage current		TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low level input leakage current		TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–100		–5	µA
$I_{LKG(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_I	Input Capacitance		V_{IN} = 0.4 x sin(2 x π x 2E + 6 x t) + 2.5 V		5		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)							
V_{OH}	High level output voltage		See Figure 5, I_O = –2 mA.	0.8 V_{IO}			V
V_{OL}	Low level output voltage – IO level shifting version		See Figure 5, I_O = 2 mA.			0.2 V_{IO}	V
nFAULT TERMINAL (FAULT AND STATUS OUTPUT)							
V_{OH}	High level output voltage		See Figure 5, I_O = –2 mA.	0.8 V_{IO}			V
V_{OL}	Low level output voltage – IO level shifting version		See Figure 5 I_O = 2 mA.			0.2 V_{IO}	V
nSTB TERMINAL (STANDBY MODE INPUT)							
V_{IH}	High level input voltage			0.7 V_{IO}			V
V_{IL}	Low level input voltage					0.3 V_{IO}	V
I_{IH}	High level input leakage current		nSTB = V_{CC} = V_{IO} = 5.5 V	1		10	µA
I_{IL}	Low level input leakage current		nSTB = 0 V, V_{CC} = V_{IO} = 5.5 V	–1		1	µA

ADVANCE INFORMATION

Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{LKG(OFF)}$	Unpowered leakage current	nSTB = 5.5 V, V_{CC} = 0V, V_{IO} = 0 V	–1	0	1	µA
EN TERMINAL (ENABLE MODE INPUT)						
V_{IH}	High level input voltage		0.7 V_{IO}			V
V_{IL}	Low level input voltage				0.3 V_{IO}	V
I_{IH}	High level input leakage current	EN = V_{CC} = V_{IO} = 5.5 V	1		10	µA
I_{IL}	Low level input leakage current	EN = 0 V, V_{CC} = V_{IO} = 5.5 V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	EN = 5.5 V, V_{CC} = 0V, V_{IO} = 0 V	–1	0	1	µA
INH TERMINAL (INHIBIT OUTPUT)						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = –0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current	INH = 0 V, Sleep Mode	-5		5	µA
Wake TERMINAL (WAKE INPUT)						
V_{IH}	High level input voltage	Standby and Sleep Mode	V_{SUP} - 2			V
V_{IL}	Low level input voltage	Standby and Sleep Mode			V_{SUP} - 3	V
I_{IH}	High level input current	WAKE = V_{SUP} – 1 V	–25	–15		µA
I_{IL}	Low level input current	WAKE = 1 V		15	25	µA

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7.8 Switching Characteristics

Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, High TXD to Driver Recessive	See Figure 15, Normal mode. R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		50	TBD	ns
t_{pLD}	Propagation delay time, Low TXD to Driver Dominant			40	TBD	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			10	TBD	ns
t_R	Differential output signal rise time			45	TBD	µs
t_F	Differential output signal fall time			45	TBD	µs
t_{TXD_DTO}	Dominant Time Out(2)	See Figure 14, R_L = 60 Ω, C_L = open	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus recessive input to high RXD	See Figure 14, $C_{L(RXD)}$ = 15 pF Char Range: TBD if wider range needed to look at. Typical Conditions for DS: CANL = 1.5 V, CANH = 4 V.		50	TBD	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			50	TBD	ns
t_R	Output signal rise time (RXD)			8	TBD	ns
t_F	Output signal fall time (RXD)			8	TBD	ns
t_{BUS_DOM}	Dominant time out	See Figure 17, R_L = 60 Ω, C_L = open	1.4		3.8	ms
t_{CBF}	Bus fault detection time	45 Ω ≤ R_{CM} ≤ 70 Ω, C_L = open	1.9			µs
Wake Terminal (Wake input)						
t_{WAKE_HT}	WAKE hold time	Time required for LWU from a H to L or L to H on WAKE	5		50	µS
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal Mode, See Figure 17, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	175	ns
t_{MODE1}	Mode change time	See Figure 15 and Figure 16. Mode change time for leaving Sleep Mode to entering normal and silent mode after V_{CC} and V_{IO} have crossed UV thresholds			20	µs
t_{MODE2}	Mode change time	Mode changes between Normal, Silent and Standby Modes, and Sleep to Standby Mode transition			10	µs
$t_{UV\_RE-ENABLE}$	Re-enable time after UV event	Time for device to return to normal operation from UV_{VCC} or UV_{VIO} under voltage event			200	µs
t_{Power_Up}	Power up time on V_{SUP}	See Figure 16		250		µs
t_{WK_FILTER}	Bus time to meet Filtered Bus Requirements for Wake Up Request	See Figure 17, sleep mode.	0.5		1.85	µs
$t_{WK\_TIMEOUT}$	Bus Wake-up timeout value		0.5		2	ms
t_{UV}	Undervoltage filter time for V_{IO} and V_{CC}	V_{IO} ≤ UV_{VIO} or V_{CC} < UV_{VCC}	159		340	ms
$t_{Go\_To\_Sleep}$	Minimum hold time for transition to sleep mode	EN = H and nSTB = L	5		50	µs
FD Timing Parameters						

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V. For dual supply devices V_{IO} = 3.3 V. R_L = 60 Ω.
(2) The TXD dominant timeout ($t_{(TXD\_DTO)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(TXD\_DTO)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(TXD\_DTO)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(TXD\_DTO)}$

ADVANCE INFORMATION

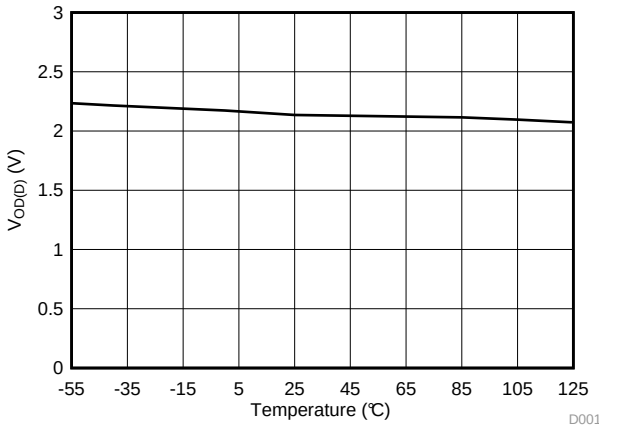
Switching Characteristics (continued)

Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns, all devices	Normal Mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		155		210	
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns, all devices		400		550	
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		120		220	
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns, all devices		-65		40	
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns, G device variants only		-45		15	

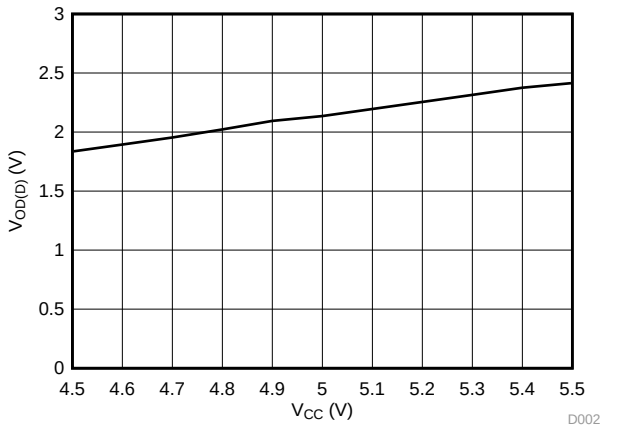
ADVANCE INFORMATION

7.9 Typical Characteristics



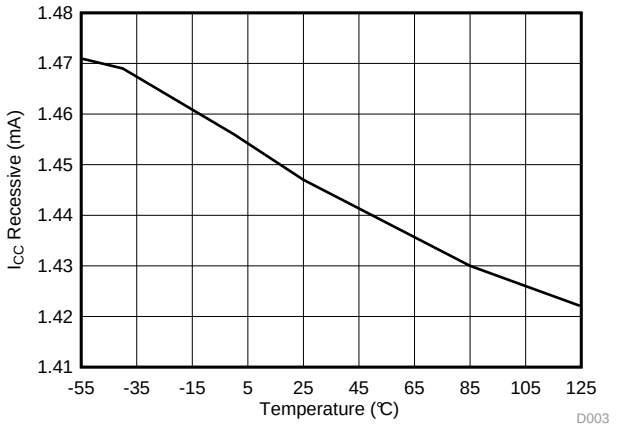
V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = Open | RCM = Open | STB = 0 V

Figure 1. $V_{OD(D)}$ over Temperature



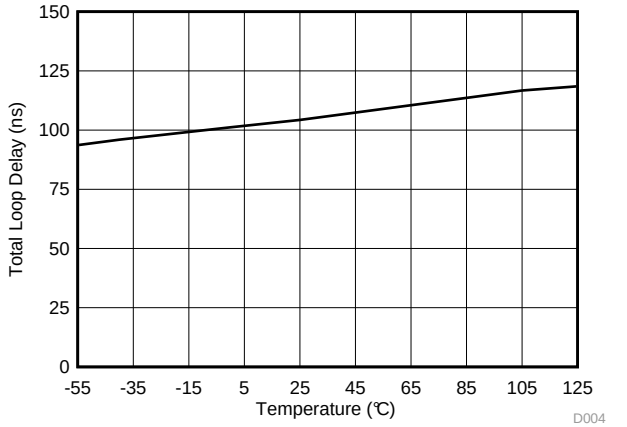
V_{IO} = 5 V | STB = 0 V | R_L = 60 Ω
C_L = Open | RCM = Open | Temp = 25°C

Figure 2. $V_{OD(D)}$ over V_{CC}



V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = Open | RCM = Open | STB = 0 V

Figure 3. I_{CC} Recessive over Temperature



V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = 100 pF | C_{L_RXD} = 15 pF | STB = 0 V

Figure 4. Total Loop Delay over Temperature

ADVANCE INFORMATION

8 Parameter Measurement Information

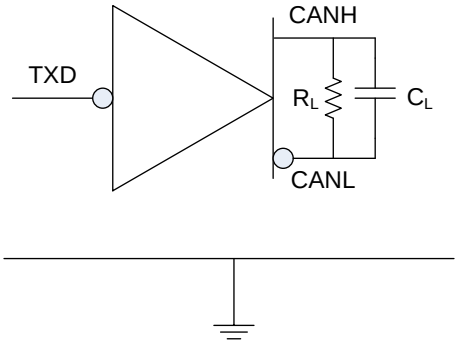


Figure 5. Supply Test Circuit

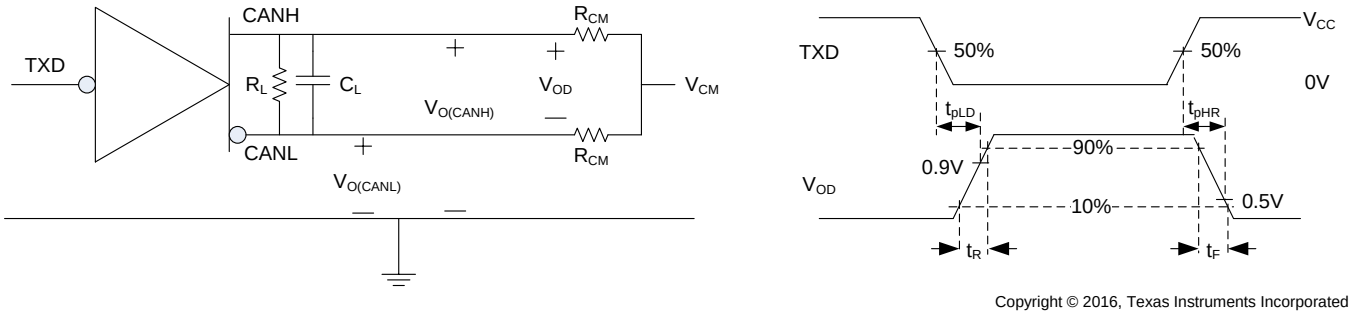


Figure 6. Driver Test Circuit and Measurement

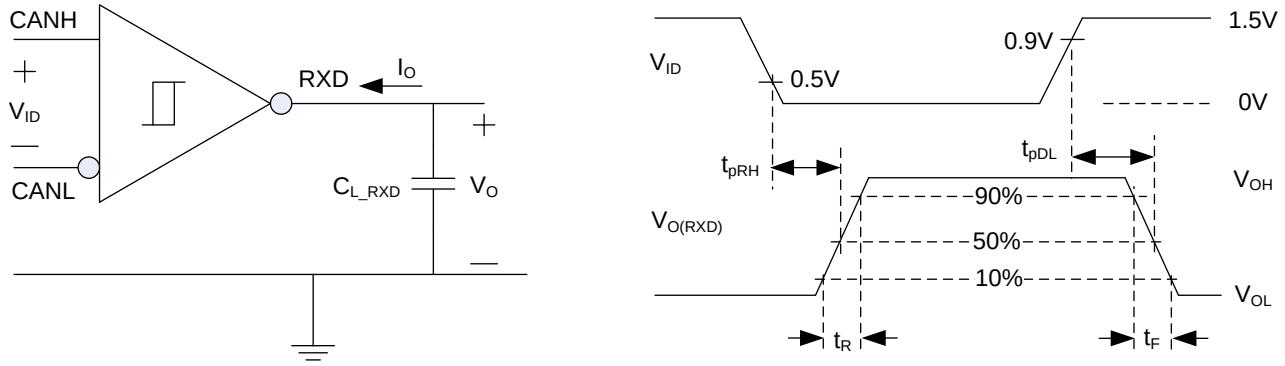


Figure 7. Receiver Test Circuit and Measurement

Parameter Measurement Information (continued)

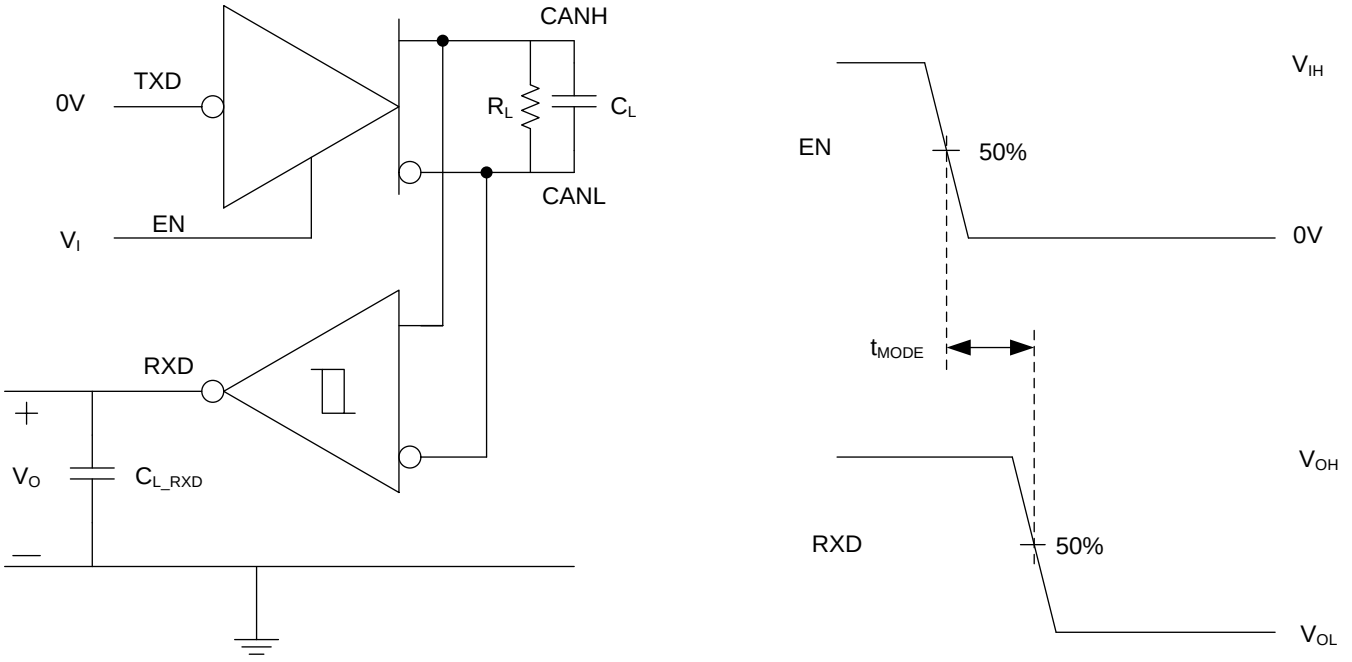


Figure 8. t_{MODE} Test Circuit and Measurement, Silent to Normal Mode

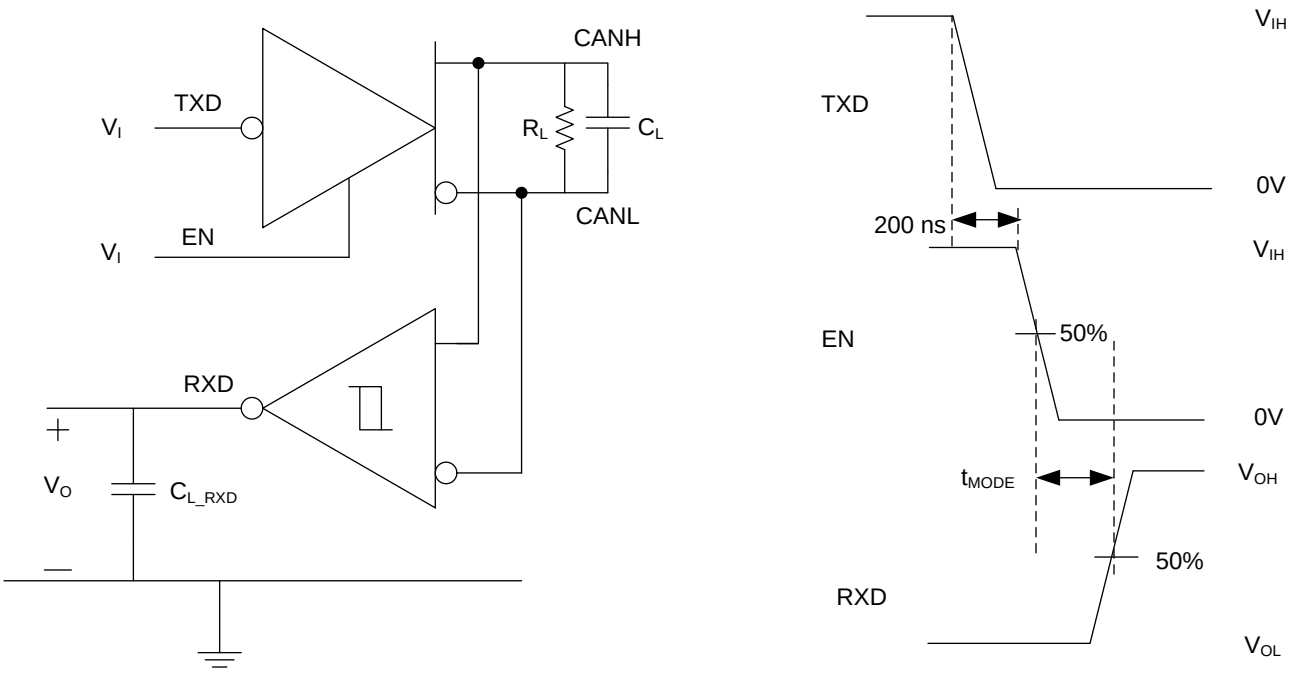


Figure 9. $t_{PROP(LOOP)}$ Test Circuit and Measurement, From Silent to Normal Mode

ADVANCE INFORMATION

Parameter Measurement Information (continued)

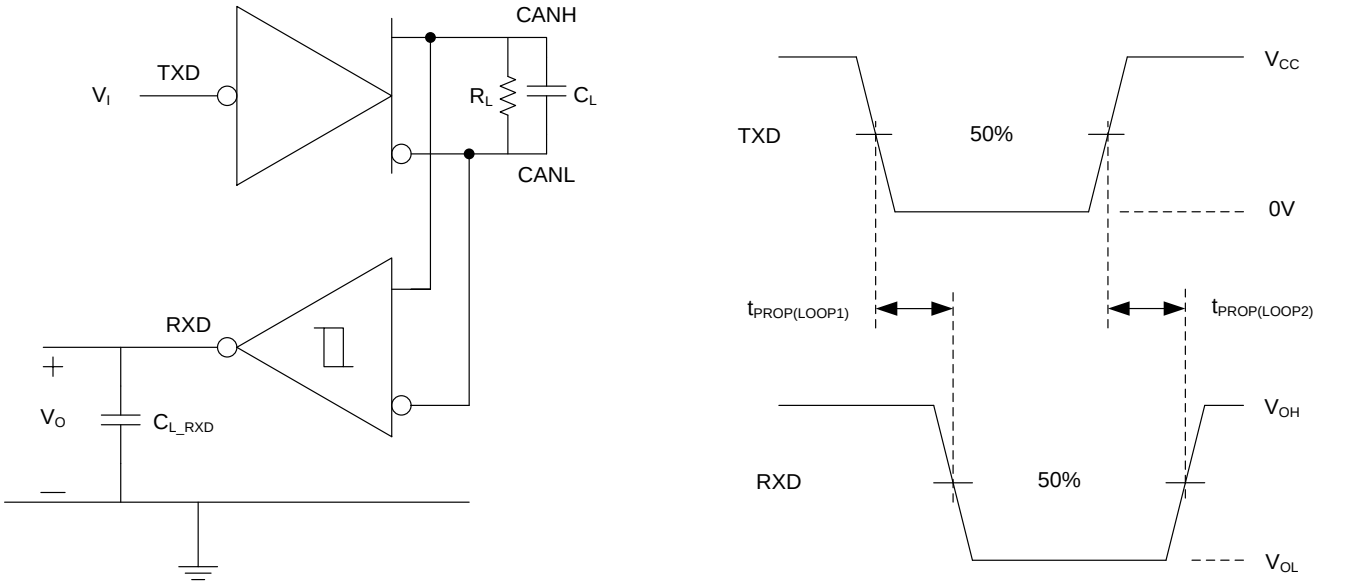


Figure 10. $t_{PROP(LOOP)}$ Test Circuit and Measurement

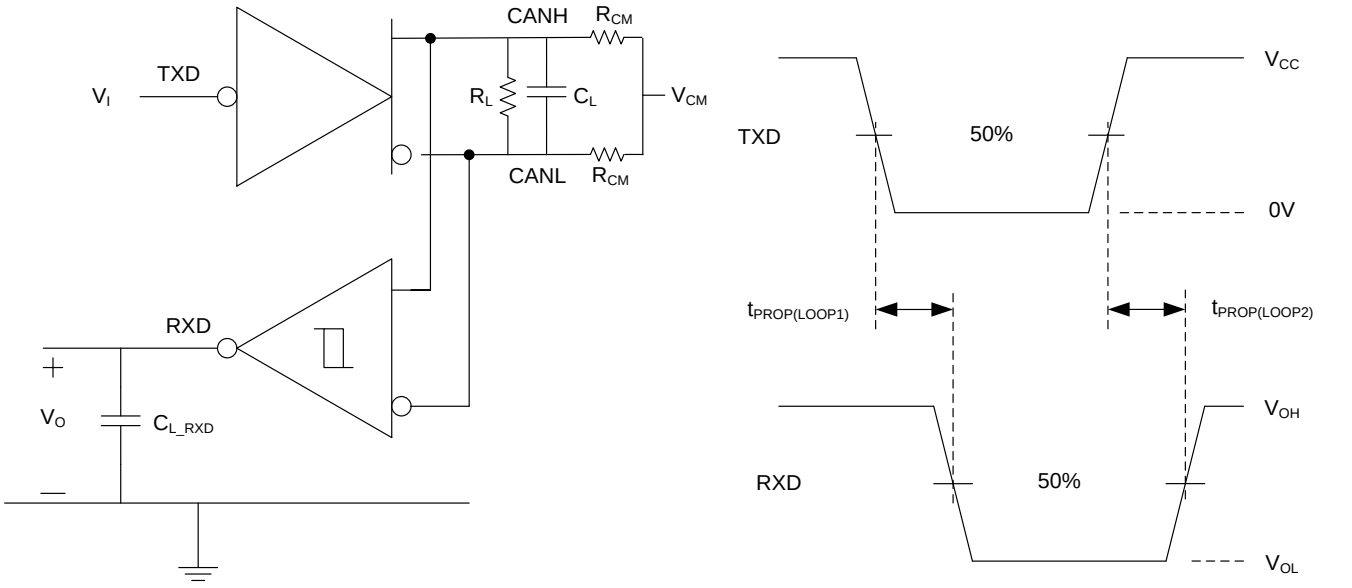


Figure 11. $t_{PROP(LOOP)}$ Test Circuit and Measurement with CM Range

ADVANCE INFORMATION

Parameter Measurement Information (continued)

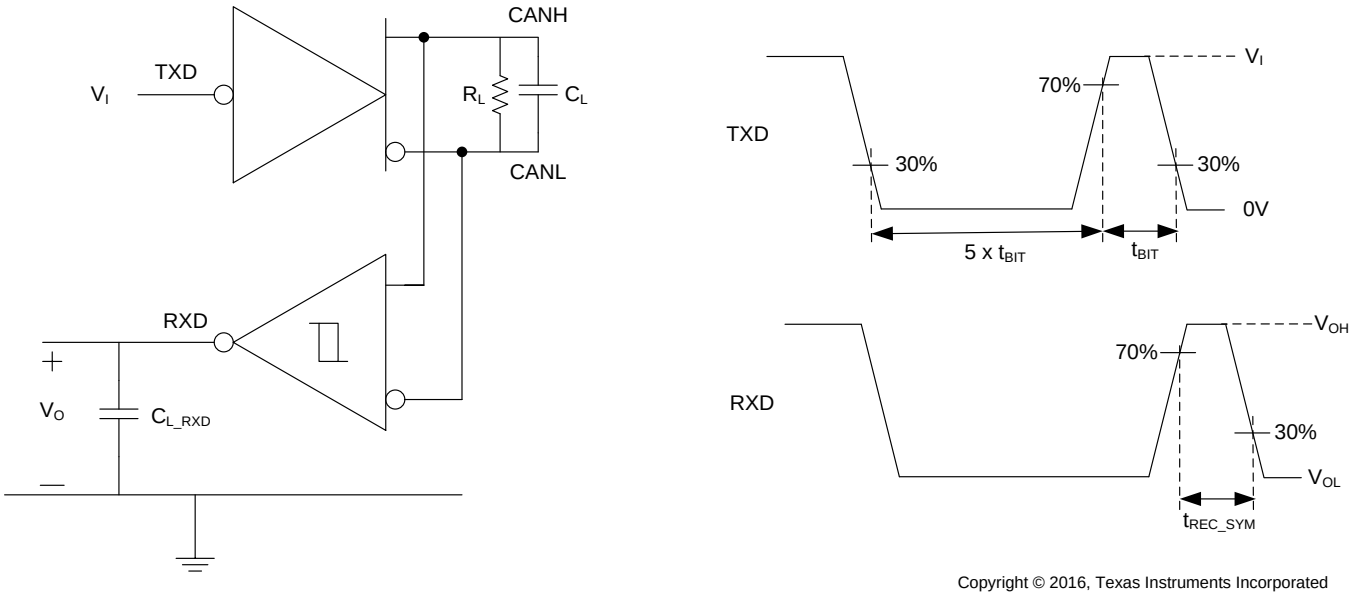


Figure 12. Loop Delay Symmetry Test Circuit and Measurement

ADVANCE INFORMATION

Parameter Measurement Information (continued)

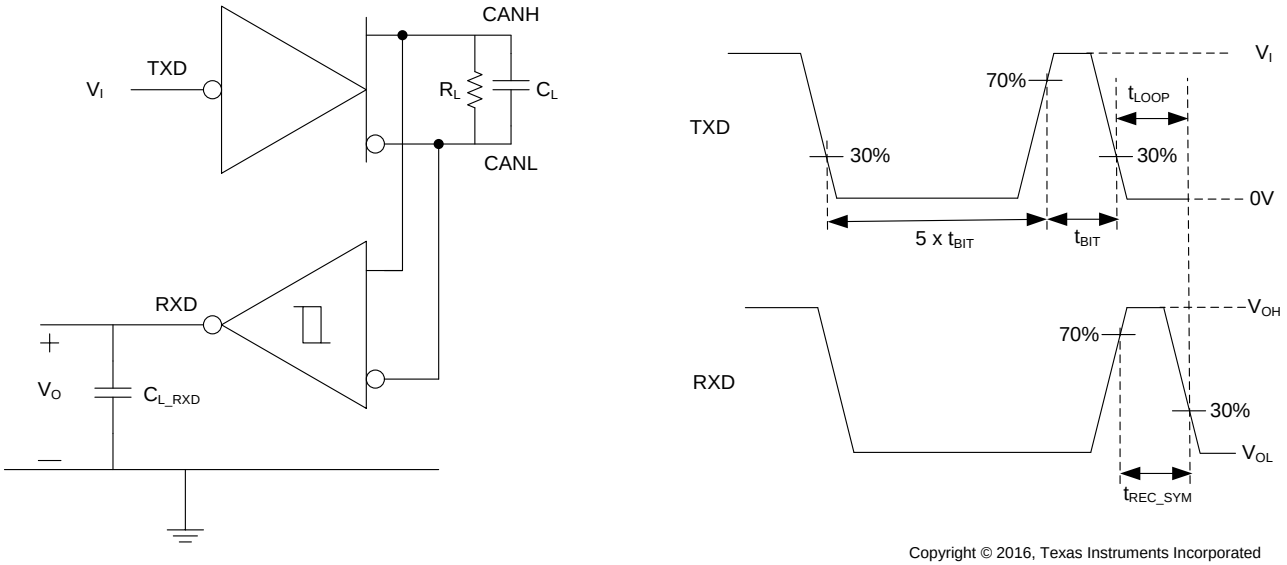


Figure 13. CHAR Loop Delay Symmetry Test Circuit and Measurement

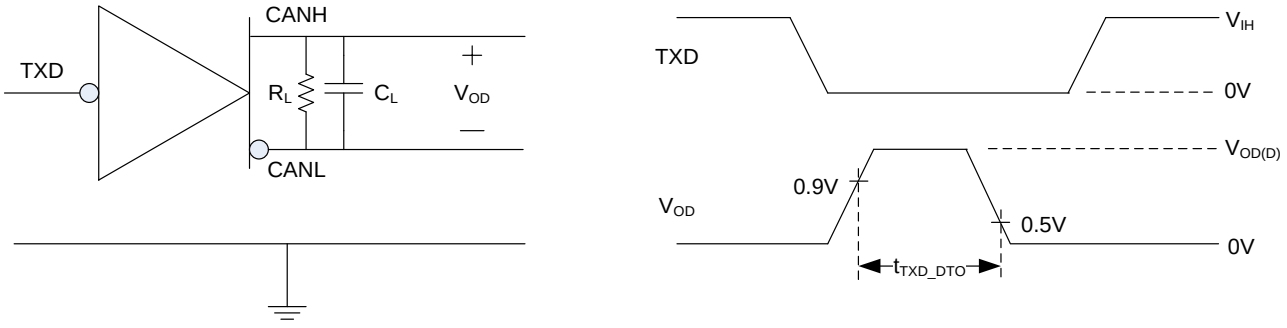


Figure 14. TXD Dominant Timeout Test Circuit and Measurement

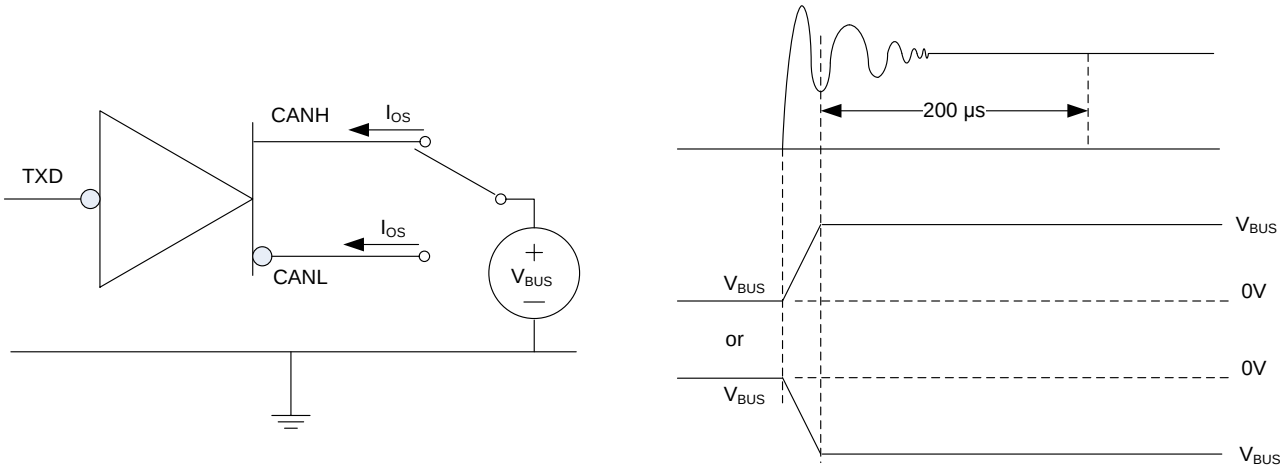


Figure 15. Driver Short-Circuit Current Test and Measurement

ADVANCE INFORMATION

Parameter Measurement Information (continued)

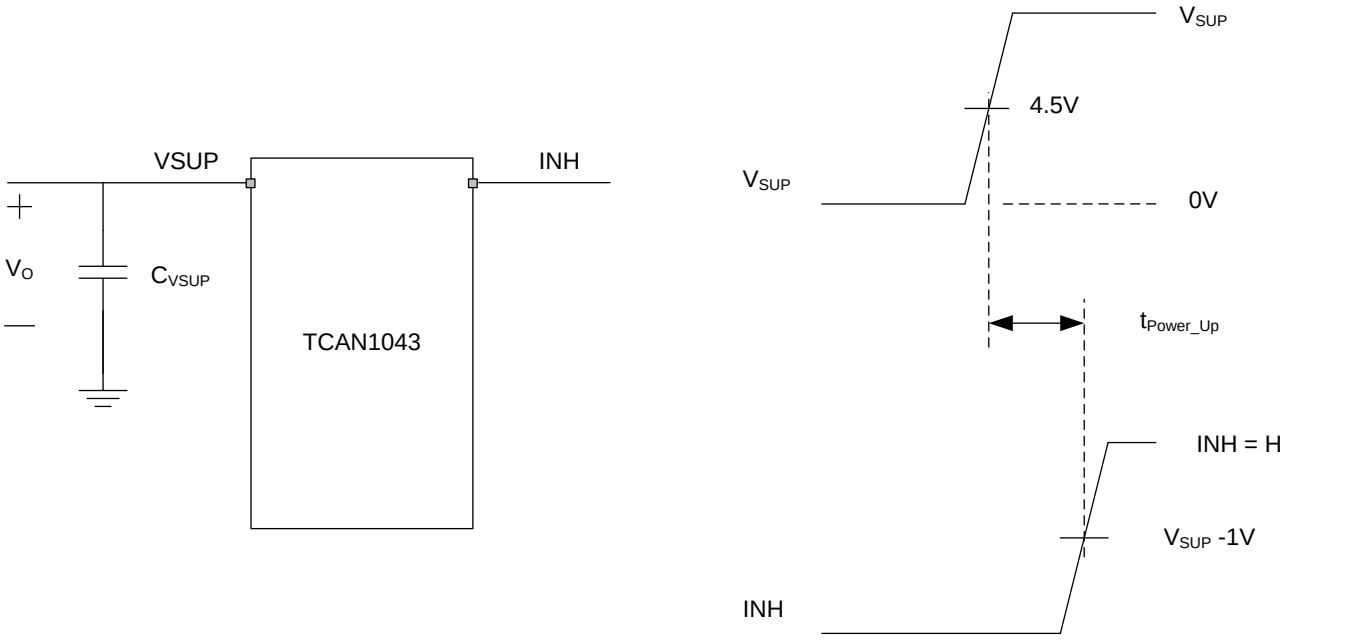


Figure 16. t_{Power_Up} Timing Measurement

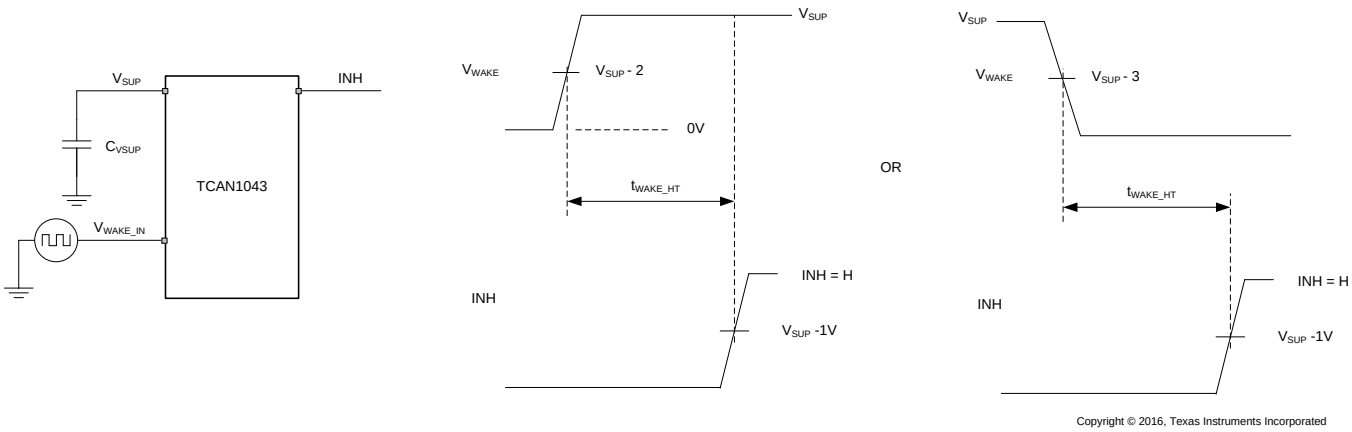


Figure 17. t_{WAKE_HT} While Monitoring INH Output

ADVANCE INFORMATION

Parameter Measurement Information (continued)

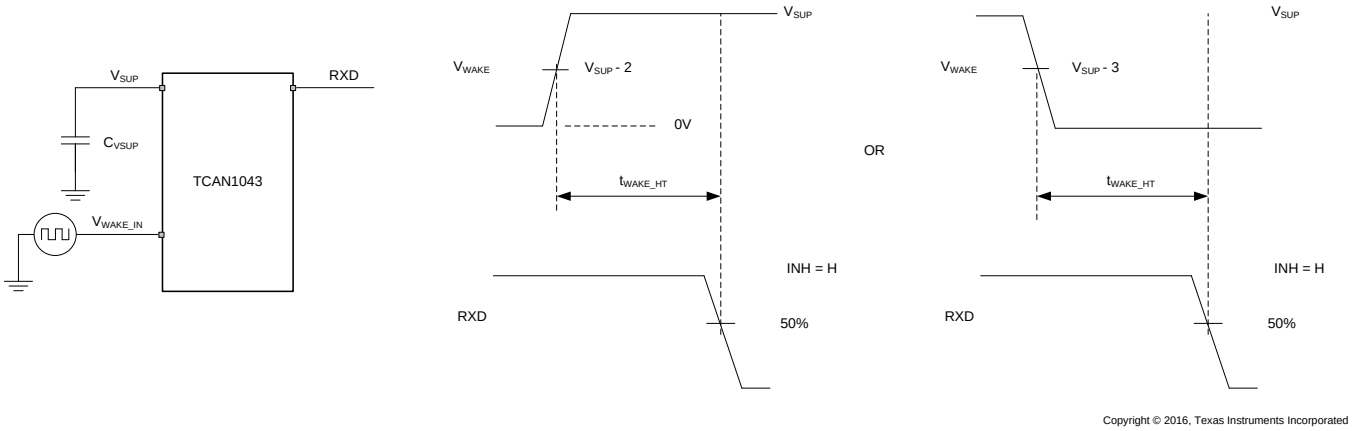


Figure 18. t_{WAKE_HT} While Monitoring RXD Output

ADVANCE INFORMATION

9 Detailed Description

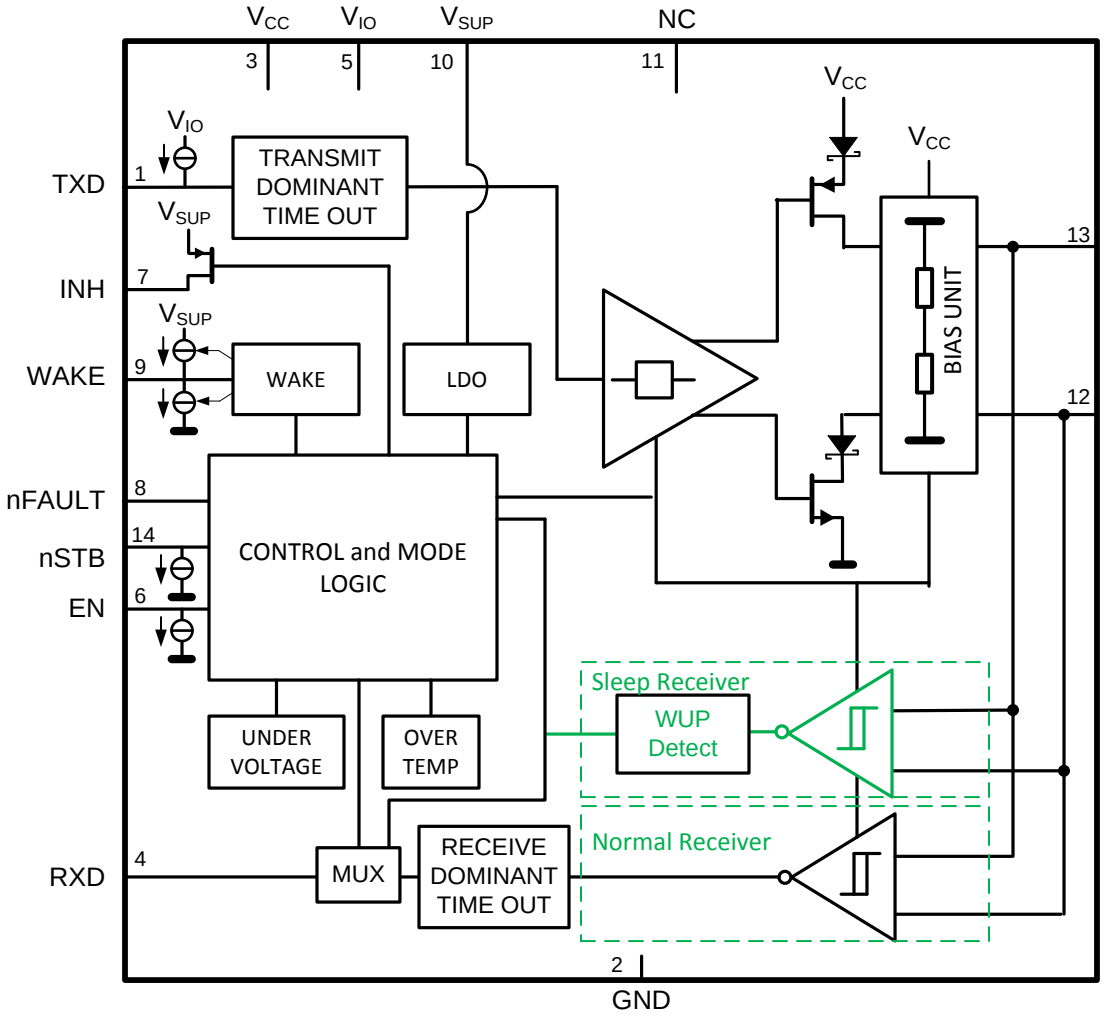
9.1 Overview

The TCAN1043xx-Q1 meets or exceeds the specifications of the ISO 11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO11898-2/5 according to the GIFT/ICT High Speed CAN test specification.

This device provides CAN transceiver differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN network robustness. Various versions of the device are available to support CAN and CAN with Flexible Data Rate (FD) protocol at various data rate optimizations:

- Classic CAN: CAN and CAN FD with data rates up to 1 Mbps
- CAN FD 2 Mbps: CAN FD to 2 Mbps
- CAN FD 5 Mbps: CAN FD to 5 Mbps

9.2 Functional Block Diagram



ADVANCE INFORMATION

9.3 Feature Description

9.3.1 Internal and External Indicator Flags (nFAULT and RXD)

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake up requests and a “cold” power-up sequence on the V_{SUP} battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake up request and the faults are multiplexed (ORed) to the nFAULT output.

Table 1. Device Status Indicator Flags

EVENT	FLAG NAME	CAUSE	INDICATORS(1)	FLAG IS CLEARED	COMMENT
Power-up	PWRON	Power up on VSUP and any return of VSUP after it has been below UV_{VSUP}	nFAULT = L upon entering Silent mode from Standby, Go-to-Sleep, or Sleep mode	After transition to normal mode	
Wake-up Request	WAKERQ(2)	Wake up event on CAN bus, state transition on WAKE pin, or initial power up	nFAULT = RXD = L after wake up in standby mode, go-to-sleep mode, and sleep mode	After transition to normal mode, or either a UV_{VCC} or UV_{VIO} event	Wake up request may only be set from standby, Go-to-sleep, or sleep mode. Resets timers for UV_{VCC} or UV_{VIO}
Wake-up Source Recognition(3)	WAKESR	Wake up event on CAN bus, state transition on WAKE pin, initial power up	Available upon entering normal mode(4) , nFAULT = L indicates wake from WAKE terminal, nFAULT = H indicates wake from CAN bus	After four recessive to dominant edges on TXD in normal mode,leaving normal mode, or either a UV_{VCC} or UV_{VIO} event	A LWU source flag is set on intial power up
Under voltage	UVVCC	Under voltage V_{CC}	Not externally indicated	VC_C returns, or Wake-up request occurs	
	UVVIO	Under voltage V_{IO}	Not externally indicated	V_{IO} returns, or Wake-up request occurs	
	UVVSUP	Under voltage V_{SUP}	Not externally indicated	V_{SUP} returns	V_{SUP} undervoltage event will trigger the PWRON and WAKERQ flags upon return of VSUP
CAN Bus Failures	CBF	CANH shorted to GND, V_{CC}, V_{SUP} or CANL shorted to GND, V_{CC}, V_{SUP}	nFAULT = L in Normal mode only(5)	Upon leaving Normal mode	Failure must persist for four consecutive dominant to recessive transistions
Local Faults	TXDDTO	TXD Dominant Time Out, dominant (low) signal for $t \geq t_{TXD\_DTO}$	nFAULT = L upon entering Silent mode from Normal mode	RXD = L and TXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	CAN driver remains disabled until the TXDDTO is cleared
	TXDRXD	TXD and RXD pins are shorted together for $t \geq t_{TXD\_DTO}$			CAN driver remains disabled until the TXDRXD is cleared
	CANDOM	CAN bus dominant fault, when dominant bus signal received for $t \geq t_{BUS\_DOM}$		RXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	Driver remains enabled
	TSD	Thermal Shutdown, junction temperature $\geq T_{TSD}$		T_J drops below t_{TSD} and either RXD = L and TXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	CAN driver remains disabled until the TSD is cleared

(1) V_{IO} and V_{SUP} are present
(2) Transitions to Go-to-sleep mode is blocked until WAKERQ flag is cleared
(3) Wake-up source recognition will reflect the first wake up source. If additional wake-up events occur the source will still indicate the original wake up source
(4) Indicator is only available in normal mode until the flag is cleared
(5) CAN Bus failure flag will be indicated after four recessive to dominant edges on TXD

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9.3.2 Power-Up Flag (PWRON)

This is an internal and external flag that is set and controls the power up state of the device. The device will power on to standby mode with the PWRON flag set after V_{SUP} has cleared the under voltage lock out for V_{SUP}, UV_{VSUP}

9.3.3 Wake-Up Request Flag (WAKERQ)

This is an internal and external flag that can be set in standby, Go-to-sleep, or Sleep mode. This flag is set when either a valid local wake up (LWU) request occurs, or a valid remote wake request occurs, or on power up on V_{SUP}. The setting of this flag clears t_{UV} timer for the UV_{VCC} or UV_{VIO}. This flag is cleared upon entering normal mode or during a under voltage event on V_{CC} or V_{IO}.

9.3.4 Wake-Up Source Recognition Flag (WAKESR)

This flag is an internal and external flag that is set high or low after a valid local wake up (LWU) request occurs, or a valid remote wake request occurs. This flag is only available in Normal mode before four recessive to dominant transitions occur on TXD. If the nFAULT pin is high after entering normal mode, this indicates that a remote wake request was received. If the nFAULT output is low after entering Normal mode, this indicates that a local wake up event occurred. Upon power up on V_{SUP}, or after and under voltage event on V_{SUP}, the local wake up request is indicated on nFAULT.

9.3.5 Undervoltage Fault Flags

The TCAN1043xx-Q1 device comes with undervoltage detection circuits on all three supply terminals: V_{SUP}, V_{CC}, and V_{IO}. These flags are internal flags and are not indicated on the nFAULT terminal.

9.3.5.1 Undervoltage on V_{CC} Fault

This internal flag is set when the voltage on V_{CC} drops below the undervoltage detection voltage threshold, UV_{VCC}, for longer than t_{UV}.

9.3.5.2 Undervoltage on V_{IO} Fault

This internal flag is set when the voltage on V_{IO} drops below the undervoltage detection voltage threshold, UV_{VIO}, for longer than t_{UV}.

9.3.5.3 Undervoltage on V_{SUP} Fault

This internal flag is set when the voltage on V_{SUP} drops below the undervoltage detection voltage threshold, UV_{VSUP}. While this flag is not externally indicated, the PWRON and WAKERQ flags are set once the V_{SUP} supply returns

9.3.6 CAN Bus Failure Fault Flag

The TCAN1043xx-Q1 devices are able to detect the following six faults that can occur on the CANH and CANL bus terminals. These faults are only detected in Normal mode and are only indicated via the nFAULT terminal while in Normal mode.

1. CANH bus pin shorted V_{SUP}
2. CANH bus pin shorted V_{CC}
3. CANH bus pin shorted GND
4. CANL bus pin shorted V_{SUP}
5. CANL bus pin shorted V_{CC}
6. CANL bus pin shorted GND

These failures are detected while transmitting a dominant signal on the CAN bus. If one of these fault conditions persists for four consecutive dominant bit transmissions, the nFAULT indicates a CAN bus failure flag in Normal mode by driving the nFAULT pin low. The CAN bus driver remains active.

The bus fault failure circuitry is able to detect bus faults for a range of differential resistance loads (R_{CBF}) and for any time greater than t_{CBF_MIN}.

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9.3.7 Local Faults

Local faults are detected in both Normal mode and Silent mode, but are only indicated via the nFAULT pin when transitioned form Normal mode to Silent mode. All other mode transitions clear the local fault flag indicators.

9.3.7.1 TXD Dominant Timeout (TXD DTO)

During Normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, expires the CAN driver is disabled. This keeps the bus free for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD terminal, thus clearing the dominant time out. The receiver and RXD terminal will reflect what is on the CAN bus and the bus terminals will be biased to recessive level during a TXD DTO. This fault is indicated via the TXDDTO flag shown on the nFAULT terminal.

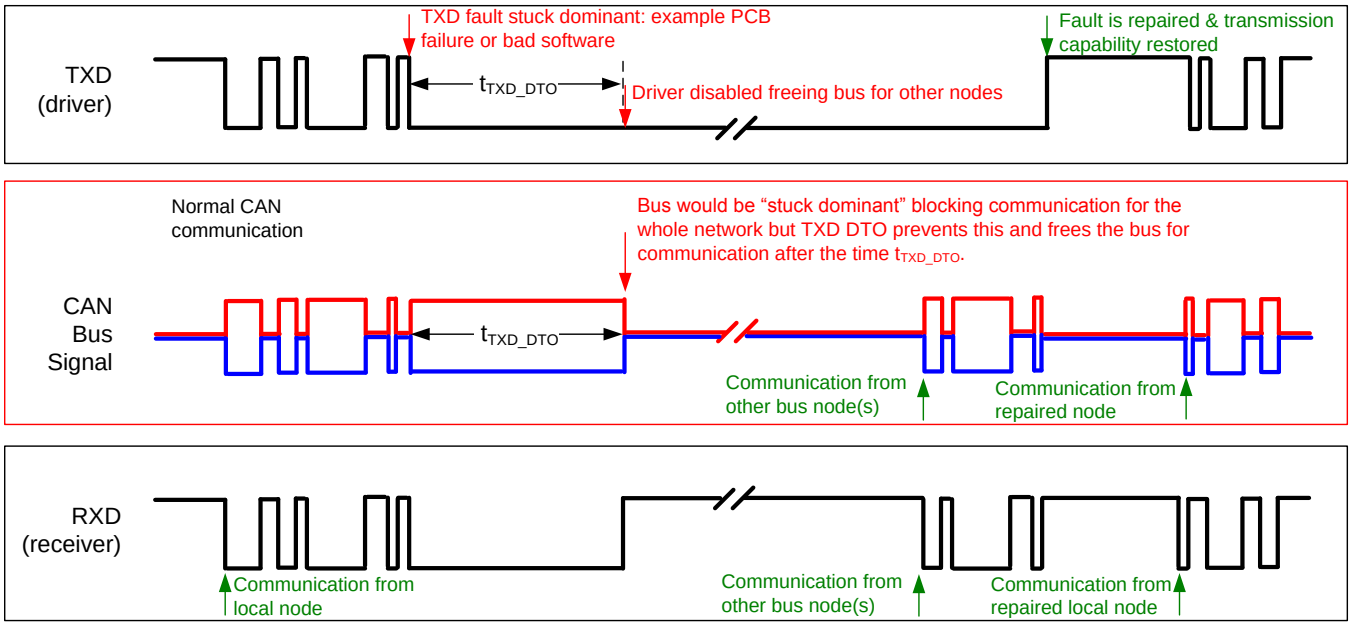

Figure 19. Example Timing Diagram for TXD DTO

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated by: Minimum Data Rate = 11 bits / t_{TXD_DTO} = 11 bits / 1.2 ms = 9.2 kbps.

9.3.7.2 TXD Shorted to RXD Fault

The TXDRXD flag is set if the device detects that the TXD and RXD lines have been shorted together for t ≥t_{TXD_DTO}. This fault is then indicated via the nFAULT terminal. The CAN driver is disabled until the TXDRXD fault is cleared.

This fault is only indicated in Normal mode and Silent mode.

9.3.7.3 CAN Bus Dominant Fault

The CAN bus dominant fault detects if the CAN bus is stuck in a permanent dominant (low) state. This fault is detected when the device detects a dominant on the bus for time ≥ t_{BUS_DOM}. This fault is then indicated via the CANDOM flag shown on the nFAULT terminal.

This fault is only indicated in Normal mode and Silent mode.

NOTE

If the CAN bus is stuck in a permanent dominant state no message traffic is possible.

9.3.7.4 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to the bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again causing the device to reenter thermal shut down. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output. This fault is indicated via the TSD flag shown on the nFAULT terminal.

NOTE

During thermal shutdown the CAN bus driver is turned off thus no transmission is possible from TXD to the bus. The CAN bus terminals are biased to recessive level during a thermal shutdown and the receiver to RXD path remains operational.

9.3.7.5 RXD Recessive Fault

The RXD recessive fault detects if the RXD terminal is stuck (clamped) in a permanent recessive state. This fault is detected when the device transmits four dominant bits to the bus via TXD but the RXD output does not follow. This fault is then indicated via the RXDREC flag shown on the nFAULT terminal.

NOTE

If the RXD terminal is forced or clamped recessive the CAN controller in the µProcessor will not recognize bus usage and could start transmitting at any time possibly causing corruption on the bus. This feature prevents a local fault on the RXD line from corrupting the entire CAN bus.

9.3.7.6 Undervoltage Lockout (UVLO)

The supply terminals have under voltage detection which puts the device in protected mode if one of the supply rails drop below the threshold voltage. This protects the bus and system during an under voltage event on either V_{SUP}, V_{CC} or V_{IO} supply terminals. These faults are internal fault flags and are not indicated via the nFAULT terminal.

During an undervoltage event on V_{CC} or V_{IO} the device goes into protected mode and the driver is disabled. After the UV timer expires the device will transition into sleep mode and the INH pin goes into a high impedance state. In the event of a UV on V_{IO} where the mode pins are no longer driven, the device transitions into standby mode (due to internal fail safe biasing on the NSTB and EN pins) until the UV timer expires and the device transitions into sleep mode.

The V_{CC} and V_{IO} undervoltage detection circuits share the same timer. Therefore, if an undervoltage on one supply occurs and the timers starts, and then during the undervoltage the other supply has an undervoltage event before the first supply recovers the timer will not reset.

NOTE

Once an under voltage condition is cleared and the supplies have returned to valid levels the device typically needs 200 µs to transition to normal operation.

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9.3.7.7 Unpowered Device

The device is designed to be an "ideal passive" or “no load” to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is un-powered so they will not load down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

Logic terminals also have extremely low leakage currents when the device is un-powered so they will not load down other circuits which may remain powered.

9.3.7.8 Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{IO} to force a recessive input level if the terminal floats. The STB terminal is also pulled up to force the device into low power Standby mode if the terminal floats.

The device has internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 2 for details on terminal bias conditions.

Table 2. Terminal Failsafe Biasing

TERMINAL	PULL UP or PULL DOWN	COMMENT
TXD	Pull up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
nSTB	Pull down	Weakly biases nSTB terminal towards low power Standby mode to prevent excessive system power
EN	Pull down	Weakly biases EN terminal towards low power mode to prevent excessive system power

NOTE

The internal bias should not be relied on by design, especially in noisy environments but should be considered a fall back protection. Special care needs to be taken when the device is used with MCUs utilizing open drain outputs. TXD is weakly internally pulled up. The TXD pull up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the microprocessor's CAN controller. An adequate external pull up resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the CAN transceiver.

9.3.7.9 CAN Bus Short Circuit Current Limiting

The TCAN1043xx-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with Equation 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

NOTE

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

ADVANCE INFORMATION

9.4 Device Functional Modes

The device has four main operating modes: Normal mode, Standby mode, Silent mode and Sleep mode, and one transitional mode called Go-to-Sleep mode. Operating mode selection is made via the nSTB and EN input terminals in conjunction with supply conditions and wake events.

Table 3. Operating Modes

V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ Flag	Mode	Driver	Receiver	RXD	Bus Bias	INH
> UV_{VCC} & > UV_{VIO}	> UV_{VSUP}	H	H	X	Normal	Enabled	Enabled	Mirrors Bus State	V_{CC}/2	ON
> UV_{VCC} & > UV_{VIO}	> UV_{VSUP}	L	H	X	Silent	Disabled (OFF)	Enabled	Mirrors Bus State	V_{CC}/2	ON
> UV_{VCC} & > UV_{VIO}	> UV_{VSUP}	H	L	Cleared	Go to Sleep(1)	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	ON(2)
				Cleared	Sleep(3)	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	OFF
				Set	Standby	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	LOW signals wake up	Weak pull to GND	ON
> UV_{VCC} & > UV_{VIO}	> UV_{VSUP}	L	L	X	Standby	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	LOW signals wake up	Weak pull to GND	ON
< UV_{VCC} & <UV_{VIO}	> UV_{VSUP}	X	X	X	Sleep	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	OFF (High Z)
X	< UV_{VSUP}	X	X	X	Protected	Disabled (OFF)	Disabled (OFF)	High Z	High Z	OFF (High Z)

(1) Go-to-sleep: Transitional mode for EN = H, nSTB = L until $t_{go\_to\_sleep}$ timer has expired
(2) The INH pin will transition to high Z (off) after $t_{go\_to\_sleep}$ timer has expired
(3) Mode change from Go-to-Sleep mode to sleep mode once $t_{go\_to\_sleep}$ timer has expired

9.4.1 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 20 and Figure 21.

Recessive bus state is when the bus is biased to a common mode of about V_{CC}/2 (2.5 V) via the high resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of approximately 0 V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case, the differential voltage of the bus will be greater than the differential voltage of a single driver.

The host microprocessor of the CAN node uses the TXD terminal to drive the bus and receives data from the bus on the RXD terminal.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 20 and Figure 21.

ADVANCE INFORMATION

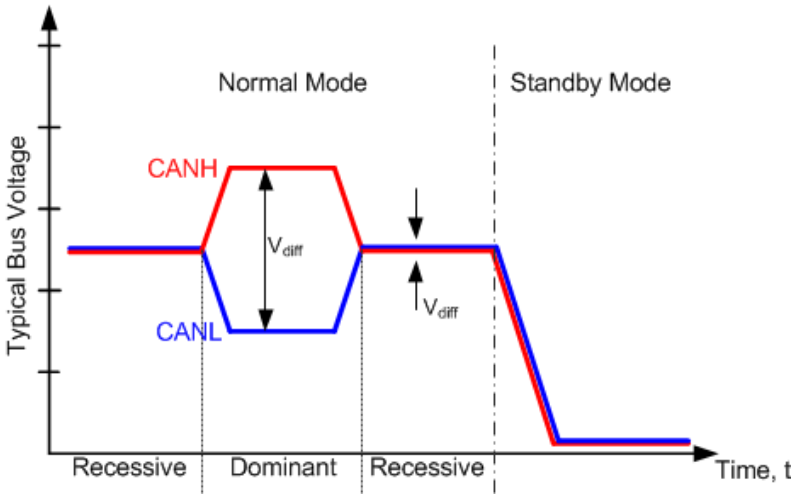
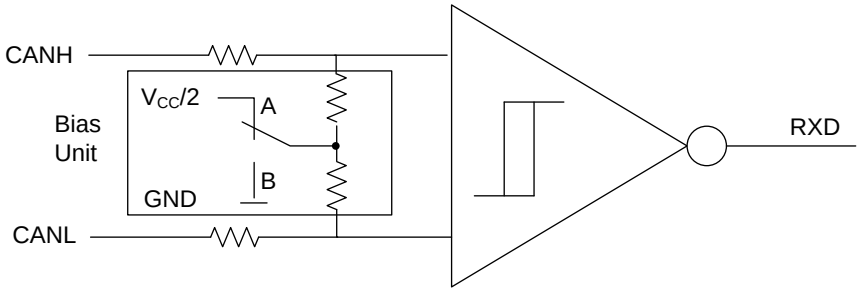


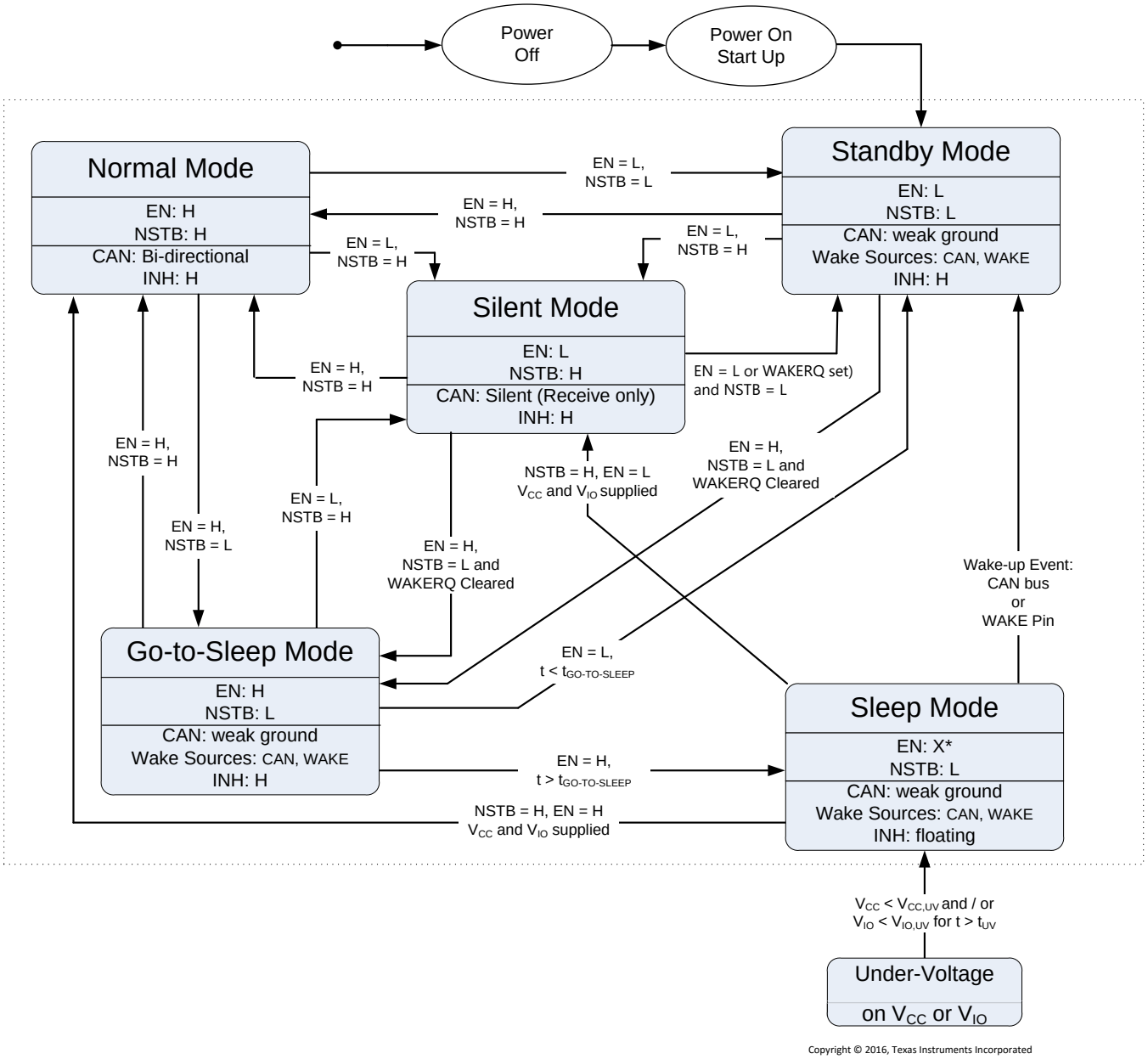
Figure 20. Bus States (Physical Bit Representation)



A. Normal and Silent Modes
B. Sleep and Standby Modes

Figure 21. Bias Unit (Recessive Common Mode Bias) and Receiver

ADVANCE INFORMATION



*The enable pin can be in a logical high or low state while in sleep mode but since it has an internal pull-down, the lowest possible power consumption will occur when the pin is left either floating or pulled low externally.

Figure 22. State Diagram

9.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD

Entering Normal mode clears both the WAKERQ and PWRON flags.

9.4.3 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode the CAN driver is disabled but the receiver is fully operational. CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

In Silent mode, the PWRON, and Local Failure Flags can be polled.

9.4.4 Standby Mode

Standby mode is a low power mode where the driver and receiver are disabled reducing current consumption. However, this is not the lowest power mode of the device. The INH terminal is on allowing the rest of the system to resume normal operation.

During standby mode, a wake up request (WAKERQ) is indicated by the RXD terminal being low. The wake up source is identified via the nFAULT pin after the device is returned to normal mode.

9.4.5 Go to Sleep Mode

Go to sleep mode is the transitional mode of the device from any state to sleep. In this state, the driver and receiver are disabled reducing the current consumption; however, the INH terminal is on allowing the rest of the system to resume normal operation. If the device is held in this state for time ≥ $t_{go\_to\_sleep}$ the device transitions to sleep mode and the INH is turned off (high Z).

Entering Go to Sleep Mode from Standby Mode is gated if the WAKERQ flag is set. Once the flag is cleared this transition is no longer gated.

9.4.6 Sleep Mode with Remote Wake and Local Wake Up Requests

Sleep mode is the lowest power mode of the device. The CAN driver and main receiver are turned off and bi-directional CAN communication is not possible.

The low power receiver with bus monitor and WAKE circuits are supplied via the V_{SUP} supply are enabled. This low power receiver is able to monitor the bus for any activity that validates the wake up pattern (WUP), and the WAKE monitoring circuit monitors for state changes on the WAKE terminal for a local wake up (LWU) event. The V_{CC} and V_{IO} supplies may be turned off or be controlled via the INH output for additional system level current savings.

The valid wake up sources in sleep mode are:

- Remote Wake Request: CAN Bus activity that validates the WUP
- Local Wake Up (LWU) Request: State change on WAKE terminal

Additionally, EN and nSTB can be used to change modes if both V_{IO} and V_{CC} are powered.

If a bus wake up pattern (WUP) or local wake up (LWU) event occurs the internal WAKERQ flag is set and the device transitions to Standby mode which in turn sets the INH output high. The wake up source recognition flag (WAKESR) is set either high or low to identify which wake event occurred. This flag can be polled via the nFAULT pin after the device is returned to normal mode only until there have been four recessive to dominant transitions on the TXD pin.

The wake source (WAKESR) flag has two states:

- Low: This indicated that the wake up source was via the WAKE pin.
- High: This indicates that a remote wake request via the CAN bus occurred.

NOTE

If both a local wake and a remote wake request occur, the device will indicate whichever event was completed first.

The device will transition into sleep mode if at any time either or both the V_{CC} or V_{IO} supplies have an under voltage condition that lasts longer than timer t_{UV}.

NOTE

If V_{IO} remains active in sleep mode, it is recommended to drive EN pin low once device has transitioned into sleep mode to reduce current consumption due to the internal pull-down on the EN terminal.

ADVANCE INFORMATION

9.4.6.1 Remote Wake Request via Wake Up Pattern (WUP)

These devices use the multiple filtered dominant wake up pattern (WUP) from ISO11898-2 (2016) to qualify bus traffic into a request to wake the host microprocessor and system power supply or supplies. The WUP is active for both sleep and standby modes and results in RXD pin being driven low after a valid pattern is received.

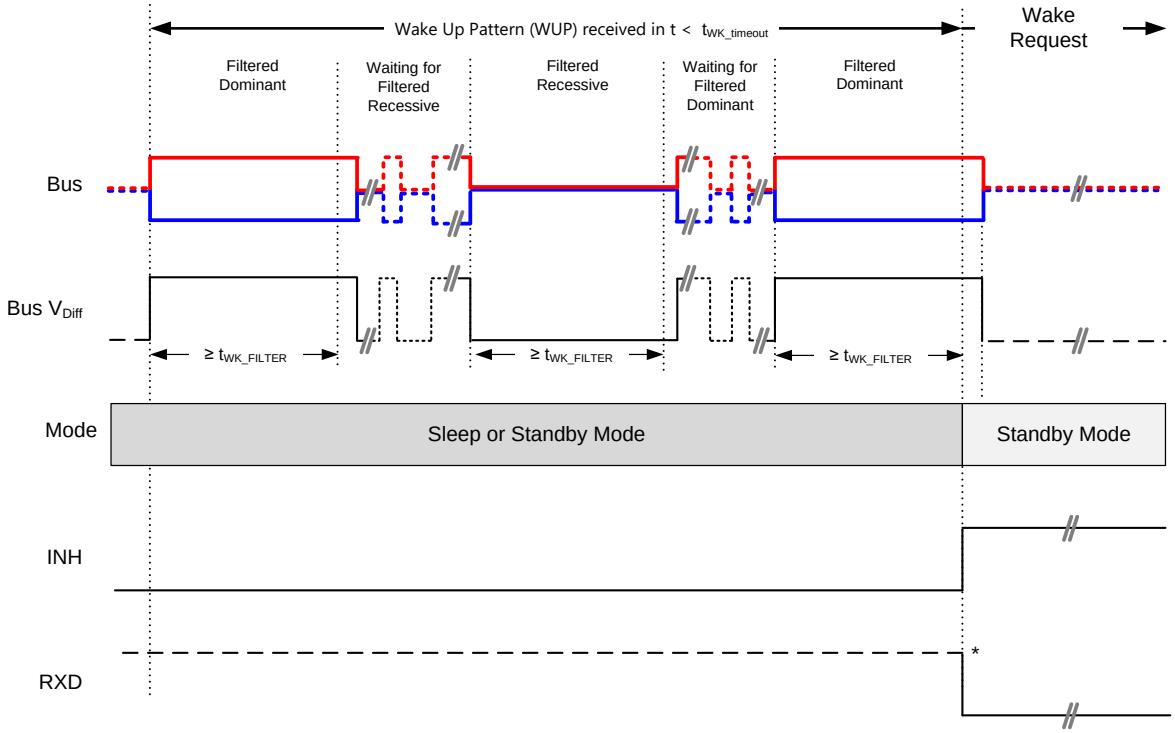
The wake up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered dominant bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic will not reset the bus monitor. Once a filtered recessive is received the bus monitor is now waiting on a filtered dominant and again, other bus traffic will not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor will recognize the WUP and transition to standby mode, drive the INH output high and set the RXD terminal low (if V_{IO} is present) to signal the wake up request.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ will never be detected as part of a WUP and thus no wake request will be generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake request may be generated. Bus state times more than $t_{WK\_FILTER(MAX)}$ will always be detected as part of a WUP and thus a wake request will always be generated. See Figure 23 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

If the device is switched to normal mode or an under voltage event occurs on V_{CC} or V_{IO} supplies the wake request will be lost

ISO11898-2 (2016) has two sets of times for a short and long wake up filter times. The t_{WK_FILTER} timing for the TCAN1043xx-Q1 devices have been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps will trigger the filter in either bus state.



The RXD pin is only driven once V_{IO} is present.

Figure 23. Wake Up Pattern (WUP)

For an additional layer of robustness and to prevent false wake-ups, these devices implement a timeout feature. For a remote Wake up event to successfully occur, the entire Wake Up Pattern (WUP) must be received within the timeout value (see Figure 23). If not, the internal logic will be reset and the part will remain in its current state without waking up. The full pattern must then be retransmitted (within the timeout value), the other constraints mentioned in this section and figure Figure 23 still apply.

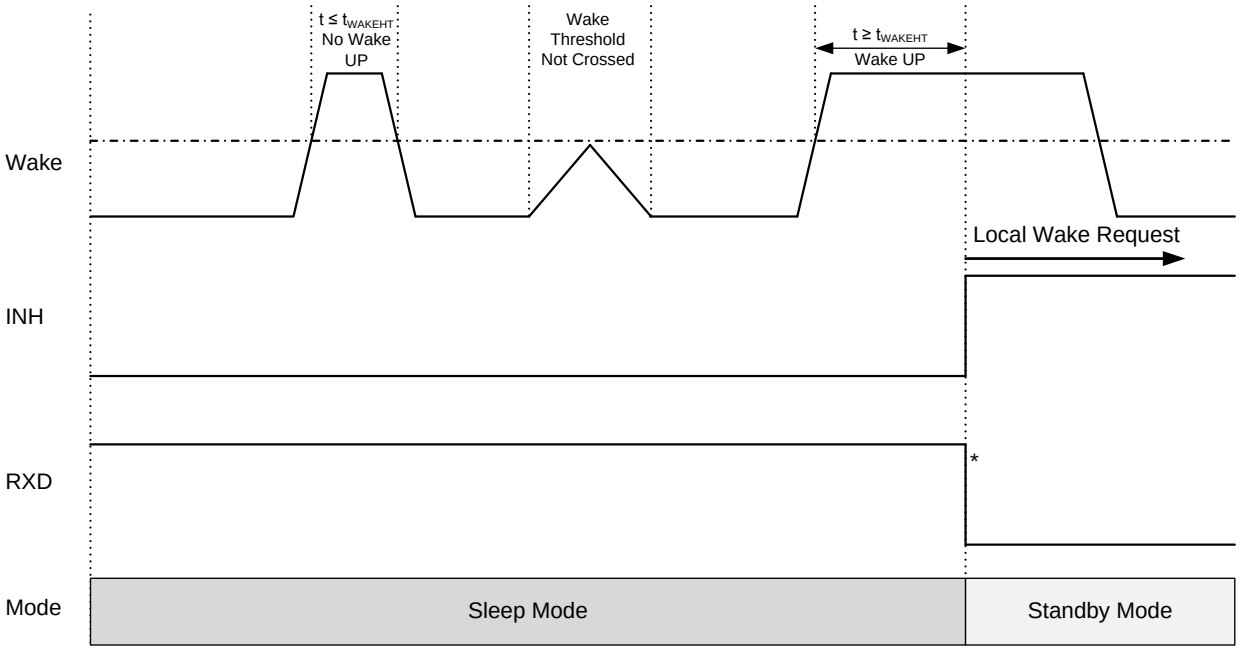
9.4.6.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a high voltage input terminal which can be used for local wake up (LWU) requests via a voltage transition. The terminal triggers a local wake up (LWU) event on either a low to high, or a high to low transition since it has a bi-directional input thresholds (falling or rising edge).

This terminal may be used with a switch to V_{SUP} or to ground. If the terminal is unused it should be pulled to ground or V_{SUP} to avoid unwanted parasitic wake up events.

The LWU circuitry is active in Sleep Mode with Remote Wake and Local Wake Up Requests, Standby Mode and *Go to Sleep Mode*. If a valid LWU event occurs the device will transition to standby mode. The LWU circuitry is not active in Normal mode, Silent mode

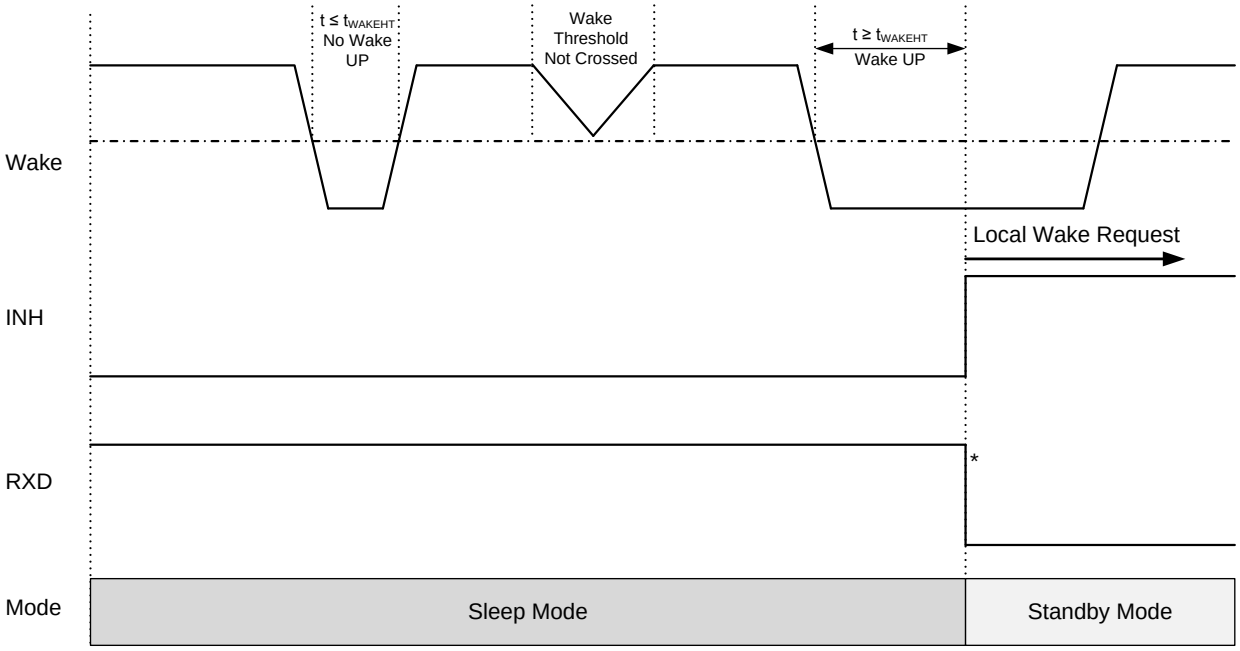
To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(min)}$. A constant high level on WAKE will have an internal pull-up to V_{SUP} and a constant low level on WAKE will have an internal pull-down to GND.



The RXD pin is only driven once V_{IO} is present.

Figure 24. Local Wake Up – Rising Edge

ADVANCE INFORMATION



The RXD pin is only driven once V_{IO} is present.

Figure 25. Local Wake Up – Falling Edge

9.4.7 Driver and Receiver Function Tables

Table 4. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS(2)		DRIVEN BUS STATE(3)
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Common Mode Biased to V_{CC}/2
Silent	X	Z	Z	Common Mode Biased to V_{CC}/2
Standby	X	Z	Z	Common Mode Biased to GND
Go to Sleep	X	Z	Z	Common Mode Biased to GND
Sleep	X	Z	Z	Common Mode Biased to GND

(1) H = high level, L = low level, X = irrelevant.
(2) H = high level, L = low level, Z = high Z receiver bias.
(3) For Bus state and bias see Figure 3 and Figure 4.

ADVANCE INFORMATION

Table 5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL (1)
Normal	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H
Standby	$V_{ID} \geq 1.15$ V	Dominant	H L if either remote or local wake events have occurred
	$V_{ID} \leq 0.4$ V	Indeterminate	
	0.5 V < V_{ID} < 1.15 V	Recessive	
	Open ($V_{ID} \approx 0$ V)	Open	
Sleep and Go to Sleep (WUP Monitor)	$V_{ID} \geq 1.15$ V	Dominant	H L if either remote or local wake events have occurred and $_{VIO}$ is present. Tri-State if V_{IO} or V_{SUP} are not present
	0.4 V , V_{IO} < 1.15 V	Indeterminate	
	$V_{ID} \leq 0.4$ V	Recessive	
	Open ($V_{ID} \approx 0$ V)	Open	

(1) H = high level, L = low level

9.4.8 Digital Inputs and Outputs

All devices have a V_{IO} supply that is used to set the digital inputs thresholds. The input thresholds are ratio metric to V_{IO} supply using CMOS input levels, making them scalable for µPs with digital IOs from 2.8 V to 5 V. The high level output voltages for the RXD and nFAULT output pins will be driven to V_{IO} level for logic high output.

9.4.9 INH (Inhibit) Output

The inhibit output terminal is used to control system power management devices allowing for extremely low system current consumption in sleep mode. This terminal can be used to enable and disable local power supplies. The pin has two states: driven high, and high impedance (High Z).

When high (on) the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state the output will be left floating. The INH pin will be high for normal, silent, go to sleep, and standby modes. It is low when in sleep mode.

NOTE

This terminal should be considered a “high voltage logic” terminal, not a power output thus should be used to drive the EN terminal of the system’s power management device and not used as a switch for the power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside the system module.

ADVANCE INFORMATION

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TCAN1043xx-Q1 transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5 V regulator can be used to drive bot V_{CC} and V_{IO} as shown in Figure 26 or independent 5 V and 3.3 V regulators can be used to drive V_{CC} and V_{IO} separately as shown in Figure 27. The bus termination is shown for illustrative purposes.

10.2 Typical Application

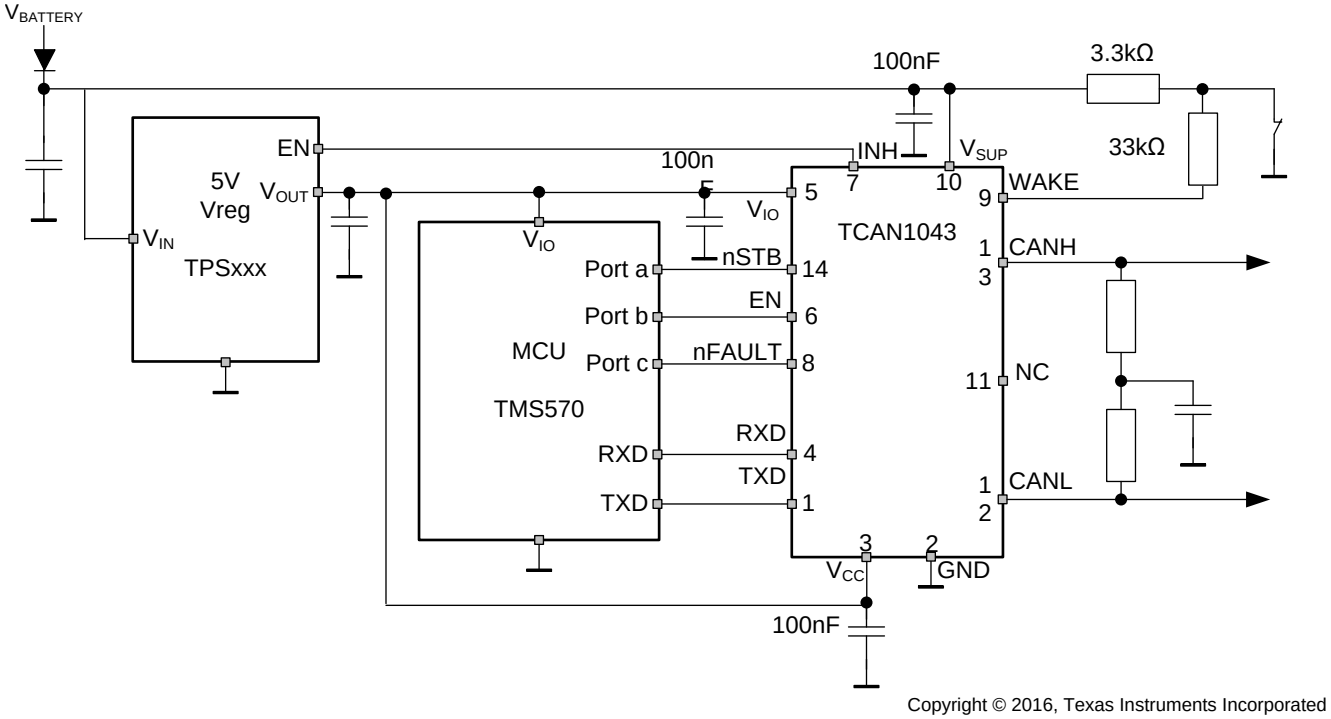


Figure 26. Typical CAN Bus Application Using TCAN1043xx-Q1 with 5 V µC

ADVANCE INFORMATION

Typical Application (continued)

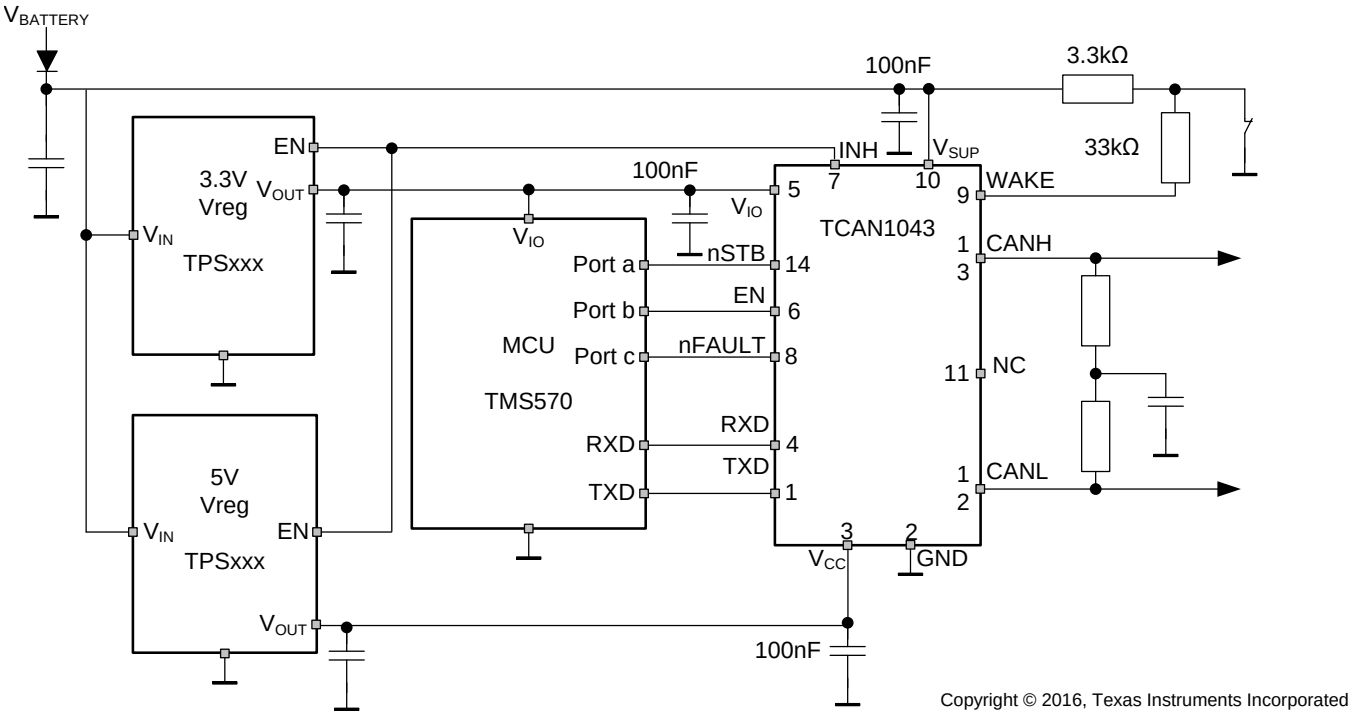


Figure 27. Typical CAN Bus Application Using TCAN1043xx-Q1 with 3.3 V µC

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1043xx-Q1 family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In ISO11898-2 the driver differential output is specified with a 60-Ω bus load (the two termination resistors in parallel) where the differential output must be greater than 1.5 V. The TCAN1043xx-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1043xx-Q1 is a minimum of 30 kΩ. If 167 TCAN1043xx-Q1 transceivers are in parallel on a bus, this is equivalent to a 180-Ω differential load in parallel with the 60 Ω from termination gives a total bus load of 45 Ω. Therefore, the TCAN1043xx-Q1 family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2 V minimum differential input voltage requirement at each receiving node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate..

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

ADVANCE INFORMATION

Typical Application (continued)

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Termination

The ISO11898-2 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

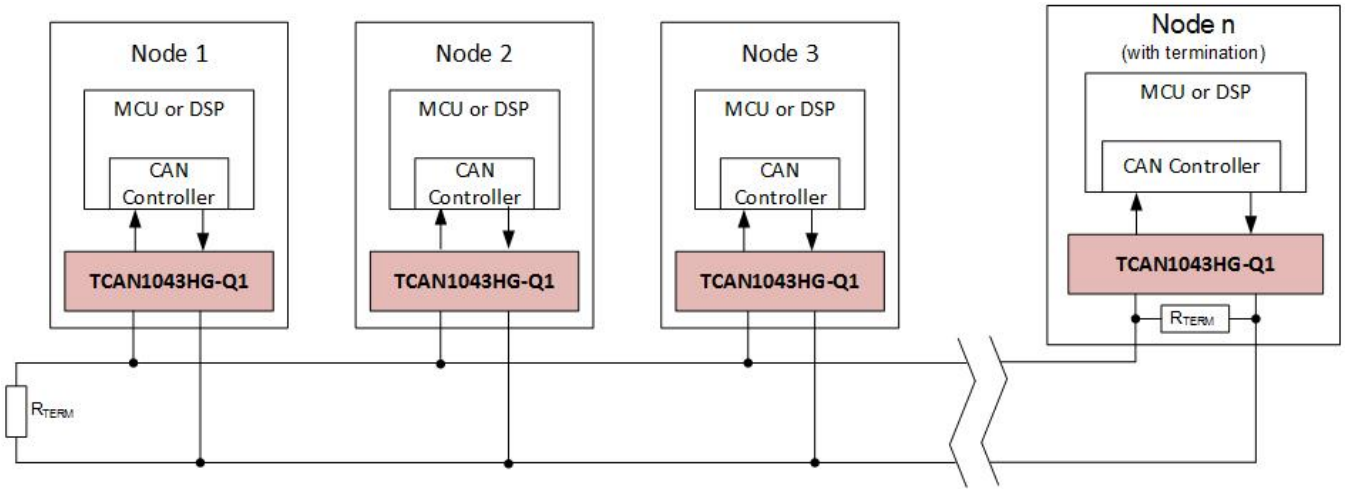


Figure 28. Typical CAN Bus Application

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may used, see Figure 29. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

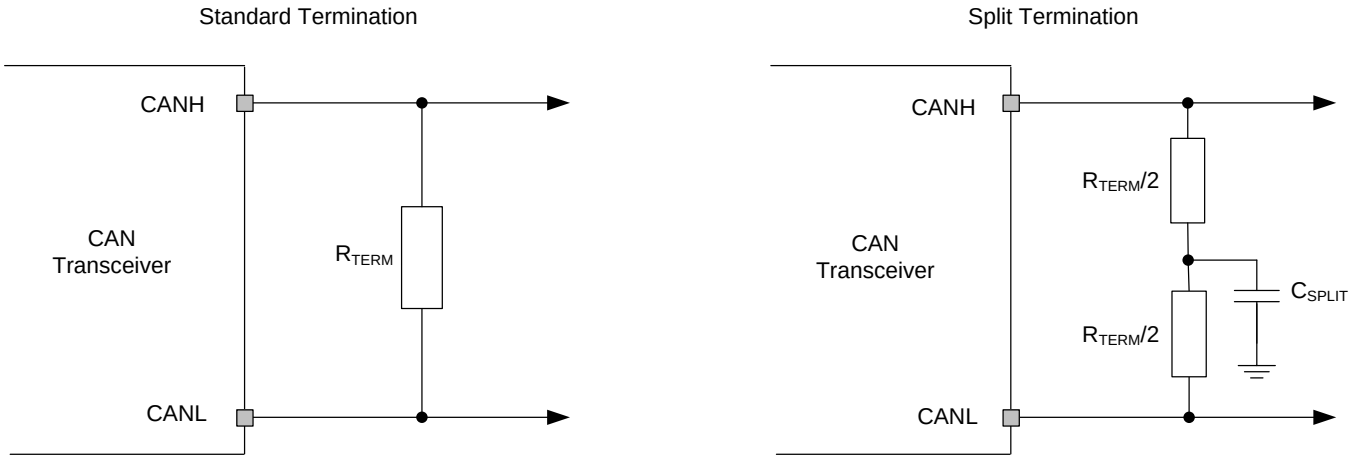
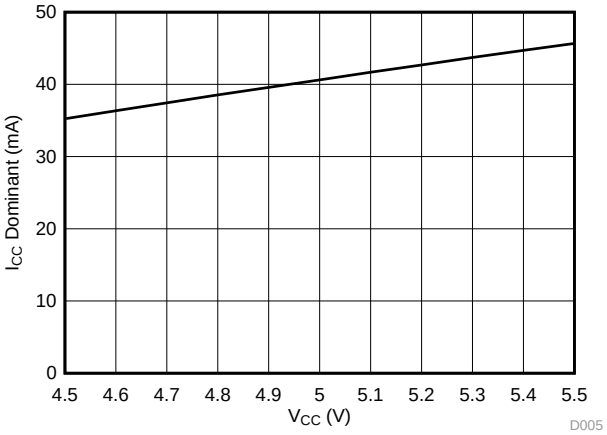


Figure 29. CAN Bus Termination Concepts

Typical Application (continued)

10.2.3 Application Curves



V_{CC} = 4.5 V to 5.5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = Open Temp = 25°C STB = 0 V

Figure 30. I_{CC} Dominant Current over V_{CC} Supply Voltage

11 Power Supply Requirements

The TCAN1043xx-Q1 device is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The device also has an IO level shifting supply input, V_{IO} , designed for a range between 2.8 V and 5.5 V. To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

ADVANCE INFORMATION

12 Layout

12.1 Layout

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

12.1.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been shown as added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C3 and C4. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the TCAN1043xx-Q1 transceiver and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.

NOTE

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Consideration for optimization and re-use between 8 Terminal to 14 Terminal CAN transceivers with and without partial networking.
- Consideration in layout for options to pursue “Dual CAN” device.
- Consideration in layout for options to pursue a SBC of a CAN plus VREG device.

12.2 Layout Example

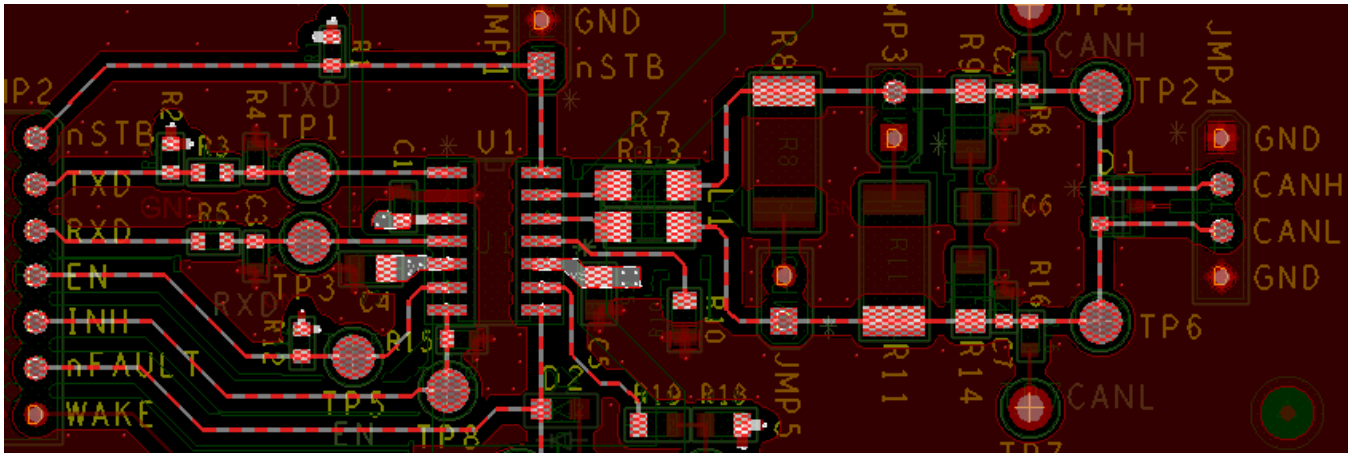


Figure 31. Example Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TCAN1043-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1043H-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1043HG-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1043G-Q1	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

tri-state, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCAN1043DQ1	PREVIEW	SOIC	D	14	75	TBD	Call TI	Call TI	-40 to 125		
PTCAN1043HGDQ1	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125		Samples
TCAN1043DMTRQ1	PREVIEW	VSON	DMT	14	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1043DMTTQ1	PREVIEW	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125		
TCAN1043DQ1	PREVIEW	SOIC	D	14	75	TBD	Call TI	Call TI	-40 to 125		
TCAN1043DRQ1	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		
TCAN1043GDMTRQ1	PREVIEW	VSON	DMT	14	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1043GDMTTQ1	PREVIEW	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125		
TCAN1043GDQ1	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125		
TCAN1043GDRQ1	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HDMTRQ1	PREVIEW	VSON	DMT	14	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HDMTTQ1	PREVIEW	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HDQ1	PREVIEW	SOIC	D	14	75	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HDRQ1	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HGDMTRQ1	PREVIEW	VSON	DMT	14	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HGDMTTQ1	PREVIEW	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HGDQ1	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125		
TCAN1043HGDRQ1	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

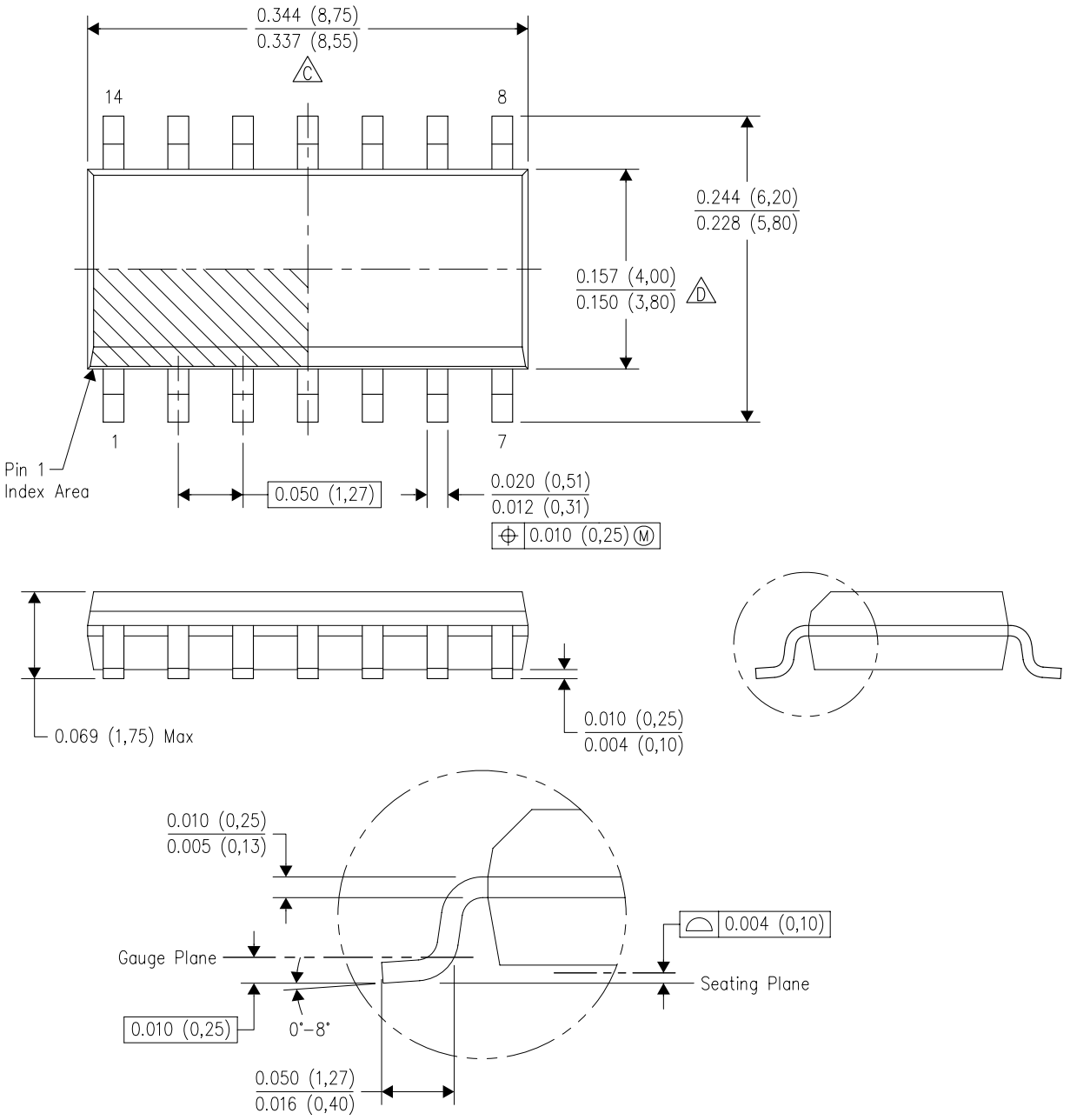
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265