

# TCA9543A Low Voltage 2-Channel I<sup>2</sup>C Bus Switch With Interrupt Logic And Reset

## 1 Features

- 1-of-2 Bidirectional Translating Switches
- I<sup>2</sup>C Bus and SMBus Compatible
- Two Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Pins Allowing up to Four TCA9543A Devices on the I<sup>2</sup>C Bus
- Channel Selection Via I<sup>2</sup>C Bus, in Any Combination
- Power-up With All Switch Channels Deselected
- Low R<sub>ON</sub> Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 1.65-V to 5.5-V
- 5.5-V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100-mA Per JESD78
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 1500-V Charged-Device Model (C101)

## 2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I<sup>2</sup>C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

## 3 Description

The TCA9543A is a dual bidirectional translating switch controlled by the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Either individual SC<sub>n</sub>/SD<sub>n</sub> channel or both channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs ( $\overline{\text{INT1}}$ – $\overline{\text{INT0}}$ ), one for each of the downstream pairs, are provided. One interrupt output ( $\overline{\text{INT}}$ ) acts as an AND of the two interrupt inputs.

An active-low reset ( $\overline{\text{RESET}}$ ) input allows the TCA9543A to recover from a situation where one of the downstream I<sup>2</sup>C buses is stuck in a low state. Pulling  $\overline{\text{RESET}}$  low resets the I<sup>2</sup>C state machine and causes both of the channels to be deselected, as does the internal power-on reset function.

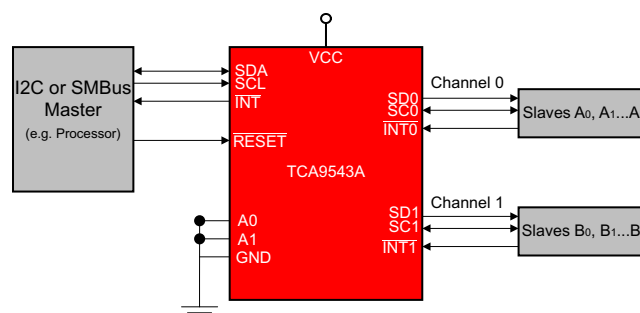
The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the TCA9543A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9543A	TSSOP (14)	5.00 mm × 4.40 mm
	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Application Diagram



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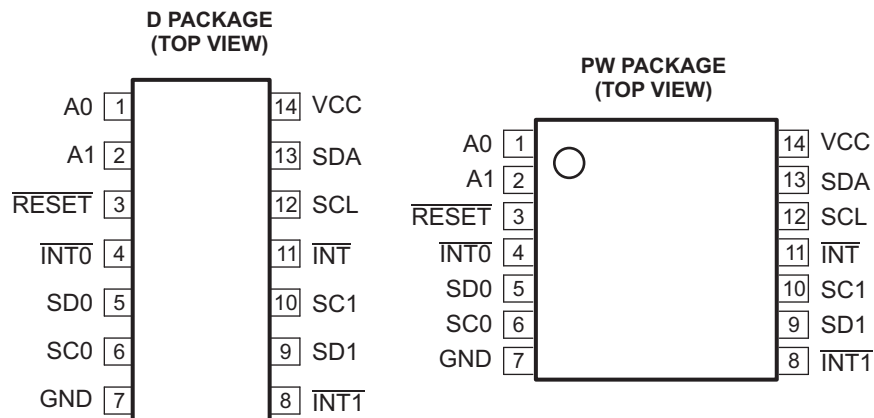
## 5 Revision History

### Changes from Original (September 2012) to Revision A

**Page**

• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Added D package to the datasheet. ....	<b>1</b>
• Changed Handling Ratings table to ESD Ratings. ....	<b>4</b>
• Added D package to the Thermal Information table. ....	<b>4</b>

## 6 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NO.	NAME D, PW	
1	A0	Address input 0. Connect directly to $V_{CC}$ or ground.
2	A1	Address input 1. Connect directly to $V_{CC}$ or ground.
3	RESET	Active-low reset input. Connect to $V_{CC}$ or $V_{DPU0}^{(1)}$ through a pull-up resistor, if not used.
4	INT0	Active-low interrupt input 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor.
5	SD0	Serial data 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor.
6	SC0	Serial clock 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor.
7	GND	Ground
8	INT1	Active-low interrupt input 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor.
9	SD1	Serial data 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor.
10	SC1	Serial clock 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor.
11	INT	Active-low interrupt output. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor.
12	SCL	Serial clock line. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor.
13	SDA	Serial data line. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor.
14	VCC	Supply power

(1)  $V_{DPUX}$  is the pull-up reference voltage for the associated data line.  $V_{DPUM}$  is the master I<sup>2</sup>C reference voltage while  $V_{DPU0}$  and  $V_{DPU1}$  are the slave channel reference voltages.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
I <sub>I</sub>	Input current		±20	mA
I <sub>O</sub>	Output current		±25	mA
	Continuous current through VCC		±100	mA
	Continuous current through GND		±100	mA
P <sub>tot</sub>	Total power dissipation		400	mW
T <sub>A</sub>	Operating free-air temperature range	-40	85	°C
T <sub>stg</sub>	Storage temperature range	-60	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6
		A1, A0, INT1, INT0, RESET	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>
		A1, A0, INT1, INT0, RESET	-0.5	0.3 × V <sub>CC</sub>
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TCA9543A		UNIT	
	PW	D		
	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	130.9	102.8	°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	59.2	63.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	72.7	57.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.5	26.7	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	72.1	56.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>PORR</sub>	Power-on reset voltage, VCC rising	No load: V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>				1.2	1.5	V
V <sub>PORF</sub>	Power-on reset voltage, VCC falling <sup>(4)</sup>	No load: V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>			0.8	1		V
V <sub>pass</sub>	Switch output voltage	V <sub>SWin</sub> = V <sub>CC</sub> , I <sub>SWout</sub> = -100 μA		5 V		3.6		V
				4.5 V to 5.5 V		2.6	4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.4		
				2.3 V to 2.7 V	1.0		1.8	
				1.8 V		0.8		
			1.65 V to 1.95 V	0.5		1.1		
I <sub>OH</sub>	$\overline{\text{INT}}$	V <sub>O</sub> = V <sub>CC</sub>		1.65 V to 5.5 V			10	μA
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V		1.65 V to 5.5 V	3	7		mA
		V <sub>OL</sub> = 0.6 V			6	10		
I <sub>I</sub>	$\overline{\text{INT}}$	V <sub>OL</sub> = 0.4 V			3			
	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V	-1		1	μA
	SC1–SC0, SD1–SD0	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V	-1		1	
	A1, A0	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V	-1		1	
	$\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V	-1		1	
$\overline{\text{RESET}}$	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V	-1		1		
I <sub>CC</sub>	Operating mode	f <sub>SCL</sub> = 400 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup> I <sub>O</sub> = 0 t <sub>r,max</sub> = 300 ns	5.5 V		50		μA
				3.6 V		20		
				2.7 V		11		
				1.65 V		6		
				5.5 V		35		
				3.6 V		14		
				2.7 V		5		
	1.65 V		2					
	Standby mode	Low inputs	V <sub>I</sub> = GND <sup>(3)</sup> I <sub>O</sub> = 0	5.5 V	1.6	2		
				3.6 V	1.0	1.3		
				2.7 V	0.7	1.1		
				1.65 V	0.4	0.55		
		High inputs	V <sub>I</sub> = V <sub>CC</sub> I <sub>O</sub> = 0	5.5 V	1.6	2		
				3.6 V	1.0	1.3		
2.7 V				0.7	1.1			
1.65 V	0.4	0.55						
ΔI <sub>CC</sub>	Supply-current change	$\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$	One $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ input at 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V		3	20	μA
			One $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>			3	20	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>			2	15	
			SCL or SDA input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>			2	15	

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V<sub>CC</sub>), T<sub>A</sub> = 25°C.

(3)  $\overline{\text{RESET}}$  = V<sub>CC</sub> (held high) when all other input voltages, V<sub>I</sub> = GND

(4) The power-on reset circuit resets the I<sup>2</sup>C bus logic when V<sub>CC</sub> < V<sub>PORF</sub>.

## Electrical Characteristics<sup>(1)</sup> (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
C <sub>i</sub>	A1, A0	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V	4.5	6		pF
	$\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V	4.5	6		
	$\overline{\text{RESET}}$	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V	4.5	5.5		
C <sub>io(OFF)</sub> <sup>(5)</sup>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup> , Switch OFF	1.65 V to 5.5 V	15	19		pF
	SC1–SC0, SD1–SD0			6	8		
R <sub>ON</sub>	Switch on-state resistance	V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA	4.5 V to 5.5 V	4	10	16	Ω
			3 V to 3.6 V	5	13	20	
		V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 10 mA	2.3 V to 2.7 V	7	16	45	
			1.65 V to 1.95 V	10	25	70	

 (5) C<sub>io(ON)</sub> depends on the device capacitance and load that is downstream from the device.

## 7.6 I<sup>2</sup>C Interface Timing Requirements

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 5](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		0 <sup>(1)</sup>		μs
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start		4.7	1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup		4.7	0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold		4	0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup		4	0.6		μs
t <sub>vdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid	1		1	μs
t <sub>vdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid	0.6		0.6	μs
t <sub>vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low	1		1	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		400	pF

 (1) A device internally must provide a hold time of at least 300-ns for the SDA signal (referred to as the V<sub>IH</sub> min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

 (2) C<sub>b</sub> = total bus capacitance of one bus line in pF

 (3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see [Figure 5](#))

## 7.7 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 7](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{(1)}$	Propagation delay time	$R_{ON} = 20 \Omega, C_L = 15$ pF	SDA or SCL	SDn or SCn	0.3	ns
		$R_{ON} = 20 \Omega, C_L = 50$ pF			1	
$t_{iv}$	Interrupt valid time <sup>(2)</sup>	$\overline{INTn}$	$\overline{INT}$		4	$\mu$ s
$t_{ir}$	Interrupt reset delay time <sup>(2)</sup>	$\overline{INTn}$	$\overline{INT}$		2	$\mu$ s

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) Data taken using a 4.7-k $\Omega$  pullup resistor and 100-pF load (see [Figure 7](#))

## 7.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7](#))

PARAMETER		MIN	MAX	UNIT
$t_{PWRL}$	Required low-level pulse duration of $\overline{INTn}$ inputs <sup>(1)</sup>	1		$\mu$ s
$t_{PWRH}$	Required high-level pulse duration of $\overline{INTn}$ inputs <sup>(1)</sup>	0.5		$\mu$ s
$t_{WL}$	Pulse duration, $\overline{RESET}$ low	4		ns
$t_{rst}^{(2)}$	$\overline{RESET}$ time (SDA clear)		500	ns
$t_{REC}$	Recovery time from $\overline{RESET}$ to start	0		ns

(1) The device has interrupt input rejection circuitry for pulses less than the listed minimum.

(2)  $t_{rst}$  is the propagation delay measured from the time the  $\overline{RESET}$  terminal is first asserted low to the time the SDA terminal is asserted high, signaling a stop condition. It must be a minimum of  $t_{WL}$ .

### 7.9 Typical Characteristics

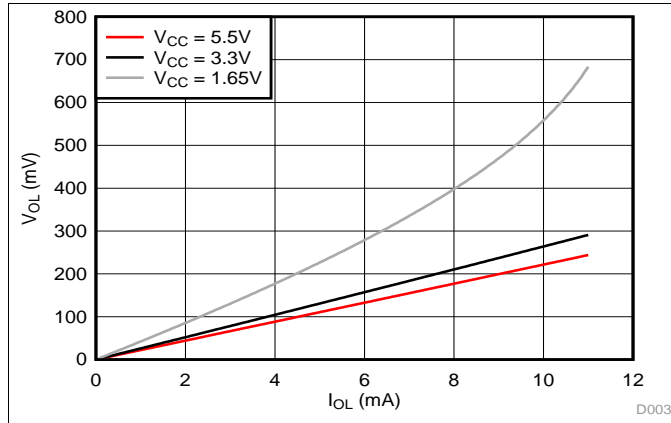


Figure 1. SDA Output Low Voltage ( $V_{OL}$ ) vs Load Current ( $I_{OL}$ ) at Three  $V_{CC}$  Levels

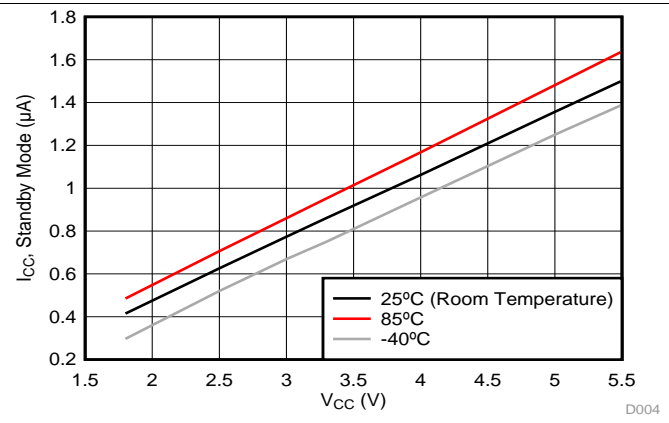


Figure 2. Standby Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points

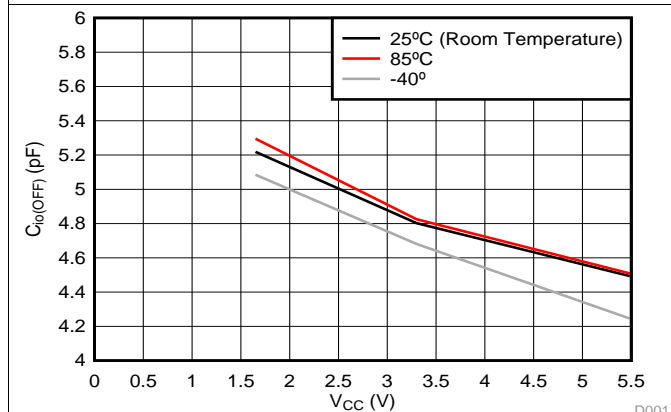


Figure 3. Slave channel (SCn/SDn) capacitance ( $C_{io(OFF)}$ ) vs. Supply Voltage ( $V_{CC}$ ) at Three Temperature Points

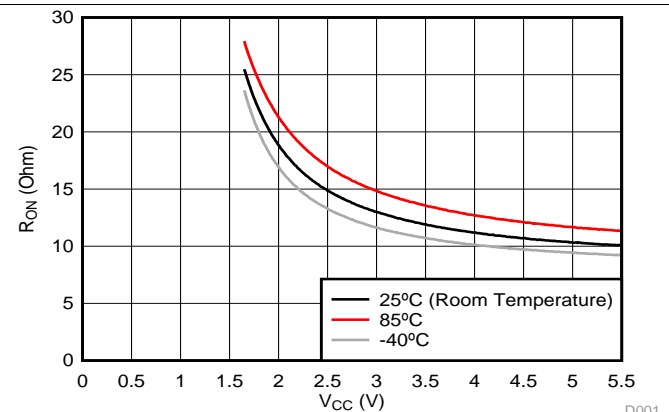
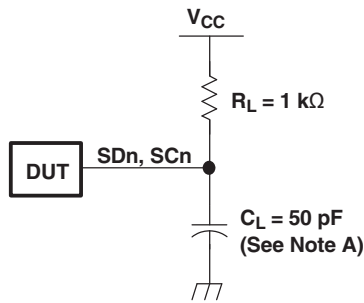


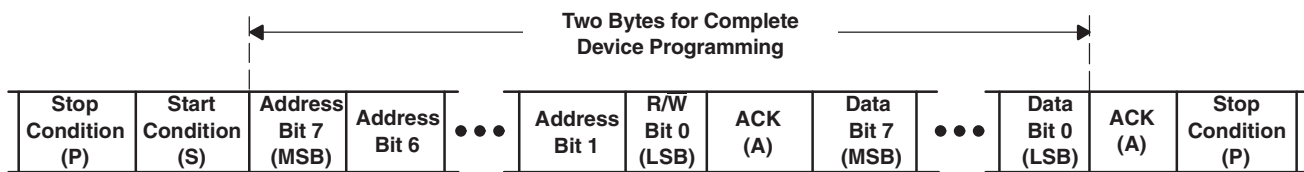
Figure 4. ON-Resistance ( $R_{ON}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperatures



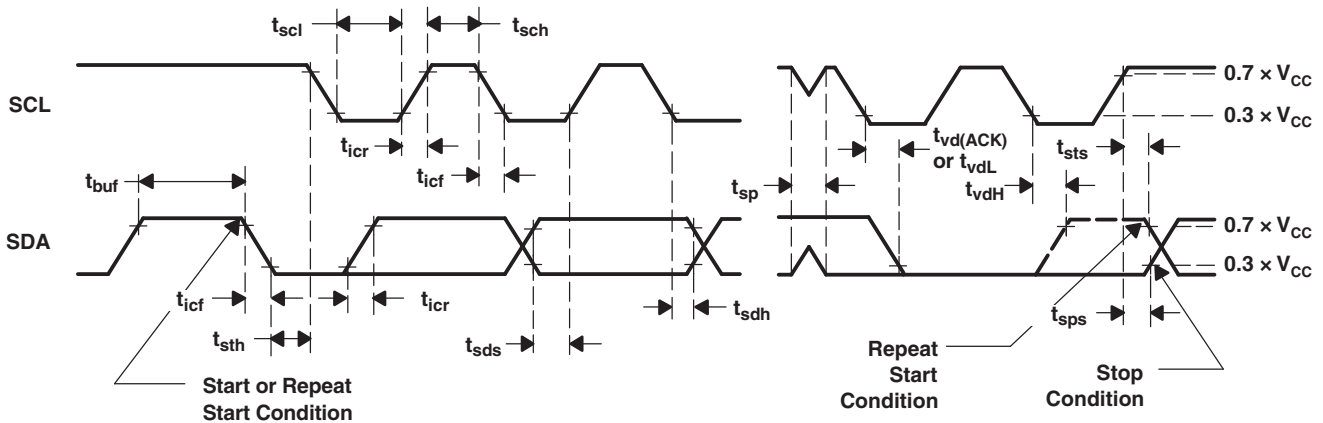
## 8 Parameter Measurement Information



I<sup>2</sup>C PORT LOAD CONFIGURATION



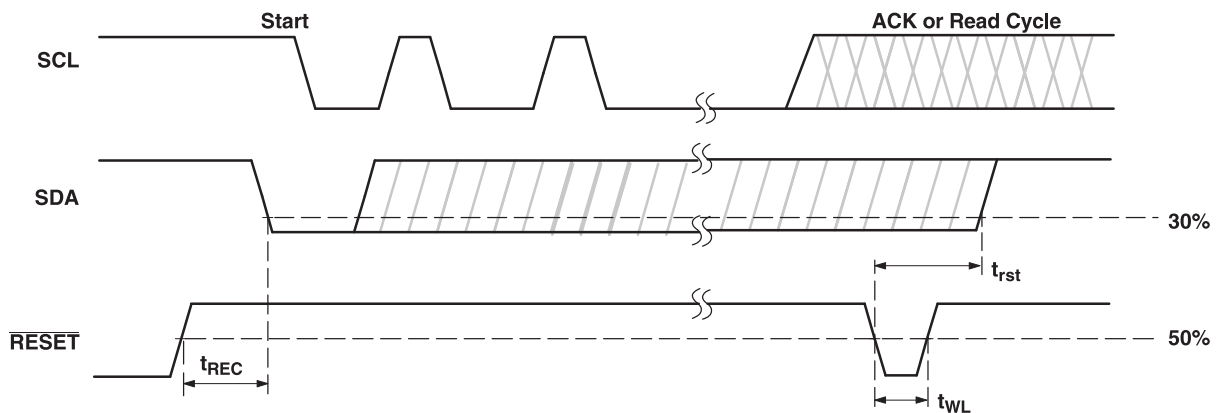
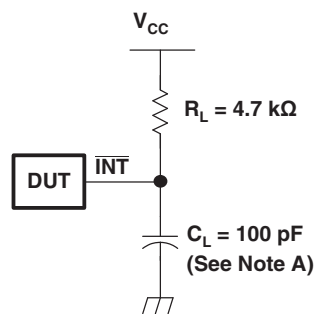
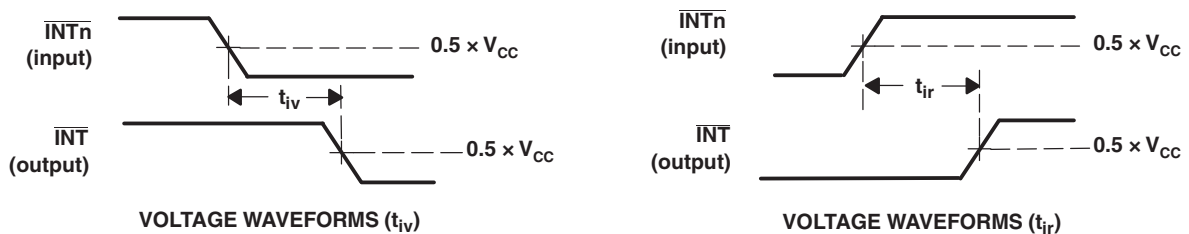
BYTE	DESCRIPTION
1	I <sup>2</sup> C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 30$  ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 5. I<sup>2</sup>C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

**Parameter Measurement Information (continued)**

**Figure 6. Reset Timing**

**INTERRUPT LOAD CONFIGURATION**


- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 30$  ns.

**Figure 7. Interrupt Load Circuit and Voltage Waveforms**

## 9 Detailed Description

### 9.1 Overview

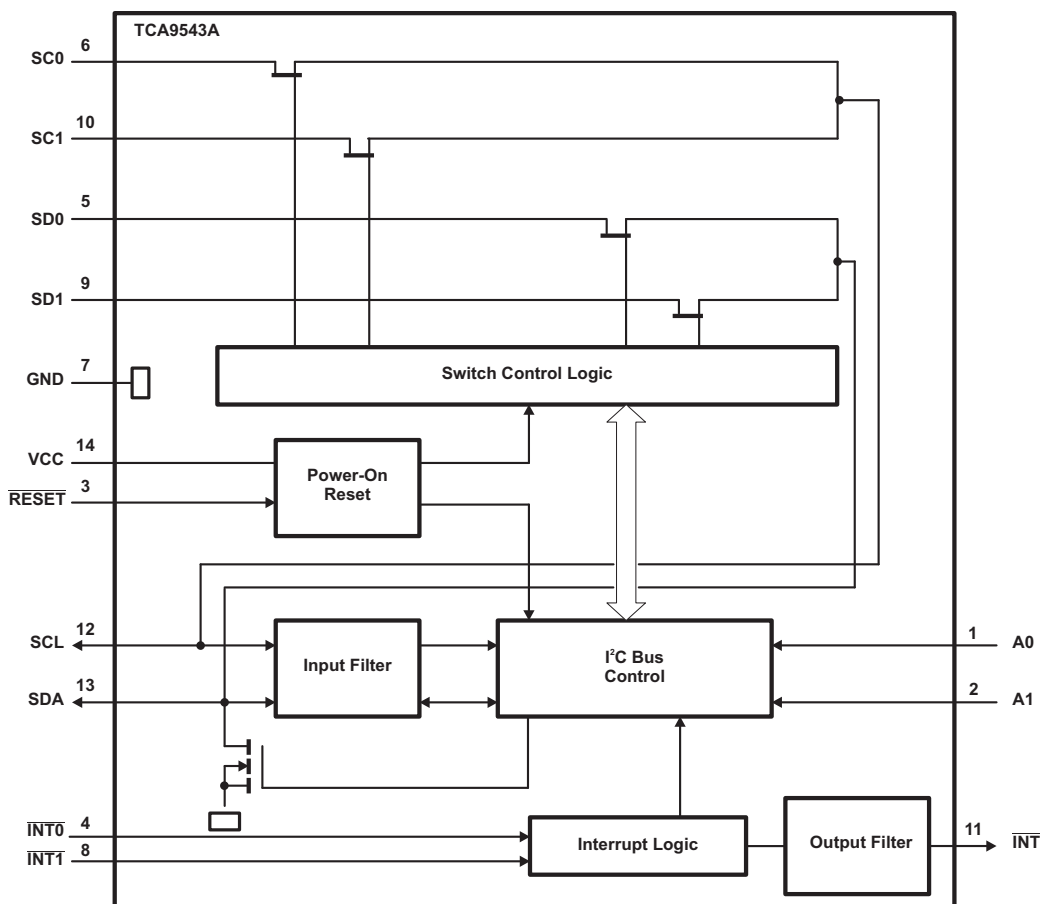
The TCA9543A is a 2-channel, bidirectional translating I<sup>2</sup>C switch. The master SCL/SDA signal pair is directed to two channels of slave devices, SC0/SD0-SC1/SD1. Either individual downstream channel can be selected as well as both channels. The TCA9543A also supports interrupt signals in order for the master to detect an interrupt on the  $\overline{\text{INT}}$  output terminal that can result from any of the slave devices connected to the INT1-INT0 input terminals.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the TCA9543A to recover should one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V<sub>CC</sub>, also known as a power-on reset (POR). Either using the  $\overline{\text{RESET}}$  function or causing a POR will cause both channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C master device that is switched to communicate with multiple I<sup>2</sup>C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The TCA9543A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

The TCA9543A is a dual channel bidirectional translating switch for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9543A features I<sup>2</sup>C control using a single 8-bit control register in which bits 1 and 0 control the enabling and disabling of the two switch channels of I<sup>2</sup>C data flow. The TCA9543A also supports interrupt signals for each slave channel and this data is held in bits 5 and 4 of the control register. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the TCA9543A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I<sup>2</sup>C bus enters a fault state, the TCA9543A can be reset to resume normal operation using the RESET terminal feature or by a power-on reset which results from cycling power to the device.

### 9.4 Device Functional Modes

#### 9.4.1 RESET Input

The RESET input can be used to recover the TCA9543A from a bus-fault condition. The registers and the I<sup>2</sup>C state machine within this device initialize to their default states if this signal is asserted low for a minimum of  $t_{WHL}$ . Both channels also are deselected in this case. RESET must be connected to V<sub>CC</sub> through a pull-up resistor.

#### 9.4.2 Power-On Reset

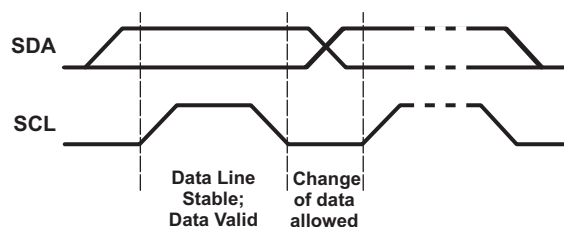
When power is applied to V<sub>CC</sub>, an internal power-on reset holds the TCA9543A in a reset condition until V<sub>CC</sub> has reached V<sub>PORR</sub>. At this point, the reset condition is released and the TCA9543A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V<sub>CC</sub> must be lowered below V<sub>PORF</sub> to reset the device.

### 9.5 Programming

#### 9.5.1 I<sup>2</sup>C Interface

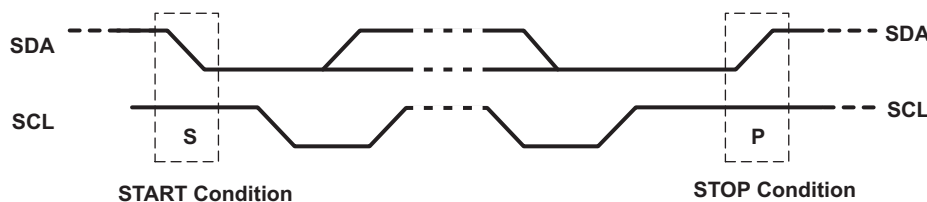
The I<sup>2</sup>C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time is interpreted as control signals (see Figure 8).



**Figure 8. Bit Transfer**

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 9).



**Figure 9. Definition of Start and Stop Conditions**

### Programming (continued)

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see Figure 10).

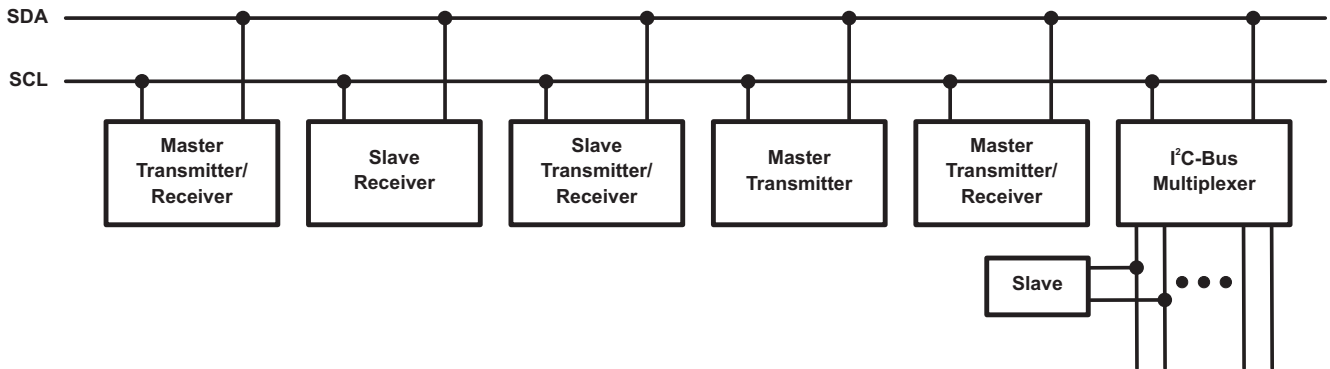


Figure 10. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 11). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

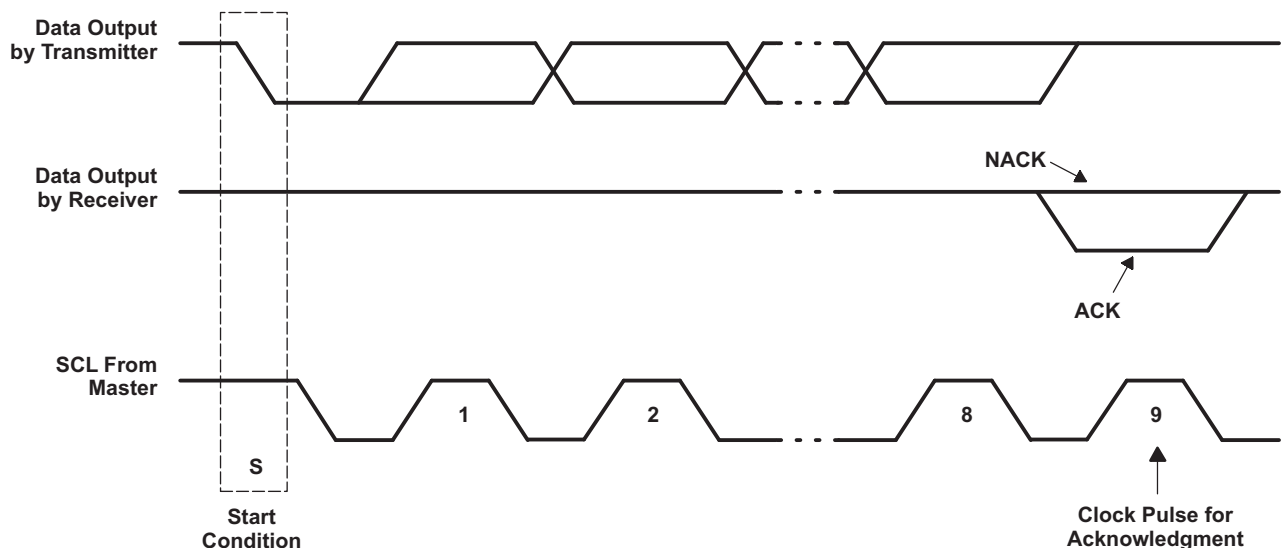


Figure 11. Acknowledgment on I<sup>2</sup>C Bus

Data is transmitted to the TCA9543A control register using the write mode shown in Figure 12.

## Programming (continued)

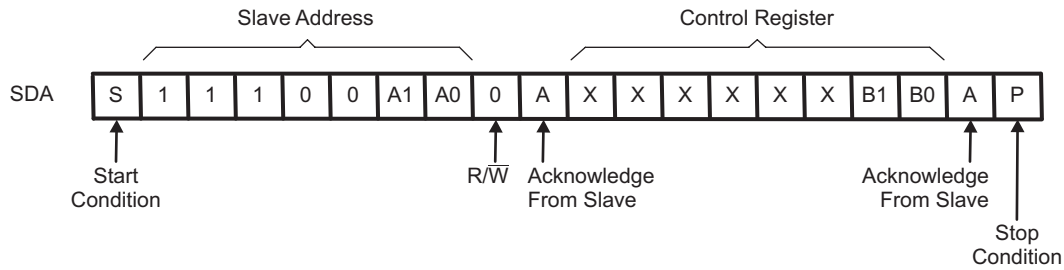


Figure 12. Write Control Register

Data is read from the TCA9543A control register using the read mode shown in Figure 13.

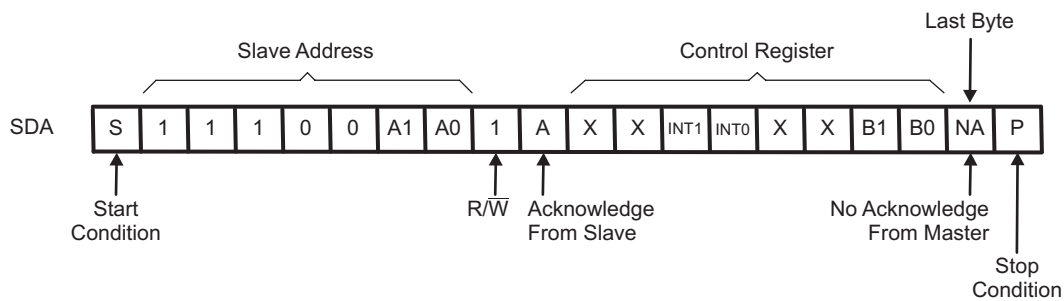


Figure 13. Read Control Register

## 9.6 Register Maps

### 9.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the TCA9543A is shown in Figure 14. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address terminals and they must be pulled high or low.

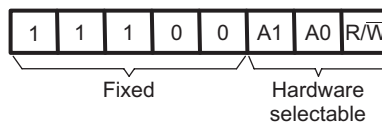


Figure 14. Slave Address TCA9543A

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

### 9.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TCA9543A, which is stored in the control register (see Figure 15). If multiple bytes are received by the TCA9543A, it saves the last byte received. This register can be written and read via the I<sup>2</sup>C bus.

## Register Maps (continued)

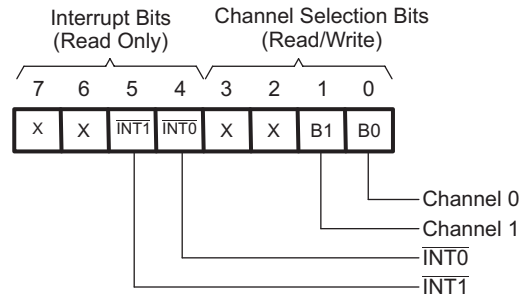


Figure 15. Control Register

### 9.6.3 Control Register Definition

One or both SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the TCA9543A has been addressed, the control register is written. The two LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)<sup>(1)</sup>

D7	D6	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$	D3	D2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

### 9.6.4 Interrupt Handling

The TCA9543A provides two interrupt inputs (one for each channel) and one open-drain interrupt output (see [Table 2](#)). When an interrupt is generated by any device, it is detected by the TCA9543A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bit 4 and Bit 5 of the control register correspond to the  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$  inputs of the TCA9543A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the TCA9543A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the TCA9543A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to  $V_{CC}$  through a pull-up resistor.

**Table 2. Control Register Read (Interrupt)<sup>(1)</sup>**

D7	D6	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$	D3	D2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Two interrupts can be active at the same time.



## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

Applications of the TCA9543A will contain an I<sup>2</sup>C (or SMBus) master device and up to two I<sup>2</sup>C slave devices. The downstream channels are ideally used to resolve I<sup>2</sup>C slave address conflicts. For example, if two identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0 and 1. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and the other channel switched off, the data can be retrieved, and the I<sup>2</sup>C master can move on and read the next channel.

In an application where the I<sup>2</sup>C bus will contain many additional slave devices that do not result in I<sup>2</sup>C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across both channels. If both switches will be enabled simultaneously, additional design requirements must be considered (See [Design Requirements](#) and [Detailed Design Procedure](#)).

### 10.2 Typical Application

A typical application of the TCA9543A will contain anywhere from 1 to 3 separate data pull-up voltages,  $V_{DPUX}$ , one for the master device ( $V_{DPU M}$ ) and one for each of the selectable slave channels ( $V_{DPU 0}$  and  $V_{DPU 1}$ ). In the event where the master device and both slave devices operate at the same voltage, then the pass voltage,  $V_{pass} = V_{DPU X}$ . Once the maximum  $V_{pass}$  is known,  $V_{CC}$  can be selected easily using [Figure 17](#). In an application where voltage translation is necessary, additional design requirements must be considered (See [Design Requirements](#)).

[Figure 16](#) shows an application in which the TCA9543A can be used.

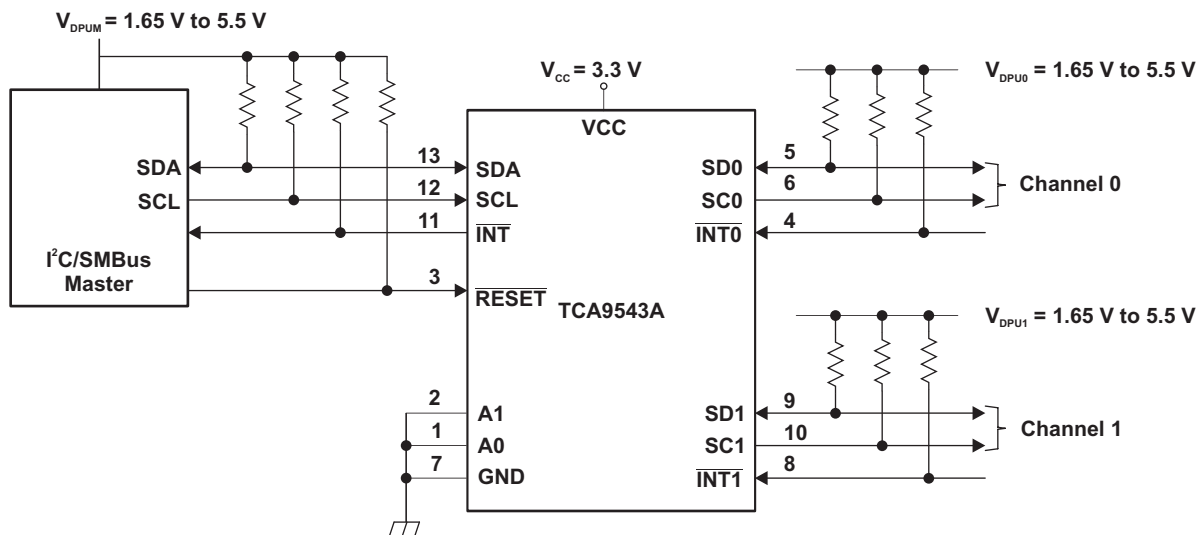


Figure 16. Typical Application Schematic

#### 10.2.1 Design Requirements

The pull-up resistors on the  $\overline{INT1}$ - $\overline{INT0}$  terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

## Typical Application (continued)

The A0 and A1 terminals are hardware selectable to control the slave address of the TCA9543A. These terminals may be tied directly to GND or  $V_{CC}$  in the application.

If both slave channels will be activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the TCA9543A are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

Figure 17 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the TCA9543A to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 17,  $V_{pass(max)}$  is 2.7 V when the TCA9543A supply voltage is 4 V or lower, so the TCA9543A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 16).

### 10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of  $V_{DPUX}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9543A,  $C_{io(OFF)}$ , the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If both channels will be activated simultaneously, each of the slaves on both channels will contribute to total bus capacitance.

Typical Application (continued)

10.2.3 Application Curves

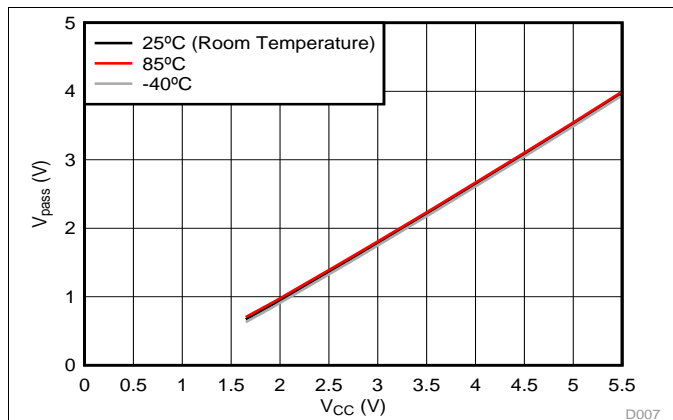
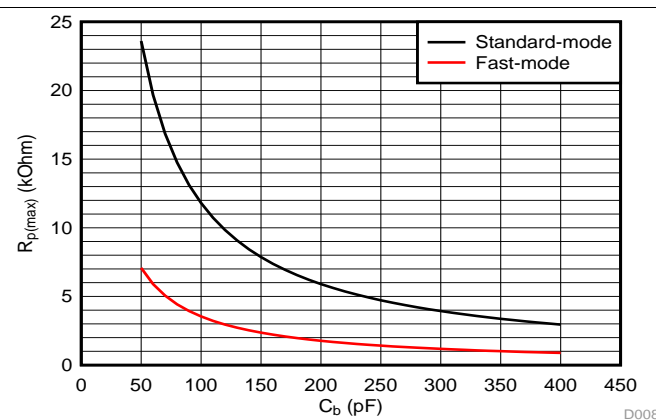
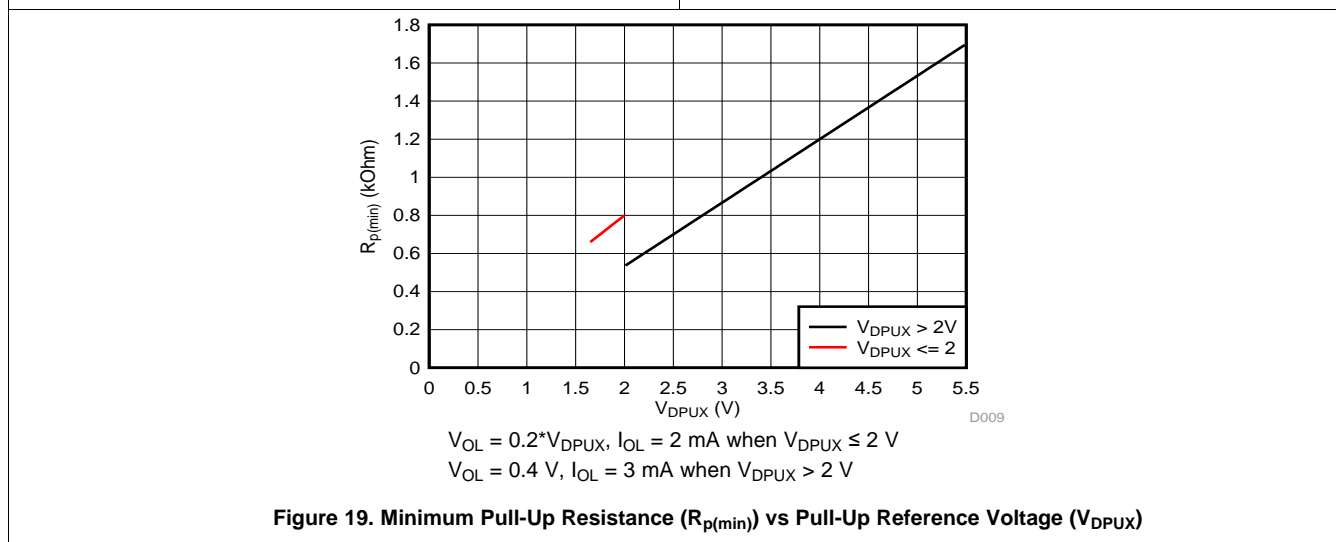


Figure 17. Pass-Gate Voltage (V<sub>pass</sub>) vs Supply Voltage (V<sub>CC</sub>) at Three Temperature Points



Standard-mode (f<sub>SCL</sub> = 100 kHz, t<sub>r</sub> = 1 μs)      Fast-mode (f<sub>SCL</sub> = 400 kHz, t<sub>r</sub> = 300 ns)

Figure 18. Maximum Pull-Up Resistance (R<sub>p(max)</sub>) vs Bus Capacitance (C<sub>b</sub>)



V<sub>OL</sub> = 0.2 \* V<sub>DPUX</sub>, I<sub>OL</sub> = 2 mA when V<sub>DPUX</sub> ≤ 2 V  
 V<sub>OL</sub> = 0.4 V, I<sub>OL</sub> = 3 mA when V<sub>DPUX</sub> > 2 V

Figure 19. Minimum Pull-Up Resistance (R<sub>p(min)</sub>) vs Pull-Up Reference Voltage (V<sub>DPUX</sub>)

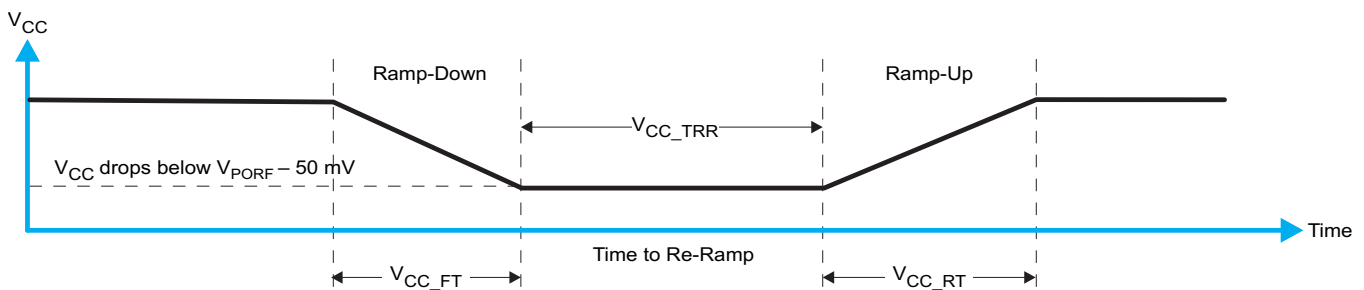
## 11 Power Supply Recommendations

The operating power-supply voltage range of the TCA9543A is 1.65-V to 5.5-V applied at the VCC terminal. When the TCA9543A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I<sup>2</sup>C bus logic is initialized properly.

### 11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9543A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in [Figure 20](#).



**Figure 20. V<sub>CC</sub> is Lowered Below the POR Threshold, Then Ramped Back Up to V<sub>CC</sub>**

[Table 3](#) specifies the performance of the power-on reset feature for TCA9543A for both types of power-on reset.

**Table 3. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>**

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>CC_FT</sub>	Fall time	1		100	ms
V <sub>CC_RT</sub>	Rise time	0.1		100	ms
V <sub>CC_TRR</sub>	Time to re-ramp (when V <sub>CC</sub> drops below V <sub>PORF(min)</sub> – 50 mV or when V <sub>CC</sub> drops to GND)	40			μs
V <sub>CC_GH</sub>	Level that V <sub>CC</sub> can glitch down to, but not cause a functional disruption when V <sub>CC_GW</sub> = 1 μs			1.2	V
V <sub>CC_GW</sub>	Glitch width that will not cause a functional disruption when V <sub>CC_GH</sub> = 0.5 × V <sub>CC</sub>			10	μs
V <sub>PORF</sub>	Voltage trip point of POR on falling V <sub>CC</sub>	0.8		1.25	V
V <sub>PORR</sub>	Voltage trip point of POR on rising V <sub>CC</sub>	1.05		1.5	V

(1) All supply sequencing and ramp rate values are measured at T<sub>A</sub> = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 21 and Table 3 provide more information on how to measure these specifications.

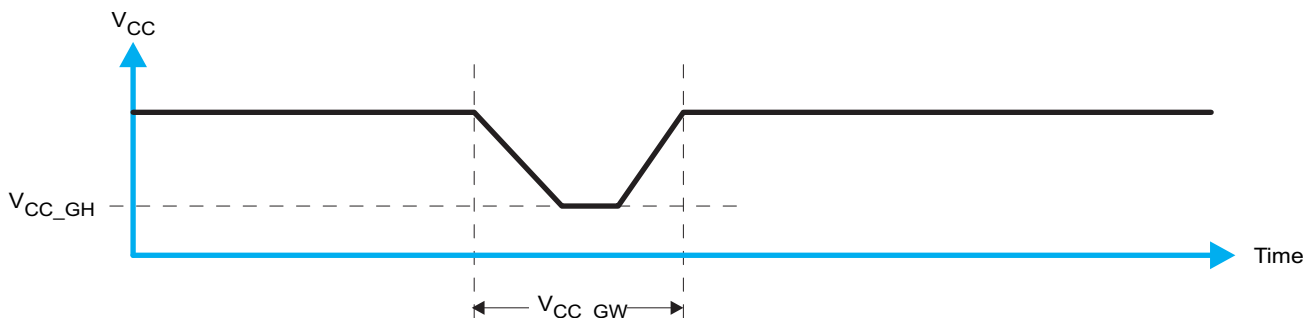


Figure 21. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 22 and Table 3 provide more details on this specification.

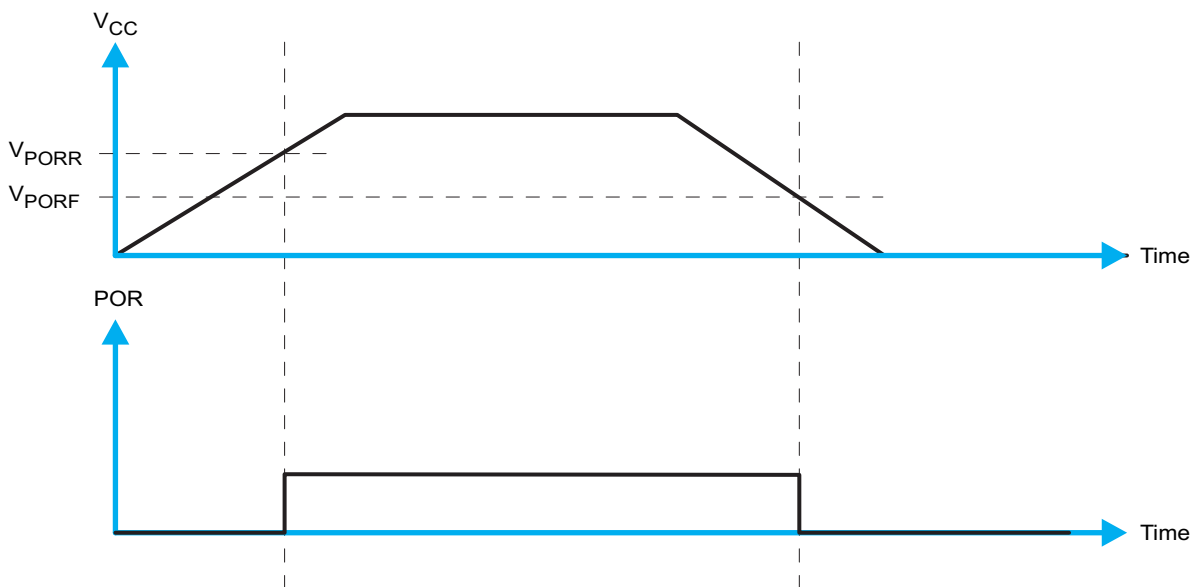


Figure 22.  $V_{POR}$

## 12 Layout

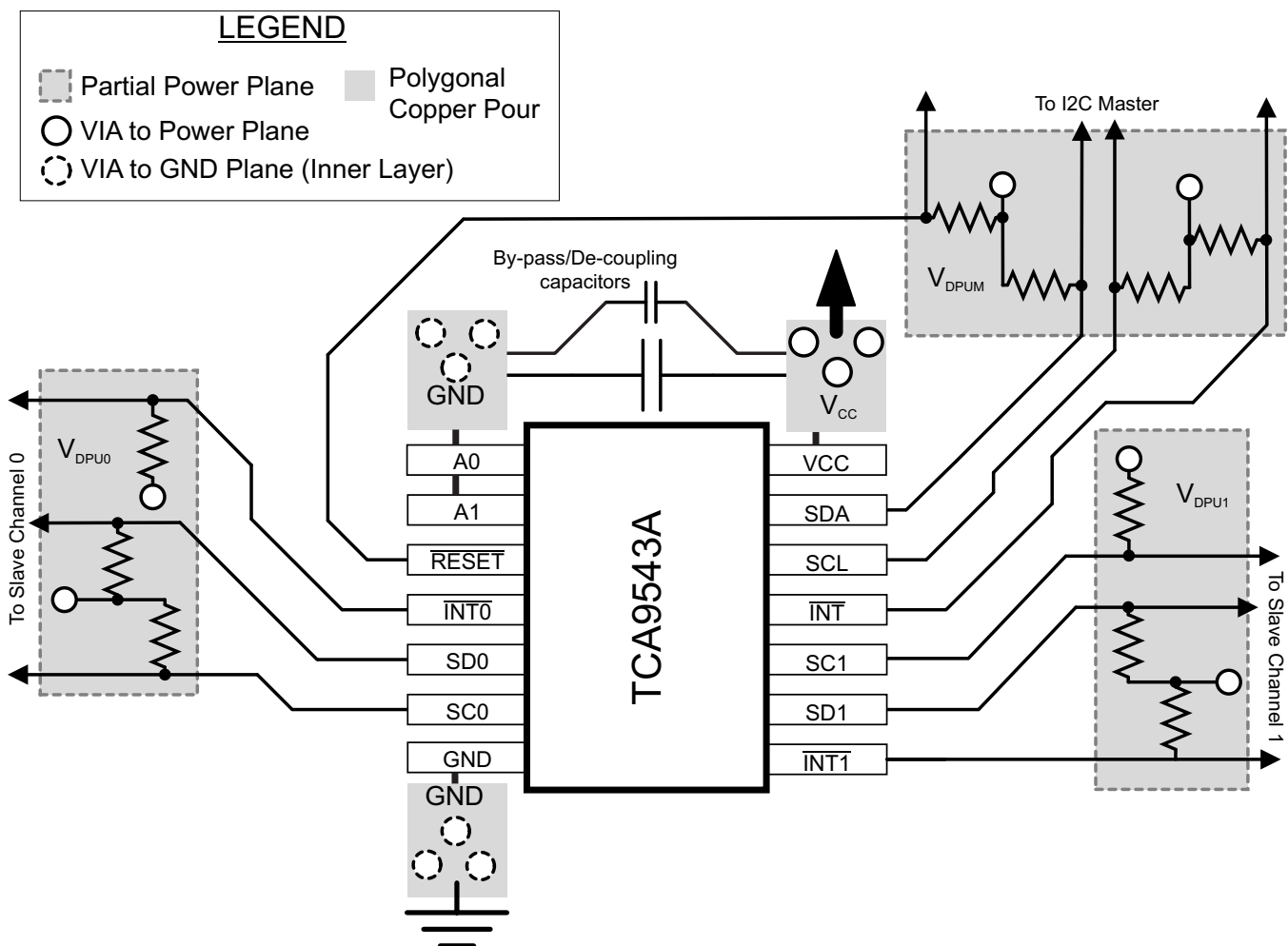
### 12.1 Layout Guidelines

For PCB layout of the TCA9543A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all  $V_{DPUX}$  voltages and  $V_{CC}$  could be at the same potential and a single copper plane can connect all of the pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required,  $V_{DPUM}$ ,  $V_{DPU0}$ , and  $V_{DPU1}$ , may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SC<sub>n</sub>, SD<sub>n</sub> and  $\overline{INT}_n$ ) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

### 12.2 Layout Example



**Figure 23. Layout Example**

## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9543ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9543A	<a href="#">Samples</a>
TCA9543APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW543A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9543ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCA9543APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9543ADR	SOIC	D	14	2500	367.0	367.0	38.0
TCA9543APWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

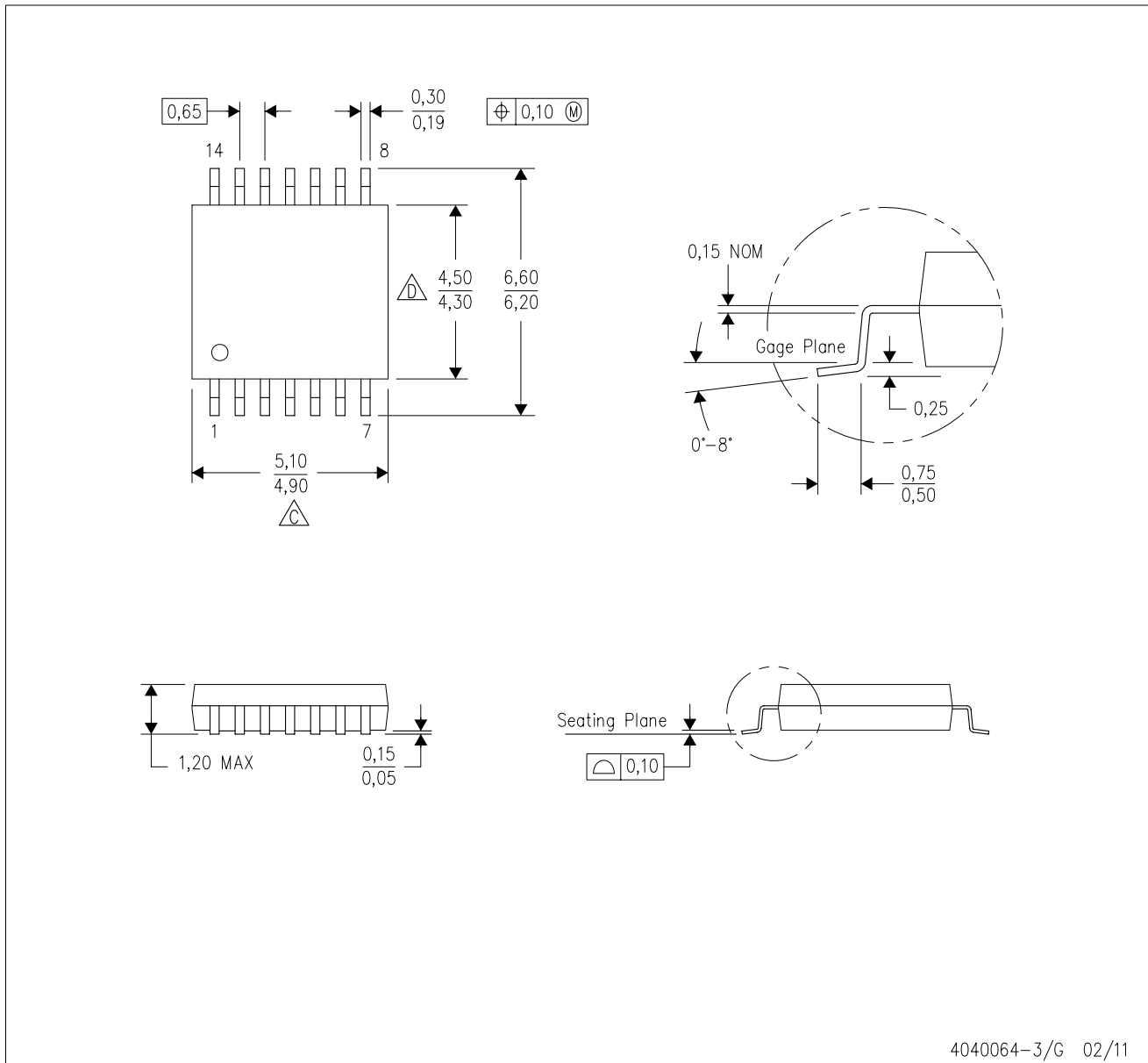
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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