1. GENERAL

The TC8830AF is a single chip CMOS LSI for voice recording / playback using the ADM (Adaptive Delta Modulation). It composes a voice recording system with a static RAM for voice memory and an audio circuit including a microphone, speaker, amplifier, etc. as an external circuit.

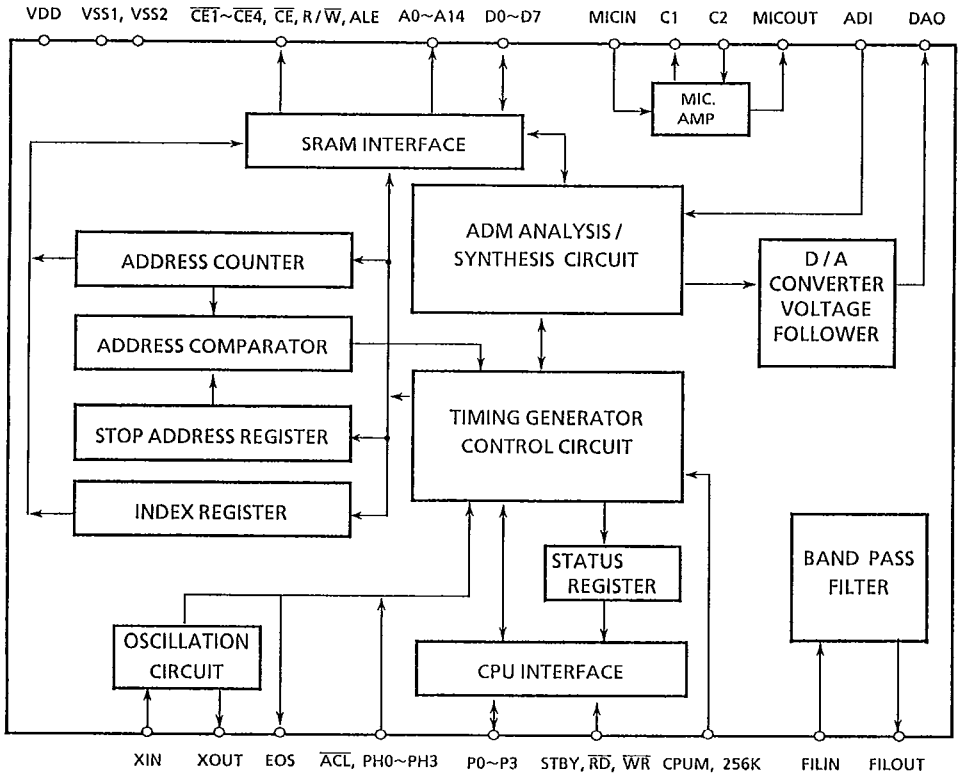
2. FEATURES

- ☐ SRAMs (Static RAM) are used as a voice data memory up to 4 pieces of 64Kbit, or 4 pieces of 256Kbit.
- ☐ It's possible to expanse at memory up to 8Mbit by external circuit.
- ☐ It's connectable to microprocessor easily and controlled by 11 kinds of command.
- ☐ Capable of recording / playback maximum 16 phrases at the manual control.
- ☐ 4 kinds of bit rates (32K, 16K, 11K, 8K bps) are provided.
- ☐ Recording / playback time is up to sixty four seconds (with four 256Kbit SRAMs and bit rate to be 16K bps).
- ☐ On-chip microphone amplifier for recording and band pass filter for playback.
- ☐ It's possible to memory back up by standby function.
- ☐ On-chip ceramic oscillation circuit.
- ☐ Single 5V power supply.
- ☐ 67-pin flat package.

◦ The bit rate means the number of bits per second to be used.

3. BLOCK DIAGRAM AND SYSTEM CONFIGURATION

3.1 TC8830AF Block Diagram



3.2 Block Diagram Description

(1) Address counter

The 20-bit counter to indicate address of the external SRAMs and counted up with 8 sampling under recording and playback. Values can be set or read by commands at the CPU control.

(2) Stop Address register

The 20-bit register to indicate address to stop recording / playback. Values can be set by commands at the CPU control, but can not be read.

(3) Address comparator

When the contents of the address counter agree with those of the stop address register, the address counter is stopped.

(4) Index register

The register to indicate address of the index area on SRAMs in the label index mode (Refer to section 5.3).

(5) Status register

The 4-bit register which shows the status of TC8830AF. When $\overline{RD}$ pin is L label, TC8830AF gives this contents to data bus (P0~P3) at the CPU control.

(6) CPU interface

The interface circuit for the external microprocessor. This circuit has also the chattering elimination circuit in the manual control. This chattering elimination circuit has an effect on P0 to P3 pins (Start and Stop etc.).

(7) Sram interface

The interface circuit for the external SRAM.

(8) Microphone amplifier

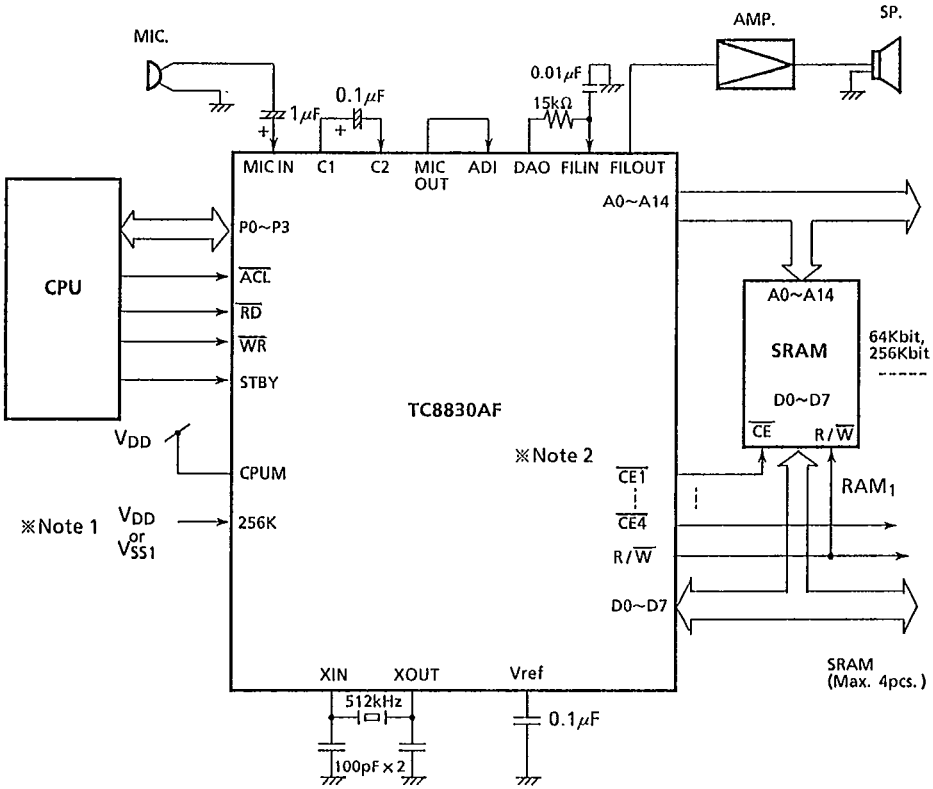
Output of MICOUT pin is biased to Vref level, and can be connected directly to ADI pin.

(9) Band pass filter

On chip the 1'st order high pass filter and 2'nd order low pass filter.

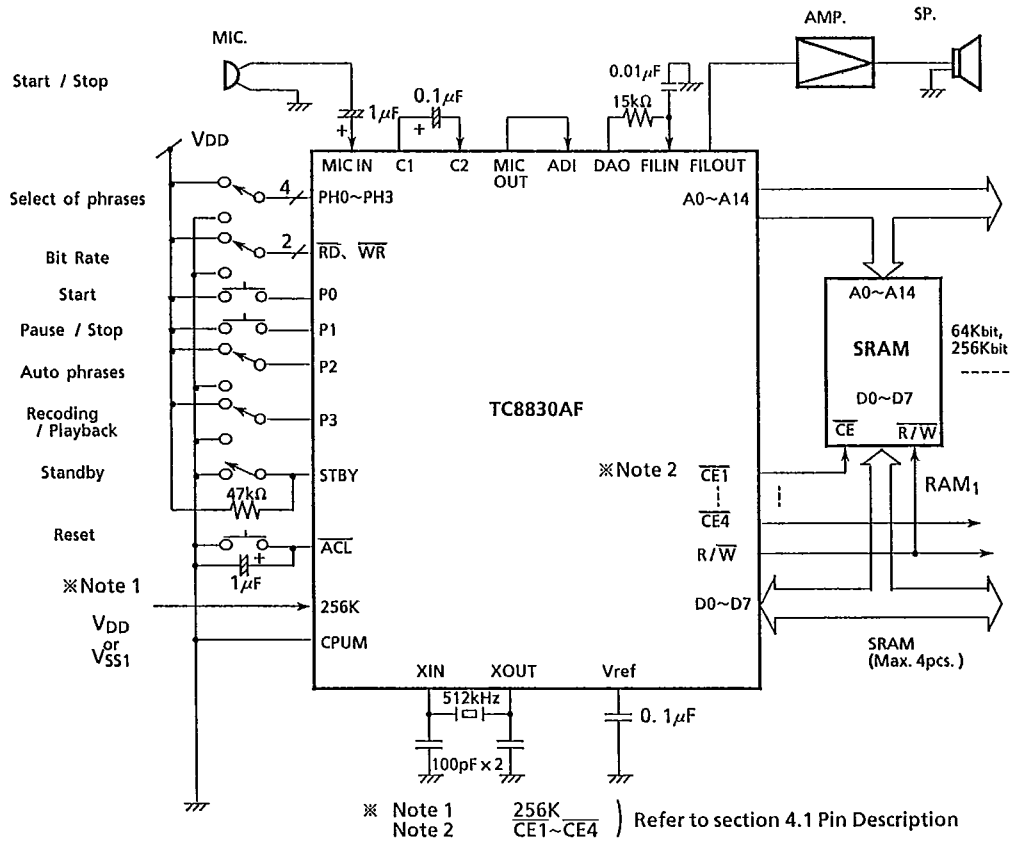
3.3 Example of Voice Recording System

3.3.1 CPU Control Type

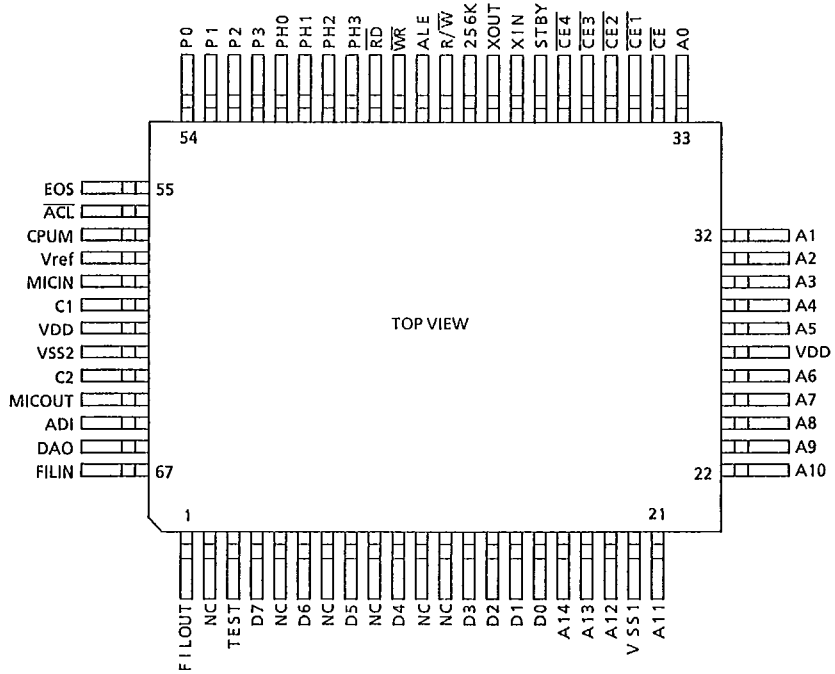


※ Note 1, Note 2, 256K, CE1~CE4) Refer to section 4.1 Pin Description

3.3.2 Manual Control Type



4. PIN ASSIGNMENT



4.1 Pin Connection

4.2 Pin Desctiptions

name	no.	Structure				Functional explanation
		Manual control		CPU control		
		I/O	Pull-up / down	I/O	Pull-up / down	
FILOUT	1	Out	–	Out	–	Output pin of the on-chip Band Pass Filter.
TEST	3	In	Pull-down	In	Pull-down	Input pin for test circuit. (Connect to VSS1)
D7 D6 D5 D4 D3 D2 D1 D0	4 6 8 10 13 14 15 16	I/O	Pull-up	I/O	Pull-up	Data I/O pins. Connect to I/O pins of SRAMs. At the CPU control, this pins are high impedance by DMA function.
A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	17 18 19 21 22 23 24 25 26 28 29 30 31 32 33	Out	–	Out	–	Address output pins for SRAMs. At the connect to 64K SRAM, not use A13 and A14 pins. At the CPU control, this pins are high impedance by DMA function.
VSS1 VSS2	20 62	Power Supply	–	Power Supply	–	Power supply pins to be connected to ground. VSS1 is for digital circuit and VSS2 is for analog circuit.
VDD	27 61	Power Supply	–	Power Supply	–	Power supply pins to be connected to positive.
$\overline{CE}$	34	Out	–	Out	–	Chip nable output pins for SRAMs. Use for memory capacity up. At the CPU control, this pins are high impedance by DMA function.

name	no.	Structure				Functional explanation
		Manual control		CPU control		
		I/O	Pull-up / down	I/O	Pull-up / down	
$\overline{CE1}$ $\overline{CE2}$ $\overline{CE3}$ $\overline{CE4}$	35 36 37 38	Out	–	Out	–	Chip enable output pins for SRAMs. At the CPU control, this pins are high impedance by DMA function.
STBY	39	In	None	In	None	Input pin f standby mode.
XIN XOUT	40 41	In Out	–	In Out	–	Input and output pins of the ceramic oscillator.
256K	42	In	None	In	None	Input pin for SRAM capacity select.
R / $\overline{W}$	43	Out	–	Out	–	Read or write strobe output pin for SRAMs. Connect to R / $\overline{W}$ pin of SRAMs. At the CPU control, this pins are high impedance by DMA function.
ALE	44	Out	–	Out	–	Address latch enable pin for memory capacity up. At the CPU control, this pins are high impedance by DMA function.
$\overline{WR}$	45	In	Pull-down (at STBY = L)	In	None	In the CPU control mode, input pin for write strobe (P0 to P3). In the manual control mode, used for bit rate with $\overline{RD}$.
$\overline{RD}$	46	In	Pull-down (at STBY = L)	In	None	In the CPU control mode, input pin for read strobe (P0 to P3). In the manual control mode, used for bit rate with $\overline{WR}$.
PH3 PH2 PH1 PH0	47 48 49 50	In	Pull-down (at STBY = L)	In	Pull-down (at STBY = L)	Input pins for phrase select in the manual control mode.
P3 P2 P1 P0	51 52 53 54	In	Pull-down	I/O	None	In the CPU control mode, these are bidirectional data bus for commands or status between CPU and TC8830AF. In the manual control flowing, 1) P0 start input 2) P1 stop input 3) P2 auto phrase function select 4) P3 recording or playback select

name	no.	Structure				Functional explanation
		Manual control		CPU control		
		I/O	Pull-up / down	I/O	Pull-up / down	
EOS	55	Out	–	Out	–	Output pin for end of speech. Gives high level signal under the recording / playback waiting, and low level signal under the recording / playback.
$\overline{ACL}$	56	In	Pull-up	In	Pull-up	Input pin for reset signal.
CPUM	57	In	None	In	None	Input pin for mode change. Fix to low level at the manual control mode, to high level at the CPU control mode.
Vref	58	I/O	–	I/O	–	Pin for connecting the capacitor to the reference voltage circuit of the on-chip Op-Amp.
MICIN	59	In	–	In	–	Input pin for on-chip MICAMP(First stage). Microphone should be connected to this pin through capacitor.
C1	60	Out	–	Out	–	Output pin for on-chip MICAMP(First stage).
C2	63	In	–	In	–	Input pin for on-chip MICAMP (second stage). C1 should be connected to this pin through capacitor.
MIC OUT	64	Out	–	Out	–	Output pin for on-chip MICAMP (second stage).
ADI	65	In	–	In	–	Input pin of the voice analysis circuit. Connected to MICOUT. Otherwise, signal should be input via a coupling capacitor.
DAO	66	Out	–	Out	–	Output pin of the voice synthesis circuit with voltage follower. Output signal is biased to Vref. No voice appears at recording..
FILIN	67	In	–	In	–	Input pins of the on-chip Band pass Filter.

5 SPECIFICATIONS

5.1 Recording / Reproducing Part

System	ADM system
D / A Converter	10-bit voltage type
Bit rate	32K / 16K / 11K / 8K bps
Number of max. phrases	At the manual control 16 phrases Auto phrase mode at the manual control ..... 63 phrases Label index mode at the CPU control ..... 63 phrases Direct mode at the CPU control ..... No restriction

5.2 Others

Microphone amplifier	Two-stage, Gain = 46dB (TYP.)
Filter	On chip filter for 2nd order low pass + 1st order high pass
RAM for storing voice data	Up to 4 pcs. of 64Kbit, or 4 pcs. of 256Kbit. Example of usable memory (Access time) At the manual control ..... 200nS max Label index mode at the CPU control ..... 200nS max Direct mode at the CPU control ..... 300nS max
Oscillation frequency	512 kHz

5.3 Operations and Functions

When composing a voice Recording / playback system with TC8830AF, control method is classified into the CPU control and the manual control using switches.

5.4 Manual Control

5.4.1 Selection of Phrase

Using 4 input pins of PH0~PH3, The recording / playback of maximum 16 phrases can be performed. Before starting the recording / playback. And using auto phrase function (refer to section 5.4.7), maximum 63 phrases can be performed. Phrase No. should be specified in 4bit code. Phrase number is as follows, and should be selected at sequence from low order phrase at the recording, but can be selected at random at the playback.

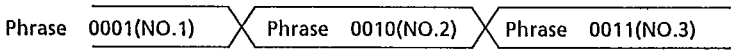
Table 5.1 Example of phrase number

Pin name / Phrase No	(MSB) PH3	PH2	PH1	(LSB) PH0
No.0	0	0	0	0
No.1	0	0	0	1
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
No.15	1	1	1	1

1 = H level
0 = L Level

Recording

Recording is made in order of phrase NO.1、NO.2、NO.3



Playback

Playback is made in order of phrase NO.3、NO.1、NO.2

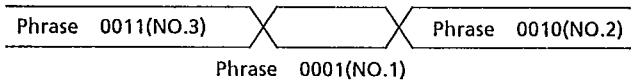


Fig.5.1 Example of phrase selection

5.4.2 Selection of Bit Rate

The TC8830AF can use 4 kinds of bit rates as shown in Table 5.2, 8K, 11K, 16K and 32K bps, which are selected by $\overline{WR}$ and $\overline{RD}$ pins.

The bit rate should be select under the recording waiting state or playback waiting state.

Table 5.2 Bit rate

Pin name / Bit rate	$\overline{WR}$	$\overline{RD}$
8Kbps	0	0
11Kbps	0	1
16Kbps	1	0
32Kbps	1	1

1 = H level
0 = L Level

5.4.3 Recording

The TC8830AF has the 20-bit address counter, and voice data is written into SRAMs from the address designated by it's value. When the recording newly, first, it is necessary to reset the address counter and index area (refer to section 5.6) by $\overline{ACL}$ signal.

Setting the P3 pin to H level results in the recording waiting state. When the P0 pin goes to H level (Start input), the recording starts and the address counter is added successively. When the P1 is set at H level (Stop input) or when the value on the address counter reaches the maximum address (Refer to section 5.5.6) of SRAMs by ADDRESS OVER FLOW DETECTOR (refer to section 5.6) , the recording is stopped. Since this maximum address is changed with SRAMs capacity. Further, the recording is stopped when error address in the SRAM.

However, when the SRAMs capacity is fully used, subsequent recording is not allowed to protect the data stored previously in SRAMs. Therefore, the address counter should be reset by the $\overline{ACL}$ signal before new recording.

When the recording starts, a value of the address counter at the start (Start address) and when the recording ends, that at the stop (Stop address) are automatically written into a part of SRAM, respectively.

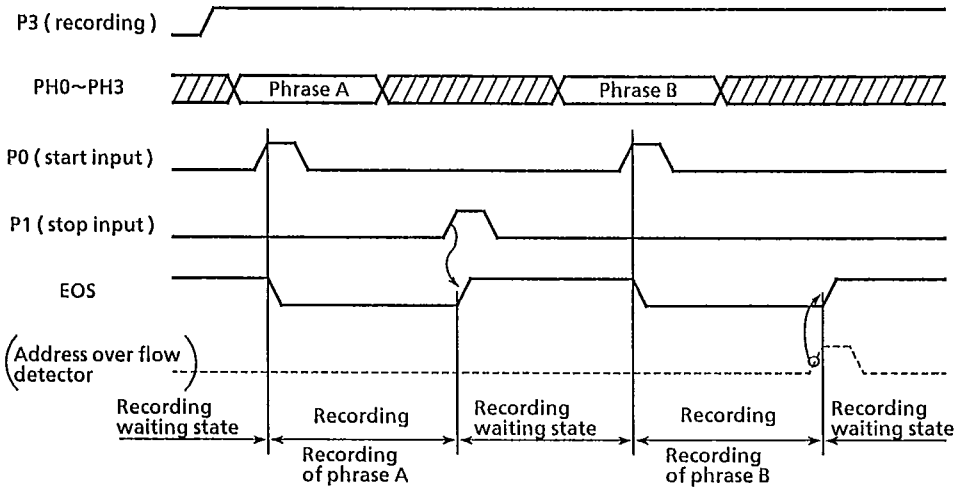
5.4.4 Playback and Pause Function

Setting the P3 pin to L level results in the playback waiting state. When the P0 pin is set at H level, the TC8830AF starts the playback after loading the start address and stop address, which have been written at the recording, into the address counter and stop address register, respectively.

When the P1 pin is set at H level during the playback, the playback is paused. Playback is continued when the P0 pin is set at H level under this condition.

The playback is stopped when the P1 pin is set at H level during the playback pause state or when the value of the address counter agrees with the stop address by ADDRESS COMPARATOR FLIPFLOP (refer to section 5.5.7).

5.4.5 Timing of Recording / Playback



TC8830AF not receive start input under the recording

Fig.5.2 Timing of recording

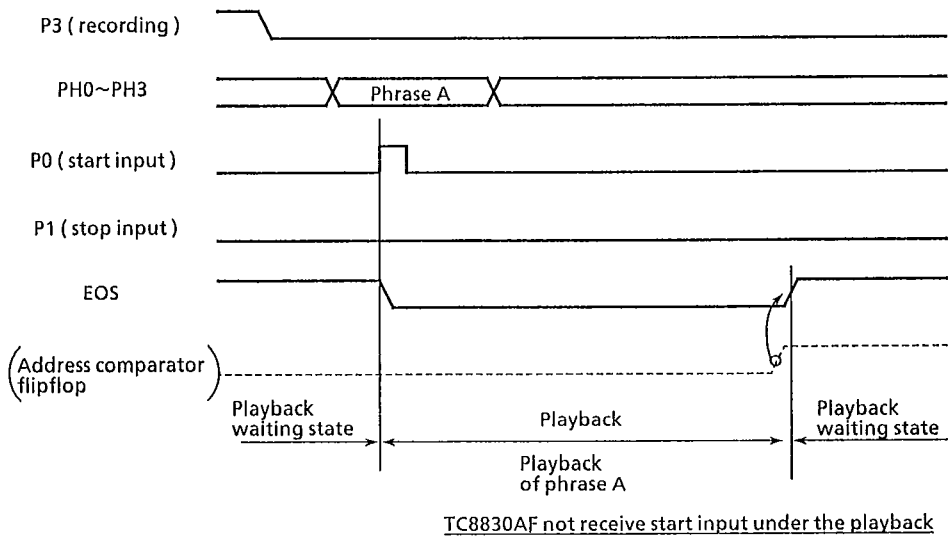


Fig.5.3 Timing of playback

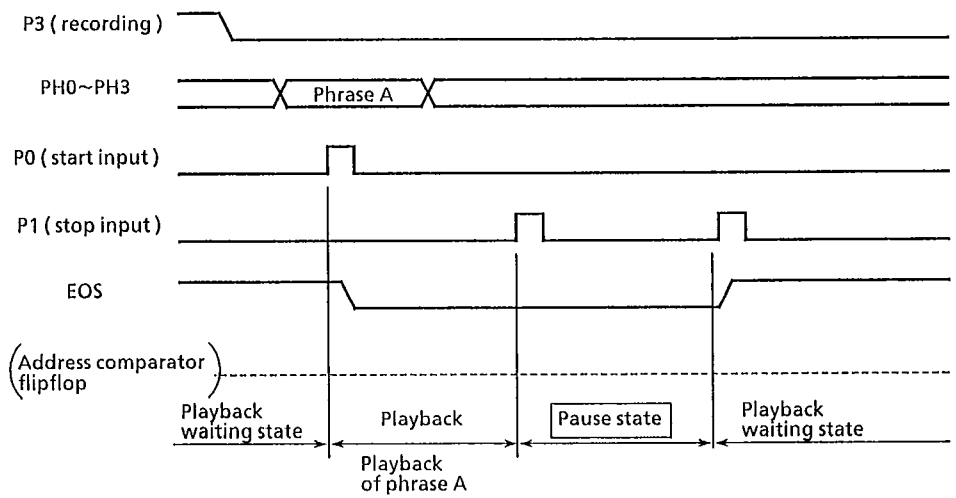


Fig.5.4 Timing of playback stop

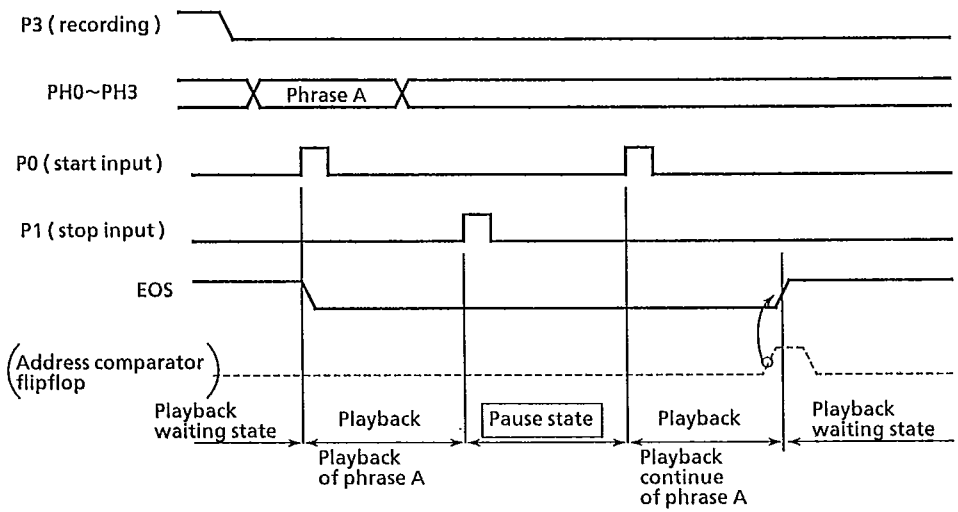


Fig.5.5 Timing of playback release

5.4.6 Restriction of Start Input

When the recording and playback starts, there is the following restriction between P0 pin (start input) and P1 pin (recording).

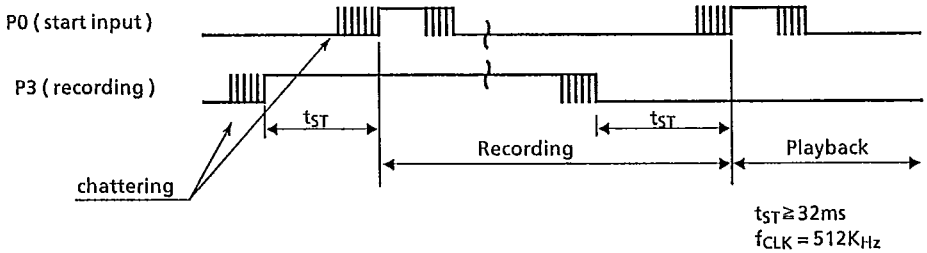


Fig.5.6 Timing of change at recording / playback

5.4.7 Auto Phrase Function

Phrase No. can be increased automatically at the recording and playback.

Initial value of phrase No. setting by PH0~PH3 pins. This function is enabled when the P2 pin is set to H level under this state.

Valid phrase is No. 0~62. if over the No. 62, lost to content of SRAM. And over the phrase No. 16 is not direct playback

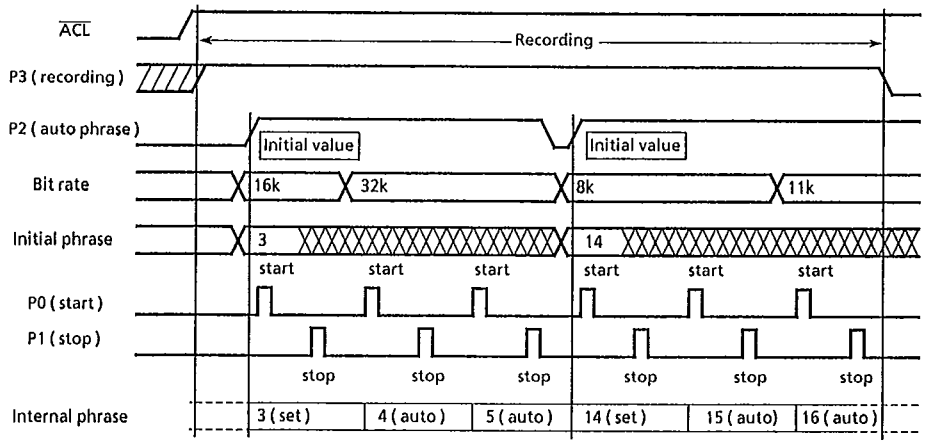


Fig.5.7 Auto phrase recording

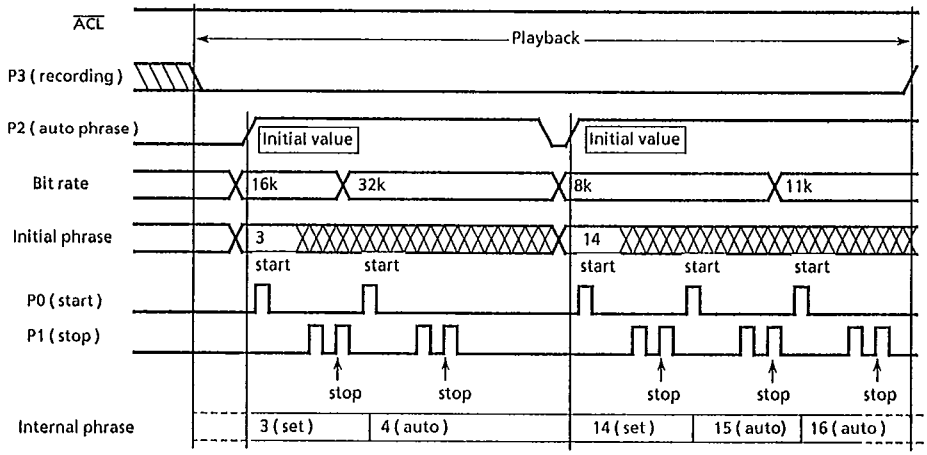


Fig.5.8 Auto phrase playback

5.4.8 Status Change at The Manual Control

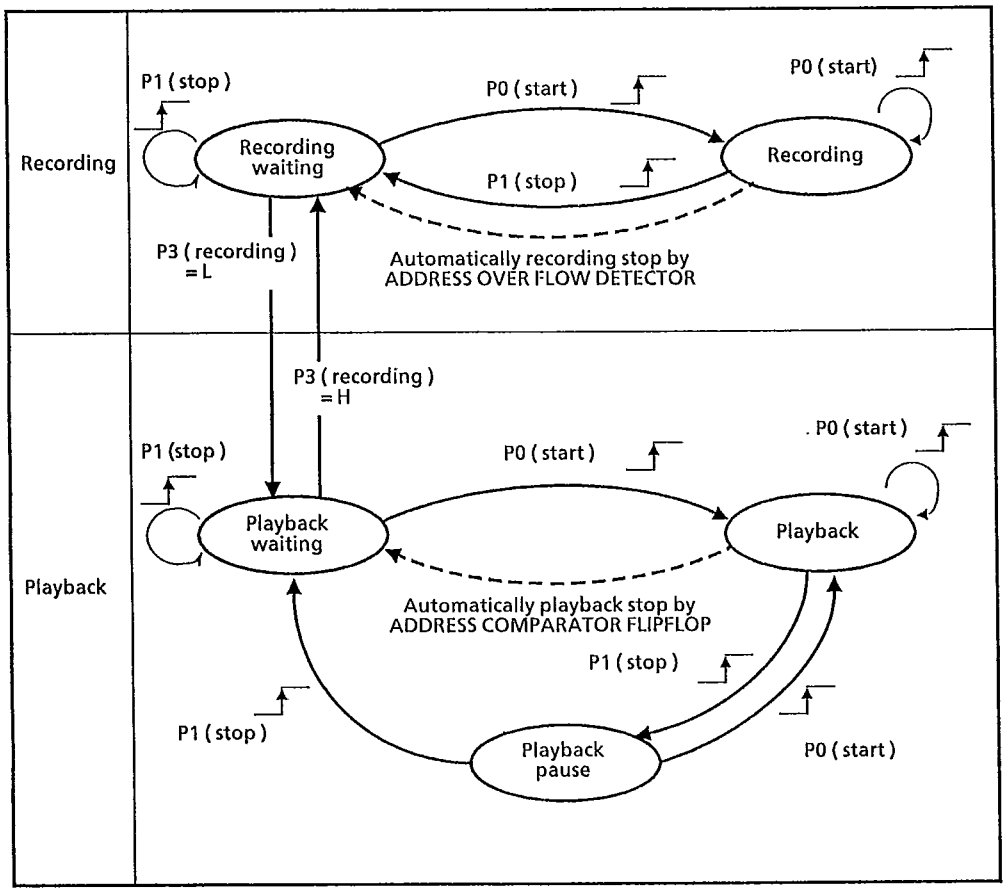
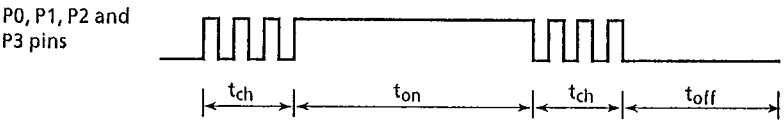


Fig.5.9 Status change at the manual control

5.4.9 Chattering Elimination Circuit

At the manual control, the chattering elimination circuit is actuated to prevent from malfunction due to the switches connected to the P0~P3 pins.



	MIN.
t_{on}	32800 / f_{CLK}
t_{off}	32800 / f_{CLK}

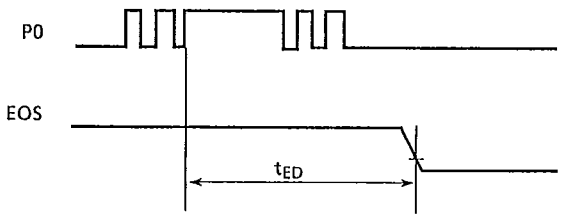
t_{on}, t_{off} is about 64 ms, at f_{CLK} = 512 kHz

Fig.5.10 Chattering elimination circuit

Input signal should be applied stably for more than t_{ON} and t_{OFF}.

Start and stop signals should be applied stably for more than t_{ON} and t_{OFF}.

5.4.10 EOS Delay Time at Manual Control



	MIN.	MAX.
t_{ED}	16400 / f_{CLK}	32800 / f_{CLK}

t_{ED} is about min 32 ms, max 64 ms, at f_{CLK} = 512 kHz

Fig.5.11 EOS delay time at manual control

5.5 CPU Control

At the CPU control, the operation is controlled by 11 kinds of commands and a CPU can read the status of TC8830AF by 4bit status register.

In addition, the TC8830AF has the ADDRESS OVERFLOW DETECTOR (Note 1) and ADDRESS COMPARATOR FLIPFLOP (Note 2) which control the recording and playback operations.

(Note 1) ADDRESS OVERFLOW DETECTOR ..... Refer to section 5.5.5

(Note 2) ADDRESS COMPARATOR FLIPFLOP ..... Refer to section 5.5.6

5.5.1 How to Write Commands

As shown in Fig. 5.12, ①using $\overline{RD}$ pulse, read status from TC8830AF and check BUSY flag ②If not busy state, after setting up command in P0~P3, write a command using $\overline{WR}$ pulse. In case of such 3 nibble commands as LABEL, keep at command processing time (refer to section 5.2.5), ③write the 2'nd and 3'rd nibbles.

After the 1'st and 2'nd nibbles of a 3 nibble command, other commands can not be written.

This also applies to 7 nibble commands like ADLD1 and ADLD2.

How to write DTRD and ADRD commands, refer to section 5.5.2

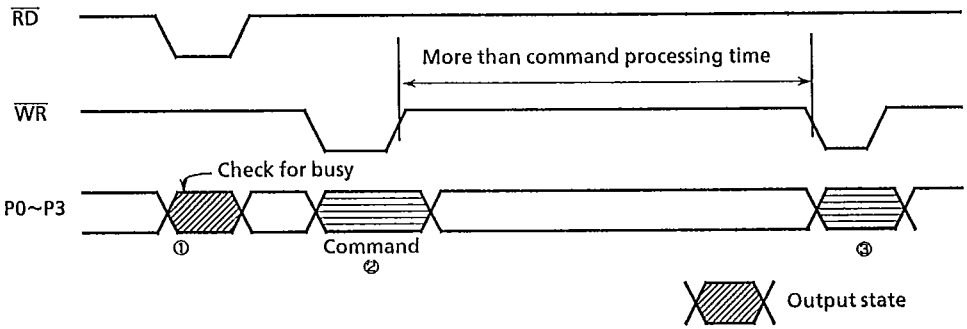


Fig.5.12 How to write command

5.5.2 Commands of TC8830AF

(1) Should not be issued D3 | 0 | 0 | 0 | 0 | D0

(2) NOP (1 nibble) D3 | 0 | 0 | 0 | 1 | D0

No operation. But under the recording waiting state, this command sets into the playback waiting state. In addition, this command is used to reset OVR flag in the status register.

(3) START (1 nibble) D3 | 0 | 0 | 1 | 0 | D0

This command is used to start the recording / playback in the DIRECT MODE from the address shown by the address counter. In addition, this command is used to set $\overline{EOS}$ flag in the status register.

(4) STOP (1 nibble) D3 | 0 | 0 | 1 | 1 | D0

When this command is executed under the recording, the recording is stopped. A value of the address counter is written into the INDEX AREA of SRAM as the stop address. In addition, this command is used to reset $\overline{EOS}$ flag in the status register. When this command is executed two times under the playback, playback stops, to reset $\overline{EOS}$ flag in the status register.

(5) ADLD1 (6 nibbles) D3 | 0 | 1 | 0 | 0 | D0

Sets the successive 5 nibbles data in the address counter. Resets the ADDRESS COMPARATOR FLIPFLOP. In addition, this command sets into the playback waiting state.

(6) ADLD2 (6 nibbles) D3 | 0 | 1 | 0 | 1 | D0

Sets the successive 5 nibbles data in the stop address register. Sets the ADDRESS COMPARATOR FLIPFLOP. Set a value of ADLD2 is more than ADLD1. In addition, this command sets into the playback waiting state.

(7) CNDT (2 nibbles) D3 | 0 | 1 | 1 | 0 | D0

Specifies bit rate and enable / disable of ADDRESS OVER FLOW DETECTOR with the successive 1 nibble data. In addition, this command sets into the playback waiting state.

(8) LABEL (3 nibbles) D3 | 0 | 1 | 1 | 1 | D0

Specifies Phrase No. by the successive 2 nibbles data and starts the recording / playback. When this command is issued under the recording waiting state, the contents of the address counter is written into the index area of SRAM and recording starts. In the playback waiting state, starts the playback after reading start address and stop address from index area of SRAM.

(9) ADRD (1 nibble) D3 | 1 | 0 | 0 | 0 | D0

Reads the contents of the address counter. The contents are come out by 4 bits at a time from the low order address side against 5 successive read accesses. During this period, the contents of the status register can not be read. Next command should not be issued without performing 5 read accesses. In addition, this command sets into the playback waiting state.

(10) REC (1 nibble) D3 | 1 | 0 | 0 | 1 | D0

Changes the playback waiting state to the recording waiting state.

(11) DTRD (1 nibble) D3 | 1 | 0 | 1 | 0 | D0

Reads out data of SRAMs in 8 bits data from the address shown by the address counter for the successive 2 read access. During this period, the contents of the status register can not be read, the address counter is not increased. In addition, this command sets into the playback waiting state.

(12) DTWR (2 nibbles) D3 | 1 | 0 | 1 | 1 | D0

Writes 8 bits of the successive 2 nibble data into SRAMs from the address shown by the address counter, the address counter is not increased. In addition, this command sets into the playback waiting state.

(13) Should not be issued

D3 | 1 | 1 | 0 | 0 | D0

(14) Should not be issued

D3 | 1 | 1 | 0 | 1 | D0

(15) Should not be issued

D3 | 1 | 1 | 1 | 0 | D0

(16) Should not be issued

D3 | 1 | 1 | 1 | 1 | D0

Note Under the recording / playback, any command other than STOP should not be issued.

Table 5.3 Command list

	1'st nibble P3 P2 P1 P0	2'nd nibble P3 P2 P1 P0	3'rd nibble P3−P0	4th nibble P3−P0	5th nibble P3−P0	6th nibble P3−P0
NOP	0 0 0 1	—	—	—	—	—
START	0 0 1 0	—	—	—	—	—
STOP	0 0 1 1	—	—	—	—	—
ADLD1	0 1 0 0	A3 A2 A1 A0	A7−A4	A11−A8	A15−A12	A19−A16
ADLD2	0 1 0 1	S3 S2 S1 S0	S7−S4	S11−S8	S15−S12	S19−S16
CNDT	0 1 1 0	0 OV BR1 BR0				
LABEL	0 1 1 1	LB3 LB2 LB1 LB0	* * LB5 LB4	LB = Phrase no.		
ADRD	1 0 0 0	1'st read A3 A2 A1 A0	2'nd read A7−A4	3'rd read A11−A8	4th read A15−A12	5th read A19−A16
REC	1 0 0 1	—	—	—	—	—
DTRD	1 0 1 0	1'st read D3 D2 D1 D0	2'nd read D7−D4	—	—	—
DTWR	1 0 1 1	D3 D2 D1 D0	D7−D4	—	—	—

Auto recording stop	OV
Disable	0
Enable	1

Bit rate	BR1	BR0
8K bps	0	0
11K bps	0	1
16K bps	1	0
32K bps	1	1

* = Don't care

Note A waiting time of 137μs is required between issuing the ADRD / DTRD commands and reading the first nibble data. (f_{CLK} = 512kHz)

5.5.3 Status Register

The status register consists of 4 bits. When the $\overline{RD}$ pin is set to L level at the CPU control, data of the status register is came out to P0~P3 pins and the internal operating status of the TC8830AF can be checked. Each flag of the status register is explained in following (Table 5.4).

(1) OVR flag

It is indicated that the recording ends as the address counter exceeded maximum address of SRAMs under the recording. This status is reset by NOP commands.

(2) BUSY flag

When this flag is set, it indicates that the TC8830AF is in reset state or processing a command internally. Don't give any command from microprocessor. If the command is given, the internal status may possibly becomes uncertainty. When the ADLD1, ADLD2 and LABEL command is issued, until input of required data ends, this flag is not released.

(3) $\overline{EOS}$ flag

This flag becomes set under the recording / playback waiting state, and reset during recording or playback. The value is the same as a value appeared at the EOS pin.

Table 5.4 Status register

Pins name	P3	P2	P1	P0
Status register	---	OVR	BUSY	$\overline{EOS}$

5.5.4 BUSY Flag

Conditions for setting BUSY flag set are broadly classified into the following conditions.

(1) Reset process

When the $\overline{ACL}$ pin becomes L level, BUSY flag becomes set. When the $\overline{ACL}$ pin returns to H level again, the internal state of TC8830AF is initialized and after all are completed, BUSY flag becomes reset.

(2) Command process

When it is detected that $\overline{WR}$ pins have become H level from L level at the CPU control, BUSY flag becomes set. When the process of command is completed, BUSY flag returns to reset again. The command process is actually started after return of $\overline{WR}$ pin to H level has been detected.

5.5.5 Command Processing Time

Times required for processing commands are shown below. When commands is issued successively, issue them at intervals of more than these command processing times.

Table 5.5 Status register

Command ($\overline{ACL}$)	processing time
Reset process ($\overline{ACL}$)*	24600 / f_{CLK} (sec)
NOP, START, STOP, ADLD1, ADLD2, CNDT, REC, DTWR commands write	35 / f_{CLK} (sec)
LABEL, DTRD, ADRD commands write	70 / f_{CLK} (sec)
Data write of ADLD1, ADLD2, CNDT, DTWR command	35 / f_{CLK} (sec)
Data write of LABEL command	70 / f_{CLK} (sec)
Read access after the DTRD, ADRD command	70 / f_{CLK} (sec)

*Note; No count Oscillation rise time (Oscillation rise time is several mS in case of CSB512)

f_{CLK} = Oscillation frequency (Hz)

5.5.6 Address Overflow Detector

When the address counter exceeds maximum address that is detected by this detector during the recording with LABEL command at the CPU control. Enable or disable of detector is selected by CNDT command.

This detector is enable only at the manual control.

When the address overflow is detected, the recording is stopped, a value of the maximum address is written into the index area of SRAM as the stop address, and then the address counter is preset at address 100 (HEX). In addition, the OVR and $\overline{EOS}$ flag in the status register is set.

5.5.7 Address Comparator Flipflop

When this flipflop has been set, the recording / playback is stopped if the contents of the address counter agree with those of the stop address register. When it has been reset, the recording / playback is not stopped until the STOP command is given. (Exception : Address overflow in the preceding item).

5.5.8 Change of Internal Blocks

Table 5.6 Change of internal blocks

Command ($\overline{ACL}$)	Register etc.				Internal flag		EOS Output (Note)	Status flag	
	Index register	Address counter	Stop address register	Bit rate	Address overflow detector	Rec mode		OVER	$\overline{EOS}$ (Note)
$\overline{ACL}$	R	R→S (100_H)	R	R	ENABLE	R	H level	R	R
NOP						R		R	
START		START					L level		S
STOP		STOP					H level		R
ADLD1		S				R			
ADLD2			S			R			
CNDT				S	S	R			
LABEL	S	S	S						
ADRD						R			
REC						S			
DTRD						R			
DTWR						R			

S : SET

R : RESET

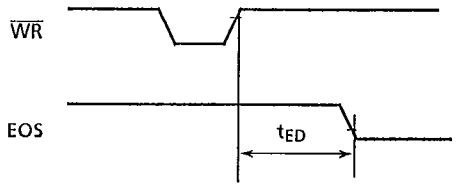
START : Address counter Operate

STOP : Address counter stop

Brank : No change

(Note) $\overline{EOS}$ flag means that set is '1' and reset is '0'

5.5.9 EOS Delay Time at CPU Control



t_{ED}	MIN	MAX
START	32 / f_{CLK}	48 / f_{CLK}
LABEL (recording)	32 / f_{CLK}	48 / f_{CLK}
LABEL (playback)	48 / f_{CLK}	96 / f_{CLK}

f_{CLK} = Oscillation frequency

Fig.5.13 EOS delay time at CPU control

5.5.10 Modes in CPU Control

There are two modes about both recording and playback at the CPU control.

(1) Direct mode — Designate start / stop address, and bit rate by each command.

(2) Label index mode — Designate phrase by LABEL command, start / stop address are written into the some part (Index area) of SRAM. Refer to section 5.3 LABEL INDEX MODE.

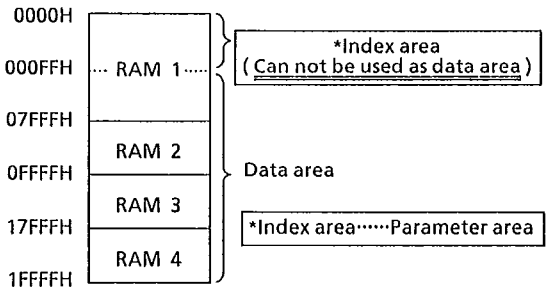


Fig.5.14 Memory map (In case of 256K SRAM)

5.5.11 Status Change at The CPU Control

At the CPU control, the TC8830AF is controlled by 11 kinds of command. The relations between the recording and playback state and commands which are concerned with the recording and playback operations are as follows.

Table 5.7 Status change table at the CPU control

State \ Command	START command	LABEL command	STOP command
Recording waiting	Starts recording	Starts recording	Kept in the recording waiting state
Recording	Don't give the START command	Don't give the LABEL command	Stop recording and returns to the recording waiting state
Playback waiting	Starts playback	Starts playback	Kept in the playback waiting state
Playback	Don't give the START command	Don't give the LABEL command	Placed in the playback waiting state (executed two times)

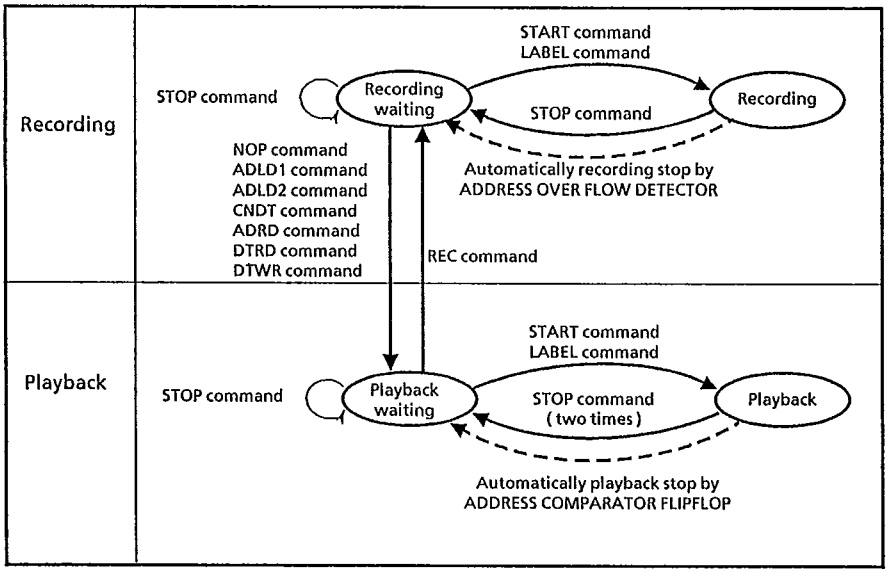


Fig.5.15 Status change at the CPU control

5.5.12 Example for The Flowchart of Recording / Playback at LABEL INDEX MODE

(1) Recording

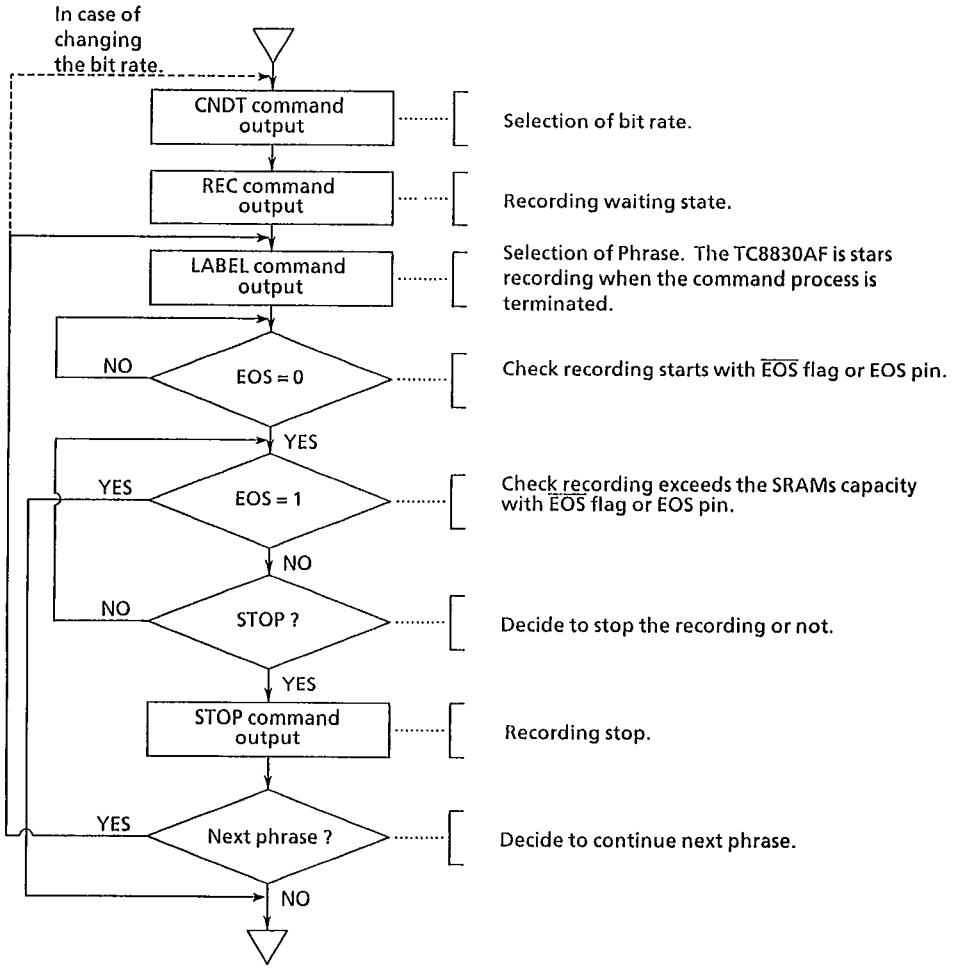


Fig.5.16 Recording procedure at the LABEL INDEX MODE

(2) Playback

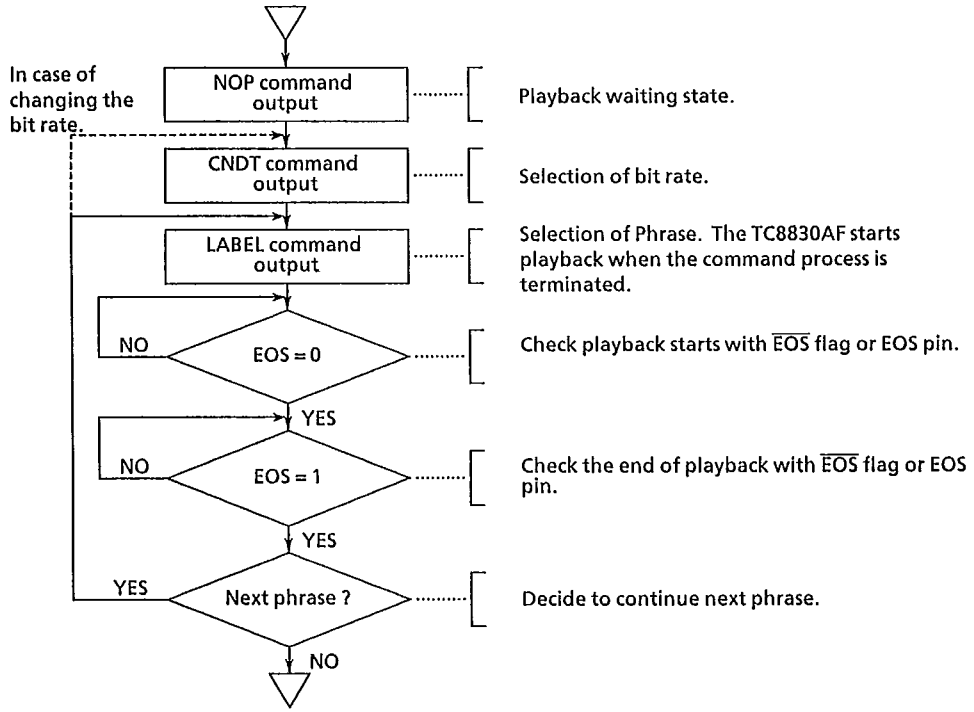


Fig.5.17 Reproducing procedure at the LABEL INDEX MODE

5.5.13 Example for The Flowchart of Recording / Playback at DIRECT MODE

(1) Recording

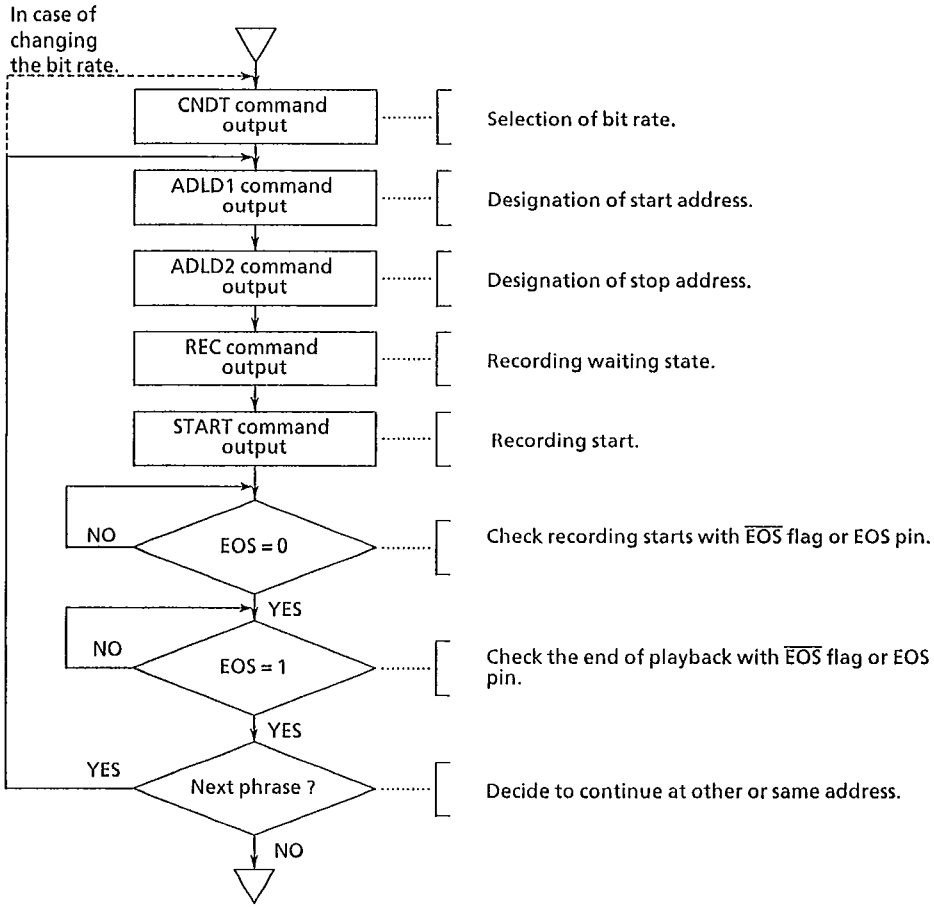


Fig.5.18 Recording procedure at the DIRECT MODE

(2) Reproducing

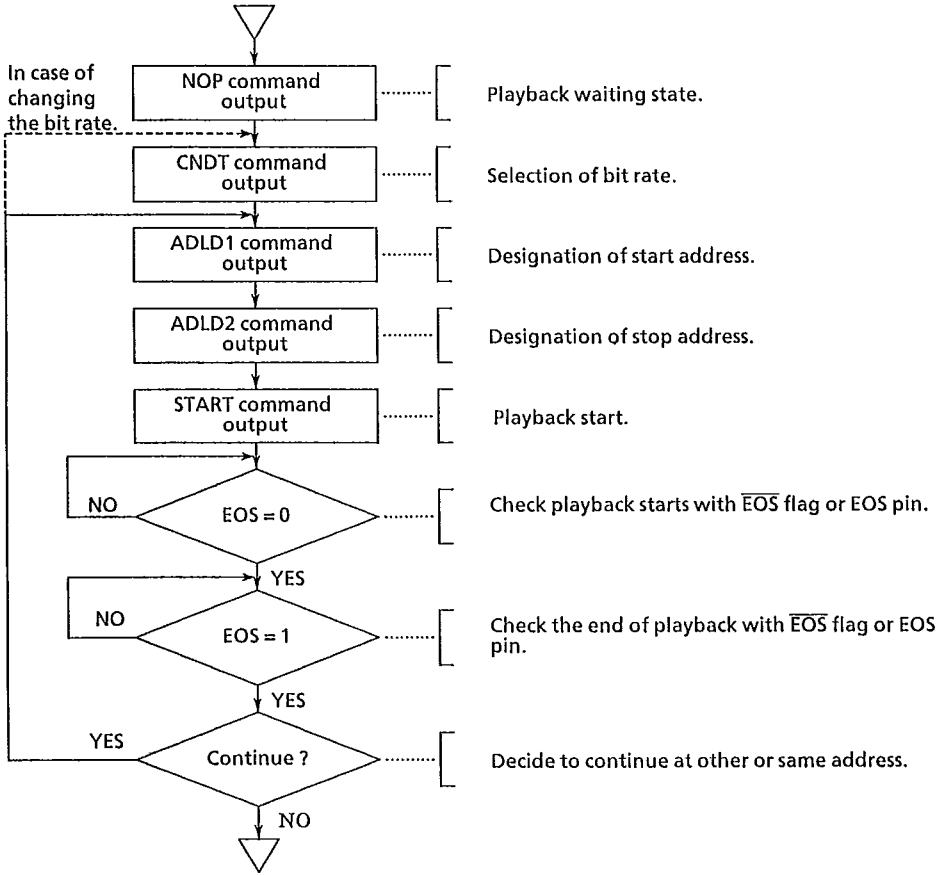


Fig.5.19 Reproducing procedure at the DIRECT MODE

5.5.14 Write / Read Data of SRAMs

(1) Data write

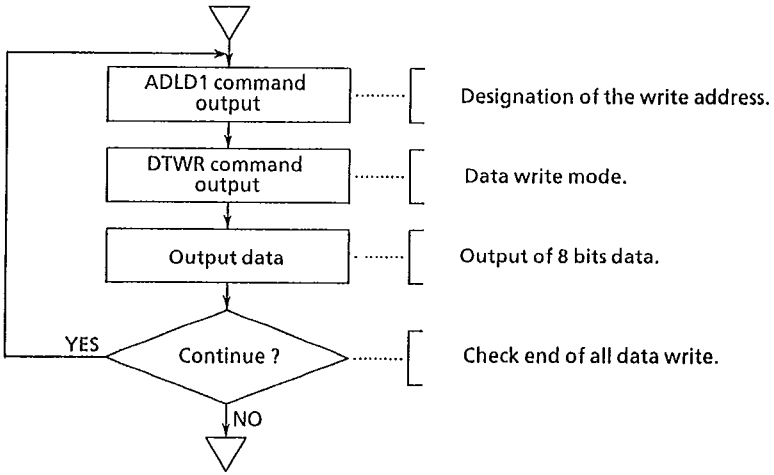


Fig.5.20 Data write procedure

(2) Data read

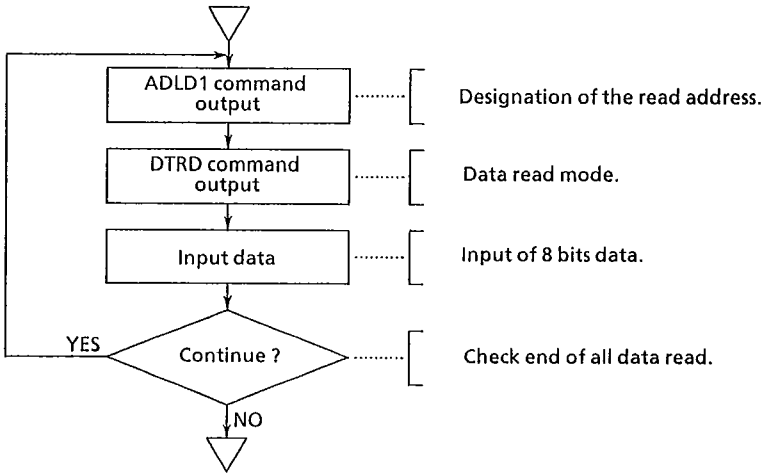


Fig.5.21 Data read procedure

5.5.15 Read Address

ADRD command is used to read a content of address counter at stop of recording and playback

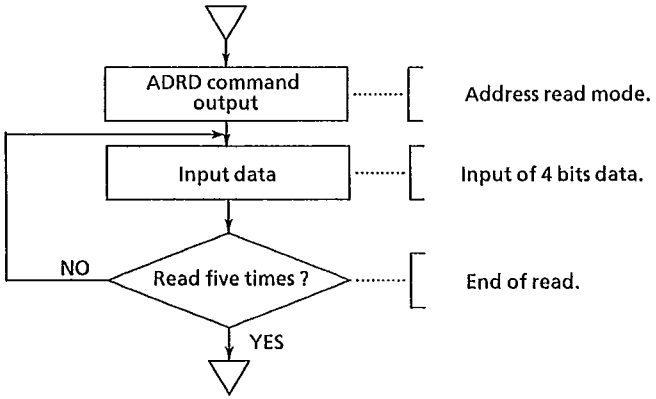


Fig.5.22 Address read procedure

5.5.16 How to DTRD / ADRD Commands

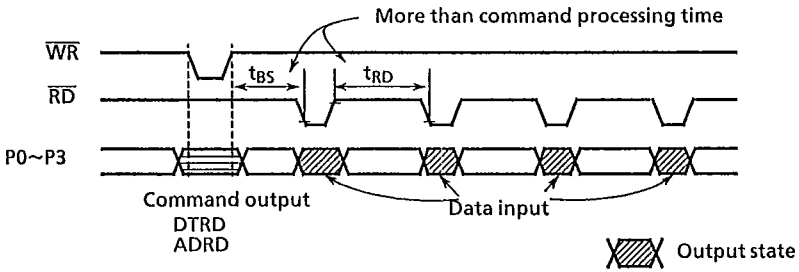


Fig.5.23 How to DTRD / ADRD command

5.6 Label Index Mode

The recording / playback methods for manual control and the LABEL INDEX MODE at the CPU control are described here.

At the manual control (LABEL command under CPU control), the address is indirectly specified using phrase number and index area in which TC8830AF writes the start addresses and stop address of each phrase. The memory maps of SRAMs at the LABEL INDEX MODE are as follow.

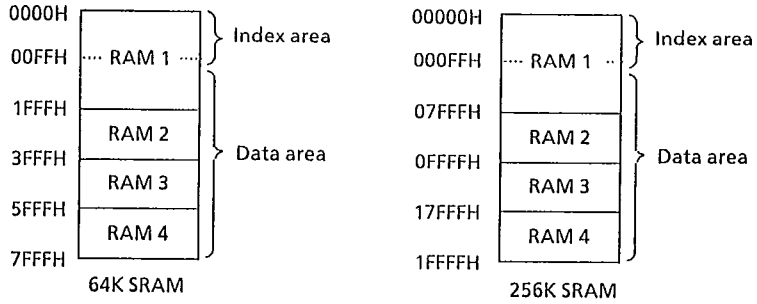


Fig.5.24 Memory map in the LABEL INDEX MODE

Maximum address that can be changed varies depending upon type and quantity of connected SRAMs. In any case, address 0 (HEX) ~ FF (HEX) are used as the index area, and the succeeding address 100 (HEX) and up become the voice data area.

Start address and stop address are recorded in the index area by the TC8830AF at the recording. And data read out from this area are loaded on the address counter at the playback.

5.6.1 Recording of Phrase

In performing the recording newly, Reset the TC8830AF by the $\overline{ACL}$ signal then address counter is preset to 100 (HEX) and 0 clear to index area.

A bit rate and a phrase No. are specified and start signal is issued, then the recording starts. The contents of the address counter (Start address) is written into the index area of SRAM before recording. During the recording, the value of the address counter is increased successively.

When the stop signal is issued during the recording, the recording ends and the contents of the address counter (Stop address) is written into the index area. Thereafter the value of the address counter are added with one to prepare for next recording.

To perform the recording for other phrase successively, phrase No. is newly designated and the start signal is issued (Fig.5.25). New phrase No. should be selected more than old phrase.

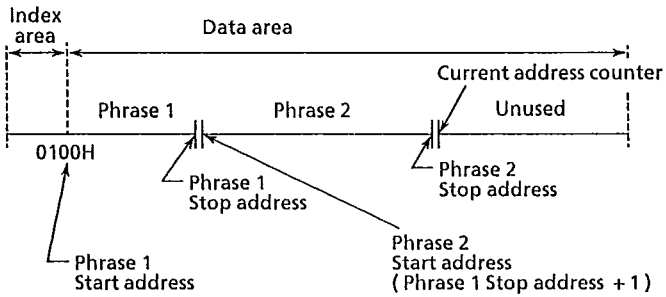


Fig.5.25 In case of recording two phrases

5.6.2 Playback of Phrase

When any recorded phrase No. is selected and start input is given, voice corresponding to that phrase No. is reproduced. Phrase No. can be designated irrespective of sequence of the recording. Giving the two stop input during playback, this phrase stop.

If the playback is started by designating phrase No. that was not used for the recording, not sound at this phrase.

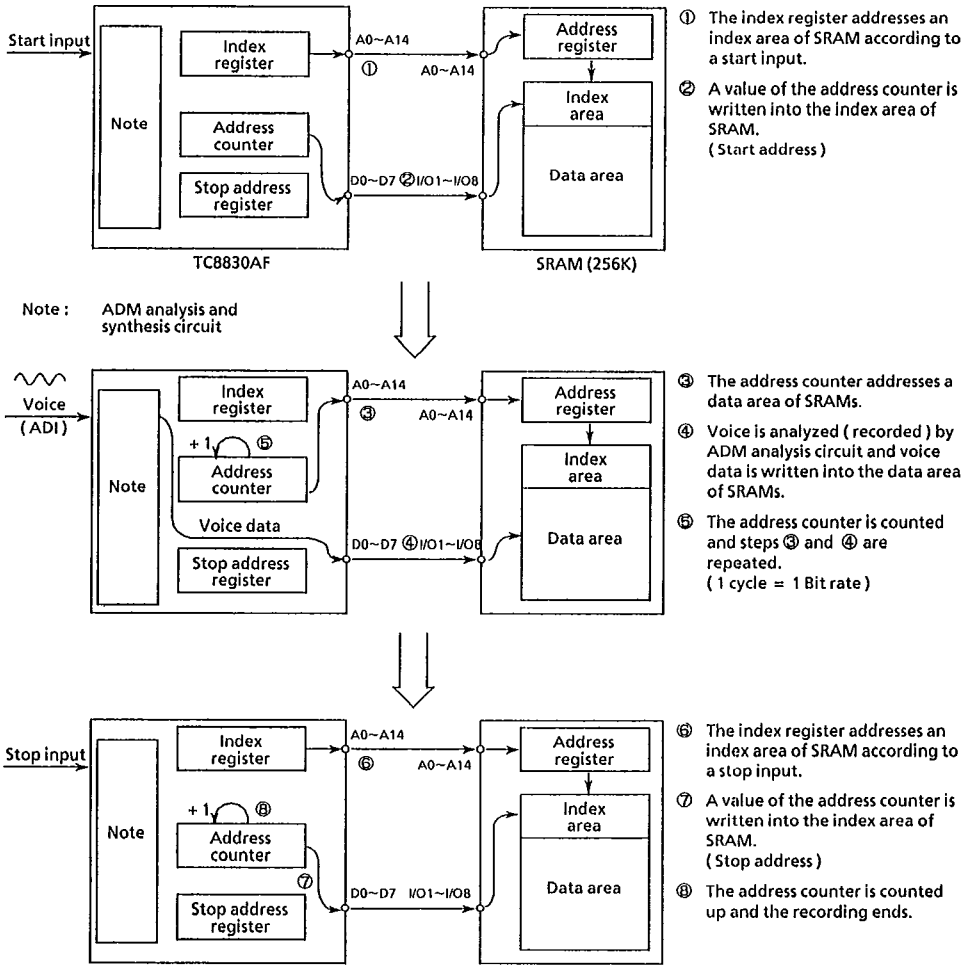
The playback is started after the start address and stop address are set in the TC8830AF from the index area of SRAM. When the playback ends, the value of the address counter are added with (+ 1)

5.6.3 Addition of Phrase

First, reproduce the last phrase at the recording completely so that the address counter can indicate the address next to the stop address of the last phrase. Change the playback waiting state to the recording waiting state. Don't reset the TC8830AF at this state. When the recording is made by designating any more than end of recorded phrase No. to be added.

5.6.4 Label Index Mode Operations

The operations of the TC8830AF and SRAMs in LABEL INDEX MODE are described in the following.



① The index register addresses an index area of SRAM according to a start input.

② A value of the address counter is written into the index area of SRAM.
(Start address)

③ The address counter addresses a data area of SRAMs.

④ Voice is analyzed (recorded) by ADM analysis circuit and voice data is written into the data area of SRAMs.

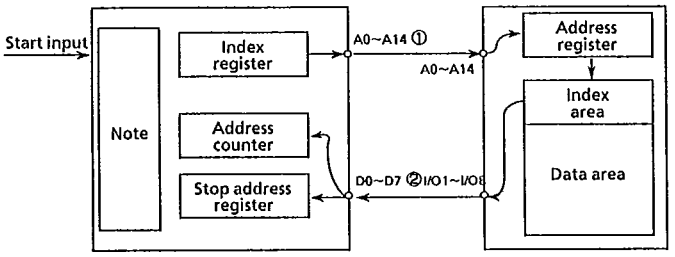
⑤ The address counter is counted and steps ③ and ④ are repeated.
(1 cycle = 1 Bit rate)

⑥ The index register addresses an index area of SRAM according to a stop input.

⑦ A value of the address counter is written into the index area of SRAM.
(Stop address)

⑧ The address counter is counted up and the recording ends.

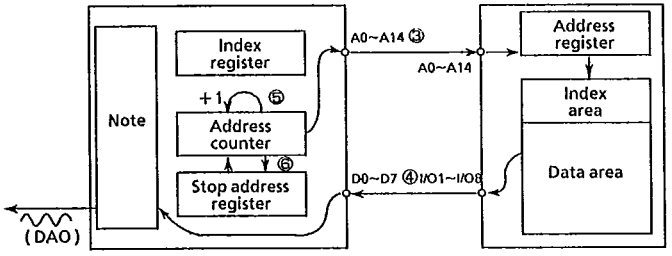
Fig.5.26 Recording



Note : ADM analysis and synthesis circuit

① The index register addresses an index area of SRAM according to a start input.

② Start address, stop address and bit rate are loaded to TC8830AF from the index area.



③ The address counter addresses a data area of SRAMs.

④ Voice data is fed into ADM analysis and synthesis circuit to produce voice.

⑤ The address counter of TC8830AF is counted up.

⑥ The address counter and the stop address register of the TC8830AF are compared and when they agree with each other, the playback stops at next address. If not, steps ③ and ⑤ are repeated.

Fig.5.27 Playback

5.6.5 The Index Area

The index area is used for the recording / playback at the manual control and LABEL INDEX MODE at the CPU control. This area consists of 2K bits from address 0 (HEX) to FF (HEX), securing for 63 phrase (32 bits per phrase).

At the recording, start address and stop address of each phrase are written into index area. And at the playback, the contents of this area are read out and set in the address counter, etc. The contents of the index area for each phrase are shown in the table 5.8. A0~A19 denote the start address and A19 represent the most significant bits of them respectively. Further, stop address equal start address of next phrase.

To read out the contents of the index area, obtain the top address of the index area corresponding to each phrase from phrase No. , and after setting it in the address counter by the ADLD1 command, read it in unit of 8 bits by the DTRD command. On the contrary, to write data into the index area, after setting the top address of the index area in the same manner as above, write data by the DTWR command.

The index area is cleared to by the $\overline{ACL}$ signal.

Don't select the start and stop address in index area by ADLD1 or ADLD2 commands at the DIRECT MODE.

Table 5.8 Memory map of index area

	RAM Address	RAM Data							
	(HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Start address of phrase No.0	00_H	A7	A6	A5	A4	A3	A2	A1	A0
	01_H	A15	A14	A13	A12	A11	A10	A9	A8
	02_H	-	-	-	-	A19	A18	A17	A16
	03_H	-	-	-	-	-	-	-	-
Start address of phrase No.1	04_H	A7	A6	A5	A4	A3	A2	A1	A0
	05_H	A15	A14	A13	A12	A11	A10	A9	A8
	06_H	-	-	-	-	A19	A18	A17	A16
	07_H	-	-	-	-	-	-	-	-
Start address of phrase No.2	08_H	A7	A6	A5	A4	A3	A2	A1	A0
	09_H	A15	A14	A13	A12	A11	A10	A9	A8
	$0A_H$	-	-	-	-	A19	A18	A17	A16
	$0B_H$	-	-	-	-	-	-	-	-
Start address of phrase No.61	$F4_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$F5_H$	A15	A14	A13	A12	A11	A10	A9	A8
	$F6_H$	-	-	-	-	A19	A18	A17	A16
	$F7_H$	-	-	-	-	-	-	-	-
Start address of phrase No.62	$F8_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$F9_H$	A15	A14	A13	A12	A11	A10	A9	A8
	FA_H	-	-	-	-	A19	A18	A17	A16
	FB_H	-	-	-	-	-	-	-	-
Stop address of phrase No.62	FC_H	A7	A6	A5	A4	A3	A2	A1	A0
	FD_H	A15	A14	A13	A12	A11	A10	A9	A8
	FE_H	-	-	-	-	A19	A18	A17	A16
	FF_H	-	-	-	-	-	-	-	-

5.7 DMA Function

The TC8830AF has the DMA function at the CPU control. When both the $\overline{RD}$ and $\overline{WR}$ pins are set to L level at the CPU control, the A0~A14, D0~D7, $\overline{CE}$, $\overline{CE1}$~$\overline{CE4}$ and R/$\overline{W}$ pins are placed in the high impedance state.

This function is possible to release the connected SRAMs from the TC8830AF.

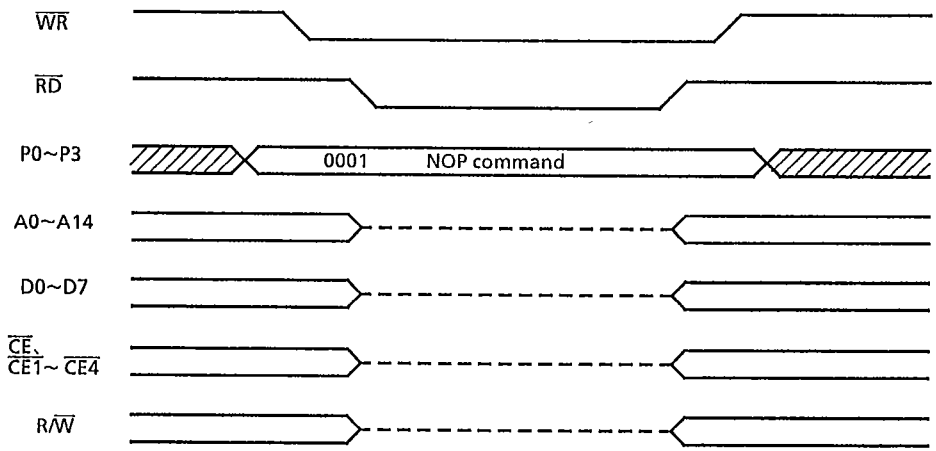


Fig.5.28 Timing of DMA function

This function selecting at the recording waiting state or playback waiting state.

Placing DMA function, set the $\overline{RD}$ pin at H level after setting the $\overline{WR}$ pin at L level. If the $\overline{RD}$ pin is first set at L level, the P0~P3 pins are placed in the output state until the $\overline{WR}$ pin becomes L level.

Releasing DMA function, set the $\overline{WR}$ pin at H level after setting the $\overline{RD}$ pin at H level, write the NOP command into the TC8830AF.

5.8 Standby Function

When the STBY pin set at H level under the recording waiting state or playback waiting state, the TC8830AF is placed at standby state. The status is shown below.

(1) Oscillator stop and low power state.

(2) Sets the $\overline{CE}$ and $\overline{CE1}$~$\overline{CE4}$ pins at H level, and external SRAMs places to the minimum standby current mode. At this state, the contents of SRAMs can be remained.

(3) A0, A2~A14, D0~D7, ALE and R/$\overline{W}$ pins at L level.

(4) A1 and EOS pins at H level.

(5) Internal pull down resisters are unconnected (P0~P3, $\overline{RD}$, $\overline{WR}$ PH0~PH3).

(6) D / A converter stops and low power state.

(7) The microphone amplifier and band pass filter stops and low power state.

5.9 Reset Operation

5.9.1 The Status Under Reset Operation

When the $\overline{ACL}$ pin is set at L level, TC8830AF stops all operation such as recording / playback.

Further, BUSY flag in status register becomes set during this period.

5.9.2 The Status After rRset Operation

When the $\overline{ACL}$ pin becomes from L to H level, the internal state of TC8830AF is initialized as shown below.

(1) Set the playback waiting state.

(2) Address counter and stop address register are preset to 100 (HEX).

(3) 0 clear to index area of SRAMs, ADDRESS OVERFLOW DETECTOR is enable state and ADDRESS COMPARATOR FLIPFLOP is reset.

(4) At the CPU control, bit rate becomes 8kbps.

(5) OVR flag in status register are reset.

After terminating the above completely, BUSY flag is reset.

5.9.3 Reset Processing After Power On

When the after power on, the following items become unstable.

(1) Recording and playback state.

(2) Address counter.

(3) ADM analysis / synthesis circuit.

(4) Other processing circuits such as start and stop processing.

Therefore, to initialize this unstable condition and assure proper operations, apply $\overline{ACL}$ signal.

$\overline{ACL}$ signal to be given after power ON and it's pulse width are shown in Fig.5.29.

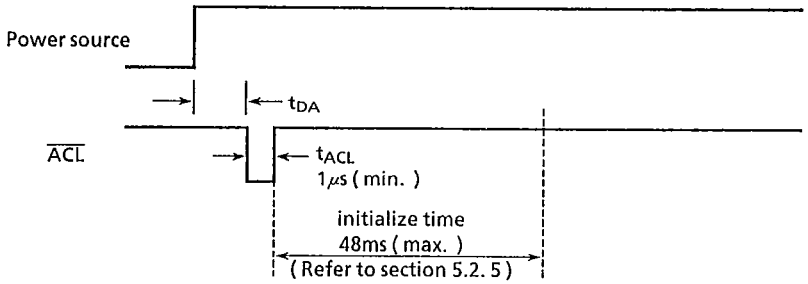


Fig.5.29 $\overline{ACL}$ pulse width

However, if width of t_{DA} after power ON is long, the unstable status lasts and causes malfunction (start recording / playback, etc.) in Fig.5.29.

So, a power on reset circuit is constructed by attaching a 1μF capacitor to the $\overline{ACL}$ pin, makes the system initialization is possible immediately after power ON as illustrated in Fig.5.30.

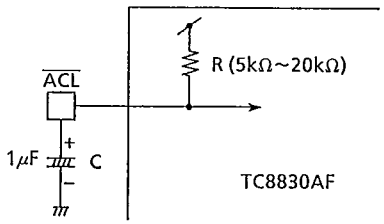


Fig.5.30 Power on reset circuit

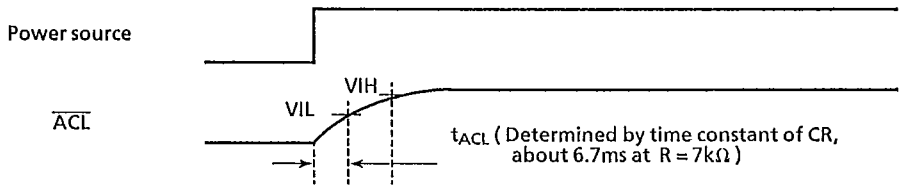


Fig. 5.31 $\overline{ACL}$ input at power on reset

However, the power on reset is effective only for a rapid step power rise and when power rise is gentle or power on / off is repeated in short cycle, no system initialization is performed.

Further, if the $\overline{ACL}$ pin can be controlled by a CPU regardless of power on / off at TC8830AF side, the system initialization can be made as shown in Fig. 5.32

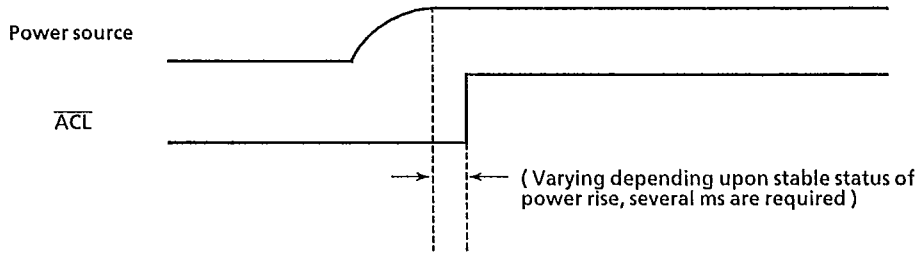


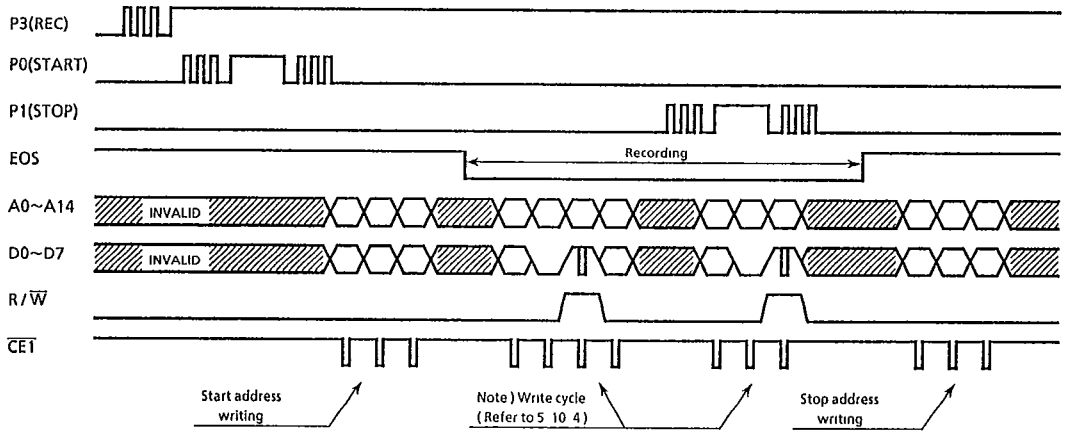
Fig. 5.32 System initialization by CPU control

5.10 Access Timing at SRAM

SRAM access timing is different at manual control and CPU control. Each access timing is shown below and AC characteristics refer to section 6.4.

5.10.1 Recording / Playback at Manual Control

(1) Recording (Force the stop input)



(2) Recording (Address overflow)

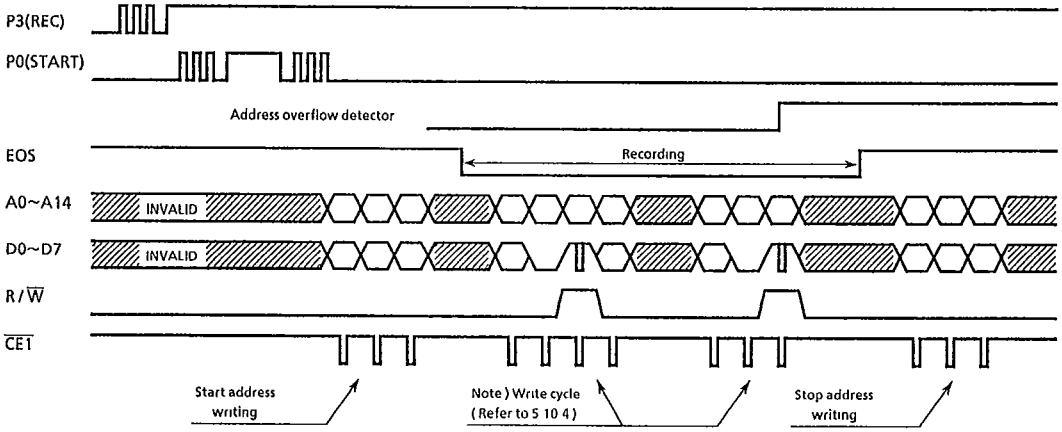
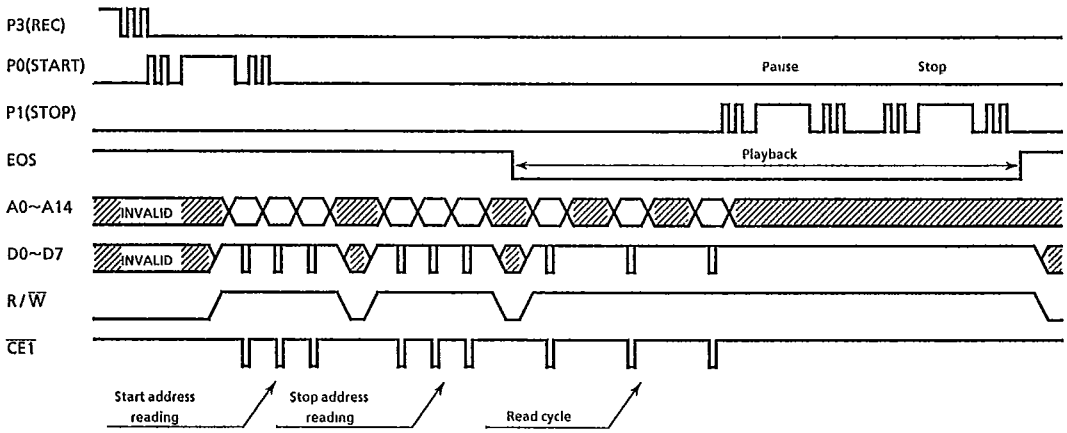


Fig. 5.33 Recording at manual control

(3) Playback (Force the stop input)



(4) Playback (Auto stop)

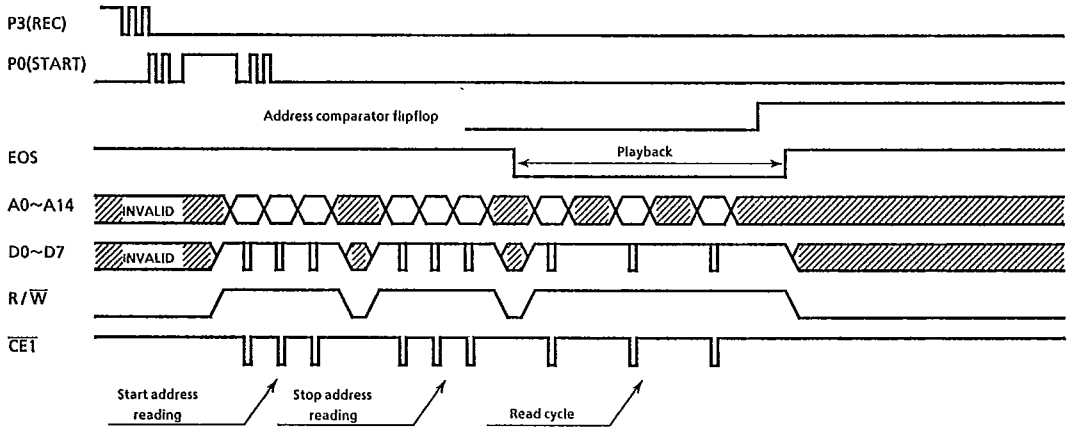
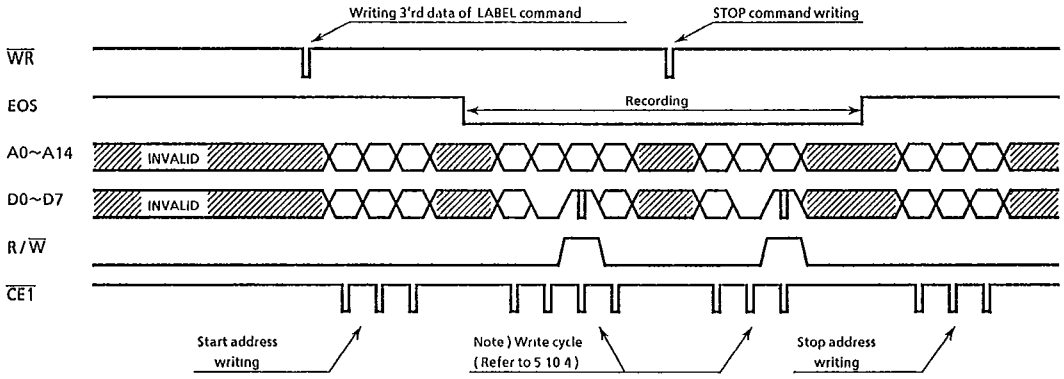


Fig. 5.34 Playback at manual control

5.10.2 Recording / Playback at CPU Control with LABEL INDEX MODE

(1) Recording (Force the stop command)



(2) Recording (Address over flow)

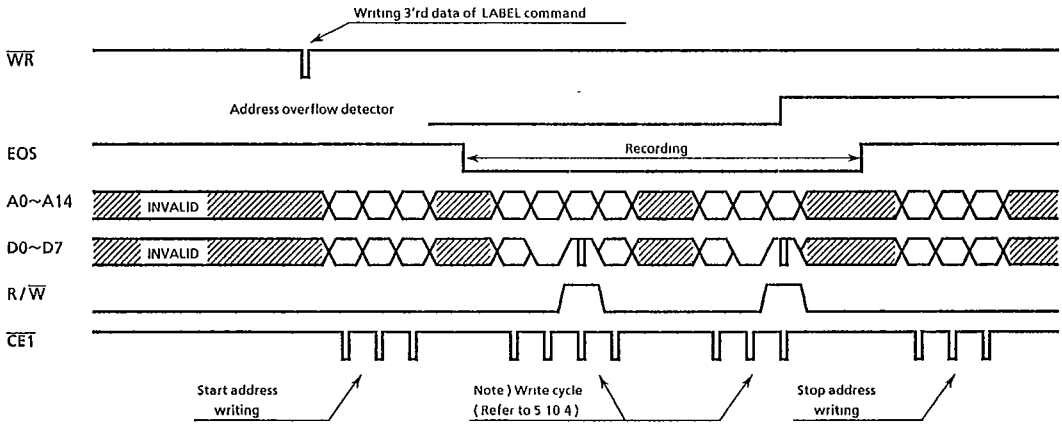
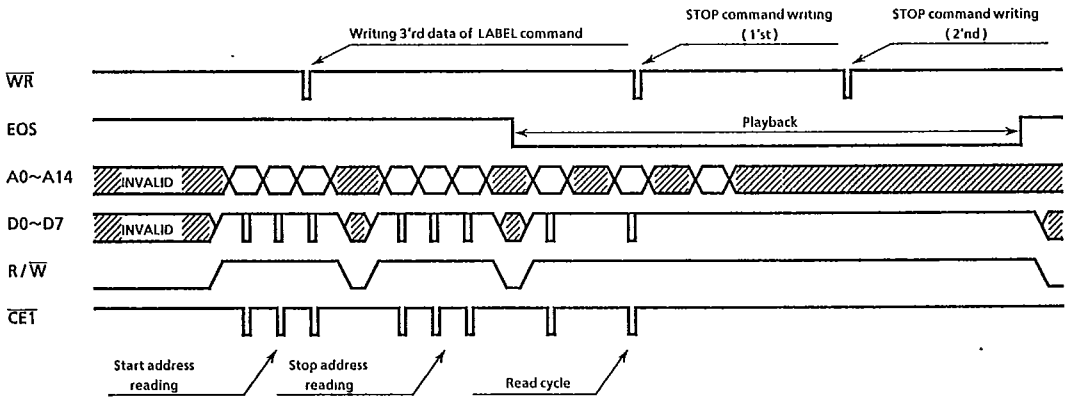


Fig. 5.35 Recording at CPU control with LABEL INDEX MODE

(3) Playback (Force the stop command)



(4) Playback (Auto stop)

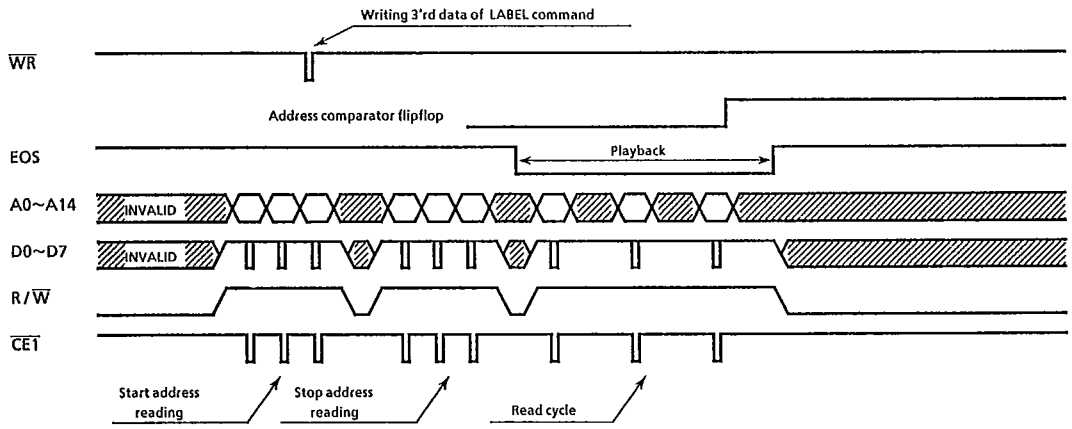
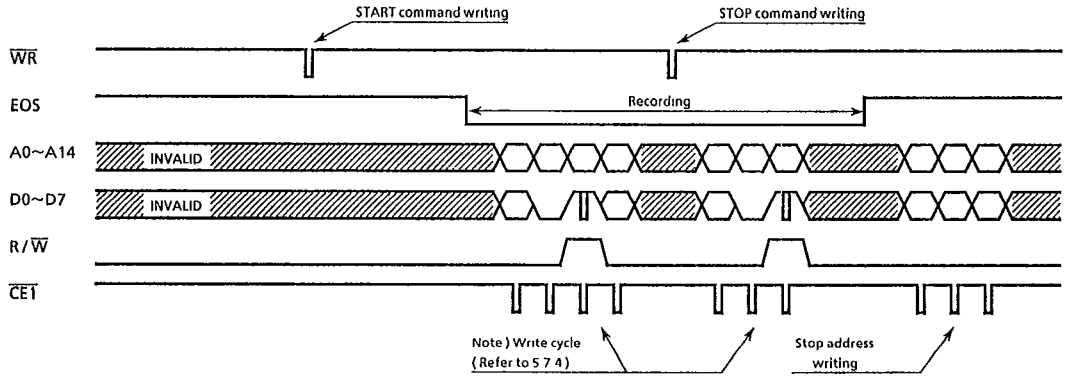


Fig.5.36 Playback at CPU control with LABEL INDEX MODE

5.10.3 Recording / Playback at CPU Control with DIRECT MODE

(1) Recording (Force the stop command)



(2) Recording (Auto stop)

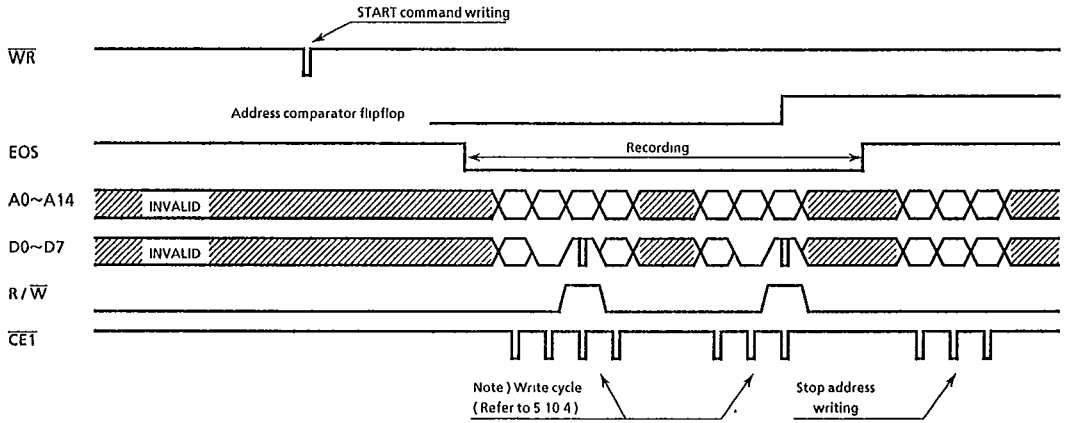
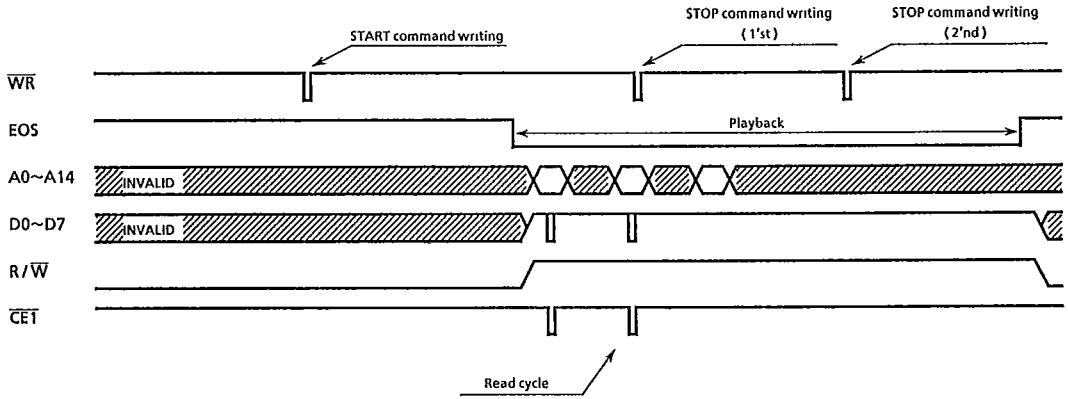


Fig.5.37 Recording at CPU control with DIRECT MODE

(3) Playback (Force the stop command)



(4) Playback (Auto stop)

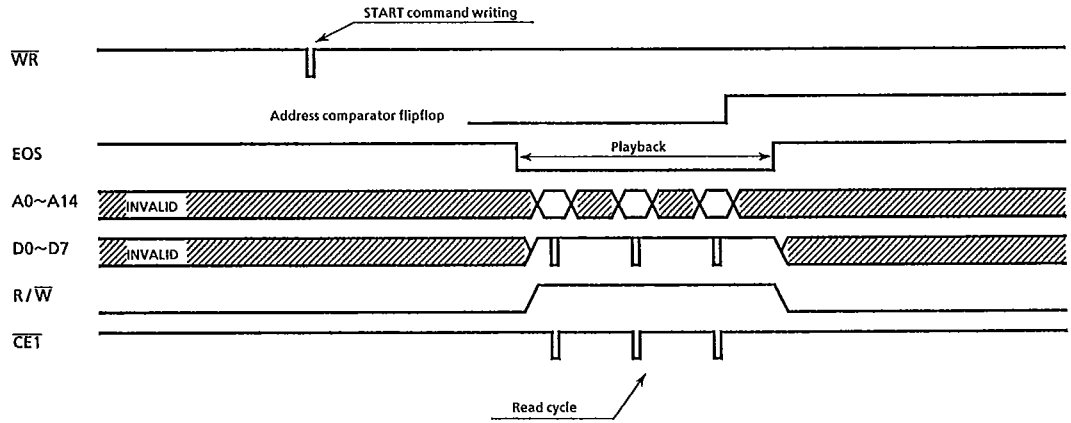


Fig.5.38 Playback at CPU control with DIRECT MODE

5.10.4 Write Cycle

At the recording, TC8830AF is check for number of connected SRAMs. Write timing is explained in following. Further, pulse width etc. refer to section 6.4 AC characteristics.

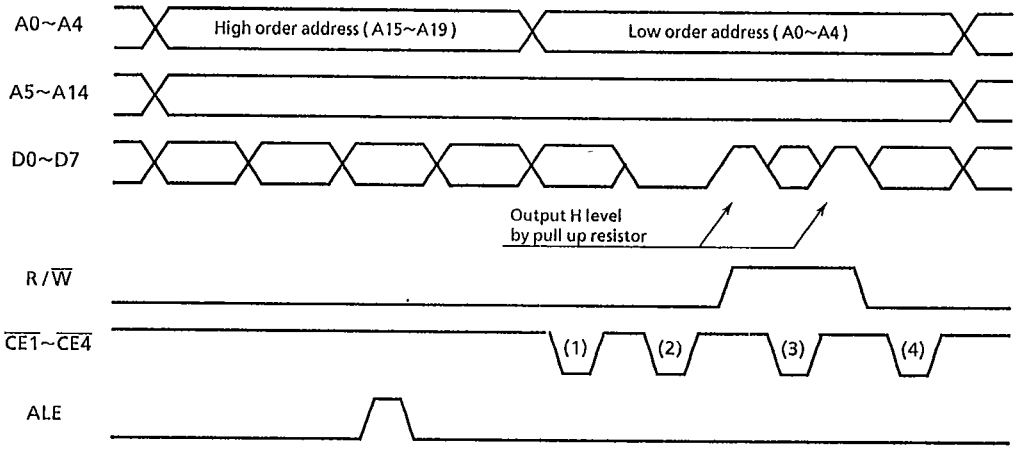


Fig.5.39 Write cycle timing

$\overline{CE1}$~$\overline{CE4}$ pins select to 4 pieces SRAM. $\overline{CE}$(1)~(4) are

$\overline{CE}$(1) Dummy cycle, invalid

$\overline{CE}$(2) Writing L level to SRAM.

$\overline{CE}$(3) Reading the data of step (2). In case of connected SRAM, read out the data is L level, if not connected, the data is II level by internal pull up resister. Stops to recording when the read out data is H level.

$\overline{CE}$(4) When the read data of step (3) is H level, valid of voice data writing to the SRAM.

ALE pin of fig.5.39 means Address Latch Enable, it's possible to expanse SRAMs up to 8Mbit.

5.11 Precautions

5.11.1 At The Both CPU Control and Manual Control.

(1) Under the recording / playback, other than stop should not be issued.

(2) When the $\overline{ACL}$ pin is L level,0 clear to index area of SRAM.

(3) In case of use for standby function, this mode sets at recording / playback waiting state.

5.11.2 At The Manual Control.

(1) The recording phrase number select at sequence from low order phrase.

(2) The maximum address is auto check under the recording, if bad address at SRAMs, stop the recording.

(3) In case of use for auto phrase function, not direct access of more than phrase No.16.

5.11.3 At The CPU Control

(1) Label index mode

- The recording phrase number select at sequence from low order phrase.
- The maximum address is auto check under the recording, if bad address at SRAMs, stop the recording.

(2) Direct mode

- Don't setting the start and stop address at index area.
- Setting to stop address more than start address.

(3) Other

- Keeps at command processing time for data read of DTRD and ADRD command.
- Releasing DMA function, set the $\overline{WR}$ pin at H level after setting the $\overline{RD}$ pin at H level, write the NOP command into the TC8830AF.

5.12 Connection of SRAMs

The TC8830AF uses SRAMs (Static RAMs) for the storage of voice data.

Up to 4 pieces of 64K or 256Kbit SRAMs are directly connected to the TC8830AF. But it is impossible to connect together with different capacity SRAMs in capacity. Select of capacity for 64K / 256K is 256K pin.

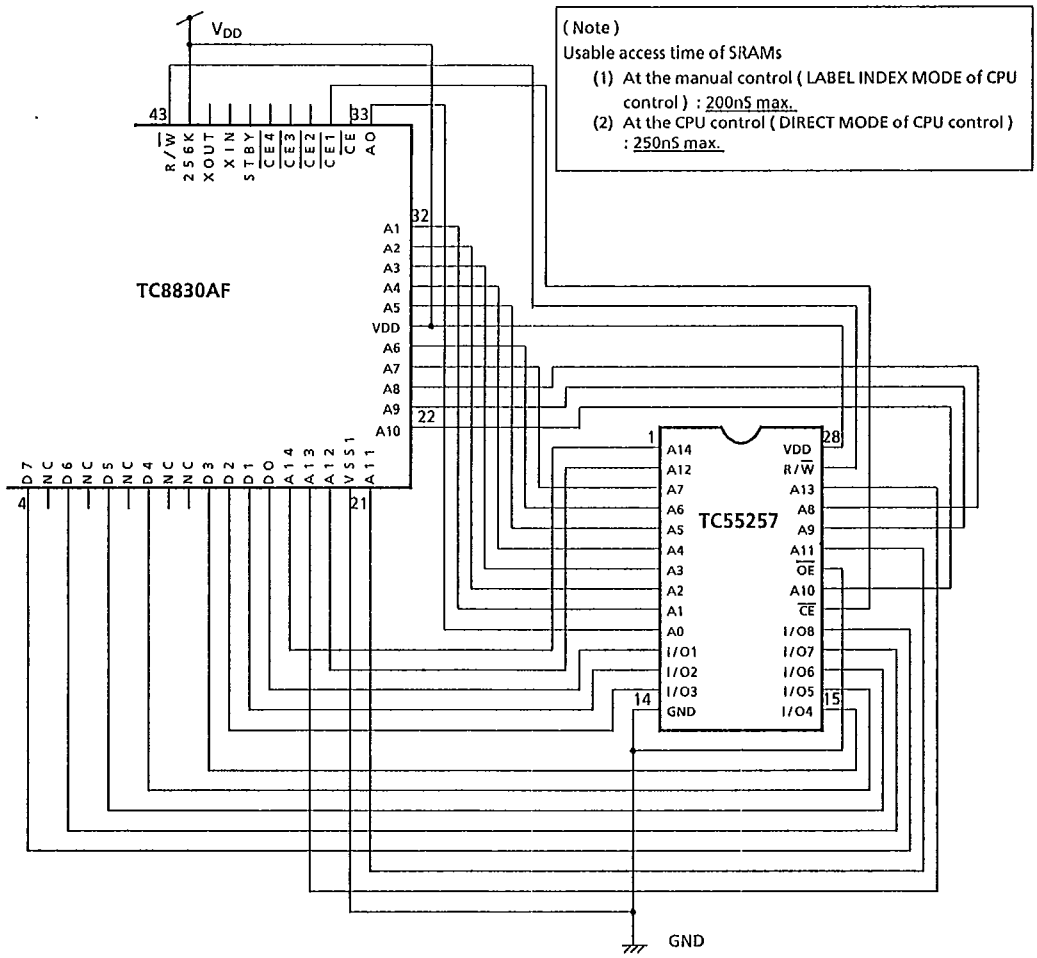


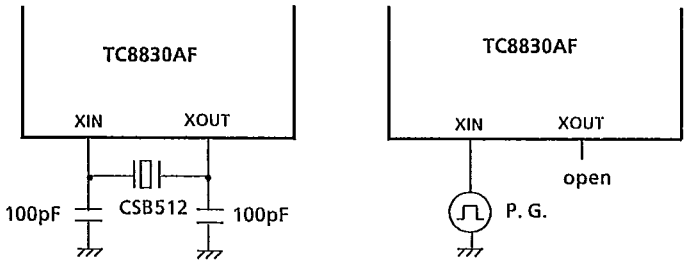
Fig.5.40 Connection of SRAM (In case of 256K DRAM)

Fig.5.40 shows the connection with SRAM. In case of two or more SRAMs, $\overline{CE1}$ pin of TC8830AF must be connected to the $\overline{CE}$ pin of 1st SRAM, the $\overline{CE2}$ to the $\overline{CE}$ of 2nd SRAM and so on, That is, $\overline{CE1}$~$\overline{CE4}$ pins must be connected to the $\overline{CE}$ pins of each SRAM respectively. Other pins for SRAM of TC8830AF may be connected in parallel to every SRAM.

5.13 Clock Generator

TC8830AF has clock generator, ceramic resonator and capacitor are connected between XIN and XOUT pins.

If using external clock, it should be fed to XIN pin directly. (XOUT should be left open).



(a) Using internal oscillator (b) Using external oscillator

Fig.5.41 Oscillator

5.14 Analog Circuit

The TC8830AF incorporates microphone amplifier and band pass filter. Therefore, voice recording / playback system is easily composed with a microphone and an audio amplifier circuit.

5.14.1 Microphone Amplifier Part

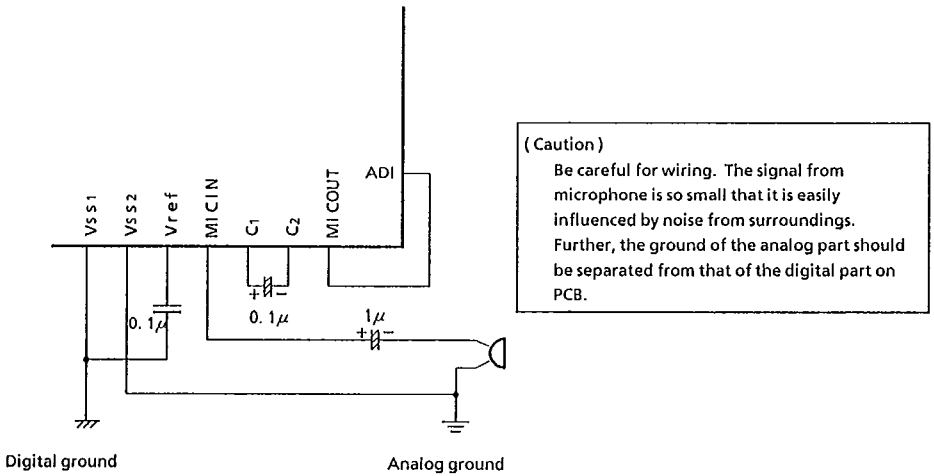


Fig.5.42 Connection of microphone

Microphone amplifier includes two stage.

①Between MICIN and C1 → Gain is about 26dB

②Between C2 and MICOUT → Gain is about 20dB

So, there are three ways ①, ②, and ① + ②. One is selected according to the type of microphone. C1 or MICOUT pin should be connected to ADI pin at the case of ①, ②, and ① + ②, respectively.

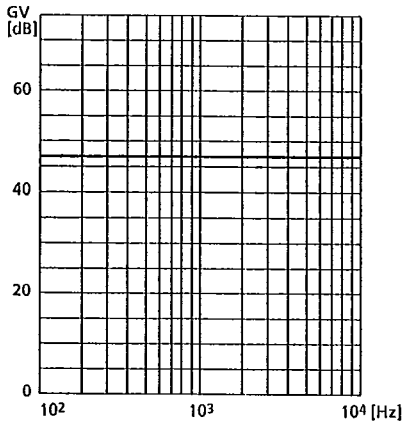


Fig.5.43 Frequency characteristics of microphone amplifier
(Between MICIN and MICOUT)

Fig.5.43 Shows microphone amplifier characteristic between MICIN and MICOUT with couplings C1 and C2.

Further, when on-chip Microphone amplifier is not used, it is possible to apply voice signal directly into ADI pin. If a voice signal which is applied to ADI pin is not biased to Vref level, a coupling capacitor of about 0.1 μF~ 1μF should be inserted into the circuit.

Microphone amplifier not operating under the others of recording waiting state and recording. in case of use for on-chip microphone amplifier, should be a waiting time for change playback waiting state to recording waiting state. This time is about 100ms at the case of connected 0.1 μF between C1 and C2 pins.

5.14.2 Filter Part

The frequency characteristic of the band pass filter which is on chip the TC8830AF is shown in Fig.5.44.

The band pass filter consists of a combination of the 1'st order high pass filter and 2'nd order low pass filter.

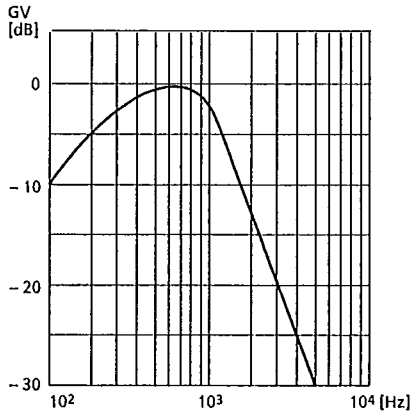


Fig.5.44 Frequency characteristics of band pass filter
(Between FILIN and FILOUT)

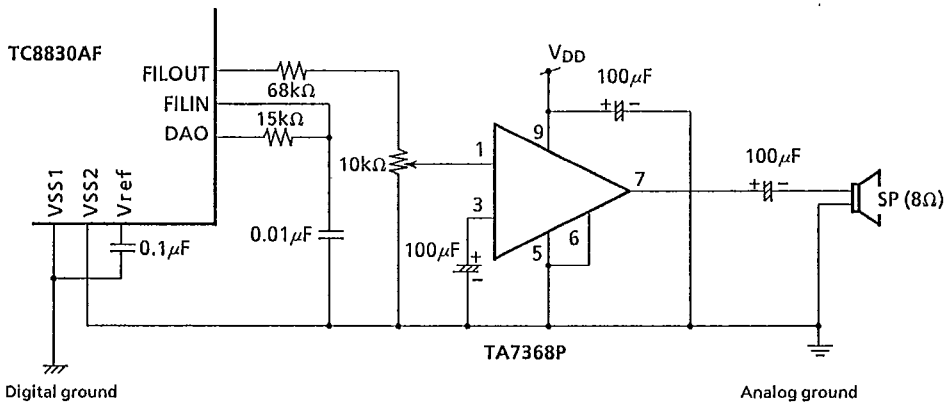


Fig.5.45 Connection of audio amplifier

5.14.3 Equivalent Circuit

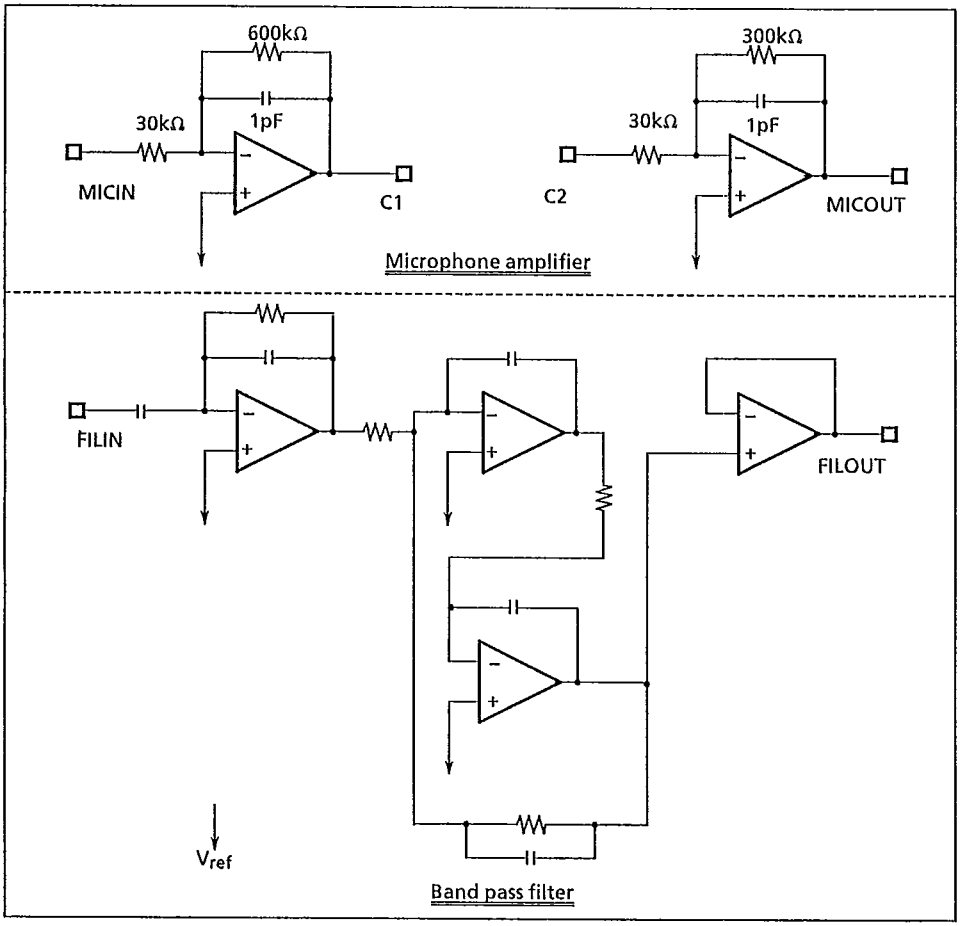


Fig.5.46 Equivalent circuit of analog part

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	−0.3 ~ 7.0	V
V_{IN}	Input voltage	−0.3 ~ V_{DD} + 0.3	V
V_{OUT}	Output voltage	−0.3 ~ V_{DD} + 0.3	V
T_{STG}	Storage temperature	−55 ~ 125	°C

6.2 Recommended Operating Conditions

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	4.5 ~ 6.5	V
V_{IN}	Input voltage	0 ~ V_{DD}	V
V_{OUT}	Output voltage	0 ~ V_{DD}	V
T_{OPR}	Operating temperature	−10 ~ 70	°C
f_{CLK}	Oscillation frequency	512	kHz

6.3 DC Characteristics (V_{DD} = 5V ± 10%, Ta = 25°C)

SYMBOL	ITEM		CONDITION	MIN.	TYP.	MAX.	UNIT
f_{CLK1}	Operating frequency 1		Manual control or LABEL INDEX MODE at CPU control	400	512	600	kHz
f_{CLK2}	Operating frequency 2		DIRECT MODE at CPU control	250	512	1000	
I_{IH1}	Input high current 1 (P0~P3, $\overline{WR}$, $\overline{RD}$, PH0~PH3)		V_{IN} = VDD, CPUM = L	10	50	150	μA
I_{IH2}	Input high current 2 (TEST)		V_{IN} = VDD	50	100	500	
I_{IL1}	Input low current 1 (D0~D7)		V_{IN} = 0V	10	50	150	
I_{IL2}	Input low current 2 ($\overline{ACL}$)		V_{IN} = 0V	100	500	1000	
I_{ILK}	Input leakage current		V_{IN} = 0~V_{DD}, CPUM = H	–	–	1.0	
I_{OLK}	Output leakage current		V_{IN} = 0~V_{DD}, $\overline{WR}$, $\overline{RD}$ = L	–	–	1.0	
V_{IH1}	Input high voltage 1		P0~P3, $\overline{WR}$, $\overline{RD}$	2.4	–	–	V
V_{IH2}	Input high voltage 2		Except above	3.4	–	–	
V_{IL1}	Input low voltage 1		P0~P3, $\overline{WR}$, $\overline{RD}$	–	–	0.8	
V_{IL2}	Input low voltage 2		Except above	–	–	0.6	
I_{OH}	Output high current		V_{OUT} = 2.4 V	0.4	–	–	mA
I_{OL}	Output low current		V_{OUT} = 0.4 V	0.4	–	–	
I_{SS1O}	Supply current 1 (V_{SS1})	Operation mode	Under no signal I_{OUT} = 0 mA	–	–	3	mA
I_{SS1S}		Standby mode	Under no signal I_{OUT} = 0 mA	–	–	3	μA
I_{SS2O}	Supply current 2 (V_{SS2})	Operation mode	Under no signal I_{OUT} = 0 mA	–	–	3	mA
I_{SS2S}		Standby mode	Under no signal I_{OUT} = 0 mA	–	–	3	μA
V_{OUT}	Reference voltage of analog part		Vref	–	2.8	–	V

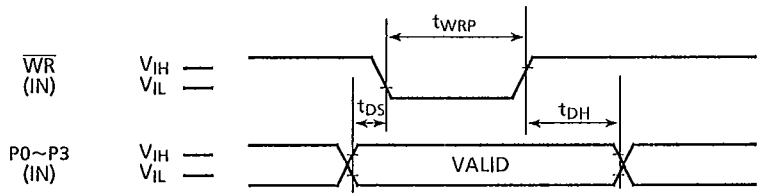
Precautions:
1) Each TYP. value is measured under VDD=5.0V, Ta=25°C.
2) MIN. MAX. values are defined by their absolute values.
3) Supply current measured by external oscillator of 512kHz.

6.4 AC Characteristics (V_{DD} = 5V, Ta = 25°C, CL = 50pF)

6.4.1 Data Write

(1) Except data write after the DTWR command (command write)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{DS}	Data set up time	0	—	—	ns
t_{DH}	Data hold up time	200	—	—	
t_{WRP}	$\overline{WR}$ pulse width	400	—	—	



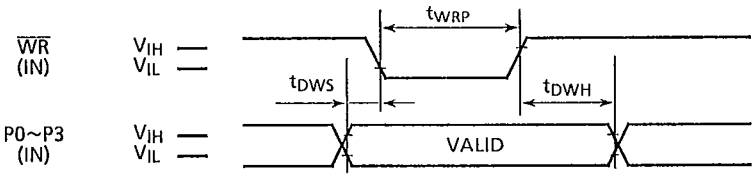
Input level
- V_{IH} = 2.6V
- V_{IL} = 0.6V

Comparison level
- V_{IH} = 2.4V
- V_{IL} = 0.8V
- V_{OH} = 2.4V
- V_{OL} = 0.8V

(2) Data write after the DTWR command

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{DWS}	Data write set up time	0	—	—	ns
t_{DWH}	Data write hold time	500 + t_H	—	—	

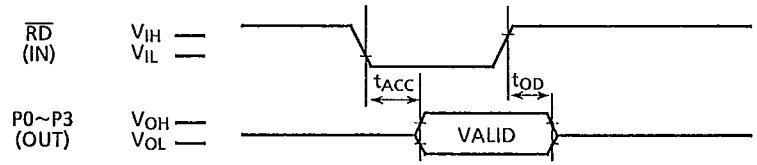
t_H = Data hold time of SRAM



6.4.2 Data Read

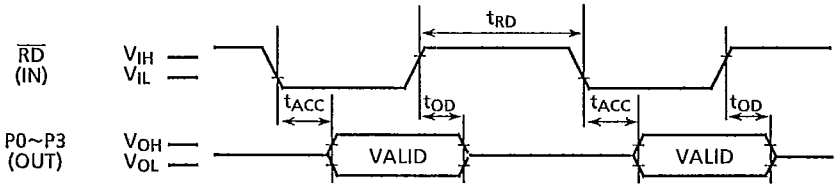
(1) Status read

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Read access time	—	—	800	ns
t_{OD}	Output disable time	—	—	200	



(2) Address read

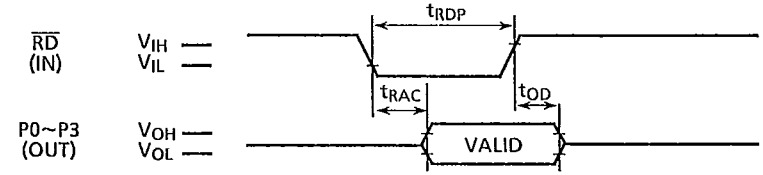
SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{RD}	Read disable time	$70/f_{CLK}$	—	—	sec.



(3) Data read after the DTRD command

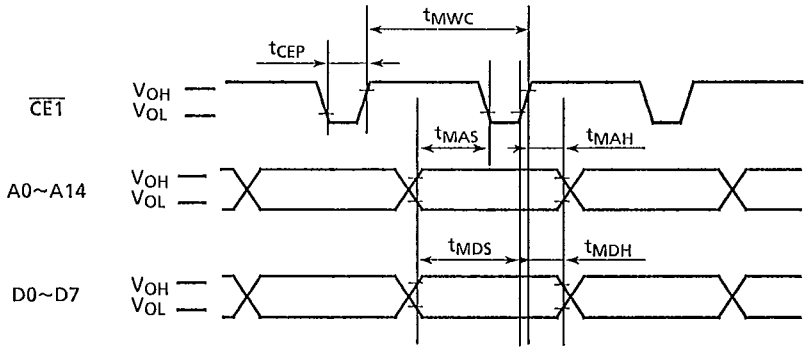
SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{RAC}	Data read access time	—	—	$2+t_{AC}$	μs
t_{RDP}	Data read $\overline{RD}$ pulse width	$3+t_{AC}$	—		

t_{AC} = Access time of SRAM



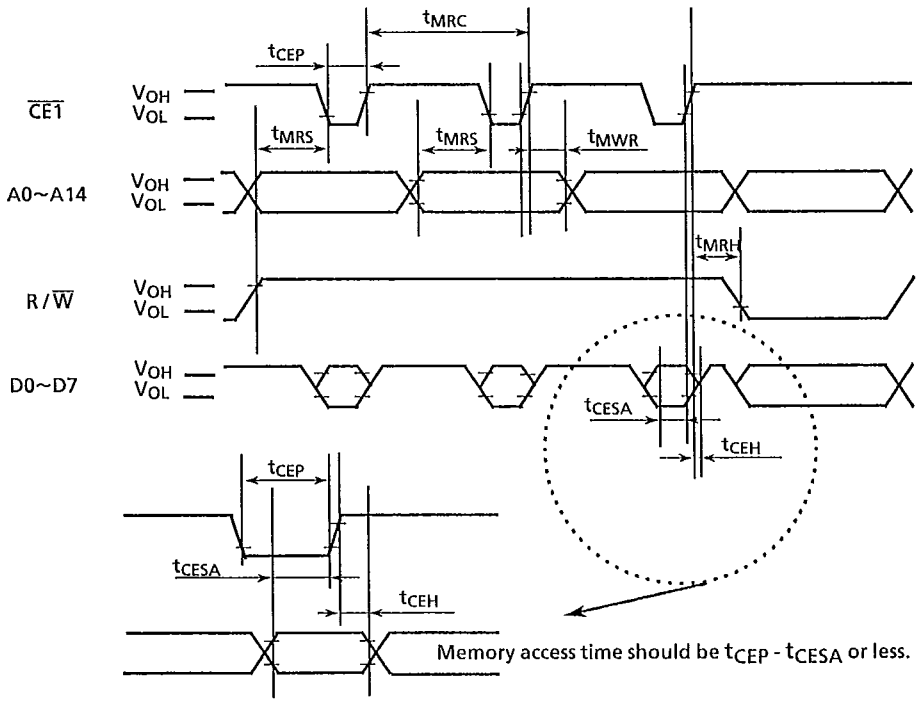
6.4.3 Write Cycle of Start Address and Stop Address
(at the Manual control and LABEL INDEX MODE in the CPU control)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{CEP}	$\overline{CE}$ pulse width	—	1/2fCLK	—	sec.
t_{MWC}	Memory write cycle time	—	4/fCLK	—	
t_{MAS}	Memory address set up time	—	3/fCLK	—	
t_{MAH}	Memory address hold time	—	1/2fCLK	—	
t_{MDS}	Memory data set up time	—	7/2fCLK	—	
t_{MDH}	Memory data hold time	—	1/2fCLK	—	



6.4.4 Read Cycle of Start Address and Stop Address
(at the Manual control and LABEL INDEX MODE in the CPU control)

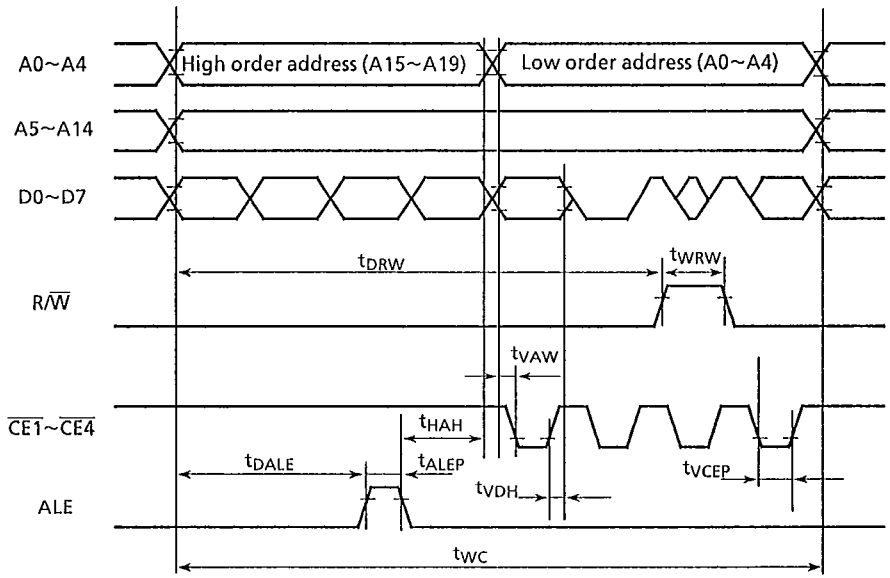
SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{MRS}	Memory read command set up time	—	3 / fCLK	—	sec.
t_{MRH}	Memory read command hold time	—	1 / 2fCLK	—	
t_{MRC}	Memory read write cycle	—	4 / fCLK	—	
t_{CESA}	Memory data set up time	600	—	—	ns
t_{CEH}	Memory data hold time	0	—	—	



6.4.5 Voice Data Write Cycle

SYMBOL	ITEM	BIT RATE				UNIT
		32Kbps	16Kbps	11Kbps	8Kbps	
t_{WC}	Write cycle time	128 / fCLK	256 / fCLK	384 / fCLK	512 / fCLK	sec.
t_{VCEP}	Voice data $\overline{CE}$ pulse width	4 / fCLK	4 / fCLK	4 / fCLK	4 / fCLK	
t_{VAW}	Write address set up time	4 / fCLK	4 / fCLK	4 / fCLK	4 / fCLK	
t_{VDH}	Voice data hold time	8 / fCLK	24 / fCLK	40 / fCLK	56 / fCLK	
t_{DALE}	ALE delay time	36 / fCLK	68 / fCLK	100 / fCLK	132 / fCLK	
t_{ALEP}	ALE pulse width	4 / fCLK	4 / fCLK	4 / fCLK	4 / fCLK	
t_{HAH}	High order address hold time	88 / fCLK	184 / fCLK	280 / fCLK	376 / fCLK	
t_{DRW}	R/$\overline{W}$ delay time	96 / fCLK	192 / fCLK	288 / fCLK	384 / fCLK	
t_{WRW}	R/$\overline{W}$ pulse width	16 / fCLK	32 / fCLK	48 / fCLK	64 / fCLK	

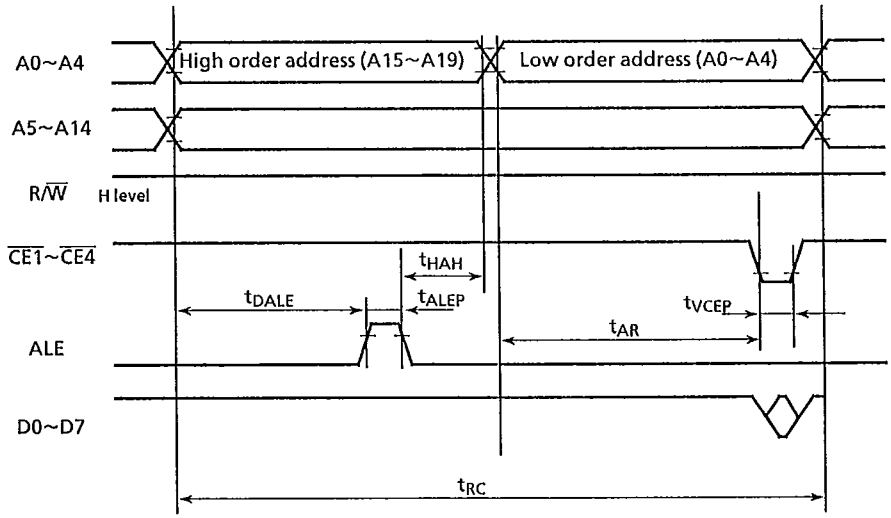
Every value is typ. value



6.4.6 Voice Data Read Cycle

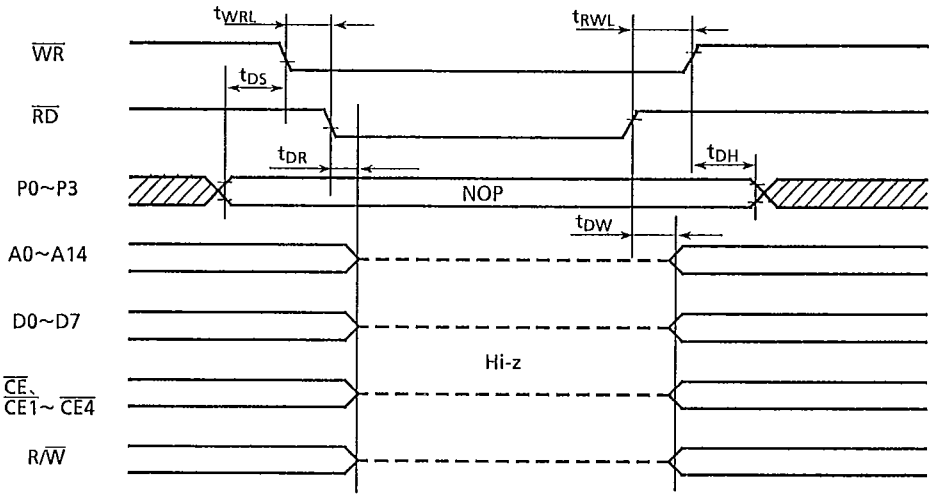
SYMBOL	ITEM	BIT RATE				UNIT
		32Kbps	16Kbps	11Kbps	8Kbps	
t_{RC}	Read cycle time	128 / fCLK	256 / fCLK	384 / fCLK	512 / fCLK	sec.
t_{AR}	Read address set up time	4 / fCLK	4 / fCLK	4 / fCLK	4 / fCLK	

Every value is typ. value



6.4.7 DMA Function

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{WRL}	Write to read disable time	1.0	—	—	μs
t_{RWL}	Read to write disable time	100	—	—	ns
t_{DR}	Hi-z delay time	—	—	300	
t_{DW}	Data set delay time	—	—	300	
t_{DS}	Data set up time	0	—	—	
t_{DH}	Data hold time	200	—	—	



6.5 Characteristics of Analog Circuit

(Unless otherwise specified : VSS1 = VSS2 = 0V, VDD = 5V, Ta = 25 °C, fin = 1 kHz)

6.5.1 Microphone Amplifier

SYMBOL	ITEM	PINS	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN1}	Range of input voltage	MICIN	MICAMP (1) + (2)	–	12	16	mV_{p-p}
V_{IN2}		MICIN	MICAMP (1)	–	120	160	
V_{IN3}		C2	MICAMP (2)	–	240	320	
G_{V1}	Pass band gain	MICIN – MICOUT	$V_{IN} = 6mV_{p-p}$, $f_{IN} = 100Hz \sim 10kHz$, Output load = 100kΩ, 30pF	–	46	–	dB
G_{V2}		MICIN – C1		–	26	–	
G_{V3}		C2 – MICOUT		–	20	–	
THD	Total harmonic distortion	MICIN – MICOUT	$V_{IN} = 6mV_{p-p}$	–	–	2	%
R_{IN1}	Input impedance	MICIN	–	–	30	–	kΩ
R_{IN2}		C2		–	30	–	
R_{OUT1}	Output impedance	C1	–	–	7	–	kΩ
R_{OUT2}		MICOUT		–	7	–	

6.5.2 Band Pass Filter

SYMBOL	ITEM	PINS	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Range of input voltage	FILIN	–	–	–	4.0	V_{p-p}
G_V	Pass band gain	FILIN – FILOUT	$V_{IN} = 1.0V_{p-p}$, Output load = 100kΩ, 30pF	–	–	0	dB
THD	Total harmonic distortion	FILIN – FILOUT	$V_{IN} = 1.0V_{p-p}$	–	–	4	%
R_{IN}	Input impedance	FILIN	–	–	7	–	MΩ
R_{OUT}	Output impedance	FILOUT	–	–	5	–	kΩ

2

6.5.3 Audio In

SYMBOL	ITEM	PIN	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Range of input voltage	ADI	–	–	–	3.2	V_{p-p}
R_{IN}	Input impedance	ADI	–	–	50	–	kΩ

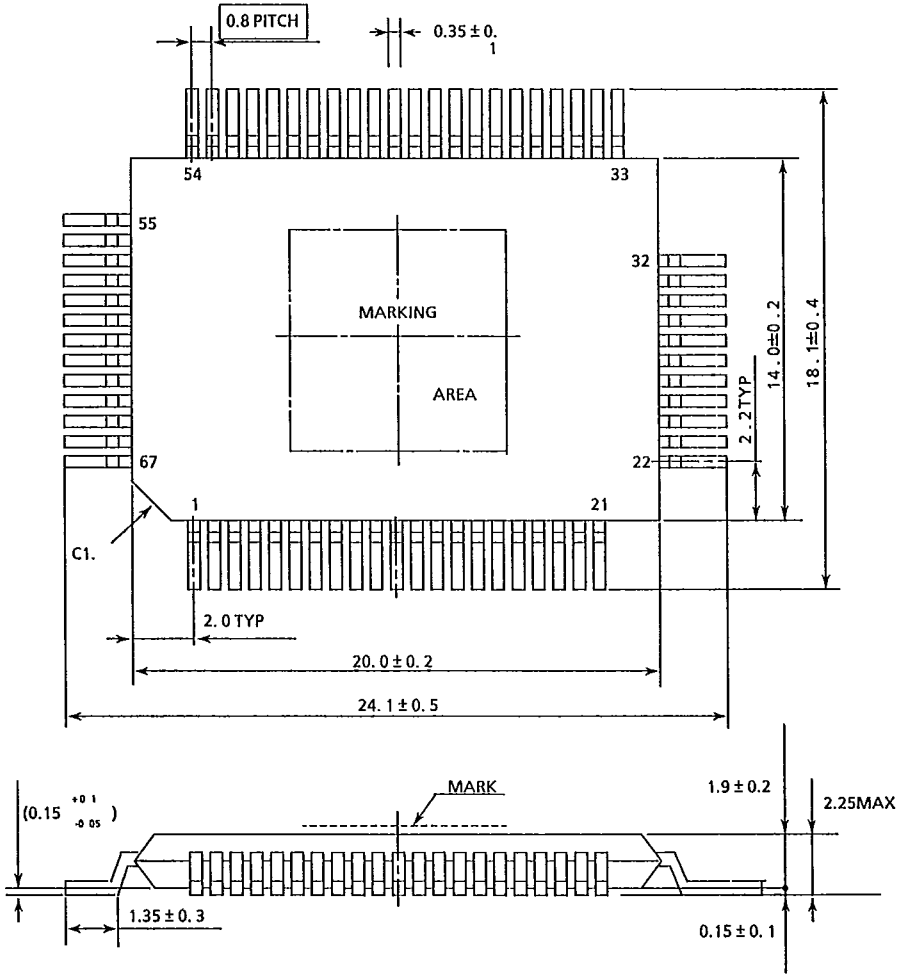
6.5.4 Audio Out

SYMBOL	ITEM	PIN	CONDITION	MIN.	TYP.	MAX.	UNIT
R_{OUT}	Output impedance	DAO	–	–	5	–	kΩ

7. OUTLINE DRAWINGS

67 PIN FLAT PACKAGE
(67-4-BS)

Unit in mm



8. APPLICATION CIRCUIT

MANUAL CONTROL TYPE