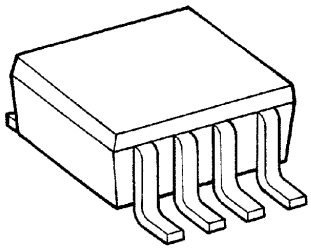
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC7WH240FU, TC7WH240FK

## DUAL BUS BUFFER
## INVERTED, 3-STATE OUTPUTS

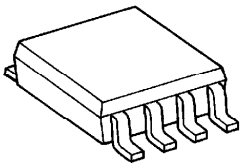
The TC7WH240 is an advanced high speed CMOS DUAL BUS BUFFERS fabricated with silicon gate CMOS technology.
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
The 7WH240 is an inverting 3-state buffer having two active-low output enables.
This device is designed to be used with 3-state memory address drivers, etc.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V system and two supply system such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC7WH240FU



SSOP8-P-0.65

TC7WH240FK



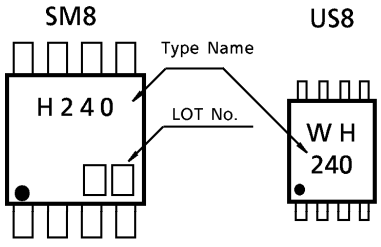
SSOP8-P-0.50A

Weight
SSOP8-P-0.65 : 0.02g (Typ.)
SSOP8-P-0.50A : 0.01g (Typ.)

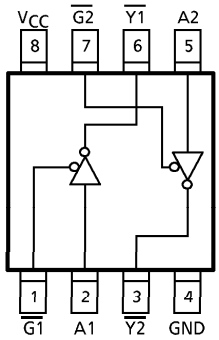
**FEATURES**

- High Speed ..... $t_{pd}$ = 3.9ns (Typ.) at $V_{CC}$ = 5V
- Low Power Dissipation ..... $I_{CC}$ = 2$\mu$A (Max.) at Ta = 25°C
- High Noise Immunity ..... $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operation Voltage Range ... $V_{CC}$ (opr) = 2~5.5V
- Low Noise ..... $V_{OLP}$ = 0.8V (Max.)

**MARKING**




**PIN ASSIGNMENT** (TOP VIEW)

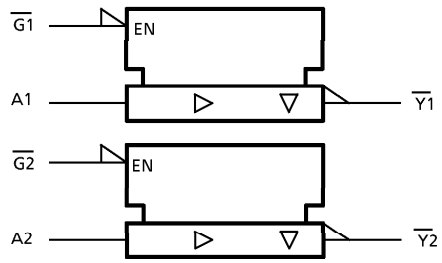



980508EBA2

**MAXIMUM RATINGS** (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | −0.5~7.0 | V |
| DC Input Voltage | $V_{IN}$ | −0.5~7.0 | V |
| DC Output Voltage | $V_{OUT}$ | −0.5~$V_{CC}$+0.5 | V |
| Input Diode Current | $I_{IK}$ | −20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$ / Ground Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 300 (SM8) | mW |
| | | 200 (US8) | |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |
| Lead Temperature (10 s) | $T_L$ | 260 | °C |

**LOGIC DIAGRAM**




**TRUTH TABLE**

| INPUTS | | OUTPUTS |
|---|---|---|
| $\overline{G}$ | A | $\overline{Y}$ |
| L | L | H |
| L | H | L |
| H | × | Z |

× : Don't Care
Z : High Impedance

**RECOMMENDED OPERATING CONDITIONS**

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2~5.5 | V |
| Input Voltage | $V_{IN}$ | 0~5.5 | V |
| Output Voltage | $V_{OUT}$ | 0~$V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | −40~85 | °C |
| Input Rise and Fall Time | dt / dv | 0~100 ($V_{CC}$ = 3.3 ± 0.3V) | ns / V |
| | | 0~20 ($V_{CC}$ = 5 ± 0.5V) | |

**DC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | SYMBOL | TEST CONDITION | | $V_{CC}$ (V) | Ta = 25°C MIN. | Ta = 25°C TYP. | Ta = 25°C MAX. | Ta = −40~85°C MIN. | Ta = −40~85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | — | | 2.0 | 1.5 | — | — | 1.5 | — | V |
| | | | | 3.0~5.5 | $V_{CC}$ ×0.7 | — | — | $V_{CC}$ ×0.7 | — | |
| Low-Level Input Voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.5 | — | 0.5 | V |
| | | | | 3.0~5.5 | — | — | $V_{CC}$ ×0.3 | — | $V_{CC}$ ×0.3 | |
| High-Level Output Voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −8mA | 4.5 | 3.94 | — | — | 3.8 | — | |
| Low-Level Output Voltage | $V_{OL}$ | $V_{IN}$ = $V_{IL}$ | $I_{OL}$ = 50μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 8mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| 3-State Output Off-State Current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.25 | — | ±2.5 | μA |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 0~5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 2.0 | — | 20.0 | μA |

**AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f = 3ns$)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | | | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $C_L$ (pF) | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Propagation Delay Time | $t_{pLH}$ $t_{pHL}$ | | 3.3 ± 0.3 | 15 | — | 5.3 | 7.5 | 1.0 | 9.0 | ns |
| | | | | 50 | — | 7.8 | 11.0 | 1.0 | 12.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 3.6 | 5.5 | 1.0 | 6.5 | |
| | | | | 50 | — | 5.1 | 7.5 | 1.0 | 8.5 | |
| 3-State Output Enable Time | $t_{pZL}$ $t_{pZH}$ | $R_L = 1k\Omega$ | 3.3 ± 0.3 | 15 | — | 6.6 | 10.6 | 1.0 | 12.5 | ns |
| | | | | 50 | — | 9.1 | 14.1 | 1.0 | 16.0 | |
| | | | 5.0 ± 0.5 | 15 | — | 4.7 | 7.3 | 1.0 | 8.5 | |
| | | | | 50 | — | 6.2 | 9.3 | 1.0 | 10.5 | |
| 3-State Output Disable Time | $t_{pLZ}$ $t_{pHZ}$ | $R_L = 1k\Omega$ | 3.3 ± 0.3 | 50 | — | 10.3 | 14.0 | 1.0 | 16.0 | ns |
| | | | 5.0 ± 0.5 | 50 | — | 6.7 | 9.2 | 1.0 | 10.5 | |
| Output to Output Skew | $t_{osLH}$ $t_{osHL}$ | (Note 1) | 3.3 ± 0.3 | 50 | — | — | 1.5 | — | 1.5 | ns |
| | | | 5.0 ± 0.5 | 50 | — | — | 1.0 | — | 1.0 | |
| Input Capacitance | $C_{IN}$ | | | | — | 4 | 10 | — | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | | | — | 6 | — | — | — | pF |
| Power Dissipation Capacitance (Note 2) | $C_{PD}$ | | | | — | 17 | — | — | — | pF |

(Note 1) : Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

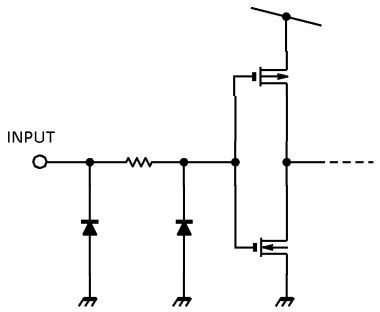
(Note 2) : $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \quad \text{(per bit)}$$

**NOISE CHARACTERISTICS** (Ta = 25°C, Input $t_r = t_f = 3ns$)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | TYP. | LIMIT | UNIT |
|---|---|---|---|---|---|---|
| Quiet Output Maximum Dynamic $V_{OL}$ | $V_{OLP}$ | $C_L$ = 50pF | 5.0 | 0.5 | 0.8 | V |
| Quiet Output Minimum Dynamic $V_{OL}$ | $V_{OLV}$ | $C_L$ = 50pF | 5.0 | − 0.5 | − 0.8 | V |
| Minimum High Level Dynamic Input Voltage | $V_{IHD}$ | $C_L$ = 50pF | 5.0 | — | 3.5 | V |
| Maximum Low Level Dynamic Input Voltage | $V_{ILD}$ | $C_L$ = 50pF | 5.0 | — | 1.5 | V |

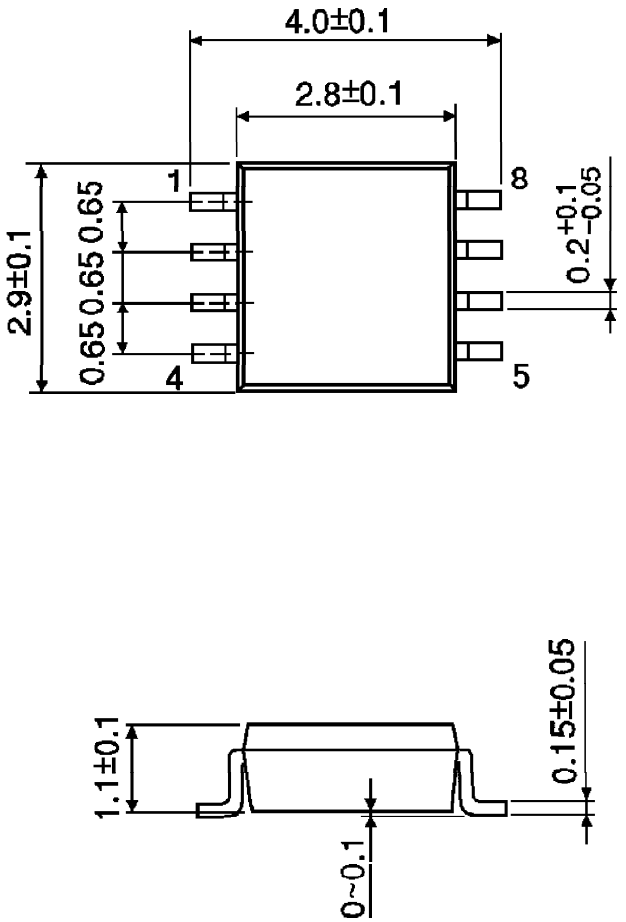
**INPUT EQUIVALENT CIRCUIT**



**OUTLINE DRAWING**

SSOP8-P-0.65

Unit : mm

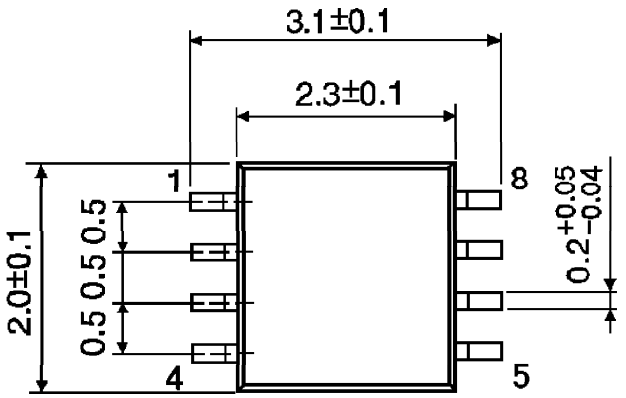


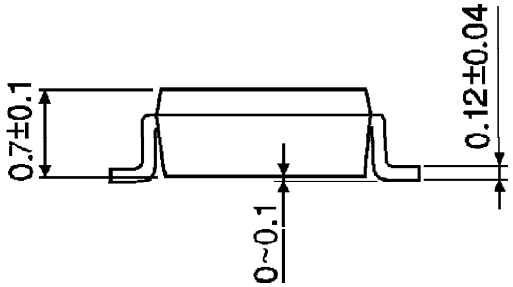

Weight : 0.02g (Typ.)

**OUTLINE DRAWING**

SSOP8-P-0.50A

Unit : mm




Weight : 0.01g (Typ.)