TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX16245AFT

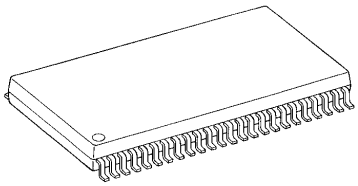
LOW-VOLTAGE 16-BIT BUS TRANSCEIVER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16245AFT is a high performance CMOS 16bit BUS TRANSCEIVER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This 16bit bus transceiver is controlled by direction control (DIR) inputs and output enable ($\overline{OE}$) inputs which are common to each byte. It can be used as two 8bit transceiver or one 16bit transceiver. The direction of data transmission is determined by the level of the DIR inputs. The $\overline{OE}$ inputs can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



TSSOP48-P-0061-0.50

Weight : 0.25g (Typ.)

FEATURES

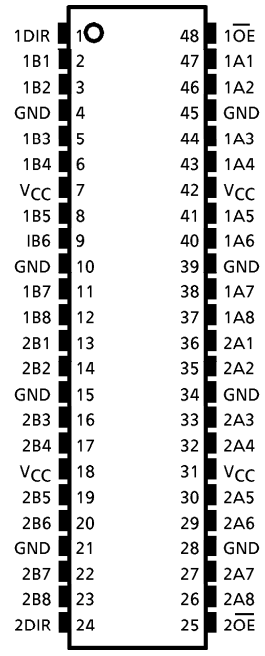
- Low Voltage Operation : $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation : t_{pd} = 5.2 ns (max.) at $V_{CC} = 3.0 \sim 3.6V$
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA (MIN) at $V_{CC} = 3.0V$
- Latch-up Performance : ±500mA
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs

NOTE

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

.2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

PIN CONNECTION



(TOP VIEW)

961001EBA2

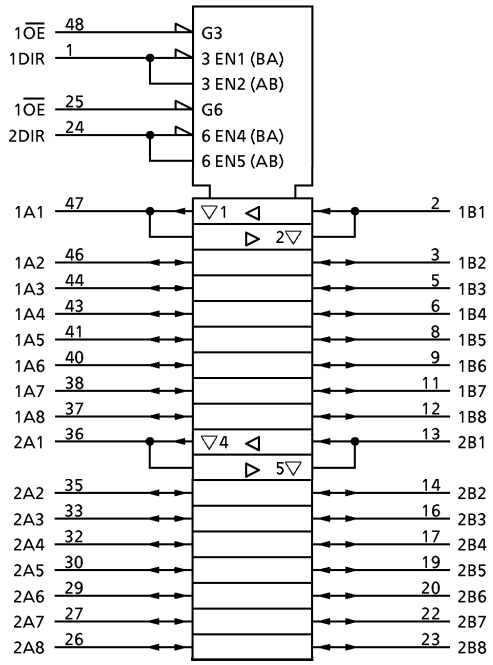
TRUTH TABLE

INPUT		FUNCTION		OUTPUT
$1\overline{OE}$	1DIR	BUS 1A1-1A8	BUS 1B1-1B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

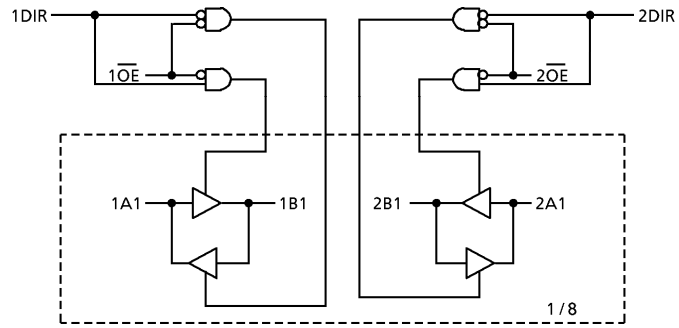
INPUT		FUNCTION		OUTPUT
$2\overline{OE}$	2DIR	BUS 2A1-2A8	BUS 2B1-2B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

X : Don't Care
Z : High impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



961001EBA2'

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{OE}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC}+0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC}/Ground Current Per Supply Pin	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) Output in Off-State
(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) V_{OUT}<GND, V_{OUT}>V_{CC}

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage (DIR, $\overline{OE}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~5.5 (Note 5)	V
		0~V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns/V

(Note 4) Data Retention Only
(Note 5) Output in Off-State
(Note 6) High or Low State
(Note 7) V_{CC} = 3.0~3.6V
(Note 8) V_{CC} = 2.7~3.0V
(Note 9) V_{IN} = 0.8~2.0V, V_{CC} = 3.0V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} −0.2	—	V
				I_{OH} = −12mA	2.7	2.2	—	
				I_{OH} = −18mA	3.0	2.4	—	
				I_{OH} = −24mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
				I_{OL} = 12mA	2.7	—	0.4	
				I_{OL} = 16mA	3.0	—	0.4	
				I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN} / V_{OUT} = 5.5V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±20.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

AC characteristics (Ta = −40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig.1, 2)	2.7	—	6.2	ns
			3.3 ± 0.3	1.5	5.2	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	2.7	—	7.5	ns
			3.3 ± 0.3	1.5	6.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	2.7	—	7.0	ns
			3.3 ± 0.3	1.5	6.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic switching characteristics
(Ta = 25°C, Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

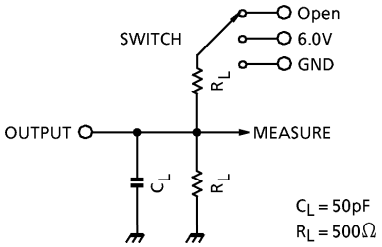
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP	UNIT
Input Capacitance	C_{IN}	DIR, $\overline{OE}$	3.3	7	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn	3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 11)	3.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16$. (Per bit)

Fig.1 Test circuit



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0V
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}

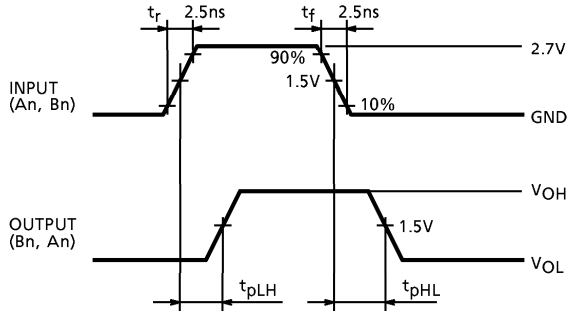
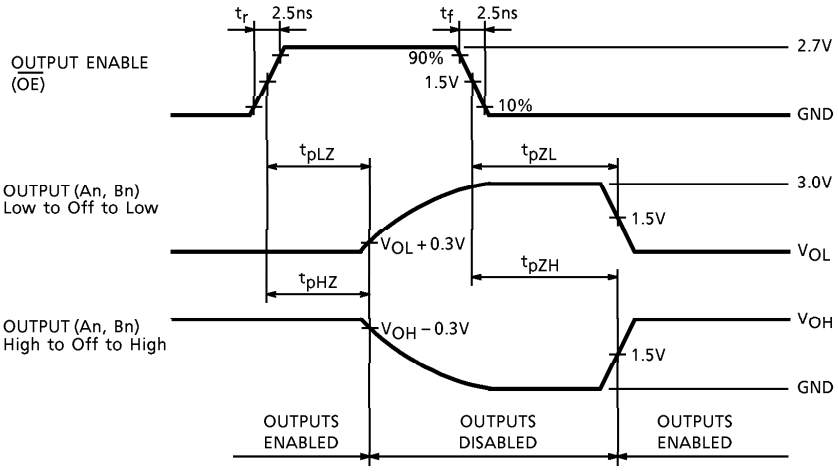
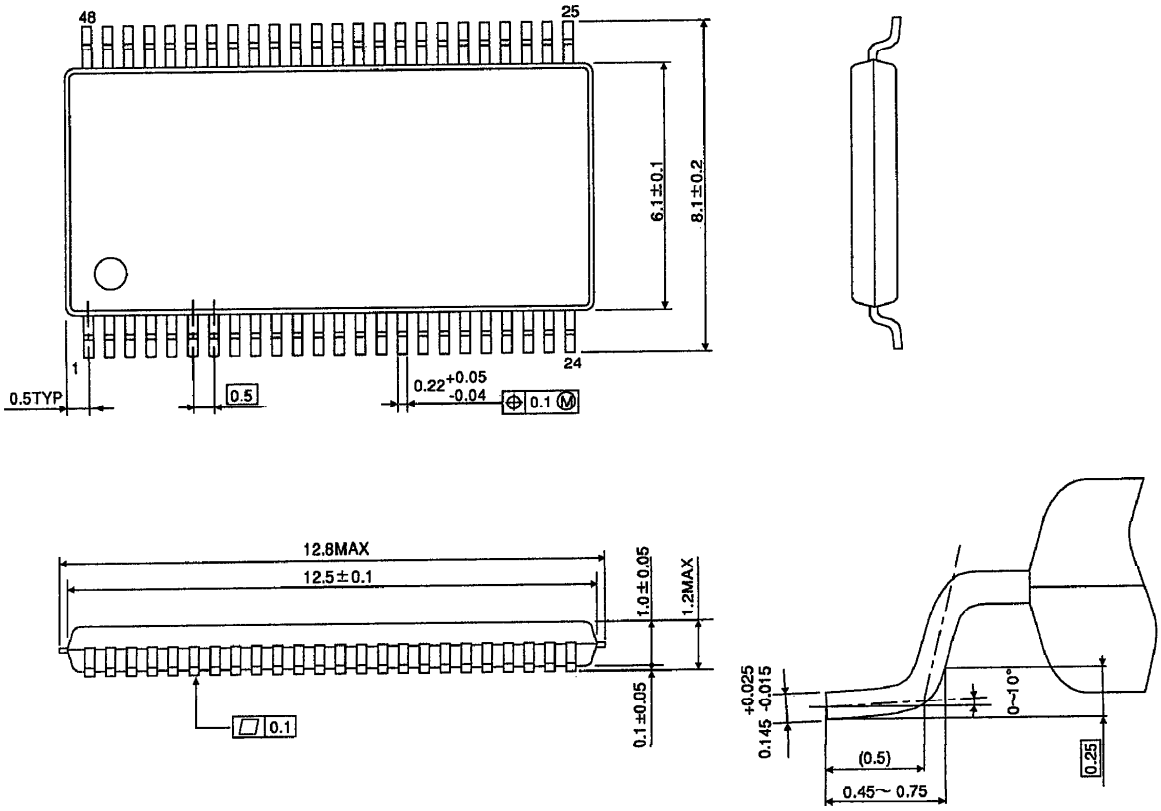


Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



OUTLINE DRAWING

TSSOP48-P-0061-0.50 Unit : mm



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