TOSHIBA
NAND memory
Toggle DDR1.0
Technical Data Sheet

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TOSHIBA
Semiconductor & Storage Products
Memory Division

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1. INTRODUCTION

1.1. General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.

Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.

Toggle DDR1.0 NAND supports the interface speed of up to 100 MHz, which is faster than the data transfer rate offered by SDR NAND. Toggle DDR NAND transfers data at high speed using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

This device supports both SDR interface and Toggle DDR interface. When starting, the device is activated in SDR mode. The interface mode can be changed into Toggle DDR interface utilizing specific command issued by the Host.

1.2. Definitions and Abbreviations

SDR
Acronym for single data rate.

DDR
Acronym for double data rate.

Address
The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

Column
The byte location within the page register.

Row
Refer to the block and page to be accessed.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Plane
The unit that consists of a number of blocks. There are one or more Planes per LUN.

Page register
Register used to transfer data to and from the Flash Array.

Cache register
Register used to transfer data to and from the Host.

Defect area
The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2

Device
The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)
The minimum unit that can independently execute commands and report status. There are one or more LUNs per $\overline{CE}$.

Target
An independent NAND Flash component with its own $\overline{CE}$ signal.

SR[x] (Status Read)
SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to section 5.13 for the definition of bit meanings within the status register.

1.3. Features

Organization

Part number	TC58TEG5DCJ TC58TEG5DCJTA00 (T_{OPER}: 0～70℃) TC58TEG5DCJTAI0 (T_{OPER} : -40～+85℃)
Device capacity	17664 × 256 × 1060 × 8 bits
Page size	17664 Bytes
Block size	(4M + 320 K) Bytes
Plane size	2396651520 Bytes
Plane per one LUN	1 Planes
LUN per one target	1 LUNs
Target per one device	1 targets

- **Modes**

  Basic Operation
  Page Read Operation (with Random Data Output), Data Out After Status Read, Sequential Cache Read Operation, Random Cache Read Operation, Page Program Operation (with Random Data Input), Cache Program Operation, Block Erase Operation, Copy-Back Program Operation (with Random Data Input), Set Feature Operation, Get Feature Operation, Read ID Operation, Read Status Operation, Reset Operation, Reset LUN Operation

  Extend Operation
  Page Copy (2) Operation, Device Identification Table Read Operation, Read Status Enhanced Operation, Read LUN #0 Status Operation

- **Mode control**
  Serial input/output
  Command control

- **Power supply**
  V_{CC} = 2.7 V to 3.6 V
  V_{CCQ} = 2.7 V to 3.6 V / 1.7 V to 1.95V

- **Access time**
  - Cell array to register 100 μs max (TENTATIVE)
    50 μs typ. (TENTATIVE)
  - Data Transfer rate 100 MHz

- **Program/Erase time**
  - Auto Page Program 1400 μs/page typ. (TENTATIVE)
  - Auto Block Erase 5 ms/block typ. (TENTATIVE)

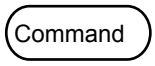
- **Operating current**
  - Read TBD mA max. (per 1 chip)
  - Program (avg.) TBD mA max. (per 1 chip)
  - Erase (avg.) TBD mA max. (per 1 chip)
  - Standby TBD μA max. (per 1 chip)

- **Package**
  (Weight: TBD g typ.)

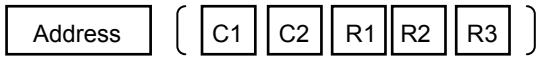
- **Reliability**
  Refer to APPLICATION NOTES AND COMMENTS.

1.4. Diagram Legend

Diagrams in the Toggle DDR1.0 datasheet use the following legend:

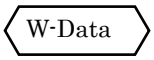


This legend shows the command data. Refer to the Table 29 for more information about the command data.

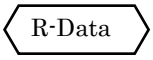


This legend shows the Address data. The addresses are comprised of 2 cycles column address and 3 cycles row address.

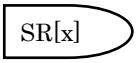
C1: Column address 1
C2: Column address 2
R1: Row address 1
R2: Row address 2
R3: Row address 3



This legend shows Host writing data (data input) to the device.



This legend shows Host reading data (data output) from the device.



This legend shows Host reading the status register within a particular LUN.

2. PHYSICAL INTERFACE

2.1. Pin Descriptions

Table 1 Pin Descriptions

SDR	Toggle DDR1.0	Pin Function
DQ[7:0]	DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE	ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one.
$\overline{WE}$	$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
-	DQS	**DATA STROBE** Output with read data, input with write data. Edge-aligned with read data, centered in write data.
Vcc	Vcc	**POWER** VCC is the power supply for device.
VccQ	VccQ	**DQ POWER** The VccQ is the power supply for input and/or output signals.
Vss	Vss	**GROUND**
VssQ	VssQ	**DQ GROUND** The VssQ is the power supply ground
NC	NC	**No connection** NCs are not internally connected. They can be driven or left unconnected.
NU	NU	**Not use** NUs must be left unconnected.

NOTE:

1) Connect all Vcc and Vss pins of each device to common power supply outputs.

2) Do not leave all Vcc, VccQ, Vss and VssQ disconnected.

2.2. PIN ASSIGNMENT (TOP VIEW)

Tx58TEG5DCJ

SDR only	SDR/Toggle DDR1.0			SDR/Toggle DDR1.0	SDR only
Vcc	Vcc	1	48	Vss	Vss
Vss	Vss	2	47	NC	NC
NC	NC	3	46	VssQ	NU or VssQ
NC	NC	4	45	VccQ	NU or VccQ
NC	NC	5	44	DQ7	DQ7
NC	NC	6	43	DQ6	DQ6
RY/BY	RY/BY	7	42	DQ5	DQ5
RE	RE	8	41	DQ4	DQ4
CE	CE	9	40	VssQ	NU or VssQ
NC	NC	10	39	VccQ	NU or VccQ
NC	NC	11	38	VccQ	VccQ
V_{CC}	V_{CC}	12	37	V_{CC}	V_{CC}
V_{SS}	V_{SS}	13	36	V_{SS}	V_{SS}
NC	NC	14	35	DQS	NU
NC	NC	15	34	VccQ	VccQ
CLE	CLE	16	33	VssQ	NU or VssQ
ALE	ALE	17	32	DQ3	DQ3
WE	WE	18	31	DQ2	DQ2
WP	WP	19	30	DQ1	DQ1
NC	NC	20	29	DQ0	DQ0
NC	NC	21	28	VccQ	NU or VccQ
NC	NC	22	27	VssQ	NU or VssQ
Vss	Vss	23	26	NC	NC
Vcc	Vcc	24	25	Vss	Vss

2.3. BLOCK DIAGRAM

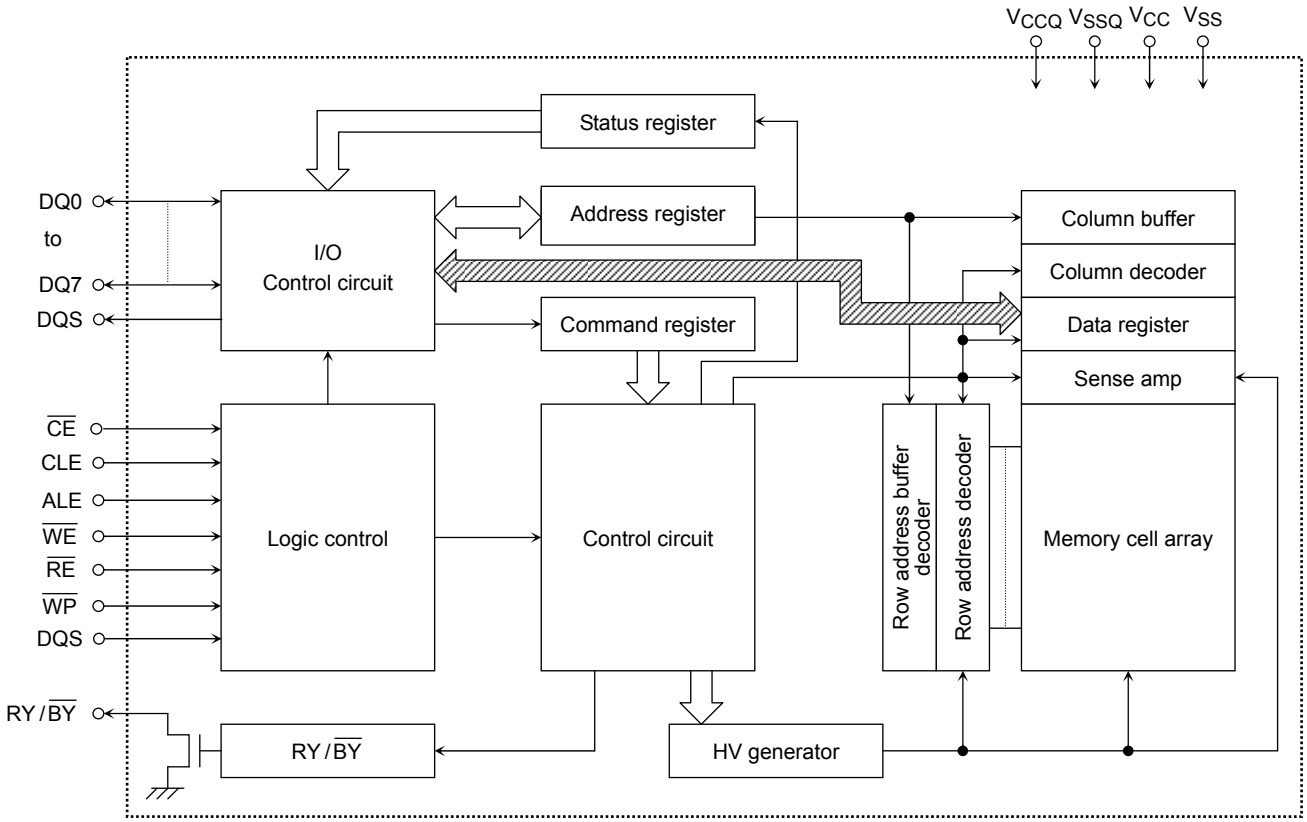


Figure 1. Block Diagram

2.4. Independent Data Buses

There may be two independent 8-bit data buses in some packages, with two, four or eight $\overline{CE}$ signals. If the device supports two independent data buses, then $\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, and $\overline{CE}$ 7 (if connected) shall use the second data bus. $\overline{CE}$ 0, $\overline{CE}$ 2 $\overline{CE}$ 4, and $\overline{CE}$ 6 shall always use the first data bus pins. Note that all $\overline{CE}$ s may use the first data bus and the first set of control signals ($\overline{RE}$ 0, CLE0, ALE0, $\overline{WE}$ 0, and $\overline{WP}$ 0) if the device does not support independent data buses. Table 2 defines the control signal to $\overline{CE}$ signal mapping when there are two independent x8 data buses.

Table 2 Dual Channel(x8) Data Bus Signal to $\overline{CE}$ mapping

Signal Name	CE
R/$\overline{B}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 4
R/$\overline{B}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 5
R/$\overline{B}$ 2	$\overline{CE}$ 2, $\overline{CE}$ 6
R/$\overline{B}$ 3	$\overline{CE}$ 3, $\overline{CE}$ 7
$\overline{RE}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{RE}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
CLE0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
CLE1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
ALE0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
ALE1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
$\overline{WE}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{WE}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
$\overline{WP}$ 0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
$\overline{WP}$ 1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7
DQS0	$\overline{CE}$ 0, $\overline{CE}$ 2, $\overline{CE}$ 4, $\overline{CE}$ 6
DQS1	$\overline{CE}$ 1, $\overline{CE}$ 3, $\overline{CE}$ 5, $\overline{CE}$ 7

Implementations may tie the data lines and control signals ($\overline{RE}$, CLE, ALE, $\overline{WE}$, $\overline{WP}$, and DQS) together for the two independent 8-bit data buses externally to the device.

2.5. Absolute Maximum DC Rating

Stresses greater than those listing in Table 3 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 4 is not recommended. Extended exposure beyond these conditions may affect device reliability.

Table 3 Absolute Maximum Rating

Parameter	Symbol		Rating	Unit
Voltage on any pin relative to VSS	VCC		-0.6 to +4.6	V
	VIN	VccQ(3.3V)	-0.6 to +4.6	
		VccQ(1.8V)	-0.2 to +2.4	
	VI/O	VccQ(3.3V)	-0.6 to +4.6	
		VccQ(1.8V)	-0.2 to +2.4	

2.6. Operating Temperature Condition

Table 4 Operating Temperature Condition

Symbol	Parameter	Part Number	Rating	Unit
TOPER	Operating Temperature Range for Commercial	TC58TEG5DCJTA00	0～70	℃
	Operating Temperature Range for Industrial	TC58TEG5DCJTAI0	-40～+85	
T_{SOLDER}	Soldering Temperature (10 s)		260	
T_{STG}	Storage Temperature		-55～+150	

NOTE:

1) Operating Temperature (T_{OPER}) is the case surface temperature on the center/top side of the NAND.

2) Operating Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between the range specified in the table under all operating conditions.

2.7. Recommended Operating Conditions

Table 5 Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Ground Voltage	VSS	0	0	0	V
Supply Voltage for 1.8V I/O signaling	VccQ	1.7	1.8	1.95	V
Supply Voltage for 3.3V I/O signaling	VccQ	2.7	3.3	3.6	V
Ground Voltage for I/O signaling	VssQ	0	0	0	V

VccQ and Vcc may be distinct and unique voltages. The device shall support one of the following VccQ/Vcc combinations,

Vcc = 3.3V, VccQ = 3.3V
Vcc = 3.3V, VccQ = 1.8V

All parameters, timing modes and other characteristics are related to the supported voltage combination.

2.8. Valid Blocks

Table 6 Valid Blocks

Part Number	Min	Max	Unit
TC58TEG5DCJ	1009	1060	Blocks

NOTE:

1) The device occasionally contains unusable blocks.

2) The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

3) The specification for the minimum number of valid blocks is applicable over the device lifetime.

4) The number of valid blocks includes extended blocks.

2.9. AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from VccQ and VssQ levels. Table 7 defines the maximum values that the AC overshoot or undershoot may attain. These values apply for both 3.3V and 1.8V VccQ levels.

Table 7 AC Overshoot/Undershoot Specification

Parameter	Maximum Value	Unit
	67~100Mhz	
Max. peak amplitude allowed for overshoot area	1	V
Max. peak amplitude allowed for undershoot area	1	V
Max. overshoot area above VccQ	1.8	V*ns
Max. undershoot area above VssQ	1.8	V*ns

NOTE:

1) This specification is intended for devices with no clamp protection and is guaranteed by design.

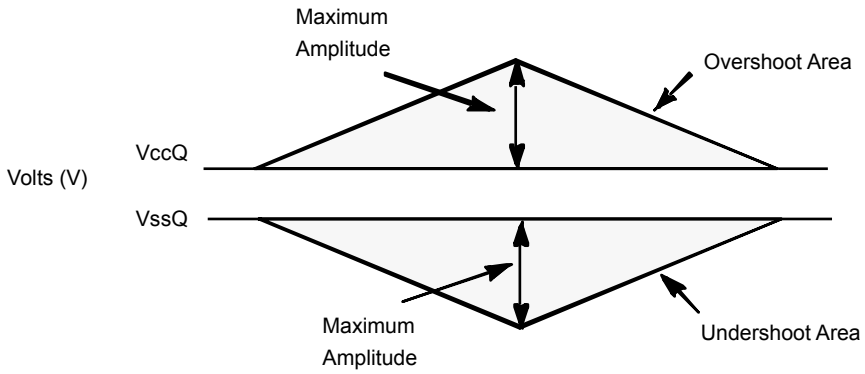


Figure 2. Overshoot/Undershoot Diagram

2.10. DC Operating Characteristics

Table 8 DC & Operating Characteristics for Toggle VccQ=3.3V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Operation Current	I_{CC1}	-	-	-	TBD	mA
Page Program Operation Current	I_{CC2}	-	-	-	TBD	
Erase Operation Current	I_{CC3}	-	-	-	TBD	
DQ Burst Read Current for Vcc	I_{CC4R}	t_{RC}= t_{RC}(min.), Half data switchiing	-	-	80	
DQ Burst Write Current for Vcc	I_{CC4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	80	
DQ Burst Read Current for Vccq	I_{CCQ4R}	t_{RC}= t_{RC}(min.) Half data switching, Cload=0pF, Nominal driver strength	-	-	50	
DQ Burst Write Current for Vccq	I_{CCQ4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	10	
Bus Idle Current	I_{CC5}	-	-	-	TBD	
Stand-by Current(CMOS)	I_{SB}	$\overline{CE}$ =VccQ-0.2, $\overline{WP}$ =0V/VccQ	-	-	TBD	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to VccQ(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to VccQ(max)	-	-	±10	
AC Input High Voltage	V_{IH} (AC)	-	0.8 xVccQ	-	NOTE 5)	V
DC Input High Voltage	V_{IH} (DC)	-	0.7 xVccQ	-	VccQ +0.3	
AC Input Low Voltage	V_{IL} (AC)	-	NOTE 5)	-	0.2 xVccQ	
DC Input Low Voltage	V_{IL} (DC)	-	-0.3	-	0.3 xVccQ	
Output High Voltage Level	V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE:

1) Typical value is measured at Vcc=3.3V, T_{OPER} =25℃. Not 100% tested.

2) V_{OH} and V_{OL} should be available on these two conditions; Output Strength is nominal and VccQ=3.3V, Rpd/Rpu are all VccQx0.5. If the drive strength settings are supported, Table 12shall be used to derive the output driver impedance values.

3) Icc1,2 are without data cache.

4) Icc1/2/3, I_{SB} are the value of one chip, and an unselected chip is in Standby mode.

5) Refer to AC Overshoot and Undershoot requirements.

Table 9 DC & Operating Characteristics for Toggle VccQ=1.8V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Operation Current	I_{CC1}	-	-	-	TBD	mA
Page Program Operation Current	I_{CC2}	-	-	-	TBD	
Erase Operation Current	I_{CC3}	-	-	-	TBD	
DQ Burst Read Current for Vcc	I_{CC4R}	t_{RC}= t_{RC}(min.) Half data switchiing	-	-	80	
DQ Burst Write Current for Vcc	I_{CC4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	80	
DQ Burst Read Current for Vccq	I_{CCQ4R}	t_{RC}= t_{RC}(min.) Half data switching Cload=0pF, Nominal driver strength	-	-	50	
DQ Burst Write Current for Vccq	I_{CCQ4W}	t_{DSC} = t_{DSC} (min.) Half data switching	-	-	10	
Bus Idle Current	I_{CC5}	-	-	-	TBD	
Stand-by Current(CMOS)	I_{SB}	$\overline{CE}$ =VccQ-0.2, $\overline{WP}$ =0V/VccQ	-	-	TBD	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to VccQ(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to VccQ(max)	-	-	±10	
AC Input High Voltage	V_{IH} (AC)	-	0.8 xVccQ	-	NOTE 5)	V
DC Input High Voltage	V_{IH} (DC)	-	0.7 xVccQ		VccQ +0.3	
AC Input Low Voltage	V_{IL} (AC)	-	NOTE 5)	-	0.2 xVccQ	
DC Input Low Voltage	V_{IL} (DC)	-	-0.3	-	0.3 xVccQ	
Output High Voltage Level	V_{OH}	I_{OH}=-100µA	VccQ-0.1	-	-	
Output Low Voltage Level	V_{OL}	I_{OL}= 100µ A	-	-	0.1	
Output Low Current(R/ $\overline{B}$)	I_{OL}(R/ $\overline{B}$)	V_{OL}=0.2V	3	4	-	mA

NOTE:

1) Typical value is measured at Vcc=3.3V, T_{OPER}=25℃. Not 100% tested.

2) V_{OH} and V_{OL} should be available on these two conditions; Output Strength is nominal and VccQ=1.8V, Rpd/Rpu are all VccQx0.5. If the drive strength settings are supported, Table 12 shall be used to derive the output driver impedance values.

3) Icc1,2 are without data cache.

4) Icc1/2/3, I_{SB} are the value of one chip, and an unselected chip is in Standby mode.

5) Refer to AC Overshoot and Undershoot requirements.

Table 10 DC & Operating Characteristics for SDR VccQ=1.8V and 3.3V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IL}	V_{IN} = 0 V to V_{CC}	—	—	±10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 V to V_{CC}	—	—	±10	
Power On Reset Current	I_{CCO0} *1	$\overline{CE}$ = V_{IL}	—	—	TBD	mA
Read Mode Current	I_{CCO1} *2	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	TBD	
Auto Page Program Current	I_{CCO2} *2	—	—	—	TBD	
Auto Block Erase current	I_{CCO3}	—	—	—	TBD	
Standby Current	I_{CCS}	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC},	—	—	TBD	µA
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	—	0.4	
Output current of RY/$\overline{BY}$ pin	I_{OL} (RY/$\overline{BY}$)	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	8	—	mA

NOTE:

1)*1: Icco0 is the average current during R/B signal="Busy" state.

2)*2: All operation current are without data cache.

2.11. Input/Output Capacitance (T_{OPER} =25°C, f=1MHz)

Table 11 Input/ Output capacitance

SYMBOL	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input	V_{IN}=0V	-	10	pF
C_{OUT}	Output	V_{OUT}=0V	-	10	pF

2.12. DQ Driver Strength

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive, Nominal, Overdrive 1 options. The Toggle DDR1.0 supports all four driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section. A device is only required to meet driver strength values for either 3.3V VccQ or 1.8V VccQ, and is not required to meet driver strength values for both 3.3V VccQ and 1.8V VccQ.

Table 12 DQ Drive Strength Settings

Setting	Driver Strength	VccQ
Overdrive 1	1.4x = 25 Ohms	3.3 V
Nominal	1.0x = 35 Ohms	
Underdrive	0.7x = 50 Ohms	
Overdrive 1	1.4x = 25 Ohms	1.8 V
Nominal	1.0x = 35 Ohms	
Underdrive	0.7x = 50 Ohms	

The impedance values corresponding to several different VccQ values are defined in Table 14 for 3.3V and 1.8V VccQ. The test conditions that shall be used to verify the impedance values are specified in Table 13. The terms T_{OPER}(Min) and T_{OPER}(Max) are in reference to the minimum and maximum operating temperature defined for the device.

Table 13 Testing Conditions for Impedance Values

Condition	Temperature	VccQ (3.3V)	VccQ (1.8V)	Process
Minimum Impedance	TOPER (Min) degrees Celsius	3.6 V	1.95 V	Fast - fast
Nominal Impedance	25 degrees Celsius	3.3 V	1.8 V	Typical
Maximum Impedance	TOPER (Max) degrees Celsius	2.7 V	1.7 V	Slow-slow

Table 14 Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to VssQ	Minimum		Nominal		Maximum		Units
			VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	
Overdrive1	Rpd	VccQ 0.2	8.0	10.5	15.0	19.0	30.0	44.0	ohms
		VccQ 0.5	15.0	13.0	25.0	25.0	45.0	47.0	ohms
		VccQ 0.8	20.0	16.0	35.0	32.5	65.0	61.5	ohms
	Rpu	VccQ 0.2	20.0	16.0	35.0	32.5	65.0	61.5	ohms
		VccQ 0.5	15.0	13.0	25.0	25.0	45.0	47.0	ohms
		VccQ 0.8	8.0	10.5	15.0	19.0	30.0	44.0	ohms
Nominal	Rpd	VccQ 0.2	12.0	15.0	22.0	27.0	40.0	62.5	ohms
		VccQ 0.5	20.0	18.0	35.0	35.0	65.0	66.5	ohms
		VccQ 0.8	25.0	22.0	50.0	52.0	100.0	88.0	ohms
	Rpu	VccQ 0.2	25.0	22.0	50.0	52.0	100.0	88.0	ohms
		VccQ 0.5	20.0	18.0	35.0	35.0	65.0	66.5	ohms
		VccQ 0.8	12.0	15.0	22.0	27.0	40.0	62.5	ohms
Underdrive	Rpd	VccQ 0.2	18.0	21.5	32.0	39.0	55.0	90.0	ohms
		VccQ 0.5	29.0	26.0	50.0	50.0	100.0	95.0	ohms
		VccQ 0.8	40.0	31.5	75.0	66.5	150.0	126.5	ohms
	Rpu	VccQ 0.2	40.0	31.5	75.0	66.5	150.0	126.5	ohms
		VccQ 0.5	29.0	26.0	50.0	50.0	100.0	95.0	ohms
		VccQ 0.8	18.0	21.5	32.0	39.0	55.0	90.0	ohms

Table 15 Pull-up and Pull-down Output Impedance Mismatch

Drive Strength	Minimum	Maximum	Unit
Overdrive 1	0.0	8.8	ohms
Nominal	0.0	12.3	ohms
Underdrive	0.0	17.5	ohms

NOTE:

1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.

2) Test conditions: VccQ = VccQ(min), Vout = VccQ×0.5

2.13. Input/Output Slew rate

The input slew rate requirements that the device shall comply with are defined in, Table 16, and Table 17. The output slew rate requirements that the device shall comply with are defined in Table 19. The testing conditions that shall be used to verify the input slew rate and output slew rate are listed in Table 18 and Table 20 respectively.

Table 16 Derating factor

Input slew rate	Up to 100MHz		Unit
	3.3Vccq	1.8Vccq	
1.0V/ns	0	0	ps
0.8V/ns	332	180	
0.6V/ns	884	482	

NOTE:

1) Derating factor listed in this table shall be applied to data setup time (tDS) and data hold time (tDH) as additional value if the slew rate is less than the minimum value defined in Table 17.

Table 17 Input Slew Rate

Vccq	Minimum slew rate
	Up to 100MHz
3.3V	1.0V/ns
1.8V	1.0V/ns

Table 18 Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	VIL (DC) to VIH (AC)
Negative Input Transition	VIH (DC) to VIL (AC)

Table 19 Output Slew Rate Requirements

Parameter	VccQ=3.3V		VccQ=1.8V		Unit
	Minimum	Maximum	Minimum	Maximum	
Overdrive 1	1.5	9.0	0.85	5.0	V/ns
Nominal	1.2	7.0	0.75	4.0	V/ns
Underdrive	1.0	5.5	0.60	4.0	V/ns

NOTE :

1) Measured with a test load of 5pF connected to VssQ.
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Table 20 Testing Conditions for Output Slew Rate

Parameter	Value
V_{OL} (DC)	0.3 * VccQ
V_{OH} (DC)	0.7 * VccQ
V_{OL} (AC)	0.2 * VccQ
V_{OH} (AC)	0.8 * VccQ
Positive Output Transition	V_{OL} (DC) to V_{OH} (AC)
Negative Output Transition	V_{OH} (DC) to V_{OL} (AC)
t_{RISE}(1)	Time during Rising Edge from V_{OL} (DC) to V_{OH} (AC)
t_{FALL}(1)	Time during Falling Edge from V_{OH} (DC) to V_{OL} (AC)
Output Slew Rate Rising Edge	(V_{OH} (AC) - V_{OL} (DC)) / t_{RISE}
Output Slew Rate Falling Edge	(V_{OH} (DC) - V_{OL} (AC)) / t_{FALL}
Output Capacitive load	50 Ohms to Vtt (Vtt=0.5*VCCQ)

NOTE :

1) Refer to Figure 3.
2) Output slew rate is verified by design and characterization. It may not be subject to production test.
3) The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.

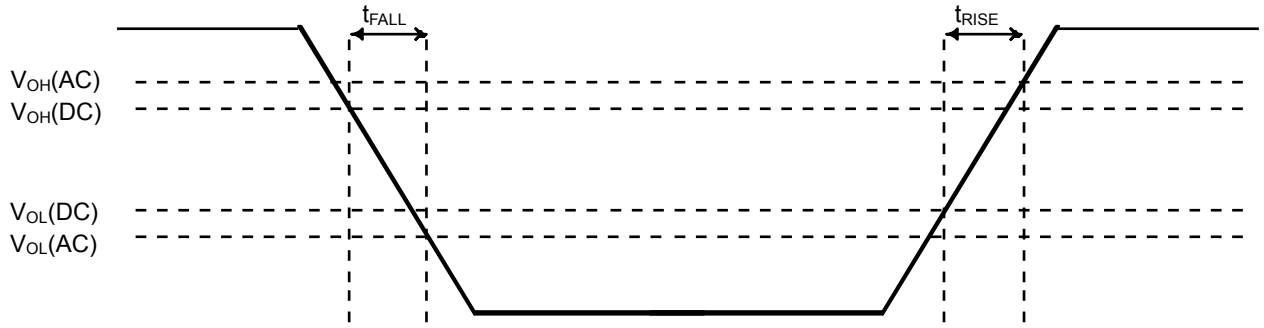


Figure 3. t_{RISE} and t_{FALL} Definition for Output Slew Rate

2.14. R/$\overline{B}$ and SR[6] Relationship

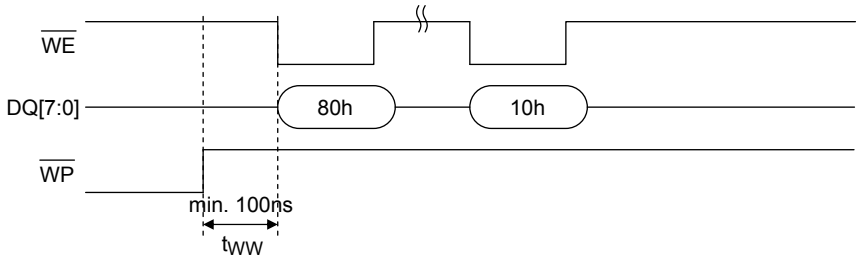
R/$\overline{B}$ represents the status of the selected target. R/$\overline{B}$ goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

2.15. Write Protect

When $\overline{WP}$ is enabled, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once $\overline{WP}$ is enabled.

Figure 4 describes the tWW timing requirement, shown with the start of a Program command. And Figure 5 shows with the start of a Erase command.

1. Enable Mode



2. Disable Mode

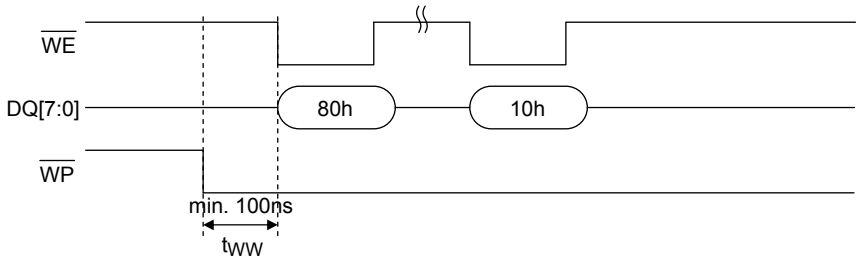
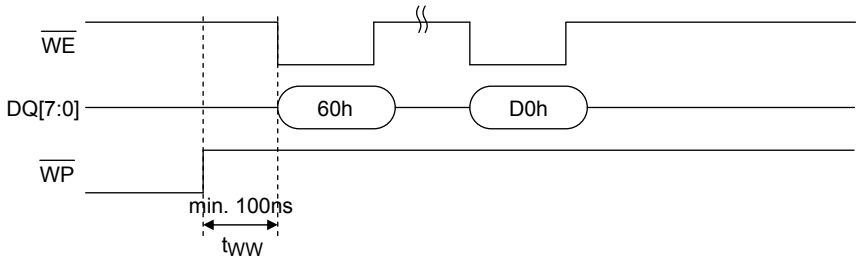


Figure 4. Write Protect timing requirements of the Program operation

1. Enable Mode



2. Disable Mode

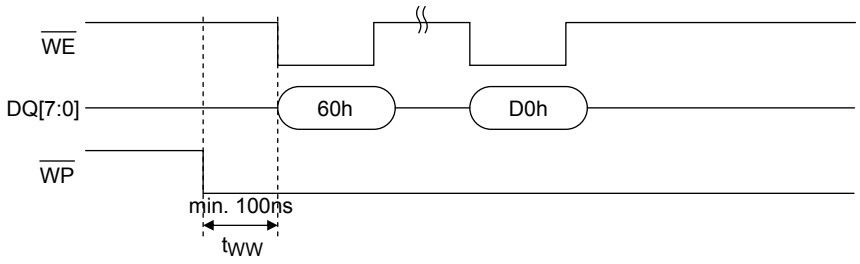


Figure 5. Write Protect timing requirements of the Erase operation

3. MEMORY ORGANIZATION

A device contains one or more targets. A target is controlled by one $\overline{CE}$ signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1.

A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of plane operations supported for the LUN. The Flash array contains a number of blocks.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations. For targets that support partial page programming with constraints, the smallest addressable unit for program operations is a partial page. A page consists of a number of bytes.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

There are several mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time.

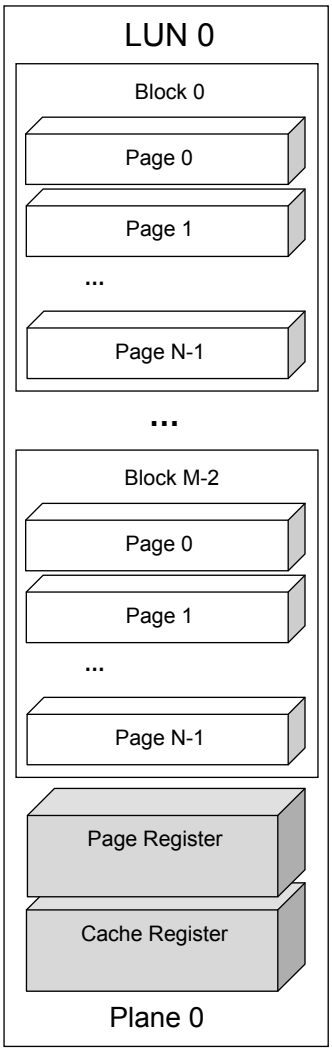


Figure 6. Target Organization

3.1. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs. When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses are not issued. For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero. The row address structure is shown in Figure 7 with the least significant row address bit to the right and the most significant row address bit to the left.

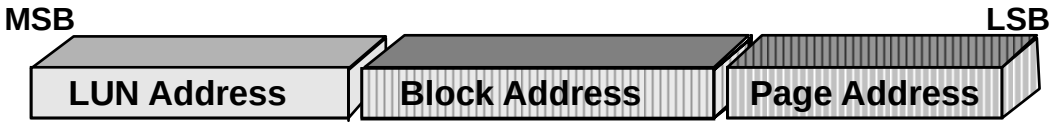


Figure 7. Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address. A host shall not access an address of a page or block beyond maximum page address or block address. The addressing of this device is shown in Table 21.

Table 21 The addressing of this device.

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First cycle (Column address 1)	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
Second cycle (Column address 2)	L	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
Third cycle (Row address 1)	R1-7	R1-6	R1-5	R1-4	R1-3	R1-2	R1-1	R1-0
Fourth cycle (Row address 2)	R2-7	R2-6	R2-5	R2-4	R2-3	R2-2	R2-1	R2-0
Fifth cycle (Row address 3)	L	L	L	L	L	R3-2	R3-1	R3-0

R1-0 to R1-7: Page address

R2-0 to R3-2: Block address

NOTE :

1) The least significant bit of Block address is also regarded as Plane Address bit. Refer to 3.1.1.

2) If the target of the device has only one LUN, no LUN Address bit is assigned.

3.1.1. Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in Figure 8.

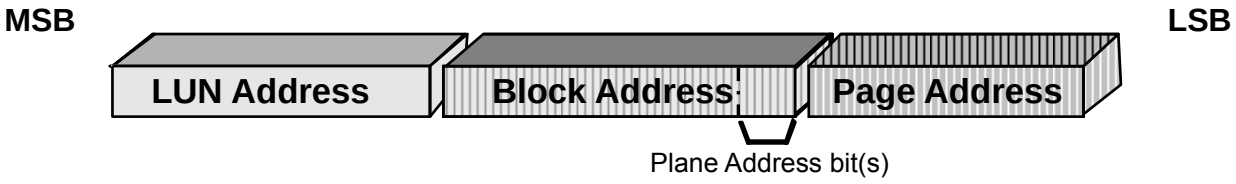


Figure 8. Position of Plane Address

3.1.2. Extended Blocks Arrangement

The device has 36 extended blocks per plane (Extended Blocks) to increase valid blocks. Extended Blocks can be accessed by the following addressing.

Table 22 Extended Blocks Arrangement

Row Address	Block Assignment	
000000h	Block 0(Plane 0)	LUN #0 Main Blocks (1024 blocks)
000100h	Block 1(Plane 0)	
000200h	Block 2(Plane 0)	
000300h	Block 3(Plane 0)	
000400h	Block 4(Plane 0)	
000050h	Block 5(Plane 0)	
|	|	
03FE00h	Block 1022(Plane 0)	
03FF00h	Block 1023(Plane 0)	
040000h	Block 1024(Plane 0)	LUN #0 Extended Blocks (36 blcoks)
040100h	Block 1025(Plane 0)	
|	|	
042200h	Block 1058(Plane 0)	
042300h	Block 1059(Plane 0)	
042400h – FFFFFFh	**Address Gap**	

NOTE：

1) エラー! 参照元が見つかりません。 is only for the device having multiple LUNs per a target and shall be ignored for the device having single LUN per a target.

3.2. Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

3.2.1. Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure 9, of the first or last page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

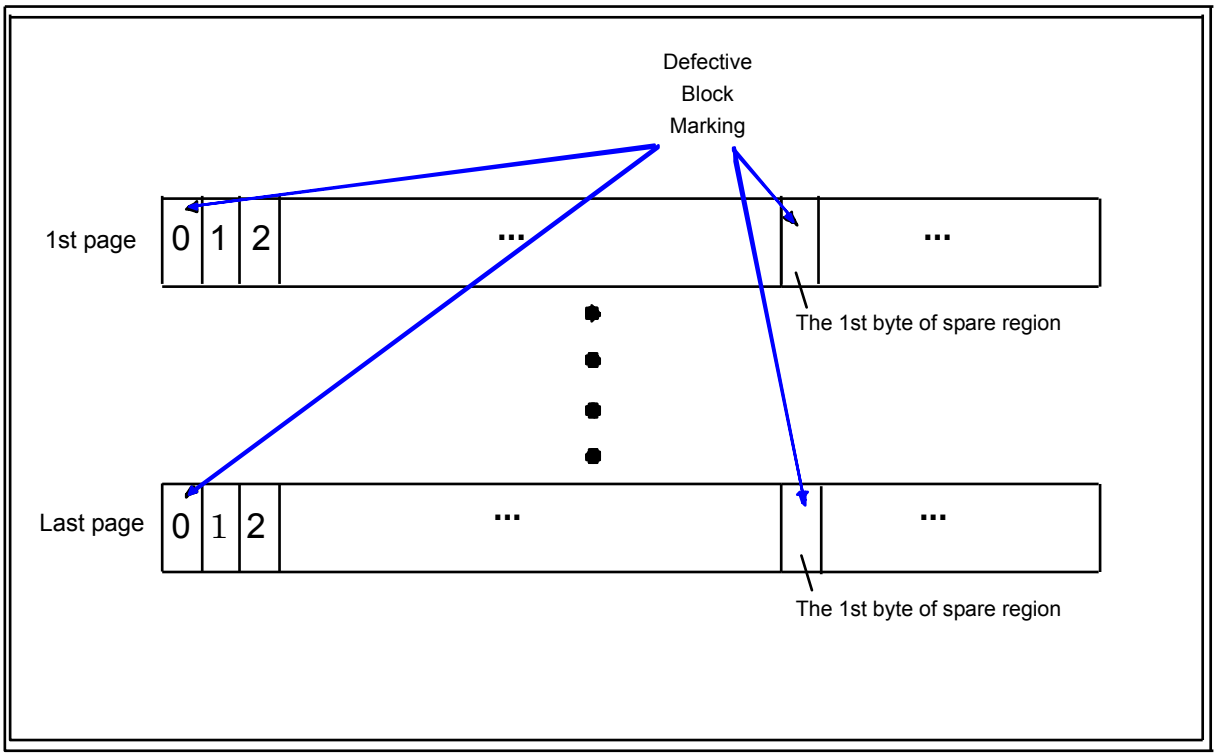


Figure 9. Area marked in first or last page of block indicating defect

3.2.2. Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 10 outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. All pages in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or last page of the block. The host shall check the Defective Block Marking location of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE :
Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

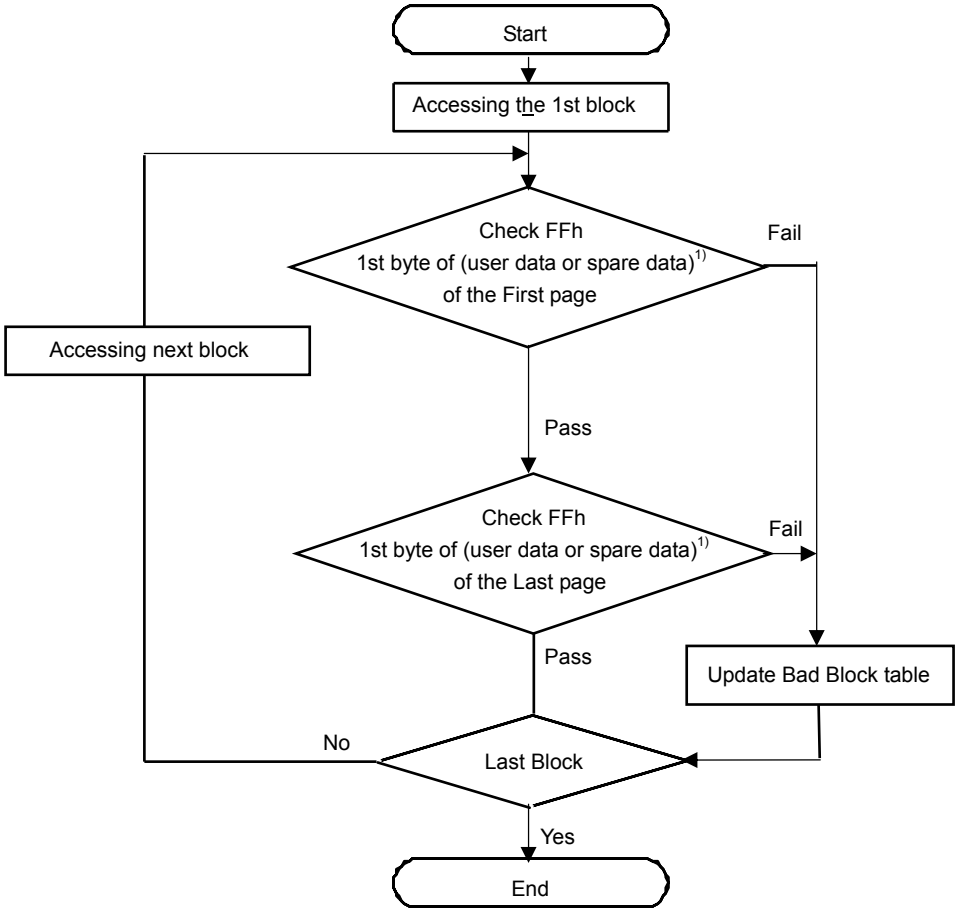


Figure 10. Flow chart to create initial invalid block table

NOTE :
1) The location for the initial invalid block may vary depending on vendors

4. FUNCTION DESCRIPTION

4.1. Discovery and Initialization

Toggle DDR1.0 NAND is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. The Reset command (FFh) must be issued to all $\overline{CE}$s as the first command after the NAND Flash device is powered on. Each $\overline{CE}$ will be busy for 5ms at the maximum after the Reset command is issued. During busy time of resetting, the acceptable command is the Read Status (70h).

WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. The two step command sequence for pro-gram/erase provides additional software protection. Figure 11 defines the Initialization behavior and timings.

4.1.1. Single Channel Discovery

Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command (FFh) to the target. Following the reset, the host should then issue the Read ID command to the target. If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected. If the ID values are not returned or any error is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done.

4.1.2. Dual Channel Discovery

If there are dual channel in a package, host should issues the Reset command (FFh) to both channels to initialize all LUNs. Note that the relationships are described between several $\overline{CE}$ and dual channels. See the Table 2 for further information.

The sequence of initialization is the same as the sequence for single channel discovery. Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command (FFh) to the target. Following the reset, the host should then issue a Read ID command to the target. If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected. If the ID values are not returned or any error is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done.

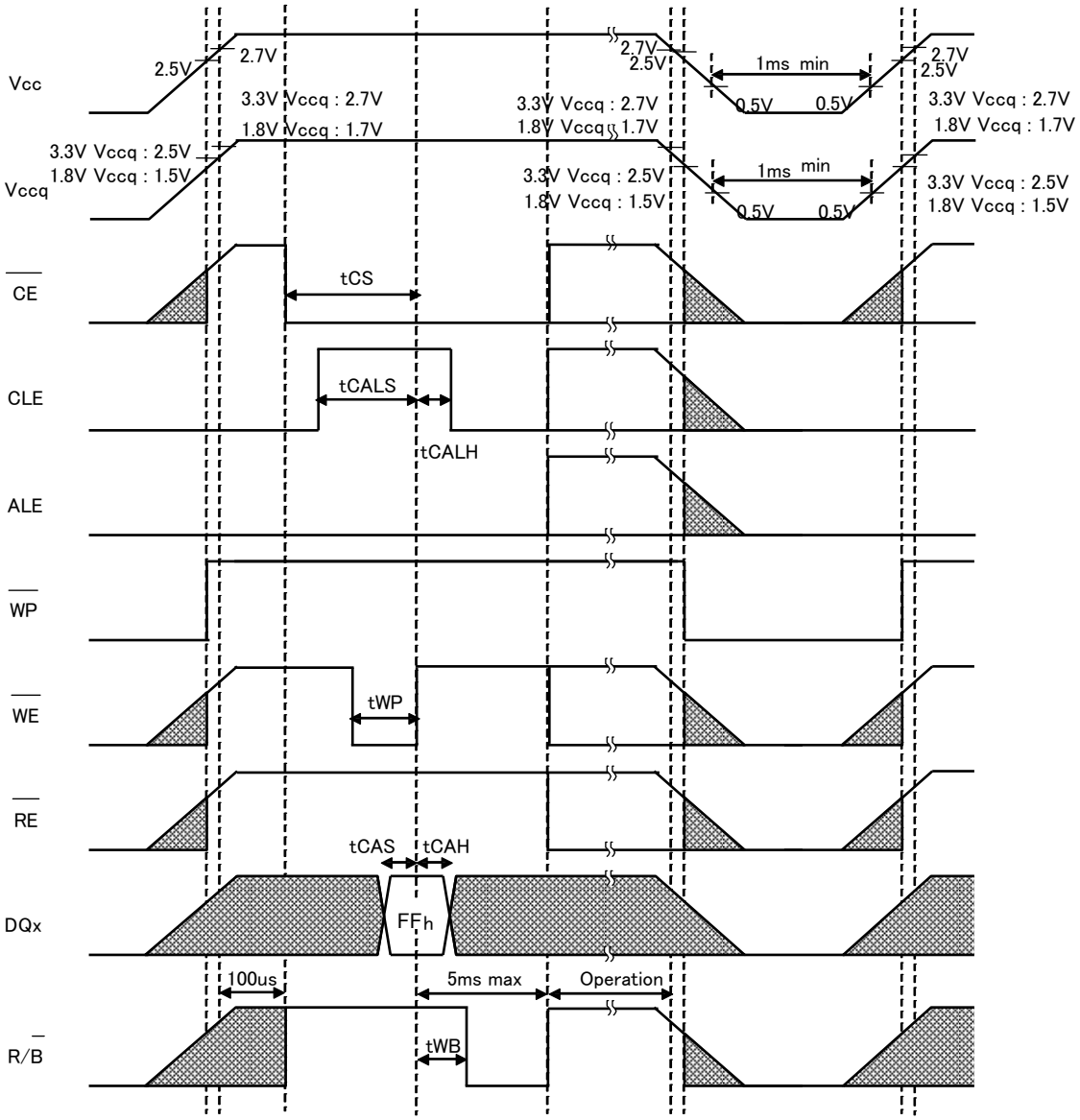


Figure 11. Initialization Timing

NOTE:

1) During the initialization, the device consumes a maximum current of I_{CC1}.

4.2. Mode Selection

After initialization, the SDR interface is active for all targets on the device. Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target. The interface can be changed by Set Feature Command defined in section 5.2.8.

Table 23 describes the bus state for the Toggle DDR1.0. Command, address and data are all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ pins. Host reads or writes data to the device using DQS signal. And data are latched on both falling and rising edges of DQS on data input.

Table 23 Toggle DDR1.0 Interface Mode Selection

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$
Command Input	H	L	L	⌐└⌐	H	X(1)	X
Address Input	L	H	L	⌐└⌐	H	X	X
Command Input	H	L	L	⌐└⌐	H	X	H
Address Input	L	H	L	⌐└⌐	H	X	H
Data Input	L	L	L	H	H	⌐└⌐	H
Data Output	L	L	L	H	⌐└⌐	⌐└⌐	X
During Read(Busy)	X	X	X	X	H	X	X
During Program(Busy)	X	X	X	X	X	X	H
During Erase(Busy)	X	X	X	X	X	X	H
Write Protect	X	X	X	X	X	X	L
Stand-by	X	X	H	X	X	X	0V/Vcc(2)

NOTE:

1) X can be VIL or VIH.

2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Table 24 describes the bus state for the SDR interface. Command, address and data are all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ pins. Host reads the data to the device using $\overline{RE}$ signal and writes the data to the device using $\overline{WE}$ signal.

Table 24 SDR Interface Mode Selection

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⌐└⌐	H	*
Data Input	L	L	L	⌐└⌐	H	H
Address input	L	H	L	⌐└⌐	H	*
Serial Data Output	L	L	L	H	⌐└⌐	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Stand-by	*	*	H	*	*	0 V/V_{CC}

NOTE:

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

4.2.1. Toggle DDR1.0 General Timing

4.2.1.1. Command Latch Cycle

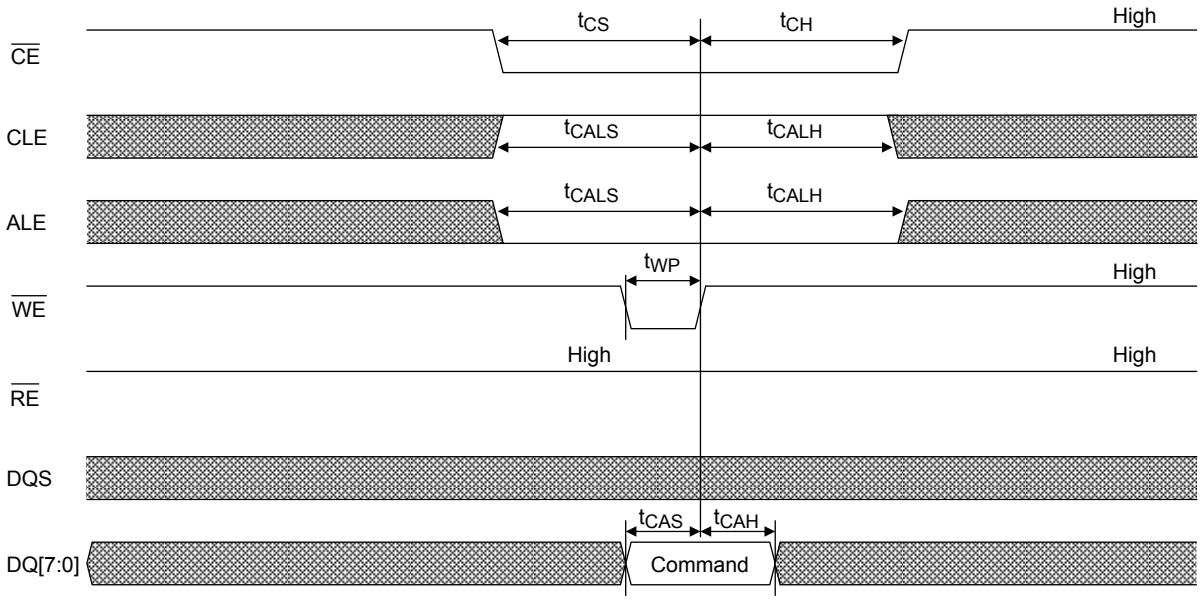


Figure 12. Command Latch Cycle Timing

NOTE :

1) Command Information is latched by $\overline{WE}$ going 'High', when $\overline{CE}$ is 'Low', CLE is 'High', and ALE is 'Low'.
2) DQS shall be set to Low when these commands (85h, 10h, 11h, or 15h) are input.

4.2.1.2. Address Latch Cycle

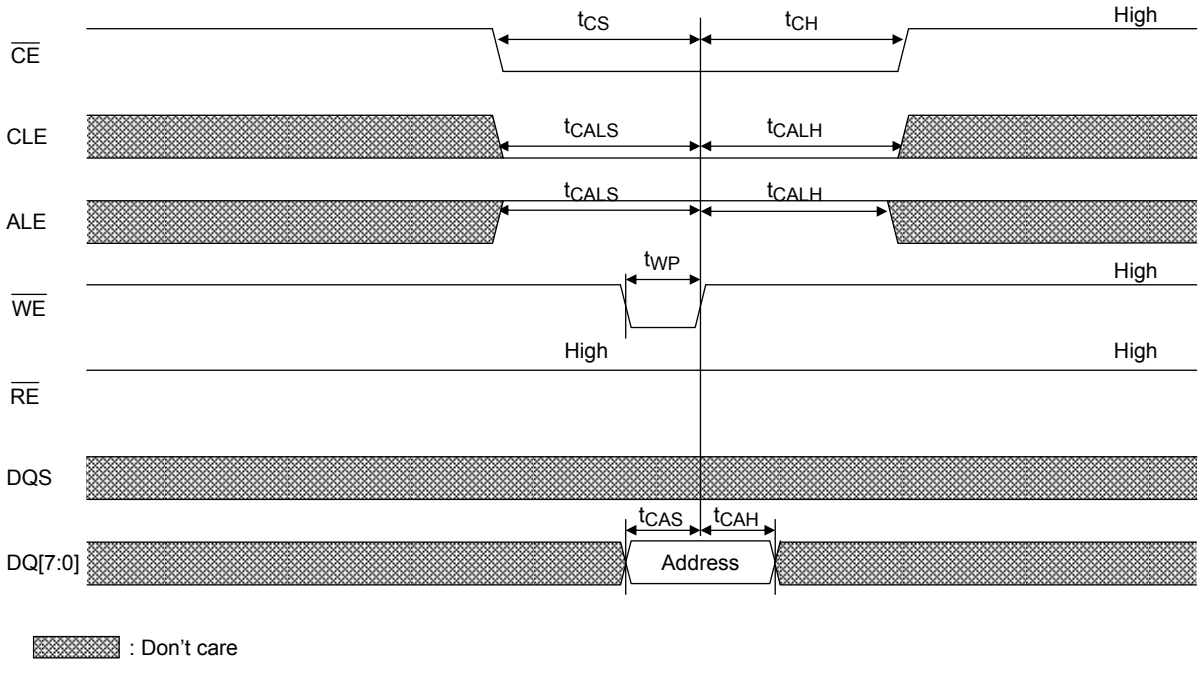


Figure 13. Address Latch Cycle Timing

NOTE :

1) Address Information is latched by $\overline{WE}$ going 'High', when $\overline{CE}$ is 'Low', CLE is 'Low', and ALE is 'High'.

4.2.1.3. Basic Data Input Timing

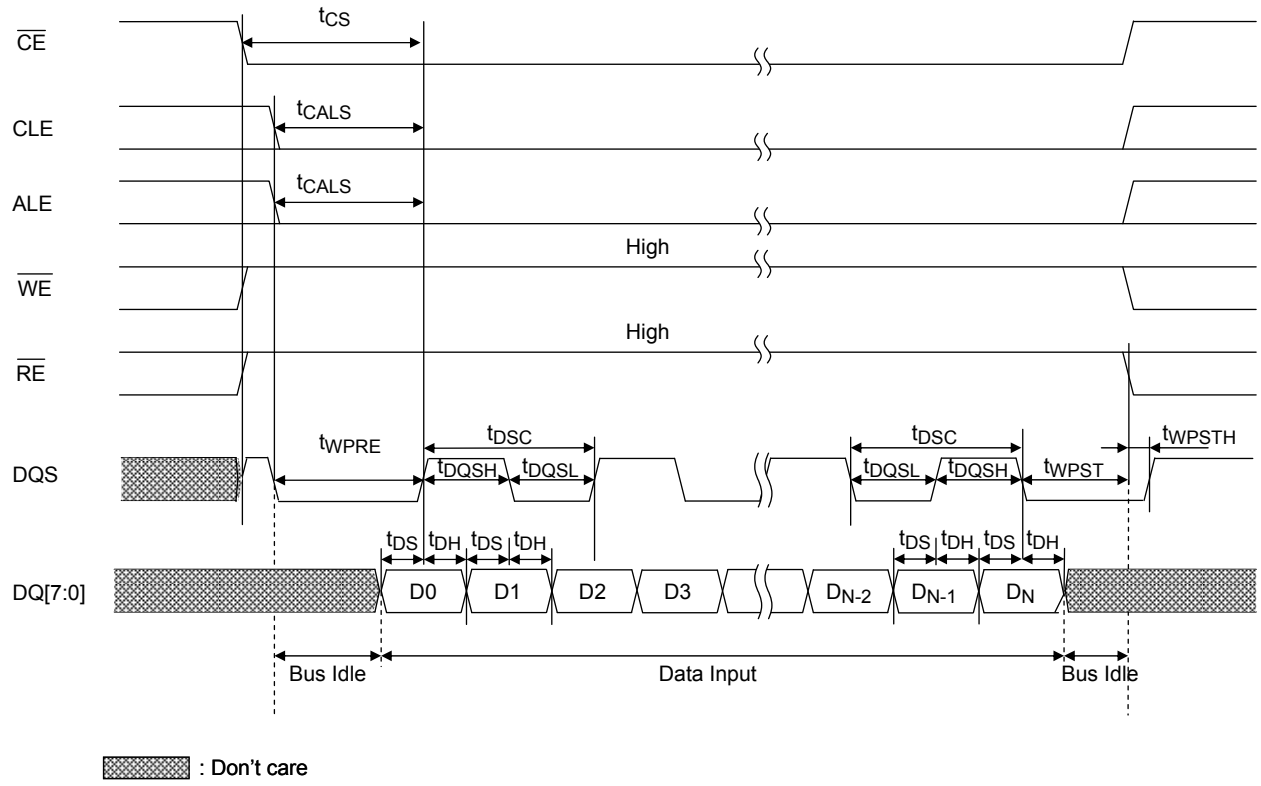


Figure 14. Basic Data Input Timing

NOTE:

1) DQS, and Data input buffers are turned-on when $\overline{CE}$ and DQS goes 'Low' and Data inputs begin with DQS, toggling simultaneously.
2) ALE and CLE should not toggle during t_{WPRE} period regardless of t_{CALS}.
3) DQS and Data input buffers are turned-off if either CLE or $\overline{CE}$ goes 'High'.
4) The least significant bit of the column address shall always be zero.
5) DQS, shall be either high or low before data-input condition is set.

4.2.1.4. Basic Data Output Timing

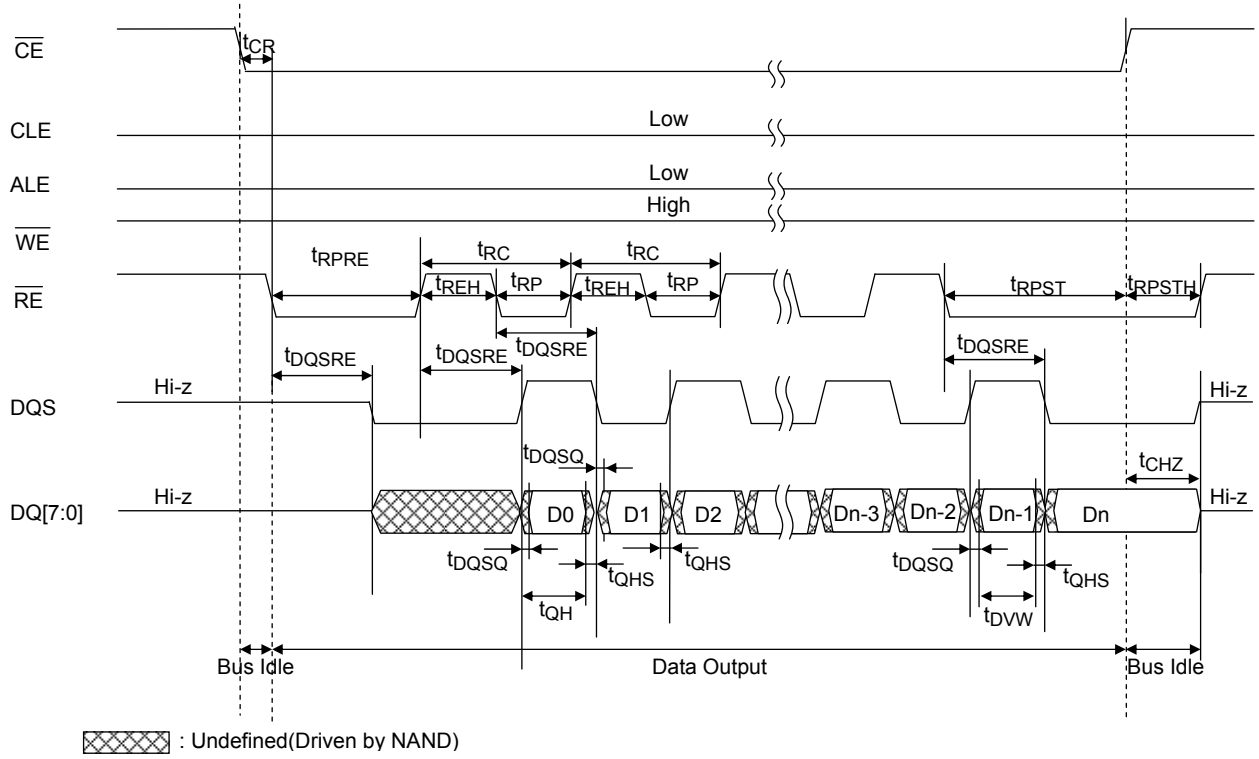


Figure 15. Basic Data Output Timing

NOTE:

1) DQS, and DQ drivers are turned-on when $\overline{CE}$ and $\overline{RE}$ goes Low for data out operation.
2) ALE and CLE should not toggle during t_{RPRE} period regardless of t_{CALS}.
3) DQS and DQ drivers turn from valid to high-z if either CLE or $\overline{CE}$ goes high.
4) The least significant bit of the column address shall always be zero.

4.2.1.5. Read ID Operation

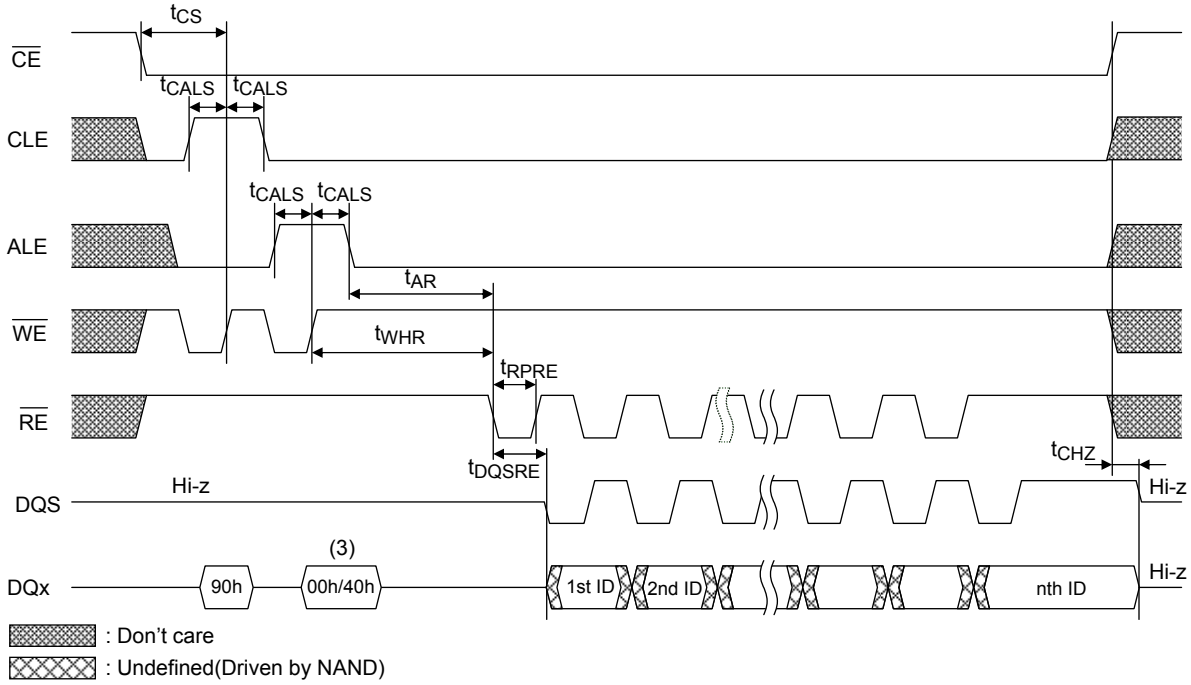


Figure 16. Read ID Operation Timing

NOTE:

1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, READ ID operation repeats each data byte twice, so that READ ID timing becomes identical to that conventional NAND
2) DQS and DQ drivers turn from valid to high-z when $\overline{CE}$ or CLE goes high.
3) Address 00h is for Toshiba conventional NAND and 40h is for new JEDEC ID information.

4.2.1.6. Status Read Cycle

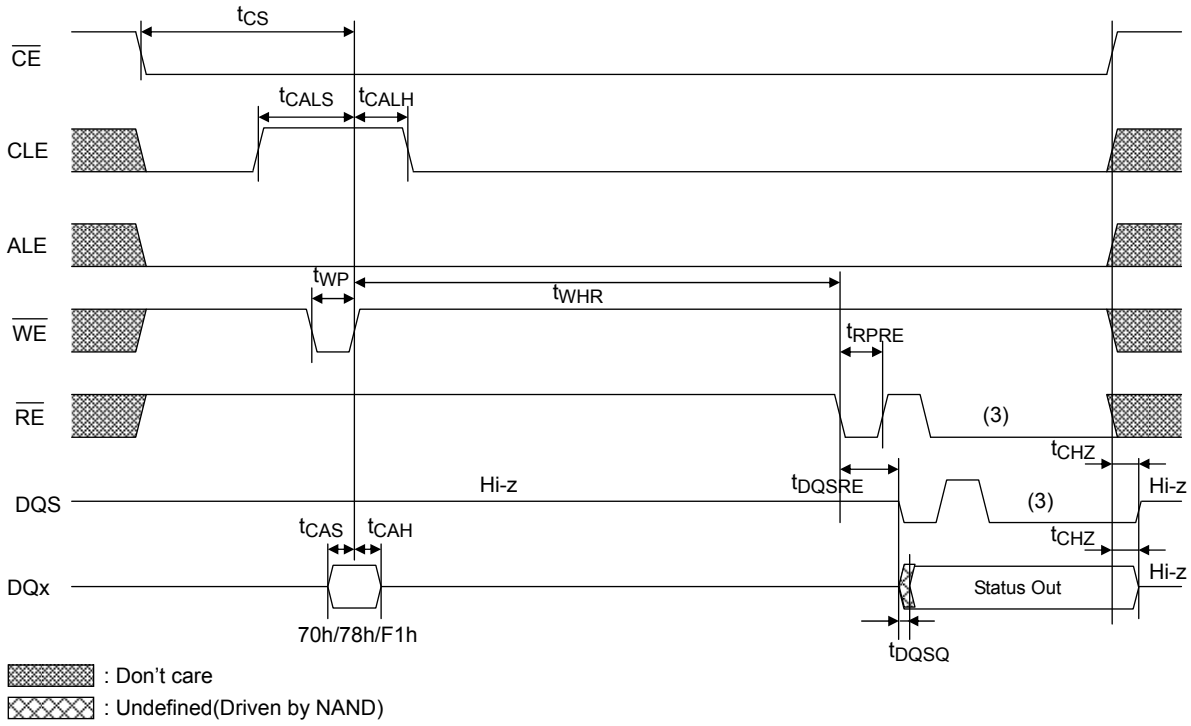


Figure 17. Status Read Cycle Timing

NOTE:

1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, Status read operation repeats same output until device status changes
2) DQS and Data out buffers turn from valid value to high-z when $\overline{CE}$ or $\overline{CLE}$ goes high.
3) $\overline{RE}$ can toggle more than once.
4) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.

4.2.1.7. Set Feature

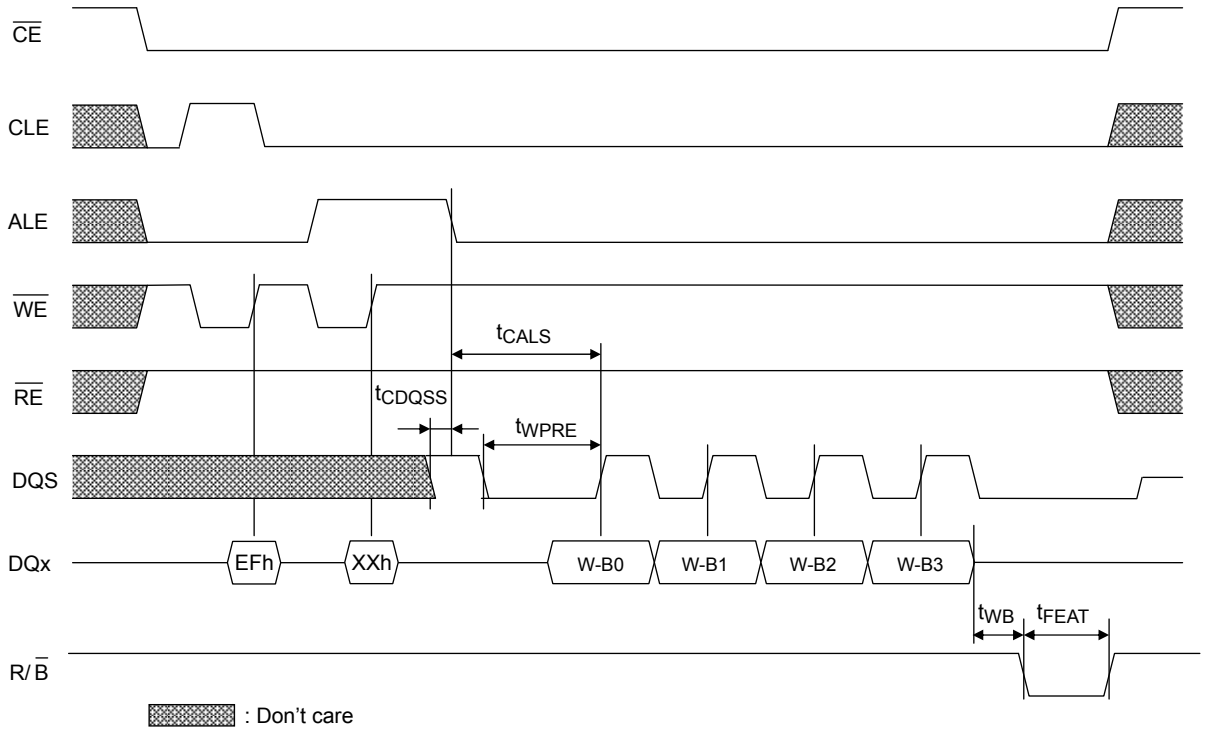


Figure 18. Set Feature Timing

4.2.1.8. Get Feature

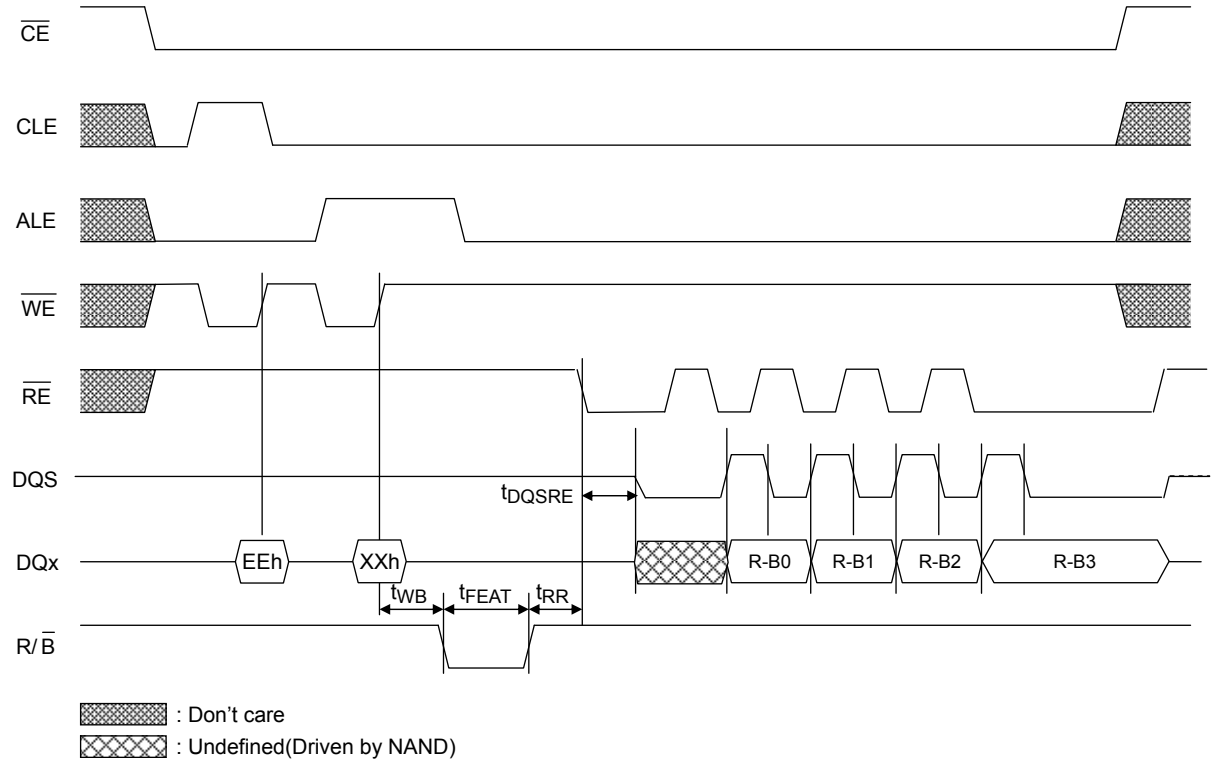


Figure 19. Get Feature Timing

4.2.1.9. Page Read Operation

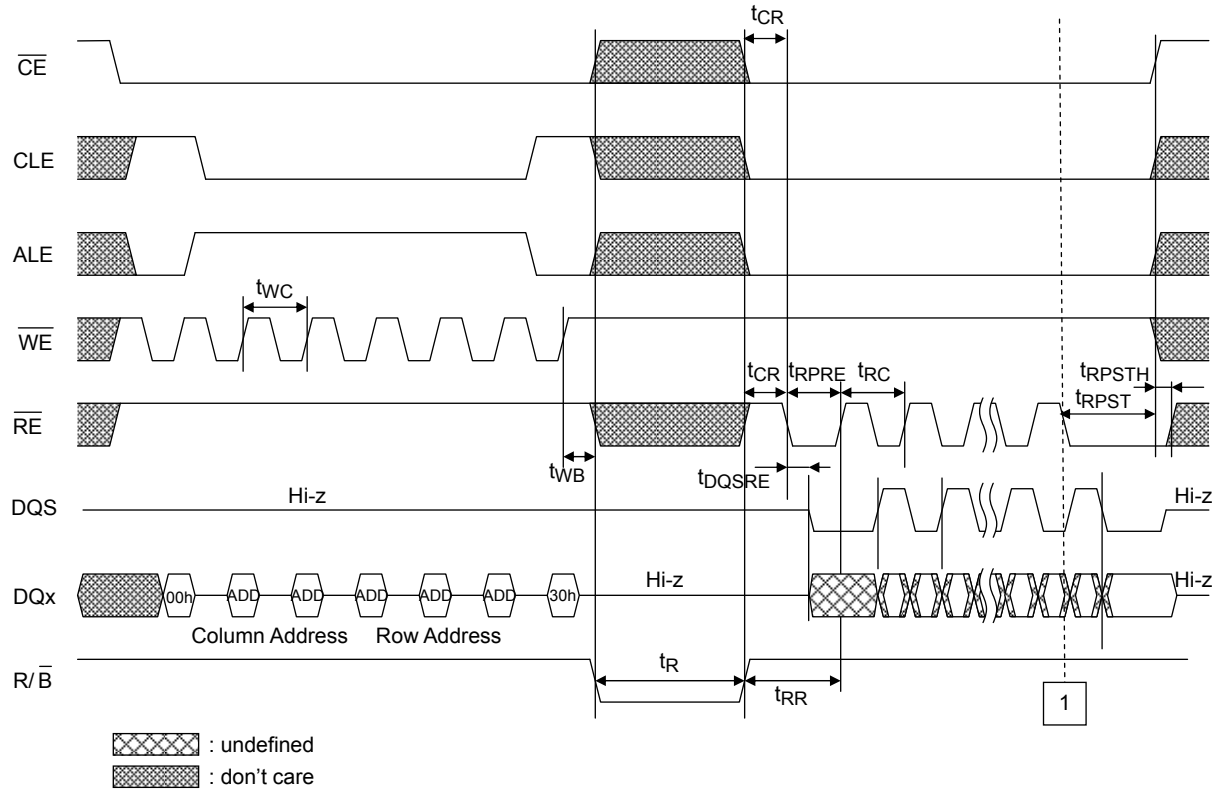


Figure 20. Page Read Operation Timing

Read Hold Operation with $\overline{CE}$ High is below

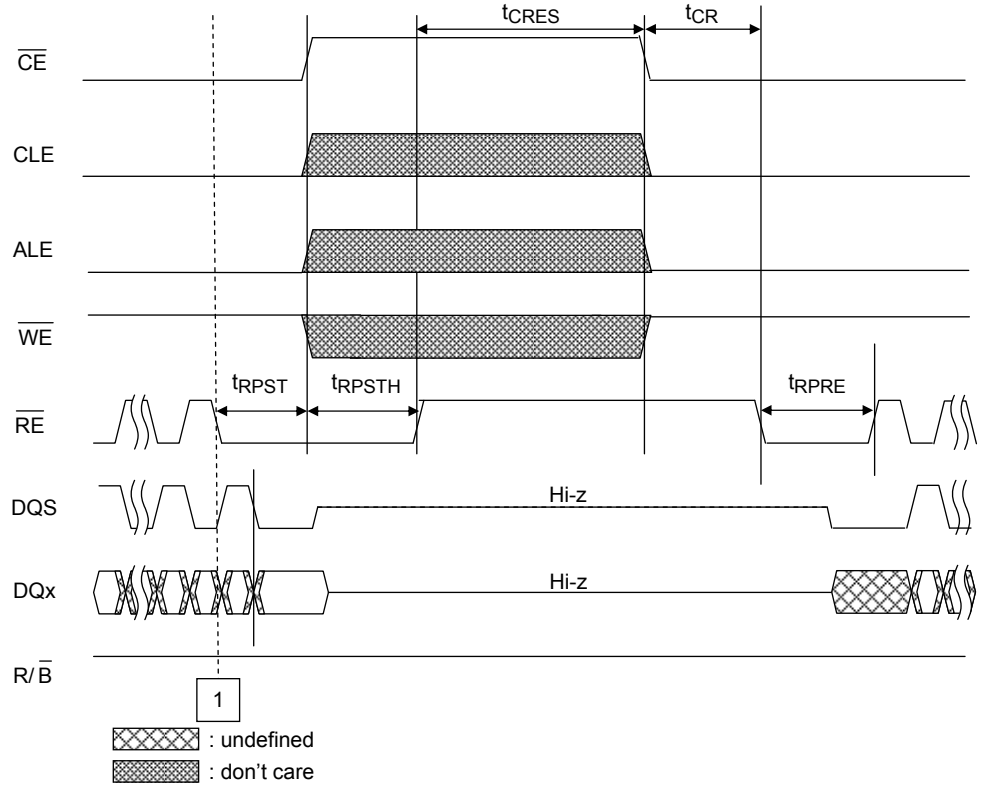


Figure 21. Read Hold Operation with $\overline{CE}$ high

4.2.1.10. Page Program Operation

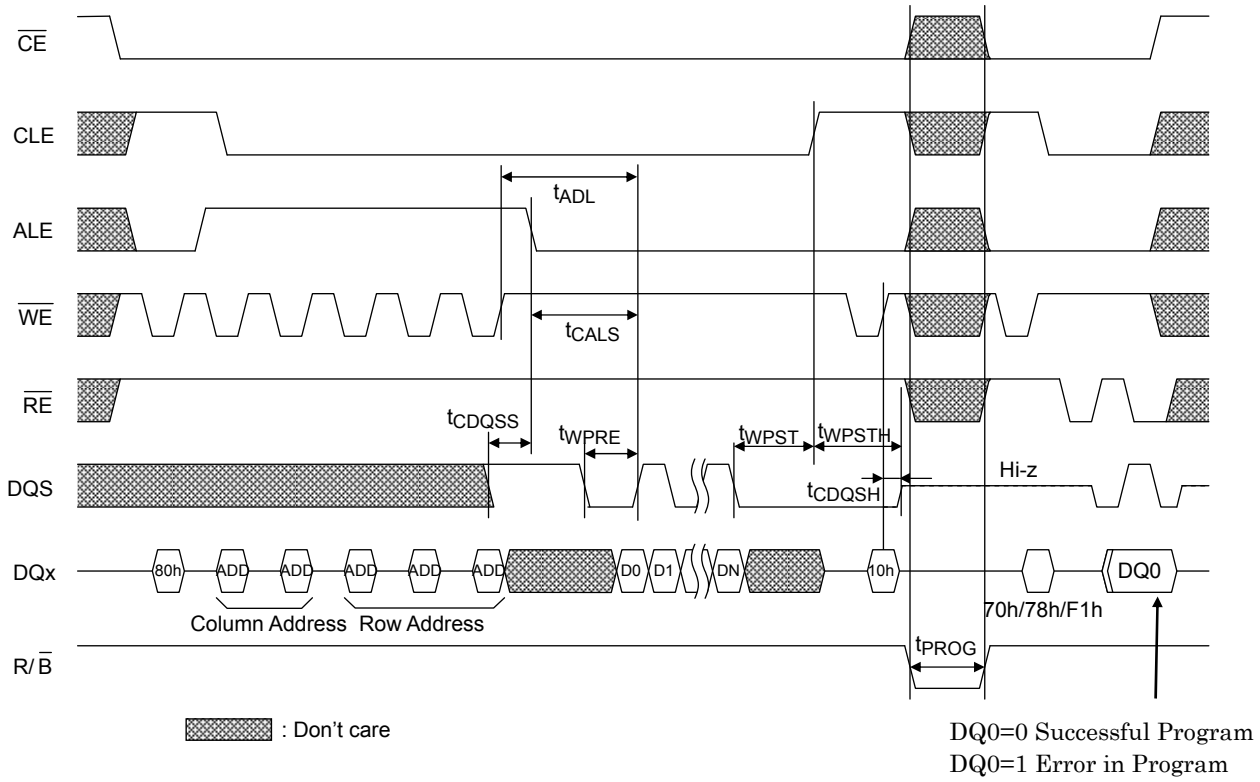


Figure 22. Page Program Operation Timing

NOTE:

1) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.

4.2.2. SDR General Timing

4.2.2.1. Command Latch Cycle

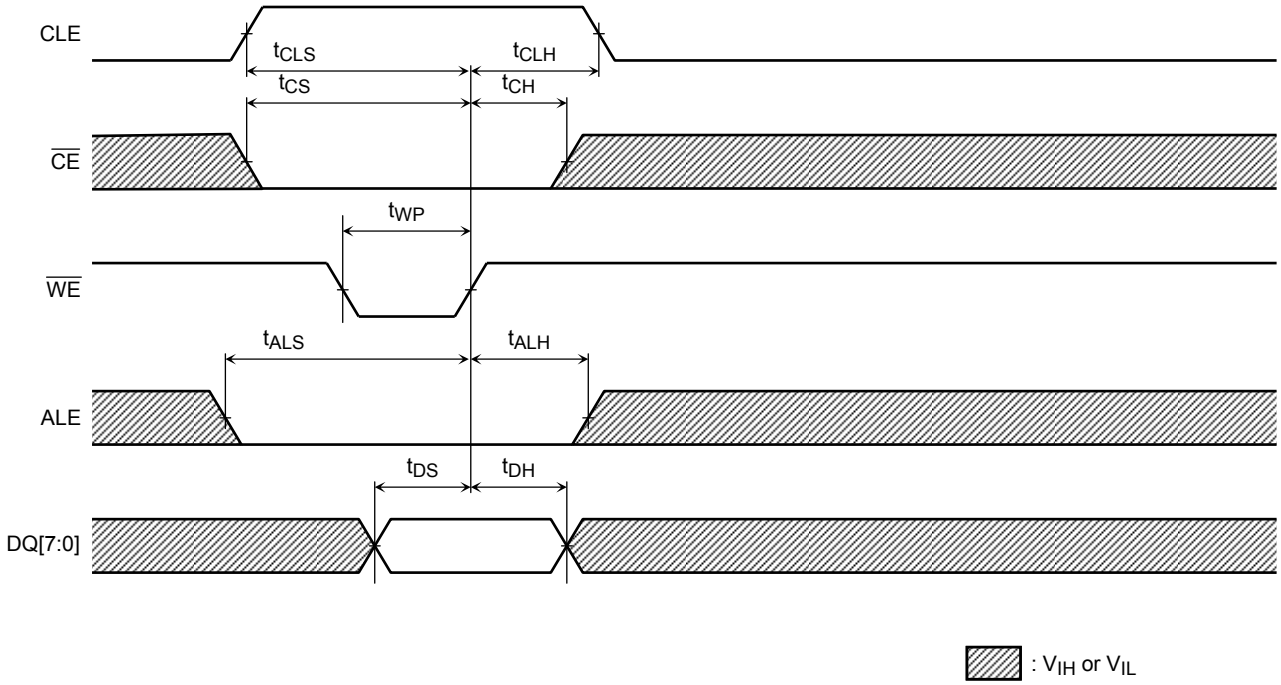


Figure 23. Command Latch Cycle Timing

4.2.2.2. Address Latch Cycle

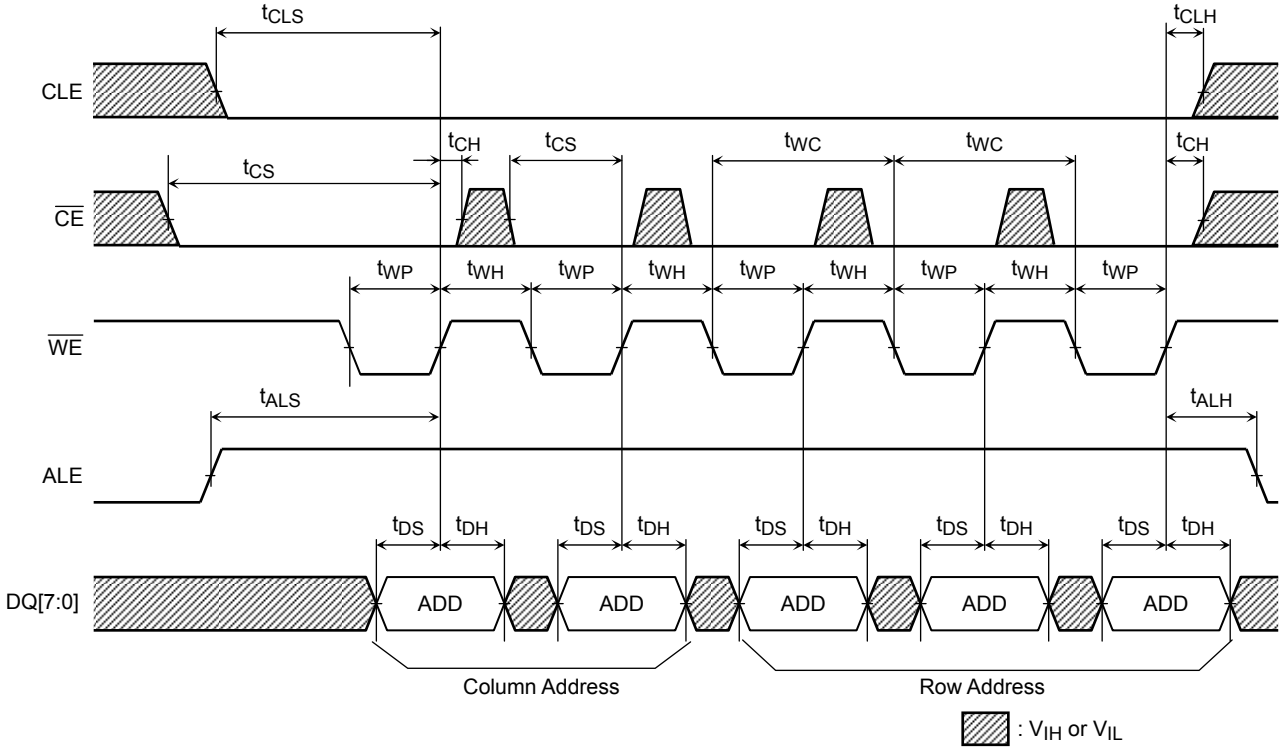


Figure 24. Address Latch Cycle Timing

4.2.2.3. Basic Data Input Timing

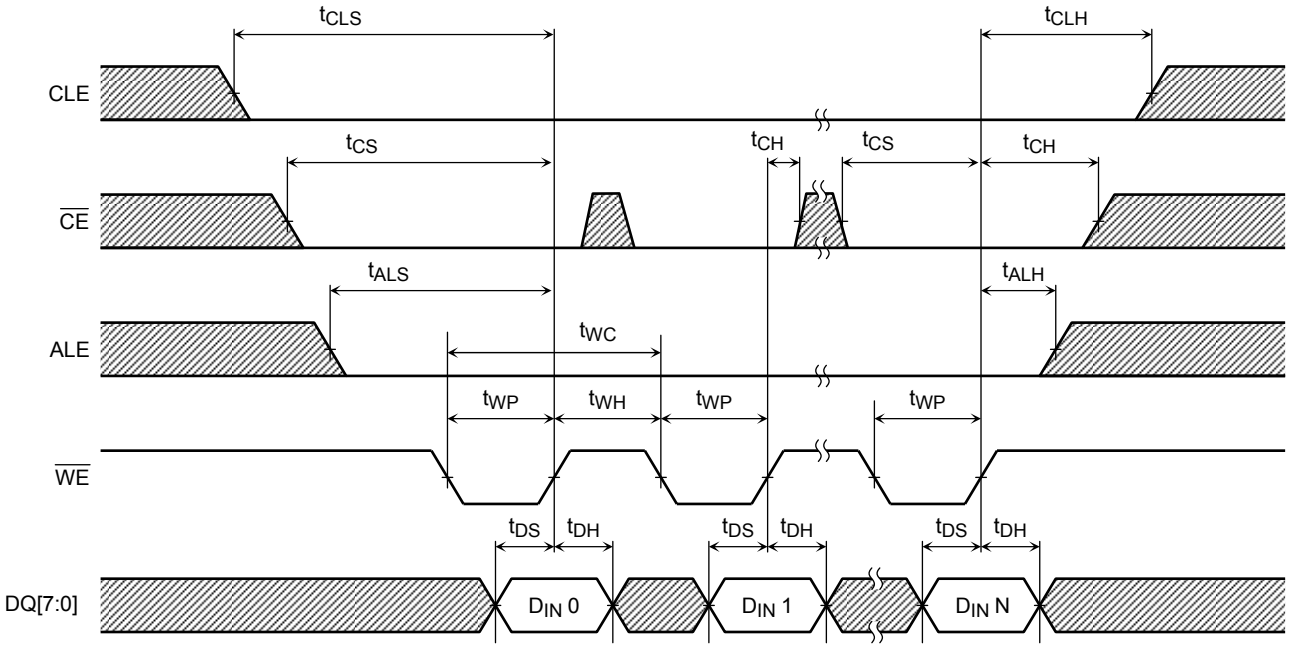


Figure 25. Basic Data Input Timing

4.2.2.4. Basic Data Output Timing

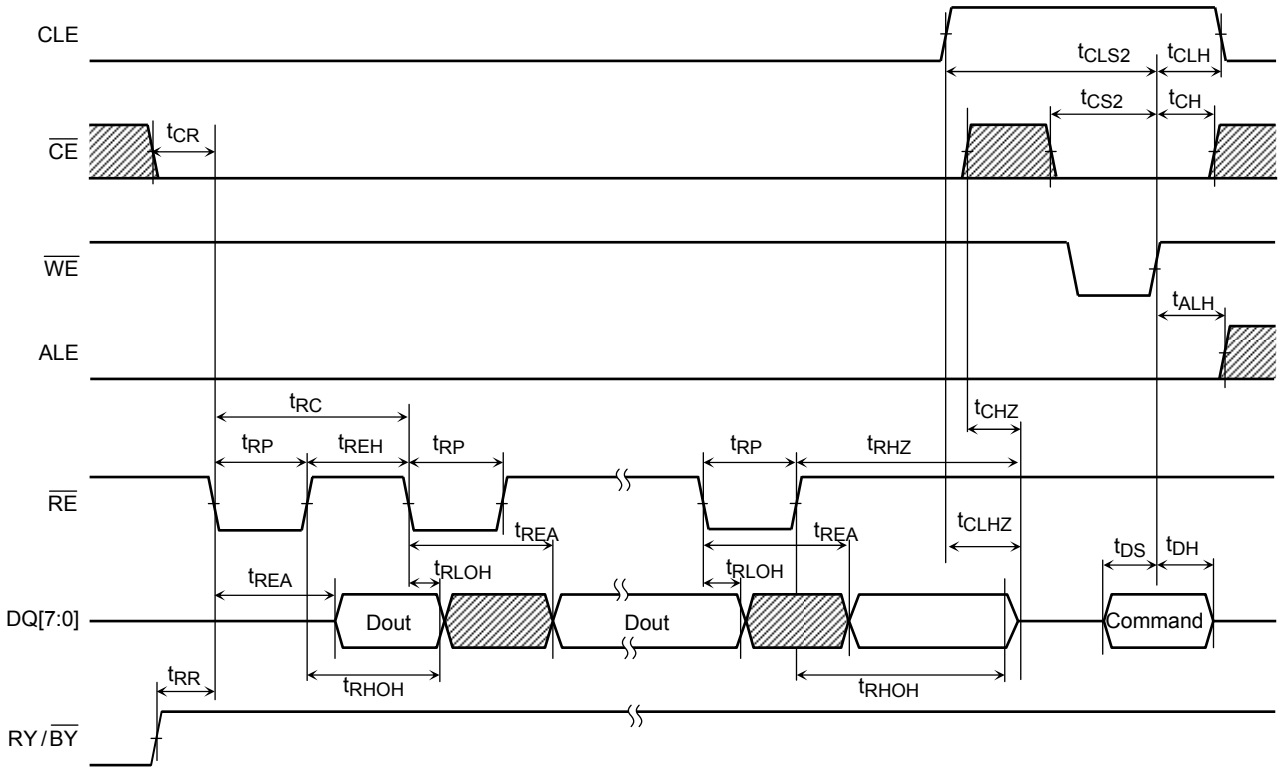


Figure 26. Basic Data Output Timing

4.2.2.5. Read ID Operation

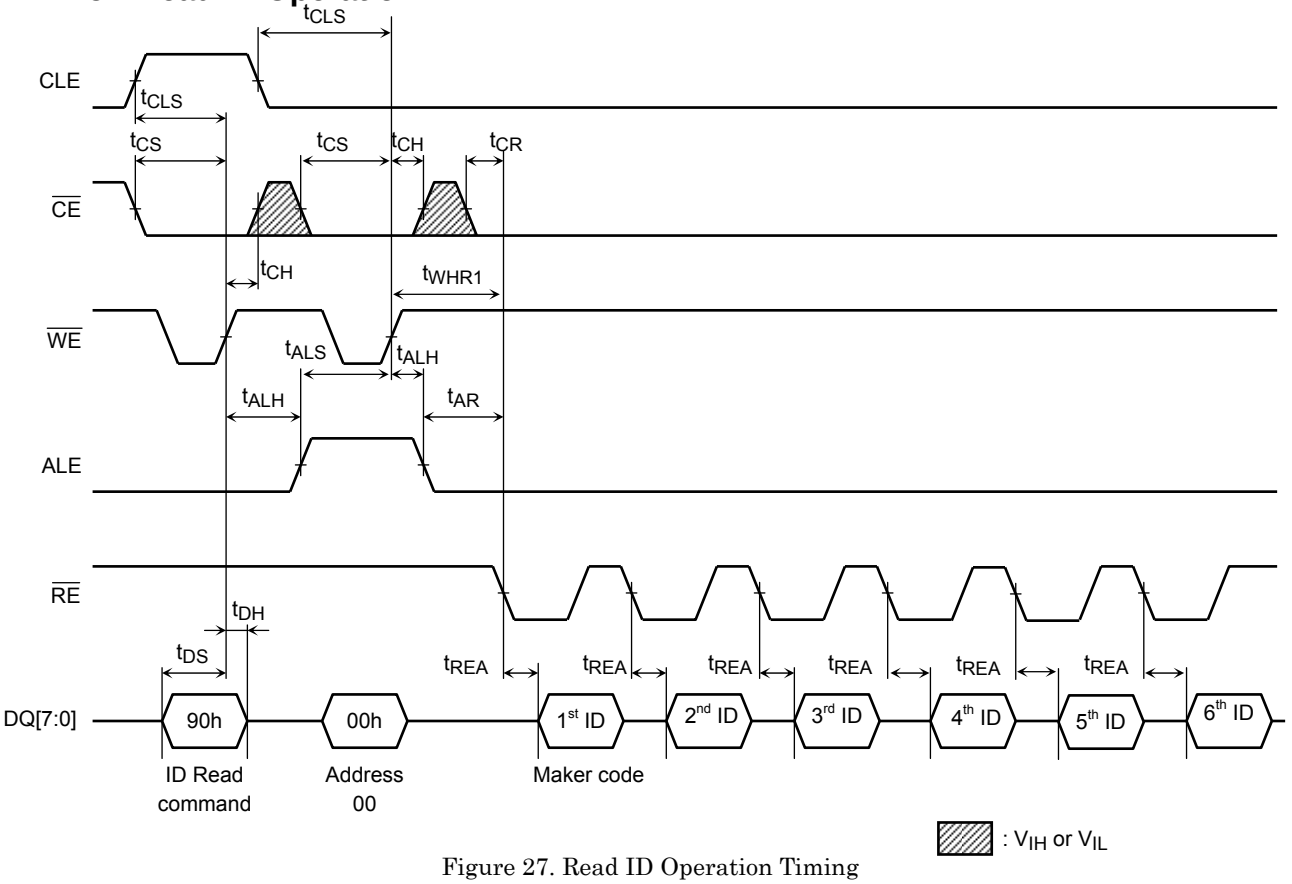


Figure 27. Read ID Operation Timing

4.2.2.6. Status Read Cycle

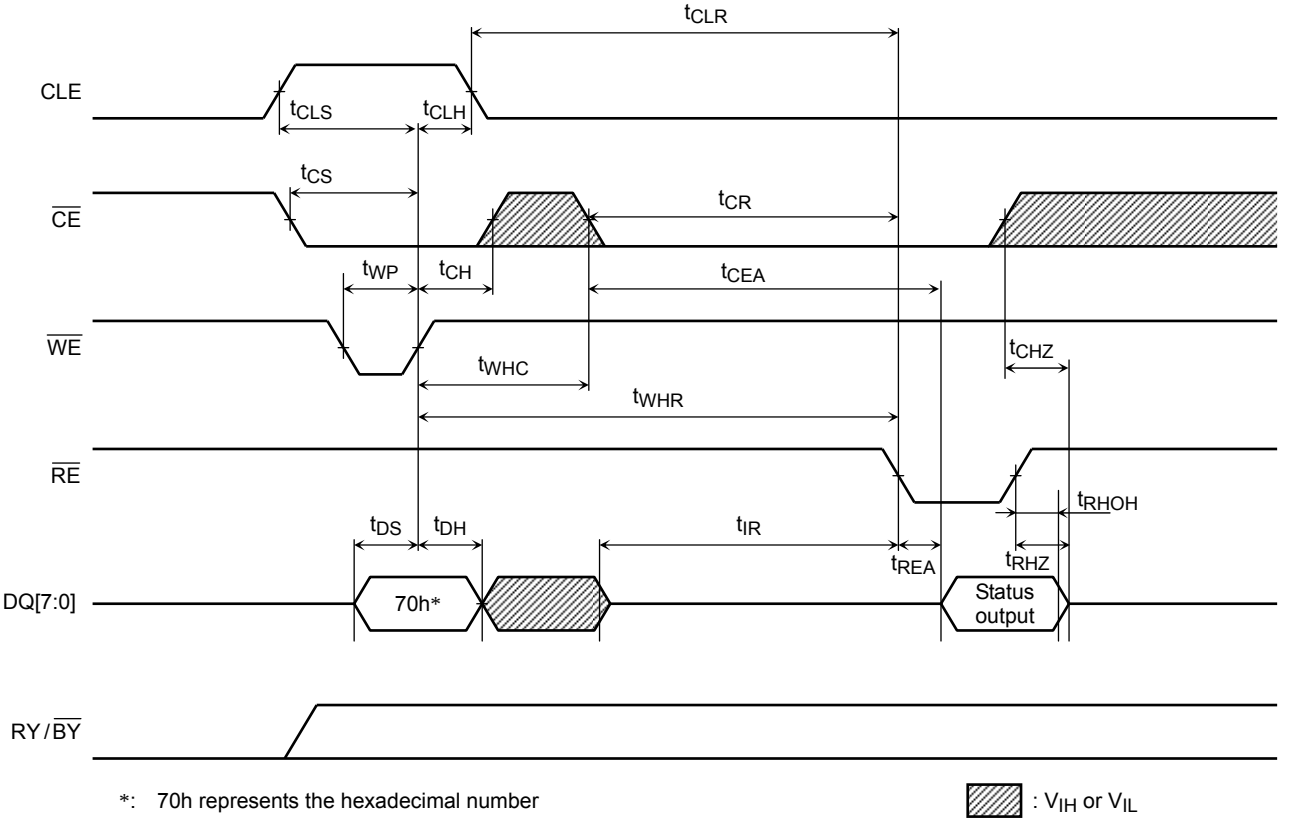


Figure 28. Status Read Cycle Timing

4.2.2.7. Set Feature

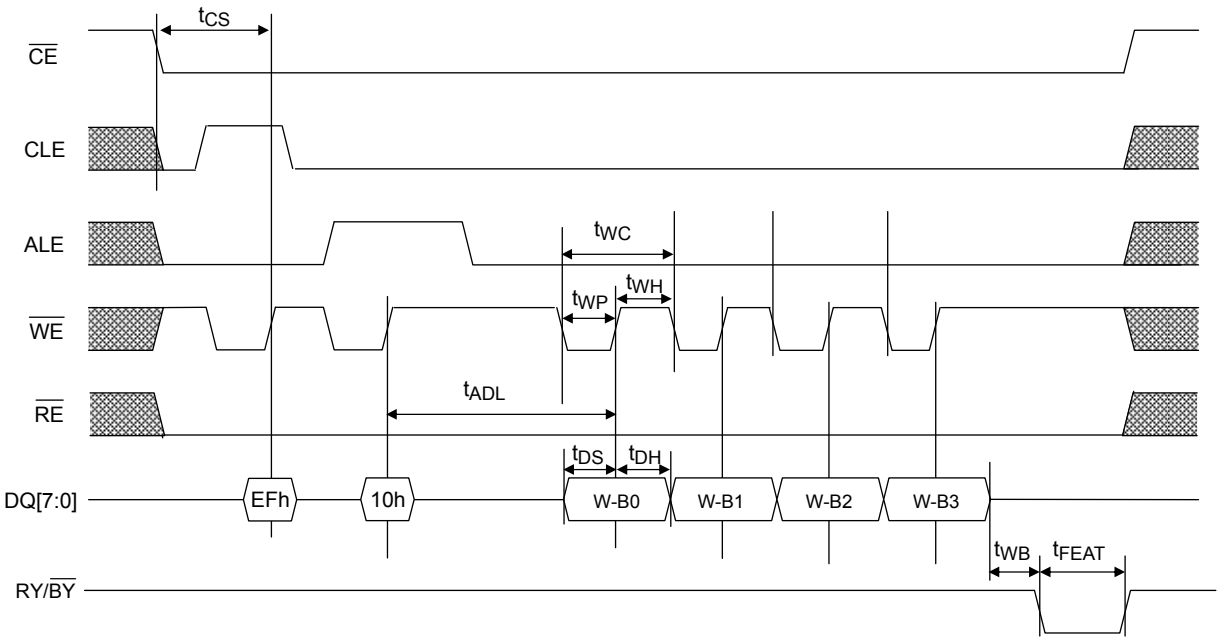


Figure 29. Set Feature Timing

4.2.2.8. Get Feature

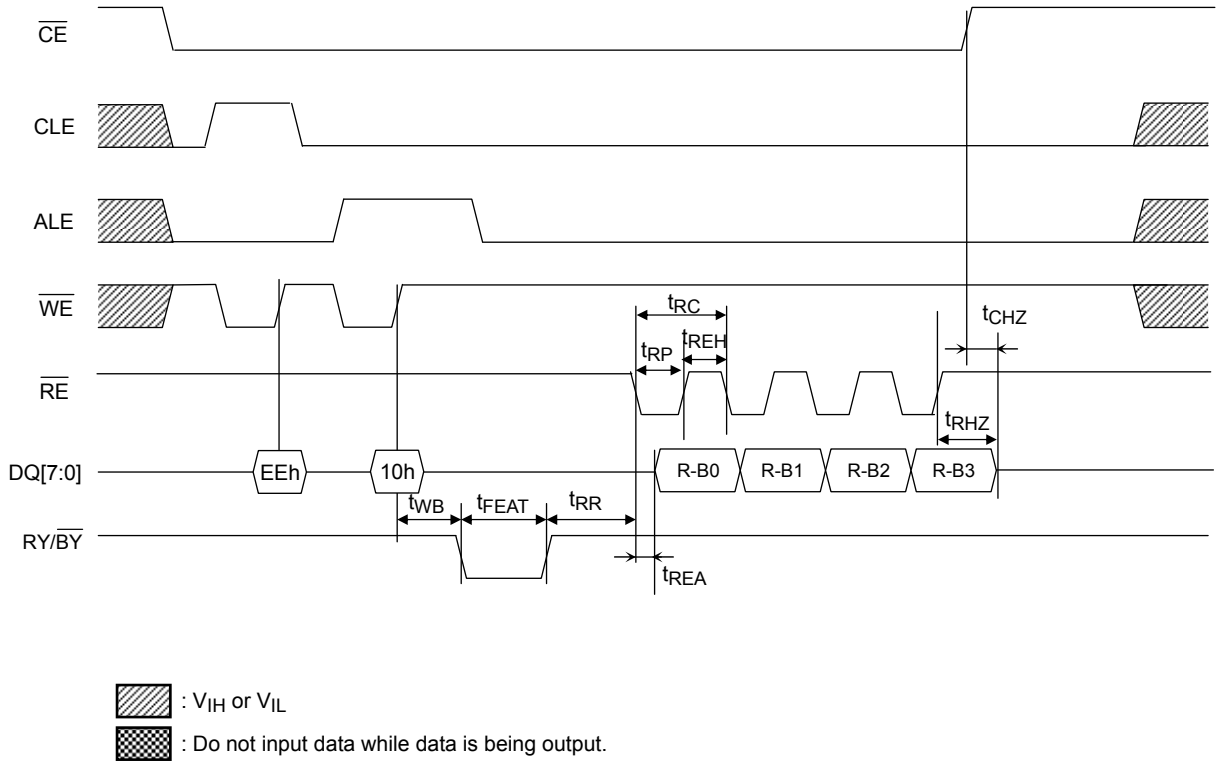


Figure 30. Get Feature Timing

4.2.2.9. Page Read Operation

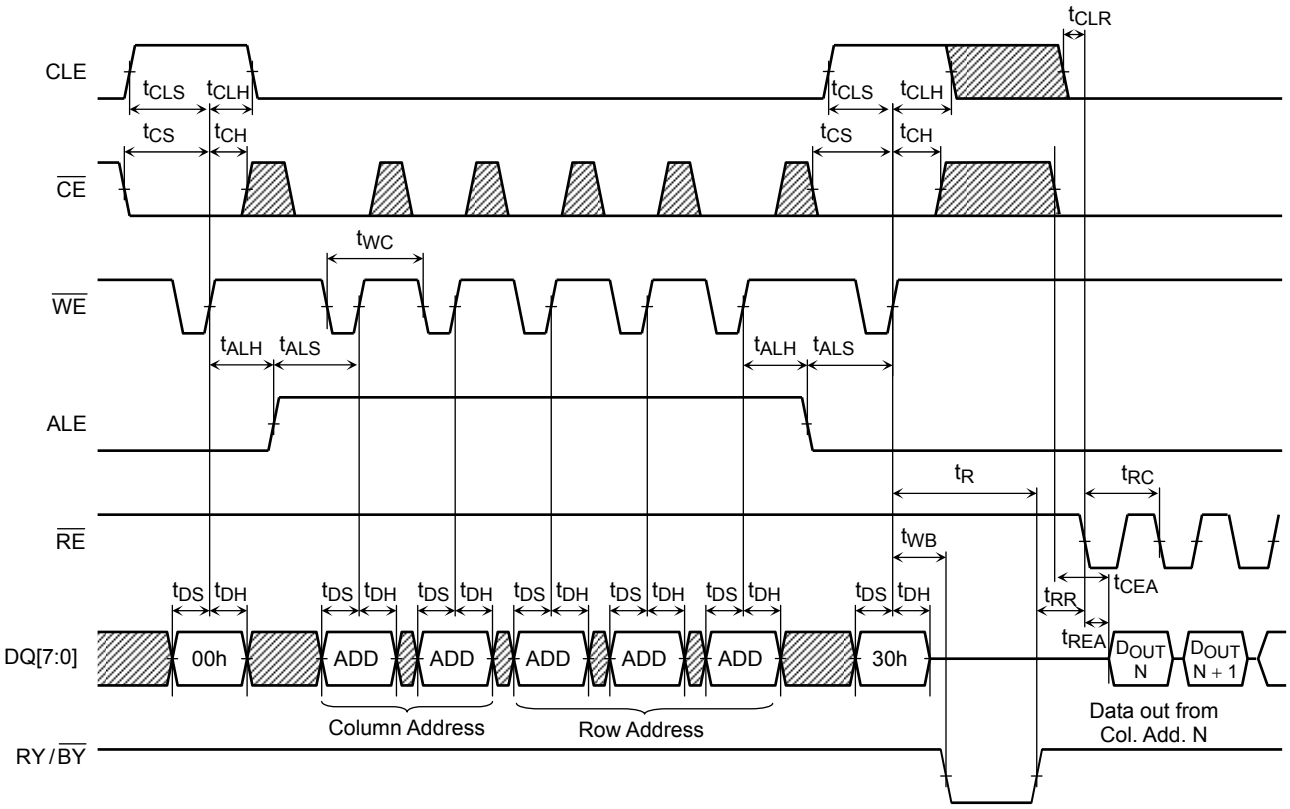
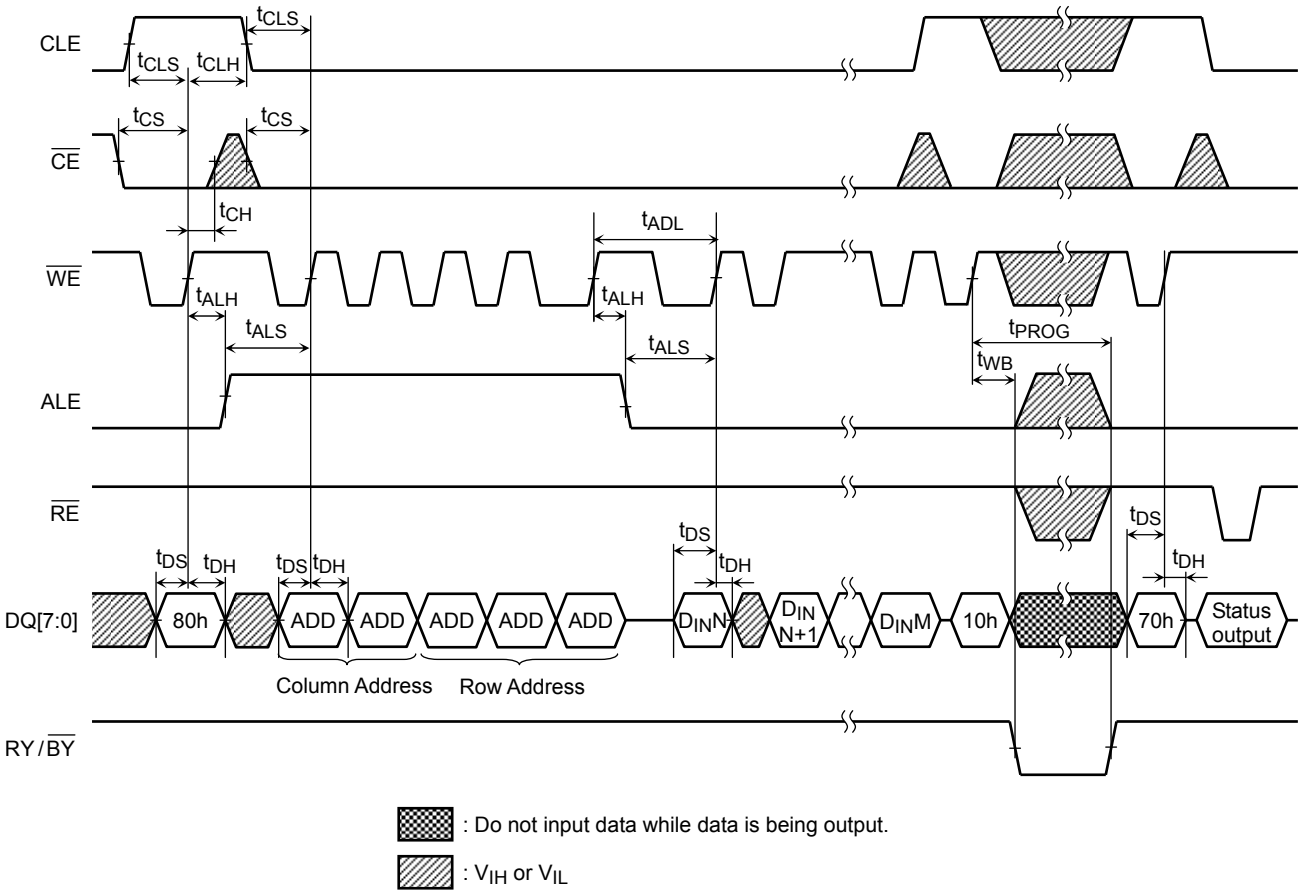


Figure 31. Page Read Operation Timing

4.2.2.10. Page Program Operation



*) M: up to 17664 (byte input data for ×8 device).

Figure 32. Page Program Operation Timing

4.3. AC Timing Characteristics

4.3.1. Timing Parameters Description

Table 25 Timing Parameters Description

Toggle DDR1.0

Parameter	Description
t_R	Data Transfer from Flash array to Register
t_{PROG}	Program Time
t_{BERASE}	Erase Time
t_{ADL}	Address to Data Loading Time
t_{AR}	ALE Low to $\overline{RE}$ Low
t_{CALH}	CLE/ALE Hold Time
t_{CALS}	CLE/ALE Setup Time
t_{CAH}	Command/Address Hold Time
t_{CAS}	Command/Address Setup Time
t_{CH}	$\overline{CE}$ Hold Time
t_{CDQSH}	DQS Hold Time for data input mode finish
t_{CDQSS}	DQS Setup Time for data input mode start
t_{CHZ}	$\overline{CE}$ High to Output Hi-Z
t_{CLHZ}	CLE High to Output Hi-Z
t_{CLR}	CLE to $\overline{RE}$ Low
t_{COH}	Data Hold Time after $\overline{CE}$ disable
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low
t_{CRES}	$\overline{RE}$ Setup Time before $\overline{CE}$ Low
t_{CS}	$\overline{CE}$ Setup Time
t_{CWAW}	Command Write Cycle to Address Write Cycle Time for Random Data Input
t_{DH}	Data Hold Time
t_{DQSH}	DQS Input High Pulse Width
t_{DQSL}	DQS Input Low Pulse Width
t_{DQSQ}	Output skew among data output and corresponding DQS
t_{DQSRE}	$\overline{RE}$ to DQS and DQ delay
t_{DSC}	Data Strobe Cycle Time
t_{DS}	Data Setup Time
t_{DVW}	Output data valid window
t_{FEAT}	Busy time for Set Feature and Get Feature
t_{QH}	Output hold time from DQS
t_{QHS}	DQS hold skew factor
t_{RC}	Read Cycle Time
t_{REH}	$\overline{RE}$ High pulse width
t_{RP}	$\overline{RE}$ Low pulse width
t_{RPP}	$\overline{RE}$ Low pulse width for Read Status at Power-up sequence
t_{RPRE}	Read Preamble
t_{RPST}	Read Postamble
t_{RPSTH}	Read Postamble Hold Time
t_{RR}	Ready to $\overline{RE}$ High
t_{RST}	Device Resetting Time(Read/Program/Erase)
t_{WB}	$\overline{WE}$ High to Busy
t_{WC}	Write Cycle Time
t_{WH}	$\overline{WE}$ High pulse width
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low
t_{WHR2}	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
t_{WP}	$\overline{WE}$ Low pulse Width

t_{WPRE}	Write Preamble
t_{WPST}	Write Postamble
t_{WPSTH}	Write Postamble Hold Time
t_{WW}	$\overline{WP}$ High/Low to $\overline{WE}$ E low
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)
t_{DCBSYR}	Cache Busy in Read Cache
$t_{DCBSYR2}$	Dummy Busy Time for Page Copy(2) Read

SDR

Parameter	Description
t_{CLS}	CLE Setup Time
t_{CLS2}	CLE Setup Time
t_{CLH}	CLE Hold Time
t_{CS}	$\overline{CE}$ Setup Time
t_{CS2}	$\overline{CE}$ Setup Time
t_{CH}	$\overline{CE}$ Hold Time
t_{WP}	$\overline{WE}$ Low pulse Width
t_{ALS}	ALE Setup Time
t_{ALH}	ALE Hold Time
t_{DS}	Data Setup Time
t_{DH}	Data Hold Time
t_{WC}	Write Cycle Time
t_{WH}	$\overline{WE}$ High pulse width
t_{ADL*}	Address to Data Loading Time
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low
t_{RR}	Ready to $\overline{RE}$ Falling Edge
t_{RW}	Ready to $\overline{WE}$ Falling Edge
t_{RP}	$\overline{RE}$ Low pulse width
t_{RC}	Read Cycle Time
t_{REA}	$\overline{RE}$ Access Time
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low
t_{CLR}	CLE Low to $\overline{RE}$ Low
t_{AR}	ALE Low to $\overline{RE}$ Low
t_{RHOH}	Data Output Hold Time from $\overline{RE}$ High
t_{RLOH}	Data Output Hold Time from $\overline{RE}$ Low
t_{RHZ}	$\overline{RE}$ High to Output High Impedance
t_{CHZ}	$\overline{CE}$ High to Output Hi-Z
t_{CLHZ}	CLE High to Output Hi-Z
t_{REH}	$\overline{RE}$ High pulse width
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low
t_{WHR1}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)
t_{WHR2}	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
t_{WB}	$\overline{WE}$ High to Busy
t_{RST}	Device Resetting Time(Read/Program/Erase)
t_{CEA}	$\overline{CE}$ Access Time
t_{FEAT}	Busy time for Set Feature and Get Feature

4.3.2. Timing Parameters Table

Table 26 AC Timing Charateristics

Toggle DDR1.0

Parameter	Symbol	100Mhz		Unit
		Min	Max	
Address to Data Loading Time	t_{ADL}	300	-	ns
ALE Low to /RE Low	t_{AR}	10	-	ns
CLE/ALE Hold Time	t_{CALH}	5	-	ns
CLE/ALE Setup Time	t_{CALS}	15	-	ns
Command/Address Hold Time	t_{CAH}	5	-	ns
Command/Address Setup Time	t_{CAS}	5	-	ns
DQS Hold Time for data input mode finish	t_{CDQSH}	100	-	ns
DQS Setup Time for data input mode start	t_{CDQSS}	100	-	ns
/CE Hold Time	t_{CH}	5	-	ns
/CE High to Output Hi-Z	t_{CHZ}	-	30	ns
CLE High to Output Hi-Z	t_{CLHZ}	-	30	ns
CLE to RE Low	t_{CLR}	10	-	ns
Data Hold Time after CE disable	t_{COH}	5	-	ns
/CE Low to /RE Low	t_{CR}	10	-	ns
/RE Setup Time before /CE Low	t_{CRES}	10	-	ns
/CE Setup Time	t_{CS}	20	-	ns
Command Write cycle to Address Write cycle Time for Random data input	t_{CWAW}	300	-	ns
Data Hold Time	t_{DH}	0.9	-	ns
DQS Input High Pulse Width	t_{DQSH}	$0.4*t_{RC}$	-	ns
DQS Input Low Pulse Width	t_{DQSL}	$0.4*t_{RC}$	-	ns
Output skew among data output and corresponding DQS	t_{DQSQ}	-	0.8	ns
/RE to DQS and DQ delay	t_{DQSRE}	-	25	ns
Data Strobe Cycle Time	t_{DSC}	10	-	ns
Data Setup Time	t_{DS}	0.9	-	ns
Output data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$		ns
Busy time for Set Feature and Get Feature	t_{FEAT}	-	1	µs
Output hold time from DQS	t_{QH}	$t_{QH} = \min[t_{REH}, t_{RP}] - t_{QHS}$		ns
DQS hold skew factor	t_{QHS}	-	0.8	ns
/RE Read Cycle Time	t_{RC}	10	-	ns
/RE High pulse width	t_{REH}	$0.4*t_{RC}$	-	ns
/RE Low pulse width	t_{RP}	$0.4*t_{RC}$	-	ns
RE Low pulse width for Read Status at Power-up sequence	t_{RPP}	30	-	ns
Read Preamble	t_{RPRE}	15	-	ns
Read Postamble	t_{RPST}	t_{DQSRE} + 0.5xtRC	-	ns
Read Postamble Hold Time	t_{RPSTH}	25	-	ns
Ready to /RE High	t_{RR}	20	-	ns
Device Resetting Time (Read/Program/Erase)	$t_{RST}^{(1)}$	10 /30 /100		µs
/WE High to Busy	t_{WB}	-	100	ns
Write Cycle Time	t_{WC}	25	-	ns
/WE High pulse width	t_{WH}	11	-	ns
/WE High to Low	t_{WHR}	120	-	ns
/WE High to /RE Low for Random data out	t_{WHR2}	300	-	ns

/WE Low pulse Width	t_{WP}	11	-	ns
Write Preamble	t_{WPRE}	15	-	ns
Write Postamble	t_{WPST}	6.5	-	ns
Write Postamble Hold Time	t_{WPSTH}	25	-	ns
/WP High/Low to /WE low	t_{WW}	100	-	ns

SDR

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}	10	—	ns
CLE Setup Time	t_{CLS2}	40	—	ns
CLE Hold Time	t_{CLH}	5	—	ns
$\overline{CE}$ Setup Time	t_{CS}	15	—	ns
$\overline{CE}$ Setup Time	t_{CS2}	32	—	ns
$\overline{CE}$ Hold Time	t_{CH}	5	—	ns
Write Pulse Width	t_{WP}	10	—	ns
ALE Setup Time	t_{ALS}	10	—	ns
ALE Hold Time	t_{ALH}	5	—	ns
Data Setup Time	t_{DS}	5	—	ns
Data Hold Time	t_{DH}	5	—	ns
Write Cycle Time	t_{WC}	20	—	ns
$\overline{WE}$ High Hold Time	t_{WH}	7	—	ns
Address to Data Loading Time	t_{ADL*}	300	—	ns
$\overline{WP}$ High to $\overline{WE}$ Low	t_{WW}	100	—	ns
Ready to $\overline{RE}$ Falling Edge	t_{RR}	20	—	ns
Ready to $\overline{WE}$ Falling Edge	t_{RW}	20	—	ns
Read Pulse Width	t_{RP}	10	—	ns
Read Cycle Time	t_{RC}	20	—	ns
$\overline{RE}$ Access Time	t_{REA}	—	16	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	9	—	ns
CLE Low to $\overline{RE}$ Low	t_{CLR}	10	—	ns
ALE Low to $\overline{RE}$ Low	t_{AR}	10	—	ns
Data Output Hold Time from $\overline{RE}$ High	t_{RHOH}	25	—	ns
Data Output Hold Time from $\overline{RE}$ Low	t_{RLOH}	5	—	ns
$\overline{RE}$ High to Output High Impedance	t_{RHZ}	—	60	ns
$\overline{CE}$ High to Output High Impedance	t_{CHZ}	—	30	ns
CLE High to Output High Impedance	t_{CLHZ}	—	30	ns
$\overline{RE}$ High Hold Time	t_{REH}	7	—	ns
Output-High-impedance-to-$\overline{RE}$ Falling Edge	t_{IR}	0	—	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{WHR}	30	—	ns
$\overline{WE}$ High to $\overline{CE}$ Low	t_{WHC}	30	—	ns
$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)	t_{WHR1}	180	—	ns
$\overline{WE}$ High to $\overline{RE}$ Low (Column Address Change in Read)	t_{WHR2}	300	—	ns
$\overline{WE}$ High to Busy	t_{WB}	—	100	ns
Device Reset Time (Ready/Read/Program/Erase)	t_{RST}	—	10/30/100	μs
$\overline{CE}$ Access Time	t_{CEA}	—	25	ns
Busy time for Set Feature and Get Feature	t_{FEAT}	—	1	μs

NOTE : The values in this table are preliminary and subject to change.

Table 27 AC Test Conditions

Toggle DDR1.0

Parameter	Condition
Input Pulse Levels	VIL to VIH
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	VccQ/2
Output Load	50 Ohms to Vtt (Vtt=0.5*VCCQ)

SDR (VCCQ=3.3V)

Parameter	Condition
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	3ns
Input comparison level	$V_{CC}/2$
Output data comparison level	$V_{CC}/2$
Output load	C_L (50 pF) + 1 TTL

SDR (VCCQ=1.8V)

Parameter	Condition
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	3ns
Input comparison level	$V_{CC}/2$
Output data comparison level	$V_{CC}/2$
Output load	C_L (30 pF) + 1 TTL

NOTE :

1) Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin. (Refer to Application Note (9) toward the end of this document.)

Table 28 Read/Program/Erase Timing Characteristics

Description	Parameter	Typ.	Max.	Unit
Data Transfer from Cell to Register	t_R	50 (TENTATIVE)	100 (TENTATIVE)	µs
Average Programming Time	t_{PROG}	1400 (TENTATIVE)	3000 (TENTATIVE)	µs
Block Erasing Time	t_{BERASE}	5 (TENTATIVE)	10 (TENTATIVE)	ms
Data Cache Busy Time in Write Cache (following 11h or 32h)	$t_{DCBSYW1}$	0.5	1	µs
Data Cache Busy Time in Write Cache (following 15h)	$t_{DCBSYW2}$	-	3000 (TENTATIVE)	µs
Cache Busy in Read Cache	t_{DCBSYR}	-	100(TENTATIVE)	µs
Dummy Busy Time for Page Copy(2) Read	$t_{DCBSYR2}$	-	105(TENTATIVE)	µs
Number of Partial Program Cycles in the Same Page	-	-	-	Cycle

NOTE :

1)t_{PROG} is the internal program time from a cache or page register to NAND array. t_R is the internal loading time from NAND array to the a cache or page register.

2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

3) tPROG and tDCBSYW2 are the average busy time in a block. The absolute maximum for one page operation is 5000µs.

5. COMMAND DESCRIPTION AND DEVICE OPERATION

5.1. Basic Command Sets

Toggle DDR1.0 NAND Flash Memory has addresses multiplexed into 8 I/Os. Command, address and data are all written through DQ [7:0] by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 29 below defines the basic command sets.

Table 29 Basic Command Sets

Function	Primary or Secondary	1st Set	Address Cycles	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
Page Read	Primary	00h	5	30h		Y
Sequential Cache Read	Primary	31h	-	-		Y
Read Start for Last Page Cache Read	Primary	3Fh	-	-		Y
Random Cache Read	Primary	00h	5	31h		Y
Page Program	Primary	80h	5	10h		Y
Cache Program	Primary	80h	5	15h		Y
Block Erase	Primary	60h	3	D0h		Y
Read for Copy-Back	Primary	00h	5	35h		Y
Copy-Back Program	Primary	85h	5	10h		Y
Random Data Input(1)	Primary	85h	2	-		Y
Random Data Output(1)	Primary	05h	2	E0h		Y
Set Feature	Primary	EFh	1	-		
Get Feature	Primary	EEh	1	-		
Read ID	Primary	90h	1	-		Y
Read Status	Primary	70h	-	-	Y	Y
Read Status2	Primary	71h	-	-	Y	Y
Reset	Primary	FFh	-	-	Y	Y
Reset LUN	-	FAh	3	-	Y	Y

NOTE:
1) Random Data Input/Output can be executed in a page.

Caution:
Any undefined command inputs are prohibited except for above command set.

5.2. Basic Operation

5.2.1. Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure 33 defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

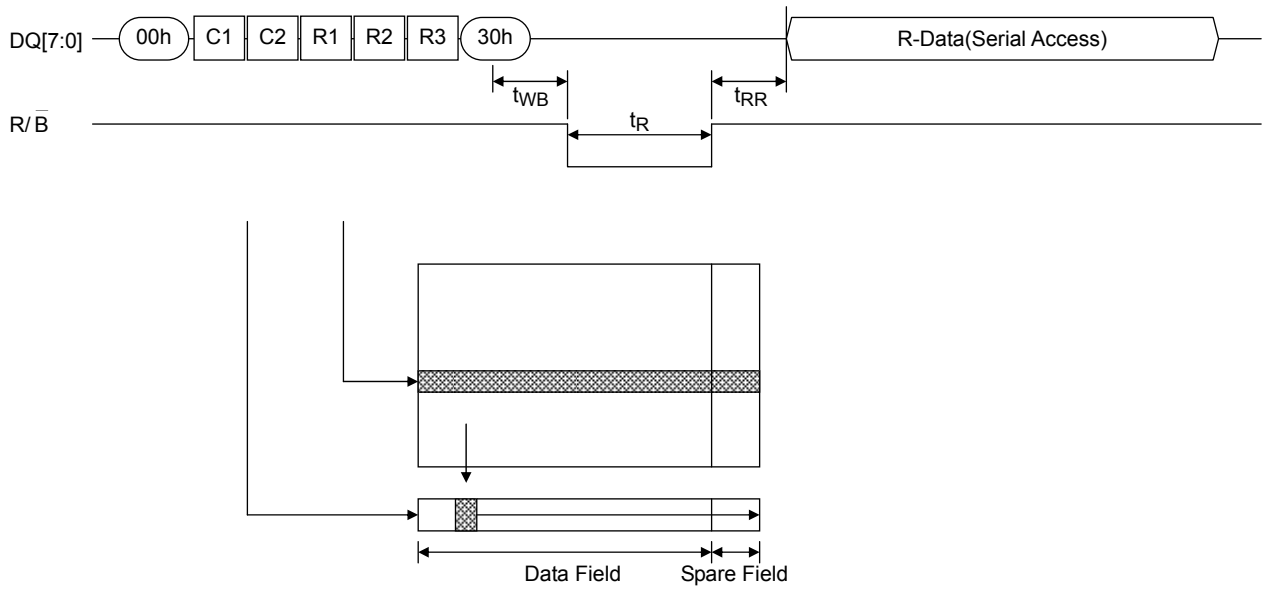


Figure 33. Page Read Timing

5.2.1.1. Page Read Operation with Random Data Output

The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure 34 defines the Random Data Output behavior and timings. The host shall not read data from the LUN until t_{WHR2}(ns) after the second(i.e. E0h) is written to the LUN.

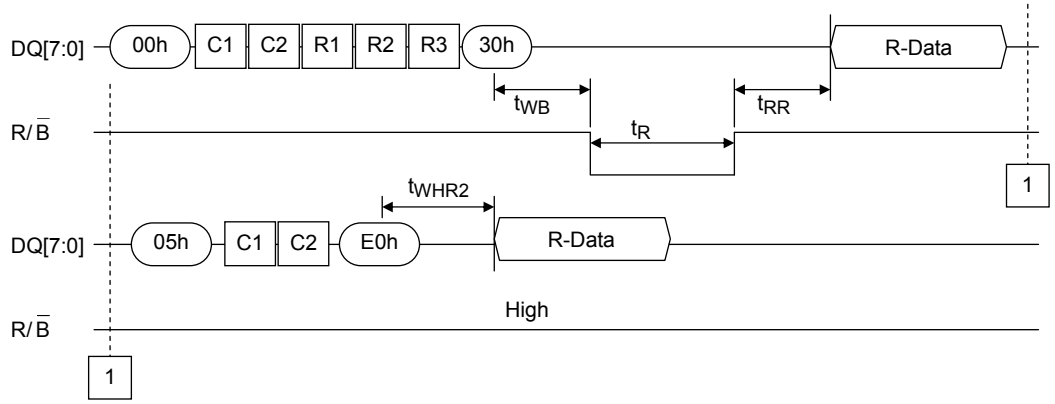


Figure 34. Page Read with Random Data Output Timing

5.2.1.2. Data Out After Status Read

While monitoring the read status to determine when the t_R (transfer from Flash array to a page register) is complete, the host shall re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

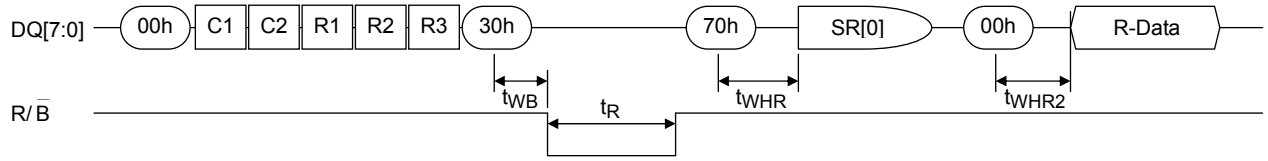
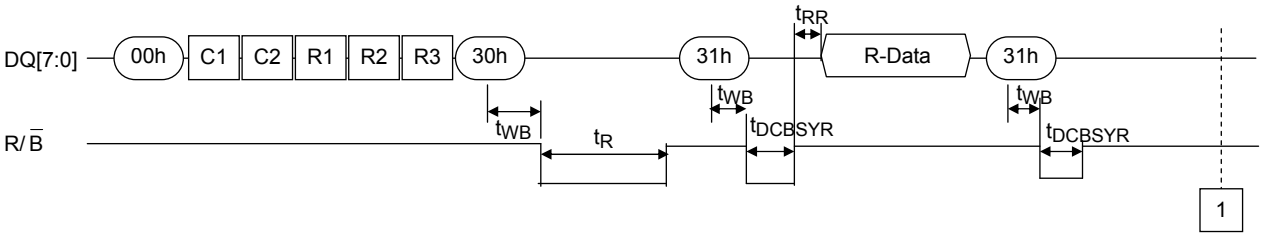


Figure 35. Data Out After Status Read Timing

5.2.2. Sequential Cache Read Operation

The Sequential Cache Read operation permits a page to be read from the page register while another page is simultaneously read from the Flash array for the selected LUN. A Read Page command shall be issued prior to the initial Sequential Cache Read command in a cache read sequence. A Sequential Cache Read command shall be issued prior to the Read Start for Last Page Cache Read command (3Fh) being issued.

The Sequential Cache Read command may be issued after the Read function is complete (i.e. SR[6] is set to one).



Data output always begins at column address 00h. When the Sequential Cache Read command (i.e. 31h) is issued, SR[6] is cleared to zero (i.e. busy). After the operation finishes, SR[6] turns to one (i.e. ready) and the host may begin to read the data loaded by the previous Sequential Cache Read operation. The data loaded by a Sequential Cache Read command from Flash array to a page register is copied to a cache register by a following Sequential Cache Read command. And the data of a final page loaded onto a page register is transferred to a cache register by 3Fh command. The host shall not issue a Sequential Cache Read command (31h) after the last page of a block is read. Figure 36 defines the Sequential Cache Read behavior and timings.

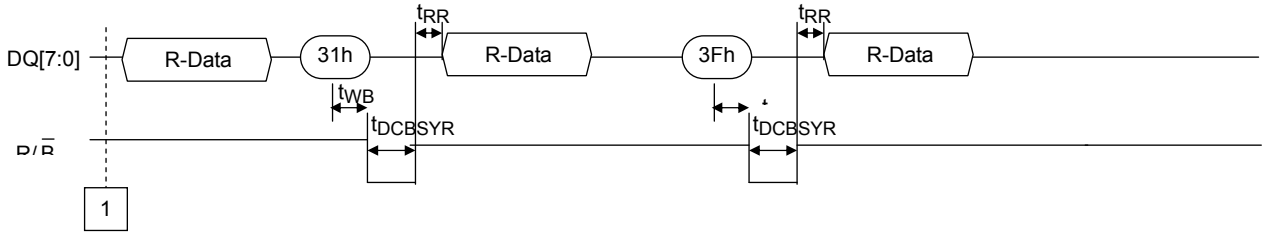


Figure 36. Sequential Cache Read Timing

5.2.3. Random Cache Read Operation

A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. A Random Cache Read command shall be issued prior to the Read Start for Last Page Cache Read command (3Fh) being issued. The page and block address can be accessed in a random manner. Data output always begins at column address 00h. Figure 37 defines the Random Cache Read behavior and timings.

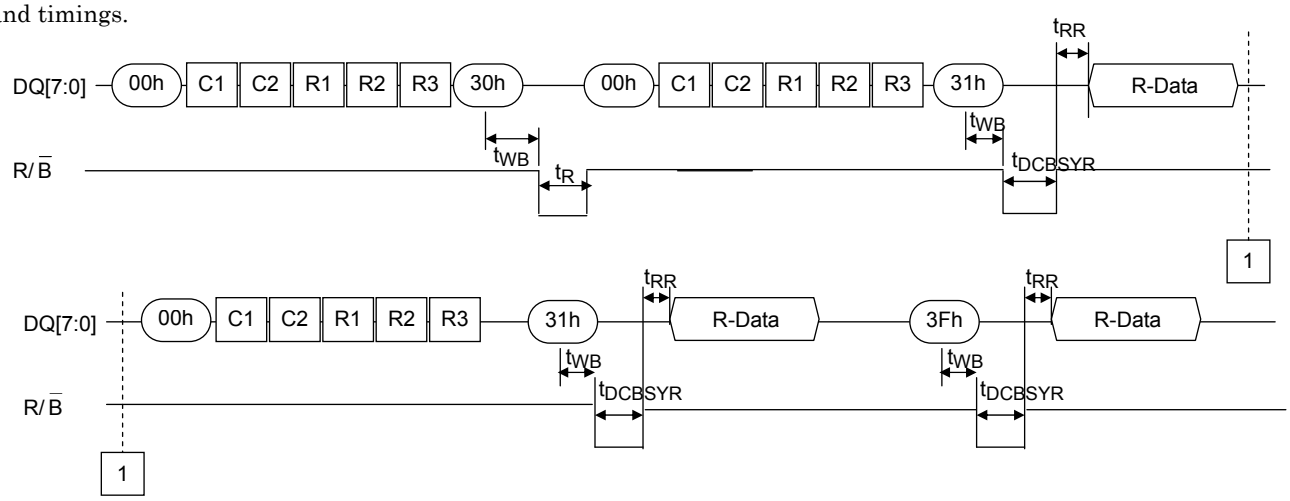


Figure 37. Random Cache Read Timing

5.2.4. Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 38 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

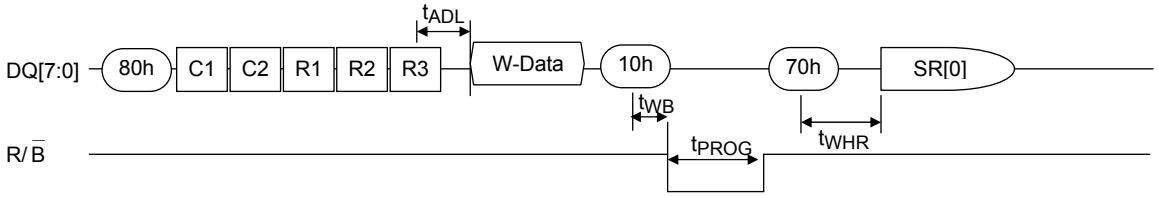


Figure 38. Page Program Timing

5.2.4.1. Program Operation with Random Data Input

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command (i.e. 85h). Random data input may be operated multiple times without limitation.

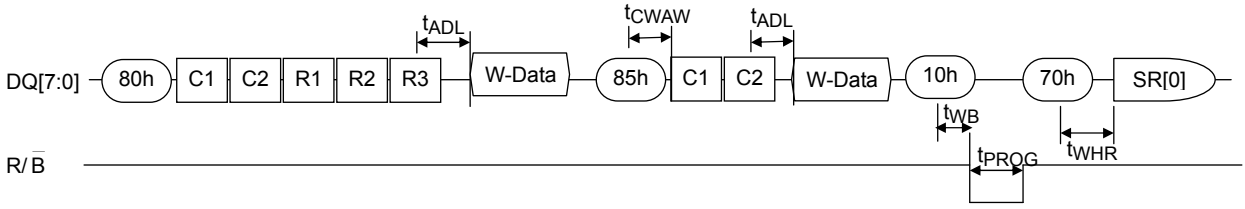


Figure 39. Program operation with Random Data Input Timing

5.2.5. Cache Program Operation

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/$\overline{B}$ returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. However, when command 10h is issued for the final page, R/$\overline{B}$ turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure 40 defines the Cache Program behavior and timings. Note that t_{PROG} at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

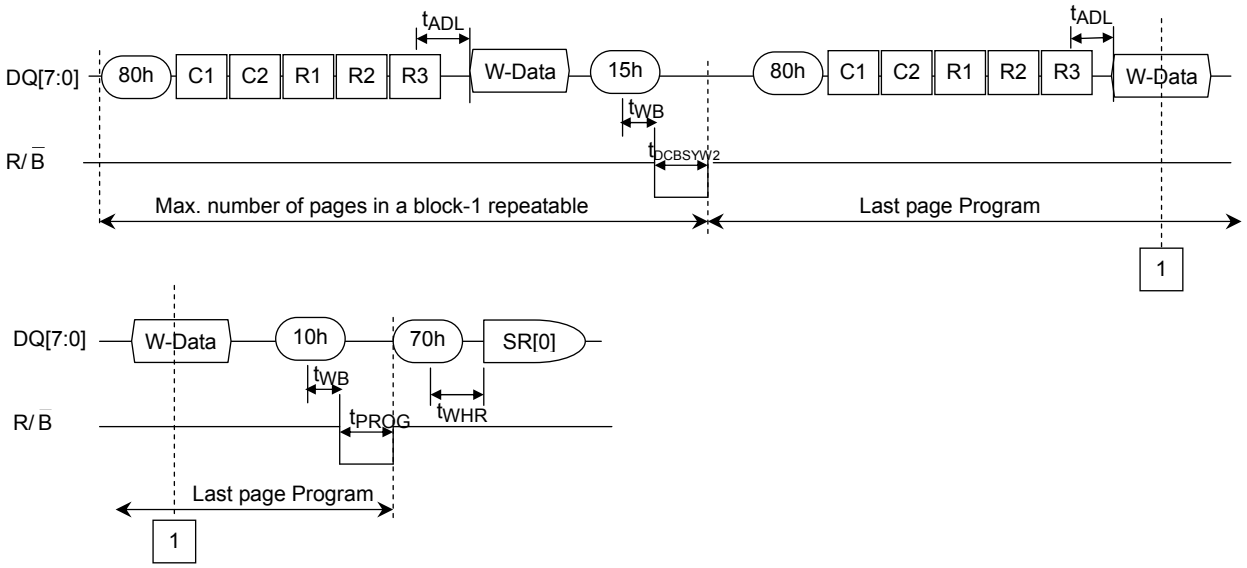


Figure 40. Cache Program Timing

5.2.6. Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while plane and block address are valid. After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure 41 defines the Block Erase behavior and timings.

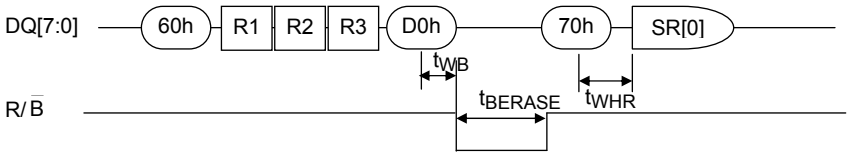


Figure 41. Block Erase Timing

5.2.7. Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page of a block to a page of the other block without data re-loading when no error within the page is found. Since the time-consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Copy-Back Program Operation shall work only within the same plane. Figure 42 defines the Copy-Back Program behavior and timings.

NOTE:

The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.

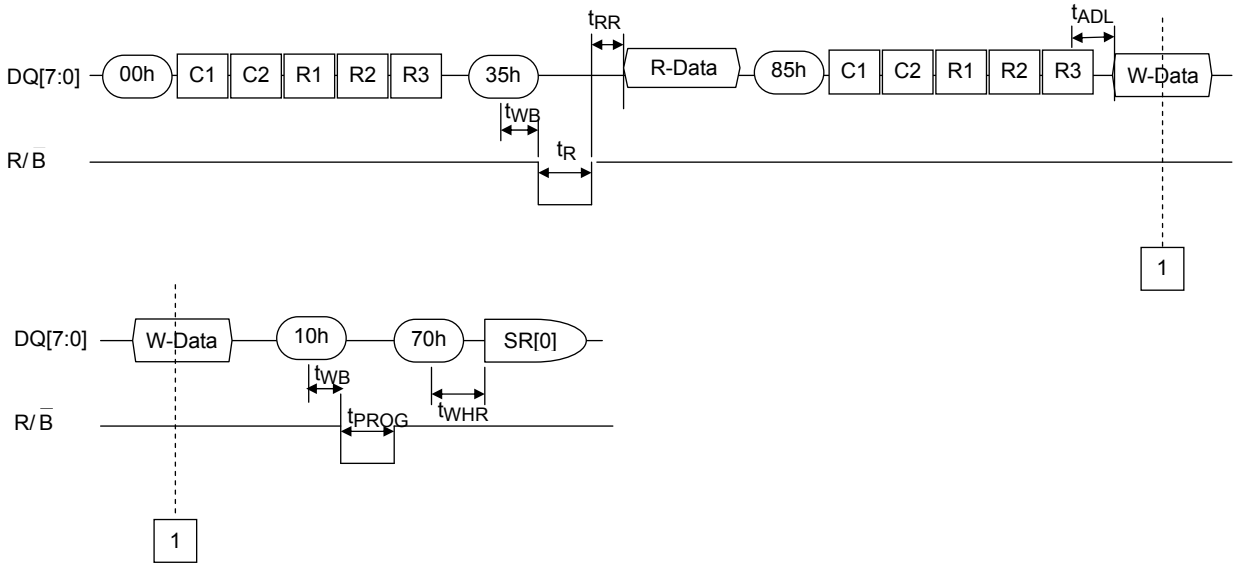


Figure 42. Copy-Back Program Timing

5.2.7.1. Copy-Back Program Operation with Random Data Input

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure 43 defines the Copy-Back Program with Random Data Input behavior and timings.

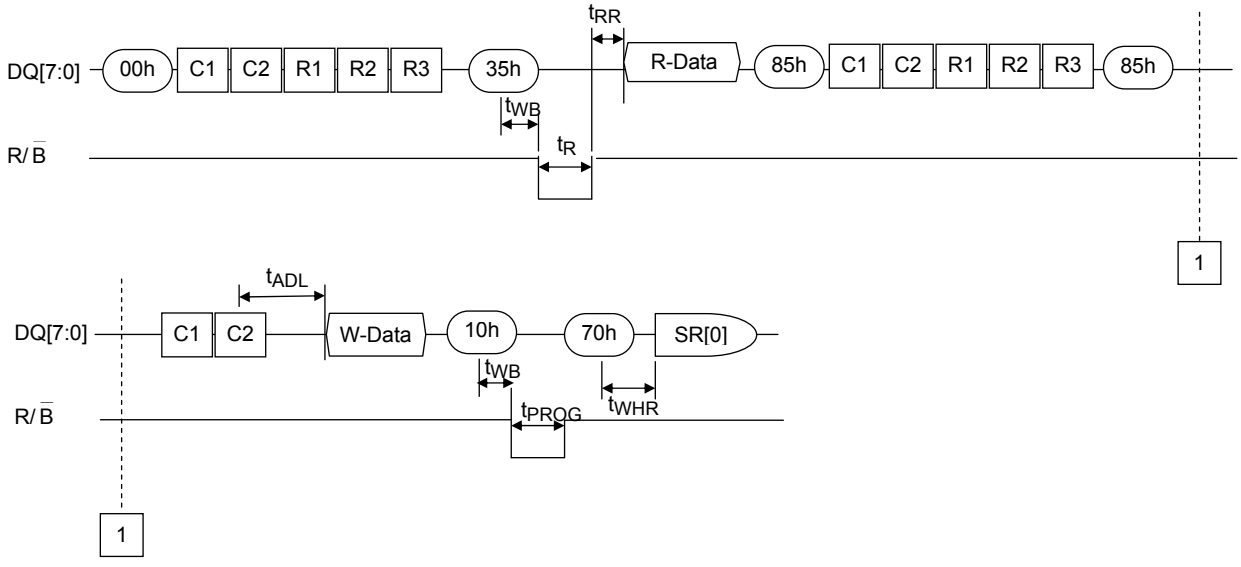


Figure 43. Copy-Back Program with Random Data Input Timing

5.2.8. Set Feature Operation

Users may set particular features using 'Set Feature' operation. Figure 44 defines the Set Features behavior and timings and Table 30 defines features that users can change. Once Set Feature operation begins, the operation shall be completed without any disturbance and interruption such as Reset operation.

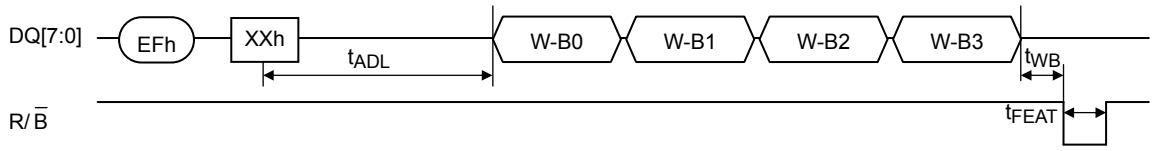


Figure 44. Set Feature Timing

NOTE:
The feature-setting shall work on lower than 133Mbps.

Table 30 Set feature addresses

1st Cycle	2nd Cycle	Description
EFh	10h	Driver strength setting
	80h	Interface change

5.2.8.1. Driver strength setting (10h)

Driver strength is configured according to the B0 value.

Table 31 Driver Strength Setting Data

B0 Value	Description
00h ~ 01h	Reserved
02h	Driver Multiplier : Underdrive
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	Driver Multiplier : Overdrive 1
07h	Reserved
08h	Reserved
09h ~ FFh	Reserved

NOTE:
B1, B2 and B3 are reserved and shall be written with 00h.

Table 32 Interface change Setting Data

B0 Value								Description
DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	
0	0	0	0	0	0	0	0	to Toggle DDR1.0
0	0	0	0	0	0	0	1	to SDR

5.2.9. Get Feature Operation

Users find how the target is set through 'Get Feature' command. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. B0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure 45 defines the Get Features behavior and timings.

If Read Status (or Read Status Enhanced) is used to monitor whether the t_{FEAT} time is complete, the host shall issue Read command (i.e. 00h) to read B0-B1-B2-B3.

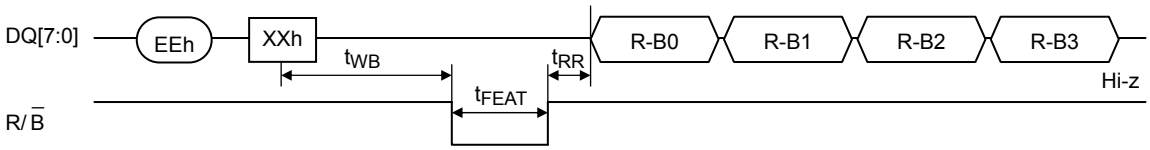


Figure 45. Get Feature Timing

NOTE:
The feature-getting shall work on lower than 133Mbps.

5.2.10. Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Figure 46 defines Read ID operation behavior and timings.

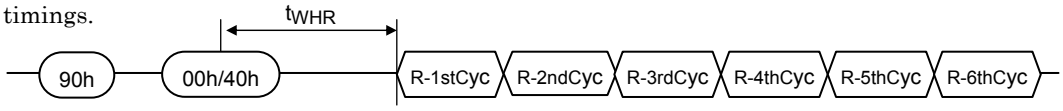


Figure 46. Read ID Timing

5.2.10.1. 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecture information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

Table 33 00h Address ID Definition Table

Cycle	Description	TC58TEG6D2H
1st Data	Maker Code	98h
2nd Data	Device Code	D7h
3rd Data	Number of LUN per Target, Cell Type, Etc.	84h
4th Data	Page Size, Block Size,etc.	93h
5th Data	Plane Number,etc.	72h
6th Data	Technology Code	57h

Table 34 2nd ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Memory Density per Target	8 Gbits	1	1	0	1	0	0	1	1	D3h
	16 Gbits	1	1	0	1	0	1	0	1	D5h
	32 Gbits	1	1	0	1	0	1	1	1	D7h
	64 Gbits	1	1	0	1	1	1	1	0	DEh
	128 Gbits	0	0	1	1	1	0	1	0	3Ah
	256 Gbits	0	0	1	1	1	1	0	0	3Ch

Table 35 3rd ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Number of LUN per Target	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		

Table 36 4th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size (w/o redundant area)	2KB							0	0
	4KB							0	1
	8KB							1	0
	16KB							1	1
Block Size (w/o redundant area)	128KB	0		0	0				
	256KB	0		0	1				
	512KB	0		1	0				
	1MB	0		1	1				
	2MB	1		0	0				
	4MB	1		0	1				
	Reserved	1		X	X				

*X : either 0 or 1

Table 37 5th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Number of Plane per Target	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		

Table 38 6th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Technology Code	130 nm process						0	0	0
	90 nm process						0	0	1
	70 nm process						0	1	0
	56 nm process						0	1	1
	43 nm process						1	0	0
	32 nm process						1	0	1
	24 nm process						1	1	0
	19 nm process						1	1	1
Interface	Conventional	0							
	Toggle DDR1.0 Mode	1							

NOTE:

As for Table 38 “6th ID data”, even if the interface is changed into Toggle DDR1.0 by SetFeature, the value of "Interface" is still 0.

5.2.10.2. 40h Address ID Definition

Toggle DDR1.0 NAND also provides six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

Table 39 40h Address ID Cycle

1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	01h

Table 40 40h Address ID Definition

Cycle	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0	1	0	1	0
2nd	E	0	1	0	0	0	1	0	1
3rd	D	0	1	0	0	0	1	0	0
4th	E	0	1	0	0	0	1	0	1
5th	C	0	1	0	0	0	0	1	1
6th	Conventional Asynchronous SDR	0	0	0	0	0	0	0	1
	Toggle DDR1.0					0	0	1	0
	Synchronous DDR					0	1	0	0

5.2.11. Read Status Operation

In the case of non-multi-plane operations, the 70h Read Status function retrieves a status value for the last operation issued. If multi-plane operations are in progress on a single LUN, then 70h Read Status returns the composite status value. Specifically, 70h Read Status shall return the combined status value of the independent status register bits according to Table 41. On the other hands, 71h Read Status returns statuses of two planes on a single LUN according to Table 42. Figure 47 defines the Read Status behavior and timings.

Table 41 Read Status Definition for 70h

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Copy-Back	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0 is only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0 is only valid when DQ 5 shows the Ready state, and DQ 1 is only valid when DQ 6 shows the Ready state.

Table 42 Read Status Definition for 71h

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail	Pass/Fail for Plane#0 (N)	Pass/Fail for Plane#1 (N)	Pass/Fail for Plane#0 (N-1)	Pass/Fail for Plane#1 (N-1)	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Copy-Back	Pass/Fail	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ 5 shows the Ready state, and DQ 3 and DQ 4 are only valid when DQ 6 shows the Ready state.

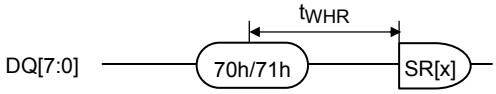


Figure 47. Read Status Timing

5.2.12. Reset Operation

Toggle DDR1.0 NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations. The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Reset during the operation with a cache register (e.g. Cache Program operation) may not just stop the most recent page operation but it may also stop the previous page operation depending on when the FF reset is input. Although the device is already in process of reset operation, a new reset command will be accepted. Figure 48 defines the Reset behavior and timings.

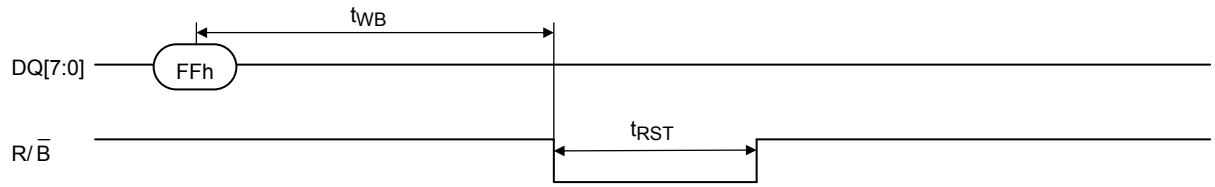


Figure 48. Reset timing

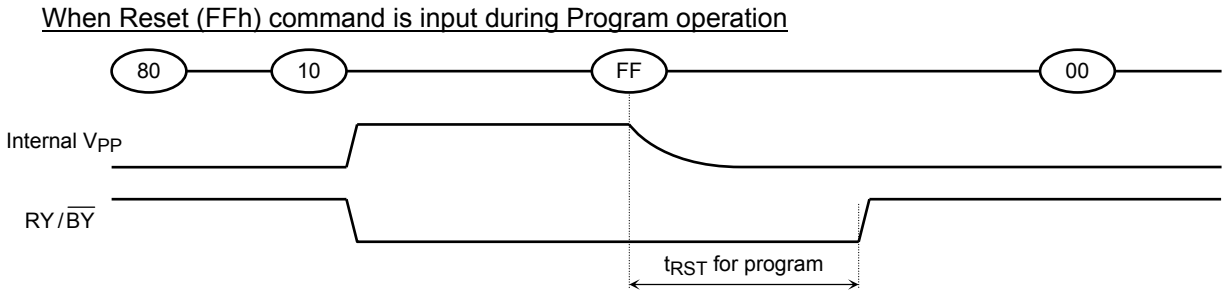


Figure 49. Reset timing during Program operation

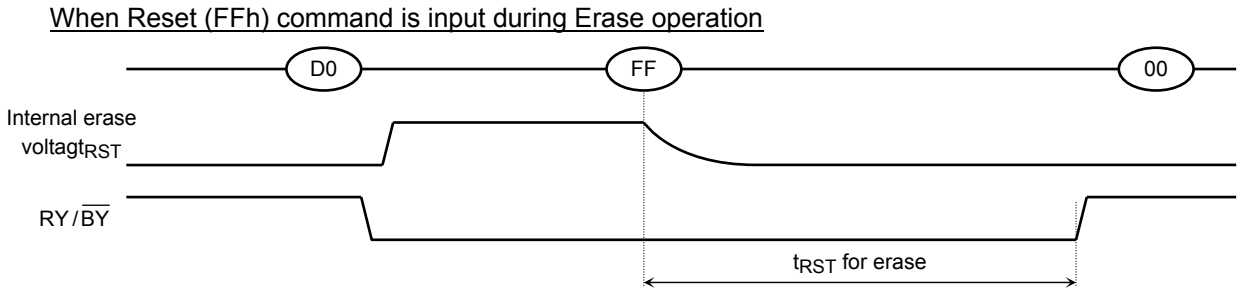


Figure 50. Reset timing during Erase operation

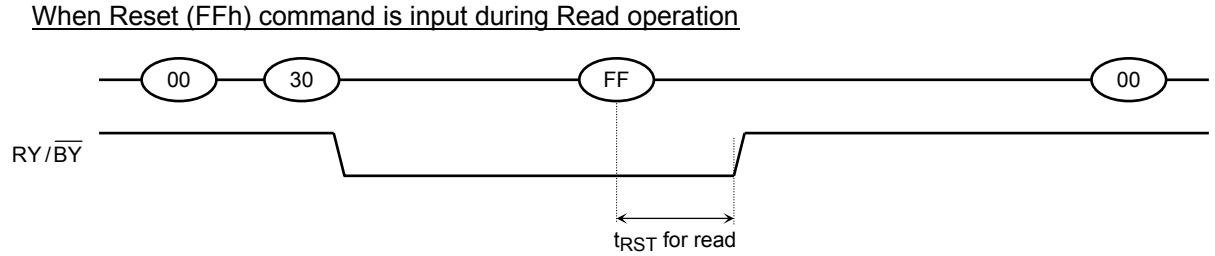


Figure 51. Reset timing during Read operation

When Read Status command (70h) is input after Reset operation

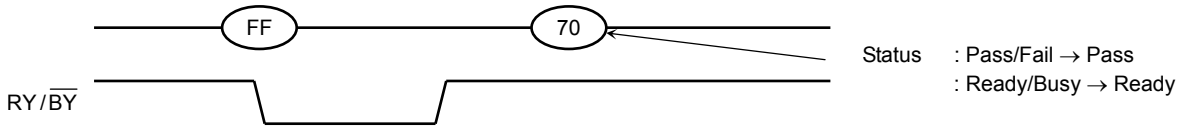


Figure 52. Status Read after Reset operation

When two or more Reset commands are input in succession

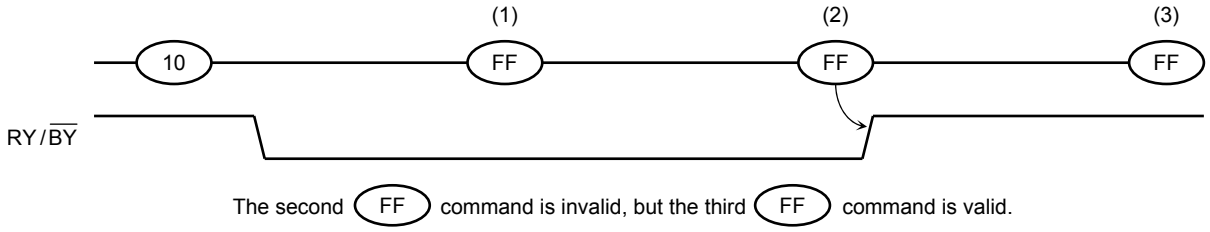


Figure 53. Successive Reset operation

5.2.13. Reset LUN Operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure 54 defines the Reset LUN behavior and timings.

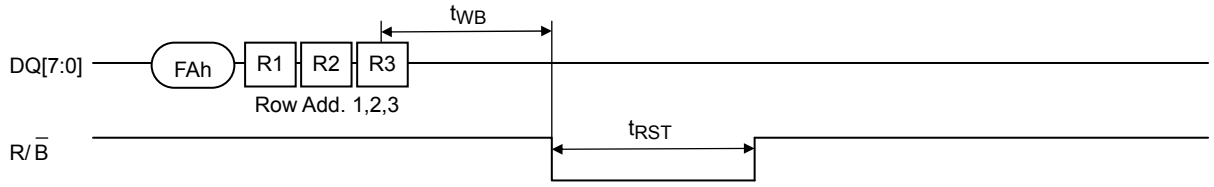


Figure 54. Single LUN Reset Timing

NOTE :
If there are multiple LUNs on a target, R/$\overline{B}$ is also affected by the rest of LUN(s) on the same target.

5.3. Extended Operation

5.3.1. Extended Command Sets

Table 43 defines the Extended Command Sets. Primary and Secondary Commands are also categorized in the table. Primary commands are recommended to use when a particular function is implemented, while Secondary commands are for alternative implementation for backward compatibility.

Table 43 Extended Command Sets

Function	Primary or secondary	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set
Page Copy (2) Read	Primary	00h--	5	--3Ah	-
Page Copy (2) Program	Primary	8Ch--	5	--15h	-
Page Copy (2) Program for Last Page	Primary	8Ch--	5	--10h	-
Device Identification Table Read	Primary	ECh--	1	-	-
Read status enhanced	Primary	78h--	3	-	-
Read LUN#0 Status	Secondary	F1h	-	-	-

5.3.2. Page Copy (2) Operation

By using Page Copy (2), data in a page of a block can be copied to a page of the other block after the data has been read out. This operation needs to be executed within a plane. If the block address is changed, this sequence shall be started from the beginning. Data input is required only if previous data output needs to be changed. If the data needs to be changed, locate the desired address with the column and row address input after 8Ch command, and change only the data that needs to be changed. Make sure $\overline{WP}$ is held to High level when Page Copy (2) operation is performed.

Figure 55 defines Page Copy (2) behavior and timings.

NOTE:

The least significant bit of page address shall be the same between source and destination pages. In other words, the page of even page address cannot be copied to the page of odd page address, and the page of odd page address cannot be copied to the page of even page address as well.

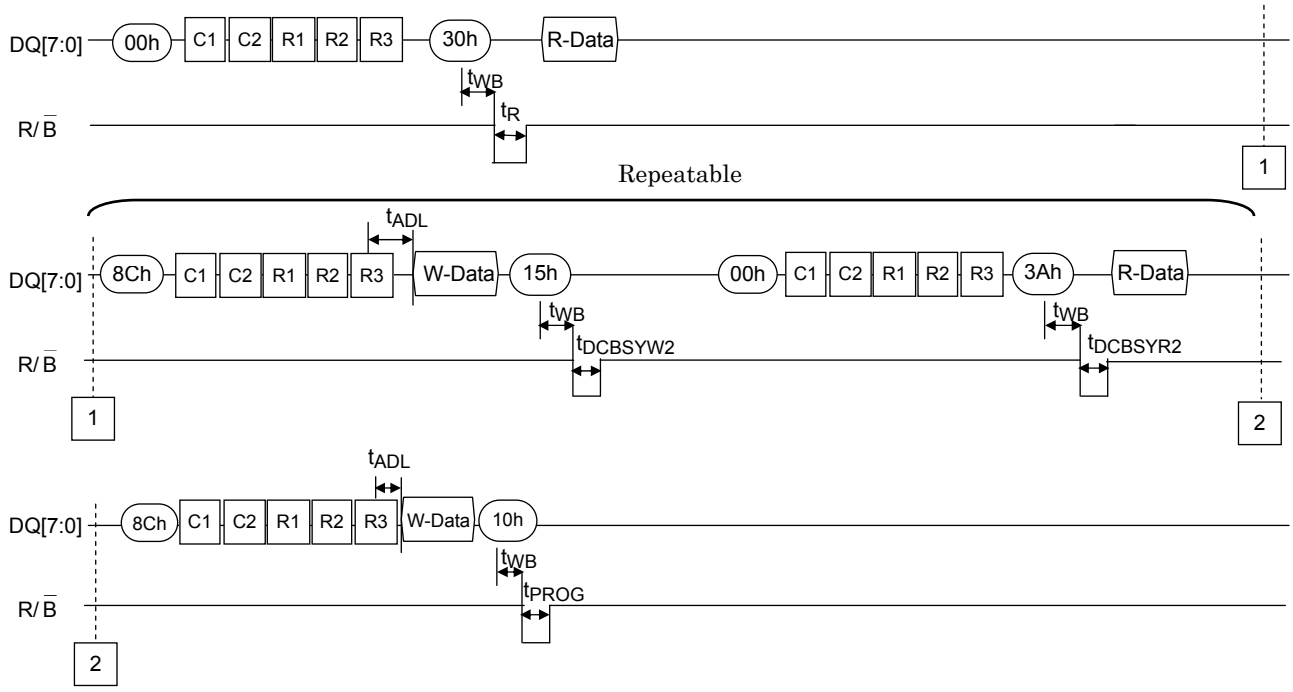


Figure 55. Example Timing with Page Copy (2)

5.3.3. Device Identification Table Read Operation

The device returns a JEDEC standard formatted parameter page during the data out phase of the READ PARAMETER PAGE command when address 40h is inputted. The READ PARAMETER PAGE command is a ECh value for the command cycle and a 40h value for the address cycle, and the bytes of the parameter page are returned in the data output (DOUT) cycles.

After the command ECh address 40h is received by the NAND device, it will go busy for a period of time (t_R in the figure) after which, the parameter page can be read from the device. The length and contents of the parameter page is to be determined (TBD). The timing associated with the bus cycles for the READ PARAMETER PAGE command is defined elsewhere in the JEDEC standard.

The READ ID command is used by the controller to identify the device that is attached. This command is used by the controller to gather information about the target flash device. Figure 56 defines the behavior and timings.

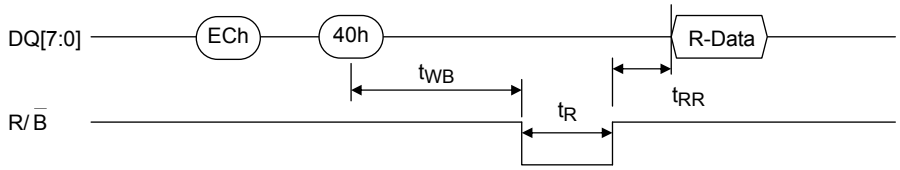


Figure 56. Device Identification Table Read Timing

5.3.4. Device Identification Table Definition

Table 44 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page.

All optional parameters that are not implemented shall be cleared to 00h by the target.

Table 44 Parameter Page Definitions

Byte	O/M	Description	Value
Revision information and features block			
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)	4Ah, 45h, 53h, 44h
4-5	M	Revision number 2-15: Reserved (0) 1: 1 = supports revision 1.0 0: Reserved (0)	02h, 00h
6-31		Reserved (0)	All 00h
Manufacturer information block			
32-43	M	Device manufacturer (12 ASCII characters) TOSHIBA	54h, 4Fh, 53h, 48h 49h, 42h, 41h, 20h 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters) TC58TEG5DCJTA00(TC58TEG5DCJTAI0)	54h, 43h, 35h, 38h 54h, 45h, 47h, 35h 44h, 43h, 4Ah, 54h 41h, 30h(49h), 30h, 20h 20h, 20h, 20h, 20h
64-69	M	JEDEC manufacturer ID (6 bytes)	98h, 00h, 00h, 00h, 00h, 00h
70-79		Reserved (0)	All 00h
Memory organization block			
80-83	M	Number of data bytes per page	00h, 40h, 00h, 00h
84-85	M	Number of spare bytes per page	00h, 05h
86-91		Reserved (0)	All 00h
92-95	M	Number of pages per block	00h, 01h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	24h, 04h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
Memory organization block			
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles	23h
102	M	Number of bits per cell	02h
103		Reserved (0)	All 00h
104	M	Multi-plane addressing 4-7: Reserved (0) 0-3: Number of plane address bits	00h
105-143		Reserved (0)	All 00h
Electrical parameters block			
144-145		Reserved (0)	All 00h
146-147	O	Toggle DDR speed grade 5-15: Reserved (0) 4: 1 = supports 10 ns speed grade (~100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz)	1Fh, 00h

		0: 1 = supports 30 ns speed grade (~33 MHz)	
148-150		Reserved (0)	All 00h
151	O	Toggle DDR features 0-7: Reserved (0)	00h
152-168		Reserved (0)	All 00h
169	M	Driver strength support 2-7: Reserved (0) 1: 1 = supports Overdrive 1 drive strength 0: 1 = supports driver strength settings	03h
170-207		Reserved (0)	All 00h
ECC and endurance block			
208-419		Reserved (0)	All 00h
Vendor specific block			
420-511		Vendor specific	Vendor specific
Redundant Parameter Pages			
512-1023		Value of bytes 0-511	Value of bytes 0-511
1024-1535		Value of bytes 0-511	Value of bytes 0-511

Byte 0-3: Parameter page signature
This field contains the parameter page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Ah.
Byte 1 shall be set to 45h.
Byte 2 shall be set to 53h.
Byte 3 shall be set to 44h.

Byte 4-5: Revision number
This field indicates the revisions of the standard that the target complies to. The target may support multiple revisions of the standard. This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.
Bit 1 when set to one indicates that the target supports revision 1.0.
Bits 2-15 are reserved and shall be cleared to zero.

Byte 32-43: Device manufacturer
This field contains the manufacturer of the device. The content of this field is an ASCII character string of twelve bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string. If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

Byte 44-63: Device model
This field contains the model number of the device. The content of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

Byte 64-69: JEDEC manufacturer ID
This field contains the JEDEC manufacturer ID for the manufacturer of the device.

Byte 80-83: Number of data bytes per page
This field contains the number of data bytes per page. The value reported in this field shall be a power of two. The minimum value that shall be reported is 512 bytes.

Byte 84-85: Number of spare bytes per page
This field contains the number of spare bytes per page. There are no restrictions on the value.

Byte 92-95: Number of pages per block
This field contains the number of pages per block.

Byte 96-99: Number of blocks per logical unit
This field contains the number of blocks per logical unit. There are no restrictions on this value.

Byte 100: Number of logical units (LUNs)
This field indicates the number of logical units the target supports. Logical unit numbers are sequential, beginning with a LUN address of zero. This field shall be greater than zero.

Byte 101: Number of Address Cycles
This field indicates the number of address cycles used for row and column addresses. The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.
Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE :
Throughout these standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

Byte 102: Number of bits per cell
This field indicates the number of bits per cell in the Flash array. This field shall be greater than zero.

Byte 104: Multi-plane addressing
This field describes parameters for multi-plane addressing.

Bits 0-3 indicate the number of bits that are used for plane addresses. This value shall be greater than 0h when multi-plane operations are supported.

Bits 4-7 are reserved.

Byte 146-147: Toggle DDR1.0 speed grade
This field indicates the Toggle DDR1.0 speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz).
Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz).
Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz).
Bit 4 when set to one indicates that the target supports the 10 ns speed grade (~100 MHz).
Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz).
Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz).
Bit 7 when set to one indicates that the target supports the 5 ns speed grade (~200 MHz).
Bits 8-15 are reserved and shall be cleared to zero.

Byte 151: Toggle DDR features
This field describes features and attributes for Toggle DDR1.0 operation. This byte is mandatory when the Toggle DDR data interface is supported.

Bits 0-7 are reserved.

Byte 169: Driver strength support
This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table TBD. If this bit is set to one, then the device shall support both the Nominal and Underdrive settings. If this bit is set to one, then the device shall power-on with a driver strength at the Nominal value defined in Table TBD. If this bit is cleared to zero, then the driver strength at power-on is undefined. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 1 when set to one indicates that the target supports the Overdrive 1 setting in Table TBD for use in the I/O Drive Strength setting. This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bits 2-7 are reserved.

Byte 420-511: Vendor specific
This field is reserved for vendor specific use.

Byte 512-1023: Redundant Parameter Page 1
This field shall contain the values of bytes 0-511 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1024-1535: Redundant Parameter Page 2
This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511 and in the first redundant parameter page. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

5.3.5. Read Status Enhanced

Read Status Enhanced function is used to check status of selected LUN and Plane specified by row address setting. Thus, the function requires row address setting steps before reading status value. Table 45 defines status values of each operation and Figure 57 defines Read Status Enhanced behavior and timings.

Table 45 Read Status Enhanced Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : “0” Not Protected : “1”
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Copy-Back	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0 is only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0 is only valid when DQ 5 shows the Ready state, and DQ 1 is only valid when DQ 6 shows the Ready state.

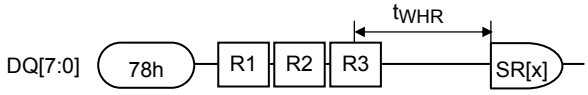


Figure 57. Read Status Timing

5.3.6. Read LUN #0 Status Operation

Read LUN#0 Status provides status value of LUN#0 without address setting. The function retrieves plane0 and plane1 status only. Table 46 defines the status values and Figure 58 defines Read LUN#0 Status behavior and timings.

Table 46 Read LUN#0 Status Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for LUN#0	Pass/Fail for Plane#0 (N)	Pass/Fail for Plane#1(N)	Pass/Fail for Plane#0 (N-1)	Pass/Fail for Plane#1(N-1)	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Copy-Back	Pass/Fail for LUN#0	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Ready/Busy	Write Protect

NOTE:

1) During Block Erase, Page Program or Copy-Back operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ 0, DQ 1 and DQ 2 are only valid when DQ 5 shows the Ready state, and DQ 3 and DQ 4 are only valid when DQ 6 shows the Ready state.

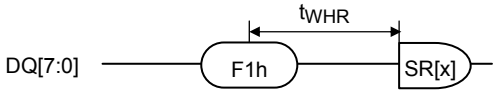


Figure 58. Read LUN#0 Status Timing

6. APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

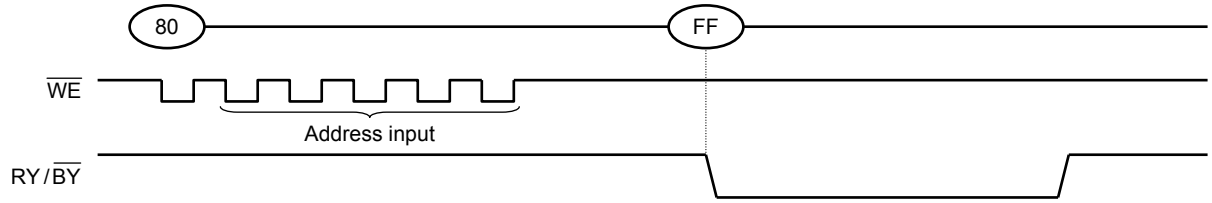
Input of a command other than those specified in this document is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Restriction of commands while in the Busy state

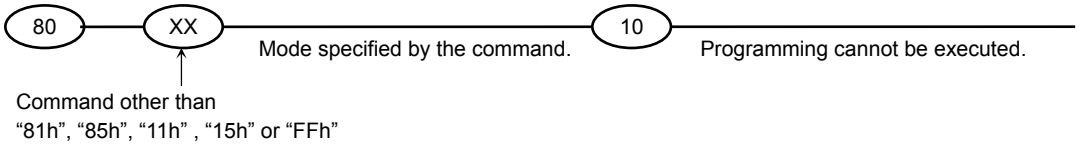
During the Busy state, do not input any command except 70h, 71h, 78h, F1h and FFh.

(3) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Multi Page Program command "81h", the Random Data Input command “85h”, Multi Page Program command “11h”, Cache Program command “15h”, the Reset command “FFh”, or Read Status commands until Page Program command “10h” is input.

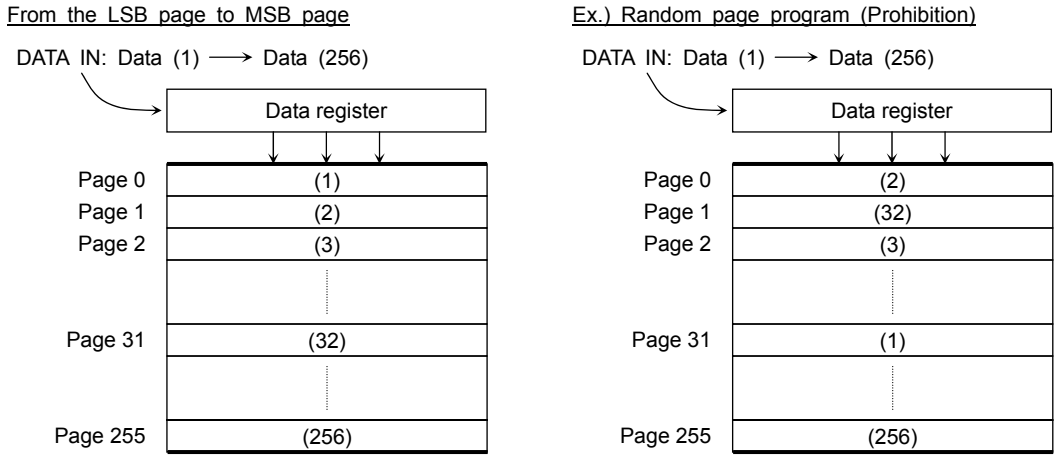


If a command other than “81h”, “85h”, “11h” , “15h”, “FFh”, or Read Status command is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

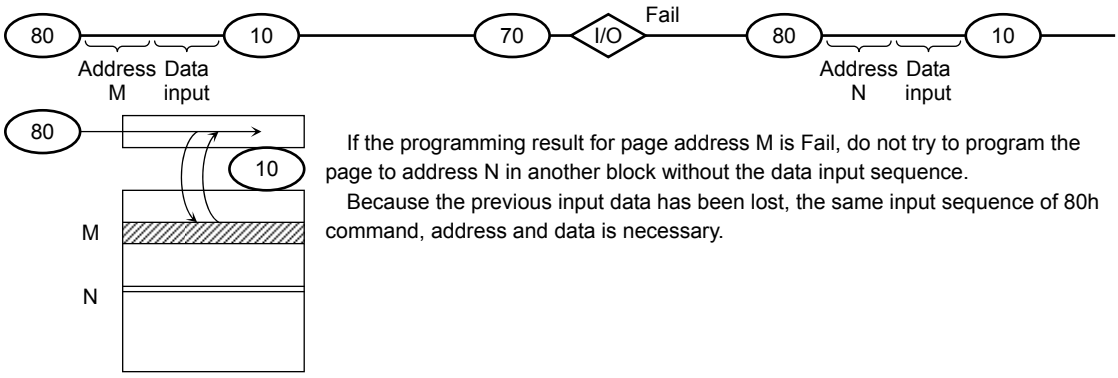


(4) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.



(5) Programming failure

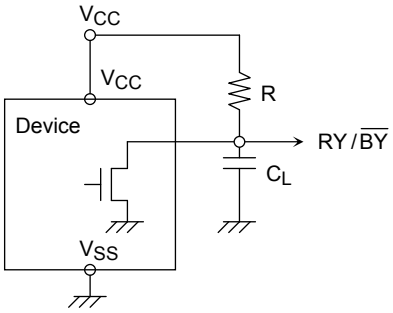


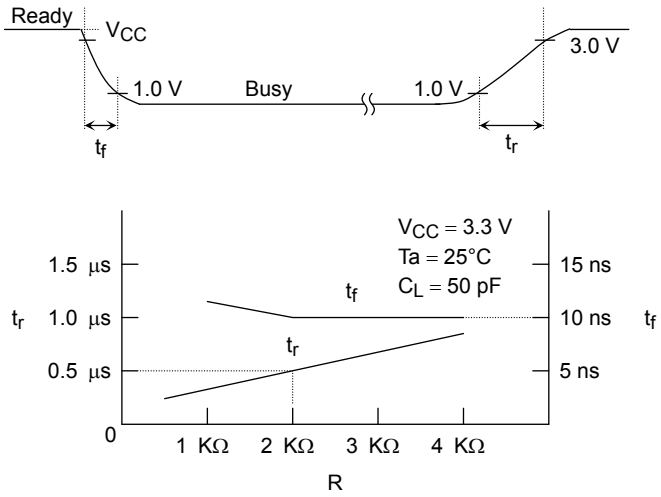
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(6) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.

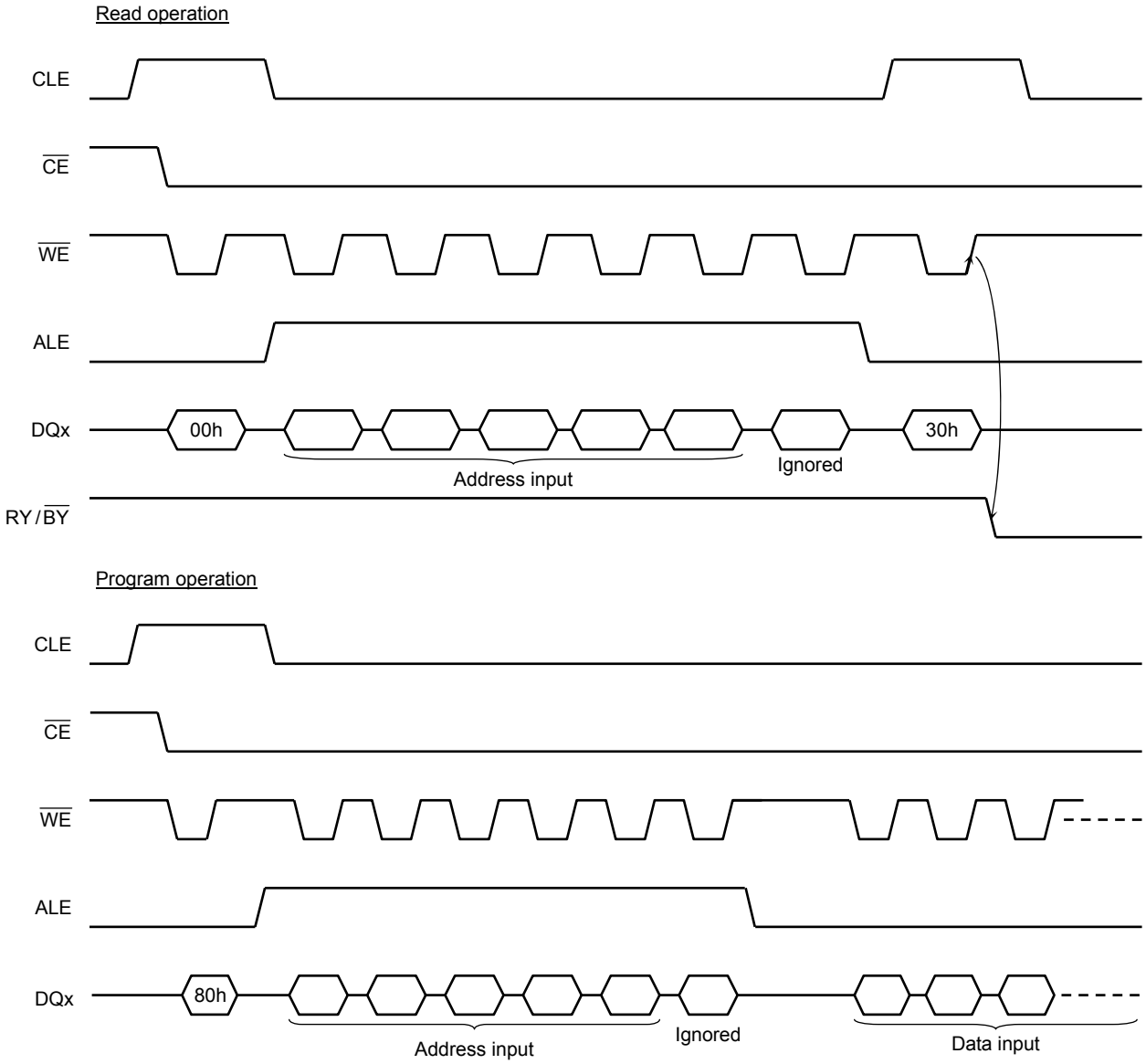




This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

(7) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

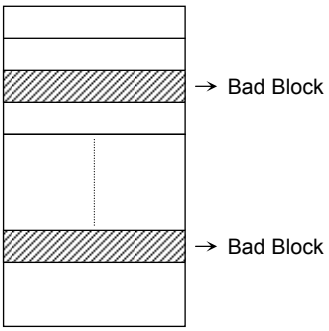


(8) Several programming cycles on the same page (Partial Page Program)

This device does not support partial page programming.

(9) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

Refer to section 2.8 for the number of valid blocks over the device lifetime.

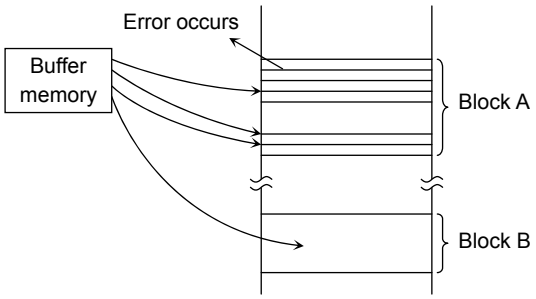
(10) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Random Bit	Programming Failure “1 to 0”	ECC

- ECC: TBD
- Block Replacement

Program



Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(11) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(12) If FF reset command is input before completion of write operation to page B, it may cause damage to data not only to the programmed page, but also to the adjacent page A as follows.

Page A	Page B	Page A	Page B
0	2	⋮	⋮
1	4	⋮	⋮
3	6	⋮	
5	8	225	228
7	10	227	230
9	12	229	232
11	14	231	234
13	16	233	236
15	18	235	238
17	20	237	240
19	22	239	242
21	24	241	244
23	26	243	246
25	28	245	248
27	30	247	250
⋮	⋮	249	252
⋮	⋮	251	254
⋮	⋮	253	255

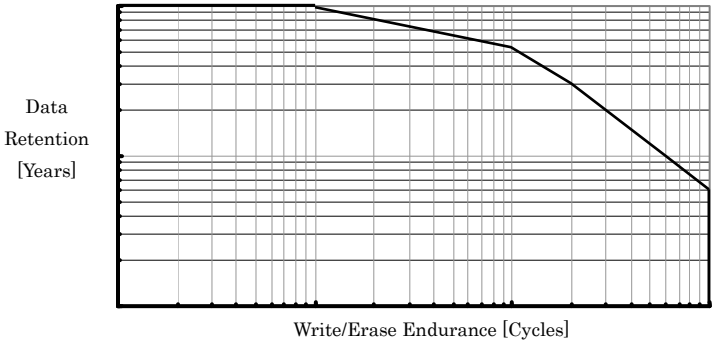
(13) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using MLC NAND flash with TBD.
For detailed reliability data, please refer to TOSHIBA's reliability note.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad.
Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The other failure modes may be recovered by a block erase.
ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

- **Write/Erase Endurance**
  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either a program or a block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- **Data Retention**
  The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

  Here is the combined characteristics image of Write/Erase Endurance and Data Retention.

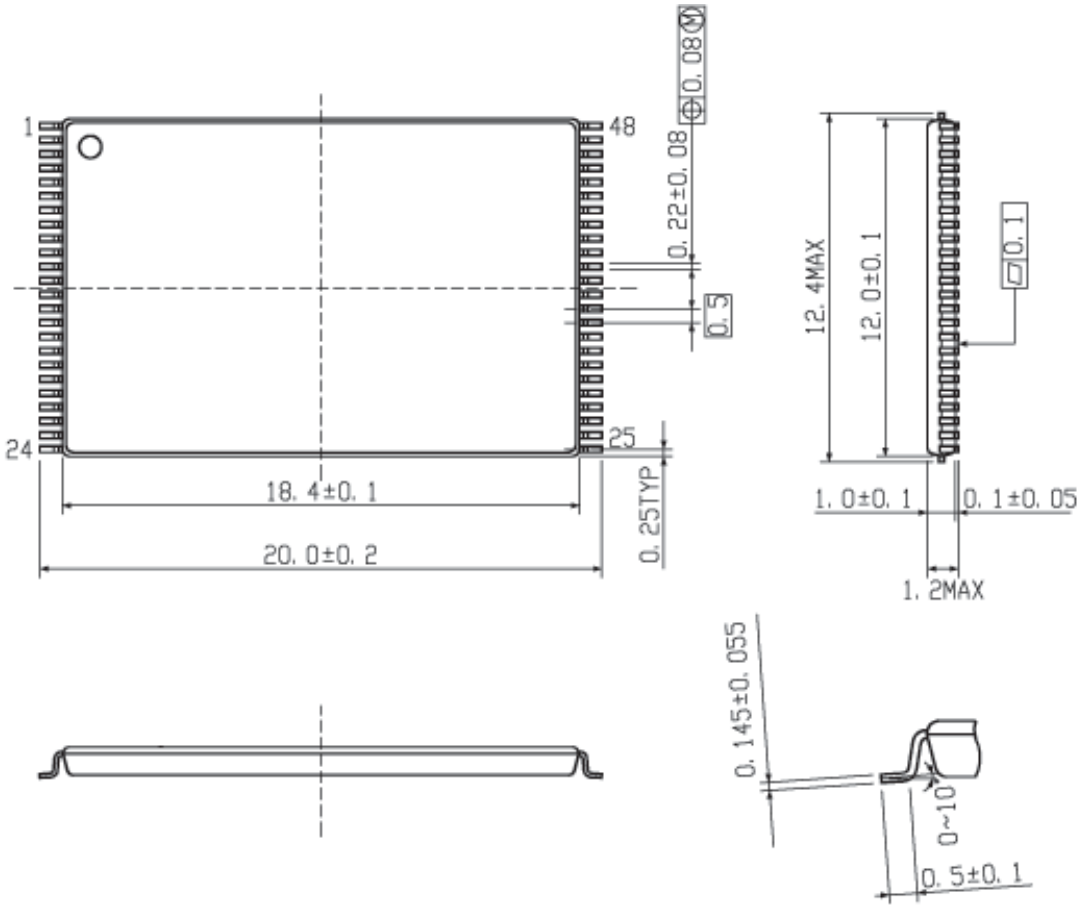


- **Read Disturb**
  A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

(14) Randomizing function

Controller shall employ randomizing function. All the columns within a page shall be filled with randomized data at programming

7. Package Dimensions



8. Revision History

Date	Rev.	Description
2012-01-26	0.0	Initial issue
2012-01-30	0.1	Clarification for the requirement of randomizing. Deleted the definition of Overdrive2 and ODT behavior.
2012-03-01	0.2	Added the definition of tRW and tRHW. Integrated SDR AC Timing table Updated Data Transfer rate Corrected 6th cycle data of 40h Address ID Definition in Read ID operation. Clarification for the address setting on Random Cache Read Operation Clarification for the requirement of randomizing

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