32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABEL READ ONLY MEMORY
SILICON STACKED GATE MOS

TC57256AD-15
TC57256AD-20

DESCRIPTION

The TC57256AD is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC 57256AD's access time is 150ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technnology reduces the maximum active current to 30 mA/6.7MHz and standby current to 100μA

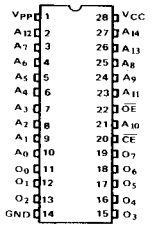
For program operation, the programming is achieved by using the high speed programming mode.

TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

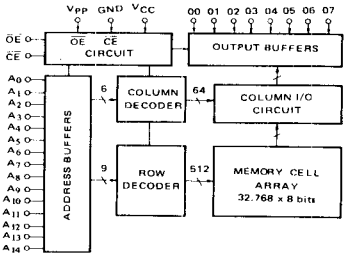
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  30mA/6.7MHZ (atcive)
  100μA (standby)
- Fast access time TC57256AD-15 150ns
  TC57256AD-20 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P EPROM i27256
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H		5V	High Impedance	
Standby	H	*		5V	High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

TOSHIBA MOS INTEGRATED CIRCUIT

TC57256AD-15, TC57256AD-20

SILICON STACKED GATE MOS

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

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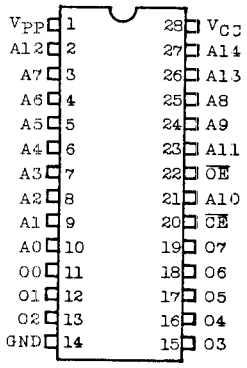
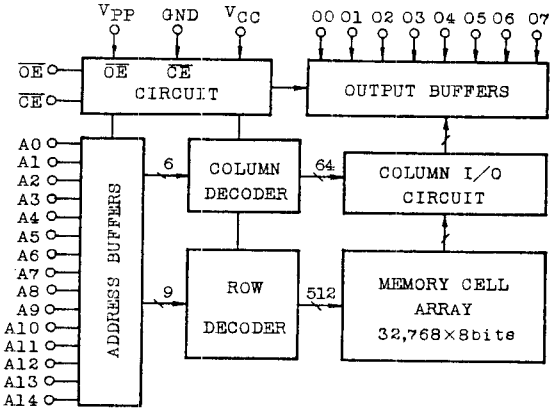
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA
- Fast access time:
  TC57256AD-15 150ns
  TC57256AD-20 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{CC}=5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ∿ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CC02}		I_{OUT}=0mA	f=1MHz	-	-	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{CC} Current	V_{PP}=V_{CC} ± 0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	

A.C. TEST CONDITIONS

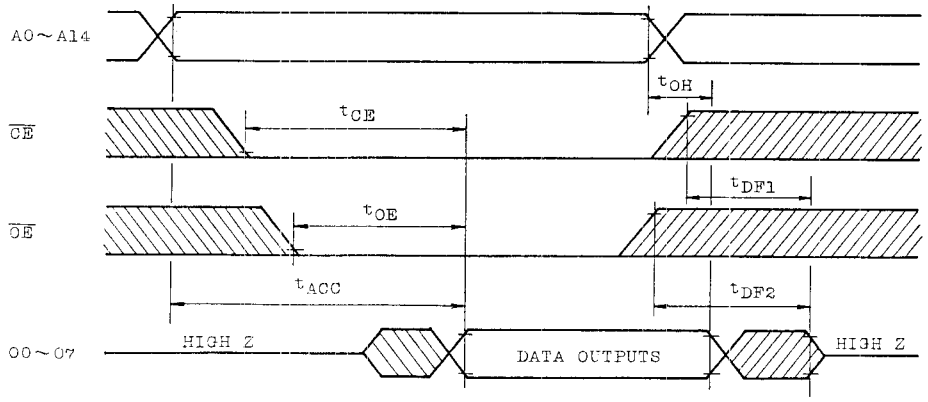
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

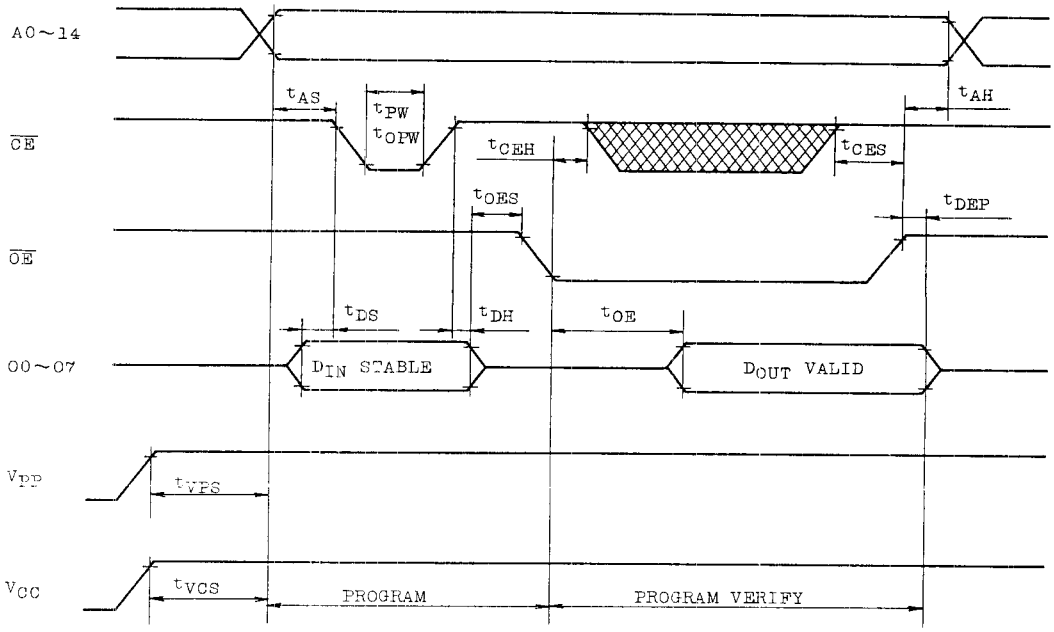
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.
Then intergrated does (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [$w \cdot sec/cm^2$].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu w/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu w/cm^2$] × (20 × 60) [sec] ≅ 15 [$w \cdot sec/cm^2$].)
The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25 ± 5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57256AD's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57256AD is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}$=V_{IH}.
The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

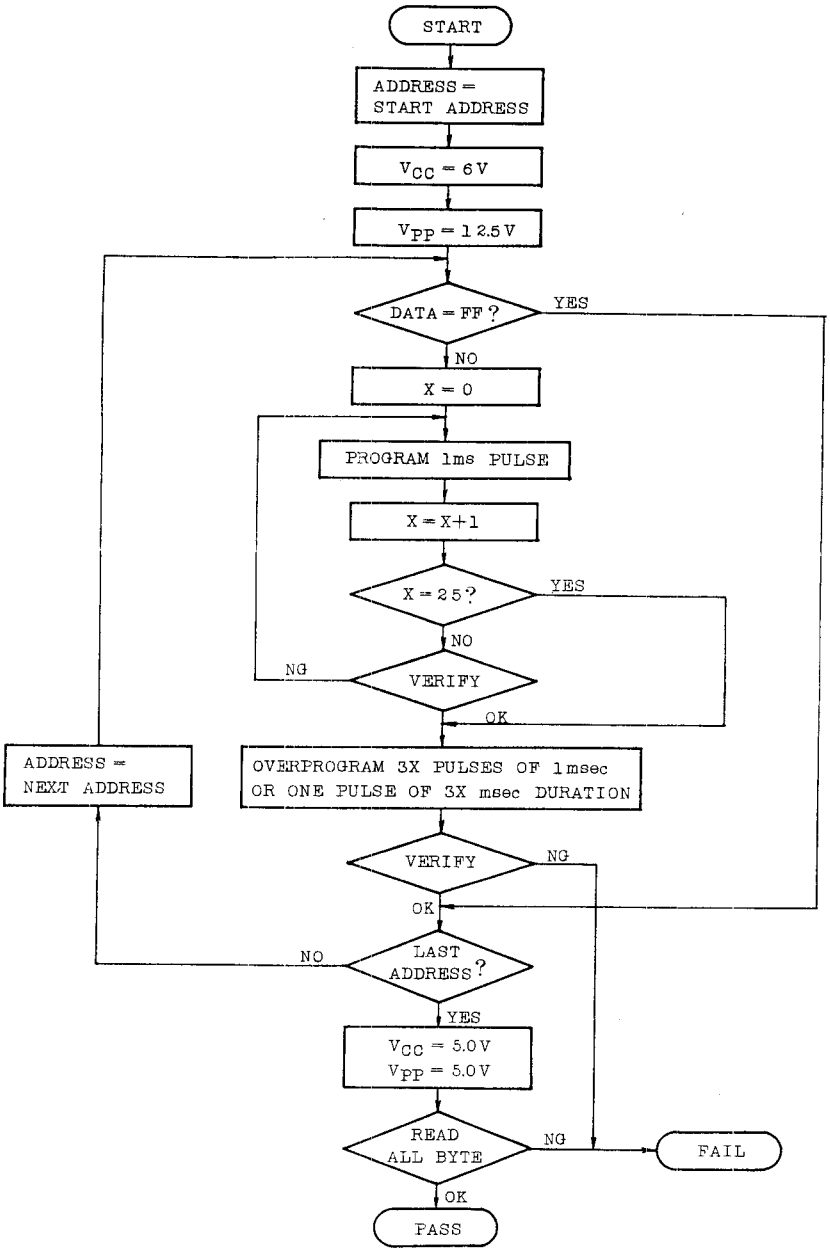
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.
Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with V_{CC}=Vpp=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electirc signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electirc signature of TC57256AD.

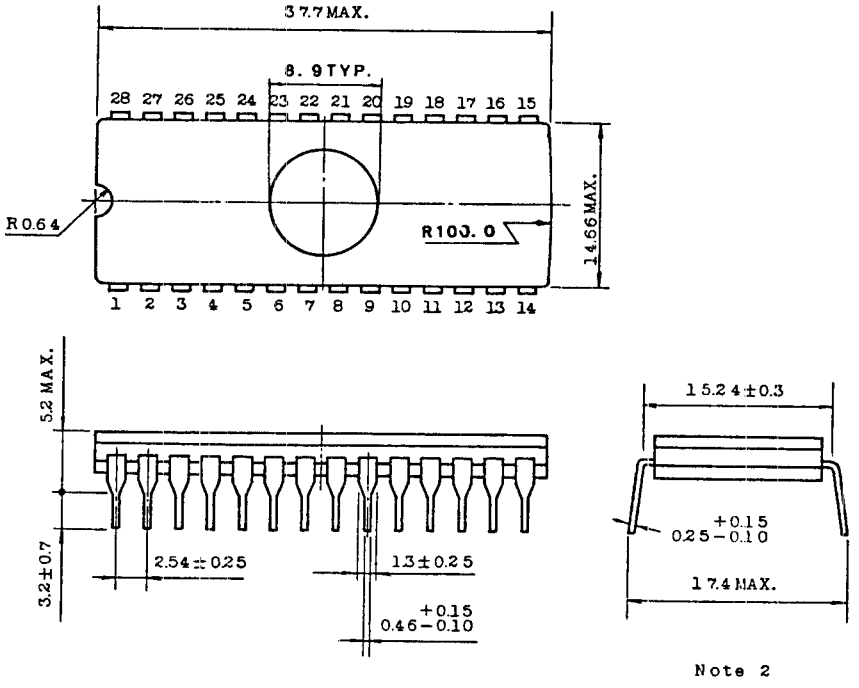
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note 1

Note 2

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.