

Toshiba BiCD process integrated circuit silicon monolithic

# TB67H401FTG

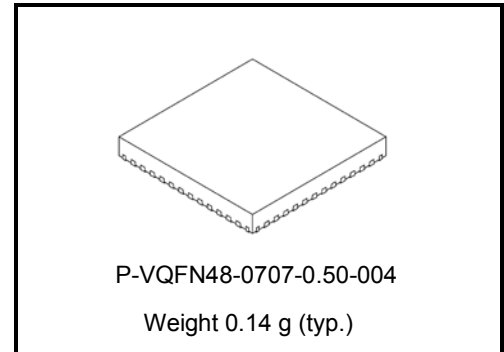
## Brushed DC Motor driver with Dual H-bridge mode

The TB67H401FTG is a brushed DC motor driver with dual integrated H-bridges. The internal H-bridges can be controlled independently.

Fabricated with the BiCD process, the TB67H401FTG is rated at 50 V, 3.0 A/ch.

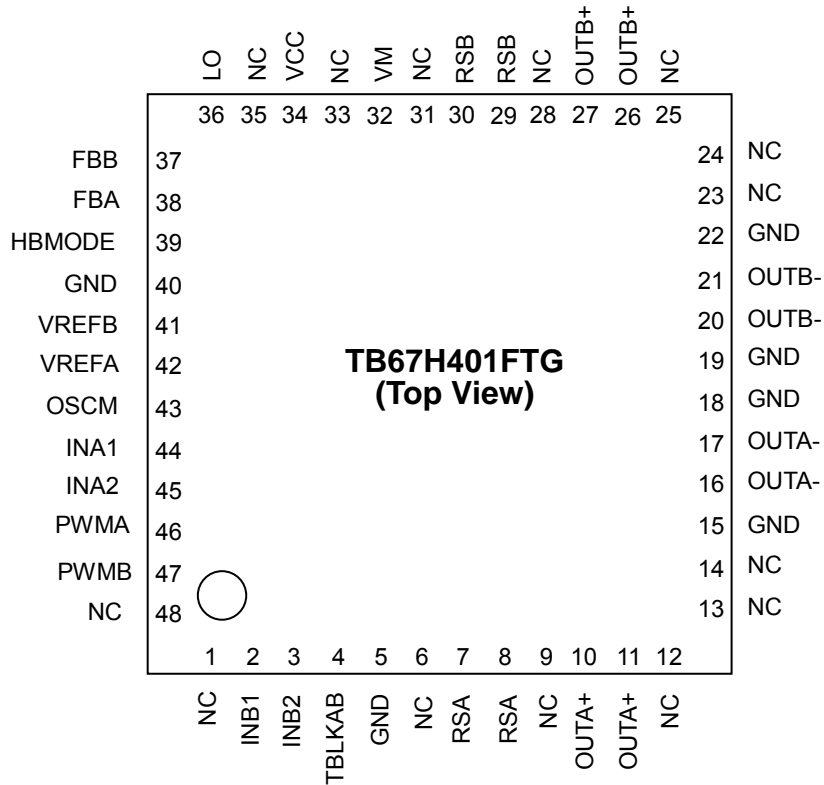
### Features

- Supporting 50 V, 3.0 A/ch 2 brushed DC motor operation
- Capable of driving two brushed DC motors using dual H-Bridge mode (3.0 A/ch)
- Capable of driving one brushed DC motor with large current, using single H-bridge mode (6.0 A)
- Current limit and current limit detection output for each H-bridge
- Low Ron (on) MOSFETs (High side + Low side=0.49  $\Omega$  (typ.), in the dual H-bridge mode)
- Error detection features (Thermal shutdown (TSD), Over current detection (ISD), Power-on-reset (POR))
- Error detection signal output (Error Output)
- Internal VCC (5 V) regulator enables the driver to be operated with a single power supply (VM)
- Adjustable internal PWM frequency using external components
- Small package with thermal pad. (QFN48: 7.0 mm x 7.0 mm)



Note: Please consider the heat condition when using the TB67H401FTG.

### Pin assignment



Note: Please solder the corner pad and the bottom thermal pad of the QFN package, to the GND pattern of the PCB.  
 Note: Pin names in the above figure are in the state when HBMODE pin is low level.

### Pin description

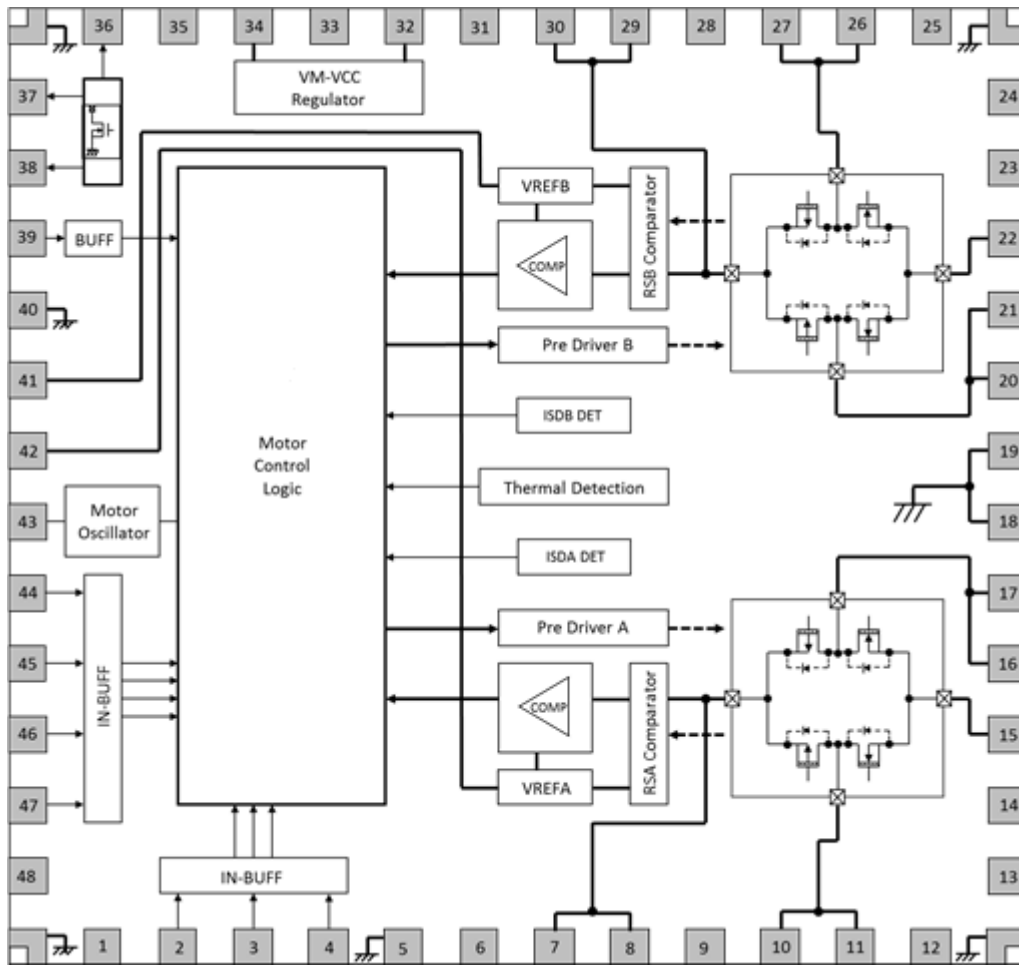
HBMODE=Low			HBMODE=High		
Pin No.	Pin name	Pin function	Pin No.	Pin name	Pin function
1	NC	Non connection	1	NC	Non connection
2	INB1	H-bridge control pin No.1 for Bch	2	NC	Non connection
3	INB2	H-bridge control pin No.2 for Bch	3	NC	Non connection
4	TBLKAB	Noise filter setting pin for constant current circuit	4	TBLK	Noise filter setting pin for constant current circuit
5	GND	Ground pin	5	GND	Ground pin
6	NC	Non connection	6	NC	Non connection
7	RSA	Current sense pin for Ach	7	RS	Current sense pin
8	RSA	Current sense pin for Ach	8	RS	Current sense pin
9	NC	Non connection	9	NC	Non connection
10	OUTA+	Motor output (+) pin for Ach	10	OUT+	Motor output (+) pin
11	OUTA+	Motor output (+) pin for Ach	11	OUT+	Motor output (+) pin
12	NC	Non connection	12	NC	Non connection
13	NC	Non connection	13	NC	Non connection
14	NC	Non connection	14	NC	Non connection
15	GND	Power ground pin for H-bridge	15	GND	Power ground pin for H-bridge
16	OUTA-	Motor output (-) pin for Ach	16	OUT+	Motor output (+) pin
17	OUTA-	Motor output (-) pin for Ach	17	OUT+	Motor output (+) pin
18	GND	Ground pin	18	GND	Ground pin
19	GND	Ground pin	19	GND	Ground pin
20	OUTB-	Motor output (-) pin for Bch	20	OUT-	Motor output (-) pin
21	OUTB-	Motor output (-) pin for Bch	21	OUT-	Motor output (-) pin
22	GND	Power ground pin for H-bridge	22	GND	Power ground pin for H-bridge
23	NC	Non connection	23	NC	Non connection
24	NC	Non connection	24	NC	Non connection
25	NC	Non connection	25	NC	Non connection
26	OUTB+	Motor output (+) pin for Bch	26	OUT-	Motor output (-) pin
27	OUTB+	Motor output (+) pin for Bch	27	OUT-	Motor output (-) pin
28	NC	Non connection	28	NC	Non connection
29	RSB	Current sense pin for Bch	29	RS	Current sense pin
30	RSB	Current sense pin for Bch	30	RS	Current sense pin
31	NC	Non connection	31	NC	Non connection
32	VM	Motor power supply pin	32	VM	Motor power supply pin
33	NC	Non connection	33	NC	Non connection
34	VCC	Internal regulator voltage monitor pin	34	VCC	Internal regulator voltage monitor pin
35	NC	Non connection	35	NC	Non connection
36	LO	Error detection flag	36	LO	Error detection flag
37	FBB	Current detection flag for Bch	37	GND	Need GND connect
38	FBA	Current detection flag for Ach	38	FB	Current detection flag
39	HBMODE	H-bridge drive mode setting pin	39	HBMODE	H-bridge drive mode setting pin
40	GND	Ground pin	40	GND	Ground pin
41	VREFB	Current threshold reference pin for Bch	41	GND	Need GND connect
42	VREFA	Current threshold reference pin for Ach	42	VREF	Current threshold reference pin
43	OSCM	Internal oscillator frequency setting pin	43	OSCM	Internal oscillator frequency setting pin
44	INA1	H-bridge control pin No.1 for Ach	44	IN1	H-bridge control pin No.1
45	INA2	H-bridge control pin No.2 for Ach	45	IN2	H-bridge control pin No.2
46	PWMA	Short brake pin for Ach	46	PWM	Short brake pin
47	PWMB	Short brake pin for Bch	47	NC	Non connection
48	NC	Non connection	48	NC	Non connection

Note: Please do not connect any PCB pattern to the NC pins.

Note: For pins with the same pin name; tie the pins together at the nearest point of the IC.

Note: Some pin names are written differently depending on the state of HBMODE. Hereafter, they are unified in the state when HBMODE is low level.

## Block diagram



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Note: When using TB67H401FTG, the GND pattern of PCB should be a solid pattern and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.

Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, GND, OUT+, OUT-) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

## Input/Output equivalent circuit 1

Pin name	Input/Output signal	Input/Output equivalent circuit
TBLKAB HBMODE PWMA PWMB INA1 INA2 INB1 INB2	Logic input pin voltage $0\text{ V} \leq V_{IN(L)} \leq 0.8\text{ V}$ $2.0\text{ V} \leq V_{IN(H)} \leq 5.5\text{ V}$	<p>Logic input pin</p> <p>1 kΩ</p> <p>100 kΩ</p> <p>GND</p>
FBA FBB LO	Logic output pin $0\text{ V} \leq V_{O(L)} \leq 0.5\text{ V}$ $4.5\text{ V} \leq V_{O(H)} \leq 5.5\text{ V}$	<p>Logic output pin</p> <p>10 kΩ to 100 kΩ</p> <p>VCC</p>
OSCM	OSCM frequency range $0.64\text{ MHz} \leq f_{OSCM} \leq 2.4\text{ MHz}$	<p>VCC</p> <p>OSCM</p> <p>1 kΩ</p> <p>500 Ω</p>

The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

## Input/Output equivalent circuit 2

Pin name	Input/Output signal	Input/Output equivalent circuit
VCC VREFA VREFB	VCC voltage range $4.75\text{ V} \leq VCC \leq 5.25\text{ V}$  VREF input voltage range $GND \leq VREF \leq 4.0\text{ V}$	
OUTA+ OUTA- OUTB+ OUTB- RSA RSB	VM operation voltage range $10\text{ V} \leq VM \leq 47\text{ V}$  Output pin voltage range $10\text{ V} \leq VM \leq 47\text{ V}$	

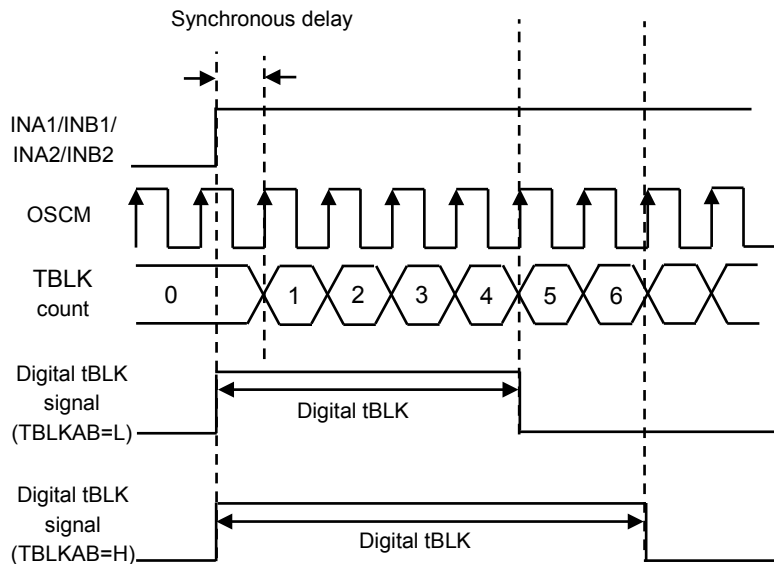
The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

## ◆Motor control functions

### 1. TBLKAB function

This pin will set the noise rejection time.

TBLKAB	TBLK noise rejection time
L	Digital tBLK = tOSCM × 4 clk
H	Digital tBLK = tOSCM × 6 clk



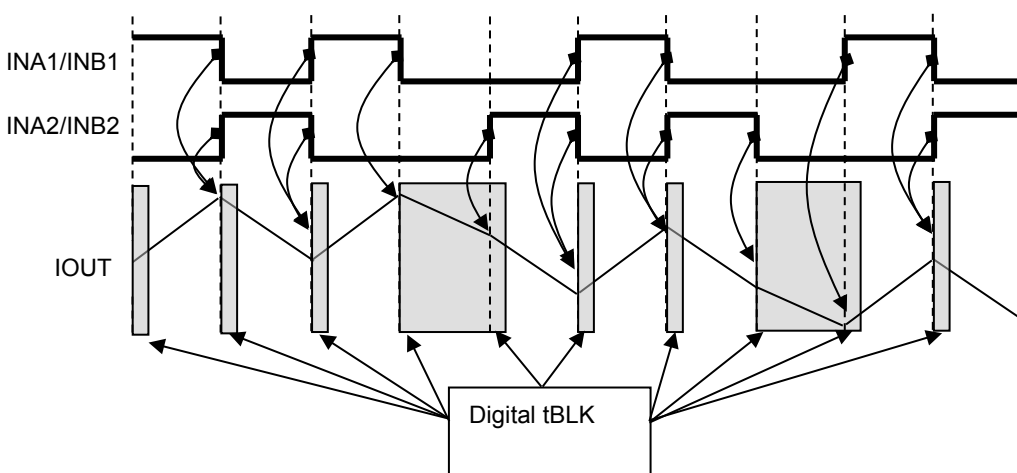
Please note that the timing charts or constants may be omitted or simplified for explanatory.

\* The Digital tBLK is used to avoid error judgment of varistor recovery current that occurs in charge drive mode when H-bridges are used with DC motors. The Digital tBLK time can be controlled with TBLKAB pin.

By setting Digital tBLK, direct PWM control and constant current control is possible, but the motor current will rise above the predefined current level (NF) while digital tBLK is active.

\* Besides Digital tBLK, Analog tBLK (400 ns (typ.)) settled by an internal constant of IC is also attached.

#### • Digital tBLK timing for Brushed DC Motor



The Digital tBLK is inserted at the beginning of each charge period of the constant current chopping, and also when either of INA1, INA2, INB1, or INB2 is switched.

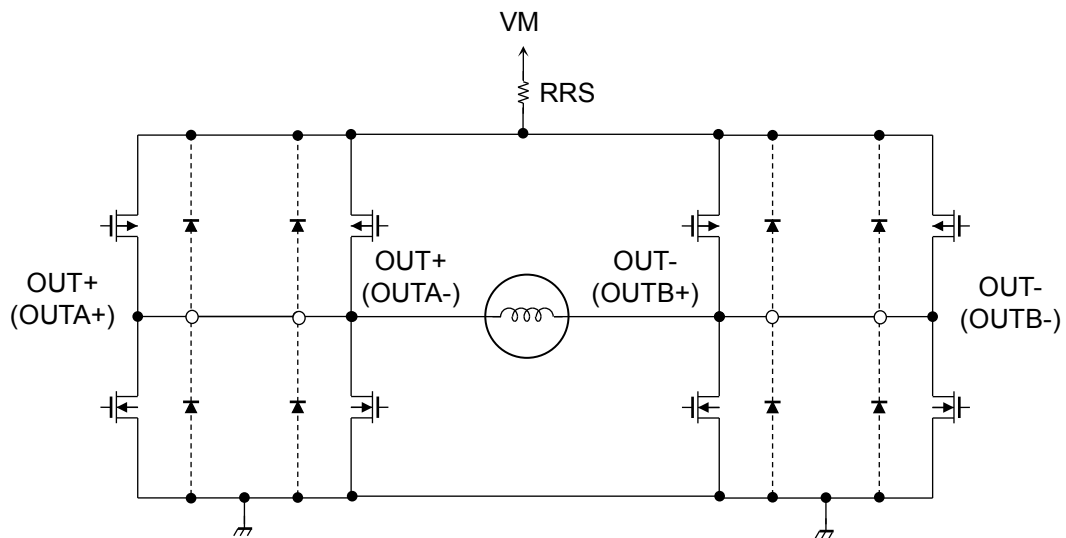
Please note that the timing charts or constants may be omitted or simplified for explanatory.

## 2. HBMODE function

Driving mode of the motor output is set by the HBMODE pin.

HBMODE	Function
High (connect to VCC )	Single H-bridge mode (Two H-bridges are controlled in parallel as one H-bridge.)
Low (connect to GND)	Dual H-bridge mode (Two H-bridges are controlled individually.)

### HBMODE=High (Single H-bridge mode)



### H-bridge function

PWM	IN1	IN2	OUT+	OUT-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	Standby
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW (Reverse rotation)
	High	High	Low	Low	Short brake

Note: When using the single H-bridge mode, the impedance within the PCB layout should be balanced. Also, there are multiple pins with the same pin name. For these pins (like VM, OUT+, OUT-, GND, RS, etc.) same named pins should be connected to each other.

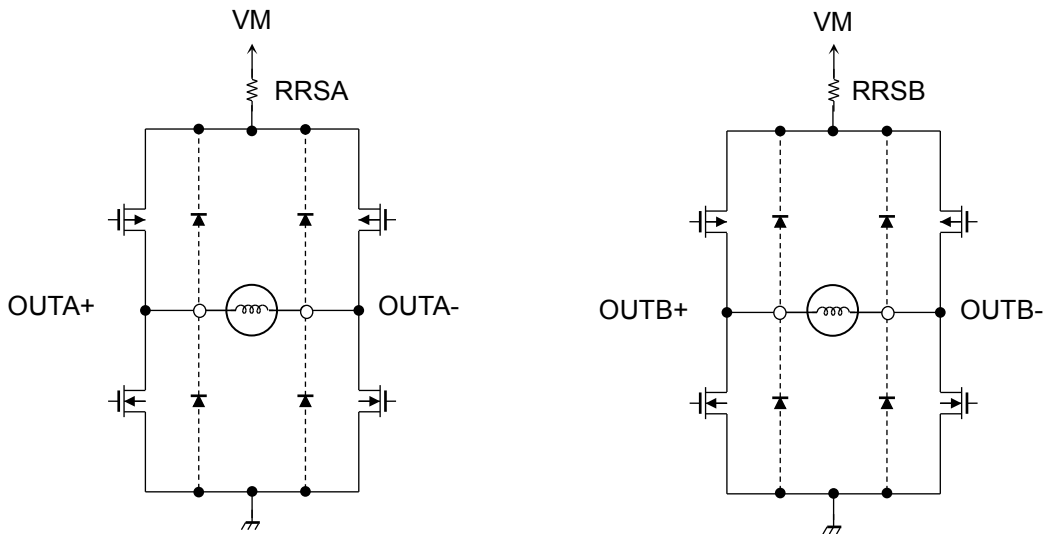
Note: The logic input level of the HBMODE pin cannot be switched during operation. Therefore when setting the HBMODE pin to high, connect to the VCC, and when setting it to low, connect to the GND by PCB pattern. Switching the HBMODE pin while the motor is operating may damage or destroy the device and the motor.

Note: Control pins are different depending on the HBMODE pin setting. For details, please refer to the section '3. INA1/INB1, INA2/INB2, and PWMA/PWMB functions'.

Note: The internal circuits are designed to avoid EMF or leakage current; when the logic signal is applied while the VM is not. Please consider the control signal timing before supplying the VM.



**HBMODE=Low (Dual H-bridge mode)**



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3. INA1/INB1, INA2/INB2, and PWMA/PWMB functions

H-bridges are controlled by INA1/INB1, INA2/INB2, and PWMA/PWMB pins. When HBMODE pin is set to high, both H-bridges are controlled by INA1, INA2, and PWMA pins; the INB1, INB2, and PWMB pins will be invalid (Don't care). When HBMODE is set to low, H-bridge Ach is controlled by INA1, INA2, and PWMA pins, and H-bridge Bch is controlled by INB1, INB2, and PWMB pins.

#### H-bridge (Ach) function

PWMA	INA1	INA2	OUTA+	OUTA-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW (Reverse rotation)
	High	High	Low	Low	Short brake

#### H-bridge (Bch) function

PWMB	INB1	INB2	OUTB+	OUTB-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW (Reverse rotation)
	High	High	Low	Low	Short brake

Note: When INA1, INA2, and PWMA are set to low, output pin of a H-bridge (Ach) will be Hi-Z. When INB1, INB2, and PWMB are set to low, output pin of a H-bridge (Bch) will be Hi-Z. The standby mode is only enabled when all 6 logic inputs (INA1, INA2, PWMA, INB1, INB2, and PWMB) are set to low. (When HBMODE pin is set to high, the standby mode will be enabled by setting all 3 inputs, INA1, INA2, and PWMA, to low.)

### 3-1. INA1/INB1, INA2/INB2, and PWMA/PWMB setting examples

There are 3 control signals (INA1/INB1, INA2/INB2, PWMA/PWMB) for each H-bridges, but will basically require only 1 or 2 signals to control each motor. Below are few examples of how you should control the motor using the control signals.

1 signal control. (ex. single direction control, forward rotation)

#### H-bridge function

PWMA/PWMB	INA1/INB1	INA2/INB2	OUTA+/OUTB+	OUTA-/OUTB-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	Tie to VCC	Tie to GND	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	Tie to VCC	Tie to GND	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW(Reverse rotation)
	High	High	Low	Low	Short brake

If you only need to rotate the motor in a single direction, tie the INA1/INB1 to VCC and INA2/INB2 to GND and switch only the PWMA/PWMB pin. This will allow a single signal control of the motor.

2 signal control. (ex. both direction control, forward/reverse rotation)

#### H-bridge function

PWMA/PWMB	INA1/INB1	INA2/INB2	OUTA+/OUTB+	OUTA-/OUTB-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
Tie to VCC	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW(Reverse rotation)
	High	High	Low	Low	Short brake

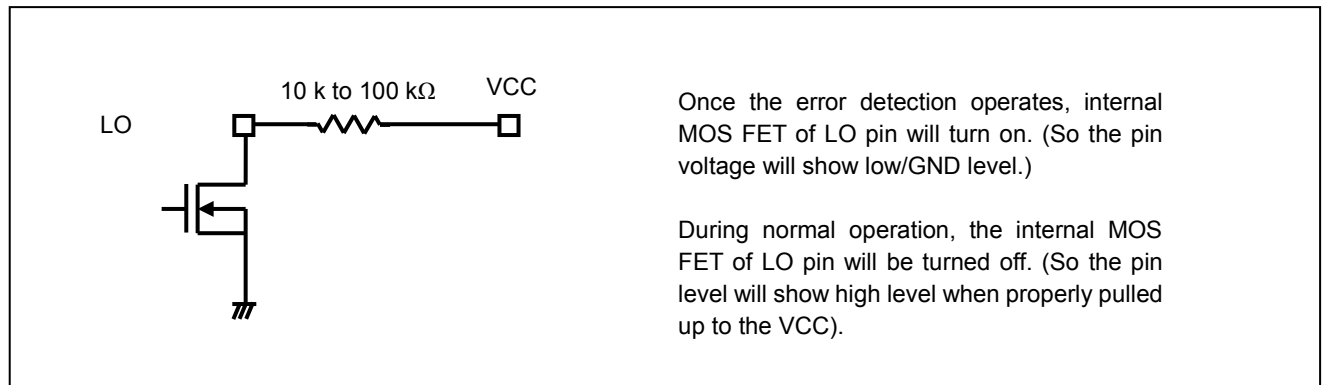
If you need to rotate the motor for both direction (forward and reverse), tie the PWMA/PWMB pin to VCC and switch the INA1/INB1 and INA2/INB2 pins for Forward/Reverse/Stop and Brake.

**4. LO (Logic Output: error detect signal output) function**

The LO pin signals the MCU/CPU that the TB67H401FTG has detected either the over current (ISD) or the over thermal (TSD) condition. The LO pin is an open drain pin, so it needs to be pulled up to the VCC, for proper usage. Use a pull-up resistor in the range of 10 k to 100 kΩ. The pin will stay High when the TB67H401FTG is operating normally, and once it detects over current (ISD) or over thermal (TSD), the pin will show Low level.

Once the error status is released by reasserting the VM or using the standby mode, LO pin will show “normal operation” status. (Leave the pins open if this function is not used.)

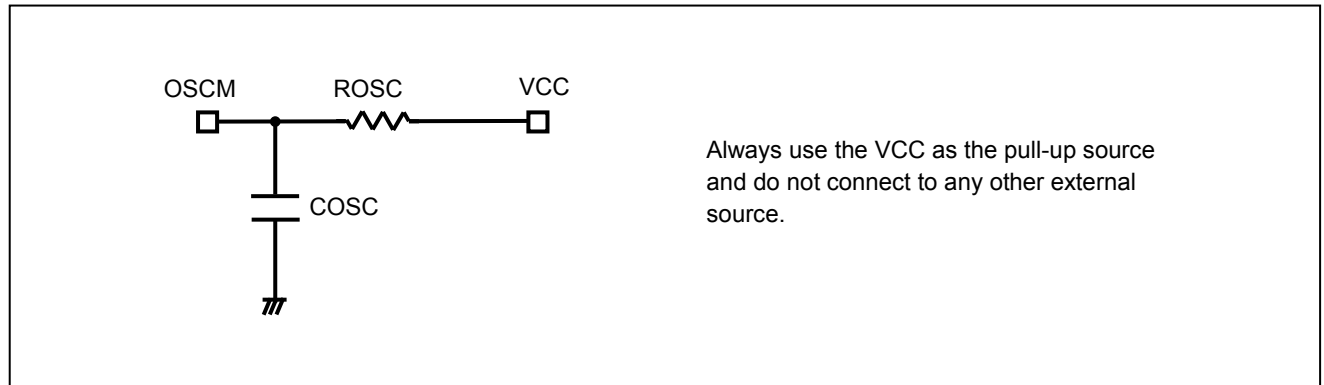
LO	Function
VCC	Normal status (Normal operation)
Low	Detected over current (ISD) or over thermal (TSD)



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**5. OSCM (internal oscillator) function**

OSCM pin is used to adjust the internal oscillator frequency for constant current PWM control. The values of the resistor and the capacitor connected to OSCM pin will set the internal oscillator frequency. Use the VCC to connect the ROSC to OSCM pin, and do not connect to any other external power source.



The equivalent circuit diagrams may be omitted for explanatory purposes.

Note: The oscillator frequency will be set by resistor (ROSC) and capacitor (COSC). When adjusting the frequency, set the COSC to 270 pF, and change the value of the ROSC resistor. For details, please refer to the following descriptions.

## OSCM oscillator frequency (chopping frequency) calculation

OSCM oscillator frequency can be calculated by using the external component values (ROSC and COSC), and the formula shown below. (This is only effective when the COSC is set to 270 pF.)

$$f_{OSCM} = 4.0 \times ROSC^{-0.8}$$

COSC and ROSC are external components required to set the oscillator frequency. To adjust the oscillator frequency, use 270 pF for COSC and change the value of ROSC.

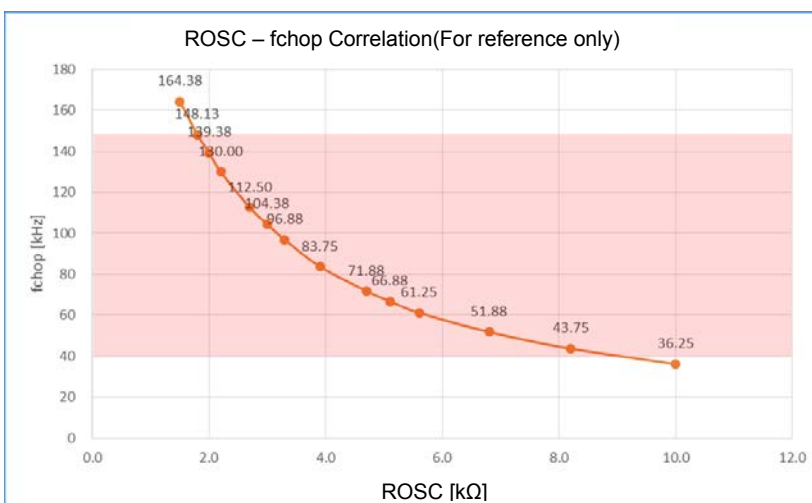
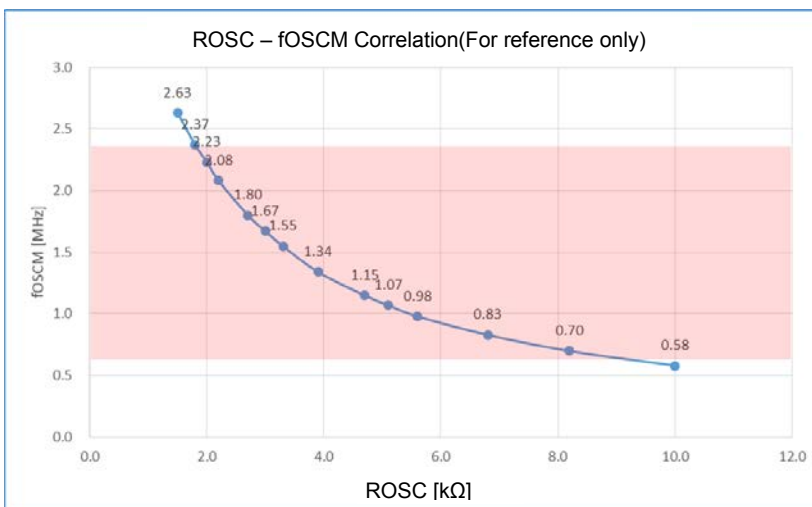
The correlation between the PWM chopping frequency (fchop) and the OSCM oscillator frequency (fOSCM) is as shown below.

$$f_{chop} = f_{OSCM} / 16$$

For normal operation, setting the frequency in the range of 50 kHz to 70 kHz and adjust by usage conditions if needed.

When the chopping frequency is set to high, the current ripple becomes smaller, which leads to a higher reproducibility of a waveform. However, the chopping frequency per unit time is increased and so the gate loss and the switching loss of the integrated MOSFET become larger, which leads to an additional heat generation. On the other hand, when the chopping frequency is set to low, the current ripple becomes larger but the heat generation is reduced. Please set the frequency according to the usage conditions and environment.

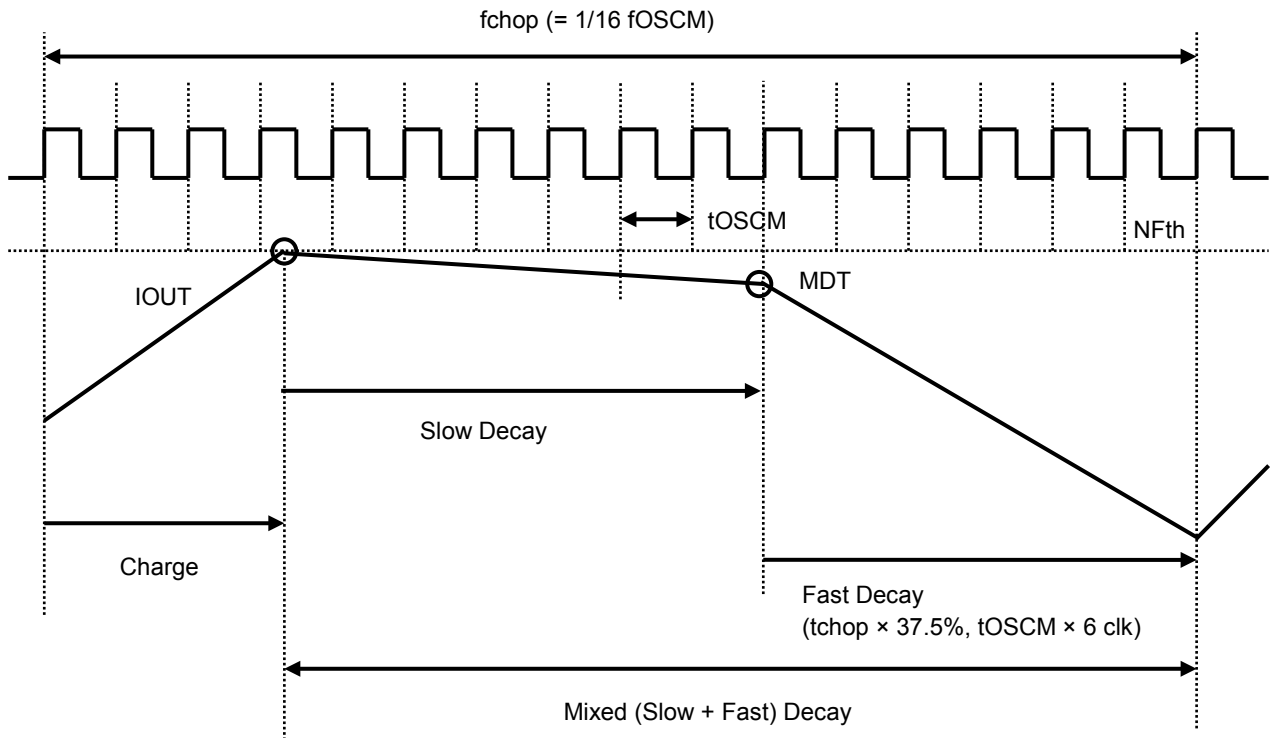
Note: Please see the correlation graph shown below, between the ROSC - fOSCM, and ROSC - fchop for reference. (The COSC capacitor value is set to 270 pF.)



**6. Current limit (Internal PWM / Mixed Decay) control**

**Current limit (Internal PWM / Mixed Decay) control**

The TB67H401FTG has a current limit (Internal PWM / Mixed Decay) control capability which monitors the motor current during PWM control, and limits the current to avoid exceeding the set threshold in a Mixed Decay manner.



Timing charts may be simplified for explanatory purposes.

The internal PWM cycle is a loop of Charge → Slow Decay → Fast Decay → Charge → ... to keep the peak current below the NF threshold (NFth). The chopping frequency (fchop) is a period of 16 counts per cycle of OSCM oscillator frequency (fOSCM). The sequence of Charge, Slow Decay, and Fast Decay is basically switched within this fchop cycle.

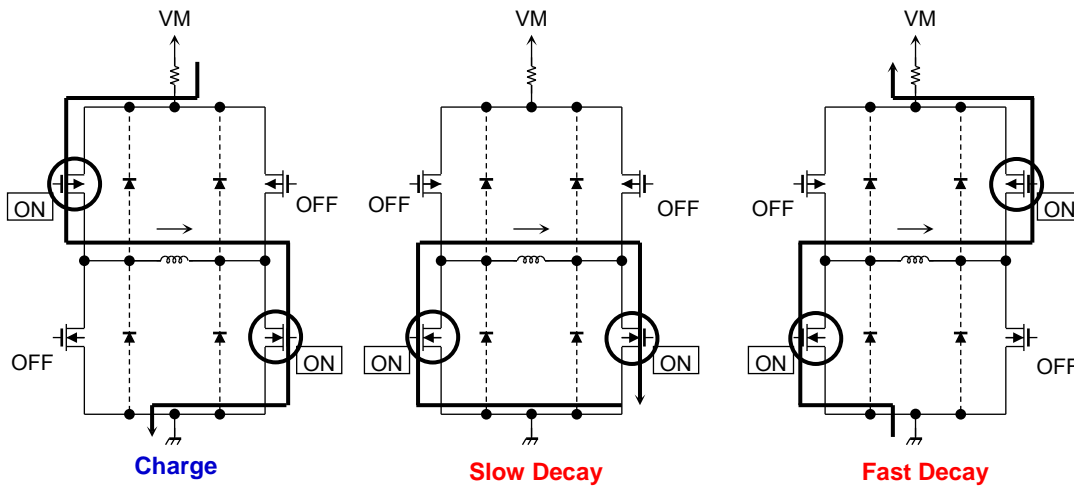
First, the current flows in from the power supply to the motor through the H-bridge (Charge) until it reaches the current limit threshold (NFth), which is set by VREF and sense resistor (RRS). Once the motor current reaches NFth, the H-bridge will switch to Slow Decay mode (gradual discharge mode) until it is at the MDT (Mixed Decay Timing).

The MDT is a fixed value, which is set for the last 6 counts of each PWM cycle. Once it reaches the MDT, the H-bridge will then switch to Fast Decay mode and recirculates the current back to the power supply for the rest of the fchop cycle.

If the motor current reaches NFth, and the time left within that fchop cycle is less than  $t_{OSCM} \times 6 \text{ clk}$  ( $t_{chop} \times 37.5\%$ ), the Slow Decay sequence will be skipped, and the H-bridge will switch directly to Fast Decay mode and will continue for the rest of the fchop cycle.

The internal PWM cycle is completely asynchronous to the external PWM, but the external signal has the higher priority so it can be switched regardless of the internal PWM cycle.

## Motor output MOSFET switching sequence



\* The TB67H401FTG has a 400ns (design target, fixed value) dead time to avoid any flow-through current during switching.

The equivalent circuits may be simplified or omitted for explanatory purposes.

## Current limit threshold calculation (for each H-bridge)

The current limit threshold is set by the VREF voltage and the value of the sense resistor (RRS).

$$I_{OUT} = V_{REF} \times 0.2 \times 1/RRS$$

Example: When the VREF voltage is set to 2.0 V and the current sense resistor (RRS) is 0.22 Ω, the current limit threshold is calculated as follows.

$$I_{OUT} = 2.0 \times 0.2 \times 1/0.22 = 1.82 \text{ A}$$

### Absolute maximum ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	VM	50	V	—
Motor output voltage	VOUT	50	V	—
Motor output current	IOUT(SHB)	6.0	A	(Note1)
	IOUT(DHB)	3.0	A/ch	(Note2)
Internal Logic power supply	VCC	6.0	V	—
Logic input voltage	VIN(H)	6.0	V	—
	VIN(L)	-0.4	V	—
LO output voltage	VLO	6.0	V	—
LO Inflow current	ILO	6.0	mA	—
Power dissipation	PD	1.3	W	(Note3)
Operating temperature	Topr	-20 to 85	°C	—
Storage temperature	Tstg	-55 to 150	°C	—
Junction temperature	Tj (max)	150	°C	—

Note1: When HBMODE pin is set to high. Please make sure that the peak current level of each H-bridge is kept under 3.0 A at all times. Also, calculate the generating heat and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

Note2: When HBMODE pin is set to low. Please make sure that the current level of each H-bridge is kept under 3.0 A at all times. Also, calculate the generating heat and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

Note3: Device alone (Ta = 25°C)

Ta: Ambient temperature

Topr: Ambient temperature while the IC is active

Tj: Junction temperature while the IC is active. Tj (max) is limited by the thermal shutdown (TSD) threshold.

Please set the usage conditions so that the peak Tj is kept under 120°C for indication.

### Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. All voltage ratings, including supply voltages, must always be followed. Other notes and considerations described in the datasheet should also be referred to.

### Operation ranges (Ta=-20 to 85°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	10	24	47	V	—
Motor output current	IOUT(SHB)	—	3.0	6.0	A	(Note1)
	IOUT(DHB)	—	1.5	3.0	A/ch	(Note2)
LO output voltage	VLO	—	3.3	VCC	V	—
Chopping frequency	fchop (range)	40	70	150	kHz	—
VREF input voltage	VREF	GND	2.0	4.0	V	—

Note1: When HBMODE pin is set to high. Please make sure that the peak current level of each H-bridge is kept under 3.0 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

Note2: When HBMODE pin is set to low. Please make sure that the current level of each H-bridge is kept under 3.0 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

## Electrical characteristics 1 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage	HIGH	VIN(H)	High level (Note)	2.0	—	5.5	V
	LOW	VIN(L)	Low level (Note)	0	—	0.8	V
Logic input hysteresis voltage		VIN(HYS)	Hysteresis voltage	0.1	—	0.3	V
Logic input current	HIGH	IIN(H)	Input voltage = 3.3 V	—	33	—	μA
	LOW	IIN(L)	Input voltage = 0 V	—	—	1	μA
Logic output pin voltage (FBB,FBA,LO)	HIGH	VO(H)	IOL = 5 mA LO = Low (10 kΩ,5V Pull Up)	4.5	4.8	5.5	V
	LOW	VO(L)		0	0.2	0.5	V
Current consumption		IM1	Standby mode	—	2	—	mA
		IM2	OUT: OPEN, INA1, INA2, INB1, and INB2: Low, Standby mode: Release	—	3.5	5.5	mA
		IM3	OUT: OPEN, Standby mode: Release	—	5.5	7	mA
Output leakage current	High-side	IOH	VM = 50 V, VOUT = 0 V	—	—	1	μA
	Low-side	IOL	VM = VOUT = 50 V	1	—	—	μA
Motor current channel differential		ΔIOUT1	Current differential between channels	-5	0	5	%
Motor current setting differential		ΔIOUT2	IOUT = 1.6 A, HBMODE = Low	-5	0	5	%
Motor output ON-resistance (High-side + Low-side)		Ron(H+L)	Tj = 25°C, Forward direction (High side + Low side)	—	0.49	0.6	Ω

Note: VIN(H) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when a pin under test is gradually raised from 0 V. VIN(L) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when the pin is then gradually lowered. The difference between VIN(H) and VIN(L) is defined as the VIN(HYS).



### Electrical characteristics 2 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
VREF input current	IREF	VREF = 2.0 V	—	0	1	μA
VCC voltage	VCC	ICC = 5.0 mA	4.75	5.0	5.25	V
VCC current	ICC	VCC = 5.0 V	—	2.5	5.0	mA
VREF gain	VREF(gain)	VREF = 2.0 V, HBMODE = Low	1/5.2	1/5.0	1/4.8	—
Thermal shutdown (TSD) threshold (Note1)	TjTSD	—	145	160	175	°C
VM power-on-reset threshold	VMPOR	Power-on-reset release	7.0	8.0	9.0	V
Over current detection (ISD) threshold (Note2)	ISD	—	4.1	4.9	5.7	A

#### Note1: Thermal shutdown (TSD)

When the TB67H401FTG detects an over temperature, the internal circuit turns off the output MOSFETs. Noise filter is built in to avoid TSD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode (INA1, INA2, INB1, INB2, PWMA, PWMB = Low) to restart the device. The TSD is triggered when the device is over heated irregularly. Make sure not to use the TSD function aggressively.

#### Note2: Over current detection (ISD)

When the TB67H401FTG detects an over current, the internal circuits turns off the output MOSFETs. Noise filter is built in to avoid ISD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode (INA1, INA2, INB1, INB2, PWMA, PWMB = Low) to restart the device. The ISD is triggered when the motor current is over rated irregularly. Make sure not to use the ISD function aggressively.

#### Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB67H401FTG or other components will be damaged or fail due to the motor back-EMF.

#### Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.

If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.

The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

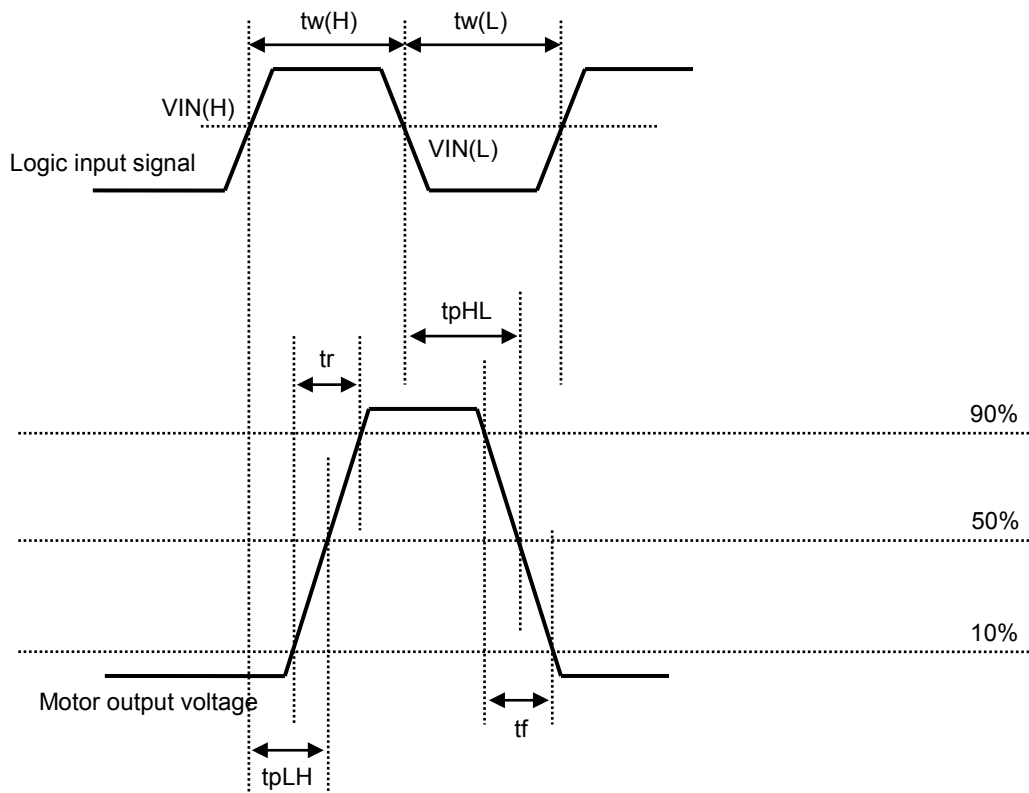
#### IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

## AC electrical characteristics (Ta = 25°C and VM = 24 V, unless otherwise specified)

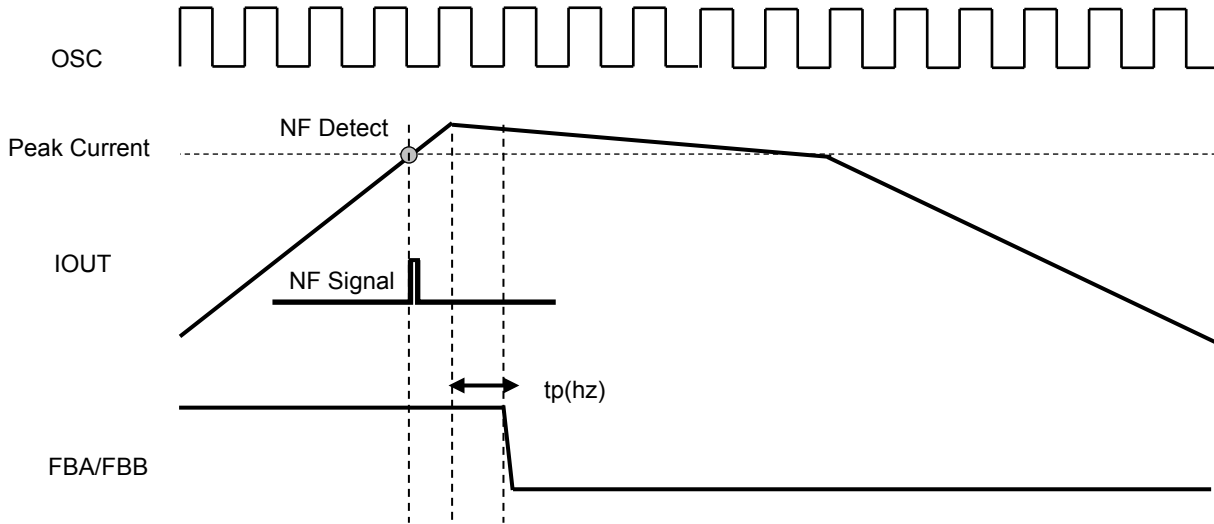
Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Minimum logic 'High' pulse width	tw(H)	Logic input signal	500	—	—	ns
Minimum logic 'Low' pulse width	tw(L)	Logic input signal	500	—	—	ns
Output MOSFET switching specifications	tr	—	30	80	130	ns
	tf	—	40	90	140	ns
	tpLH	INA1/INB1, INA2/INB2 and PWMA/PWMB to OUT	250	—	1200	ns
	tpHL	INA1/INB1, INA2/INB2 and PWMA/PWMB to OUT	250	—	1200	ns
Logic output delay time	tp(hz)	Current limit (NF Detect) - FBA/FBB (On) Pull up 10 kΩ to 5 V (OD ON)	135	—	355	ns
	tp(zh)	INA1/INB1, INA2/INB2, PWMA/PWMB - FBA/FBB (OFF) Pull up 10 kΩ to 5 V (OD OFF)	135	—	535	
OSCM oscillator accuracy	$\Delta f_{OSCM}$	COSC = 270 pF, RO SC = 5.1 kΩ	-15	—	+15	%
OSCM oscillator frequency	fOSCM	COSC = 270 pF, RO SC = 5.1 kΩ	—	1120	—	kHz

## AC characteristics timing chart



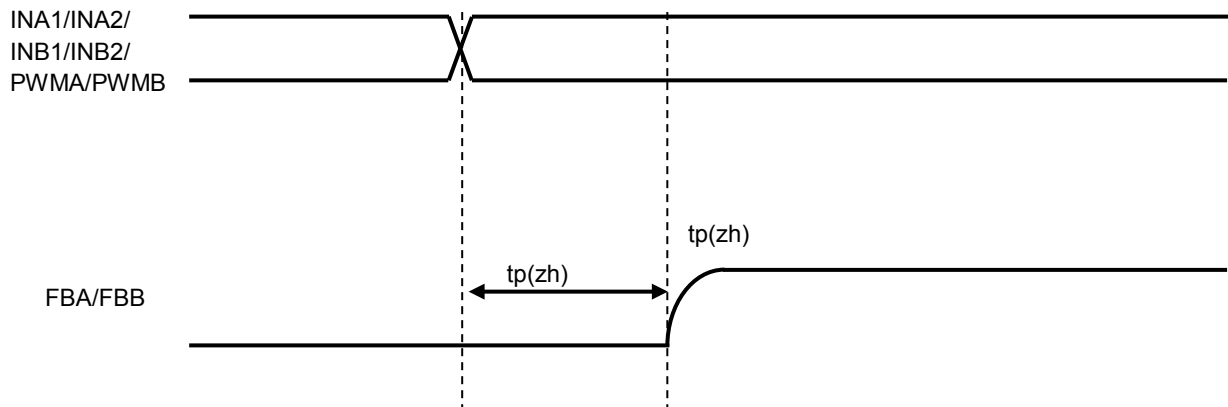
The timing chart may be simplified for explanatory purpose.

## Peak current (NF Detect) - FBA/FBB(On) Timing charts



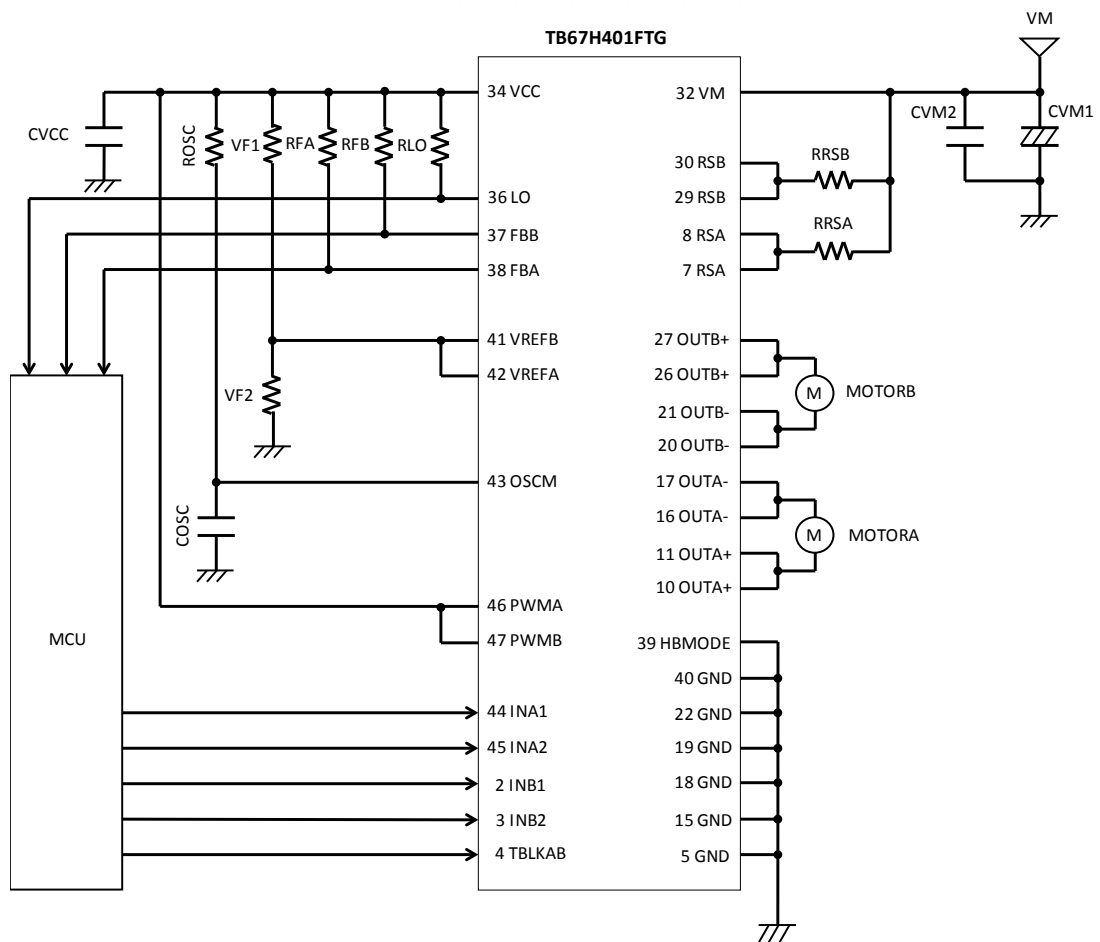
Timing charts may be simplified for explanatory purposes.

## INA1/INA2/INB1/INB2/PWMA/PWMB - FBA/FBB (OFF) Timing charts



Timing charts may be simplified for explanatory purposes.

### Application circuit example (Dual H-bridge mode)



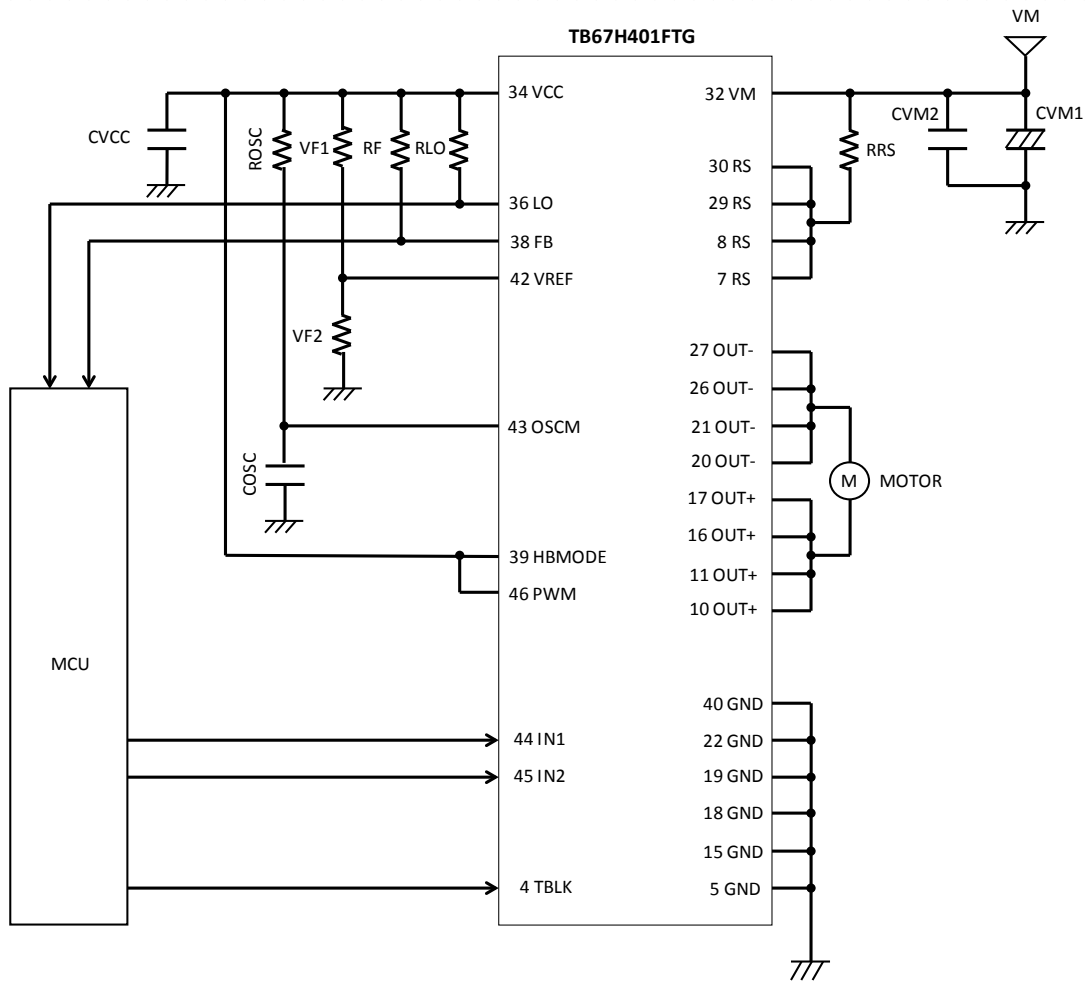
The application circuits shown in this document are provided for reference purposes only, and are not guaranteed for mass production.

Component values (for reference)

Symbol	Component	Reference value for each components
CVM1	Electrolytic capacitor	100 $\mu$ F (CVM1 $\geq$ 10 $\mu$ F)
CVM2	Ceramic capacitor	(0.1 $\mu$ F)
RRSA, RRSB	Current sense resistor	0.22 $\Omega$ (0.1 $\Omega \leq$ RRSA/RRSB)
VF1, VF2	Voltage divider	(10 k $\Omega \leq$ VF1+ VF2 $\leq$ 50 k $\Omega$ if needed)
CVCC	Ceramic capacitor	0.1 $\mu$ F
ROSC	Resistor	5.1 k $\Omega$ (1.8 k $\Omega$ to 8.2 k $\Omega$ )
COSC	Ceramic capacitor	270 pF
RLO, RFA, RFB	Pull-up resistor	10 k $\Omega$ (10 k $\Omega$ to 100 k $\Omega$ )

Values mentioned in the table above are for reference only. Each value can be adjusted per each usage condition.

## Application circuit example (Single H-bridge mode)



The application circuits shown in this document are provided for reference purposes only, and are not guaranteed for mass production.

### Component values (for reference)

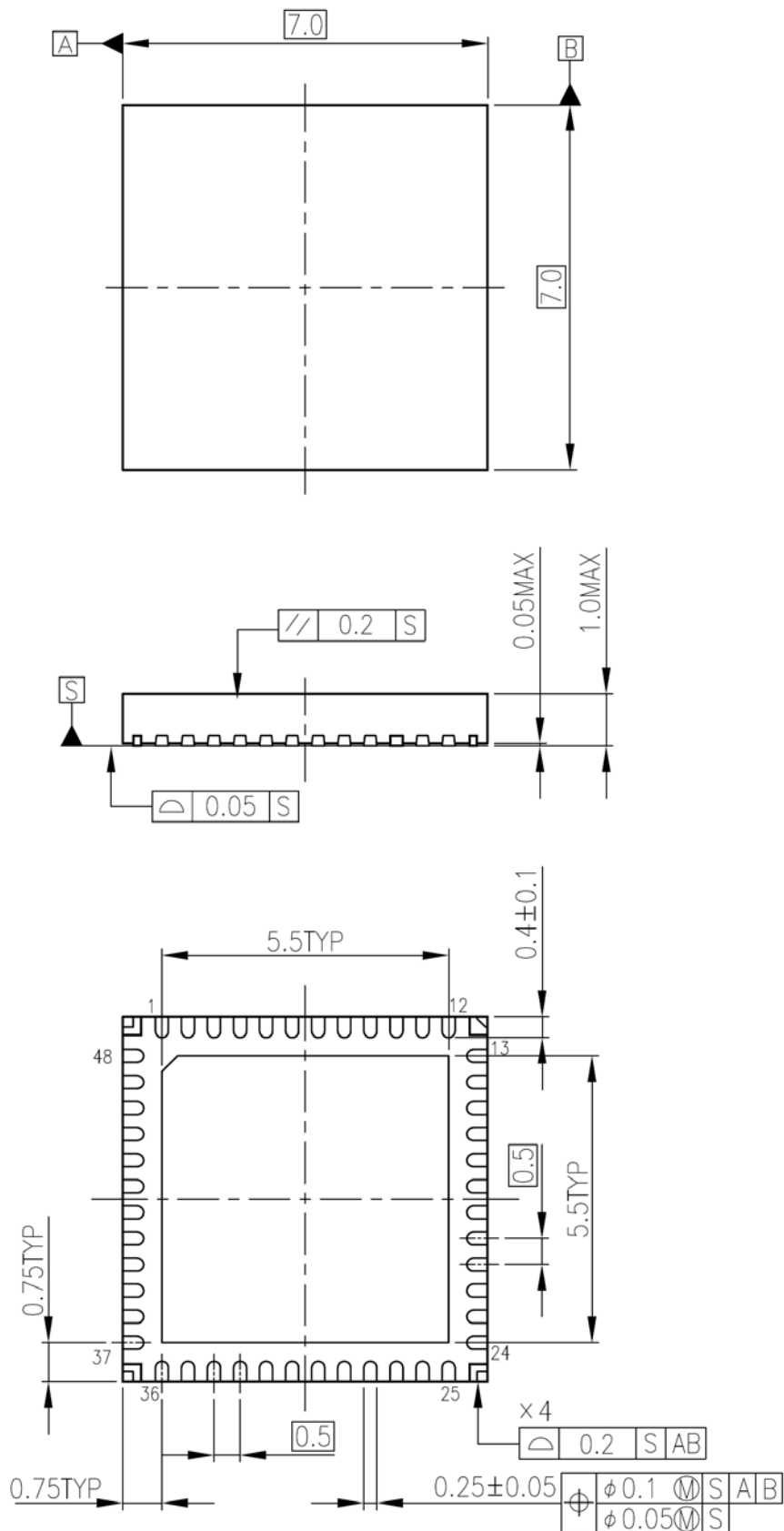
Symbol	Component	Reference value for each components
CVM1	Electrolytic capacitor	100 $\mu$ F (CVM1 $\geq$ 10 $\mu$ F)
CVM2	Ceramic capacitor	(0.1 $\mu$ F)
RRS	Current sense resistor	0.22 $\Omega$ (0.1 $\Omega \leq$ RRS)
VF1, VF2	Voltage divider	(10 k $\Omega \leq$ VF1+ VF2 $\leq$ 50 k $\Omega$ if needed)
CVCC	Ceramic capacitor	0.1 $\mu$ F
ROSC	Resistor	5.1 k $\Omega$ (1.8 k $\Omega$ to 8.2 k $\Omega$ )
COSC	Ceramic capacitor	270 pF
RLO, RF	Pull-up resistor	10 k $\Omega$ (10 k $\Omega$ to 100 k $\Omega$ )

Values mentioned in the table above are for reference only. Each value can be adjusted per each usage condition.

## Package dimensions

Unit: mm

P-VQFN48-0707-0.50-004



Weight 0.14 g (typ.)

**Notes on Contents****1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

**2. Equivalent Circuits**

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**3. Timing Charts**

Timing charts may be simplified for explanatory purposes.

**4. Application Circuits**

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Any license to any industrial property rights is not granted by provision of these application circuit examples.

**IC Usage Considerations****Notes on handling of ICs**

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.
- (5) Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occur from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

**Points to remember on handling of ICs****Over current detection circuit**

Over current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

**Thermal Shutdown Circuit**

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

**Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

**Back-EMF**

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.



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