Preliminary

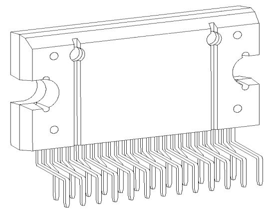
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6600HQ

PWM Chopper-Type bipolar Stepping Motor Driver IC

The TB6600HQ is a PWM chopper-type single-chip bipolar sinusoidal micro-step stepping motor driver.
Forward and reverse rotation control is available with 2-phase, 1-2-phase, W1-2-phase, 2W1-2-phase, and 4W1-2-phase excitation modes.
2-phase bipolar-type stepping motor can be driven by only clock signal with low vibration and high efficiency.

TB6600HQ



HZIP25-1.00F

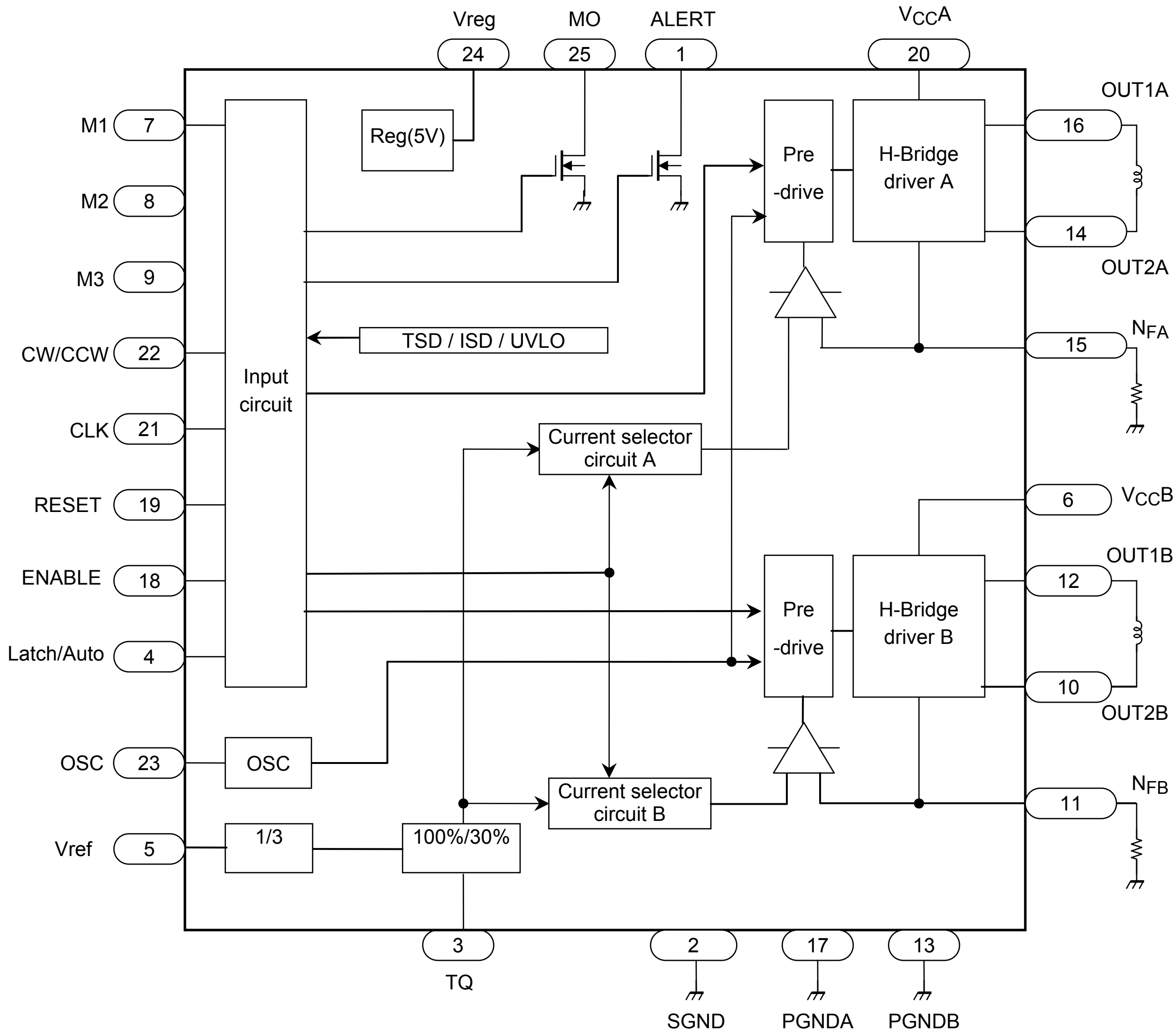
Weight:
HZIP25-1.00F: 7.7g (typ.)

Features

- Single-chip bipolar sinusoidal micro-step stepping motor driver
- BiCD 0.13 (50 V) process
- Ron (upper + lower) = 0.4 Ω (typ.)
- Forward and reverse rotation control available
- Selectable phase drive (1/1, 1/2, 1/4, 1/8, and 1/16 step)
- Output withstand voltage: V_{CC} = 50 V
- Output current: I_{OUT} = 5.0 A (absolute maximum ratings, peak, within 100ms)
  I_{OUT} = 4.5 A (operating range, maximal value)
- Packages: HZIP25-1.00F
- Built-in input pull-down resistance: 100 kΩ (typ.)
- Output monitor pins (ALERT): Maximum of I_{ALERT} = 1 mA
- Output monitor pins (MO): Maximum of I_{MO} = 1 mA
- Equipped with reset and enable pins
- Stand by function
- Single power supply
- Built-in thermal shutdown (TSD) circuit
- Built-in under voltage lock out (UVLO) circuit
- Built-in over-current detection (ISD) circuit

The following conditions apply to solderability:
About solderability, following conditions were confirmed
(1)Use of Sn-37Pb solder Bath
·solder bath temperature: 230℃·dipping time: 5 seconds·the number of times: once·use of R-type flux
(2)Use of Sn-3.0Ag-0.5Cu solder Bath
·solder bath temperature: 245℃·dipping time: 5 seconds·the number of times: once·use of R-type flux

Block Diagram



Setting of Vref

Input	Voltage ratio
TQ	
L	30%
H	100%

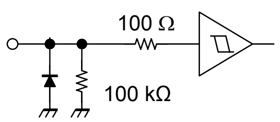
1
V1．0．14

Pin Functions

Pin No.	I/O	Symbol	Functional Description	Remark
1	Output	ALERT	TSD / ISD monitor pin	Pull-up by external resistance
2	—	SGND	Signal ground	
3	Input	TQ	Torque (output current) setting input pin	
4	Input	Latch/Auto	Select a return type for TSD and ISD.	L: Latch, H: Automatic return
5	Input	Vref	Voltage input for 100% current level	
6	Input	VccB	B channel Power supply	
7	Input	M1	Excitation mode setting input pin	
8	Input	M2	Excitation mode setting input pin	
9	Input	M3	Excitation mode setting input pin	
10	Output	OUT2B	B channel output 2	
11	—	N_{FB}	B channel output current detection pin	
12	Output	OUT1B	B channel output 1	
13	—	PGNDB	Power ground	
14	Output	OUT2A	A channel output 2	
15	—	N_{FA}	A channel output current detection pin	
16	Output	OUT1A	A channel output 1	
17	—	PGNDA	Power ground	
18	Input	ENABLE	Enable signal input pin	H: Enable, L: All outputs off
19	Input	RESET	Reset signal input pin	L: Initial mode
20	Input	VccA	A channel Power supply	
21	Input	CLK	CLK pulse input pin	
22	Input	CW/CCW	Forward/reverse control pin	L: CW, H:CCW
23	—	OSC	Resistor connection pin for internal oscillation setting	
24	Output	Vreg	Control side connection pin for power capacitor	Connecting capacitor to SGND
25	Output	MO	Electrical angle monitor pin	Pull-up by external resistance

<Terminal circuits>

Input pins
(M1, M2, M3,CLK, CW/CCW,
ENABLE, RESET, TQ, Latch/Auto)



Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	50	V
Output current (per one phase)	$I_{O\ (PEAK)}$	5.0/phase (Note 1)	A
Drain current (ALERT, DOWN)	$I_{(ALERT)}$	1	mA
	$I_{(MO)}$		
Input voltage	V_{IN}	6	V
Power dissipation	P_D	3.2 (Note 2)	W
		40 (Note 3)	
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: T = 100ms

Note 2: Ta = 25°C, No heat sink

Note 3: Ta = 25°C, with infinite heat sink.

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use the IC within the specified operating ranges.

Operating Range (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{CC}	—	8.0	—	45	V
Output current	I_{OUT}	—	—	—	4.5	A
Input voltage	V_{IN}	—	0	—	5.5	V
	V_{ref}	—	0.3	—	3.5	V
Clock frequency	f_{CLK}	—	—	—	200	kHz
Chopping frequency	f_{chop}	(　kΩ) ≦ Rosc ≦ (　kΩ)	20	40	60	kHz
OSC frequency	f_{OSC}	R_{OSC} = 51 kΩ	(2.0)	4.0	(6.0)	MHz

Note: V_{CC}A and V_{CC}B should be programmed the same voltage.
The maximum current of the operating range can not be necessarily conducted depending on various conditions because output current is limited by the power dissipation Pd.
Make sure to avoid using the IC in the condition that would cause the temperature to exceed Tj (avg.) (107°C).

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE, Latch/Auto, TQ	2.0	—	5.5	V
	Low	$V_{IN\ (L)}$		−0.2	—	0.8	
Input hysteresis voltage		V_H		—	400	—	mV
Input current		$I_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE, Latch/Auto, TQ V_{IN} = 5.0 V	—	55	80	μA
		$I_{IN\ (L)}$	V_{IN} = 0 V	—	—	1	
V_{CC} supply current		Icc_1	Output open, RESET: H, ENABLE: H、 M1:L, M2:L, M3:H (1/1-step mode) CLK:L	—	3.1	(7)	mA
		Icc_2	Output open, RESET: L, ENABLE: L M1:L, M2:L, M3:H (1/1-step mode) CLK:L	—	3.1	(7)	
		Icc_3	Standby mode (M1:L, M2:L, M3:L)	—	1.8	(4)	
Vref input circuit	Current limit voltage	V_{ref}	Vref = 3.0 V	0.9	1.0	1.1	V
	Input current	$I_{IN(ref)}$	Vref = 3.0 V	—	—	1	μA
	Divider ratio	V_{ref}/V_{NF}	Maximum current : 100%	—	3	—	—
Minimum CLK pulse width		$tw_{CLK\ H}$		2.2	—	—	μs
		$tw_{CLK\ L}$					
Output residual voltage		V_{OL} MO	I_{OL} = 1 mA	—	—	0.5	V
		V_{OL} ALERT					
Internal constant voltage		Vreg	External capacitor = 0.1 μF (in standby mode)	4.5	5.0	5.5	V
TSD operation temperature (Note)		TSD	Design target value	160	170	180	°C
TSD hysteresis(Note)		TSDhys	Design target value	30	40	50	°C
Over current detection current (Note)		ISD	All outputs, Design target value	5.0	6.5	8.0	A
Oscillation frequency		f_{OSC}	External resistance Rosc = 51 kΩ	2.8	4	5.2	MHz

Note: Pre-shipment testing is not performed.

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Output ON resistor		$Ron_U + Ron_L$	I_{OUT} = 4 A	—	0.4	0.6	Ω
Output transistor switching characteristics		t_r	V_{NF} = 0 V, Output: Open	—	(0.5)	—	μs
		t_f		—	(0.5)	—	
Output leakage current	Upper side	I_{LH}	V_{CC} = 50 V	—	—	5	μA
	Lower side	I_{LL}		—	—	5	

Description of Functions

1. Excitation Settings

The excitation mode can be selected from the following eight modes using the M1, M2 and M3 inputs. New excitation mode starts from the initial mode when M1, M2, or M3 inputs are shifted during motor operation. In this case, output current waveform may not continue.

Input			Mode (Excitation)
M1	M2	M3	
L	L	L	Standby mode (Operation of the internal circuit is almost turned off.)
L	L	H	1/1 (2-phase excitation, full-step）
L	H	L	1/2A type (1-2 phase excitation A type) (0% - 71% - 100%)
L	H	H	1/2B type (1-2 phase excitation B type) (0% - 100%)
H	L	L	1/4 (W1-2 phase excitation）
H	L	H	1/8 (2W1-2 phase excitation)
H	H	L	1/16 (4W1-2 phase excitation)
H	H	H	Standby mode (Operation of the internal circuit is almost turned off.)

Note: To change the exciting mode by changing M1, M2, and M3, make sure not to set M1 = M2 = M3 = L or M1 = M2 = M3 = H.

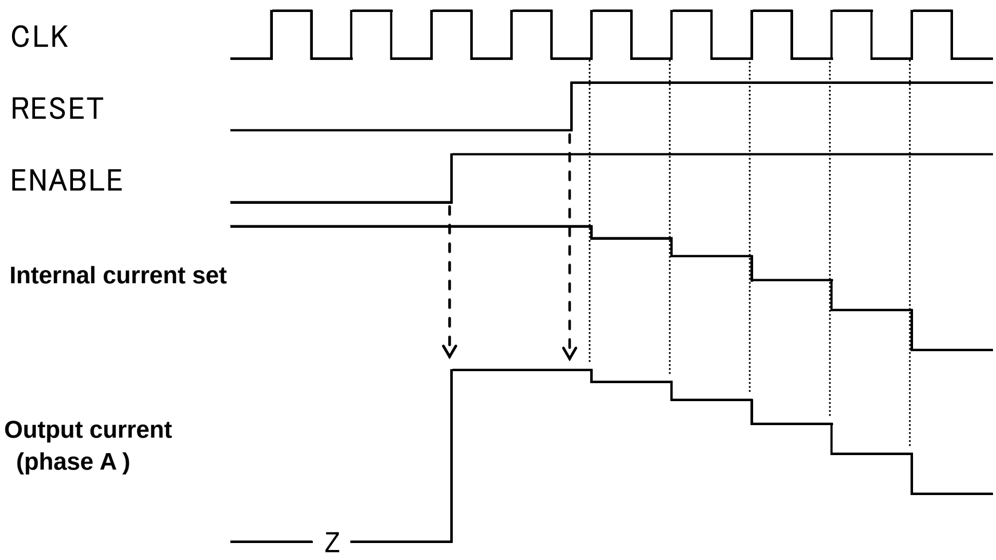
Standby mode

The operation mode moves to the standby mode under the condition M1 = M2 = M3 = L or M1 = M2 = M3 = H.
The power consumption is minimized by turning off all the operations except protecting operation.
In standby mode, output terminal MO is HZ.
To release the standby mode, release the condition of M1 = M2 = M3 = L or M1 = M2 = M3 = H.
Input signal is not accepted for about 200 μs after releasing the standby mode.

2. Function

(1) When the ENABLE signal goes Low level, it sets an OFF on the output.
(2) The output changes to the Initial mode shown in the table below when the ENABLE signal goes High level and the RESET signal goes Low level. In this mode, the status of the CLK and CW/CCW pins are irrelevant.
(3) When the ENABLE signal goes Low level, it sets an OFF on the output. In this mode, the output changes to the initial mode when the RESET signal goes Low level. Under this condition, the initial mode is output by setting the ENABLE signal High level. And the motor operates from the initial mode by setting the RESET signal High level.

(Example 1)



Input				Output mode
CLK	CW/CCW	RESET	ENABLE	
↑	L	H	H	CW
↑	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't Care

Command of the standby has a higher priority than ENABLE. Standby mode can be tured on and off regardless of the state of ENABLE.

3. Initial Mode

When RESET is used, the phase currents are as follows.

Excitation Mode	Phase A Current	Phase B Current
1/1 (2-phase excitation, full-step)	100%	-100%
1/2A type (1-2 phase excitation A type) (0% - 71% - 100%)	100%	0%
1/2B type (1-2 phase excitation B type) (0% - 100%)	100%	0%
1/4 (W1-2 phase excitation)	100%	0%
1/8 (2W1-2 phase excitation)	100%	0%
1/16 (4W1-2 phase excitation)	100%	0%

In this specification, current direction is defined as follows.
OUT1A → OUT2A: Forward direction
OUT1B → OUT2B: Forward direction

4. 100% current settings (Current value)

100% current value is determined by Vref inputted from external part and the external resistance for detecting output current. Vref is doubled 1/3 inside IC.

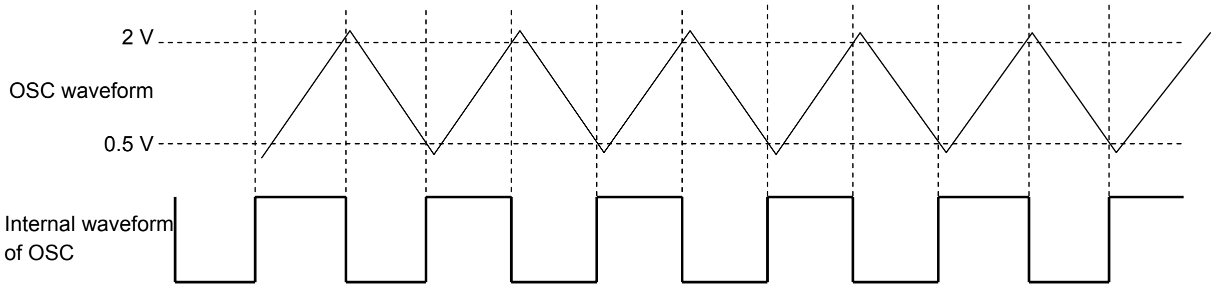
$$Io(100\%) = (1/3 \times Vref) \div R_{NF}$$

The average current is lower than the calculated value because this IC has the method of peak current detection.
R_{NF} should be 0.2 Ω or more.

5. OSC

Triangle wave is generated internally by CR oscillation by connecting external resistor to OSC terminal.
Rosc: (　　kΩ) ≤　Rosc ≤　(　　kΩ)

OSC waveform

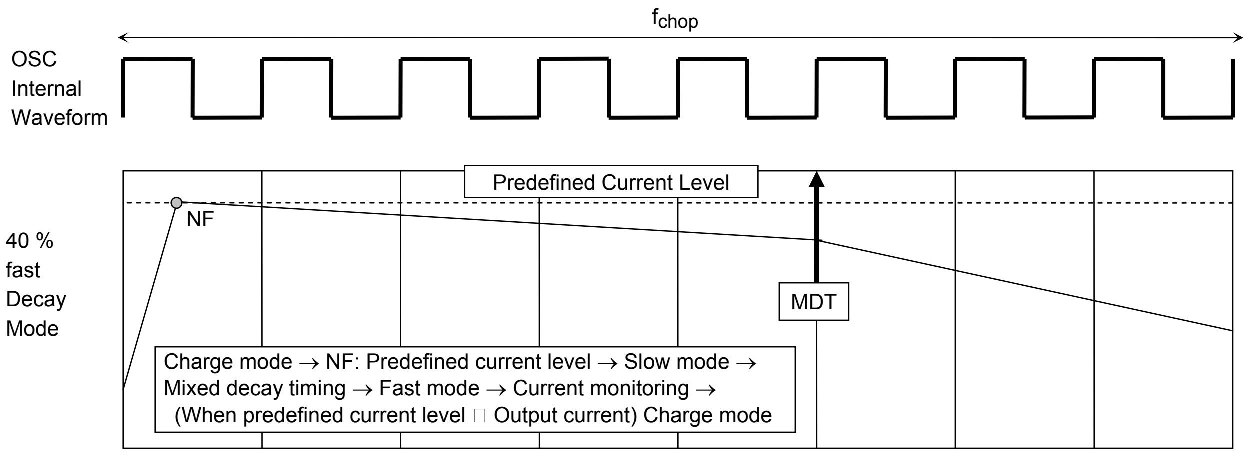


6. Decay Mode

It takes approximately five OSCM cycles for charging-discharging a current in PWM mode. The 40% fast decay mode is created by inducing decay during the last two cycles in Fast Decay mode.
The ratio 40% of the fast decay mode is always fixed.
OSCM = 20 dividing frequency of the master clock (4 MHz, typ.).

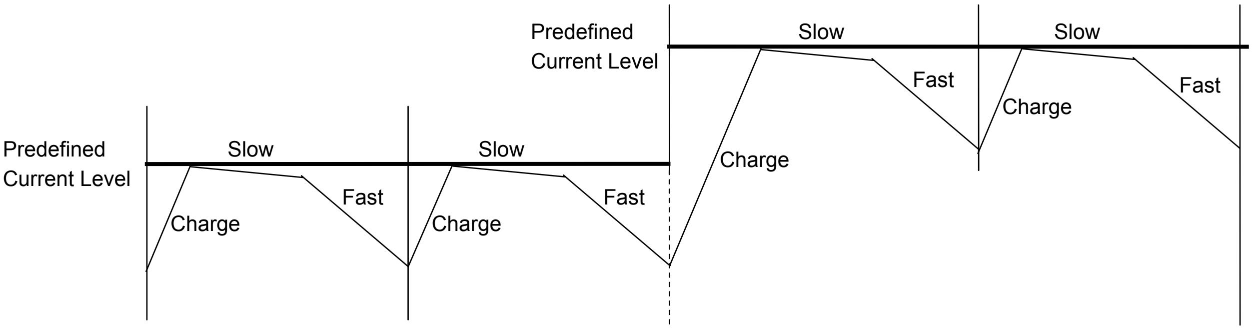
6-1. Current Waveform and Mixed Decay Mode settings

The period of PWM operation is equal to five periods of OSCM.
The ratio 40% of the fast decay mode is always fixed.
The “NF” refers to the point at which the output current reaches its predefined current level.
The smaller the MDT value, the smaller the current ripple amplitude. However, the current decay rate decreases.
MDT means the point of MDT (MIXED DECAY TIMMING) in the below diagram.

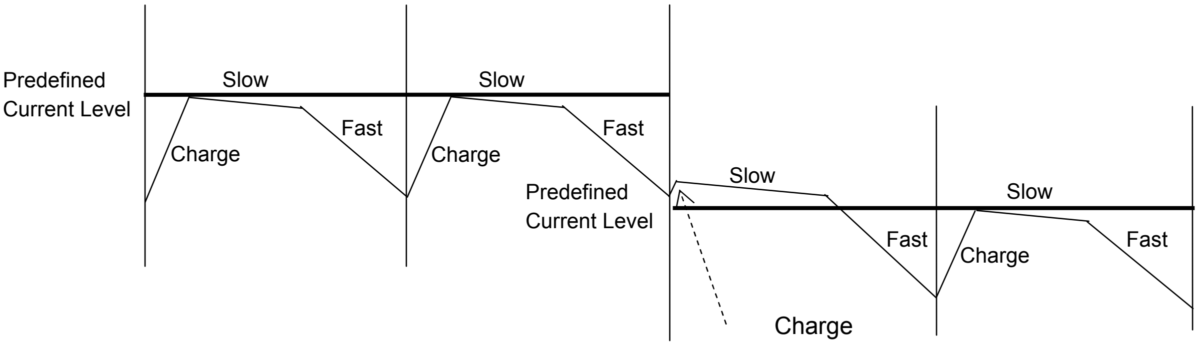


6-2. Effect of Decay Mode

- Increasing the current (sine wave)

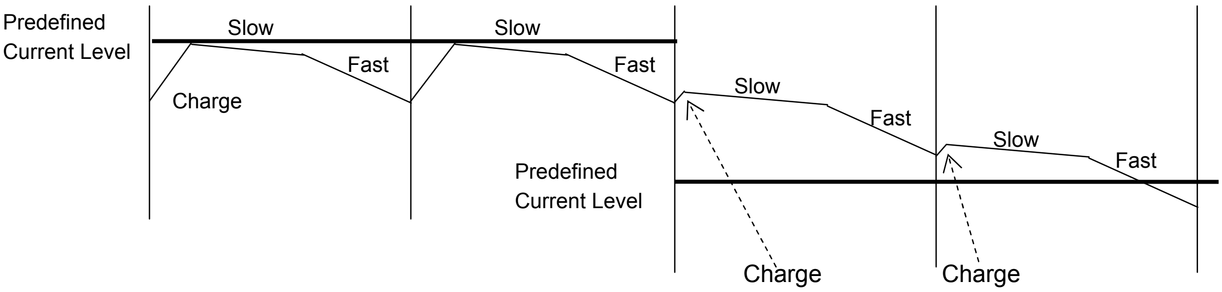


- Decreasing the current (In case the current is decreased to the predefined value in a short time because it decays quickly.)



Even if the output current rises above the predefined current at the RNF point, the current control mode is briefly switched to Charge mode for current sensing.

- Decreasing the current (In case it takes a long time to decrease the current to the predefined value because the current decays slowly.)

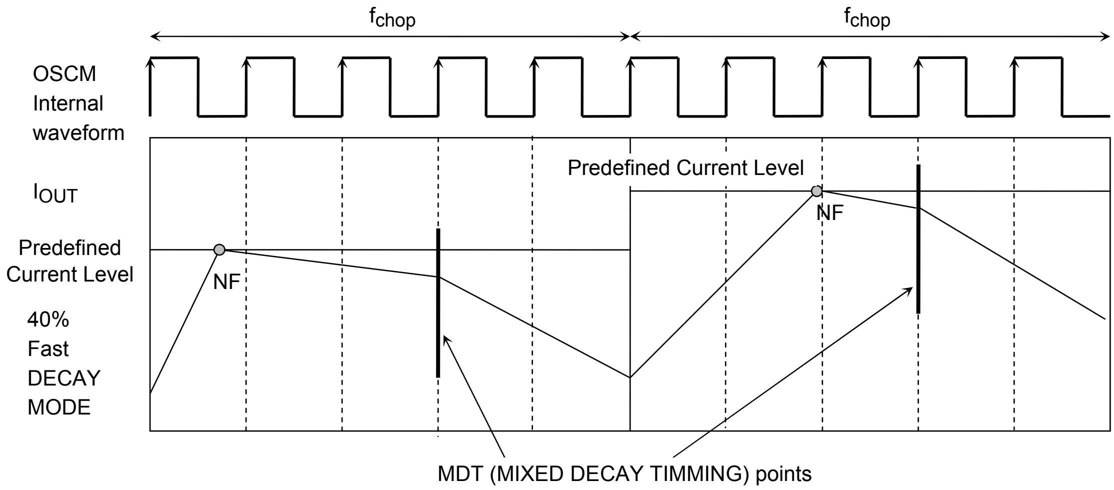


Even if the output current rises above the predefined current at the RNF point, the current control mode is briefly switched to Charge mode for current sensing.

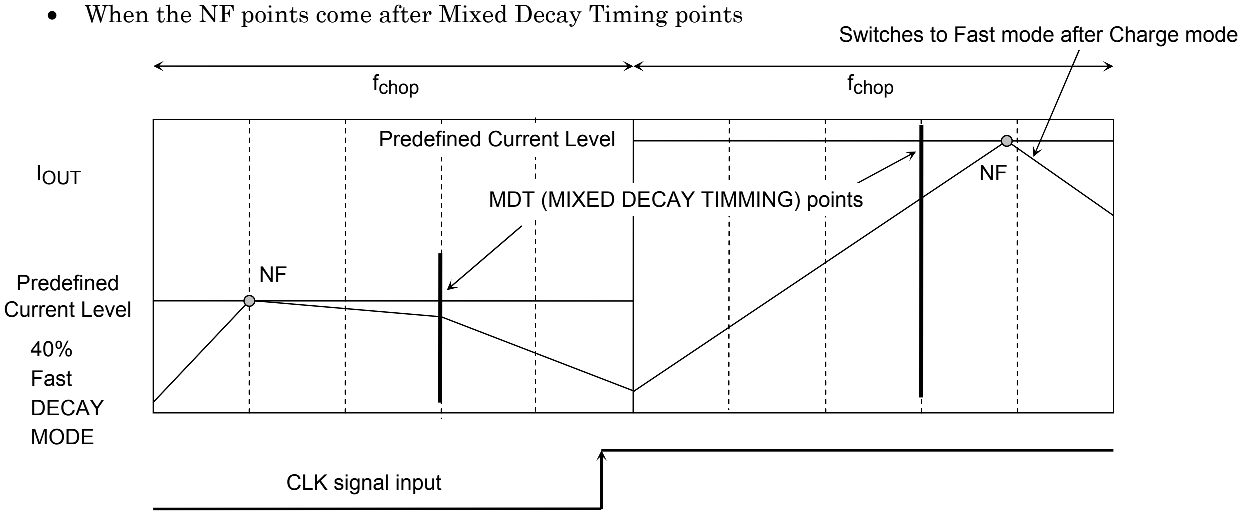
During Mixed Decay and Fast Decay modes, if the predefined current level is less than the output current at the RNF (current monitoring point), the Charge mode in the next chopping cycle will disappear (though the current control mode is briefly switched to Charge mode in actual operations for current sensing) and the current is controlled in Slow and Fast Decay modes (mode switching from Slow Decay mode to Fast Decay mode at the MDT point).

Note: The above figures are rough illustration of the output current. In actual current waveforms, transient response curves can be observed.

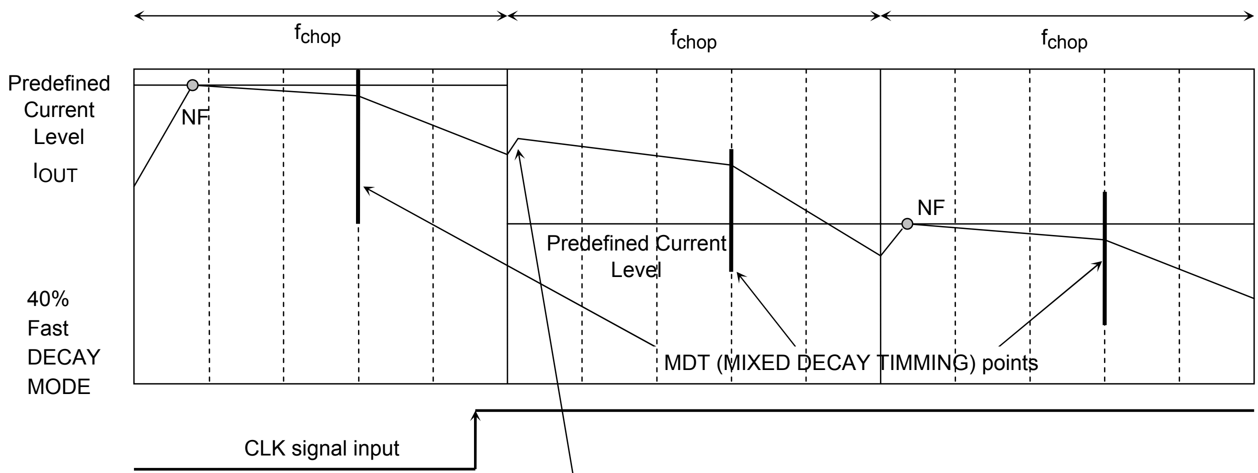
6-3. Current Waveforms in Mixed Decay Mode



- When the NF points come after Mixed Decay Timing points



- When the output current value > predefined current level in Mixed Decay mode

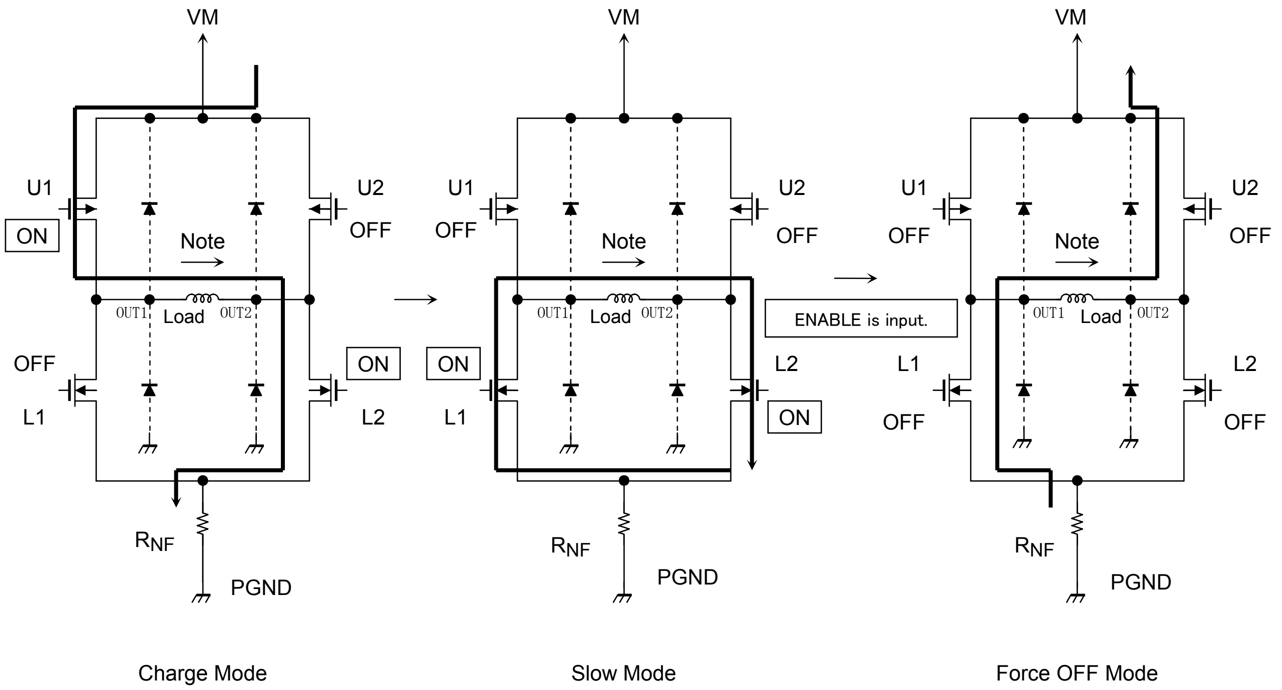


Even if the output current rises above the predefined current at the RNF point, the current control mode is briefly switched to Charge mode for current sensing.

Current Draw-out Path when ENABLE is Input in Mid Operation

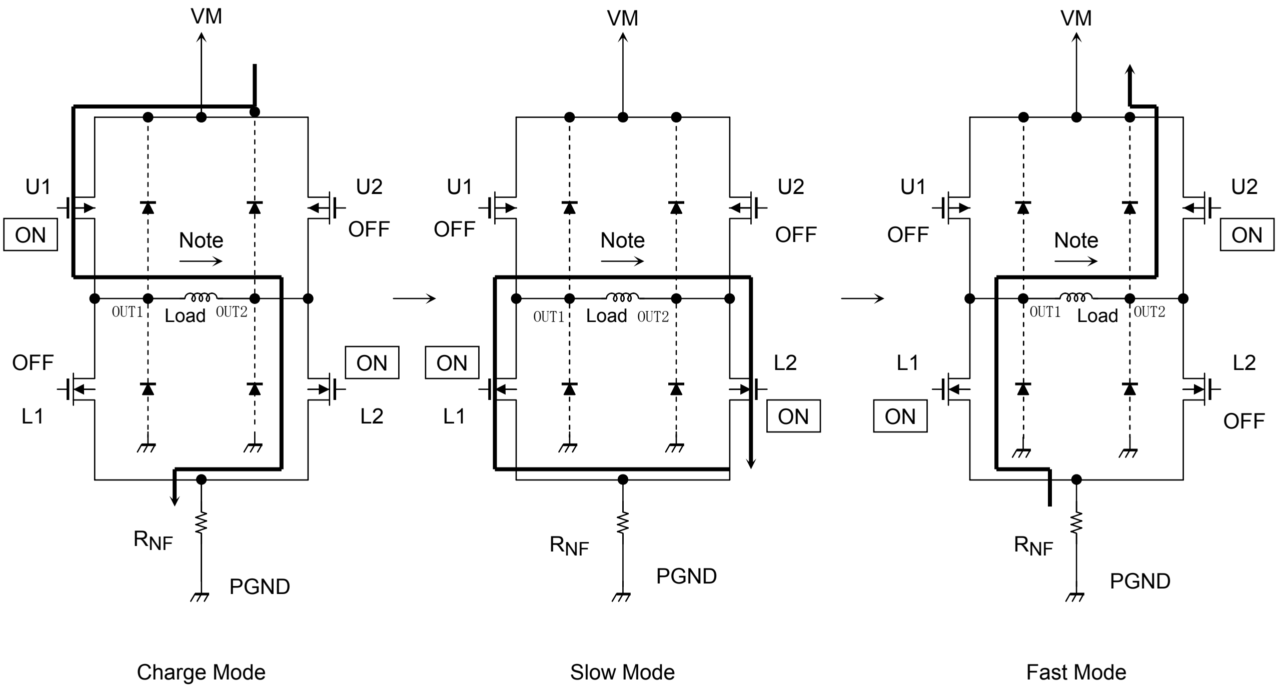
When all the output transistors are forced OFF during Slow mode, the coil energy is drawn out in the following modes:

Note: Parasitic diodes are indicated on the designed lines. However, these are not normally used in Mixed Decay mode.



As shown in the figure above, an output transistor has parasitic diodes.
Normally, when the energy of the coil is drawn out, each transistor is turned ON and the power flows in the opposite-to-normal direction; as a result, the parasitic diode is not used. However, when all the output transistors are forced OFF, the coil energy is drawn out via the parasitic diode.

Output Stage Transistor Operation Mode



Output Stage Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above chart shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following chart:

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Upon transitions of above-mentioned functions, a dead time of about 300 ns (Design target value) is inserted respectively.

Measurement Waveform

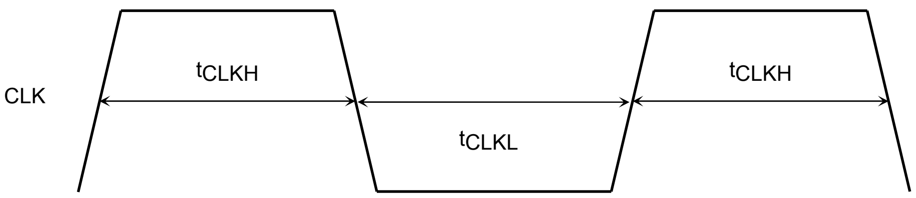


Figure 1 Timing Waveforms and Names

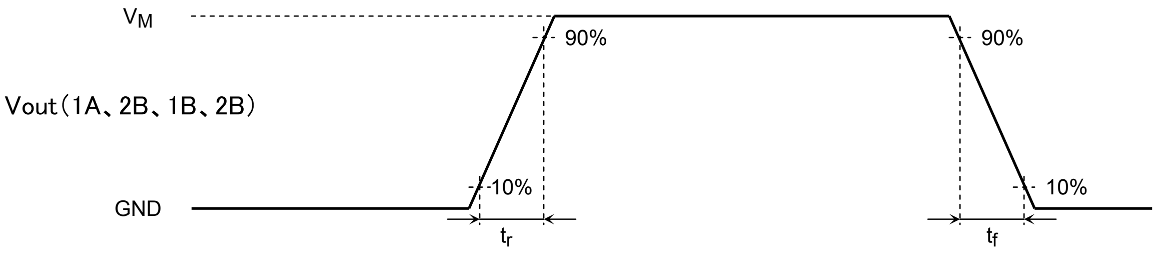


Figure 2 Timing Waveforms and Names

Latch/Auto

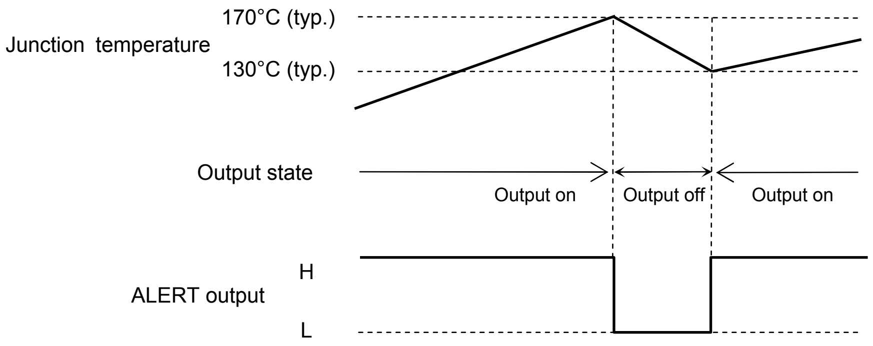
Input pin for determining the return method of TSD and ISD.
If Latch/Auto pin outputs low, TSD and ISD functions return by either of turning on power supply again or programming the ENABLE as H → L → H.
If Latch/Auto pin outputs high, they return automatically.
In standby mode, TSD function returns automatically and ISD function cannot operate regardless of the state of the Latch/Auto pin.
When power supply voltage $V_{CC}A$ and $V_{CC}B$ are less than 8 V, TSD and ISD functions cannot operate regardless of the state of the Latch/Auto pin.

Thermal Shut-Down circuit（TSD）

(1) Automatic return

TSD = 170°C （typ.） (Note)

ΔTSD = 40°C （typ.） (Note)

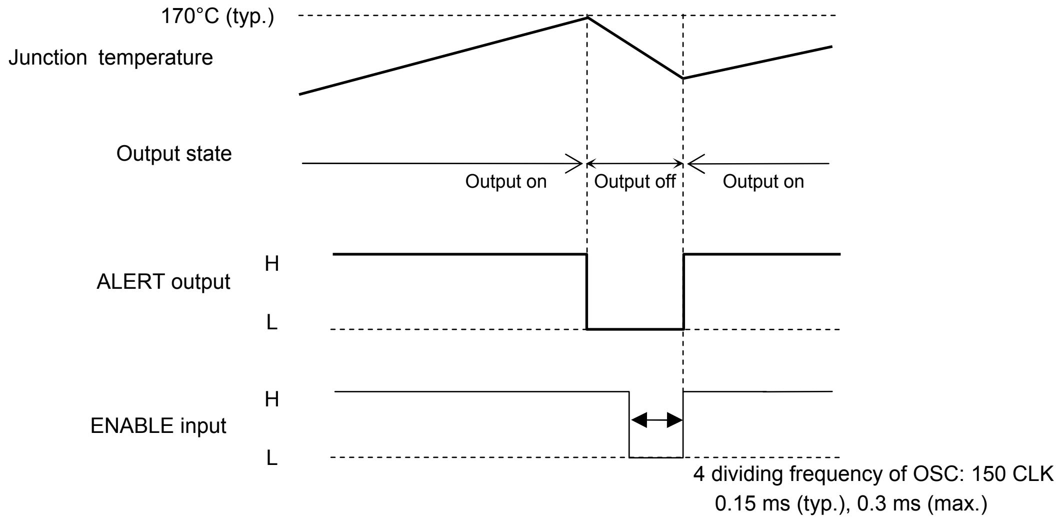


Automatic return has a temperature hysteresis shown in the above figure.

In case of automatic return, the return timing is adjusted at charge start of fshop after the temperature falls to the return temperature (It is 130℃(typ.) in the above figure).
It returns after time passes between 1st and 2nd frequency (fchop).

(2) Latch return

TSD = 170°C (typ.) ± 10 °C (Note)



The operation returns by programming the ENABLE as H → L → H shown in above figure or turning on power supply and turning on UVLO function.

Note: Pre-shipment testing is not performed.

・State of internal IC when TSD circuit operates.

States of internal IC and output correspond to the state in ENABLE mode.
After a return, the timing of output is not determined. It is the same as the case that ENABLE mode is reset.
Operation can start from initial mode by setting the reset low level.

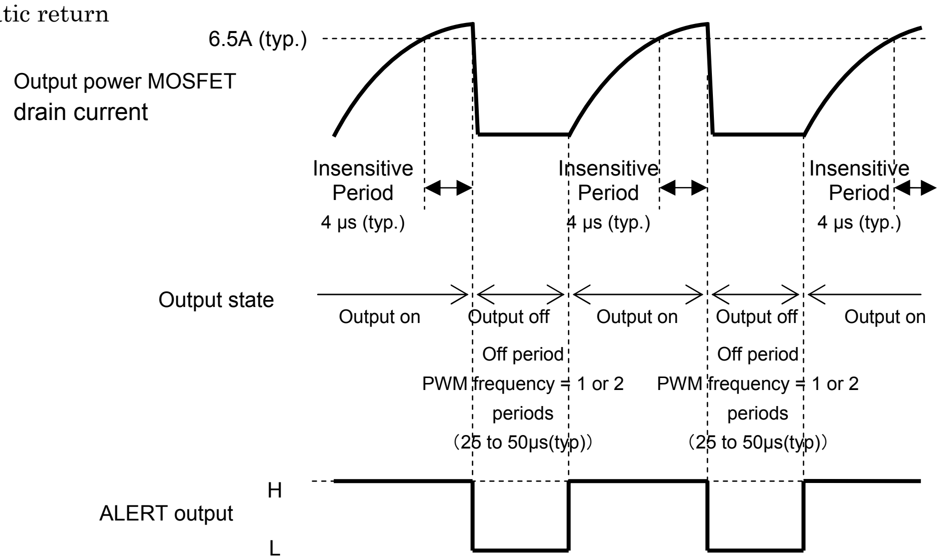
ISD (Over current detection)

Current that flow through output power MOSFETs are monitored individually. If over-current is detected in at least one of all output power MOSFETs, all output power MOSFETs are turned off then this status is kept until ENABLE signal is input. Target value in design is 6.5 A. Pulse of 0.15 ms or more should be recognized.

Masking term of 4μs (typ.) should be provided in order to protect detection error by noise.

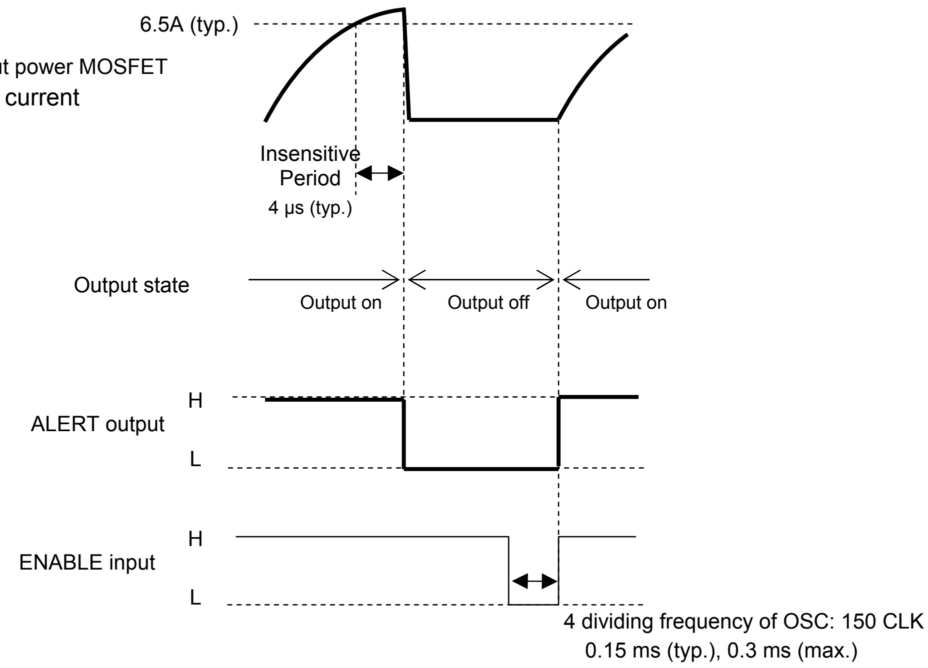
ISD＝6.5 A ± 0.15 A （Note ）

(1) Automatic return



Operation returns automatically after off period shown in above figure.

(1) Latch return



The operation returns by programming the ENABLE as H → L → H shown in above figure or turning on power supply and turning on UVLO function.

Note: Pre-shipment testing is not performed.

・State of internal IC when ISD circuit operates.

States of internal IC and output correspond to the state in ENABLE mode.
After a return, the timing of output is not determined. It is the same as the case that ENABLE mode is reset.
Operation can start from initial mode by setting the reset low level.

Under Voltage Lock Out (UVLO) circuit

Outputs are shutoff by operating at 5.5 V (Typ.) of V_{CC} or less.
It has a hysteresis of 0.5 V (Typ.) and returns to output when V_{CC} reaches 6.0 V (Typ.).

・State of internal IC when UVLO circuit operates.

The states of the internal IC and outputs correspond to the state in the ENABLE mode and the initial mode at the same time.
After a return, it can start from the initial mode.

When either of $V_{CC}A$ or $V_{CC}B$ falls to around 5.5 V and UVLO operates, output turns off.
It recovers automatically from the initial mode when both V_{CC} rise to around 6.0 V or more.

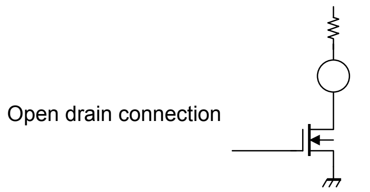
ALERT output

ALERT terminal outputs in detecting TSD or ISD.

ALERT terminal is connected to power supply externally via pull-up resistance.

V_{ALERT} = 0.5 V (max.) at 1 mA

TSD	ISD	ALERT
Under TSD detection	Under TSD detection	Low
Normal	Under TSD detection	
Under TSD detection	Normal	
Normal	Normal	Z



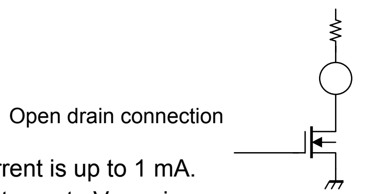
Applied voltage to pull-up resistance is up to 5.5 V. And conducted current is up to 1 mA.

MO output

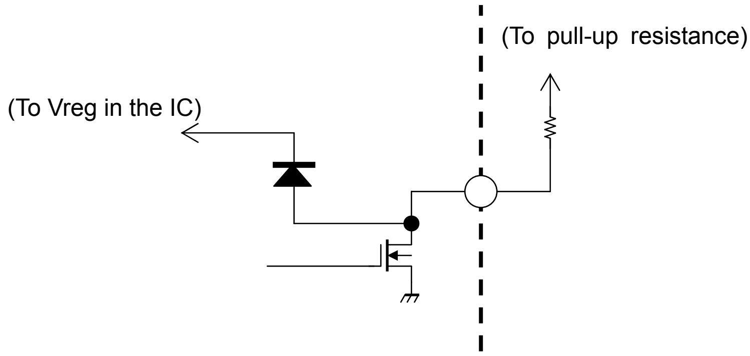
MO turns on at the predetermined state and output low.
MO terminal is connected to power supply externally via pull-up resistance.

V_{MO} = 0.5 V (max.) at 1 mA

State	MO
Initial	Low
Not initial	Z



Applied voltage to pull-up resistance is up to 5.5 V. And conducted current is up to 1 mA.
It is recommended to gain 5 V by connecting the external pull-up resistance to Vreg pin.



Voltage pull-up of MO and ALERT pins

・It is recommended to pull-up voltage to Vreg pin.

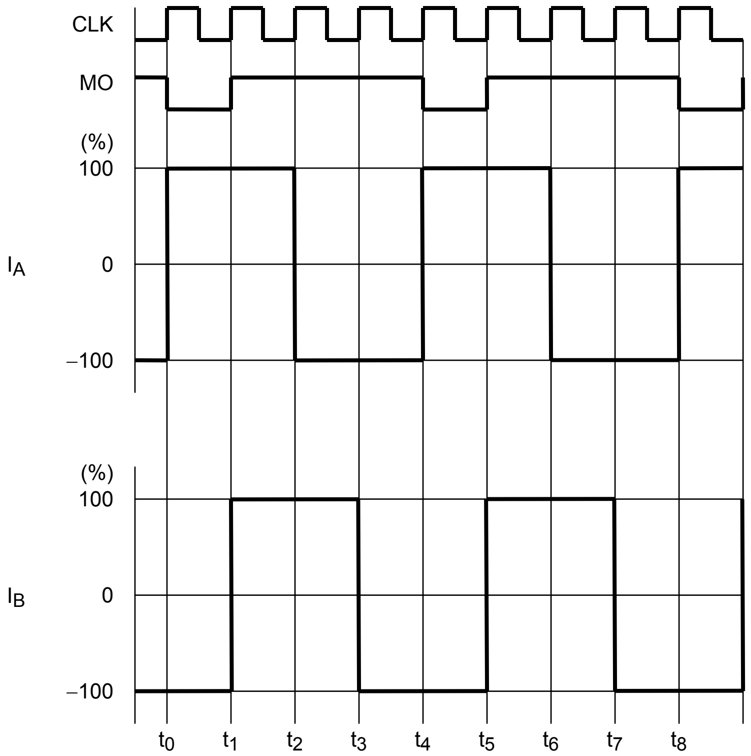
・In case of pull-up to except 5 V (for instance, 3.3 V etc.), it is recommended to use other power supply (ex. 3.3 V) while V_{CC}A and V_{CC}B output between the operation range. When V_{CC}A and V_{CC}B decrease lower than the operation range and Vreg decreases from 5 V to 0 V under the condition that other power supply is used to pull-up voltage, the current continues to conduct from other power supply to the IC inside through the diode shown in the figure. Though this phenomenon does not cause destruction and malfunction of the IC, please consider the set design not to continue such a state for a long time.

・As for the pull-up resistance for MO and ALERT pins, please select large resistance enough for the conducting current so as not to exceed the standard value of 1 mA.

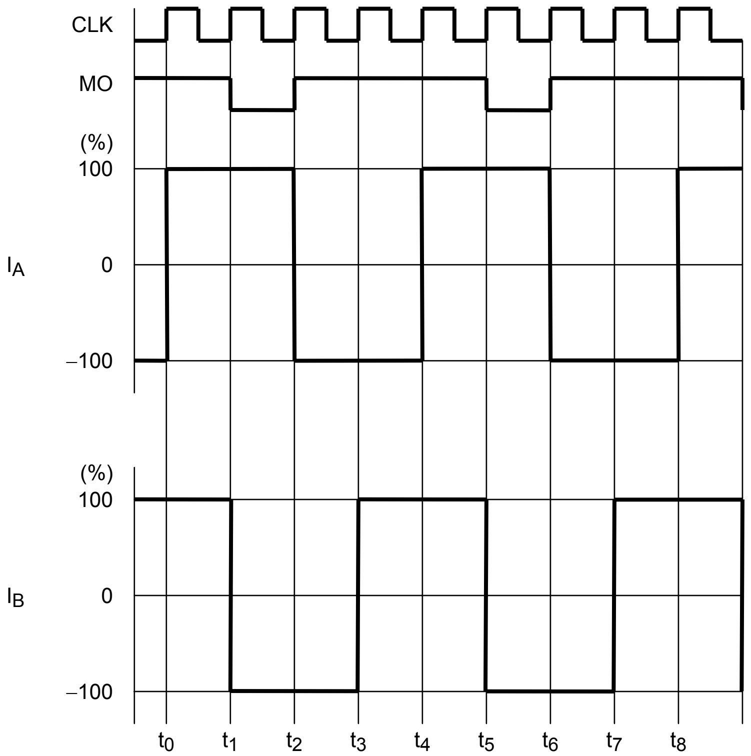
Please use the resistance of 30 kΩ or more in case of applying 5 V, and 20 kΩ or more in case of applying 3.3 V.

Sequence in each excitation mode

1/1-step Excitation Mode (M1: L, M2: L, M3: H, CW Mode)

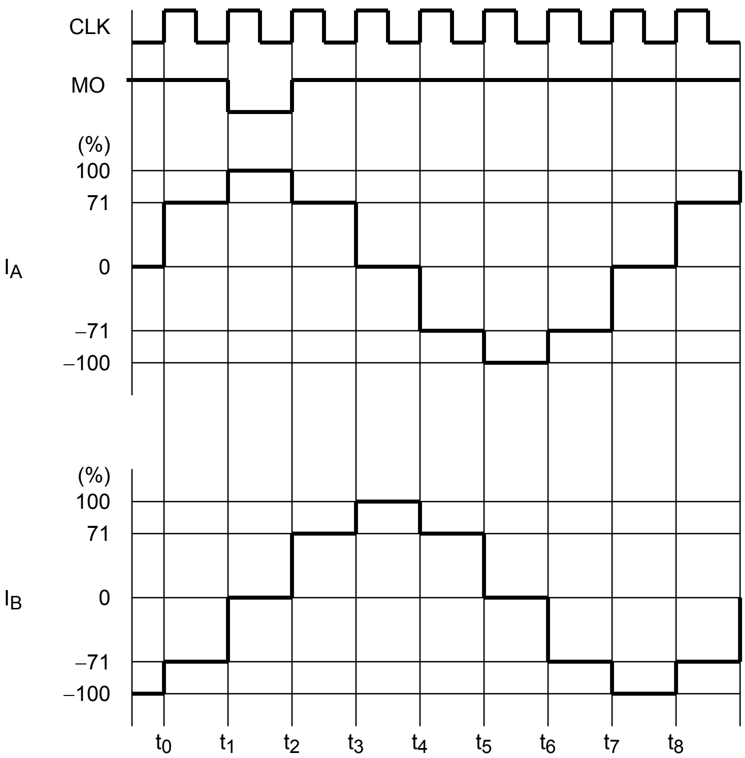


1/1-step Excitation Mode (M1: L, M2: L, M3: H, CCW Mode)

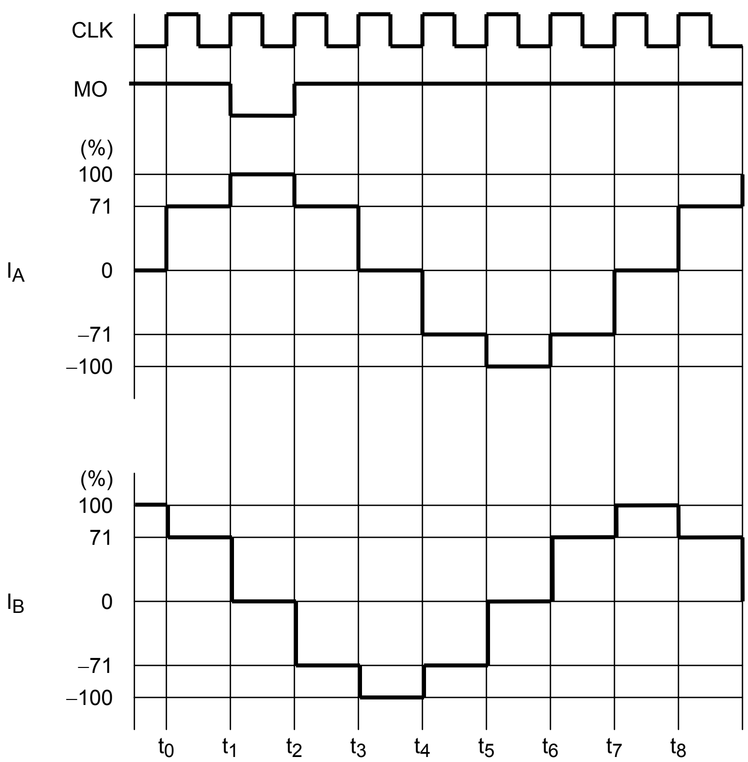


It operates from the initial state after the excitation mode is switched.

1/2-step Excitation Mode (A type)   (M1: L, M2: H, M3: L, CW Mode)

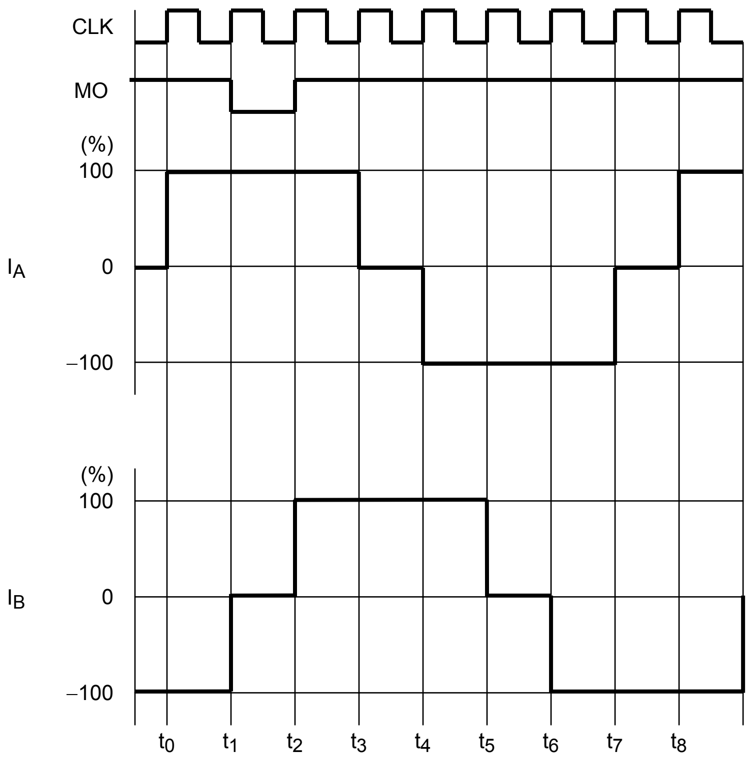


1/2-step Excitation Mode (A type)   (M1: L, M2: H, M3: L, CCW Mode)

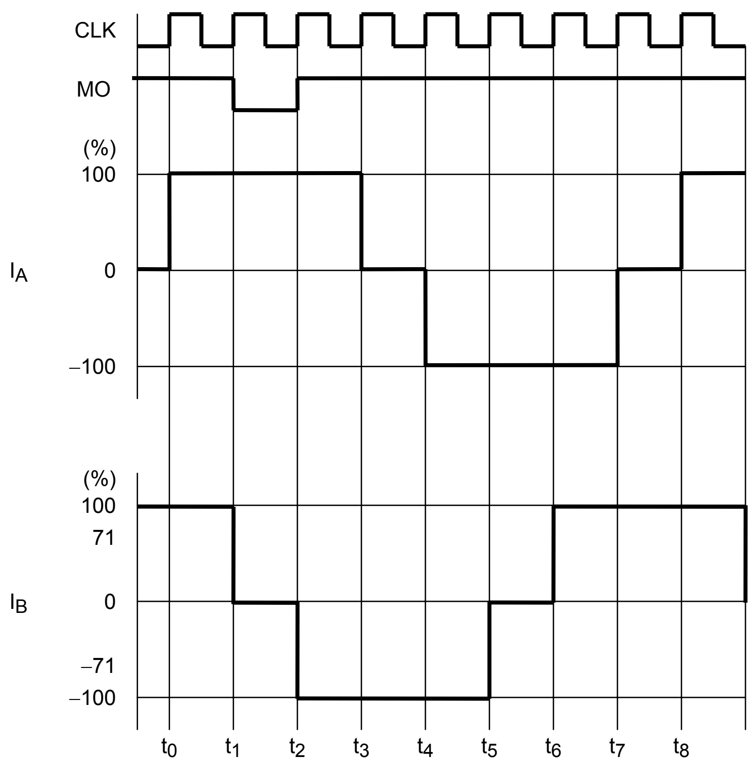


It operates from the initial state after the excitation mode is switched.

1/2-step Excitation Mode (B type) (M1: L, M2: H, M3: H, CW Mode)

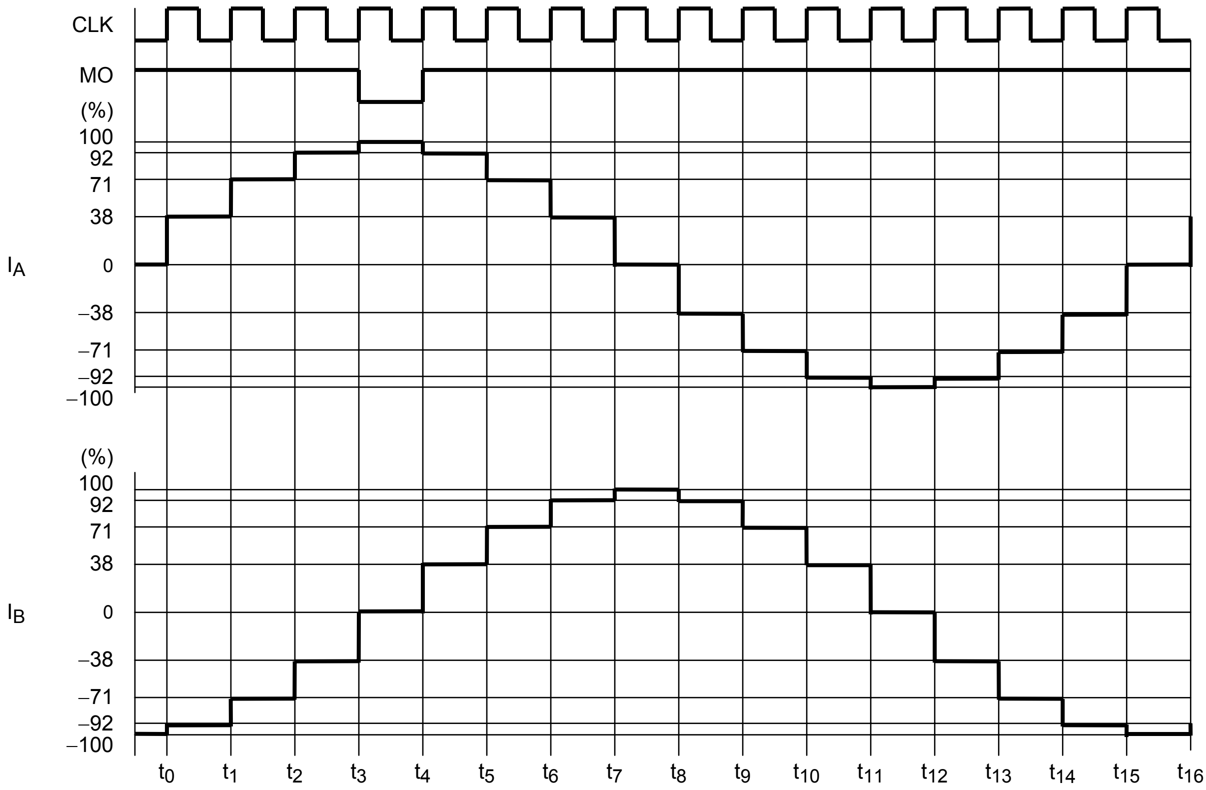


1/2-step Excitation Mode (B type) (M1: L, M2: H, M3: H, CCW Mode)

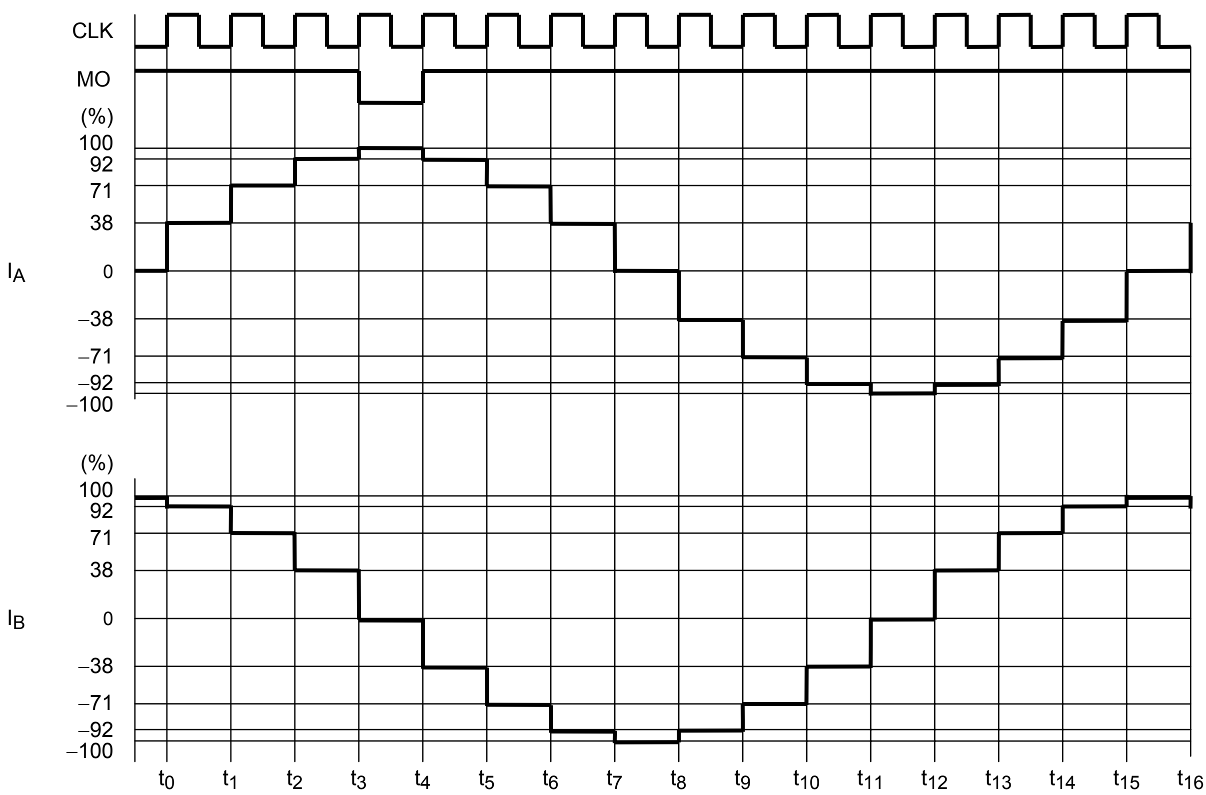


It operates from the initial state after the excitation mode is switched.

1/4-step Excitation Mode (M1: H, M2: L, M3: L, CW Mode)

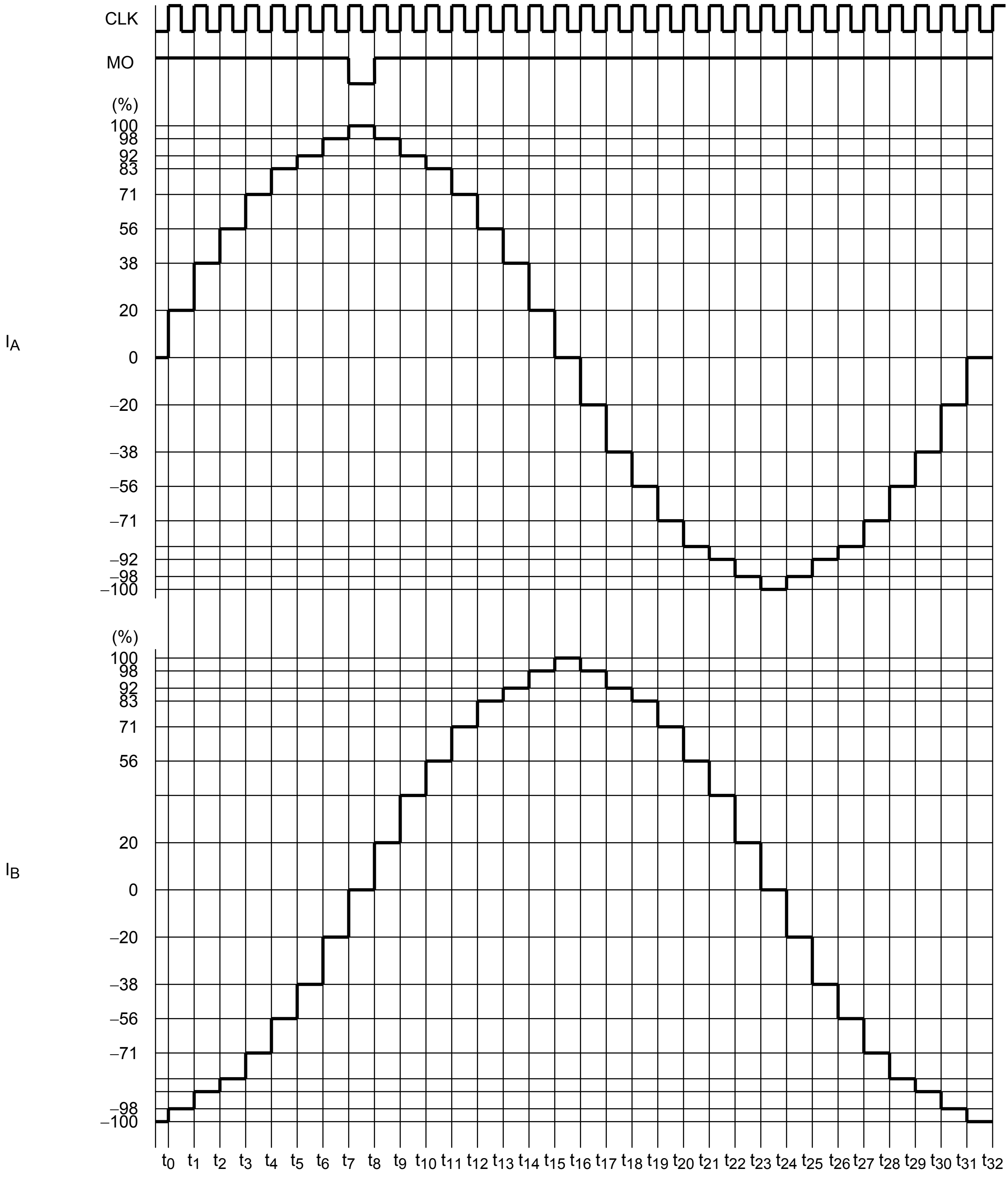


1/4-step Excitation Mode (M1: H, M2: L, M3: L, CCW Mode)



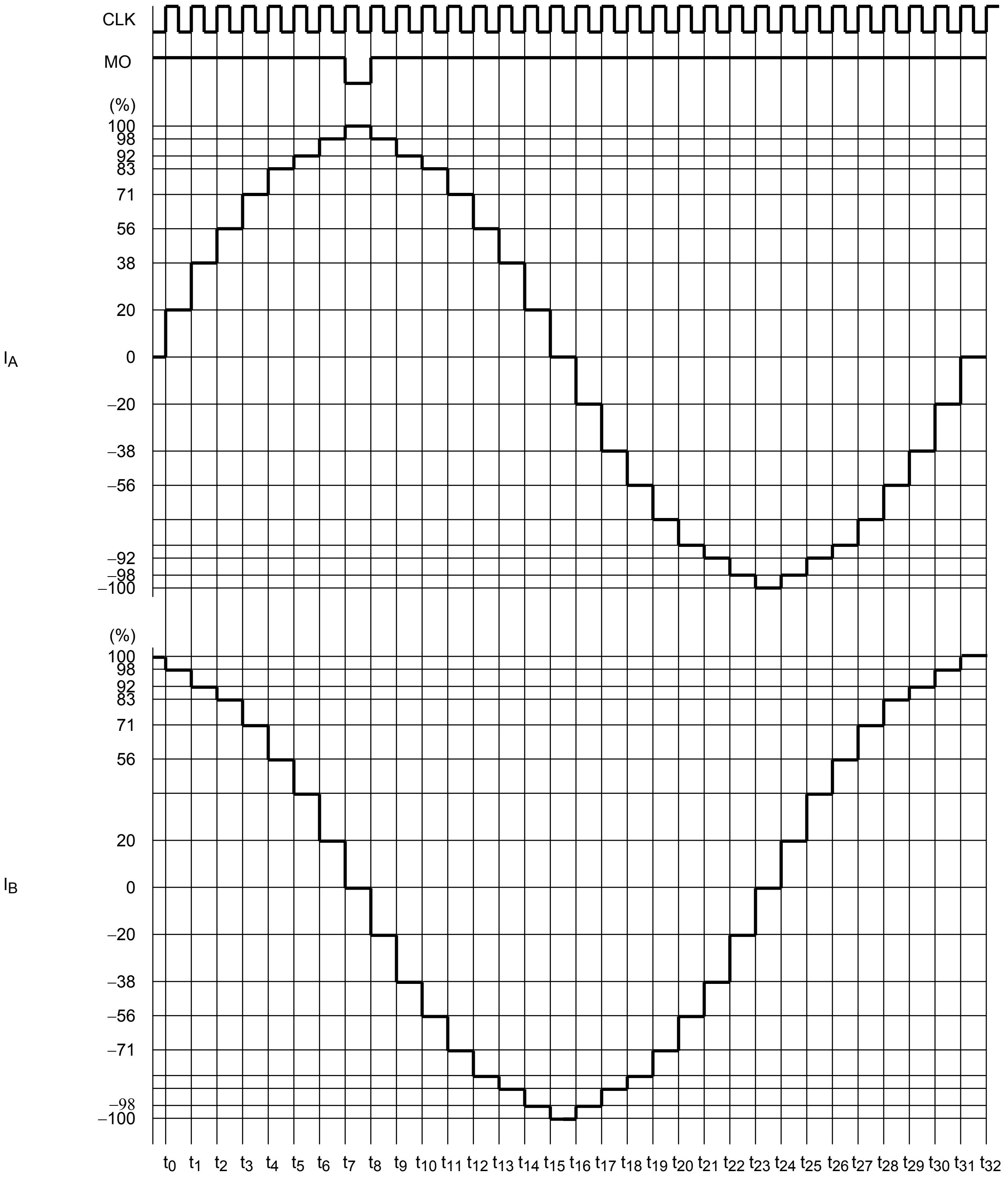
It operates from the initial state after the excitation mode is switched.

1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CW Mode)



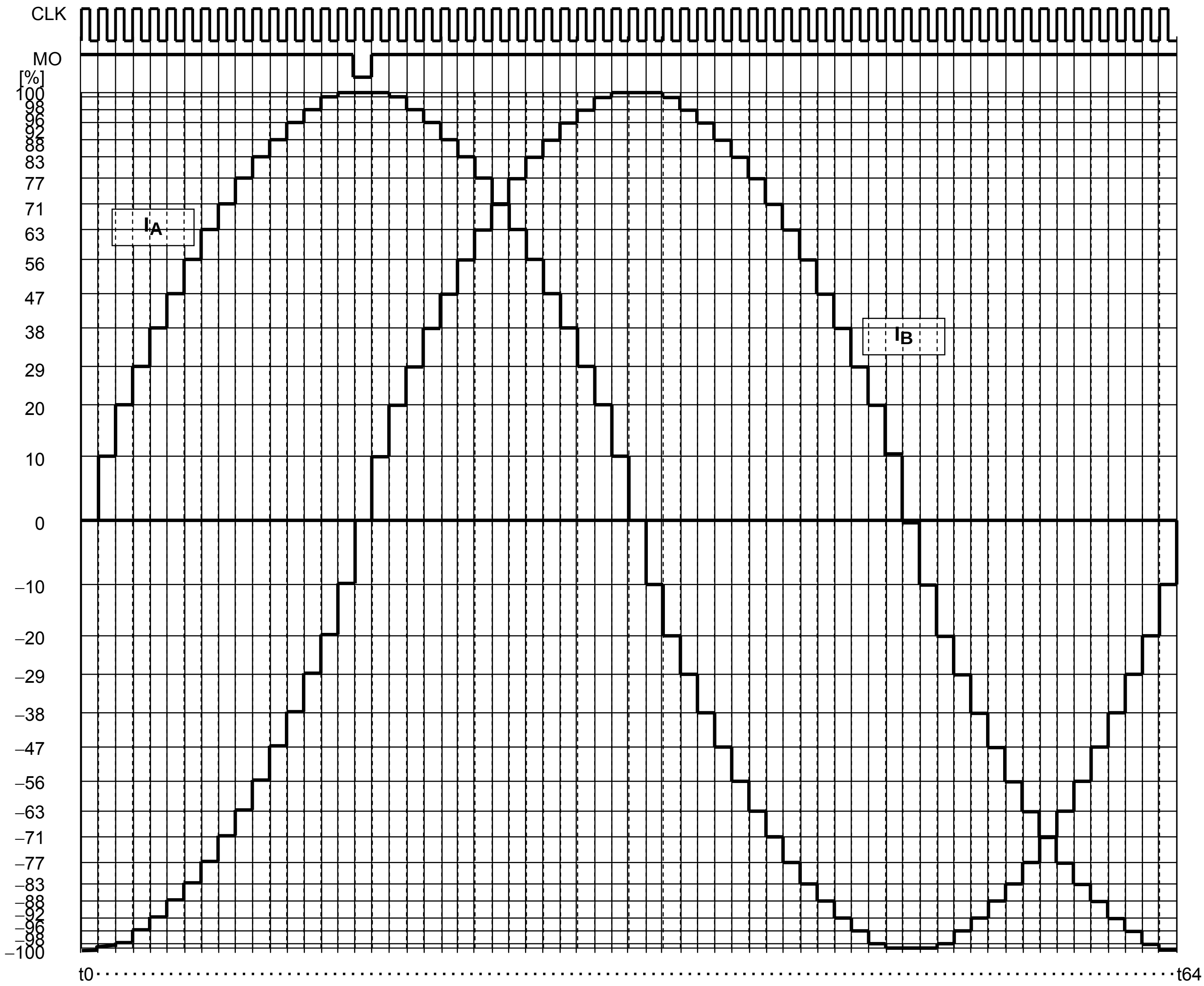
It operates from the initial state after the excitation mode is switched.

1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CCW Mode)



It operates from the initial state after the excitation mode is switched.

1/16-step Excitation Mode (M1: H, M2: H, M3: L, CW Mode)

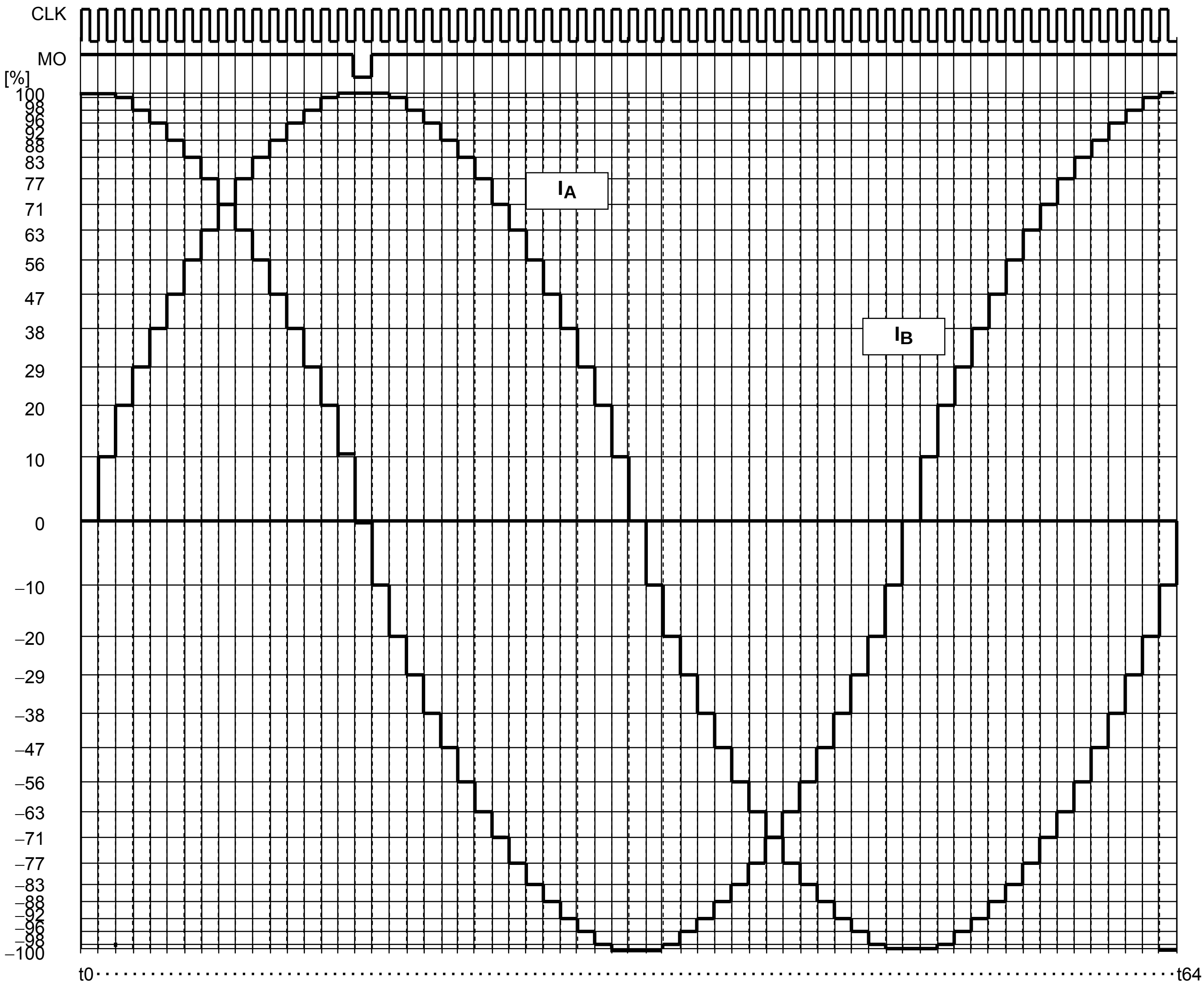


It operates from the initial state after the excitation mode is switched.

1

V1．0．14

1/16-step Excitation Mode (M1: H, M2: H, M3: L, CCW Mode)



It operates from the initial state after the excitation mode is switched.

1

V1. 0. 14

Current level

2-phase, 1-2-phase, W1-2-phase, 2W1-2-phase, 4W1-2-phase excitation (unit : %)

Current level（1/16, 1/8, 1/4, 1/2, 1/1 ）

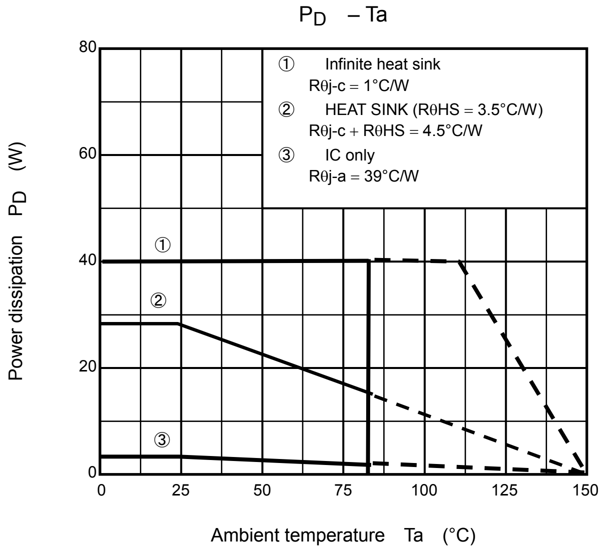
1/16, 1/8, 1/4, 1/2, 1/1	Min.	Typ.	Max.	Unit
θ16	---	100.0	---	%
θ15	95.5	99.5	100.0	
θ14	94.1	98.1	100.0	
θ13	91.7	95.7	99.7	
θ12	88.4	92.4	96.4	
θ11	84.2	88.2	92.2	
θ10	79.1	83.1	87.1	
θ9	73.3	77.3	81.3	
θ8	66.7	70.7	74.7	
θ7	59.4	63.4	67.4	
θ6	51.6	55.6	59.6	
θ5	43.1	47.1	51.1	
θ4	34.3	38.3	42.3	
θ3	25.0	29.0	33.0	
θ2	15.5	19.5	23.5	
θ1	5.8	9.8	13.8	
θ0	---	0.0	---	

1

V1．0．14

Power Dissipation

TB6600HQ



1. How to Turn on the Power

In turning on and off the power, abnormal output is not recognized. Supply monitoring circuit is added in necessary. IC is not damaged in case the order of turning on the power method is not correct. Vref is within the operation range when each input terminal (M1, M2, M3, CLK, CW/CCW, ENABLE, RESET, DCY, TQ, and Latch/Auto) is high or low level and IC is not damaged in turning on the power.

The following is an example. The sequence of turning on the power is not restricted and IC is not damaged when each input pin outputs high and the power supply pin outputs 0 V.

(Example 1): ENABLE = High → RESET = High

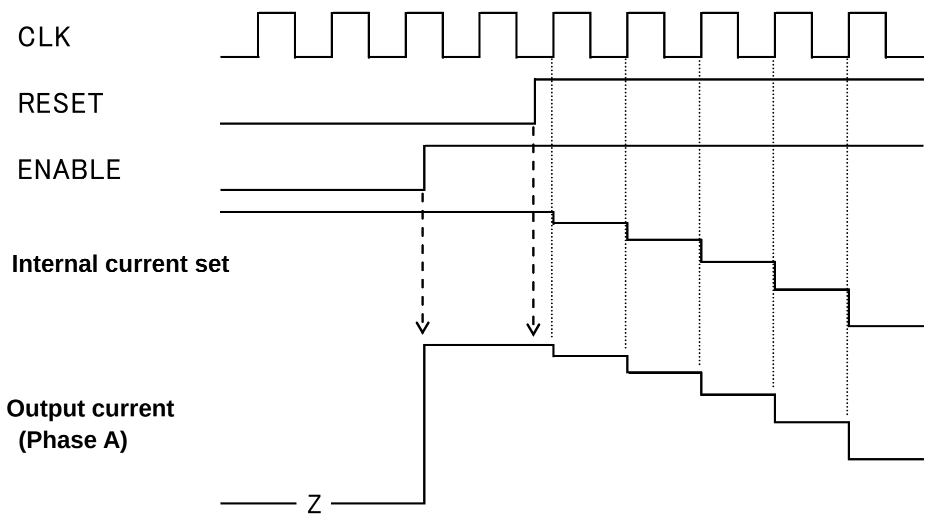
(Example 2): RESET = High → ENABLE = High

In example 1, motor can start driving from the initial mode.

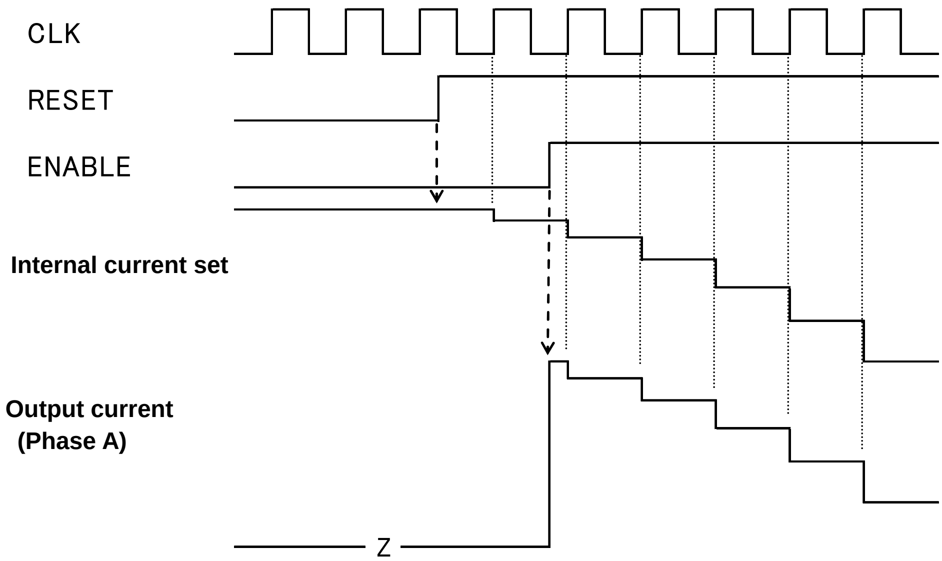
(1) CLK: Current step proceeds to the next mode with respect to every rising edge of CLK.
(2) ENABLE: It is in Hi-Z state in low level. It is output in high level.
RESET: It is in the initial mode (Phase A100% and Phase B %) in low level.
①ENABLE=Low and RESET=Low: Hi-Z. Internal current setting is in initial mode.
②ENABLE=Low and RESET=High: Hi-Z. Internal current setting proceeds by internal counter.
③ENABLE=High and RESET=Low: Output in the initial mode (Phase A100% and Phase B%).
②ENABLE=High and RESET=High: Output at the value which is determined by the internal counter.

<Recommended control input sequence>

(Example 1)



(Example 2)



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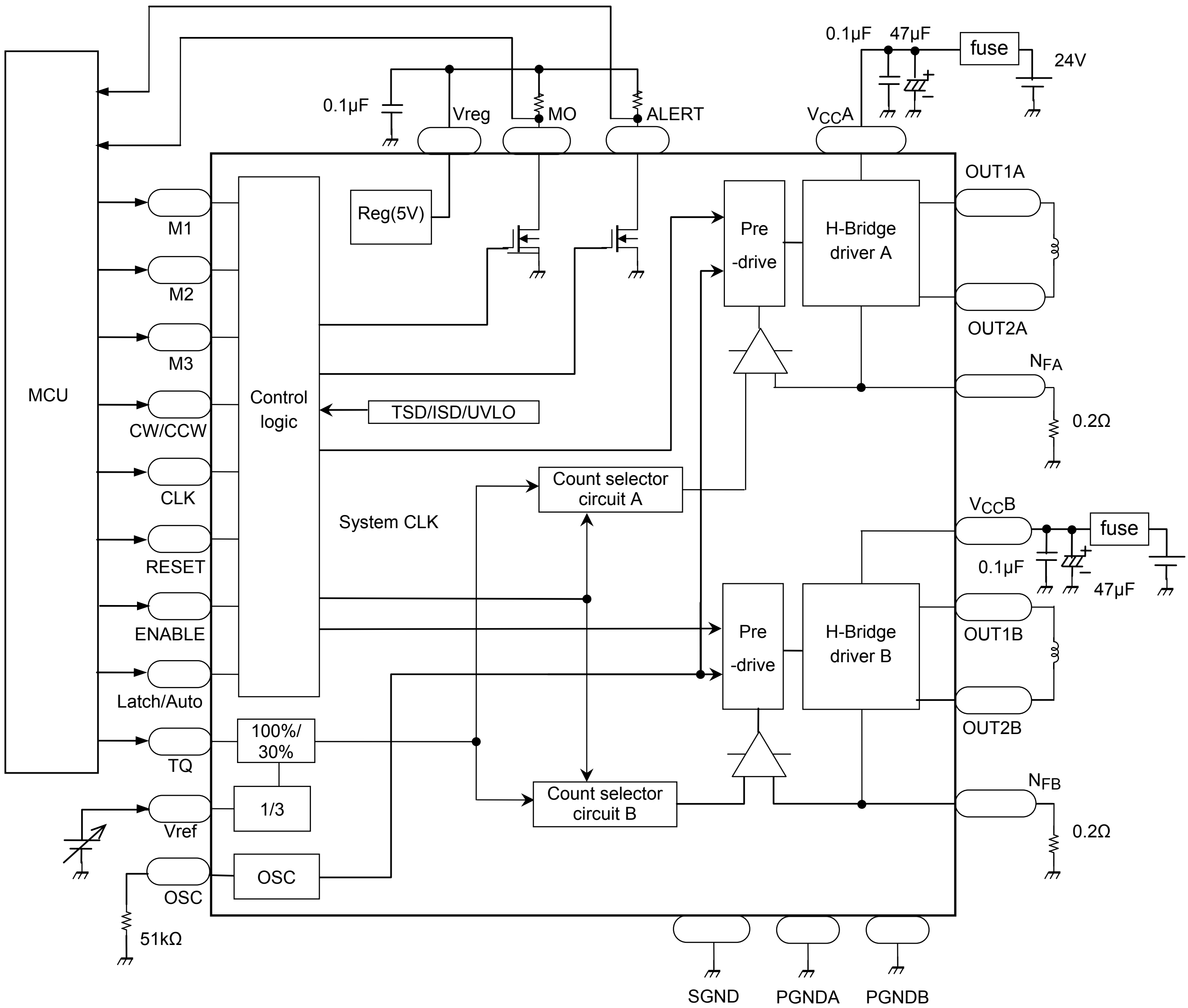
V1. 0. 14

Application Circuit

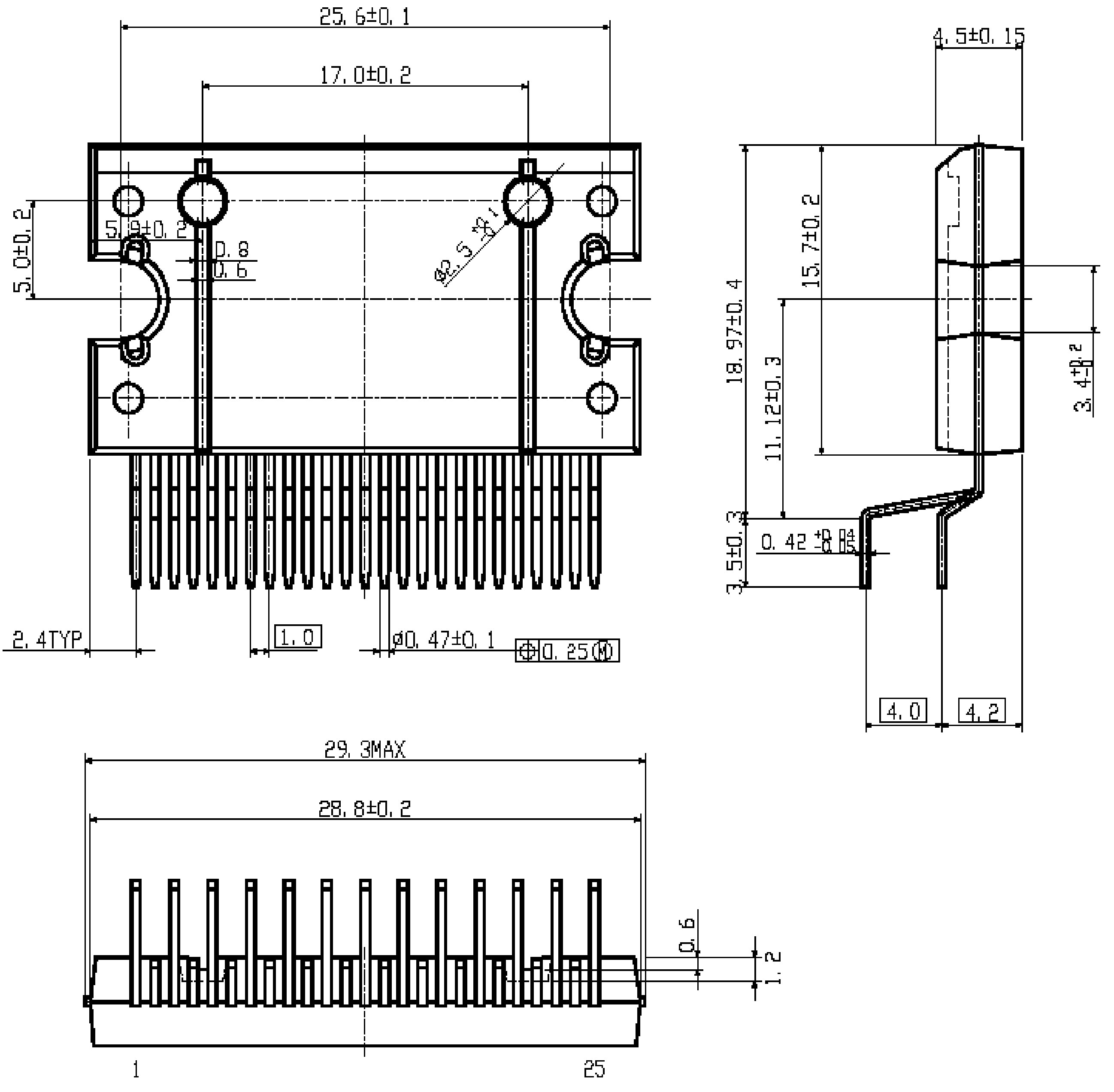


Note 1: Capacitors for the power supply lines should be connected as close to the IC as possible.

Note 2: Current detecting resistances (RNFA and RNFB) should be connected as close to the IC as possible.
External capacitor connected to Vreg: 0.1μF

Package Dimensions

Unit: mm



Weight: 7.7 g (typ.)

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V1. 0. 14

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(5) Others

Utmost care is necessary in the design of the output, V_{CC}, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

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