



# TOSHIBA Bi-CMOS Constant Current Interface Driver

## TB62701AN

16 Bit Constant Current LED Driver with Shift Register and Latch Functions

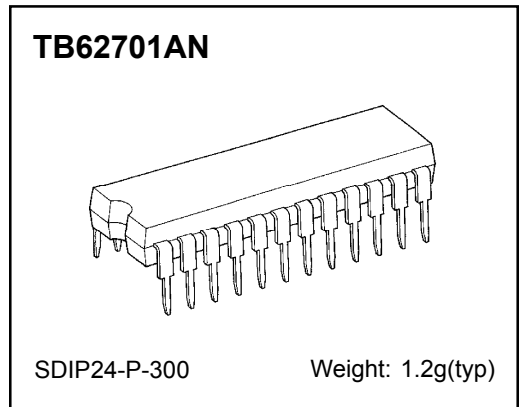
### Product Description:

The TB62701AN is specifically designed for LED display applications. The Bi-CMOS device has 16 Bi-polar constant current output channels and includes CMOS shift register and latch functions.

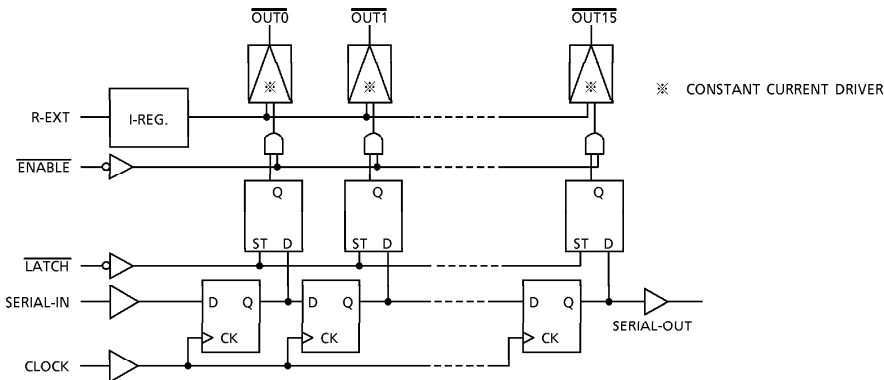
The LED drive current is programmed by the installation of a single resistor per device. Current is programmable from 5-50mA and is held constant across all 16 outputs effectively compensating for the inherent circuit and component variables which affect the brightness of the LEDs.

### Features:

- 16 Constant Current Output Channels
- Current Programmable from 5-50mA
- 5V CMOS Compatible Inputs
- Supports up to a 30V LED Supply Voltage



### Block Diagram:

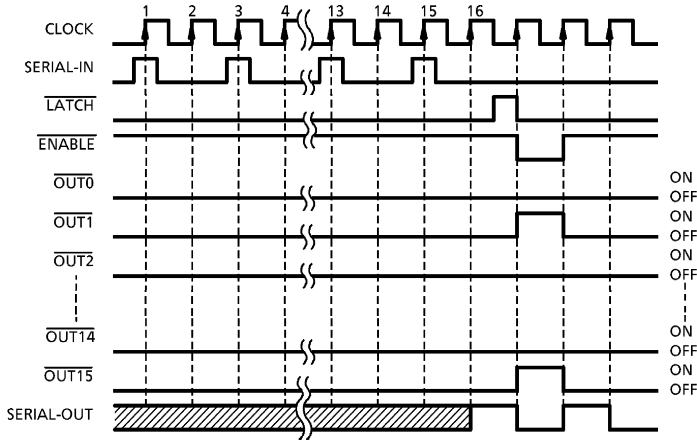


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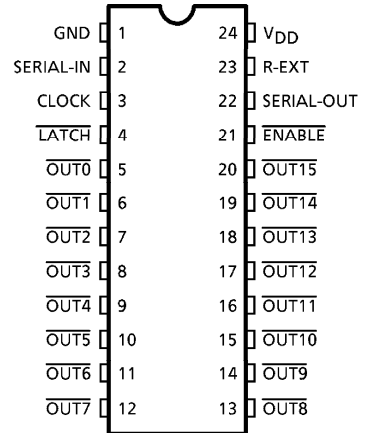
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### Timing Diagram:



### Terminal Description & Pin Out:

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL-IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up-edge
4	LATCH	"H" : data through, "L" : data hold
24	V <sub>DD</sub>	Supply voltage terminal
5~12 13~20	OUTn	Output terminals
21	ENABLE	"H" output off, "L" : latch data = "H" then output on, latch data = "L" then output off
22	SERIAL-OUT	Serial data output terminal for shift register
23	R-EXT	The register which connects between R-EXT and GND sets the constant output current.





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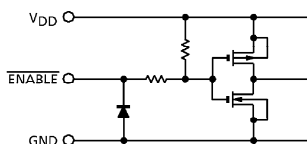
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Truth Table:

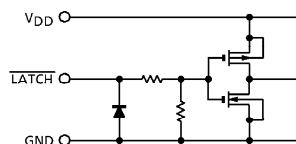
INPUT				OUTPUT $\overline{\text{OUT}}_n$ ( $t = n$ )			
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT}}_0$	$\overline{\text{OUT}}_7$	$\overline{\text{OUT}}_{15}$	SERIAL-OUT
Up	H	L	DN	DN	DN-7	DN-15	DN-15
Up	L	L	DN	No Change			DN-15
Up	*	H	DN	OFF	OFF	OFF	DN-15
Down	*	*	DN	No Change			No Change

Equivalent Circuit of Inputs and Outputs:

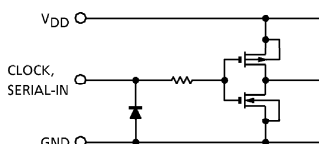
1. ENABLE terminal



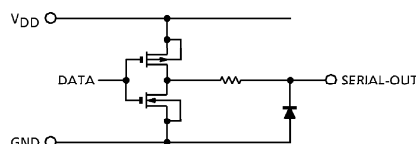
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



Maximum Ratings:

CHARACTER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0~+7.0	V
Output Voltage	VOUT	-0.5~+30	V
Output Current	IOUT	50	mA
Input Voltage	VIN	-0.4~VDD + 0.4	V
GND Terminal Current	IGND	800	mA
Clock Frequency	FCLK	2.5	MHz
Power Dissipation	PD	1.78	W
Operating Temperature	Topr	-40~+85	°C
Storage Temperature	Tstg	-55~+150	°C

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### Recommended Operating Condition

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	4.5	5.0	5.5	V
Output Voltage	VOUT	—	—	—	30.0	V
Output Current	OUTn	DC 1 circuit	—	—	45	mA
	S-OUT	IOH	—	—	-1.0	
		IOL	—	—	1.0	
Input Voltage	VIN	—	0	—	VDD	V
Data Set Up Time	tsetup(D)	—	100	—	—	ns
Data Hold Time	thold (D)	—	20	—	—	ns
Latch Set Up Time	tsetup(L)	—	300	—	—	ns
Latch Hold Time	thold (L)	—	100	—	—	ns
Clock Pulse Width	tw CLK	—	100	—	—	ns
	tw $\overline{\text{CLK}}$	—	100	—	—	ns
Latch Pulse Width	tw LAT	—	300	—	—	ns
	tw $\overline{\text{LAT}}$	—	300	—	—	ns
Clock Frequency	fCK	Cascade operation	—	—	2.0	MHz
Power Dissipation	PD	Ta=85°C	—	—	0.72	W



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#### Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Input Voltage	"H" level	V <sub>IH</sub>	—	—	70%VDD	—	VDD	V	
	"L" level	V <sub>IL</sub>	—	—	GND	—	30%VDD		
Output Leakage Current		I <sub>OH</sub>	—	V <sub>OH</sub> =30V	—	—	10	μA	
Output Voltage	S-OUT	V <sub>OL</sub>	—	I <sub>OL</sub> =+1.0mA	—	—	0.4	V	
		V <sub>OH</sub>	—	I <sub>OH</sub> =-1.0mA	4.6	—	—		
Output Current 1		I <sub>OL1</sub>	—	V <sub>CE</sub> =0.7V	REXT=560Ω (include ΔI <sub>OL1</sub> )	35.2	41.5	47.7	mA
		I <sub>OL2</sub>	—	V <sub>CE</sub> =0.4V		33.1	39.0	44.9	mA
Delta I <sub>OUT</sub>		ΔI <sub>OL1</sub>	—	REXT=560Ω I <sub>OUT</sub> =40mA, V <sub>CE</sub> =0.4V	—	±3.0	±7.0	%	
Supply Voltage Regulation		% / VDD	—	REXT=560Ω	—	18	—	% / V	
Reference Voltage		V <sub>ref</sub>	—	REXT=560Ω, T <sub>a</sub> =-40~85°C	—	1.26	—	V	
Pull Up / Down Resistor		R <sub>IN</sub>	—	—	100	200	400	kΩ	
Supply Current	"OFF"	I <sub>IDD (off) 1</sub>	—	REXT=OPEN, OUT <sub>n</sub> =Off	—	0.4	0.6	mA	
		I <sub>IDD (off) 2</sub>	—	REXT=560Ω, OUT <sub>n</sub> =Off	—	6.5	10.0		
	"ON"	I <sub>DD (on)</sub>	—	REXT=560Ω, OUT <sub>n</sub> =Off	—	13.5	20.0		

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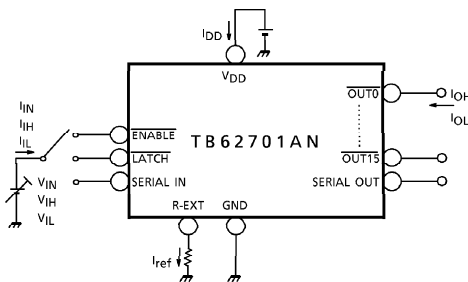


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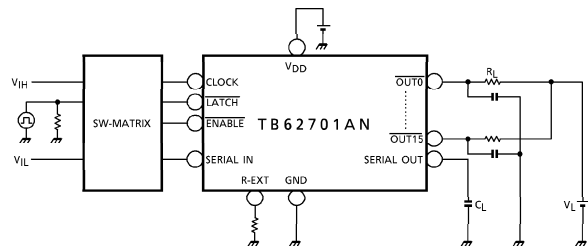
### Switching Characteristics:

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CK-S-OUT	$t_{PLH}$	VDD = 5.0V VCE = 1.0V VIH = VDD VIL = GND fCK = 2MHz REXT = 560Ω IOUT = 30mA	—	95	500	ns
	CK-OUTn			—	130	500	
	LATCH-OUTn			—	130	500	
	EN-OUTn			—	130	500	
Propagation Delay Time ("H" to "L")	CK-S-OUT	$t_{PLH}$		—	95	720	ns
	CK-OUTn			—	130	500	
	LATCH-OUTn			—	130	500	
	EN-OUTn			—	130	500	
Maximum Clock Frequency		fMAX(*1)		2.0	—	2.5	MHz
Minimum Pulse Width	CLK	tw CLK		—	45	80	ns
	LATCH	tw LAT	—	10	50		
Data Set Up Time		tsetup (D)	—	17	50	ns	
Data Hold Time		thold (D)	—	-7	10		
Latch Set Up Time	LH	$t_{LATsetup}$	—	70	200	ns	
	HL		—	70	200		
Latch Hold Time	LH	$t_{LAThold}$	—	-70	50	ns	
	HL		—	-70	50		
Maximum Clock Rise Time		tr	—	—	10	μs	
Maximum Clock Fall Time		tf	—	—	10		
Maximum Output Rise Time		tor	—	35	80	ns	
Maximum Output Fall Time		tof	—	40	80		

### DC Characteristic Test Circuit:



### AC Characteristic Test Circuit:



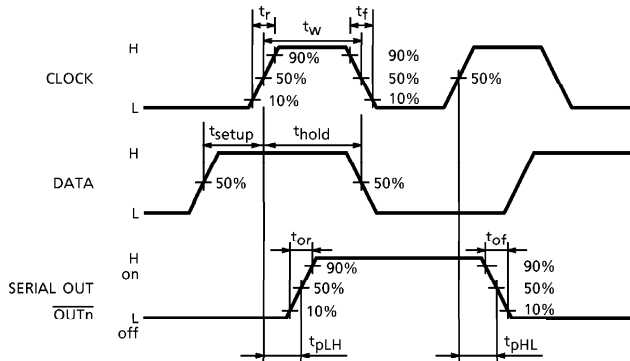


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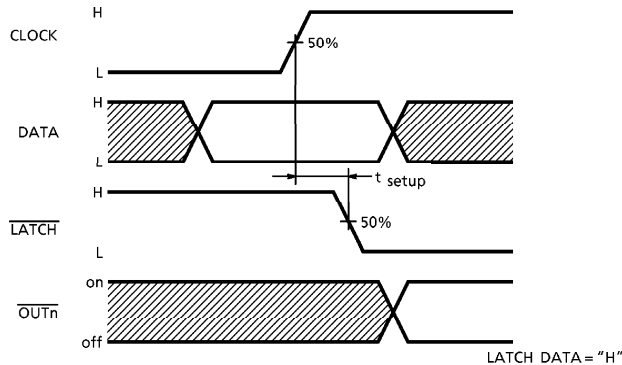
## TB62701AN

Timing Wave Form:

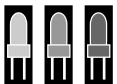
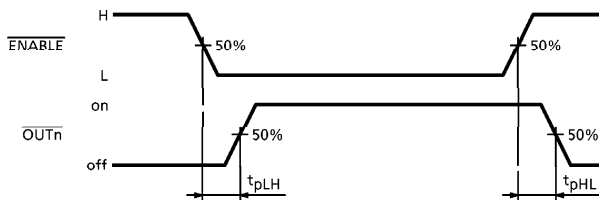
### 1. CLOCK-SERIAL OUT, OUT<sub>n</sub>



### 2. CLOCK-LATCH



### 3. ENABLE



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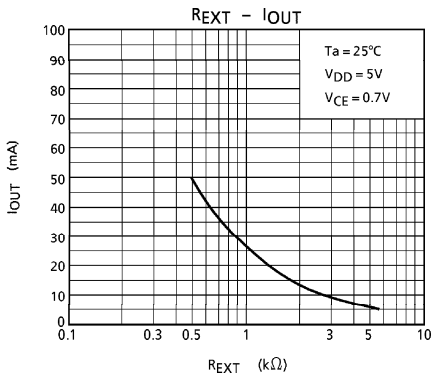
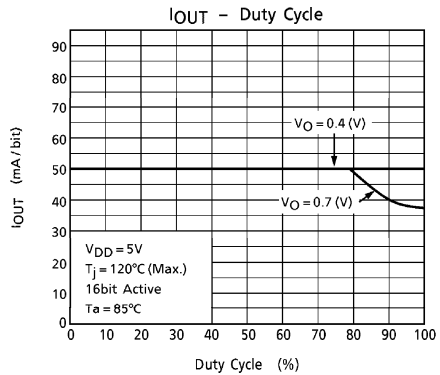
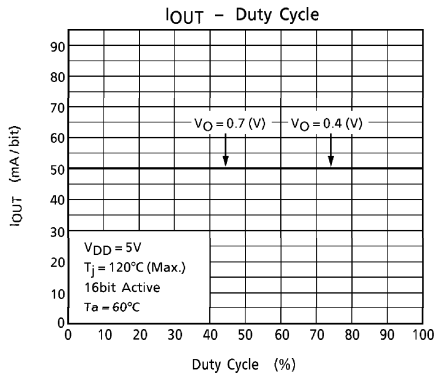
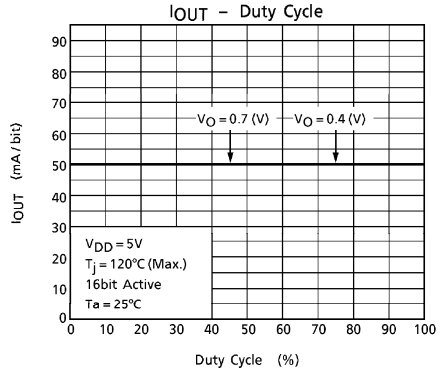
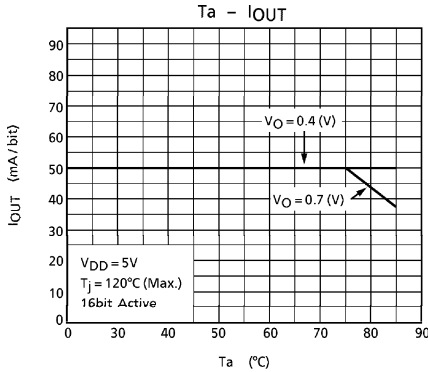
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Graphs:



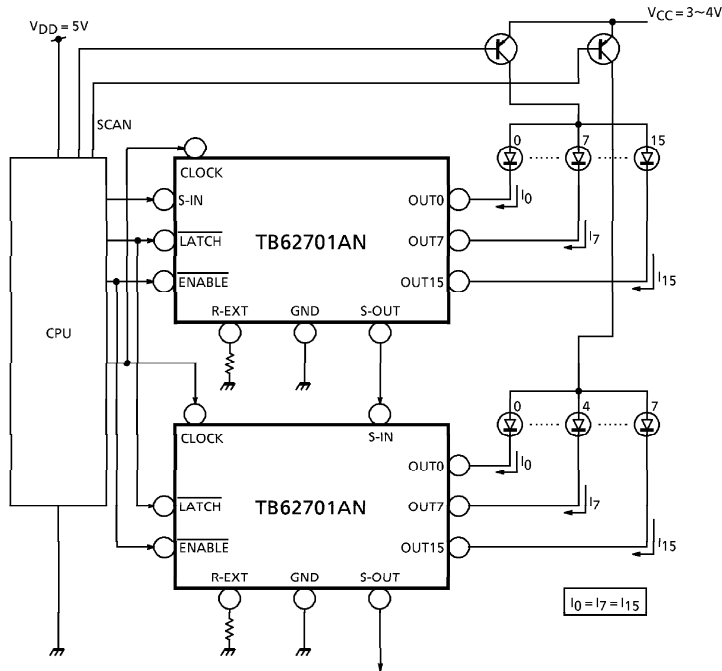




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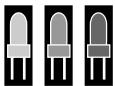
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Application Circuit:



### PRECAUTIONS for USING

Utmost care is necessary in the design of the output line,  $V_{CC}$  ( $V_{DD}$ ) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.



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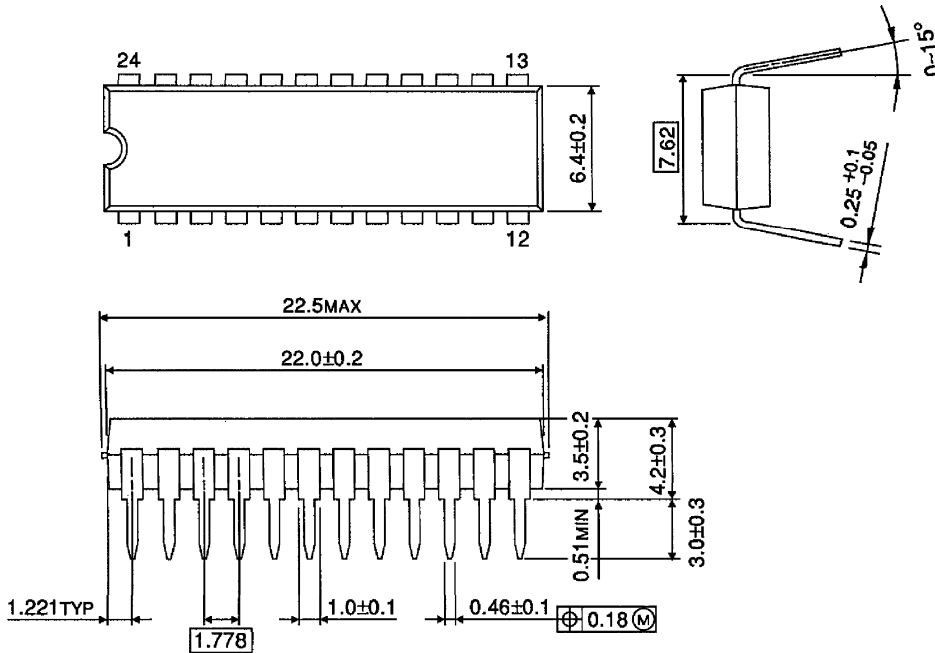


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Outline Drawing:

SDIP24-P-300-1.78

Unit : mm



Weight : 1.2g (Typ.)