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TAS5805M 23-W, Inductor-Less, Digital Input, Stereo, Closed-Loop Class-D Audio Amplifier with Enhanced Processing and Low Idle Power Dissipation

1 Features

- Supports Multiple Output Configurations
  - 2 × 23 W in 2.0 Mode (8-Ω, 21 V, THD+N=1%)
  - 45 W in Mono Mode (4-Ω, 21 V, THD+N=1%)
- Excellent Audio Performance
  - THD+N ≤ 0.03% at 1 W, 1 kHz, PVDD = 12 V
  - SNR ≥ 107 dB (A-weighted), Noise Level < 40 μV_{RMS}
- Low Quiescent Current with Hybrid Modulation
  - 16.5 mA at PVDD = 13.5 V , 22 µH + 0.68 µF Filter
- Flexible Power Supply Configurations
  - PVDD: 4.5 V to 26.4 V
  - DVDD and I/O: 1.8 V or 3.3 V
- Flexible Audio I/O
  - I^2S, LJ, RJ, TDM, 3-Wire Digital Audio Interface (No MCLK Required)
  - Supports 32, 44.1, 48, 88.2, 96 kHz Sample Rates
  - SDOUT for Audio Monitoring, Sub-Channel or Echo Cancellation
- Enhanced Audio Processing
  - Multi-Band Advanced DRC and AGL
  - 2×15 BQs, Thermal Foldback, DC Blocking
  - Input Mixer, Output Crossbar, Level Meter
  - 5 BQs + 1 Band DRC +THD Manager for the Subwoofer Channel
- Integrated Self-Protection
  - Adjacent Pin to Pin Short Without Device Damage
  - Over-Current Error (OCE)
  - Over-Temperature Warning (OTW)
  - Over-Temperature Error (OTE)
  - Under/Over-Voltage Lock-out (UVLO/OVLO)
- Easy System Integration
  - I^2C Software Control
  - Reduced Solution Size
    - Fewer Passives Required Compared to Open-Loop Devices
    - Inductor-less Operation (Ferrite Bead) for most cases where PVDD ≤ 14V

2 Applications

- LCD TV, OLED TV
- Wireless Speaker, Smart Speaker with Voice Assistant
- Soundbar, Wired Speaker , Bookshelf Stereo System
- Desktop PC, Notebook PC
- AV Receiver, Smart Home and IoT Appliance

3 Description

The TAS5805M is a high-efficiency, stereo, closed-loop Class-D amplifier offering a cost effective digital-input solution with low power dissipation and sound enrichment. The device’s integrated audio processor and 96 kHz architecture supports advanced audio process flow, including SRC, 15 BQs per channel, volume control, audio mixing, 3-band 4th order DRC, full-band AGL, THD managing and level meter.

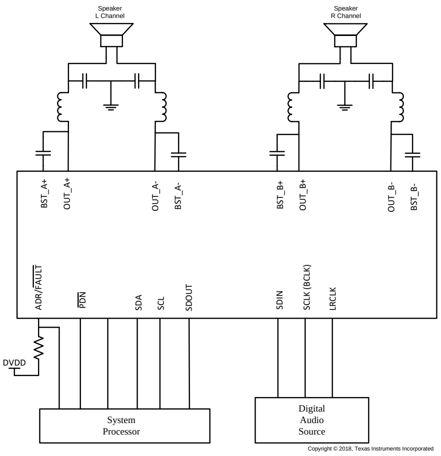
Featuring TI's proprietary Hybrid Modulation scheme, the TAS5805M consumes very-low quiescent current (<16.5 mA at 13.5V PVDD), extending battery life in portable audio applications. With advanced EMI suppression technology, designers can leverage inexpensive ferrite bead filters to reduced board space and system cost.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5805M	TSSOP (28) PWP	9.7 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

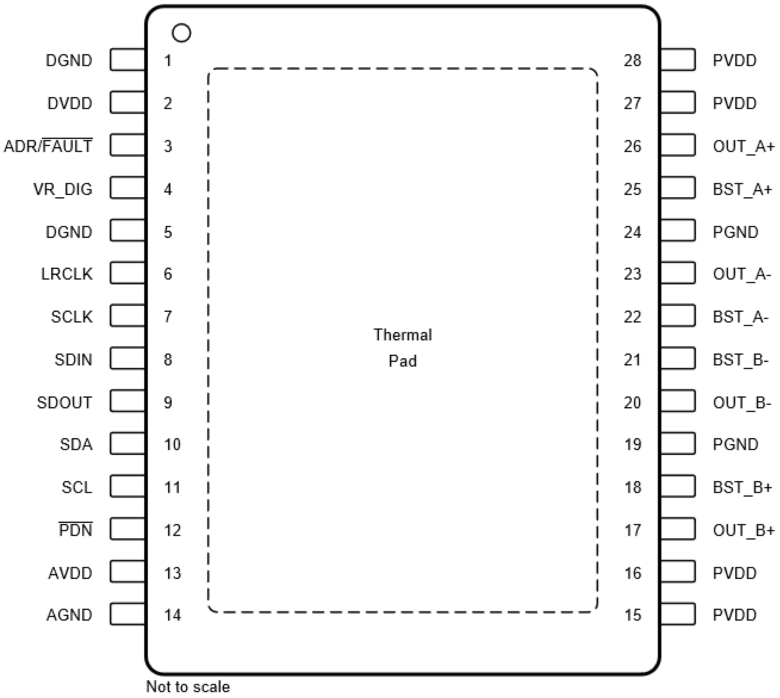
Changes from Original (May 2018) to Revision A	Page
• Released as Production Data	1

5 Device Comparison Table

ORDERABLE PART NUMBER	RECOMMENDED PVDD RANGE	Audio Process Flows	$R_{DS(ON)}$
TAS5805M	4.5 V to 26.4 V	Enhanced Audio Process Flows with ROM Fixed	180 mΩ
TAS5707/TAS5711	8 V to 26 V	Basic Audio Process Flow with ROM Fixed	180 mΩ
TAS5825M	4.5 V to 26.4 V	Flexible Advanced Audio Process Flows with Smart-Amp Features	90 mΩ

6 Pin Configuration and Functions

PWP Package
28-Pin TSSOP



Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DGND	1, 5	P	Digital ground
DVDD	2	P	3.3-V or 1.8-V digital power supply
VR_DIG	4	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
ADR/$\overline{\text{FAULT}}$	3	DI/O	Different I^{2} C device address can be set by selecting different pull up resistor to DVDD, see Table 4 for details. This pin can be programed by Register 0x60h and 0x61h after Power up bit. In this mode, the ADR/$\overline{\text{FAULT}}$ Is redefined as $\overline{\text{FAULT}}$
LRCLK	6	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^{2}S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
SCLK	7	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
SDIN	8	DI	Data line to the serial data port
SDOUT	9	DO	Serial Audio data output. The source data can be Pre-DSP or Post DSP data, by setting the register 0x30h.
SDA	10	DI/O	I2C serial control data interface input/output

[1] AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	**NO.**		
SCL	11	DI	I2C serial control clock input
$\overline{\text{PDN}}$	12	DI	Power Down, active-low.$\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators. Low, Power Down Device; High, Enable Device.
AVDD	13	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices
AGND	14	P	Analog ground
PVDD	15,16,27, 28	P	PVDD voltage input
PGND	19,24	P	Ground reference for power device circuitry. Connect this pin to system ground.
OUT_A+	26	O	Positive pin for differential speaker amplifier output A+
BST_A+	25	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
OUT_A-	23	O	Negative pin for differential speaker amplifier output A-
BST_A-	22	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
BST_B-	21	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
OUT_B-	20	O	Negative pin for differential speaker amplifier output B
BST_B+	18	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
OUT_B+	17	O	Positive pin for differential speaker amplifier output B+
PowerPAD™		P	Connect to the system Ground

7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs (2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature	–25	85	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SCL, SDA, SDIN,$\overline{\text{PDN}}$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	
R_{SPK}	Minimum speaker load	BTL Mode (4.5V≤PVDD≤16V)	3.2			Ω
		BTL Mode (16V<PVDD≤24V)	4.8			Ω
R_{SPK}	Minimum speaker load	PBTL Mode (4.5V≤PVDD≤16V)	1.6			Ω
		PBLT Mode (16V<PVDD≤24V)	2.4			Ω
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1	4.7		µH

7.4 Thermal Information

THERMAL METRIC (1)		TAS5805M TSSOP (PWP) 28 PINS			UNIT
		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5805MEVM-4 4-LAYER PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	29.1	24	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	21.8	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	8.2	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	0.3	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	8.1	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	µA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = 0$ V			–10	µA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	$I_{OH} = 2$ mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	$I_{OH} = –2$ mA			20%	V_{DVDD}
I^2C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)						
I_{cc}	Quiescent supply current on DVDD	$\overline{PDN}$=2V, DVDD=3.3V, Play mode		18		mA
I_{cc}	Quiescent supply current on DVDD	$\overline{PDN}$=2V, DVDD=3.3V, Sleep mode		0.75		mA
I_{cc}	Quiescent supply current on DVDD	$\overline{PDN}$=2V, DVDD=3.3V, Deep Sleep mode		0.75		mA
I_{cc}	Quiescent supply current on DVDD	$\overline{PDN}$=0V, DVDD=3.3V, Shutdown mode		5.5		µA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=2V,, PVDD=13.5V, LC filter=10uH+0.68uF, Fsw=768kHz, BD Modulation, Play mode		32.5		mA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=2V,, PVDD=13.5V, LC filter=22uH+0.68uF, Fsw=384kHz, Hybrid Modulation, Play mode		16.5		mA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=2V, PVDD=13.5V, Output Hiz Mode		10.4		mA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=2V, PVDD=13.5V, Sleep Mode		7.2		mA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=2V, PVDD=13.5V, Deep Sleep Mode		120		µA
I_{cc}	Quiescent supply current on PVDD	$\overline{PDN}$=0V, PVDD=13.5V, Shutdown Mode		7.2		µA
t_{off}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD). Measured at 0 dB input(1FS)	4.87		29.5	V
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 29.5 Vp/FS		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier			384		kHz
				768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization		180		mΩ

Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCE$_{\text{THRES}}$	Over-Current Error Threshold	OUTxx Overcurrent Error Threshold		5		A
OVE$_{\text{THRES(PVDD}}$	PVDD over voltage error threshold			28		V
UVE$_{\text{THRES(PVDD}}$	PVDD under voltage error threshold			4.2		V
OTE$_{\text{THRES}}$	Over temperature error threshold			160		°C
OTE$_{\text{Hystersis}}$	Over temperature error hysteresis			10		°C
OTW$_{\text{THRES}}$	Over temperature warning level	Read by register 0x73 bit3		135		°C
SPEAKER AMPLIFIER (STEREO BTL)						
|V$_{\text{OS}}$|	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 Vp gain, V$_{\text{PVDD}}$ = 12 V, BD Mode	–6.5		6.5	mV
P$_{\text{O(SPK)}}$	Continuous Output power (per channel)	V$_{\text{PVDD}}$ = 21V, SPK_GAIN = 24.8 Vp/FS, R$_{\text{SPK}}$ = 8 Ω, f = 1 kHz, THD+N = 1%, 1SPW Mode		23		W
		V$_{\text{PVDD}}$ = 21 V, SPK_GAIN = 24.8 Vp/FS, R$_{\text{SPK}}$ = 8 Ω, f = 1 kHz, THD+N = 10%, 1SPW Mode		27.5		W
		V$_{\text{PVDD}}$ = 18 V, SPK_GAIN = 20.8 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz, THD+N = 1%, BD Mode		21		W
		V$_{\text{PVDD}}$ = 18 V, SPK_GAIN = 20.8 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz, THD+N = 10%, BD Mode		25		W
		V$_{\text{PVDD}}$ = 12 V, SPK_GAIN = 13.9 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		9.9		W
		V$_{\text{PVDD}}$ = 12 V, SPK_GAIN = 13.9 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz THD+N = 10%, BD Mode		12		W
		V$_{\text{PVDD}}$ = 13.5 V, SPK_GAIN = 15.6 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		12		W
		V$_{\text{PVDD}}$ = 13.5 V, SPK_GAIN = 15.6 Vp/FS, R$_{\text{SPK}}$ = 6 Ω, f = 1 kHz THD+N = 10%, BD Mode		15		W
THD+N$_{\text{SPK}}$	Total harmonic distortion and noise (P$_{\text{O}}$ = 1 W, f = 1 KHz, R$_{\text{SPK}}$ = 6 Ω)	V$_{\text{PVDD}}$ = 12 V, Fsw=768kHz, SPK_GAIN = 13.9 Vp/FS, LC-filter, BD Mode		0.03%		
		V$_{\text{PVDD}}$ = 18 V, Fsw=768kHz, SPK_GAIN = 20.8 Vp/FS, LC-filter, BD Mode		0.03%		
I$_{\text{CN(SPK)}}$	Idle channel noise(A-weighted)	V$_{\text{PVDD}}$ = 12 V, Fsw=768kHz, LC-filter, Load=6 Ω		37		µVrms
		V$_{\text{PVDD}}$ = 18 V, Fsw=768kHz, LC-filter, Load=6 Ω		38		
DR	Dynamic range	A-Weighted, -60 dBFS method. P$_{\text{VDD}}$ = 24 V, SPK_GAIN = 29.5 Vp/FS		106		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N output level, PVDD=24V		111		dB
		A-Weighted, referenced to 1% THD+N output level, PVDD=13.5V		107.5		dB
K$_{\text{SVR}}$	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V$_{\text{rms}}$, PVDD = 12 V, input audio signal = digital zero		72		dB
X-talk$_{\text{SPK}}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz		100		dB
SPEAKER AMPLIFIER (MONO PBTL)						
P$_{\text{O(SPK)}}$	Continuous Output Power	V$_{\text{PVDD}}$ = 12 V, SPK_GAIN = 13.9 Vp/FS, R$_{\text{SPK}}$ = 4 Ω, f = 1kHz, THD+N = 1%, BD Mode		15.4		W
		V$_{\text{PVDD}}$ = 12 V, SPK_GAIN = 13.9 Vp/FS, R$_{\text{SPK}}$ = 4 Ω, f = 1kHz, THD+N = 10%, BD Mode		18.5		W
		V$_{\text{PVDD}}$ = 18V, SPK_GAIN = 22.1 Vp/FS, R$_{\text{SPK}}$ = 4 Ω, f = 1kHz, THD+N = 1%, BD Mode		33.6		W
		V$_{\text{PVDD}}$ = 18 V, SPK_GAIN = 22.1 Vp/FS, R$_{\text{SPK}}$ = 4 Ω, f = 1kHz, THD+N = 10%, BD Mode		41		W

Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz)	V_{PVDD} = 12 V, SPK_GAIN = 16.5 Vp/FS, 4.7uH + 0.68uF filter, R_{SPK} = 4 Ω, BD Mode		0.06%		
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 Vp/FS, 4.7uH + 0.68uF filter, R_{SPK} = 4 Ω, 1SPW Mode		0.07%		
DR	Dynamic range	A-Weighted, -60 dBFS method, PVDD = 24V, SPK_GAIN = 29.5 Vp/FS		106		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N output level, PVDD=13.5V		107.7		dB
		A-Weighted, referenced to 1% THD+N output level, PVDD=24V		111		dB
K_{SVR}	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V_{rms}, P_{VDD} = 19 V, input audio signal = digital zero		72		dB

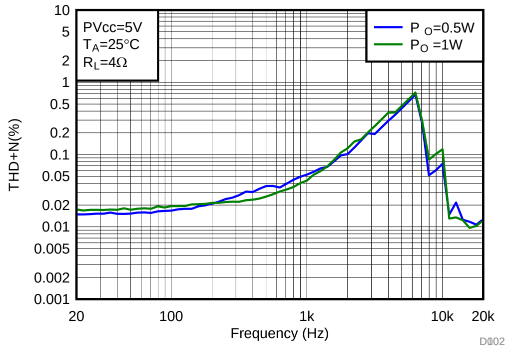
7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^{2}C Bus Timing – Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
$t_{RS\text{-}SU}$	Setup time for (repeated) START condition	4.7			µs
$t_{S\text{-}HD}$	Hold time for (repeated) START condition	4			µs
$t_{D\text{-}SU}$	Data setup time	250			ns
$t_{D\text{-}HD}$	Data hold time	0		900	ns
$t_{SCL\text{-}R}$	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
$t_{SCL\text{-}R1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
$t_{SCL\text{-}F}$	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
$t_{SDA\text{-}R}$	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
$t_{SDA\text{-}F}$	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
$t_{P\text{-}SU}$	Setup time for STOP condition	4			µs
I^{2}C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
$t_{RS\text{-}SU}$	Setup time for (repeated)START condition	600			ns
$t_{RS\text{-}HD}$	Hold time for (repeated)START condition	600			ns
$t_{D\text{-}SU}$	Data setup time	100			ns
$t_{D\text{-}HD}$	Data hold time	0		900	ns
$t_{SCL\text{-}R}$	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
$t_{SCL\text{-}R1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
$t_{SCL\text{-}F}$	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
$t_{SDA\text{-}R}$	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
$t_{SDA\text{-}F}$	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
$t_{P\text{-}SU}$	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns

7.7 Typical Characteristics

7.7.1 Bridge Tied Load (BTL) Configuration Curves

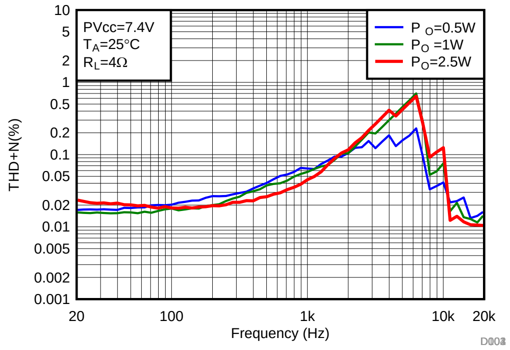
Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5805MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM Modulation mode set to 1SPW mode unless otherwise noted.



PVDD = 5 V 4.7uH+0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

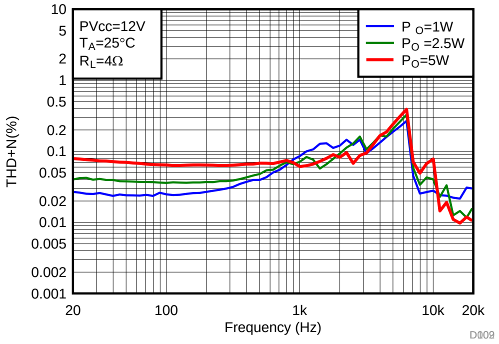
Figure 1. THD+N vs Frequency-BTL



PVDD = 7.4 V 4.7uH+0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

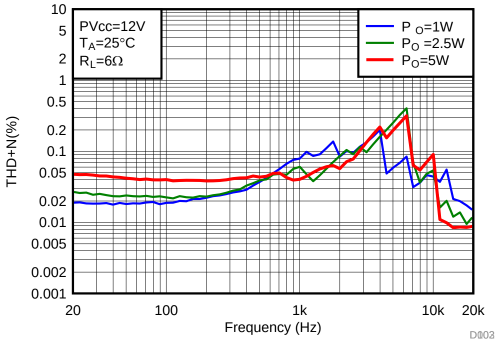
Figure 2. THD+N vs Frequency-BTL



PVDD = 12 V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 4Ω

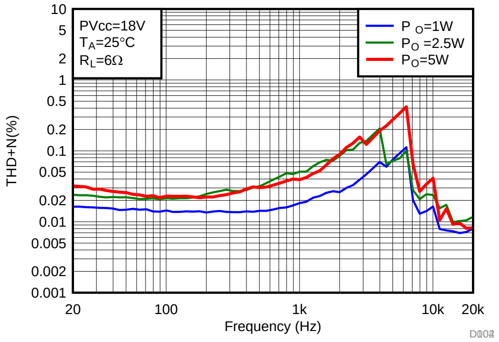
Figure 3. THD+N vs Frequency-BTL



PVDD = 12 V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

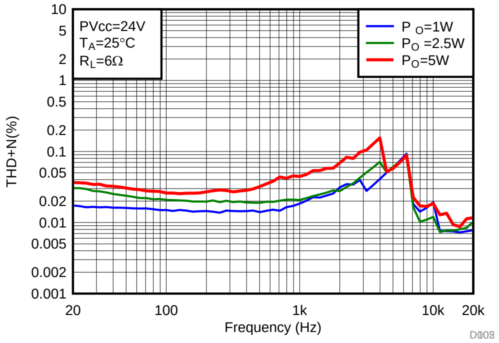
Figure 4. THD+N vs Frequency-BTL



PVDD = 18 V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

Figure 5. THD+N vs Frequency-BTL

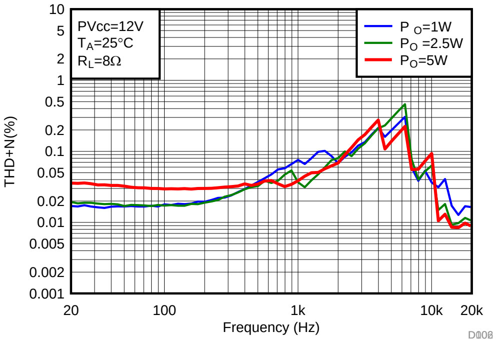


PVDD = 24 V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

Figure 6. THD+N vs Frequency-BTL

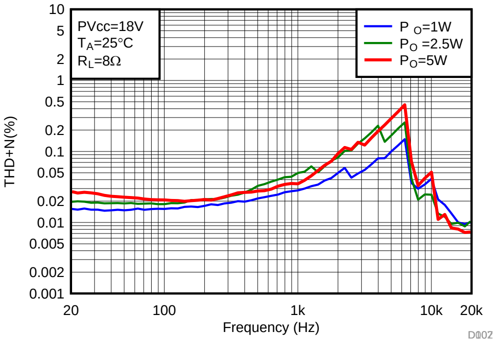
Typical Characteristics (continued)



PVDD = 12 V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

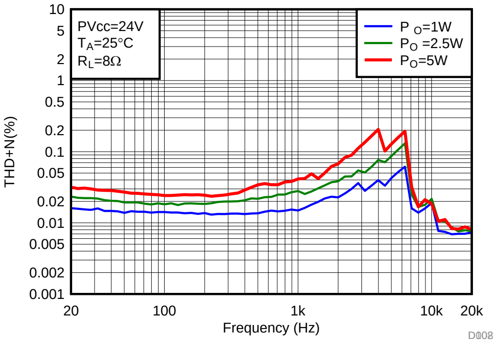
Figure 7. THD+N vs Frequency-BTL



PVDD = 18 V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

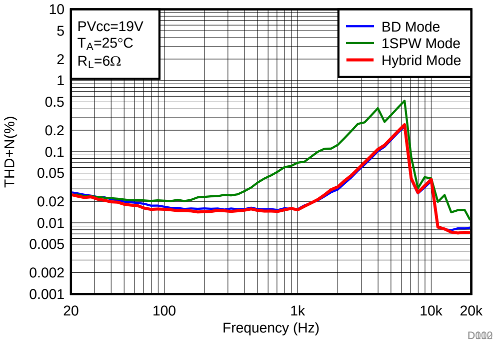
Figure 8. THD+N vs Frequency-BTL



PVDD = 24 V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

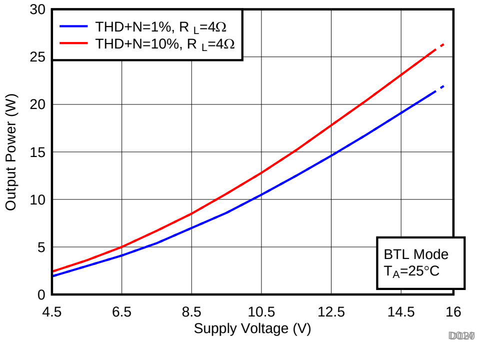
Figure 9. THD+N vs Frequency-BTL



PVDD = 19 V 10uH+0.68uF P_{OUT} = 5W

F_{SW} = 384 kHz BD/1SPW/Hybrid Load = 6Ω

Figure 10. THD+N vs Frequency-BTL

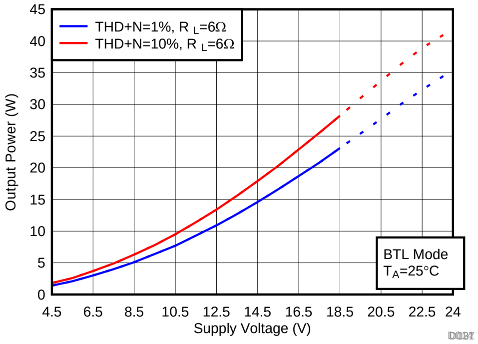


NOTE: Dashed lines represent thermally limited region for the continuous output power.

PVDD = 4.5 V~16V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 4Ω

Figure 11. Output Power vs Supply Voltage-BTL



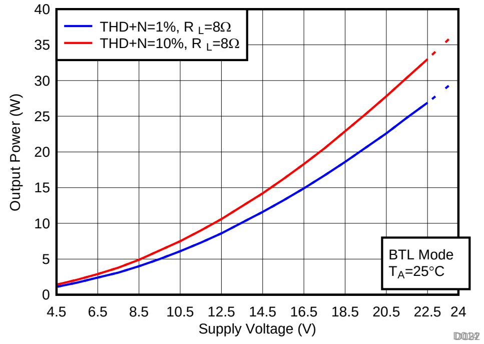
NOTE: Dashed lines represent thermally limited region for the continuous output power.

PVDD = 4.5 V~24V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

Figure 12. Output Power vs Supply Voltage-BTL

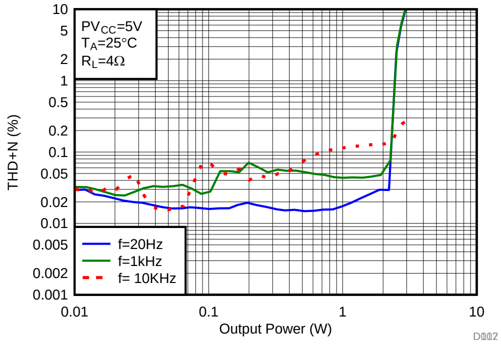
Typical Characteristics (continued)



PVDD = 4.5 V~24V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

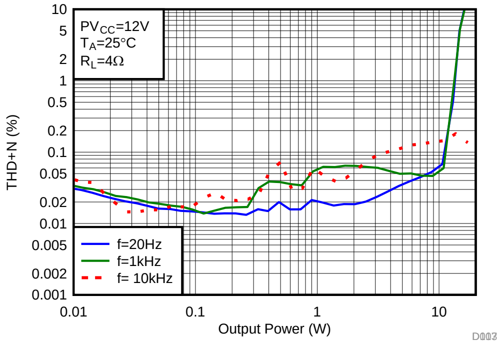
Figure 13. Output Power vs Supply Voltage-BTL



PVDD = 5V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 4Ω

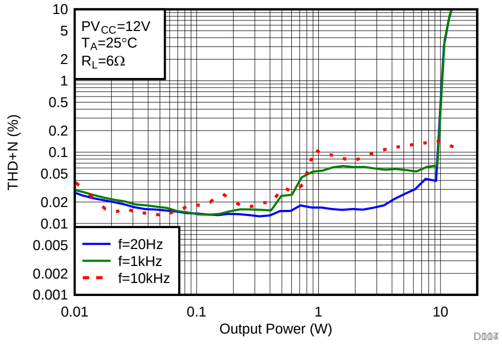
Figure 14. THD+N vs Output Power-BTL



PVDD = 12V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 4Ω

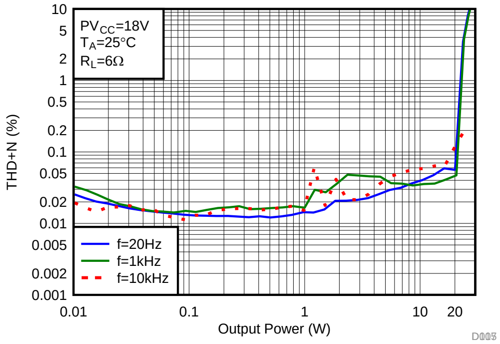
Figure 15. THD+N vs Output Power-BTL



PVDD = 12V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

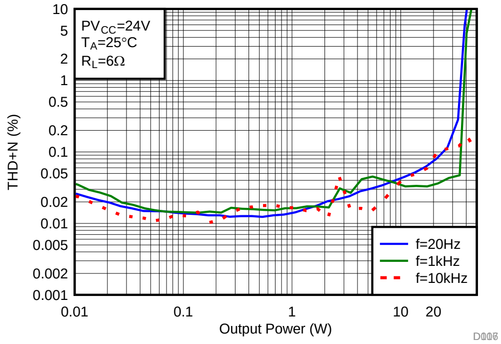
Figure 16. THD+N vs Output Power-BTL



PVDD = 18V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

Figure 17. THD+N vs Output Power-BTL

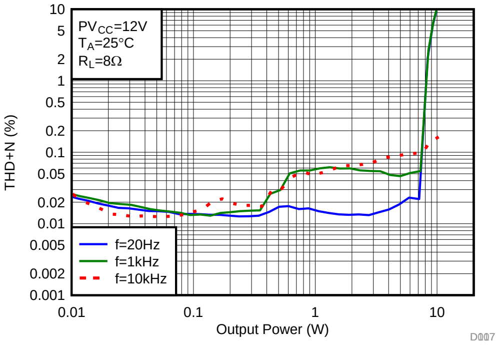


PVDD = 24V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

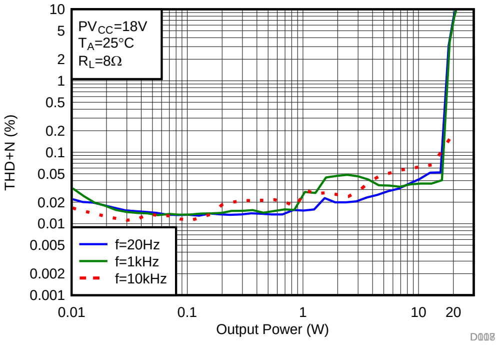
Figure 18. THD+N vs Output Power-BTL

Typical Characteristics (continued)



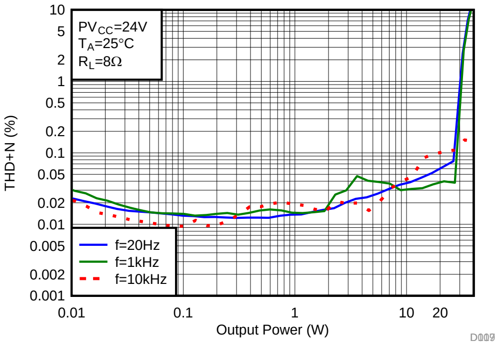
PVDD = 12V
4.7uH+0.68uF
F_{SW} = 768 kHz
1SPW Modulation
Load = 8Ω

Figure 19. THD+N vs Output Power-BTL



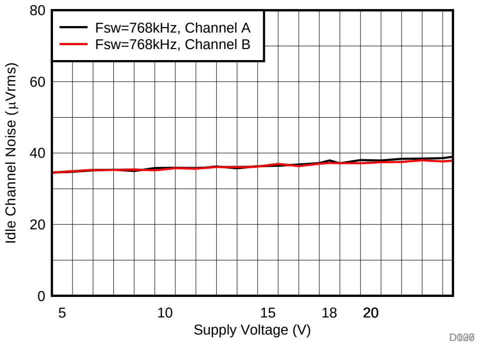
PVDD = 18V
10uH+0.68uF
F_{SW} = 768 kHz
1SPW Modulation
Load = 8Ω

Figure 20. THD+N vs Output Power-BTL



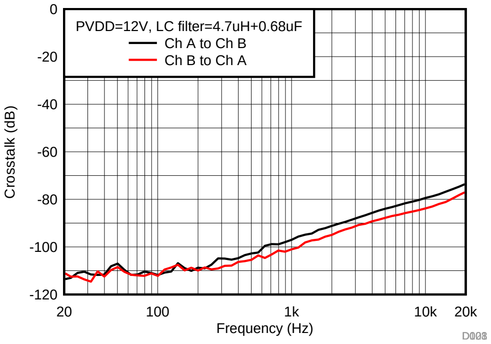
PVDD = 24V
10uH+0.68uF
F_{SW} = 768 kHz
1SPW Modulation
Load = 8Ω

Figure 21. THD+N vs Output Power-BTL



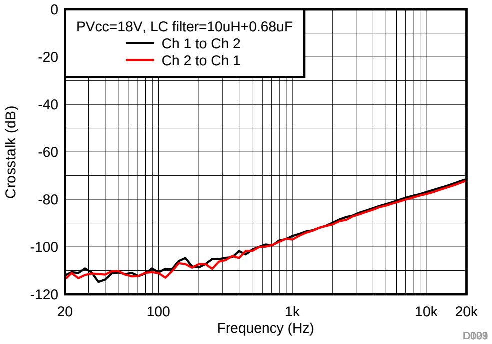
PVDD = 4.5V~24V
10uH+0.68uF
F_{SW} = 768 kHz
1SPW Modulation
Load = 8Ω

Figure 22. Idle Channel Noise vs PVDD-BTL



PVDD = 12V
4.7uH+0.68uF
Pout=1W
F_{SW} = 768 kHz
1SPW Modulation
Load = 6Ω

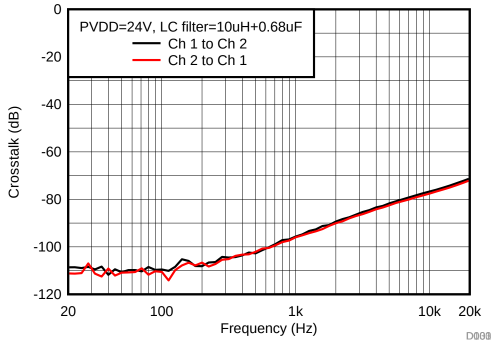
Figure 23. Crosstalk



PVDD = 18V
10uH+0.68uF
Pout=1W
F_{SW} = 768 kHz
1SPW Modulation
Load = 6Ω

Figure 24. Crosstalk

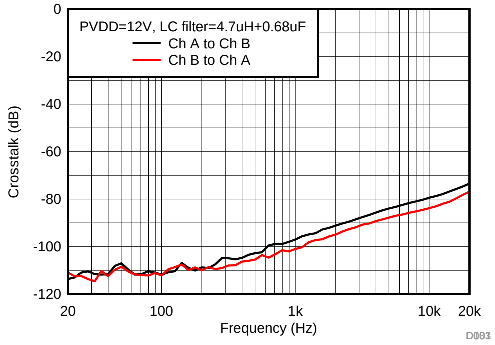
Typical Characteristics (continued)



PVDD = 24V 10uH+0.68uF Pout=1W

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

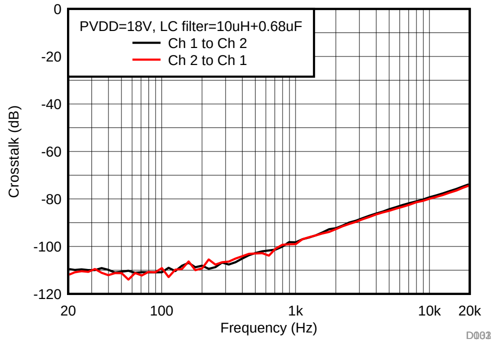
Figure 25. Crosstalk



PVDD = 12V 4.7uH+0.68uF Pout=1W

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

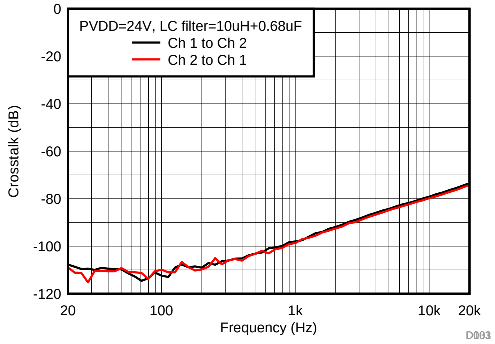
Figure 26. Crosstalk



PVDD = 18V 10uH+0.68uF Pout=1W

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

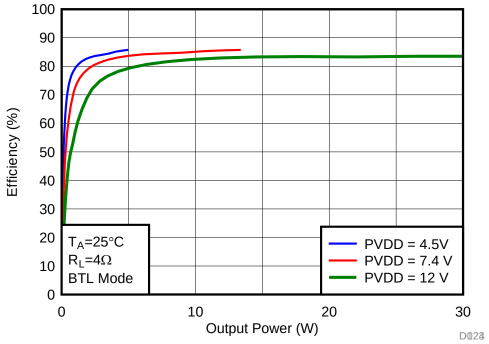
Figure 27. Crosstalk



PVDD = 24V 10uH+0.68uF Pout=1W

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

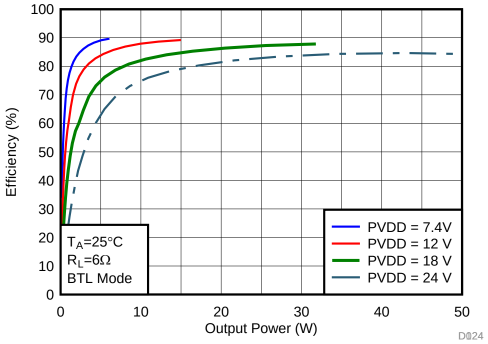
Figure 28. Crosstalk



PVDD = 4.5V/7.4V/12V 4.7uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 4Ω

Figure 29. Efficiency vs Output Power-BTL

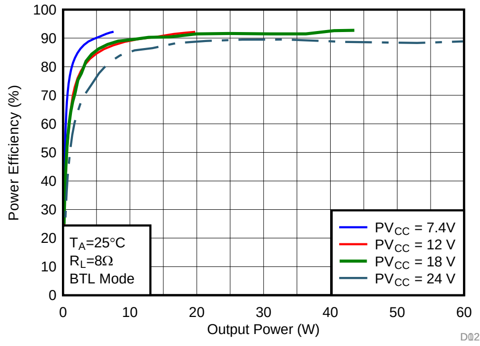


PVDD = 7.4V/12V/18V/24V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 6Ω

Figure 30. Efficiency vs Output Power-BTL

Typical Characteristics (continued)



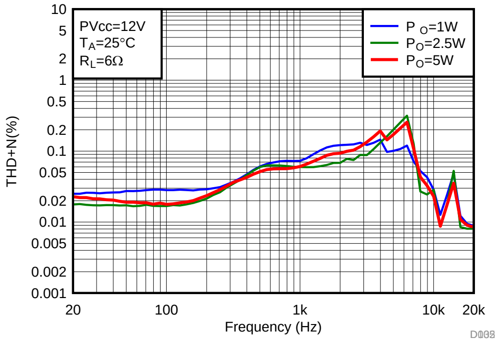
PVDD = 7.4V/12V/18V/24V 10uH+0.68uF

F_{SW} = 768 kHz 1SPW Modulation Load = 8Ω

Figure 31. Efficiency vs Output Power-BTL

7.7.2 Bridge Tied Load (BTL) Configuration Curves

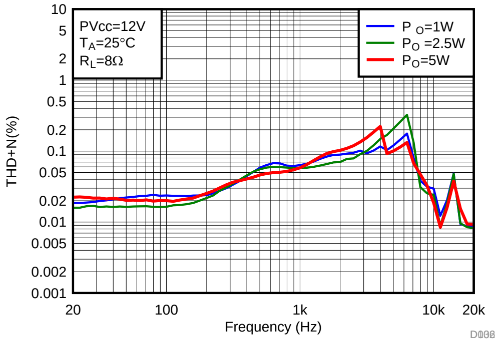
Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS805MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, Spread Spectrum Enable, Ferrite bead + Capacitor as the output filter, BD Modulation, unless otherwise noted.



PVDD = 12V Ferrite Bead + Capacitor Spread Spectrum Enable

F_{SW} = 384 kHz BD Modulation Load = 6Ω

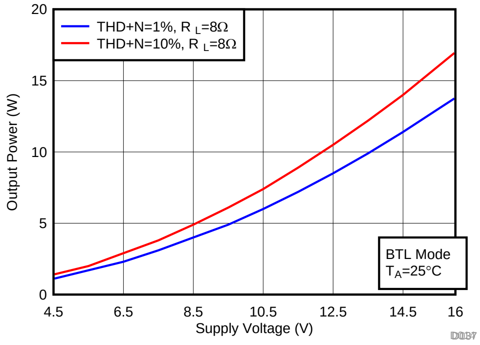
Figure 32. THD+N vs Frequency-BTL



PVDD = 12V Ferrite Bead + Capacitor Spread Spectrum Enable

F_{SW} = 384 kHz BD Modulation Load = 8Ω

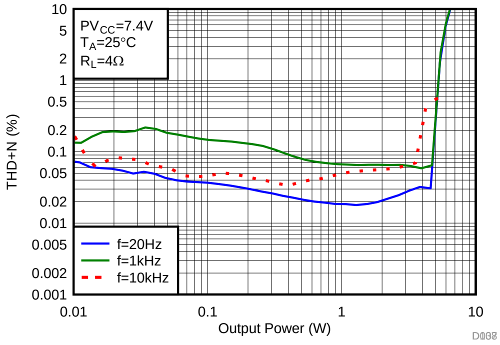
Figure 33. THD+N vs Frequency-BTL



PVDD = 4.5V~16V Ferrite Bead + Capacitor Spread Spectrum Enable

F_{SW} = 384 kHz BD Modulation Load = 8Ω

Figure 34. Output Power vs Supply Voltage-BTL

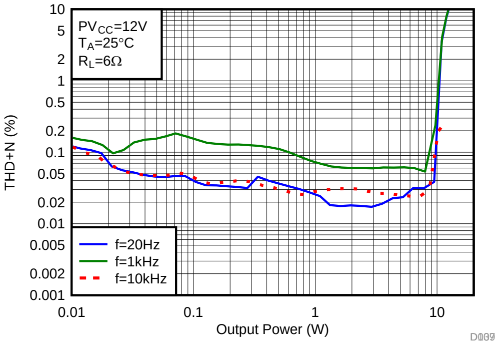


PVDD = 7.4V Ferrite Bead + Capacitor Spread Spectrum Enable

F_{SW} = 384 kHz BD Modulation Load = 4Ω

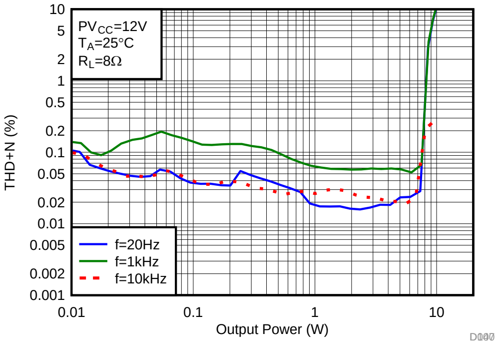
Figure 35. THD+N vs Output Power-BTL

Typical Characteristics (continued)



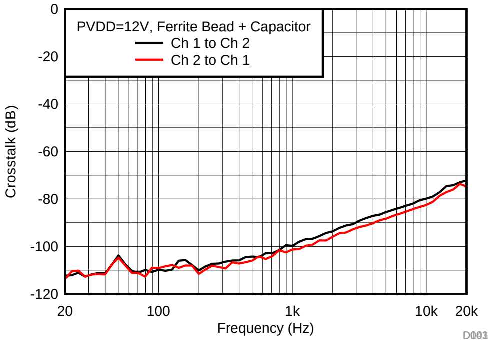
PVDD = 12V	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 6Ω

Figure 36. THD+N vs Output Power-BTL



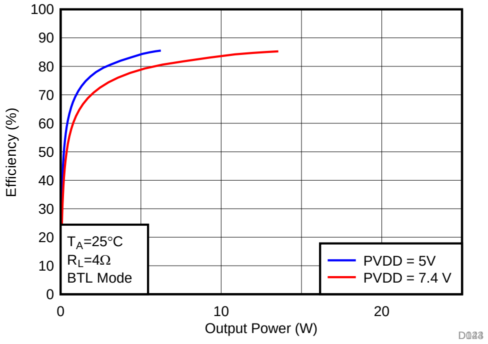
PVDD = 12V	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 8Ω

Figure 37. THD+N vs Output Power-BTL



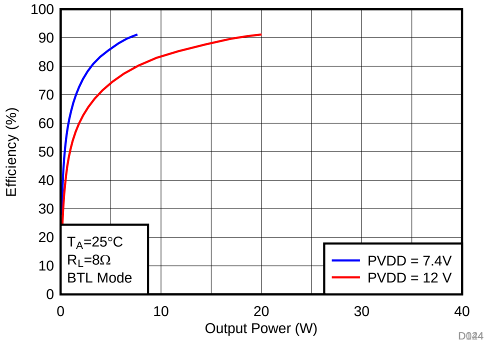
PVDD = 12V, Pout=1W	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 6Ω

Figure 38. Crosstalk



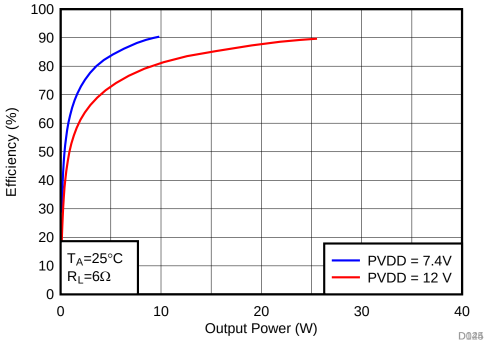
PVDD = 5V/7.4V	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 4Ω

Figure 39. Efficiency vs Output Power-BTL



PVDD = 7.4V/12V	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 8Ω

Figure 40. Efficiency vs Output Power-BTL



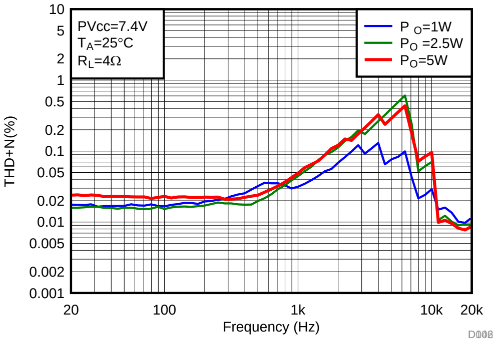
PVDD = 7.4V/12V	Ferrite Bead + Capacitor	Spread Spectrum Enable
F_{SW} = 384 kHz	BD Modulation	Load = 6Ω

Figure 41. Efficiency vs Output Power-BTL

7.7.3 Parallel Bridge Tied Load (PBTL) Configuration

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5805MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576 kHz, the LC filter used was 4.7 μH / 0.68 μF, unless otherwise noted.

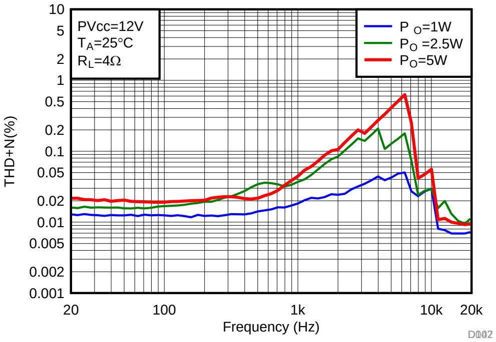
Typical Characteristics (continued)



PVDD = 7.4V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4Ω

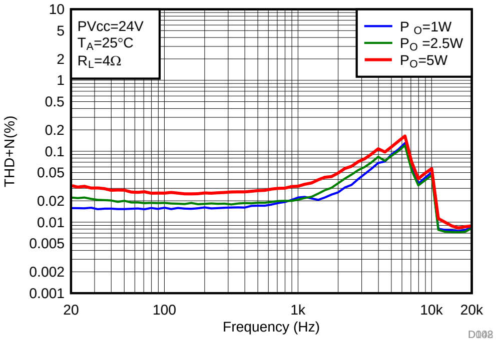
Figure 42. THD+N vs Frequency-PBTL



PVDD = 12V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4Ω

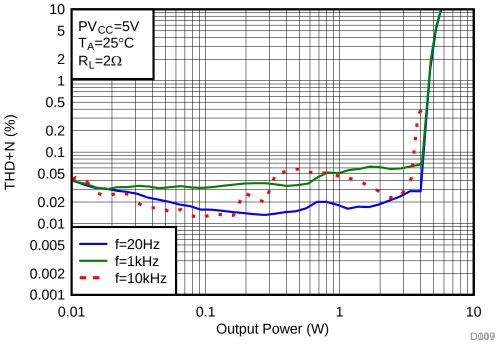
Figure 43. THD+N vs Frequency-PBTL



PVDD = 24V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4Ω

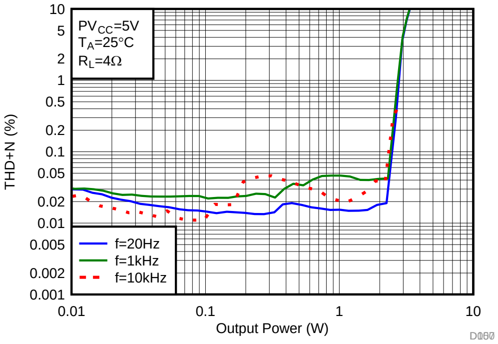
Figure 44. THD+N vs Frequency-PBTL



PVDD = 5V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 2Ω

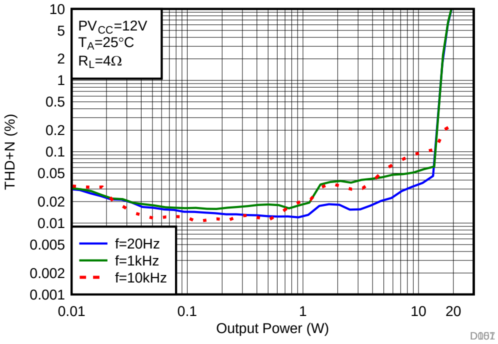
Figure 45. THD+N vs Output Power-PBTL



PVDD = 5V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4Ω

Figure 46. THD+N vs Output Power-PBTL

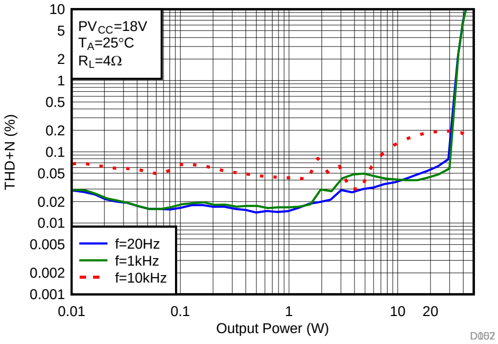


PVDD = 12V   4.7uH + 0.68uF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4Ω

Figure 47. THD+N vs Output Power-PBTL

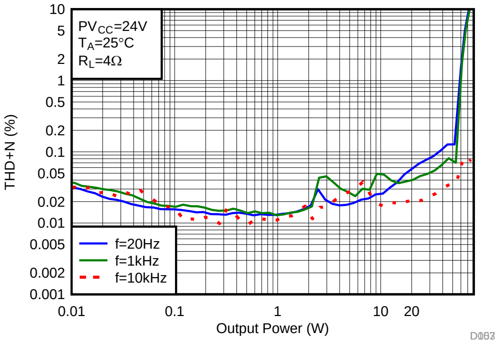
Typical Characteristics (continued)



PVDD = 18V 4.7uH + 0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

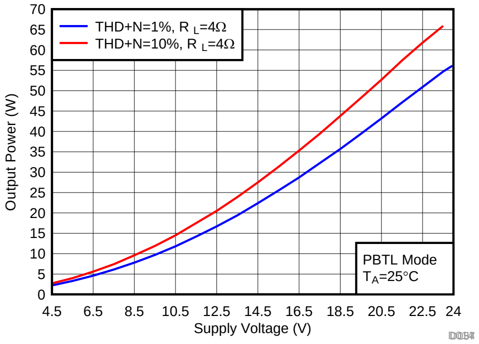
Figure 48. THD+N vs Output Power-PBTL



PVDD = 24V 4.7uH + 0.68uF

F_{SW} = 576kHz 1SPW Modulation Load = 4Ω

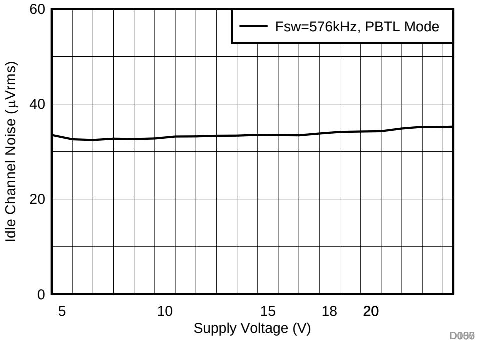
Figure 49. THD+N vs Output Power-PBTL



PVDD = 4.5V~24V 4.7uH + 0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

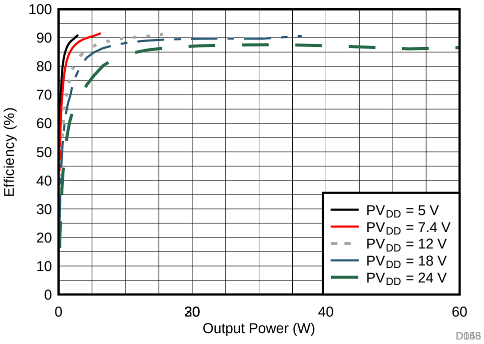
Figure 50. Output Power vs Supply Voltage-PBTL



PVDD = 4.5V~24V 4.7uH + 0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

Figure 51. Idle Channel Noise vs Supply Voltage-PBTL



PVDD = 5V/7.4V/12V/18V/24V 4.7uH + 0.68uF

F_{SW} = 576 kHz 1SPW Modulation Load = 4Ω

Figure 52. Efficiency vs Output Power

8 Parameter Measurement Information

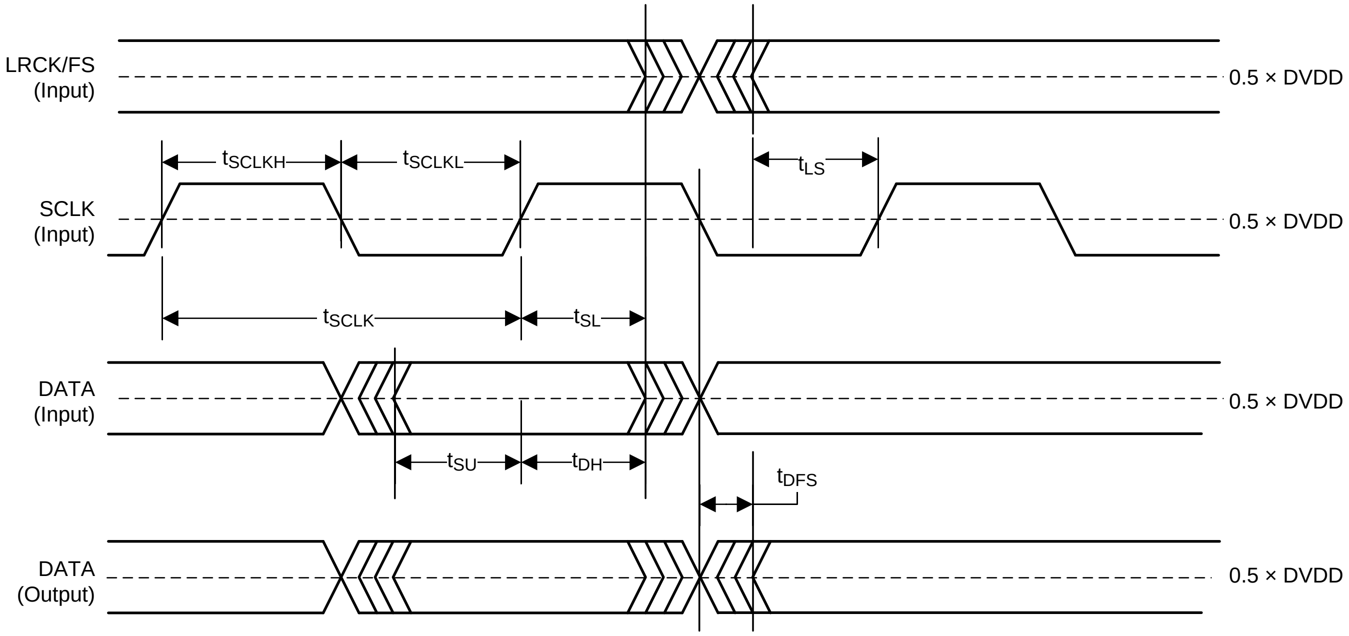


Figure 53. Serial Audio Port Timing in Slave Mode

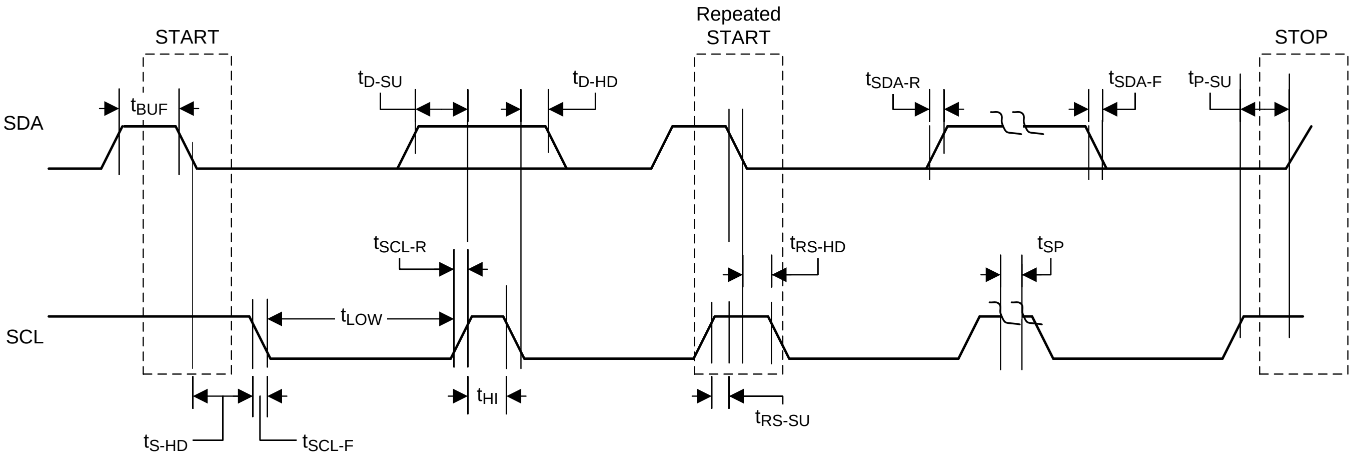


Figure 54. I^{2}C Communication Port Timing Diagram

9 Detailed Description

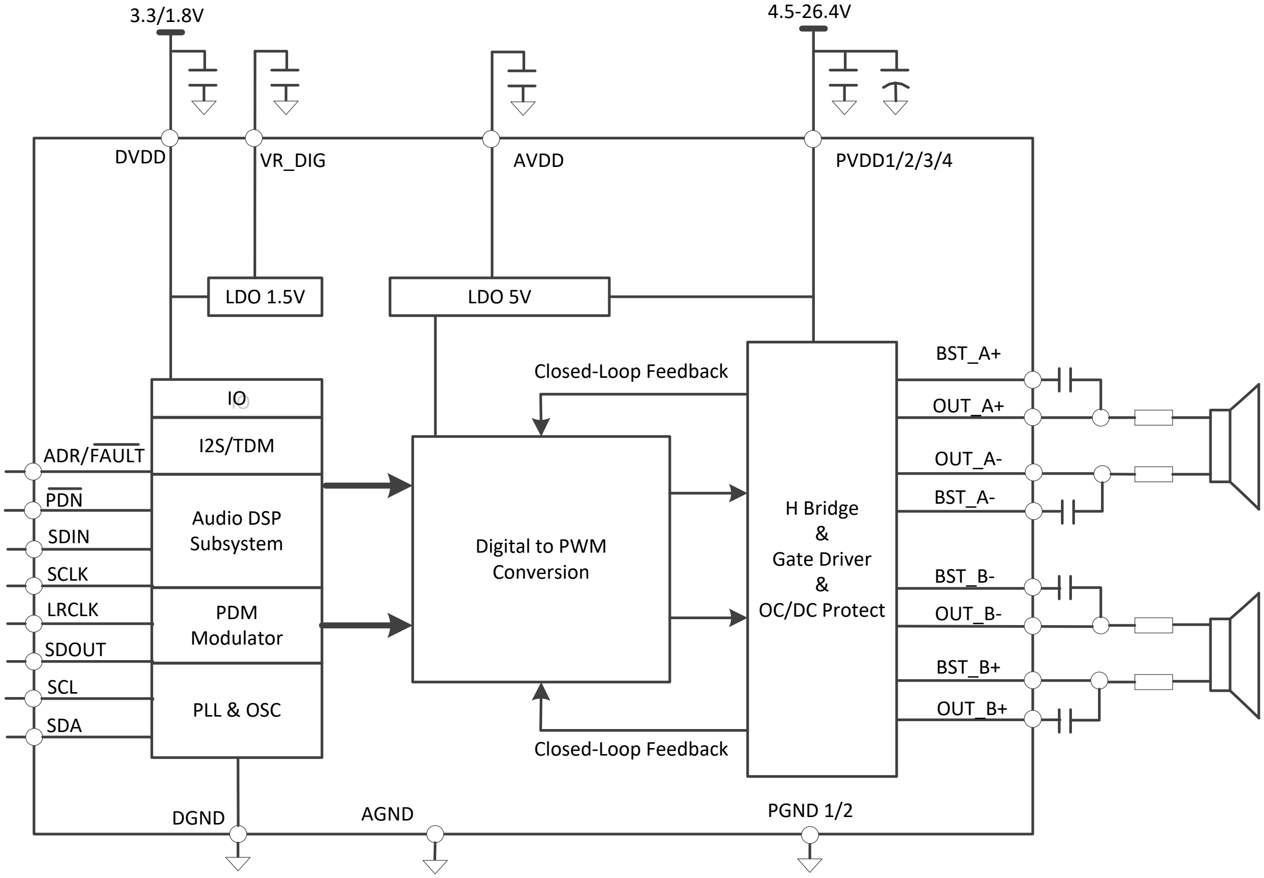
9.1 Overview

The TAS5805M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo audio DAC.
- An Audio DSP subsystem.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at different switching frequencies, and supporting a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs convert PVDD to 5 V for GVDD and AVDD and to 1.5V for DVDD respectively.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power Supplies

To facilitate system design, TAS5805M needs only a 3.3-V or 1.8-V supply in addition to the (typical) 12-V or 24-V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (AVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (AVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

9.3.2 Device Clocking

The TAS5805M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

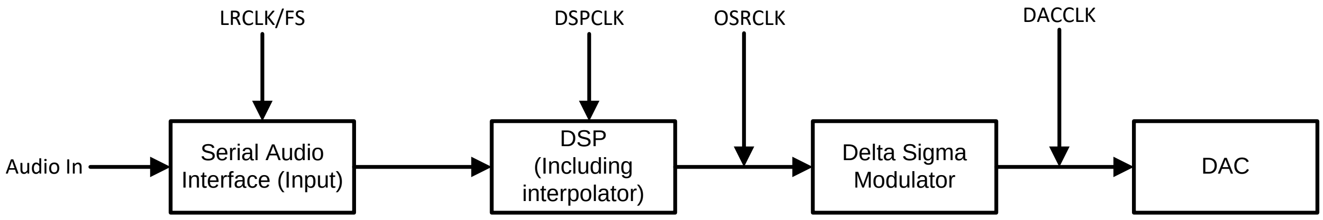


Figure 55. Audio Flow with Respective Clocks

Figure 55 shows the basic data flow and clock distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The TAS5805M device has an audio sampling rate detection circuit that automatically senses the sampling frequency. Common audio sampling frequencies of 32 kHz, 44.1kHz – 48 kHz, 88.2 kHz – 96 kHz with ±5% tolerance are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

9.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS, SCLK, and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5805M device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Feature Description (continued)

Table 1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	Up to 96	64, 32
TDM	32, 24, 20, 16	Up to 48	128,256,512
		96	128,256

When any kind of clock errors including Out of Range, SCLK-FSYNC Ratio, or Clock halt are detected, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). When all audio clocks are within the expected ranges, the device automatically returns to the state it was in.

9.3.4 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (P0-R51-D[5:4]). If the high width of LRCK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (P0-R51-D[3:2]) should be set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 56 through Figure 60. The word length are selected via Register (P0-R51-D[1:0]). The offsets of data are selected via Register (P0-R51-D[7]) and Register (P0-R52-D[7:0]). Default setting is I2S and 24 bit word length.

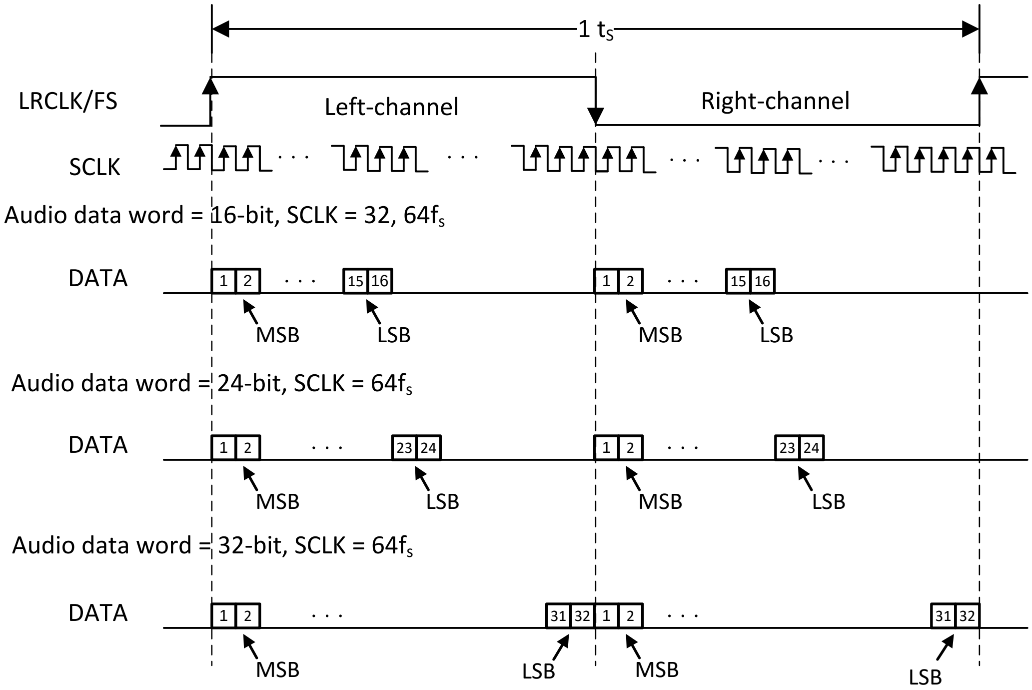
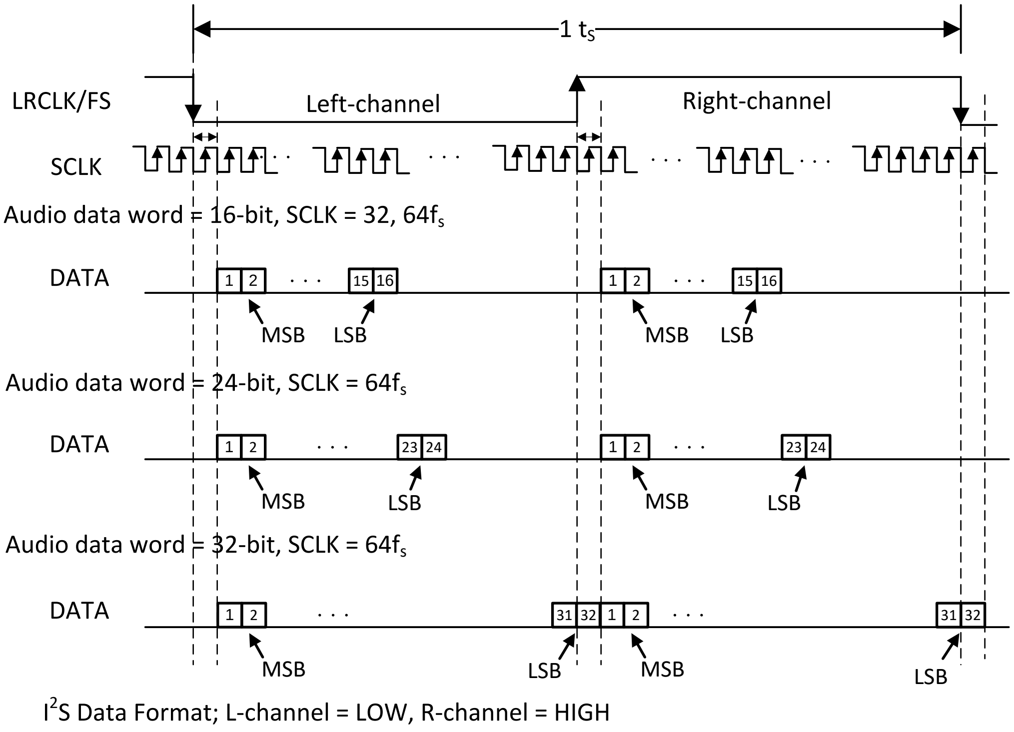
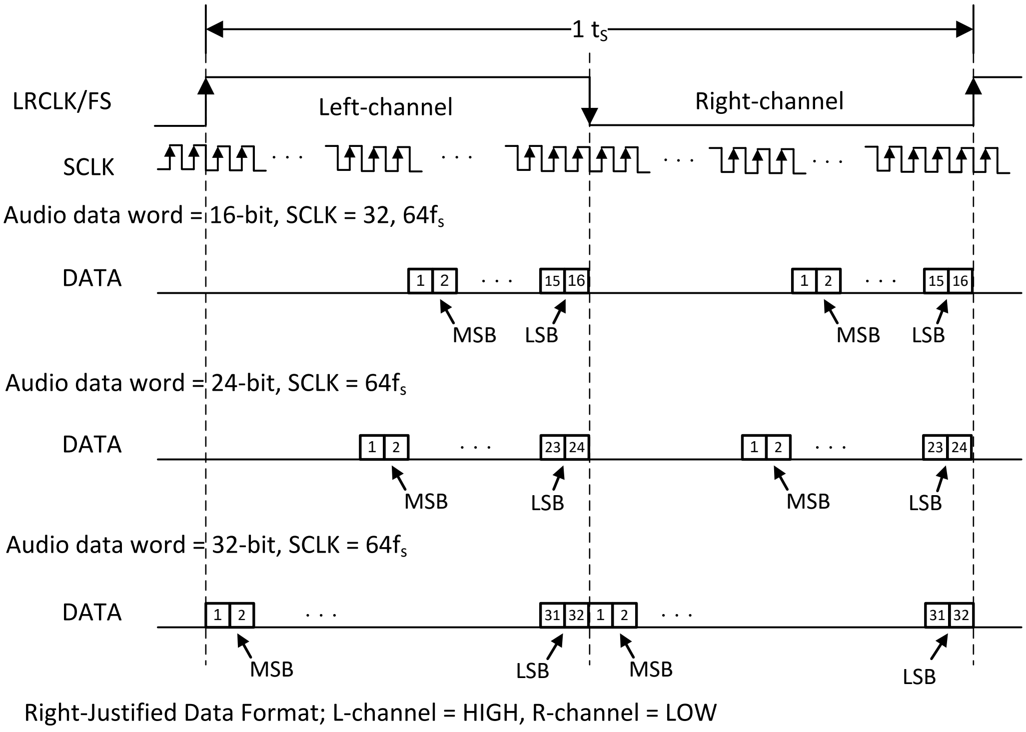


Figure 56. Left-Justified Audio Data Format



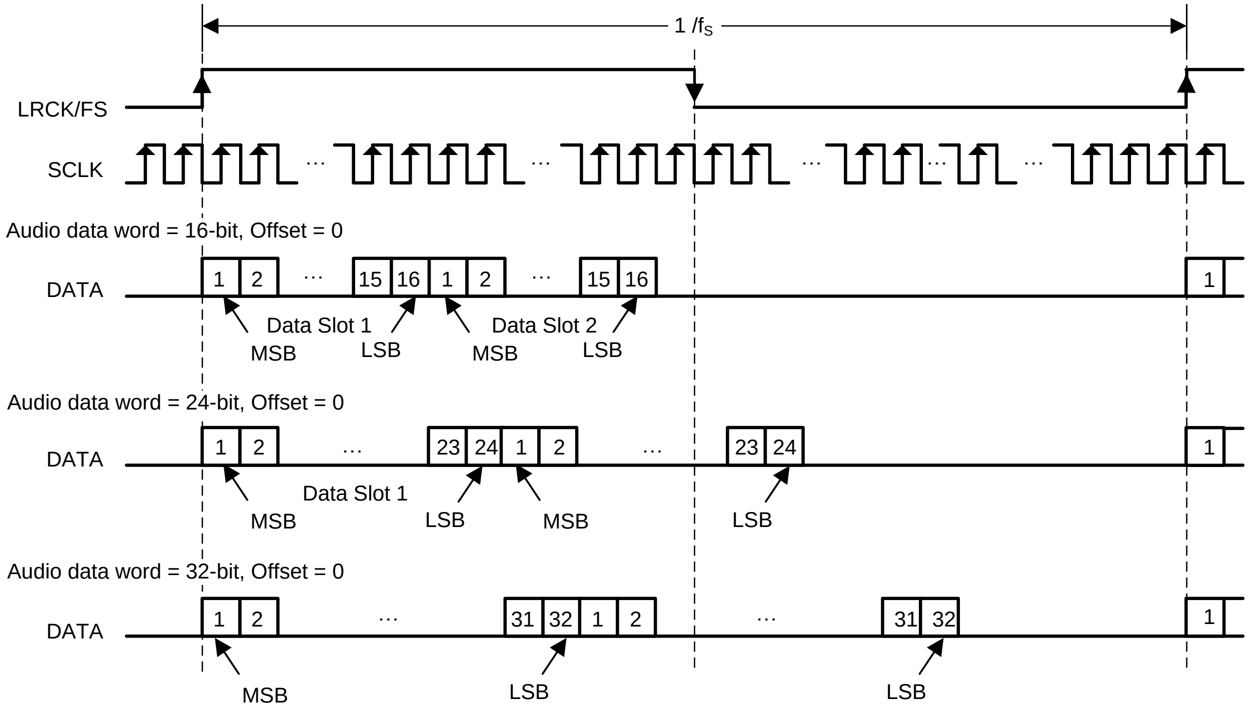
I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 57. I²S Audio Data Format



Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

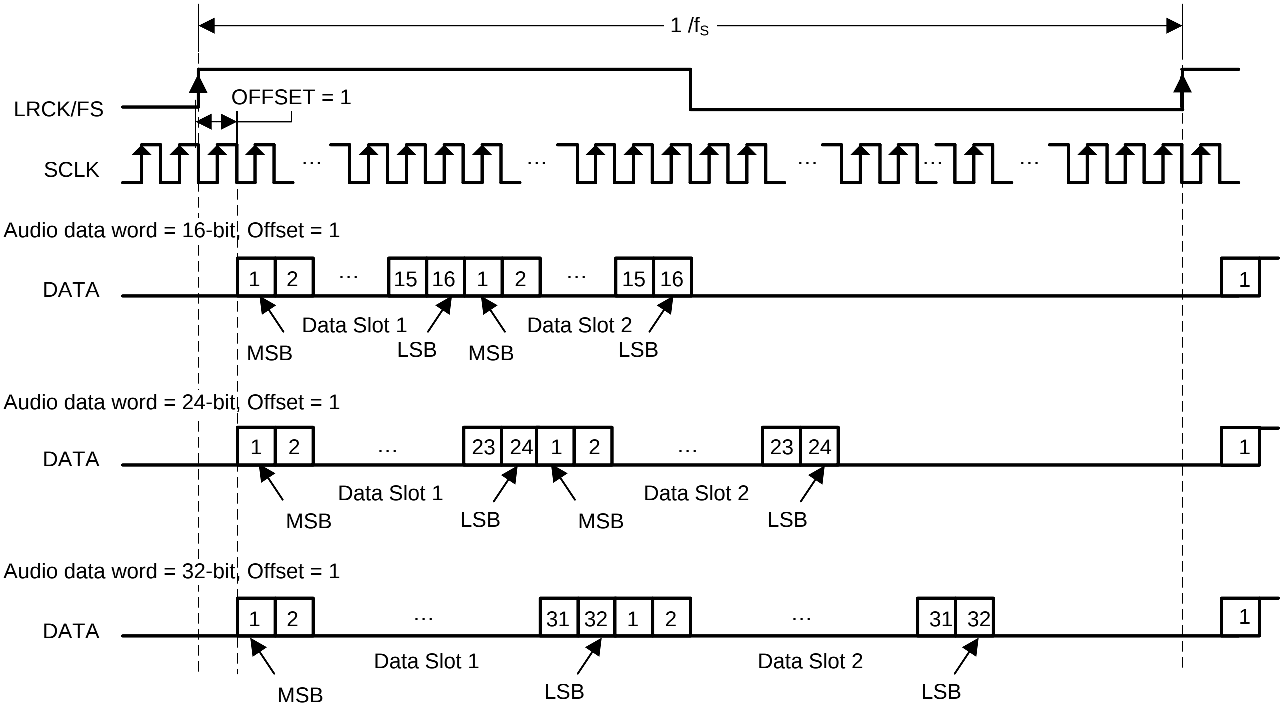
Figure 58. Right-Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 59. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 60. TDM 2 Audio Data Format

9.3.5 Digital Audio Processing

TAS5805M DSP has advanced process flows for different applications, refer to application note, *TAS5805 Process Flows* for details or request the PPC3 access for TAS5805M app .

9.3.6 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse-width- modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reducing distortion and improving immunity to the power supply noise. The analog gain is also applied in the Class-D amplifier section of the device.

9.3.6.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in Figure 61, the audio path of the TAS5805M consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class-D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain consists of digital gain shown in the digital audio path, and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

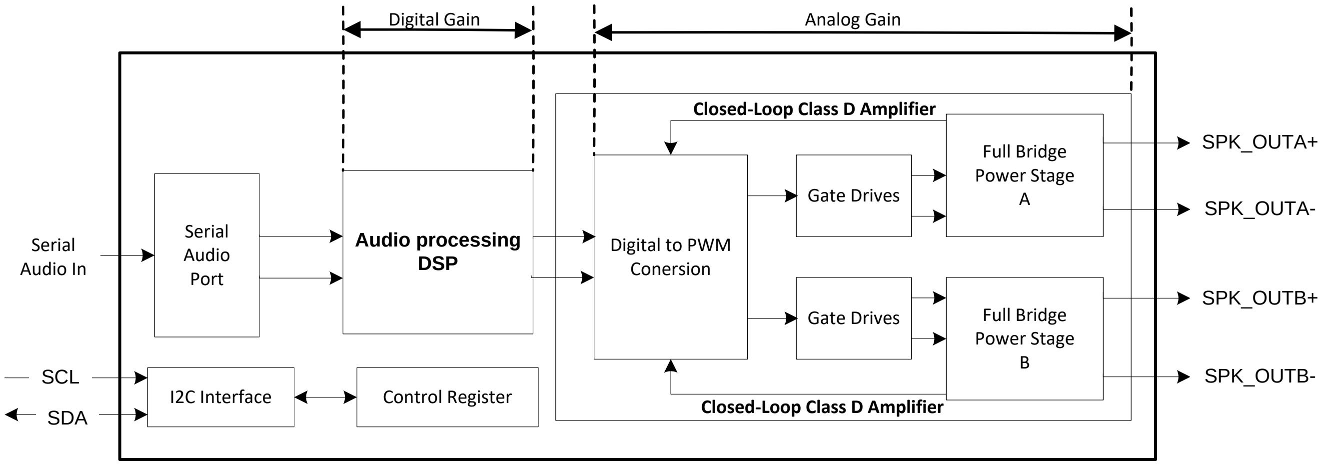


Figure 61. Speaker Amplifier Gain

As shown in Figure 61, the first gain stage of the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default. For all settings of the register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings ensure that the output signal is not clipped at different PVDD levels. 0dBFS output corresponds to 29.5-V peak output voltage.

Table 2. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER PEAK OUTPUT VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
…….	……..	…….
11111	-15.5	4.95

9.4 Device Functional Modes

9.4.1 Software Control

The TAS5805M device is configured via an I^2 C communication port.

Device Functional Modes (continued)

The I2C Communication Protocol is detailed in the I^{2}C Communication Port section. The I^{2}C timing requirements are described in the I^{2}C Bus Timing – Standard and I^{2}C Bus Timing – Fast sections.

9.4.2 Speaker Amplifier Operating Modes

The TAS5805M device can be used in two different amplifier configurations:

- BTL Mode
- PBTL Mode

9.4.2.1 BTL Mode

In BTL mode, the TAS5805M amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

9.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5805M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows for smaller, less-expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5805M device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

9.4.3 Low EMI Modes

TAS5805M employs several modes to minimize EMI during playing audio, and they can be used based on different applications.

9.4.3.1 Spread Spectrum

Spread spectrum is used in some inductor free case to minimize EMI noise. The TAS5805M supports Spread Spectrum with triangle mode.

User needs to configure register SS_CTRL0 (0x6B) to enable Spread Spectrum with triangle mode, and select spread spectrum frequency and range with SS_CTRL1 (0x6C). For 384kHz F_{SW} which configured by DEVICE_CTRL1 (0x02), the Spread Spectrum frequency and range are described inTable 3

Table 3. Triangle Mode Spread Spectrum Frequency and Range Selection

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example-Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz:

w 98 6b 03 //Enable Spread Spectrum

w 98 6c 03 //SS_TRI_CTRL[3:0]0011, Triangle Frequency = 24kHz, Spread Spectrum Range should be 25% (336kHz~432kHz)

9.4.3.2 Channel to Channel Phase Shift

This device supports channel to channel 180-degree PWM phase shift to minimize the EMI.

9.4.3.3 Multi-Devices PWM Phase Synchronization

This device supports up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 pieces of TAS5805M devices, user can select phase 0/1/2/3 for each device with register PHASE_CTRL (0x6A), which means there is a 45-degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I2S clock during the Startup Phase:

1. Halt I2S clock.
2. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x03 for device 0; Register 0x6A = 0x07 for device 1; Register 0x6A = 0x0B for device 2; Register 0x6A = 0x0F for device 3. There should be a 45-degree PWM phase shift between each device to minimize the EMI.
3. Configure each device into Hi-Z mode.
4. Provide I2S to each device. Phase synchronization for all 4 devices will be automatically done by internal sequence.
5. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
6. Device to Device PWM phase shift should be fixed with 45 degree.

9.4.4 Device State Control

Except Shutdown Mode, TAS5805M has other 4 states with different power dissipation which listed in the Electrical Characteristics Table.

- Deep Sleep Mode. Register 0x03h -D[1:0]=00, device stays in Deep Sleep Mode. In this mode, I2C block is still working. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, TAS5805M can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Device returns back to Play Mode by setting Register 0x03h -D[1:0] to 11. Unlike the Shutdown Mode (Pulling PDN Low), entering or exiting Deep Sleep Mode, the DSP is kept active.
- Sleep Mode. Register 0x03h -D[1:0]=01, device stays in Sleep Mode. In this mode, I2 C block, Digital core, DSP Memory , 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull PDN Low), enter or exit Sleep Mode, DSP is kept active.
- Output Hiz Mode. Register 0x03h -D[1:0]=10, device stays in Hiz Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally.
- Play Mode. Register 0x03h -D[1:0]=11, device stays in Play Mode.

9.4.5 Device Modulation

TAS5805M has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for TAS5805M with Register 0x02 [1:0]-DAMP_MOD.

9.4.5.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I2R losses in the load.

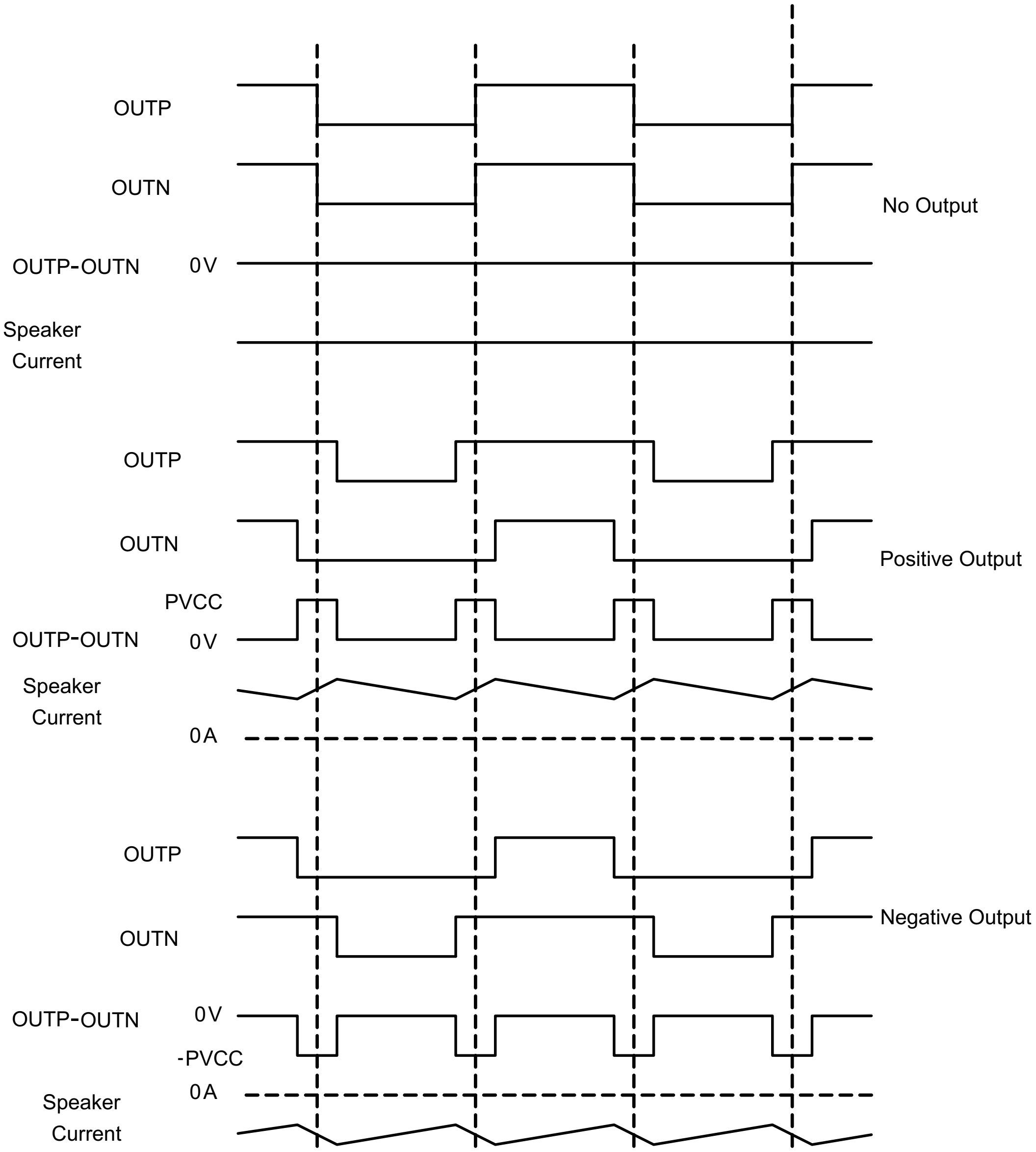


Figure 62. BD Mode Modulation

9.4.5.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~17% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

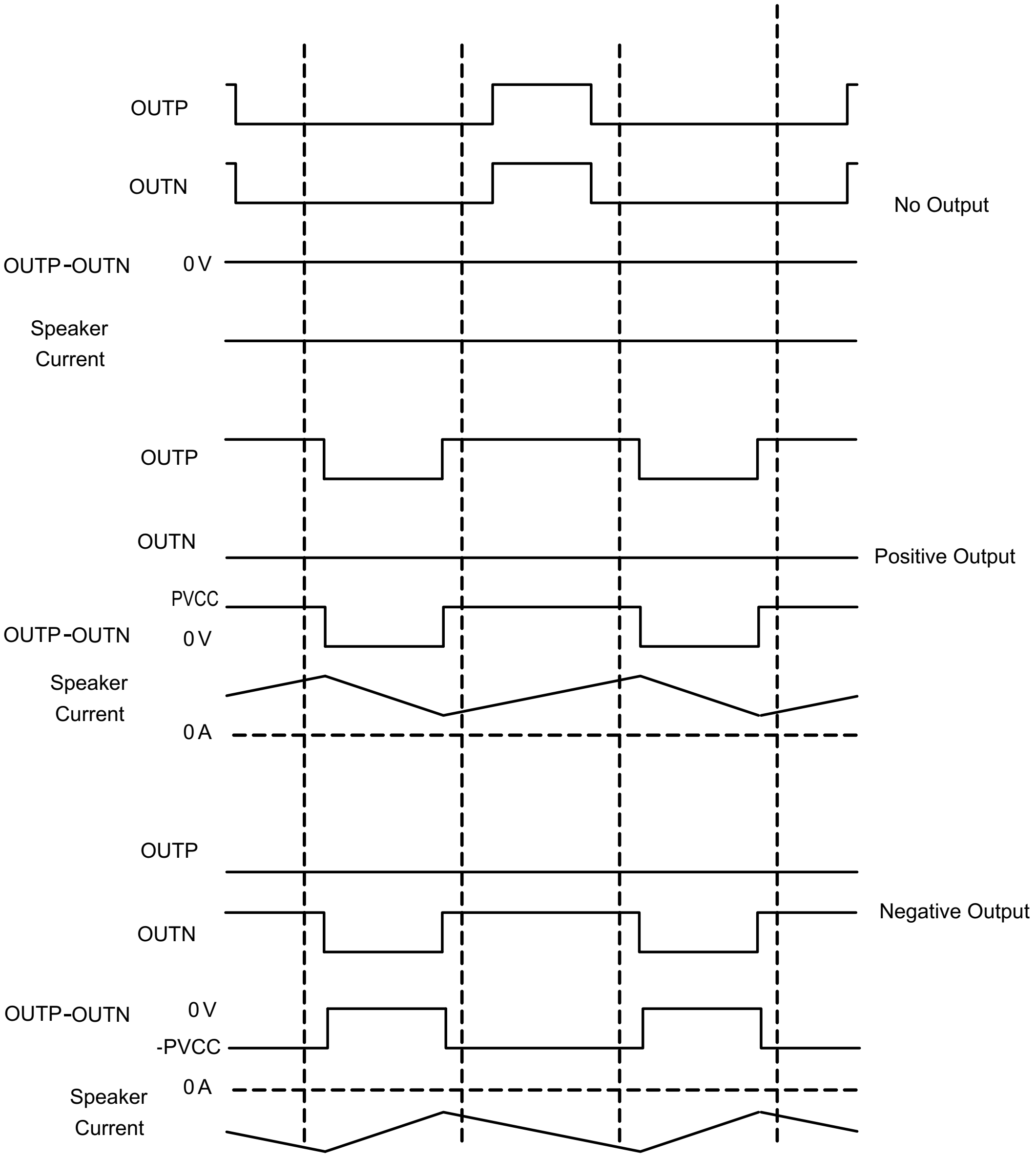


Figure 63. 1SPW Mode Modulation

9.4.5.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5805M will detect the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the Hybrid Modulation. In order to minimize the power dissipation, low switching frequency (For example, Fsw=384kHz) with proper LC filter (15uH+0.68uF or 22uH+0.68uF) is recommended.

NOTE

To use the Hybrid Modulation, users need to enter the system's PVDD value on the TAS5805M PPC3 App.

9.5 Programming and Control

9.5.1 I^2 C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I^2)C bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a slave device. Because the TAS5805M register map and DSP memory spans multi pages, the user should change from page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255.

9.5.2 Slave Address

The TAS5805M device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 01011(0x5x). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in Table 4.

Table 4. I^2 C Slave Address Configuration

ADR PIN Configuration	MSBs					User Define		LSB
4.7k Ω to DVDD	0	1	0	1	1	0	0	R/$\overline{W}$
15kΩ to DVDD	0	1	0	1	1	0	1	R/$\overline{W}$
47kΩ to DVDD	0	1	0	1	1	1	0	R/$\overline{W}$
120kΩ to DVDD	0	1	0	1	1	1	1	R/$\overline{W}$

9.5.2.1 Random Write

As shown in Figure 64, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^{2}C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

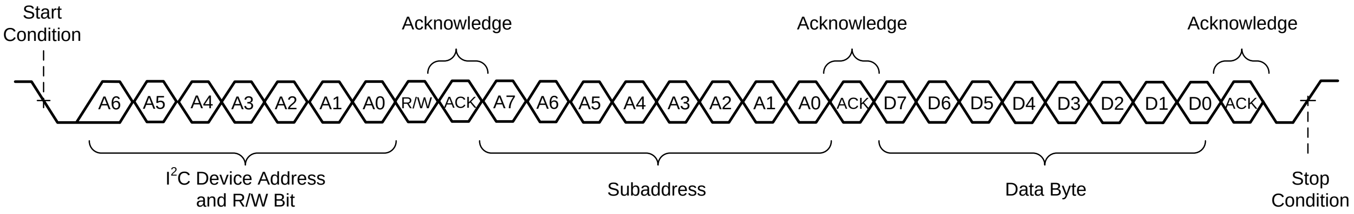


Figure 64. Random Write Transfer

9.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in Figure 65. After receiving each data byte, the device responds with an acknowledge bit and the I^2 subaddress is automatically incremented by one.

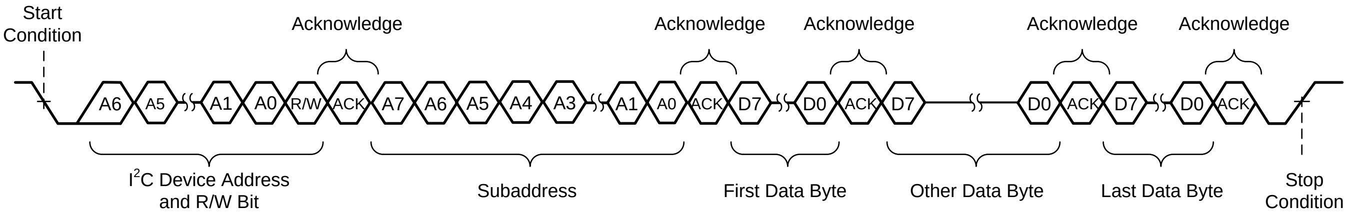


Figure 65. Sequential Write Transfer

9.5.2.3 Random Read

As shown in Figure 66, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

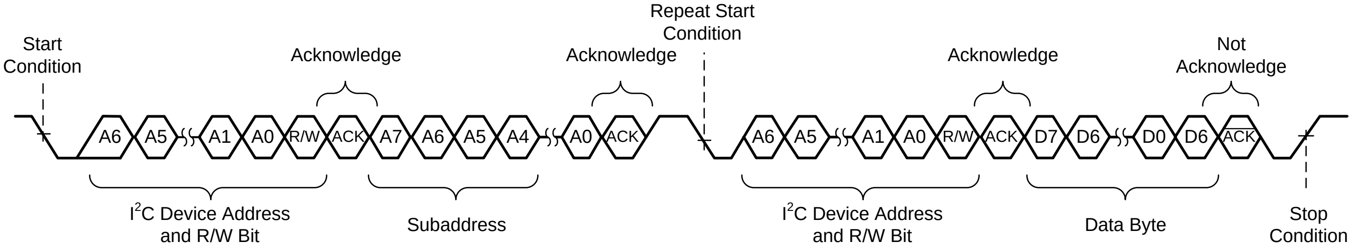


Figure 66. Random Read Transfer

9.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in Figure 67. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^{2}C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

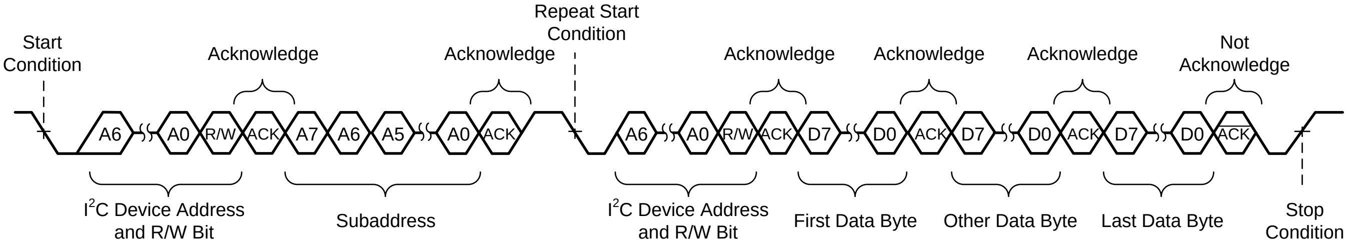


Figure 67. Sequential Read Transfer

9.5.2.5 DSP Memory Book, Page and BQ update

On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest address. The address of all Biquad Filters can be found in Register Maps

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5805M Process Flows

9.5.2.6 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

9.5.2.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I^{2}C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

9.5.2.6.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

9.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

9.5.3.1 Startup Procedures

1. Configure ADR/$\overline{\text{FAULT}}$ pin with proper setting for I^{2}C device address.
2. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first).
3. Once power supplies are stable, start SCLK, LRCLK.
4. Once I^{2}S clock are stable, configure the device via the I2C control port based on the user cases (Make sure the $\overline{\text{PDN}}$ pin = HIGH before I2C control port operating).
5. The device is now in normal operation.

It is important to note that I^{2}C control port register changes should only occur when the device is placed into SLEEP. This can be accomplished by configuring Register 0x3h-D[1:0] in the control register.

9.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h -D[1:0]=00 (DEEP SLEEP) via the I2C control port or Pull PDN low.
3. Pull $\overline{\text{PDN}}$ low.
4. The clocks can now be stopped and the power supplies brought down.
5. The device is now fully shutdown and powered off.

9.5.3.3 Protection and Monitoring

9.5.3.3.1 Overcurrent Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I^{2}C. An OCSD event activates the fault pin, and the I^2 fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OSCD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

9.5.3.3.2 DC Detect

If the TAS5805M device measures a DC offset in the output voltage, the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault.

9.6 Register Maps

9.6.1 CONTROL PORT Registers

Table 5 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Go
2h	DEVICE_CTRL_1	Register 2	Go
3h	DEVICE_CTRL_2	Register 3	Go
Fh	I2C_PAGE_AUTO_INC	Register 15	Go
28h	SIG_CH_CTRL	Register 40	Go
29h	CLOCK_DET_CTRL	Register 41	Go
30h	SDOUT_SEL	Register 48	Go
31h	I2S_CTRL	Register 49	Go
33h	SAP_CTRL1	Register 51	Go
34h	SAP_CTRL2	Register 52	Go
35h	SAP_CTRL3	Register 53	Go
37h	FS_MON	Register 55	Go
38h	BCK_MON	Register 56	Go
39h	CLKDET_STATUS	Register 57	Go
4Ch	DIG_VOL_CTRL	Register 76	Go
4Eh	DIG_VOL_CTRL2	Register 78	Go
4Fh	DIG_VOL_CTRL3	Register 79	Go
50h	AUTO_MUTE_CTRL	Register 80	Go
51h	AUTO_MUTE_TIME	Register 81	Go
53h	ANA_CTRL	Register 83	Go
54h	AGAIN	Register 84	Go
5Ch	BQ_WR_CTRL1	Register 92	Go
5Dh	DAC_CTRL	Register 93	Go
60h	ADR_PIN_CTRL	Register 96	Go
61h	ADR_PIN_CONFIG	Register 97	Go
66h	DSP_MISC	Register 102	Go
67h	DIE_ID	Register 103	Go
68h	POWER_STATE	Register 104	Go
69h	AUTOMUTE_STATE	Register 105	Go
6Ah	PHASE_CTRL	Register 106	Go
6Bh	SS_CTRL0	Register 107	Go
6Ch	SS_CTRL1	Register 108	Go
6Dh	SS_CTRL2	Register 109	Go
6Eh	SS_CTRL3	Register 110	Go
6Fh	SS_CTRL4	Register 111	Go
70h	CHAN_FAULT	Register 112	Go
71h	GLOBAL_FAULT1	Register 113	Go
72h	GLOBAL_FAULT2	Register 114	Go
73h	OT WARNING	Register 115	Go
74h	PIN_CONTROL1	Register 116	Go
75h	PIN_CONTROL2	Register 117	Go
76h	MISC_CONTROL	Register 118	Go

Table 5. CONTROL PORT Registers (continued)

Offset	Acronym	Register Name	Section
78h	FAULT_CLEAR	Register 120	Go

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

9.6.1.1 RESET_CTRL Register (Offset = 1h) [reset = 0x00]

RESET_CTRL is shown in Figure 68 and described in Table 7.

Return to Summary Table.

Figure 68. RESET_CTRL Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>RST_MOD</td><td colspan="3">RESERVED</td><td>RST_REG</td></tr>
<tr><td colspan="3">R/W</td><td>W</td><td colspan="3">R</td><td>W</td></tr>
</table>

Table 7. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_MOD	W	0	WRITE CLEAR BIT Reset Modules WRITE CLEAR BIT Reset full digital core This bit resets full digital signal chain (Include DSP and Control Port Registers). Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. 0: Normal 1: Reset modules
3-1	RESERVED	R	000	This bit is reserved
0	RST_CONTROL_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the control port registers back to their initial values. The RAM content is not cleared. 0: Normal 1: Reset control port registers

9.6.1.2 DEVICE_CTRL_1 Register (Offset = 2h) [reset = 0x00]

DEVICE_CTRL_1 is shown in Figure 69 and described in Table 8.

Return to Summary Table.

Figure 69. DEVICE_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTL	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

Table 8. DEVICE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW 000:768K 001:384K 010:310K 011:480K 100:576K 101:Reserved 110:Reserved 111:Reserved
3	RESERVED	R/W	0	This bit is reserved
2	DAMP_PBTL	R/W	0	0: SET DAMP TO BTL MODE 1:SET DAMP TO PBTL MODE
1-0	DAMP_MOD	R/W	00	00:BD MODE 01:1SPW MODE 10:HYBRID MODE

9.6.1.3 DEVICE_CTRL_2 Register (Offset = 3h) [reset = 0x10]

DEVICE_CTRL_2 is shown in Figure 70 and described in Table 9.

Return to Summary Table.

Figure 70. DEVICE_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

Table 9. DEVICE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute Both Left /Right Channel This bit issues soft mute request for the left/right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	device state control register 00: Deep Sleep 01: Sleep 10: Hiz, 11: PLAY

9.6.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [reset = 0x00]

I2C_PAGE_AUTO_INC is shown in Figure 71 and described in Table 10.

Return to Summary Table.

Figure 71. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

Table 10. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

9.6.1.5 SIG_CH_CTRL Register (Offset = 28h) [reset = 0x00]

SIG_CH_CTRL is shown in Figure 72 and described in Table 11.

Return to Summary Table.

Figure 72. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCK_RATIO_CONFIGURE				FS_MODE			
R/W				R/W			

Table 11. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured BCK ratio, the number of BCK clocks in one audio frame. 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS
3-0	FS_MODE	R/W	0000	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 4 'b0000 Auto detection 4 'b0010 8KHz 4 'b0100 16KHz 4 'b0110 32KHz 4 'b1000 44.1KHz 4'b1001 48KHz 4 'b1010 88.2KHz 4 'b1011 96KHz Others Reserved

9.6.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [reset = 0x00]

CLOCK_DET_CTRL is shown in Figure 73 and described in Table 12.

Return to Summary Table.

Figure 73. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_BCLK_RANGE	DIS_DET_FS	DIS_DET_BCLK	DIS_DET_MISS	RESERVED	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 12. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	DIS_DET_BCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256KHz and 50MHz or an error will be reported. When ignored, a BCK range error will not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error.But CLKDET_STATUS will report fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_BCLK	R/W	0	Ignore BCK Detection This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. 0: Regard BCK detection 1: Ignore BCK detection
2	DIS_DET_MISS	R/W	0	Ignore BCK Missing Detection This bit controls whether to ignore the BCK missing detection. When ignored an BCK missing will not cause a clock error. 0: Regard BCK missing detection 1: Ignore BCK missing detection
1	RESERVED	R/W	0	This bit is reserved
0	RESERVED	R/W	0	This bit is reserved

9.6.1.7 SDOUT_SEL Register (Offset = 30h) [reset = 0h]

SDOUT_SEL is shown in Figure 74 and described in Table 13.

Return to Summary Table.

Figure 74. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
							R/W

Table 13. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED		0	This bit is reserved
0	SDOUT_SEL	R	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

9.6.1.8 I2S_CTRL Register (Offset = 31h) [reset = 0x00]

I2S_CTRL is shown in Figure 75 and described in Table 14.

Return to Summary Table.

Figure 75. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCK_INV	RESERVED		RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

Table 14. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	BCK_INV	R/W	0	BCK Polarity This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode
4-0	RESERVED	R/W	00000	This bit is reserved

9.6.1.9 SAP_CTRL1 Register (Offset = 33h) [reset = 0x02]

SAP_CTRL1 is shown in Figure 76 and described in Table 15.

Return to Summary Table.

Figure 76. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB	RESERVED	DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

Table 15. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: lrclk pulse < 8 SCLK. If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, these two bits need set to 01.
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

9.6.1.10 SAP_CTRL2 Register (Offset = 34h) [reset = 0x00]

SAP_CTRL2 is shown in Figure 77 and described in Table 16.

Return to Summary Table.

Figure 77. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

Table 16. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: offset = 0 BCK (no offset) 000000001: ofsset = 1 BCK 000000010: offset = 2 BCKs and 111111111: offset = 512 BCKs

9.6.1.11 SAP_CTRL3 Register (Offset = 35h) [reset = 0x11]

SAP_CTRL3 is shown in Figure 78 and described in Table 17.

Return to Summary Table.

Figure 78. SAP_CTRL3 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">LEFT_DAC_DPATH</td><td colspan="2">RESERVED</td><td colspan="2">RIGHT_DAC_DPATH</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
</table>

Table 17. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	LEFT_DAC_DPATH	R/W	01	Left DAC Data Path. These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	RESERVED	R/W	00	This bit is reserved
1-0	RIGHT_DAC_DPATH	R/W	01	Right DAC Data Path. These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

9.6.1.12 FS_MON Register (Offset = 37h) [reset = 0x00]

FS_MON is shown in Figure 79 and described in Table 18.

Return to Summary Table.

Figure 79. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS			
R/W		R		R			

Table 18. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	BCLK_RATIO_HIGH	R	00	2 msbs of detected BCK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 4 'b0000 FS Error 4 'b0010 8KHz 4 'b0100 16KHz 4 'b0110 32KHz 4 'b1000 Reserved 4 'b1001 48KHz 4 'b1011 96KHz Others Reserved

9.6.1.13 BCK_MON Register (Offset = 38h) [reset = 0x00]

BCK_MON is shown in Figure 80 and described in Table 19.

Return to Summary Table.

Figure 80. BCK_MON Register

7	6	5	4	3	2	1	0
BCLK_RATIO_LOW							
R							

Table 19. BCK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK ratio, the number of BCK clocks in one audio frame. BCK = 32 FS~512 FS

9.6.1.14 CLKDET_STATUS Register (Offset = 39h) [reset = 0x00]

CLKDET_STATUS is shown in Figure 81 and described in Table 20.

Return to Summary Table.

Figure 81. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

Table 20. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-0	DET_STATUS	R	000000	bit0: In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag will be also asserted. bit1: This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-512FS to be valid. bit2: This bit indicates whether the BCK is missing or not. bit3:This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. bits4:This bit indicates whether the PLL is overrate bits5:This bit indicates whether the BCLK is overrate or underrate

9.6.1.15 DIG_VOL_CTL Register (Offset = 4Ch) [reset = 30h]

DIG_VOL_CTL is shown in Figure 82 and described in Table 21.

Return to Summary Table.

Figure 82. DIG_VOL_CTL Register

7	6	5	4	3	2	1	0
PGA							
R/W							

Table 21. DIG_VOL_CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA	R/W	00110000	Digital Volume These bits control both left and right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB .... and 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB .... 11111110: -103 dB 11111111: Mute

9.6.1.16 DIG_VOL_CTRL2 Register (Offset = 4Eh) [reset = 0x33]

DIG_VOL_CTRL2 is shown in Figure 83 and described in Table 22.

Return to Summary Table.

Figure 83. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

Table 22. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each updat e 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

9.6.1.17 DIG_VOL_CTRL3 Register (Offset = 4Fh) [reset = 0x30]

DIG_VOL_CTRL3 is shown in Figure 84 and described in Table 23.

Return to Summary Table.

Figure 84. DIG_VOL_CTRL3 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FAST_RAMP_DOWN_SPEED</td><td colspan="2">FAST_RAMP_DOWN_STEP</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="4">R/W</td></tr>
</table>

Table 23. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.18 AUTO_MUTE_CTRL Register (Offset = 50h) [reset = 0x07]

AUTO_MUTE_CTRL is shown in Figure 85 and described in Table 24.

Return to Summary Table.

Figure 85. AUTO_MUTE_CTRL Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">REG_AUTO_MUTE_CTRL</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
</table>

Table 24. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	REG_AUTO_MUTE_CTRL	R/W	111	bit0: 0: Disable left channel auto mute 1: Enable left channel auto mute bit1: 0: Disable right channel auto mute 1: Enable right channel auto mute bit2: 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.

9.6.1.19 AUTO_MUTE_TIME Register (Offset = 51h) [reset = 0x00]

AUTO_MUTE_TIME is shown in Figure 86 and described in Table 25.

Return to Summary Table.

Figure 86. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

Table 25. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

9.6.1.20 ANA_CTRL Register (Offset = 53h) [reset = 0x00]

ANA_CTRL is shown in Figure 87 and described in Table 26.

Return to Summary Table.

Figure 87. ANA_CTRL Register

7	6	5	4	3	2	1	0
ANA_CTRL							
R/W							

Table 26. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANA_CTRL	R/W	00000000	bit6~5: classd bandwidth control, "00": 80kHz; "01": 100kHz; "10": 120kHz; "11": 175kHz. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance. bit4: Reserved bit3: Reserved bit2~1: Reserved bit0: Reserved

9.6.1.21 AGAIN Register (Offset = 54h) [reset = 0x00]

AGAIN is shown in Figure 88 and described in Table 27.

Return to Summary Table.

Figure 88. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R/W			R/W				

Table 27. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control , with 0.5dB one step This bit controls the analog gain. 00000: 0 dB (29.5V peak voltage) 00001:-0.5db 11111: -15.5 dB

9.6.1.22 BQ_WR_CTRL1 Register (Offset = 5Ch) [reset = 0x00]

BQ_WR_CTRL1 is shown in Figure 89 and described in Table 28.

Return to Summary Table.

Figure 89. BQ_WR_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED							BQ_WR_FIRST_COEF
R/W							R/W

Table 28. BQ_WR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.

9.6.1.23 DAC_CTRL Register (Offset = 5Dh) [reset = 0xF8]

DAC_CTRL is shown in Figure 90 and described in Table 29.

Return to Summary Table.

Figure 90. DAC_CTRL Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DAC_FREQUENCY_SEL</td><td colspan="2">DAC_DITHER_EN</td><td colspan="3">DAC_DITHER</td><td colspan="2">DAC_CTRL_DEM_SEL</td></tr>
<tr><td>R/W</td><td colspan="2">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
</table>

Table 29. DAC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_FREQUENCY_SEL	R/W	1	DAC FREQ SEL 0:6.144M 1:3.072M
6-5	DAC_DITHER_EN	R/W	11	DITHER_EN, 00-disable both stage dither 01-enable main stage dither 10-enable second stage dither 11- enbale both stage dither
4-2	DAC_DITHER	R/W	110	Dither level 100-2^-7 101-2^-8 110-2^-9 111-2^-10 000-2^-13 001-2^-14 010-2^-15 011-2^-16
1-0	DAC_CTRL_DEM_SEL	R/W	00	00: Enable DEM 11: Disable DEM

9.6.1.24 ADR_PIN_CTRL Register (Offset = 60h) [reset = 0h]

ADR_PIN_CTRL is shown in Figure 91 and described in Table 30.

Return to Summary Table.

Figure 91. ADR_PIN_CTRL Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ADR_OE</td></tr>
<tr><td colspan="7"></td><td>R/W - 0x0</td></tr>
</table>

Table 30. ADR_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	ADR_OE	R/W	0	ADR Output Enable This bit sets the direction of the ADR pin 0: ADR is input 1: ADR is output

9.6.1.25 ADR_PIN_CONFIG Register (Offset = 61h) [reset = 0x00]

ADR_PIN_CONFIG is shown in Figure 92 and described in Table 31.

Return to Summary Table.

Figure 92. ADR_PIN_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED			ADR_PIN_CONFIG				
			R/W				

Table 31. ADR_PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ADR_PIN_CONFIG	R/W	00000	00000: off (low) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 0101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock missing) 00111: Reserved 01001: Reserved 01011: ADR as FAULTZ output

9.6.1.26 DSP_MISC Register (Offset = 66h) [reset = 0h]

DSP_MISC is shown in Figure 93 and described in Table 32.

Return to Summary Table.

Figure 93. DSP_MISC Register

7	6	5	4	3	2	1	0
BYPASS_CONTROL							
R/W							

Table 32. DSP_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYPASS CONTROL	R/W	00000000	bit0: 1-> bypass EQ (Only bypass EQs in L/R channel) bit1:1-> bypass DRC (Only bypass DRC in L/R channel) bit2:1-> bypass 128 tap FIR bit3:1-> Left and Right will have use unique coef 0->Right channel will share left channel coefficient bit4~bit7:reserved

9.6.1.27 DIE_ID Register (Offset = 67h) [reset = 0h]

DIE_ID is shown in Figure 94 and described in Table 33.

Return to Summary Table.

Figure 94. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-0h							

Table 33. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	0h	DIE ID

9.6.1.28 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in Figure 95 and described in Table 34.

Return to Summary Table.

Figure 95. POWER_STATE Register

7	6	5	4	3	2	1	0
STATE_RPT							
R							

Table 34. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	0: Deep sleep 1: Seep 2: HIZ 3: Play Others: reserved

9.6.1.29 AUTOMUTE_STATE Register (Offset = 69h) [reset = 0x00]

AUTOMUTE_STATE is shown in Figure 96 and described in Table 35.

Return to Summary Table.

Figure 96. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						ZERO_RIGHT_MON	ZERO_LEFT_MON
R						R	R

Table 35. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

9.6.1.30 PHASE_CTRL Register (Offset = 6Ah) [reset = 0x00]

PHASE_CTRL is shown in Figure 97 and described in Table 36.

Return to Summary Table.

Figure 97. PHASE_CTR Register

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		PHASE_SYNC_SEL	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

Table 36. PHASE_CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/W	00	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. 00: phase 0 01: phase1 10: phase2 11: phase3
1	I2S_SYNC_EN	R/W	0	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0	0: RAMP phase sync disable 1: RAMP phase sync enable

9.6.1.31 SS_CTRL0 Register (Offset = 6Bh) [reset = 0x00]

SS_CTRL0 is shown in Figure 98 and described in Table 37.

Return to Summary Table.

Figure 98. SS_CTRL0 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>RESERVED</td><td>SS_PRE_DIV_SEL</td><td>SS_MANUAL_MODE</td><td colspan="2">RESERVED</td><td>SS_RDM_EN</td><td>SS_TRI_EN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
</table>

Table 37. SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	set ramp ss controller to manual mode
3-2	RESERVED	R/W	0	This bit is reserved
1	SS_RDM_EN	R/W	0	random SS enable
0	SS_TRI_EN	R/W	0	triangle SS enable

9.6.1.32 SS_CTRL1 Register (Offset = 6Ch) [reset = 0x00]

SS_CTRL1 is shown in Figure 99 and described in Table 38.

Return to Summary Table.

Figure 99. SS_CTRL1 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">SS_RDM_CTRL</td><td colspan="4">SS_TRI_CTRL</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
</table>

Table 38. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	random SS range control
3-0	SS_TRI_CTRL	R/W	0000	triangle SS frequency and range control

9.6.1.33 SS_CTRL2 Register (Offset = 6Dh) [reset = 0x50]

SS_CTRL2 is shown in Figure 100 and described in Table 39.

Return to Summary Table.

Figure 100. SS_CTRL2 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TM_FREQ_CTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
</table>

Table 39. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	01010000	control ramp frequency in manual mode, F=61440000/N

9.6.1.34 SS_CTRL3 Register (Offset = 6Eh) [reset = 0x11]

SS_CTRL3 is shown in Figure 101 and described in Table 40.

Return to Summary Table.

Figure 101. SS_CTRL3 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TM_DSTEP_CTRL</td><td colspan="4">TM_USTEP_CTRL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
</table>

Table 40. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	control triangel mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	control triangle mode spread spectrum rise step in ramp ss manual mode

9.6.1.35 SS_CTRL4 Register (Offset = 6Fh) [reset = 0x24]

SS_CTRL4 is shown in Figure 102 and described in Table 41.

Return to Summary Table.

Figure 102. SS_CTRL4 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="2">TM_AMP_CTRL</td><td colspan="5">SS_TM_PERIOD_BOUNDRY</td></tr>
<tr><td>R/W</td><td colspan="2">R/W</td><td colspan="5">R/W</td></tr>
</table>

Table 41. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	control triangle mode spread spectrum boundary in ramp ss manual mode

9.6.1.36 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in Figure 103 and described in Table 42.

Return to Summary Table.

Figure 103. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

Table 42. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	left channel DC fault
2	CH2_DC_1	R	0	right channel DC fault
1	CH1_OC_I	R	0	left channel over current fault
0	CH2_OC_I	R	0	right channel over current fault

9.6.1.37 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in Figure 104 and described in Table 43.

Return to Summary Table.

Figure 104. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR				CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R				R	R	R

Table 43. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0h	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0h	the recent BQ is written failed
5-3	RESERVED	R	0h	This bit is reserved
2	CLK_FAULT_I	R	0h	clock fault
1	PVDD_OV_I	R	0h	PVDD OV fault
0	PVDD_UV_I	R	0h	PVDD UV fault

9.6.1.38 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in Figure 105 and described in Table 44.

Return to Summary Table.

Figure 105. GLOBAL_FAULT2 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="2">RESERVED</td><td>OTSD_I</td></tr>
<tr><td colspan="5">R</td><td colspan="2">R</td><td>R</td></tr>
</table>

Table 44. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000	This bit is reserved
0	OTSD_I	R	0	over temperature shut down fault

9.6.1.39 OT WARNING Register (Offset = 73h) [reset = 0x00]

OT_WARNING is shown in Figure 106 and described in Table 45.

Return to Summary Table.

Figure 106. OT_WARNING Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">RESERVED</td><td>OTW</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
</table>

Table 45. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	This bit is reserved
5-3	RESERVED	R	000	This bit is reserved
2	OTW	R	0	over temperature warning ,130C
1-0	RESERVED	R	00	This bit is reserved

9.6.1.40 PIN_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN_CONTROL1 is shown in Figure 107 and described in Table 46.

Return to Summary Table.

Figure 107. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDD_UV	MASK_DVDD_OV	MASK_CLK_FAULT	MASK_PVDD_UV	MASK_PVDD_OV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 46. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	mask OTSD fault report
6	MASK_DVDD_UV	R/W	0	mask DVDD UV fault report
5	MASK_DVDD_OV	R/W	0	mask DVDD OV fault report
4	MASK_CLK_FAULT	R/W	0	mask clock fault report
3	MASK_PVDD_UV	R/W	0	mask PVDD UV fault report
2	MASK_PVDD_OV	R/W	0	mask PVDD OV fault report
1	MASK_DC	R/W	0	mask DC fault report
0	MASK_OC	R/W	0	mask OC fault report

9.6.1.41 PIN_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN_CONTROL2 is shown in Figure 108 and described in Table 47.

Return to Summary Table.

Figure 108. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED		CLKFLT_LATCH_EN	OTSD_LATCH_EN	OTW_LATCH_EN	MASK_OTW	RESERVED	
		R/W	R/W	R/W	R/W		

Table 47. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	11	This bit is reserved
5	CLKFLT_LATCH_EN	R/W	1	enable clock fault latch
4	OTSD_LATCH_EN	R/W	1	enable OTSD fault latch
3	OTW_LATCH_EN	R/W	1	enable OT warning latch
2	MASK_OTW	R/W	0	mask OT warning report
1-0	RESERVED	R/W	00	This bit is reserved

9.6.1.42 MISC_CONTROL Register (Offset = 76h) [reset = 0x00]

MISC_CONTROL is shown in Figure 109 and described in Table 48.

Return to Summary Table.

Figure 109. MISC_CONTROL Register

7	6	5	4	3	2	1	0
DET_STATUS_ LATCH	RESERVED		OTSD_AUTO_ REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

Table 48. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:latch clock detection status 0:don't latch clock detection status
6-5	RESERVED	R/W	00	This bit is reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.43 FAULT_CLEAR Register (Offset = 78h) [reset = 0x00]

FAULT_CLEAR is shown in Figure 110 and described in Table 49.

Return to Summary Table.

Figure 110. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR	RESERVED						
W	R/W						

Table 49. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT. Once write this bit to 1, device will clear analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5805M device into the larger system.

10.1.1 Bootstrap Capacitors

The output stage of the TAS5805M uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22-µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22-µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22-µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

10.1.2 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1-µF or 0.1-µF capacitors as close as possible to the PVDD pins of the device.

10.1.3 Output EMI Filtering

The TAS5805M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

10.2 Typical Applications

10.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

Figure 111 shows the 2.0 (Stereo BTL) system application.

Typical Applications (continued)

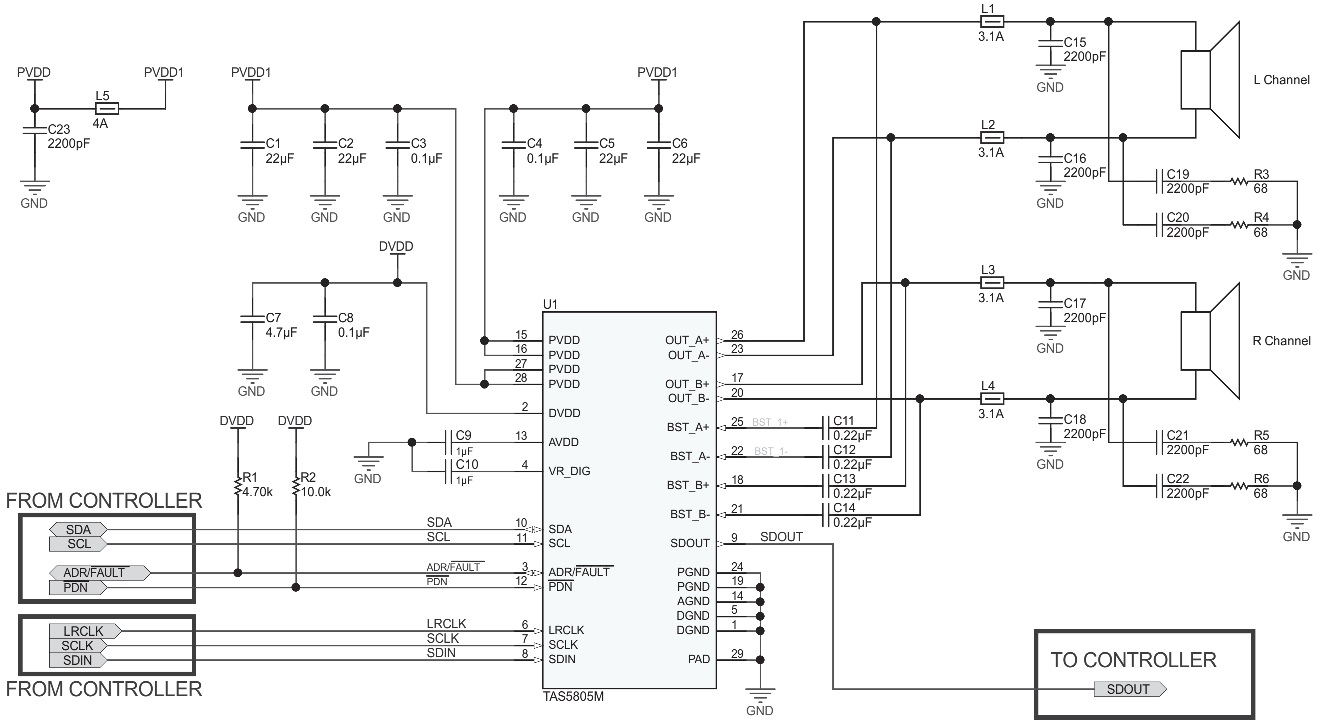


Figure 111. 2.0 (Stereo BTL) System Application Schematic with Ferrite Bead as the output filter

Typical Applications (continued)

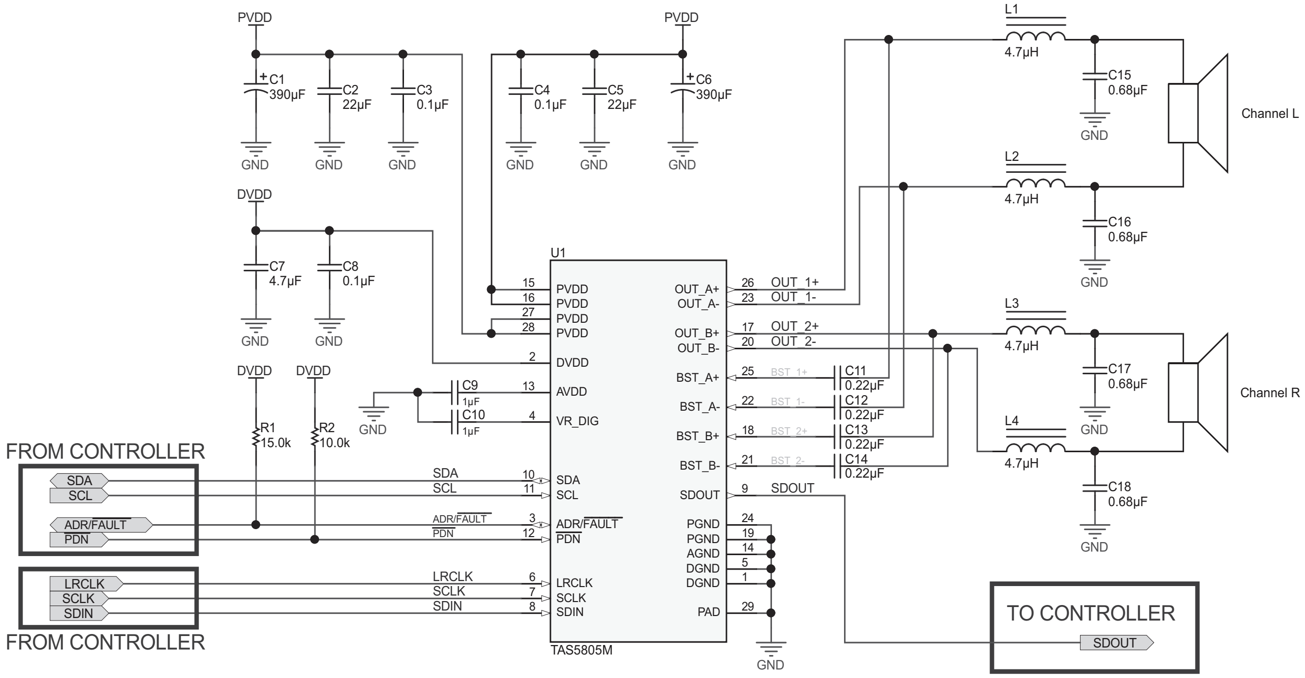


Figure 112. 2.0 (Stereo BTL) System Application Schematic with Inductor as the output filter

10.2.1.1 Design Requirements

- Power supplies:
  - 3.3-V or 1.8-V supply
  - 4.5-V to 24-V supply
- Communication: host processor serving as I^{2}C compliant master
- External memory (Such as EEPROM and FLASH) used for coefficients

The requirement for the supporting components for the TAS5805M device in a Stereo 2.0 (BTL) system is provide in Table 50 and Table 51

Table 50. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Ferrite bead as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C2,C5,C6	22uF	0805	CAP, CERM, 22 µF, 35 V, +/- 20%, JB, 0805
C3,C4	0.1uF	0402	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402
C7	4.7uF	0603	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603

Typical Applications (continued)

Table 50. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Ferrite bead as output filter) (continued)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C8	0.1uF	0603	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603
C9,C10	1uF	0603	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0603
R1	4.70k	0402	RES, 4.70 k, 1%, 0.0625 W, 0402
R2	10.0k	0404	RES, 10.0 k, 1%, 0.063 W, 0402
C11,C12,C13,C14	0.22uF	0603	CAP, CERM, 0.22 µF, 50 V, +/- 10%, X7R, 0603
C15,C16,C17,C18,C19, C20,C21,C22,C23	2200pF	0603	CAP, CERM, 2200 pF, 100 V,+/- 10%, X7R, 0603
R3,R4,R5,R6	68 ohm	0603	ES, 68, 5%, 0.1 W, 0603
L1,L2,L3,L4	300 ohm	0806	Ferrite Bead, 300 ohm @ 100 MHz, 3.1 A, 0806
L5	100 ohm	0806	Ferrite Bead, 100 ohm @ 100 MHz, 4 A, 0806

With Low EMI technology, TAS5805M keeps enough EMI margin for most of application cases where PVDD < 14V with ferrite bead (Low BOM cost). With Ferrite Bead and capacitor as the output filter, Figure 111 and Table 50 includes a good configuration (Proper value of Ferrite bead, Capacitor, Resistor) to achieve enough EMI margin for the typical case which PVDD = 12V, Speaker Load = 8Ω/6Ω, each speaker wire with 1m length, Output Power = 1W/4W/8W for each channel.

- Select Ferrite bead (L1~L5). The trade-off is impedance and rated current. If the rated current meet the system's requirement, larger impedance means larger EMI margin for the EMI, especially for the frequency band 5MHz~50MHz. The typical ferrite bead recommend for TAS5805M is NFZ2MSM series (Murata) and UPZ2012E series (Sunlord). 300 ohm @ 100MHz ferrite bead is a typical value which can pass EMI for most of application cases.
- Select capacitor (C15~C23). The trade-off is capacitor value and idle current. Larger capacitor means larger idle current, increase the capacitor value from 1nF to 2.2nF makes much help for frequency band 5MHz~100MHz.
- Using Ferrite bead as the output filter, recommend designer to use Fsw=384kHz with Spread spectrum enable, BD Modulation, refer to Spread Spectrum
- With Ferrite bead as the output power. In order to pass EMI (AC Conducted Emission) standard, an AC to DC adapter with EMI filter in it is needed. For most of applications (TV/Voice Control Speaker/Wireless speaker/Soundbar) which need a 110V~220V power supply usually has a EMI filter in the AC to DC adapter. Some cases use DC power supply and also need to test the DC Conducted Emission , this applications (Automotive/Industry) need a simple EMI filter on PVDD for TAS5805M. Refer to application note: AN-2162 Simple Success With Conducted EMI From DC to DC Converters.

Table 51. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Inductor as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C6	390uF	10mmx10mm	CAP, AL, 390 µF, 35 V, +/- 20%, 0.08 ohm, SMD
C2,C5	22uF	0603	CAP, CERM, 22 µF, 35 V, +/- 20%, JB, 0805
C3,C4	0.1uF	0402	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402
C7	4.7uF	0603	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603
C8	0.1uF	0603	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603
C9,C10	1uF	0603	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0603
R1	4.70k	0402	RES, 4.70 k, 1%, 0.0625 W, 0402
R2	10.0k	0404	RES, 10.0 k, 1%, 0.063 W, 0402
C11,C12,C13,C14	0.22uF	0603	CAP, CERM, 0.22 µF, 50 V, +/- 10%, X7R, 0603
C15,C16,C17,C18	0.68uF	0805	CAP, CERM, 0.68 µF, 50 V, +/- 10%, X7R, 0805
L1,L2,L3,L4	4.7uH	6.3x4.5x6.3mm	Inductor, Shielded, 4.7 µH, 4 A, 0.023 ohm, SMD

With Inductor as the output filter, designers can achieve ultra low idle current (with Hybrid Modulation or 1SPW Modulation) and keep large EMI margin. As the switching frequency of TAS5805M can be adjustable from 384kHz to 768kHz. Higher switching frequency means smaller Inductor value needed.

- With 768kHz switching frequency. Designers can select 10uH + 0.68uF or 4.7uH +0.68uF as the output filter, this will help customer to save the Inductor size with the same rated current during the inductor selection. With 4.7uH + 0.68uF, make sure PVDD ≤ 18V to avoid the large ripple current to trigger the OC threshold (5A).
- With 384kHZ switching frequency. Designers can select 22uH + 0.68uF or 15uH + 0.68uF or 10uH + 0.68uF as the output filter, this will help customer to save power dissipation for some battery power supply application. With 10uH + 0.68uF, make sure PVDD ≤ 18V to avoid the large ripple current to trigger the OC threshold (5A).

10.2.1.2 Detailed Design Procedures

Design Procedures can be used for Stereo 2.0, Mono, 2.1 system.

10.2.1.2.1 Step One: Hardware Integration

- Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
  - For questions and support, go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

10.2.1.2.2 Step Two: Hardware Integration

Using the TAS5805MEVM evaluation module and the PPC3 app to configure the desired device settings.

10.2.1.2.3 Step Three: Software Integration

- Using the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

10.2.1.3 Application Curves

10.2.1.3.1 Audio Performance

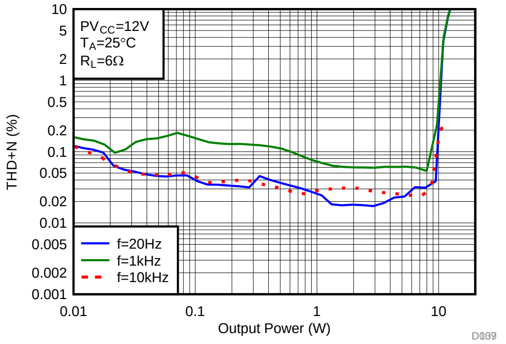


Figure 113. THD+N vs Frequency (Ferrite bead as Output Filter, Hybrid Modulation, BTL Mode)

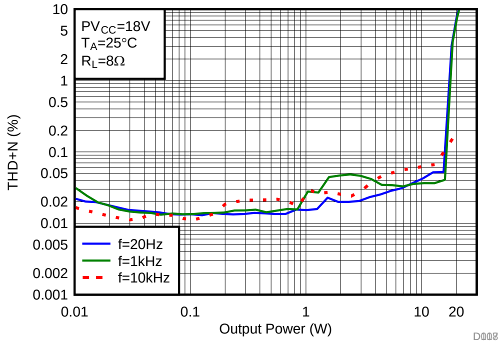
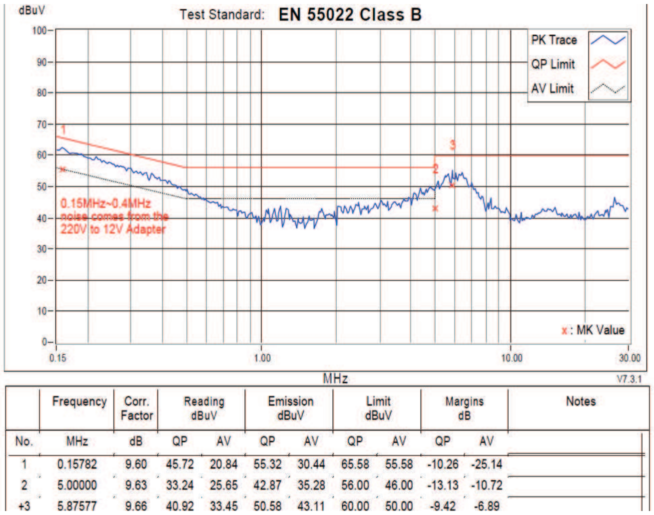


Figure 114. THD+N vs Frequency (Inductor as Output Filter, Hybrid Modulation, BTL Mode)

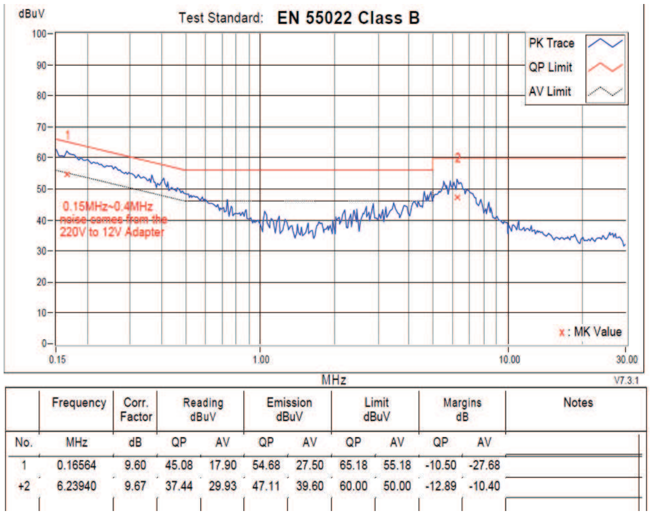
10.2.1.3.2 EN55022 Conducted Emissions Results with Ferrite Bead as output filter

With (Ferrite Bead as the output filter), 220V to 12V adapter from a major TV customer, 8-Ω speaker, Spread Spectrum Enabled, Stereo Output Power = 8W/CH, 1 meter speaker cable for each channel.



	Frequency	Corr. Factor	Reading dBuV		Emission dBuV		Limit dBuV		Margins dB		Notes
No.	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV	
1	0.15782	9.60	45.72	20.84	55.32	30.44	65.58	55.58	-10.26	-25.14	
2	5.00000	9.63	33.24	25.65	42.87	35.28	56.00	46.00	-13.13	-10.72	
+3	5.87577	9.66	40.92	33.45	50.58	43.11	60.00	50.00	-9.42	-6.89	

Figure 115. Conducted Emission with Ferrite Bead Filter - Line

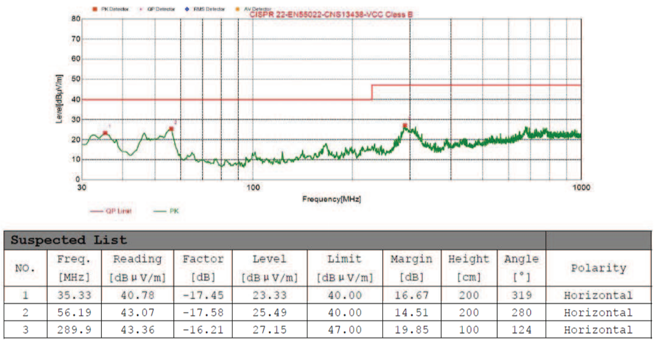


	Frequency	Corr. Factor	Reading dBuV		Emission dBuV		Limit dBuV		Margins dB		Notes
No.	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV	
1	0.16564	9.60	45.08	17.90	54.68	27.50	65.18	55.18	-10.50	-27.68	
+2	6.23940	9.67	37.44	29.93	47.11	39.60	60.00	50.00	-12.89	-10.40	

Figure 116. Conducted Emission with Ferrite Bead Filter - Neutral

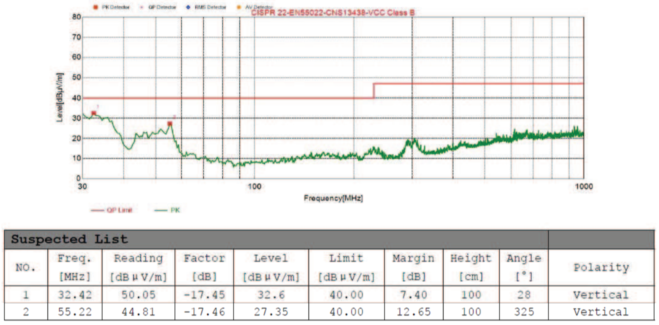
10.2.1.3.3 EN55022 Radiated Emissions Results with Ferrite Bead as output filter

With (Ferrite Bead as the output filter), 220V to 12V adapter from a major TV customer, 8-Ω speaker, Spread Spectrum Enabled, Stereo Output Power = 8W/CH, 1 meter speaker cable for each channel.



Suspected List									
NO.	Freq. [MHz]	Reading [dBμV/m]	Factor [dB]	Level [dBμV/m]	Limit [dBμV/m]	Margin [dB]	Height [cm]	Angle [°]	Polarity
1	35.33	40.78	-17.45	23.33	40.00	16.67	200	319	Horizontal
2	56.19	43.07	-17.58	25.49	40.00	14.51	200	280	Horizontal
3	289.9	43.36	-16.21	27.15	47.00	19.85	100	124	Horizontal

Figure 117. Radiated Emission with Ferrite Bead Filter - Horizontal



Suspected List									
NO.	Freq. [MHz]	Reading [dBμV/m]	Factor [dB]	Level [dBμV/m]	Limit [dBμV/m]	Margin [dB]	Height [cm]	Angle [°]	Polarity
1	32.42	50.05	-17.45	32.6	40.00	7.40	100	28	Vertical
2	55.22	44.81	-17.46	27.35	40.00	12.65	100	325	Vertical

Figure 118. Radiated Emission with Ferrite Bead Filter - Vertical

With Inductor as the output filter, the EMI margin reserve ≥ 15dB Margin for both Conducted Emission and Radiated Emission. More data are included in the application note -TAS5805M Design Considerations for EMC.

10.2.2 MONO (PBTL) Systems

In MONO mode, TAS5805M can be used as PBTL mode to drive sub-woofer with more output power.

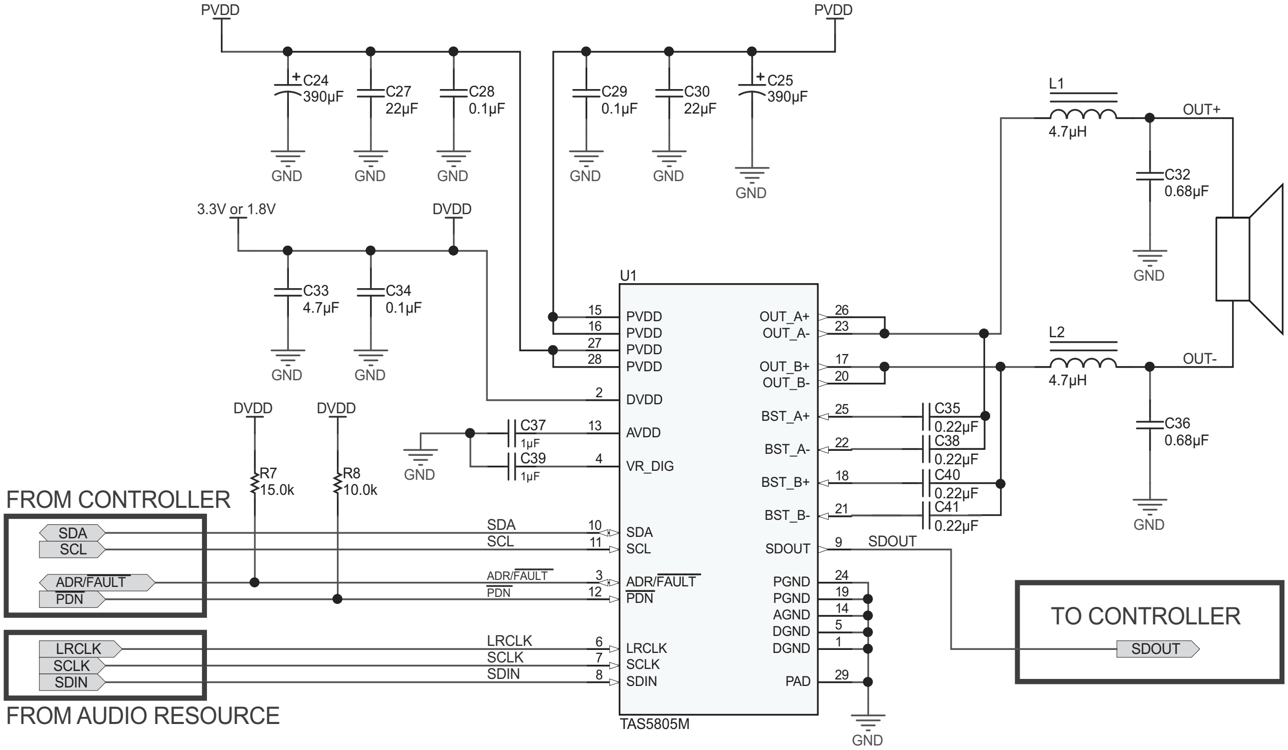


Figure 119. Mono (PBTL) System Application Schematic

10.2.2.1 Design Requirements

- Power supplies:
  - 3.3-V or 1.8-V supply
  - 4.5-V to 24-V supply
- Communication: host processor serving as I^{2}C compliant master
- External memory (Such as EEPROM and FLASH) used for coefficients

The requirement for the supporting components for the TAS5805M device in a MONO (PBTL) system is provide in Table 52

Table 52. Supporting Component Requirements for MONO (PBTL) system (With Inductor as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C24,C25	390uF	10mmx10mm	CAP, AL, 390 µF, 35 V, +/- 20%, 0.08 ohm, SMD
C27,C30	22uF	0603	CAP, CERM, 22 µF, 35 V, +/- 20%, JB, 0805
C28,C29	0.1uF	0402	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402
C33	4.7uF	0603	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603

Table 52. Supporting Component Requirements for MONO (PBTL) system (With Inductor as output filter) (continued)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C34	0.1uF	0603	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603
C37,C39	1uF	0603	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0603
R7	4.70k	0402	RES, 4.70 k, 1%, 0.0625 W, 0402
R8	10.0k	0404	RES, 10.0 k, 1%, 0.063 W, 0402
C35,C38,C40,C41	0.22uF	0603	CAP, CERM, 0.22 µF, 50 V, +/- 10%, X7R, 0603
C32,C36	0.68uF	0805	CAP, CERM, 0.68 µF, 50 V, +/- 10%, X7R, 0805
L1,L2	4.7uH		Inductor, Shielded, 4.7 µH, 8.7 A

10.2.2.2 Detailed Design Procedure

For information about the Detailed Design Procedure, see the *Detailed Design Procedures* section.

10.2.2.3 Application Curves

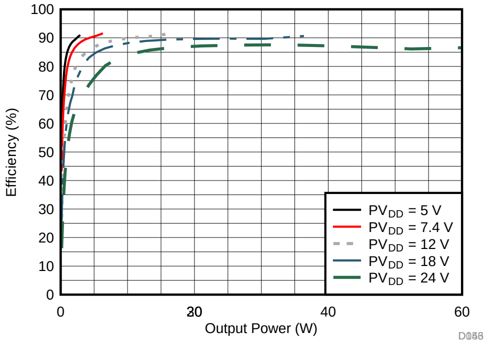


Figure 120. Efficiency vs Output Power (Inductor as Output Filter, Hybrid modulation, PBTL mode)

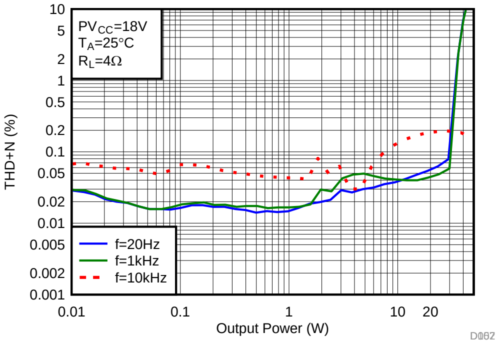


Figure 121. THD+N vs Output Power (Inductor as Output Filter, Hybrid Modulation, PBTL mode)

10.2.3 Advanced 2.1 System (Two TAS5805M Devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5805M devices are used - one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5805M device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which might come from a central systems processor. Figure 122 shows the 2.1 (Stereo BTL with Two TAS5805M devices) system application.

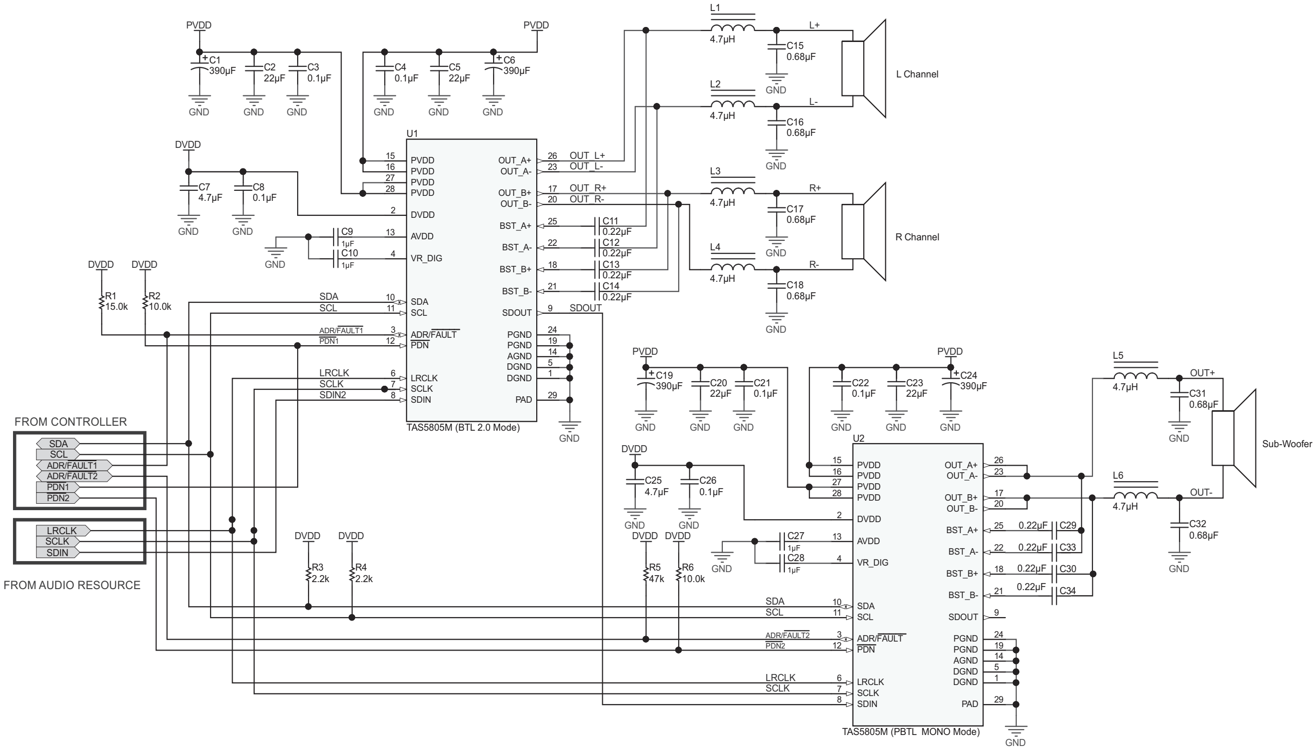


Figure 122. 2.1 (2.1 CH with Two TAS5805M Devices) Application Schematic

11 Power Supply Recommendations

The TAS5805M device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required powerup sequence. The power supplies can be powered on in any order. TI recommends waiting 1 ms to 5 ms for the DVDD power supplies to stabilize before starting I^2C communication and providing stable I^2S clock before enabling the device outputs.

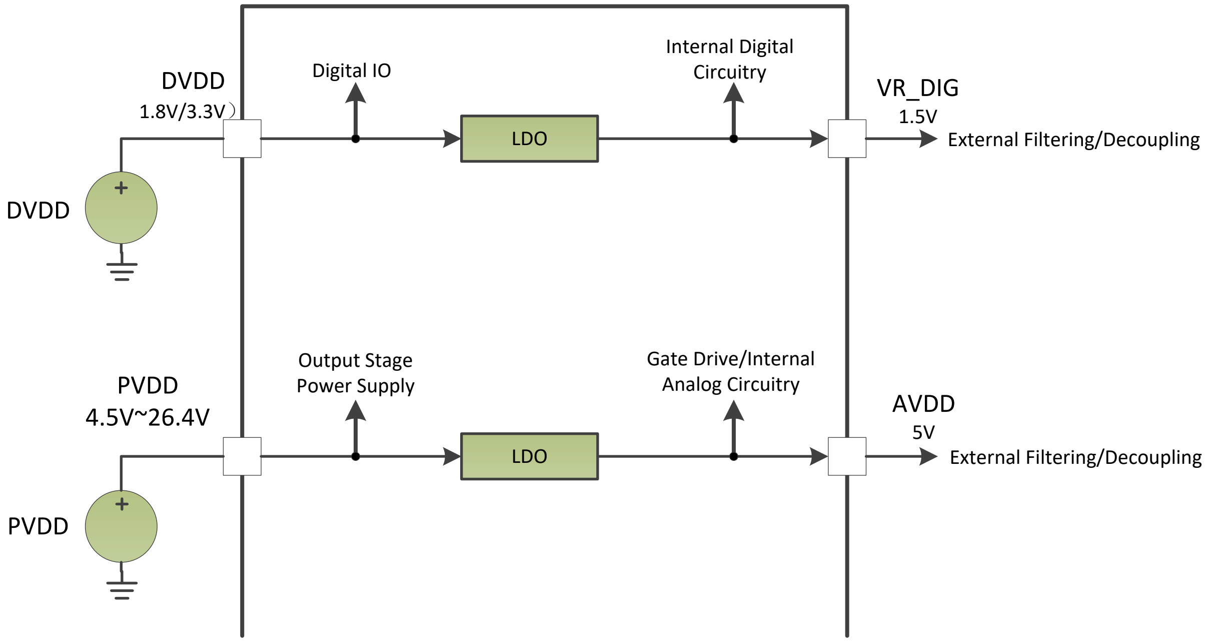


Figure 123. Power Supply Function Block Diagram

11.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in Figure 123, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Application and Implementation* section and the *Layout Example* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5805M device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

11.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5805MMEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5805M device *Application and Implementation*. Lack of proper decoupling, like that shown in the *Application and Implementation*, results in voltage spikes which can damage the device.

PVDD Supply (continued)

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5805M internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

12 Layout

12.1 Layout Guidelines

12.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the *Layout Example* section. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Example* section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

12.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5805M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5805M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the deice . For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

12.1.3 Optimizing Thermal Performance

Follow the layout example shown in the Figure 124 to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

12.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5805M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5805M device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5805M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5805M device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane

Layout Guidelines (continued)

from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

12.1.3.2 Stencil Pattern

The recommended drawings for the TAS5805M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

NOTE

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

12.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5805M device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5805M device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5805M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Layout Example* section, this interface can benefit from improved thermal performance.

NOTE

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drull must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Example* section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5805M device to open up the current path to and from the device.

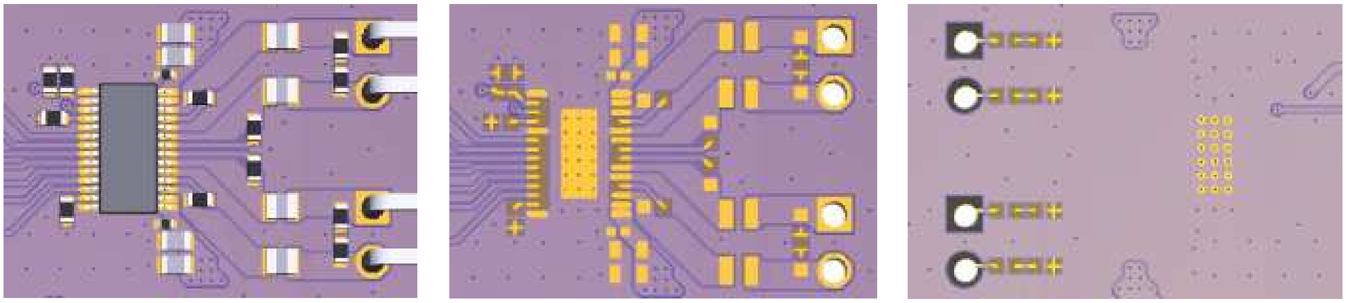
12.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to

Layout Guidelines (continued)

manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

12.2 Layout Example

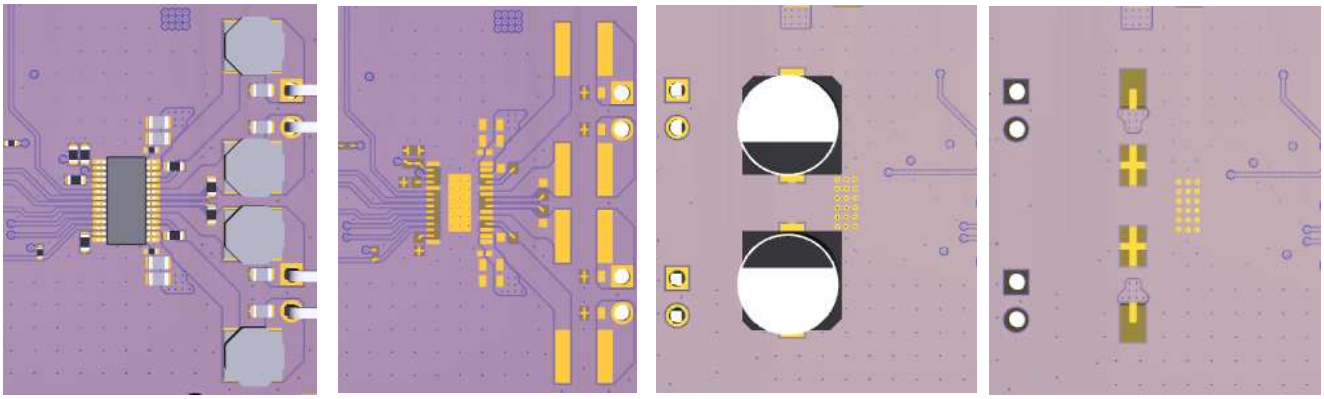


Top Layer 3D view

Top Layer Layout

Bot Layer Layout

Figure 124. 2.0 (Stereo BTL with Ferrite Bead as Output Filter) Layout View



Top Layer 3D view

Top Layer Layout

Bot Layer 3D view

Bot Layer Layout

Figure 125. 2.0 (Stereo BTL with Inductor as Output Filter) Layout View

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

The glossary listed in the *Glossary* section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. This device often configures the controls of the audio processing devices (like the) in the audio path in order to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$\mathbf{r_{DS(on)}}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

13.1.2 Development Support

For RDGUI software, please consult your local field support engineer.

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

17-Jul-2018

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTAS5805MPWPR	ACTIVE	HTSSOP	PWP	28	2000	TBD	Call TI	Call TI	-25 to 85		Samples
TAS5805MPWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5805MA1	Samples
TAS5805MPWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5805MA1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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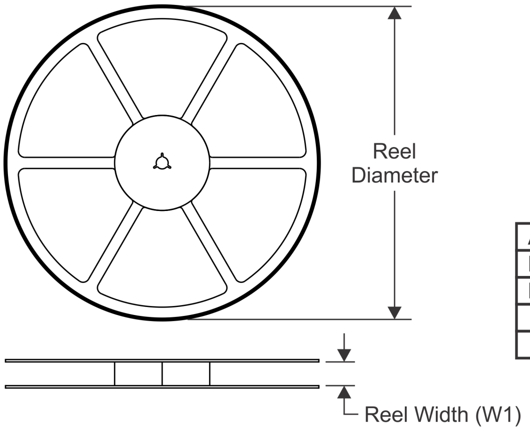
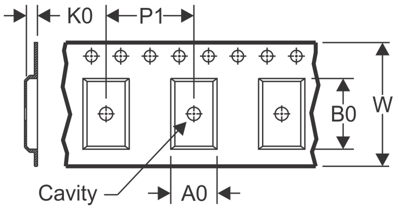
TAPE AND REEL INFORMATION

REEL DIMENSIONS

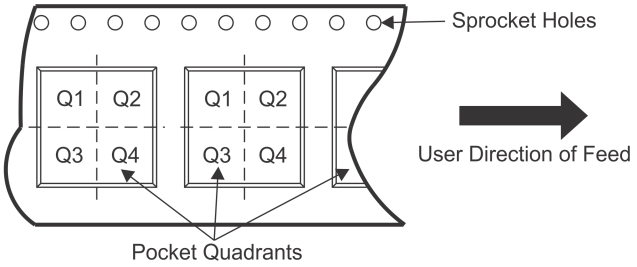


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

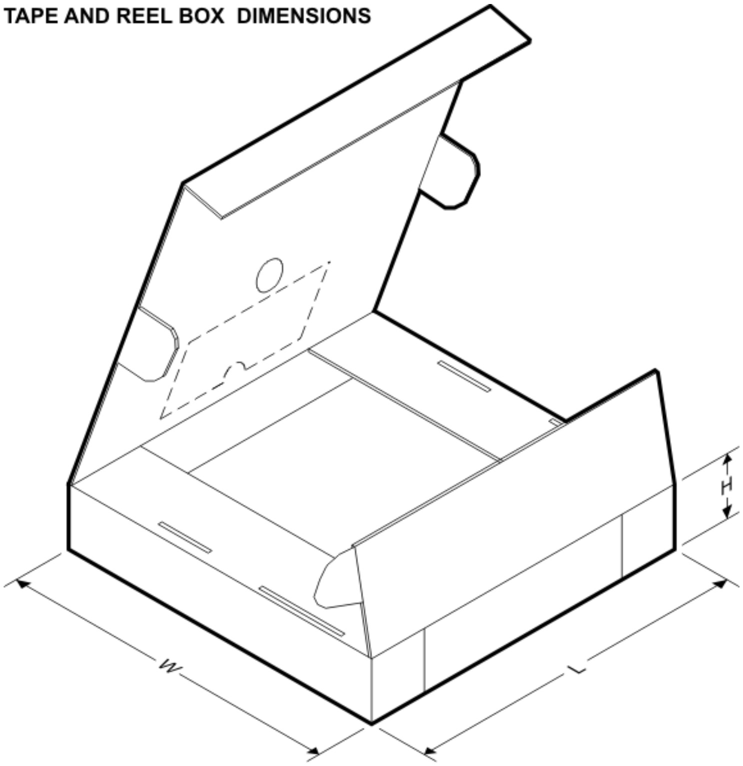
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5805MPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

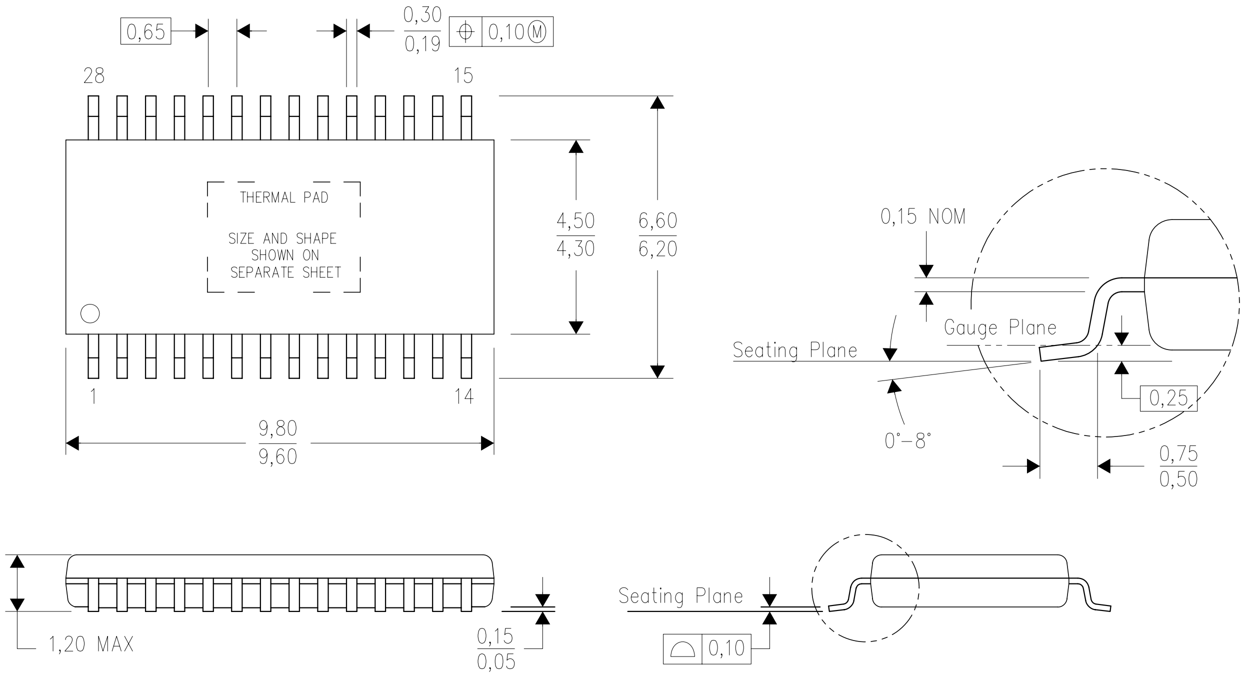
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5805MPWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



4073225–6/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO–153

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