20-W/15-W STEREO DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **2×20 W at 10% THD+N Into 8-Ω BTL at 18 V (With Heatsink for TAS5102)**
- **2×15 W at 10% THD+N Into 8-Ω BTL at 15.5 V for TAS5103**
- **2×10 W at 10% THD+N Into 8-Ω BTL at 13 V**
- **>100-dB SNR (A-Weighted)**
- **<0.1% THD+N at 1 W**
- **Thermally Enhanced Package: 32-pin HTSSOP**
  - **DAD (TAS5102) Pad Up**
  - **DAP (TAS5103) Pad Down**
- **High-Efficiency Power Stage (>90%) With 180-mΩ Output MOSFETs**
- **Wide PVDD Range from 8V to 23V**
- **Power-On Reset for Protection on Power Up Without Any Power-Supply Sequencing**
- **Integrated Self-Protection Circuits Including Undervoltage, Overtemperature, Overcurrent, Short Circuit**
- **Built-In Regulator for Gate Drive Supply**
- **Error Reporting**
- **EMI Compliant When Used With Recommended System Design**

APPLICATIONS

- **Televisions**
- **Mini/Micro Audio Systems**
- **DVD Receivers**
- **Home Theaters**

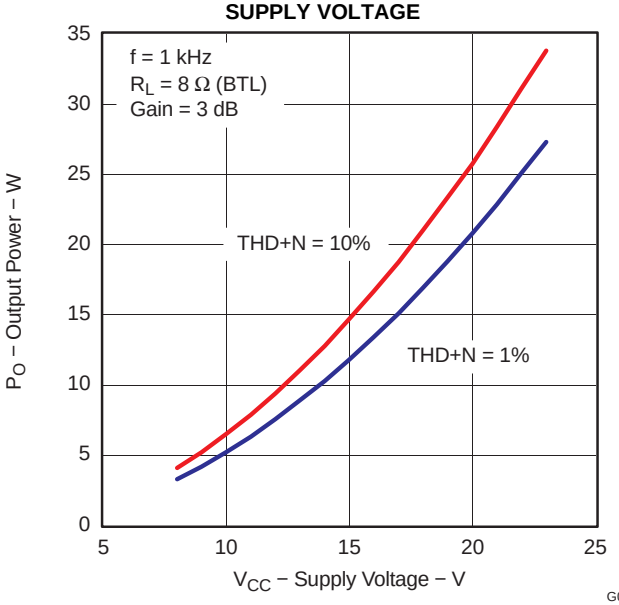
DESCRIPTION

The TAS5102/TAS5103 are integrated stereo digital amplifier power stages with an advanced protection system. The TAS5102/TAS5103 are capable of driving an 8-Ω bridge-tied load (BTL) at up to 20 W/15 W per channel with low integrated noise at the output, low THD+N performance, and low idle power dissipation.

A low-cost, high-fidelity audio system can be built using a TI chipset, comprising a modulator (e.g., TAS5086) and the TAS5102/TAS5103. This system only requires a simple passive LC demodulation filter to deliver high-quality, high-efficiency audio amplification with proven EMI compliance. These devices require two power supplies, at 3.3 V for VREG, and up to 23 V for PVDD. The TAS5102/TAS5103 does not require power-up sequencing due to internal power-on reset. The efficiency of this digital amplifier is greater than 90% into 8 Ω, which enables the use of smaller power supplies and heatsinks.

The TAS5102/3 has an innovative protection system integrated on chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and overtemperature protection. The TAS5102/TAS5103 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level music transients.

BTL OUTPUT POWER vs SUPPLY VOLTAGE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

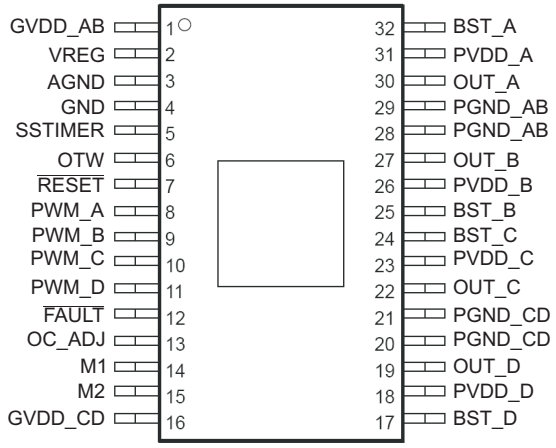
DEVICE INFORMATION

Pin Assignment

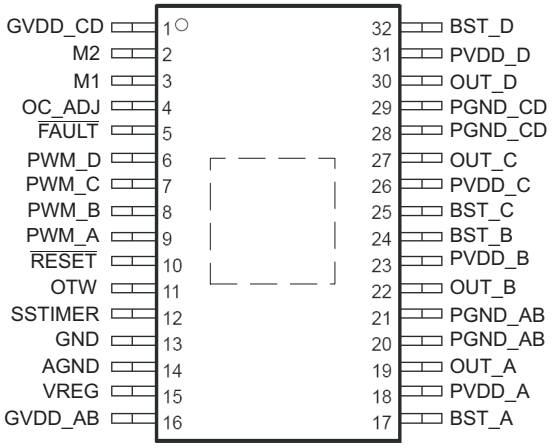
The TAS5102/TAS5103 are available in a thermally enhanced package:

- TAS5102 Pad Up 32-pin HTSSOP PowerPAD™ package (DAD)
- TAS5103 Pad Down 32-pin HTSSOP PowerPAD™ package (DAP)

DAD PACKAGE
(TOP VIEW)



DAP PACKAGE
(TOP VIEW)



MODE Selection Pins

Mode		PWM INPUT	OUTPUT CONFIGURATION	PROTECTION SCHEME
M2	M1			
0	0	2N (1) AD/BD modulation	2 channels BTL output	BTL mode (2)
0	1	1N (1) AD modulation	2 channels BTL output	BTL mode (2)
1	0	1N (1) AD modulation	4 channels SE output	Protection works similarly to BTL mode (2). Only difference in SE mode is that OUT_X is Hi-Z instead of a pulldown through internal pulldown resistor.
1	1	Reserved		

(1) The 1N and 2N naming convention is used to indicate the required number of PWM lines to the power stage per channel in a specific mode.
(2) An overcurrent protection (OC) occurring on A or B causes all channels to shut down. An OC on C or D works similarly. Global errors like overtemperature error (OTE), undervoltage protection (UVP), and power-on reset (POR) affect all channels.

Package Heat Dissipation Ratings

PARAMETER	TAS5102DAD	TAS5103DAP
$R_{\theta JC}$ (°C/W)	1.69	1.69
$R_{\theta JA}$ (°C/W)	See Note (1)	23.5

(1) The TAS5102 package is thermally enhanced for conductive cooling using an exposed metal pad area. It is impractical to use the device with the pad exposed to ambient air as the only means for heat dissipation for higher power applications.
For this reason, $R_{\theta JA}$, a system parameter that characterizes the thermal treatment, is provided in the Application Information section of the data sheet. An example and discussion of typical system $R_{\theta JA}$ values are provided in the Thermal Information section. This example provides additional information regarding the power dissipation ratings. This example should be used as a reference to calculate the heat dissipation ratings for a specific application. TI application engineering provides technical support to design heatsinks if needed. Also, for additional general information on PowerPad packages, see TI document SLMA002B.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			UNIT
	PVDD_X to GND_X DC	-0.3 to 23	V
	PVDD_X to GND_X (2)	–0.3 to 32	V
	OUT_X to GND_X (2)	–0.3 to 32	V
	BST_X to GND_X (2)	–0.3 to 43.2	V
	VREG to AGND	–0.3 to 4.2	V
	GVDD to GND	-0.3 to 13.2	V
	GND_X to GND	–0.3 to 0.3	V
	GND_X to AGND	–0.3 to 0.3	V
	GND to AGND	–0.3 to 0.3	V
	PWM_X, OC_ADJ, M1, M2 to AGND	–0.3 to 4.2	V
	$\overline{\text{RESET\_X}}$, $\overline{\text{FAULT}}$, OTW to AGND	–0.3 V to 7	V
	Maximum continuous sink current ($\overline{\text{FAULT}}$, OTW)	9	mA
T_J	Maximum operating junction temperature range,	0 to 150	°C
T_{STG}	Storage temperature range	–65 to 150	°C
	Minimum pulse duration, low	50	ns

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

ORDERING INFORMATION

T_A	PACKAGE(1)	DESCRIPTION
0°C to 70°C	TAS5102DAD	32-pin HTSSOP
	TAS5103DAP	32-pin HTSSOP

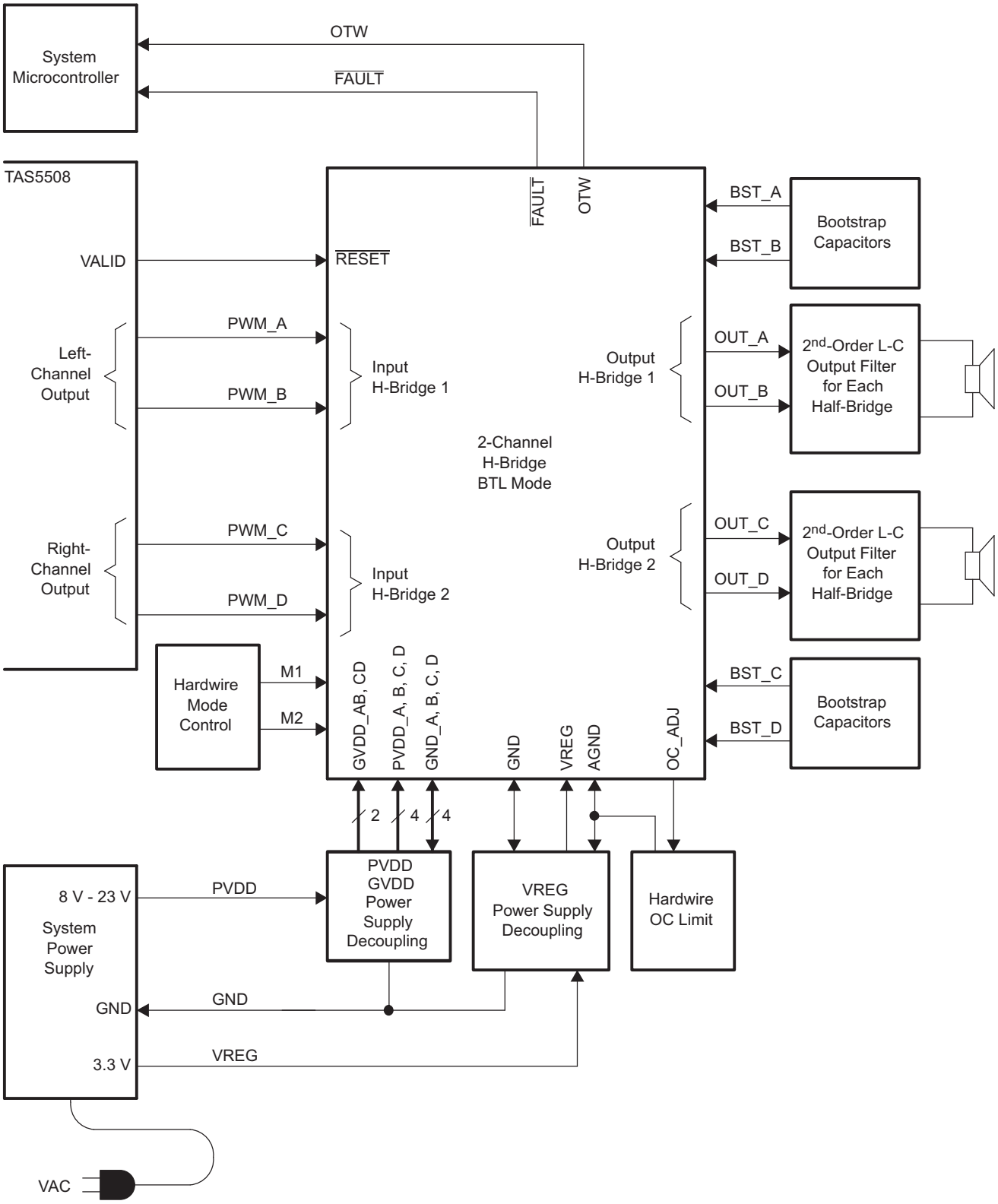
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Pin Functions

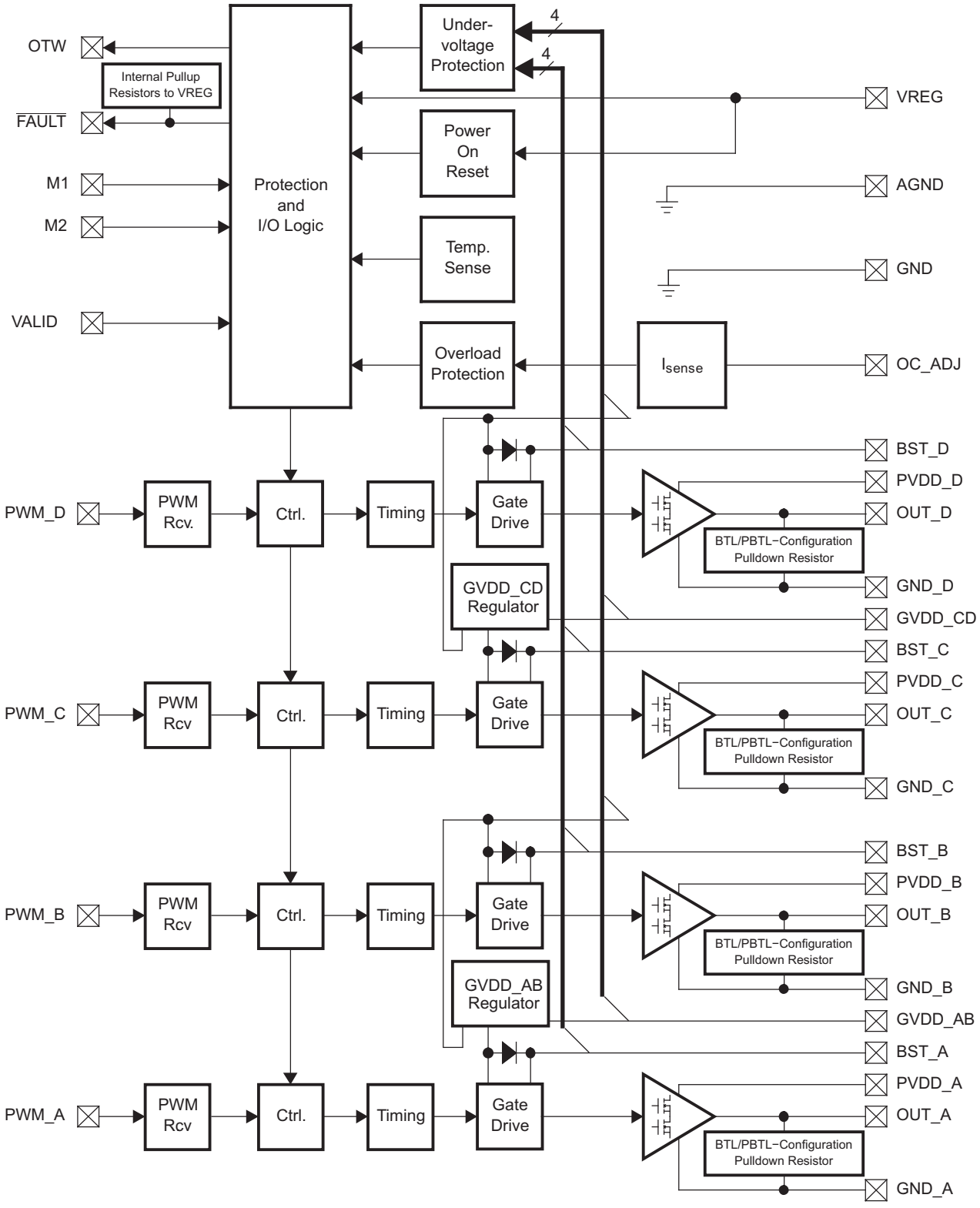
PIN			FUNCTION (1)	DESCRIPTION
NAME	TAS5102 NO.	TAS5103 NO		
AGND	3	14	P	Analog ground
BST_A	32	17	P	HS bootstrap supply (BST). External capacitor to OUT_A required.
BST_B	25	24	P	HS bootstrap supply (BST). External capacitor to OUT_B required.
BST_C	24	25	P	HS bootstrap supply (BST). External capacitor to OUT_C required.
BST_D	17	32	P	HS bootstrap supply (BST). External capacitor to OUT_D required.
$\overline{\text{FAULT}}$	12	5	O	Device error signal (shutdown); open drain
GND	4	13	P	Ground
PGND_AB	29	20	P	Power ground for half-bridges A and B
PGND_AB	28	21	P	Power ground for half-bridges A and B
PGND_CD	21	28	P	Power ground for half-bridges C and D
PGND_CD	20	29	P	Power ground for half-bridge D
GVDD_AB	1	16	P	Gate-drive voltage supply. Requires 1-μF capacitor to GND.
GVDD_CD	16	1	P	Gate-drive voltage supply. Requires 1-μF capacitor to GND.
M2	15	2	I	Mode selection 2, connect to either AGND or VREG, no pull-up or pull-down resistors
M1	14	3	I	Mode selection 1, connect to either AGND or VREG, no pull-up or pull-down resistors
OC_ADJ	13	4	O	Analog overcurrent programming. Requires resistor to ground.
OTW	6	11	O	Overtemperature warning signal, push-pull, active high
OUT_A	30	19	O	Output, half-bridge A
OUT_B	27	22	O	Output, half-bridge B
OUT_C	22	27	O	Output, half-bridge C
OUT_D	19	30	O	Output, half-bridge D
PVDD_A	31	18	P	Power supply input for half-bridge A. Requires close decoupling of 0.1-μF capacitor to GND_A.
PVDD_B	26	23	P	Power supply input for half-bridge B. Requires close decoupling of 0.1-μF capacitor to GND_B.
PVDD_C	23	26	P	Power supply input for half-bridge C. Requires close decoupling of 0.1-μF capacitor to GND_C.
PVDD_D	18	31	P	Power supply input for half-bridge D. Requires close decoupling of 0.1-μF capacitor to GND_D.
PWM_A	8	9	I	Input signal for half-bridge A
PWM_B	9	8	I	Input signal for half-bridge B
PWM_C	10	7	I	Input signal for half-bridge C
PWM_D	11	6	I	Input signal for half-bridge D
$\overline{\text{RESET}}$	7	10	I	PWM is not active if $\overline{\text{RESET}}$ goes low.
SSTIMER	5	12	I	Controls start/stop time of PWM modulation. Requires 2.2 nF capacitor to GND for AD BTL. Leave pin floating (NC) for BD BTL mode. Also, leave pin floating (NC) for SE mode.
VREG	2	15	P	Digital regulator supply filter. Requires 0.1-μF capacitor to AGND.

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{SS}	Half-bridge supply, PVDD_X	DC supply voltage	8	18	23	V
	Supply for Protection and I/O Logic, VREG	DC supply voltage	3	3.3	3.6	V
R_L (BTL)	Load impedance	Output filter: L = 10 µH, C = 470 nF. Output AD modulation, switching frequency > 350 kHz		6-8		Ω
R_L (SE)				3-4		
R_L (PBTL)				3-4		
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		200		nH
L_O (SE)				200		
L_O (PBTL)				200		
F_{PWM}	PWM frame rate		192	384	432	kHz
T_J	Junction temperature		0		125	°C

AC Characteristics (BTL)

PVDD_X = 18 V, BTL mode, R_L = 8 Ω, R_{OC} = 22 KΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, ambient temperature = 25°C (unless otherwise noted). Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V, 10% THD		20		W
		PVDD = 18 V, 7% THD		18		
		PVDD = 12 V, 10% THD		9		
		PVDD = 12 V, 7% THD		8		
THD+N	Total harmonic distortion + noise	PVDD = 18V, Po =10 W (half-power)		0.15		%
		PVDD = 12V, Po =4.5 W (half-power)		0.18		
		1 W		0.05		
V_n	Output integrated noise	A-weighted		50		µV
SNR	Signal-to-noise ratio (1)	A-weighted	94	105		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator	94	105		dB
P_D	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 4 channels switching (2)		0.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AC Characteristics (Single-Ended Output)

PVDD_X = 18 V, SE mode, R_L = 4 Ω, R_{OC} = 22 kΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, ambient temperature = 25°C (unless otherwise noted). Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V, 10% THD		10		W
		PVDD = 18 V, 7% THD		9		
		PVDD = 12 V, 10% THD		4.5		
		PVDD = 12 V, 7% THD		4		
THD+N	Total harmonic distortion + noise	PVDD = 18V, Po =5 W (half-power)		0.2		%
		PVDD = 12V, Po =2.25 W (half-power)		0.2		
V_n	Output integrated noise	A-weighted		50		μV
SNR	Signal-to-noise ratio (1)	A-weighted		105		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator		105		dB
P_D	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 4 channels switching (2)		0.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

DC Characteristics

R_L= 8 Ω, F_{PWM} = 384 kHz (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
V_{SS}	Digital Input Supply Voltage, VREG		3	3.3	3.6	V
$I_{(VREG)}$	Supply current, VREG	Operating, 50% duty cycle		6.5	10	mA
		Reset mode, no switching		6.5	10	
$I_{(PVDD\_X)}$	Total Half-bridge idle current	50% duty cycle, without output filter or load		35	50	mA
		Reset mode, no switching		5	6.3	
Output Stage MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance		180		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance		180		mΩ
I/O Protection						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X, voltage rising			5.7		V
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X, voltage falling			5.5		V
OTW(1)	Overtemperature warning			125		°C
OTW_{HYST}(1)	Temperature drop needed below OTW temperature for OTW to be inactive after the OTW event			25		°C
OTE(1)	Overtemperature error			150		°C
OTE-OTW(1)	OTE-OTW differential			25		°C
OTE_{HYST}(1)	A RESET must occur to exit shutdown and to release $\overline{FAULT}$ following an OTE event.			30		°C
OCPC	Overcurrent protection counter	F_{PWM} = 384 kHz		0.63		ms
I_{OC}	Overcurrent limit protection	Resistor—programmable, max. current, R_{OCP} = 22 kΩ		4.5		A
I_{OCT}	Overcurrent response time			150		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20kΩ.	20	22	24	kΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge. Not used in SE mode		3		kΩ

(1) Specified by design

DC Characteristics (continued)

R_L= 8 Ω, F_{PWM} = 384 kHz (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, $\overline{\text{RESET}}$	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{lkg}	Input leakage current	Static, High PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, $\overline{\text{RESET}}$			100	µA
		Static, Low PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, $\overline{\text{RESET}}$	–10		10	µA
$\overline{\text{FAULT}}$						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{FAULT}}$		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V			5.5	V
V_{OL}	Low-level output voltage	I_O = 4 mA		0.25	0.5	V

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

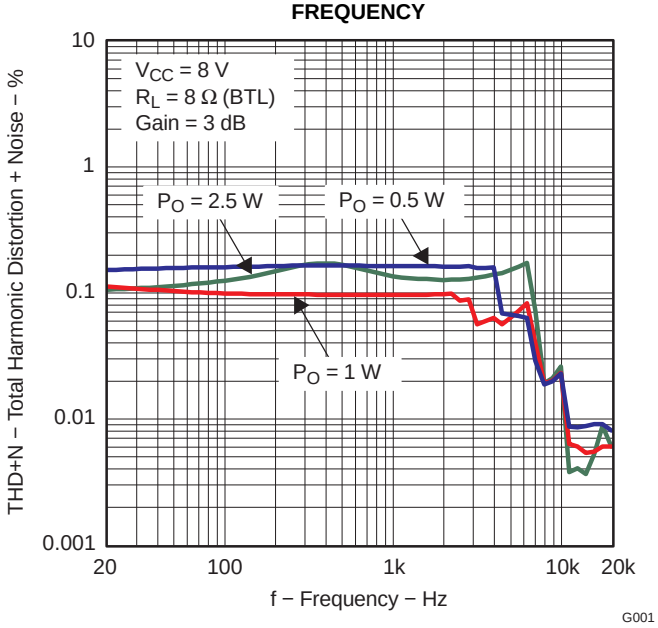


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

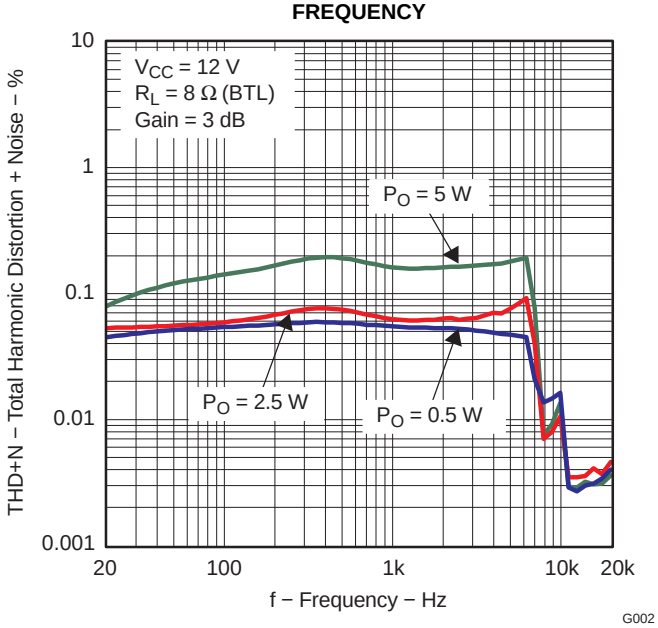


Figure 2.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

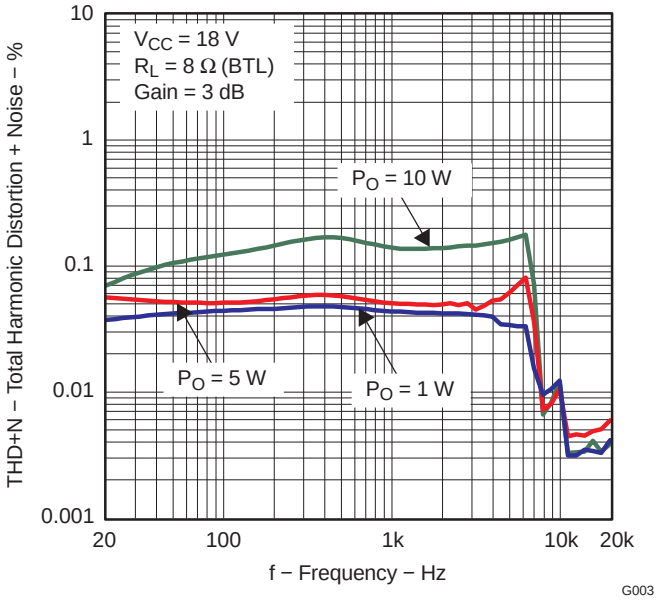


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

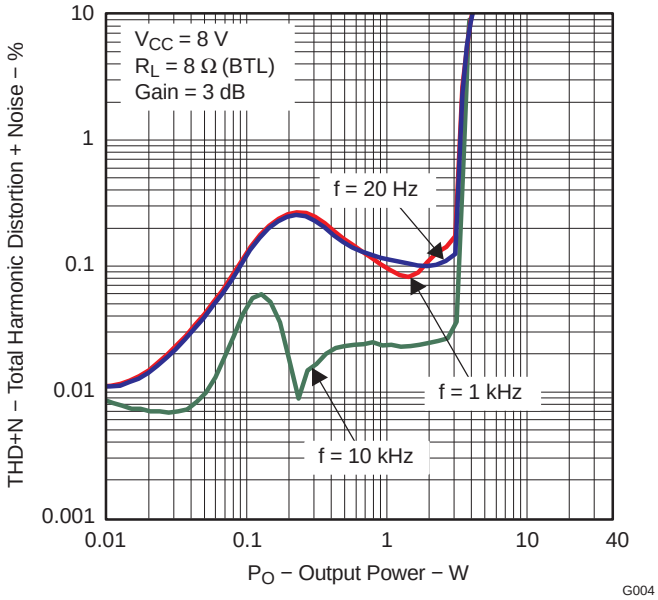


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

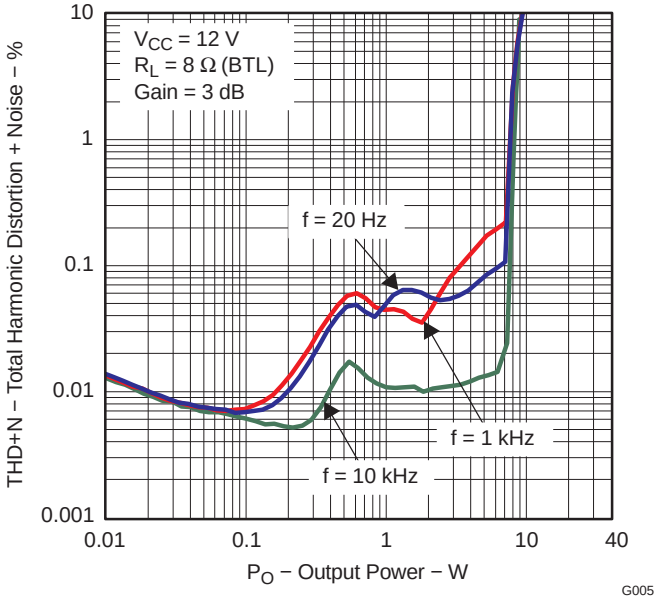


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

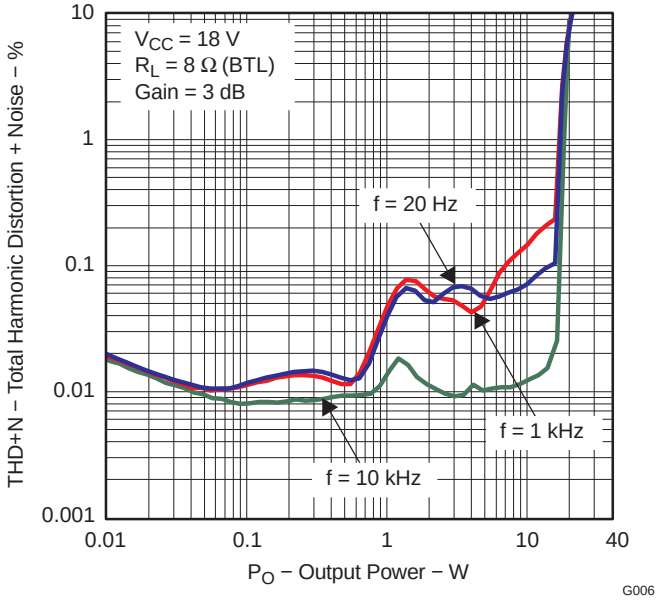


Figure 6.

TYPICAL CHARACTERISTICS (continued)

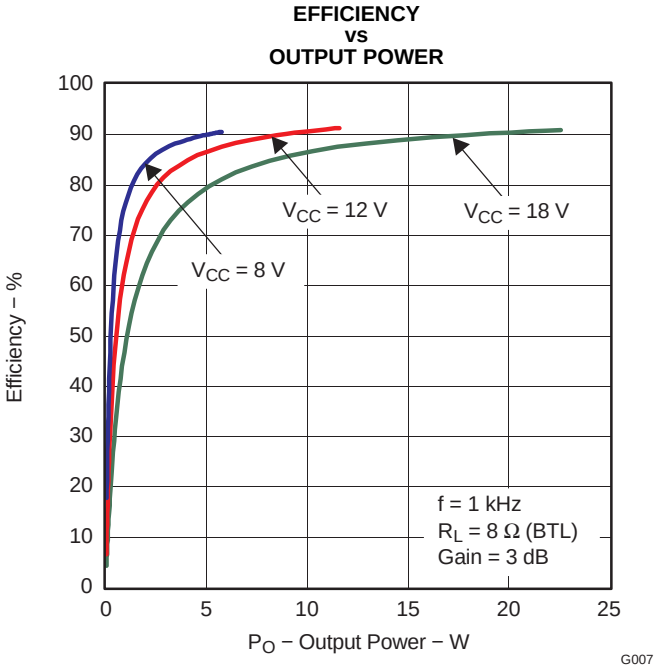


Figure 7.

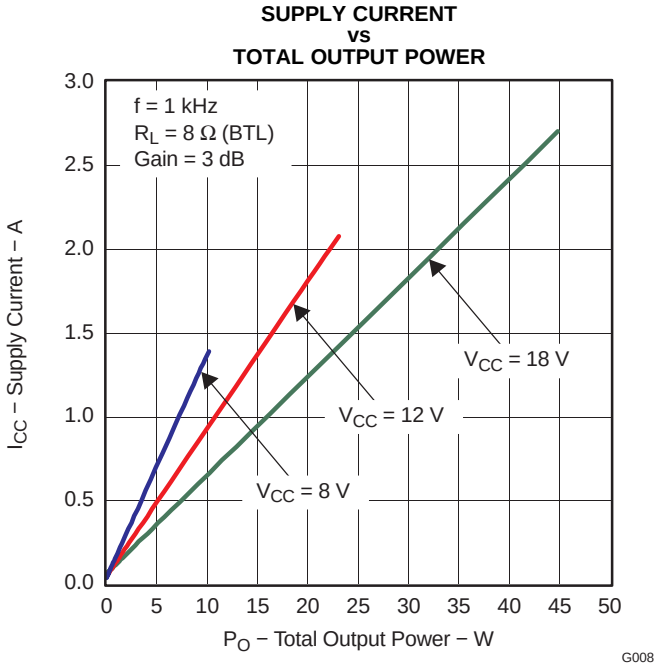


Figure 8.

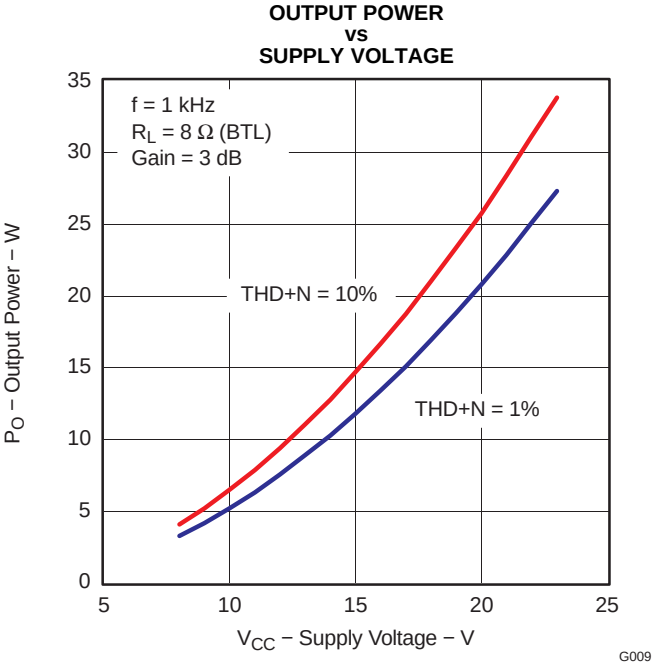


Figure 9.

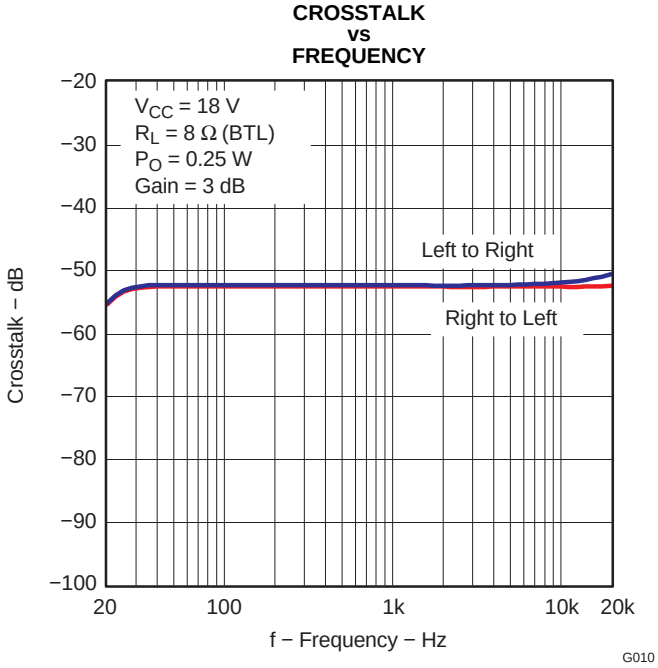


Figure 10.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

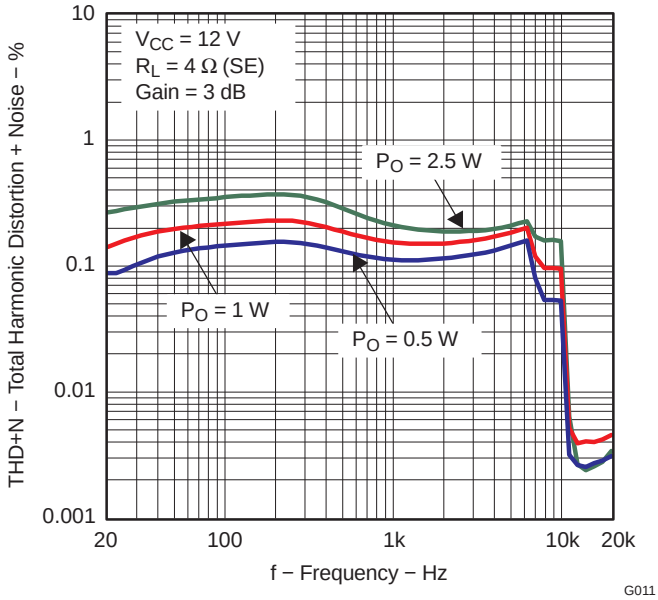


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

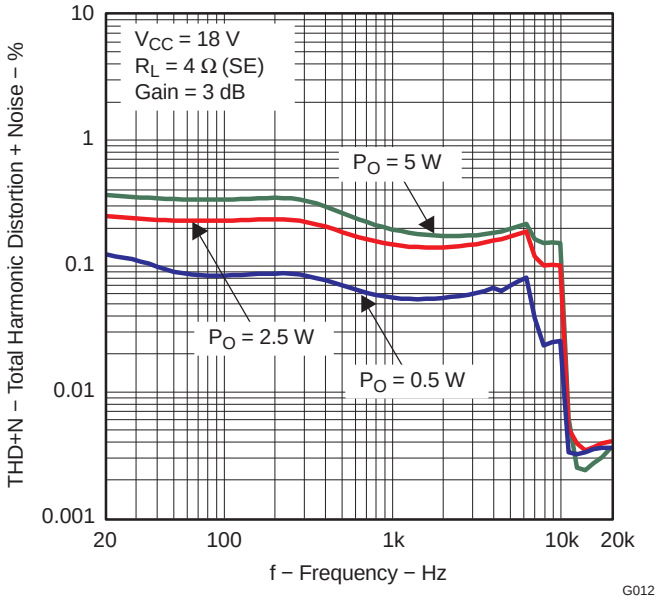


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

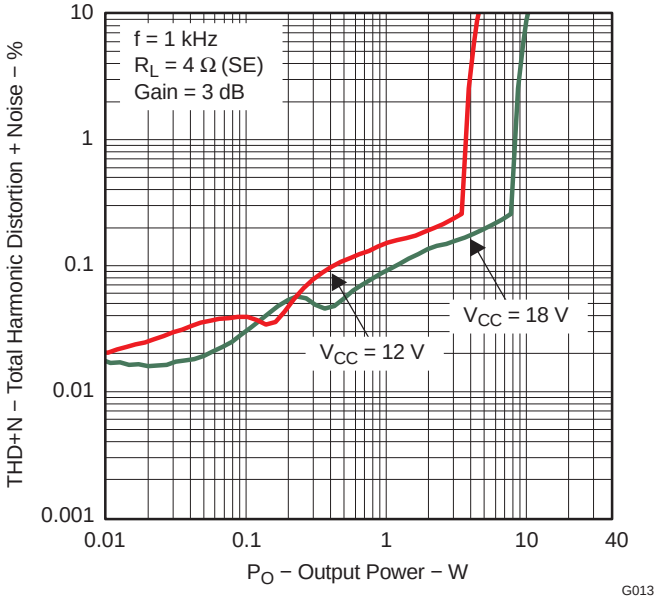


Figure 13.

OUTPUT POWER vs SUPPLY VOLTAGE

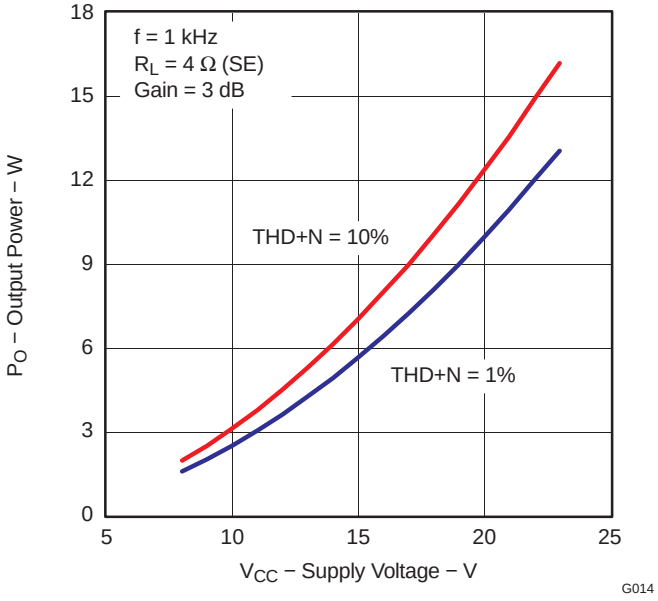


Figure 14.

TYPICAL CHARACTERISTICS (continued)

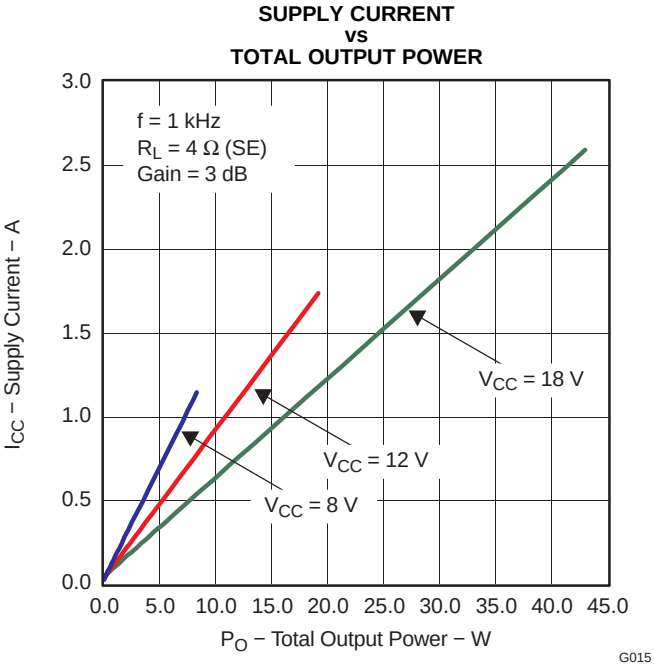


Figure 15.

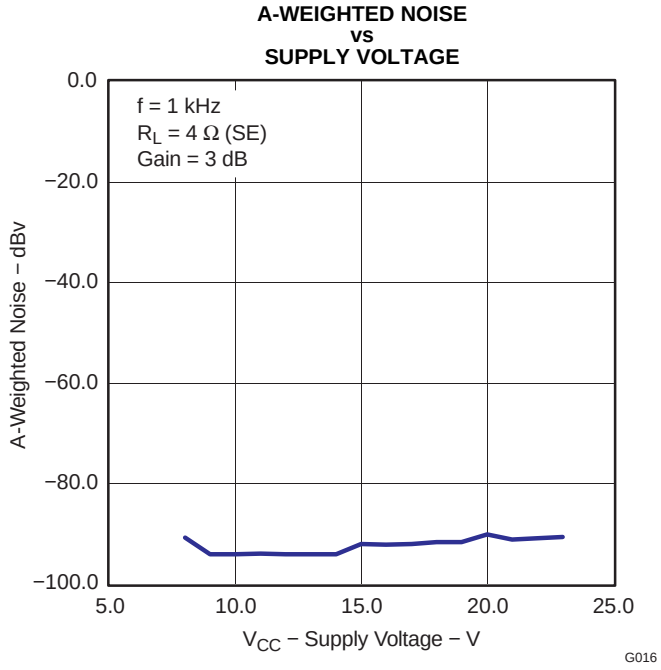


Figure 16.

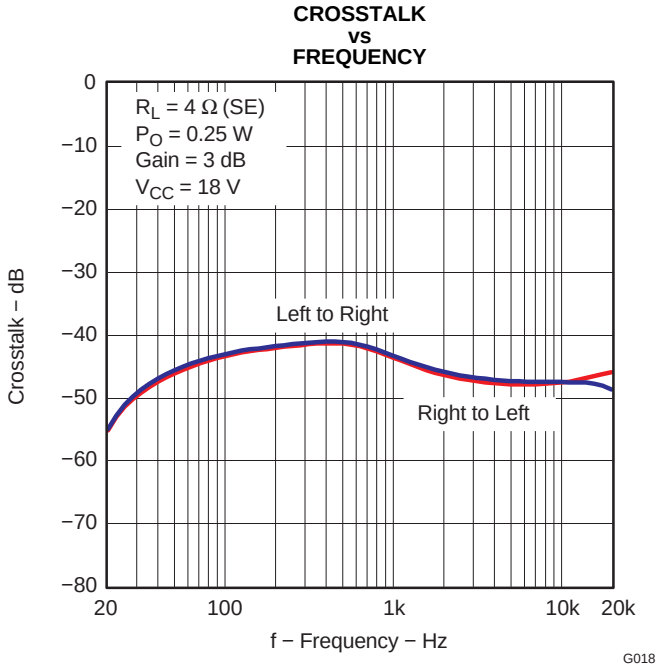


Figure 17.

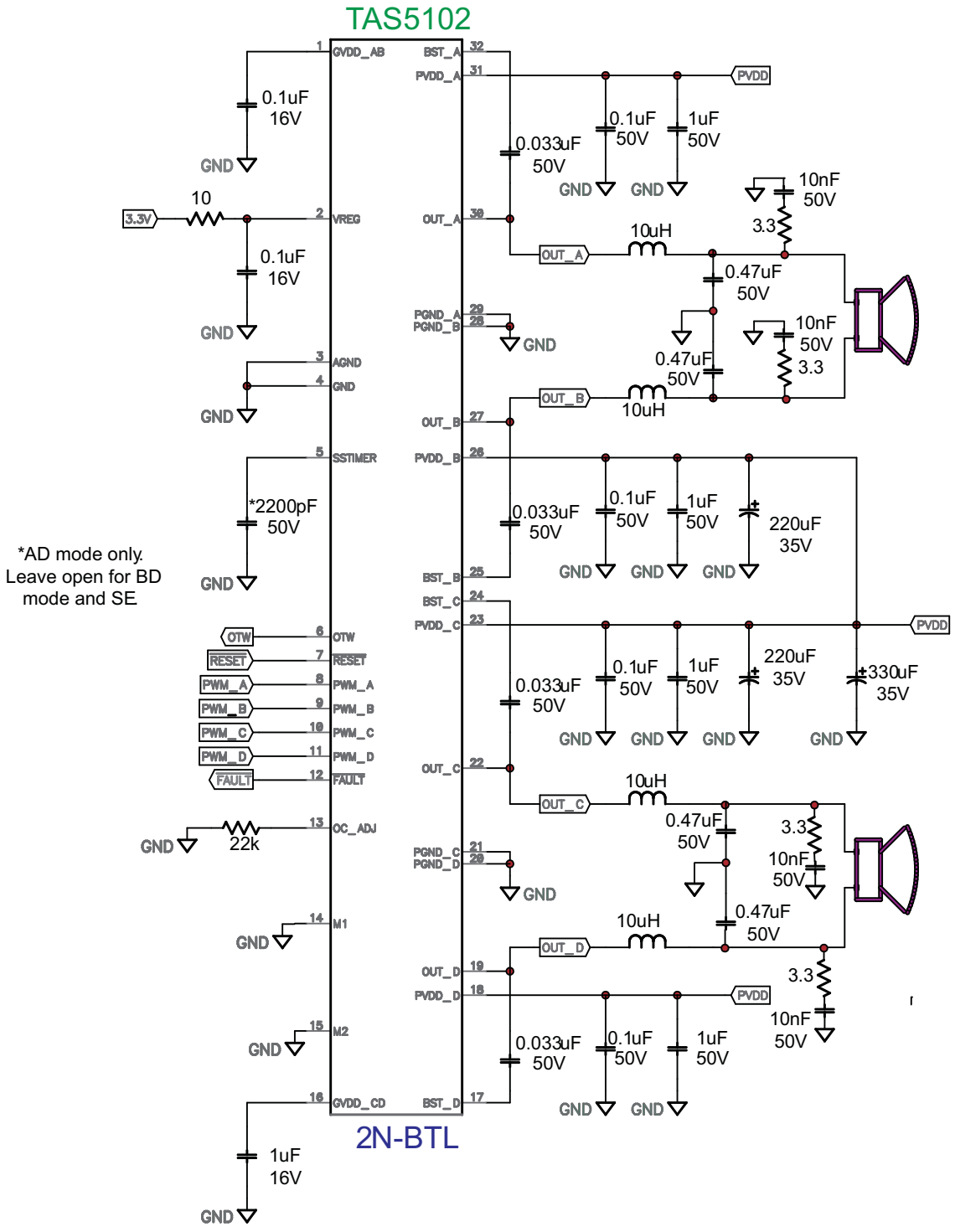


Figure 18. Typical Differential (2N) BTL Application With AD Modulation Filters

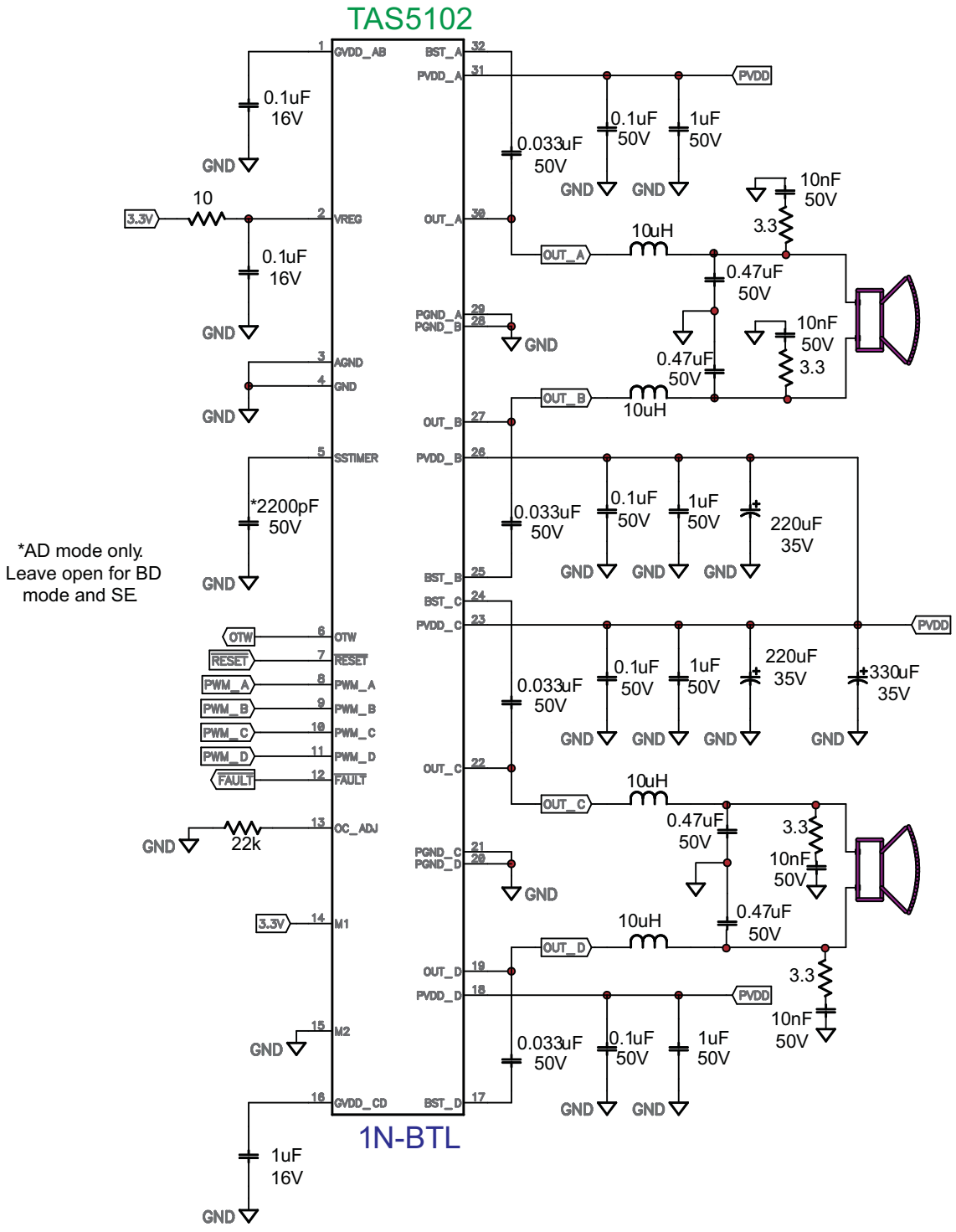


Figure 19. Typical Non-Differential (1N) BTL Application With AD Modulation Filters

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5102/3 needs only a 3.3-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). The gate drive voltages (GVDD_AB and GVDD_CD) are derived from the PVDD voltage. Separate, internal voltage regulators reduce and regulate the PVDD voltage to a voltage appropriate for efficient gave drive operation. Furthermore, an additional pin (VREG) is provided as supply for all common logic circuits. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5102/3 reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 3.3-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 18-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5102/3 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

INTEGRATED GATE DRIVE SUPPLY (GVDD)

The TAS5103 has an integrated gate drive supply, which eliminates the need for an external regulator. If the PVDD is 12 V (i.e., max PVDD < 13.2 V), it is possible to connect the PVDD to the GVDD through a ten ohm resistor. This will allow the power stage to operate as low a 7 V during dips. Otherwise the GVDD undervoltage protection will shutdown the outputs when the supply drops to 8 V. Care must be taken to not connect GVDD and PVDD together in this manner if the operating voltage is higher than 12 V.

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The outputs of the H-bridges remain in a high-impedance state until the internal gate-drive supply voltage (GVDD_XY) and external VREG voltages are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output. The output impedance is approximately 3KΩ under this condition, unless mode 1, 0 (Single-ended Mode), is used. This means that the TAS5102/3 should be held in reset for at least 200 μS to ensure that the bootstrap capacitors are charged. This also assumes that the recommended 0.033-μF bootstrap capacitors are used. Changes to bootstrap capacitor values will change the bootstrap capacitor charge time. To avoid *pops* and *clicks*, follow the recommended timing diagram in Figure 20.

When the TAS5102/3 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET}}$ is required, provided that the chipset is configured as recommended.

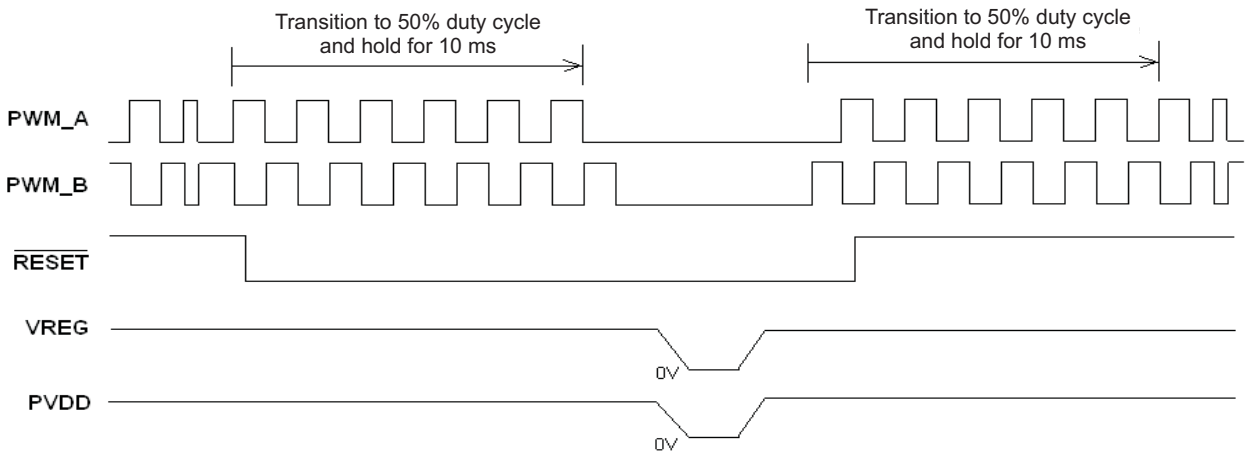


Figure 20. Power-Down/Power-Up Timing Diagram

Powering Down

The device remains fully operational as long as the gate-drive supply voltage and VREG voltages are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts, including *pops* or *clicks*. To avoid *pops* and *clicks*, follow the recommended timing diagram in Figure 20.

When the TAS5102/3 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET}}$ is required, provided that the chipset is configured as recommended.

ERROR REPORTING

The $\overline{\text{FAULT}}$ pin is an active-low, open-drain output. The OTW pin is a push-pull, active-high output. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, OTW goes high when the device junction temperature exceeds 125°C (see Table 1).

Table 1.

$\overline{\text{FAULT}}$	OTW	DESCRIPTION
0	0	Overcurrent (OC) or undervoltage (UVP) warning or overtemperature error (OTE)
0	1	Overtemperature warning (OTW) or overcurrent (OC) or undervoltage (UVP)

Table 1. (continued)

$\overline{\text{FAULT}}$	OTW	DESCRIPTION
1	0	Junction temperature lower than 125°C and no faults (normal operation)
1	1	Junction temperature higher than 125°C (overtemperature warning)

Note that asserting either $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device, resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on the $\overline{\text{FAULT}}$ output. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5102/3 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overtemperature, and undervoltage. The TAS5102/3 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overcurrent (OC) and overtemperature error (OTE), the device automatically recovers when the fault

condition has been removed. For highest possible reliability, recovering from an overcurrent fault requires external reset of the device (see the *Device Reset* section of this data sheet) no sooner than 300 ms after the shutdown.

Use of TAS5102/3 in High-Modulation-Index Capable Systems

This device requires at least 50 ns of low time on the output per 384-kHz PWM frame rate in order to keep the bootstrap capacitors charged. As an example, if the modulation index is set to 99.2% in the TAS5086, this setting allows PWM pulse durations down to 20 ns. This signal, which does not meet the 50-ns requirement, is sent to the PWM_X pin, and this low-state pulse time does not allow the bootstrap capacitor to stay charged. In this situation, the low voltage across the bootstrap capacitor can cause the bootstrap UVP circuitry to activate and shutdown the device. The TAS5102/3 device requires limiting the TAS5086 modulation index to 96.1% to keep the bootstrap capacitor charged under all signals and loads.

Therefore, TI strongly recommends using a TI PWM processor, such as TAS5508 or TAS5086, with the modulation index set at 96.1% to interface with TAS5102/3. This is done by writing 0x04 to the Modulation Limit Register (0x10) in the TAS5086 or 0x04 to the Modulation Limit Register (0x16) in the TAS5508.

Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current further increasing, i.e., it performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current condition situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are not independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

The overcurrent protection threshold is set by a resistor to ground from the OC_ADJ pin. A value of 22kΩ will result in an overcurrent threshold of 4.5 A.

Overtemperature Protection

The TAS5102/3 has a two-level temperature-protection system that asserts an active-high warning signal (OTW) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5102/3 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_XY and VREG supply voltages reach 5.7 V (typical) and 2.7 V, respectively. Although GVDD_XY and VREG are independently monitored, a supply voltage drop below the UVP threshold on VREG or either GVDD_XY pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

One reset pin is provided for control of half-bridges A/B/C/D. When $\overline{\text{RESET}}$ is asserted low, all four power-stage FETs in half-bridges A, B, C, and D are forced into a high-impedance (Hi-Z) state. Thus, the reset pin is well suited for hard-muting the power stage if needed.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

Asserting the reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, i.e., $\overline{\text{FAULT}}$ is forced high.

A rising-edge transition on the reset input allows the device to resume operation after an overcurrent fault.

SSTIMER FUNCTIONALITY

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when a transition occurs on the RESET pin. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near zero duty cycle to the duty cycle that is present on the inputs. This allows for a smooth transition with no audible *pop* or *click* noises when the RESET pin transitions from high-to-low or low-to-high.

For a high-to-low transition of the RESET pin (shutdown case), it is important for the modulator to remain switching for a period of at least 10 ms (if using a 2.2 nF capacitor). Larger capacitors will increase the start-up/shutdown time, while capacitors smaller than 2.2 nF will decrease the start-up/shutdown time. The inputs MUST remain switching on the shutdown transition to allow the outputs to slowly ramp down the duty cycle to near zero before completely shutting off. The SSTIMER pin should be left floating for BD modulation and also for SE (single-ended) mode.

THERMAL INFORMATION

The thermally augmented package provided with the TAS5102 is designed to be interfaced directly to a heatsink using a thermal interface compound (for example, Wakefield Engineering type 126 thermal grease.) The heatsink then absorbs heat from the IC and couples it to the local air. If the heatsink is carefully designed, this process can reach equilibrium and heat can be continually removed from the IC. Because of the efficiency of the TAS5102, heatsinks can be used which are much smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with roughly the following components: $R_{\theta JC}$ (the thermal resistance from junction to case, or in this instance the metal pad), thermal grease thermal resistance, and heatsink thermal resistance. $R_{\theta JC}$ has been provided in the Device Information section. The thermal grease thermal resistance can be calculated from the exposed pad area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch thick layer is about 0.054 °C-in^2/W. The approximate exposed pad area is 0.01164 in^2. Dividing the example thermal grease area resistance by the area of the pad gives the actual resistance through the thermal grease , 3.3 °C/W.

Heatsink thermal resistance is generally predicted by the heatsink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus for a single IC, the system $R_{\theta JA}$= $R_{\theta JC}$ + thermal grease resistance + heatsink resistance.

Thermal information for the TAS5103 Pad Down design can be found in TI document SLMA002B. PowerPAD Thermally Enhanced Package Application Report . Additional material regarding thermal metrics can be found in TI document SPRA953A, IC Package Thermal Metrics (Rev. A).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS5102DAD	ACTIVE	HTSSOP	DAD	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5102DADG4	ACTIVE	HTSSOP	DAD	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5102DADR	ACTIVE	HTSSOP	DAD	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5102DADRG4	ACTIVE	HTSSOP	DAD	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5103DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5103DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5103DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5103DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

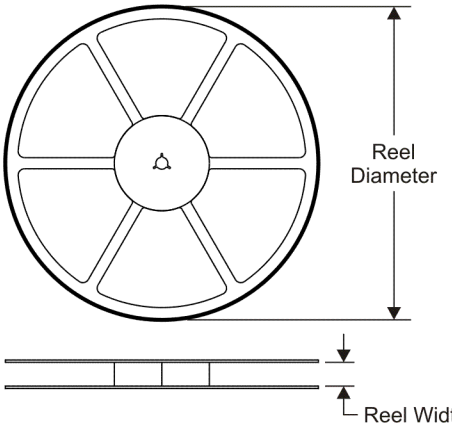
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

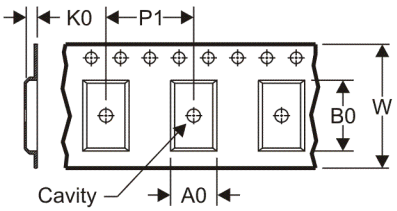
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

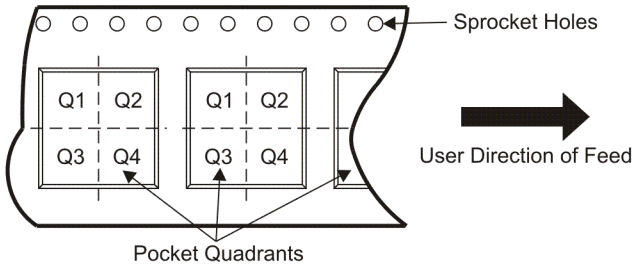


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

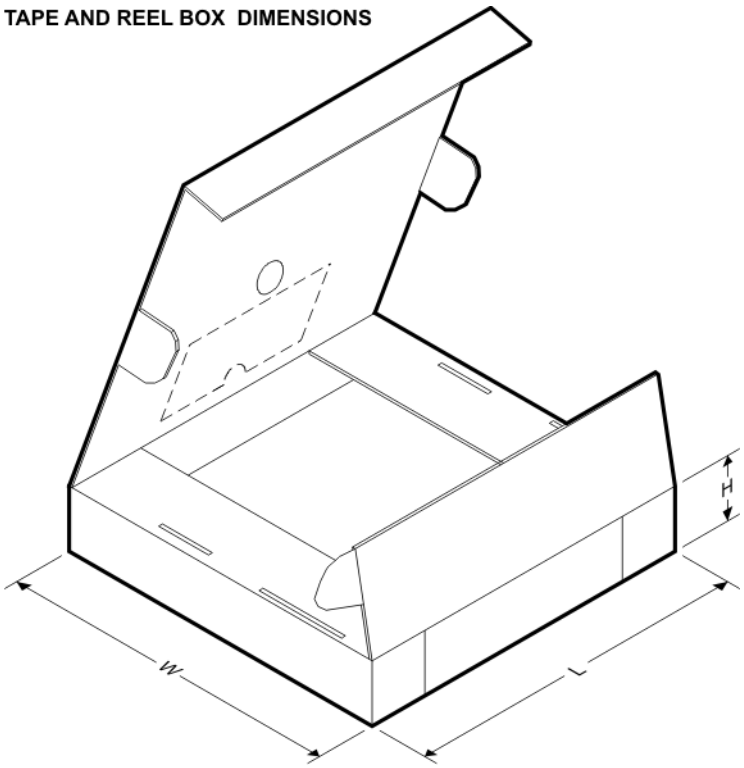
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5102DADR	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TAS5103DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

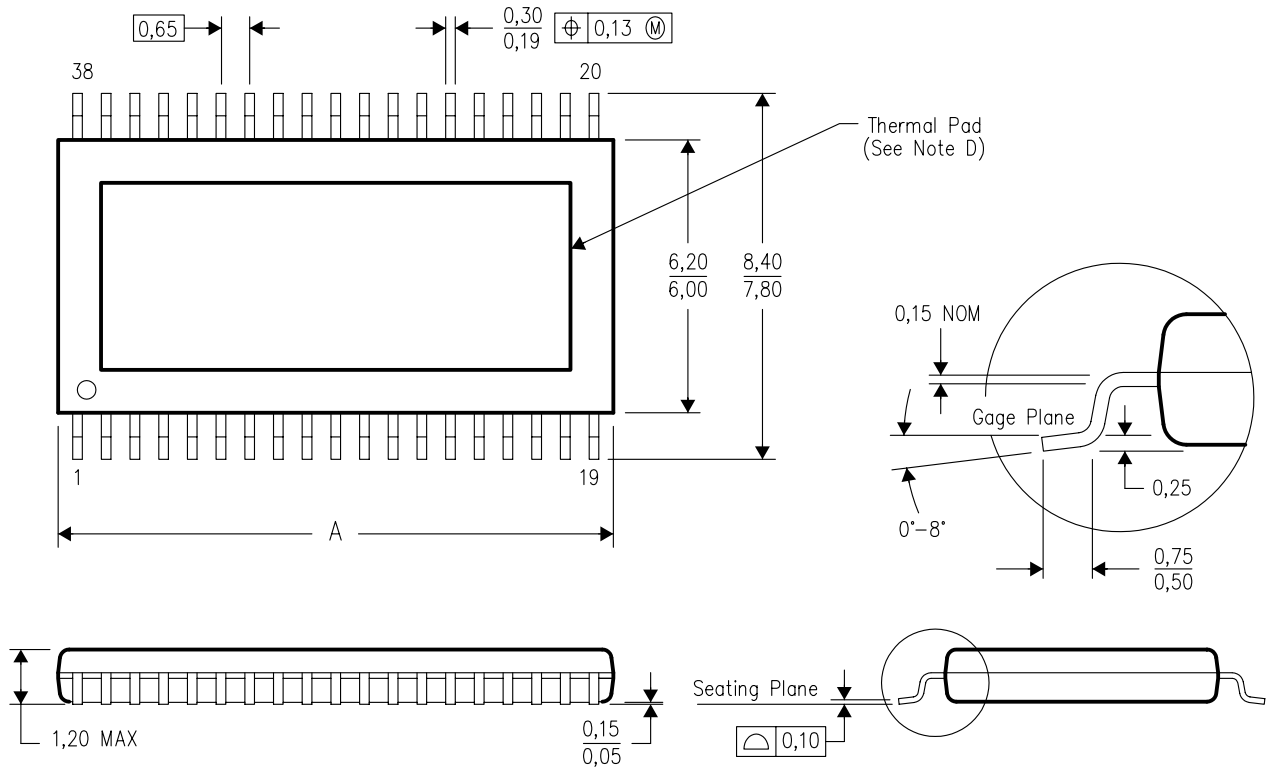


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5102DADR	HTSSOP	DAD	32	2000	346.0	346.0	41.0
TAS5103DAPR	HTSSOP	DAP	32	2000	346.0	346.0	41.0

DAD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE (DIE DOWN)

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4073258/D 11/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO–153

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