STWBC

Digital controller for wireless battery charger (WBC) transmitters Qi 1.1.2 A11 certified, PMA compatible

Datasheet - production data

VFQFPN32

Features

- Digital controller for wireless battery charger transmitter
- Multiple Qi certified and PMA standard compatible
- Support for up to 5 W applications
  - Mobile
  - Wearable, sports gear, medical
  - Remote controllers
- Native support to half-bridge and full bridge topologies
- 5 V supply voltage
- 2 firmware options
  - Turnkey solution for quick design
  - APIs available for application customization[a]
- Peripherals available via APIs[a]
  - ADC with 10 bit precision and 1 MΩ input impedance
  - UART
  - I^2C master fast/slow speed rate
  - GPIOs
- Memory
  - Flash and E^2PROM with read-while-write (RWW) and error correction code (ECC)
  - Program memory: 32 KBytes Flash; data retention 15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 KByte true data E^2PROM; data retention:15 years at 85 °C after 100 kcycles at 85 °C
  - RAM: 6 KBytes
- Reference design features
  - 2 layers PCBs
  - Active object detection
  - Graphical user interface for application monitoring
  - Evaluation boards
- Operating temperature: -40 °C up to 105 °C
- Package: VFQFPN32

Applications

- Certified Qi A11
  - Evaluation board: STEVAL-ISB027V1
  - Power rate: 5W
  - Input: 5V
- Qi A13[a]
  - Power rate: 5 W
  - Input: 5 - 16 V, 12 V
- Wearable[a]
  - Power rate: 2 W
  - Input: 5 V
- PMA[a]
  - power rate: 5 W
  - input: 5 V

a. Contact local sale representative for further details: see www.st.com.

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1 Description

The STWBC is the digital controller for wireless battery charger (WBC) transmitters (TX) from STMicroelectronics, offering the most flexible and efficient solution for controlling power transfer to a receiver (RX) in WBC-enabled applications such as phones, wearables, and other battery powered devices that use electromagnetic induction for recharging.

As a member of the Qi Wireless Power Consortium and the PMA (Power Matters Alliance), ST ensures full compatibility with these leading wireless charging protocols and holds certification for the Qi 1.1.2 A11 standard.

The STWBC performs all the functions for transmitter control: thanks to the internal 96 MHz clock and supporting both half-bridge and full bridge topologies, it is able to precisely control the amount of transmitted power to match the requirements of the receiving unit in terms of maximizing the efficiency of the power transfer.

The STWBC comes with firmware options to offer customers the ability to personalize their end product without the need of external microcontrollers:

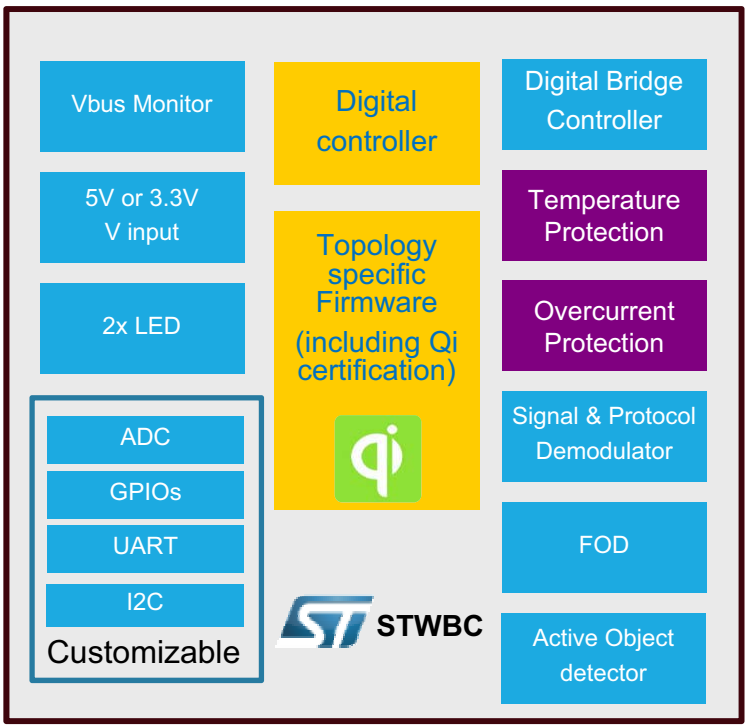
- A turnkey Qi 1.1.2 A11 certified solution, fully interoperable with Qi enabled mobile phones.
- API (application programming interface) access to customize the underlying firmware, for example modifying the behavior of the LEDs or GPIOs in response to the receiver behavior and supporting I²C and UART communication within a network.

The STWBC Qi 1.1.2 A11 certified solution is available in the STMicroelectronics STEVAL-ISB027V1 reference design, intended for all Qi compatible receivers such as in Qi enabled mobile phones.

In the reference design the STWBC integrates the foreign object detection (FOD): the digital feedback between TX and RX units allows the detection of metal objects close to the receiver that could result in potential hazards, enabling the STWBC to stop power transmission when such objects are detected.

The reference design is offered together with a complete ecosystem to support customers in building their applications, including the Qi 1.1.2 A11 certified board (STEVAL-ISB027V1), API libraries and documentation to develop software customizations, as well as a comprehensive graphical user interface to monitor real-time performance and diagnostics.

Figure 1. STWBC device architecture



2 Introduction to wireless battery charging systems

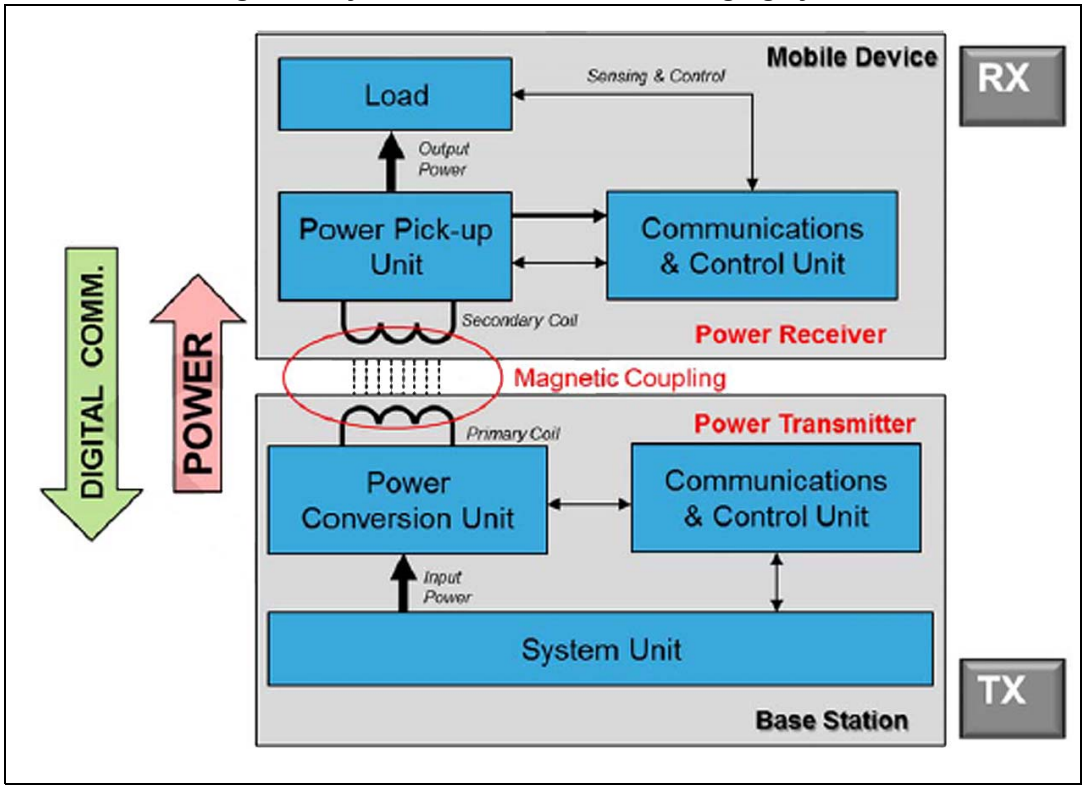
Wireless battery charging systems replace the traditional power supply cable by means of electromagnetic induction between a transmitting pad (TX) and a battery powered unit (RX), such as a mobile phone or a battery pack.

The power transmitter unit is responsible for controlling the transmitting coil and generating the correct amount of power requested by the receiver unit. The receiver unit continuously feedbacks to the transmitter the correct power level requested by modulating the transmitter carrier by means of a controlled resistive of capacitive insertion. Generating the correct amount of power guarantees the highest level of end-to-end efficiency due to reduced energy waste. Also, it helps maintaining a lower operational temperature.

The digital feedback is also used to detect foreign objects, i.e.: metal incorrectly exposed to the coils. By stopping the application as soon as a foreign object is detected the risk of damage is reduced.

Digital wireless battery transmitters can adapt the amount of energy transferred by the coil by modulating the frequency, duty cycles or coil input voltage.

Figure 2. System view of a wireless charging system



Thanks to the internal STWBC 96 MHz clock, support for half-bridge and full bridge topologies and protocol detection units, the STWBC can drive the power emitted by a transmitting coil. The STWBC firmware sits on the top of the hardware to monitor and control the correct wireless charging operations.

3 Certified Qi A11 solution

The STWBC has been certified for Qi A11, thanks to the STEVAL-ISB027V1 reference design. The certification is based on the Qi standard version 1.1.2 and supports FOD (“Foreign Object Detection”).

The STEVAL-ISB027V1 reference design provides a complete kit which includes the STWBC IC, firmware, layout, graphical interfaces and tools. The layout is based on a cost-effective 2-layer PCB.

Firmware

The STWBC firmware is available in two separate software packages:

- Turn-key: the firmware is distributed as a binary file.
- API customizable: the firmware is designed as a library and external functions as well as peripherals can be added by means of APIs.

The software APIs allow a great freedom of application customization. The STWBC and the API library can be accessed by programming the internal controller via standard programming tools such as the IAR™ Workbench® Studio.

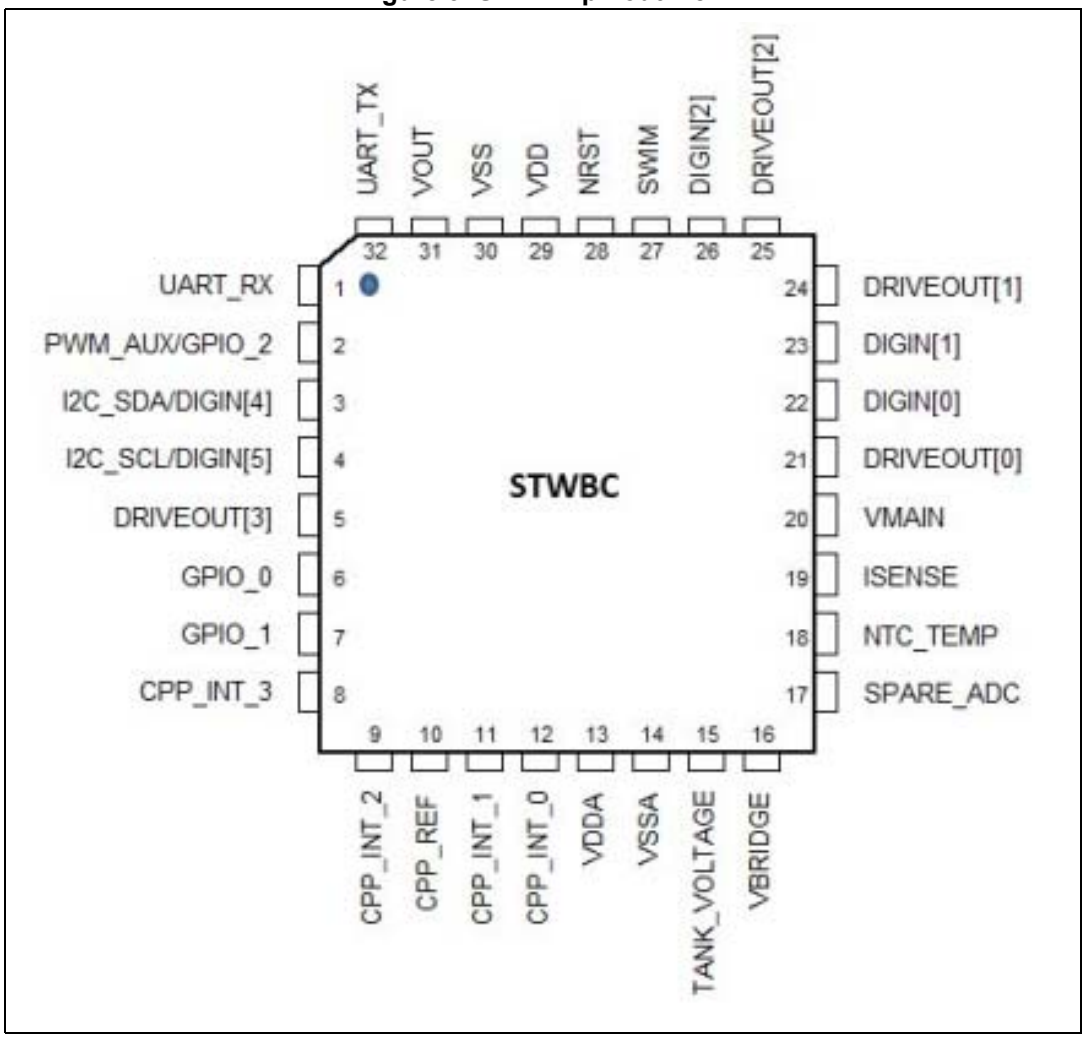
Every STWBC wireless charging architecture is a reference design supported by firmware, evaluation boards, application notes and PCB layouts notes.

4 Pinout and pin description

The STWBC is a multifunction device that can support several wireless charging architectures. The pinout is therefore application specific. *Section 4.1* shows the pinout used by the STWBC when the Qi A11 configuration is used.

4.1 Pinout for STWBC in Qi A11 configuration

Figure 3. STWBC pinout view



4.2 Pin description

Table 1. Pinout description

Pin no.	Pin name	Pin type	API firmware description	Bin firmware description
1	UART_RX(1)	DI	UART RX link	UART RX link
2	PWM_AUX/GPIO_2(1)	DO	PWM output or GPO	Not used, must not be connected to any potential
3	I2C_SDA/DIGIN [4](1)		I2C_SDA / digital input 4	inactive (internal pull-up)
4	I2C_SCL/DIGIN [5](1)		I2C_SCL / digital input 5	inactive (internal pull-up)
5	DRIVEOUT [3]	DO	Output driver for low-side branch right	Output driver for low-side branch right
6	GPIO_0(1)	DO	Digital output for the green light indicator / general purpose I/O	Digital output for the green light indicator
7	GPIO_1(1)	DO	Digital output for the red light indicator / general purpose I/O	Digital output for the red light indicator
8	CPP_INT_3	AI	Symbol detector	Symbol detector
9	CPP_INT_2	AI	Vmain monitor	Vmain monitor
10	CPP_REF	AI	External reference for CPP_INT_3 (if not used, must be tied to GND)	External reference for CPP_INT_3 (if not used, must be tied to GND)
11	CPP_INT_1	AI	Symbol detector	Symbol detector
12	CPP_INT_0	AI	Symbol detector	Symbol detector
13	VDDA	PS	Analog power supply	Analog power supply
14	VSSA	PS	Analog ground	Analog ground
15	TANK_VOLTAGE	AI	LC tank voltage probe	LC tank voltage probe
16	VBRIDGE		Inactive (to be tied to GND)	Inactive (to be tied to GND)
17	SPARE_ADC(1)		Spare analog input (to be tied to GND if not used)	Spare analog input (to be tied to GND)
18	NTC_TEMP	AI	NTC temperature measurement.	NTC temperature measurement.
19	ISENSE	AI	LC tank current measurement	LC tank current measurement
20	VMAIN	AI	Vmain monitor	Vmain monitor
21	DRIVEOUT [0]	DO	Output driver for low-side branch left	Output driver for low-side branch left
22	DIGIN [0](1)		Digital input 0	Inactive (internal pull-up)
23	DIGIN [1](1)		Digital input 1	Inactive (internal pull-up)
24	DRIVEOUT [1]	DO	Output driver for high-side branch left	Output driver for high-side branch left
25	DRIVEOUT [2]	DO	Output driver for high-side branch right	Output driver for high-side branch right
26	DIGIN [2](1)		Digital input 2	Inactive (internal pull-up)
27	SWIM	DIO	Debug interface	Debug interface

Table 1. Pinout description (continued)

Pin no.	Pin name	Pin type	API firmware description	Bin firmware description
28	NRST	DI	Reset	Reset
29	VDD	PS	Digital and I/O power supply	Digital and I/O power supply
30	VSS	PS	Digital and I/O ground	Digital and I/O ground
31	VOUT	Supply	Internal LDO output	Internal LDO output
32	UART_TX(1)	DO	UART TX link	UART TX link

1. API configurable.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}. V_{DDA} and V_{DD} must be connected to the same voltage value. V_{SS} and V_{SSA} must be connected together with the shortest wire loop.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in *Table 2*, *Table 3* and from *Table 5 on page 17* to *Table 17 on page 29* footnotes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

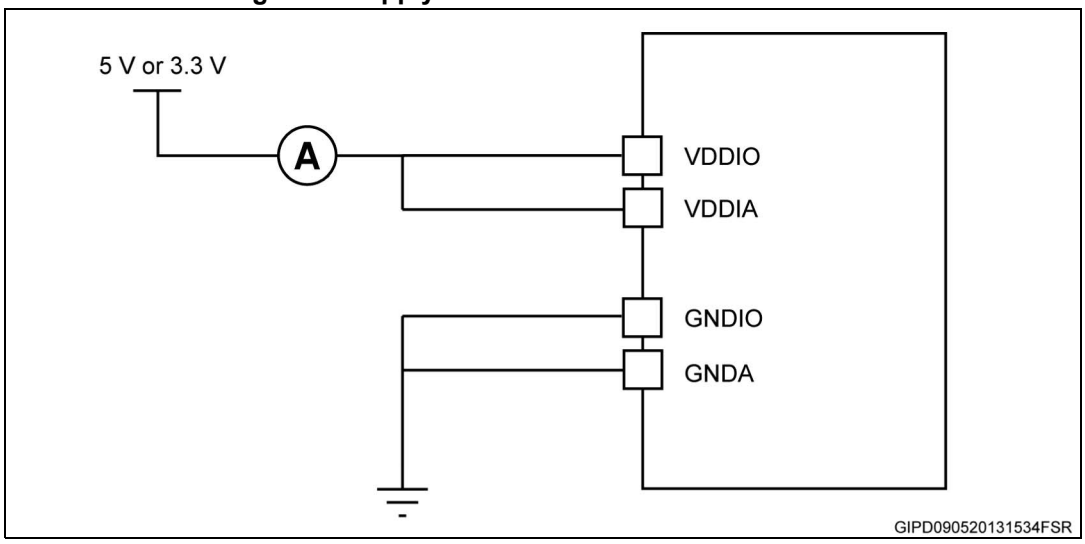
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

5.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected together as shown in *Figure 4*.

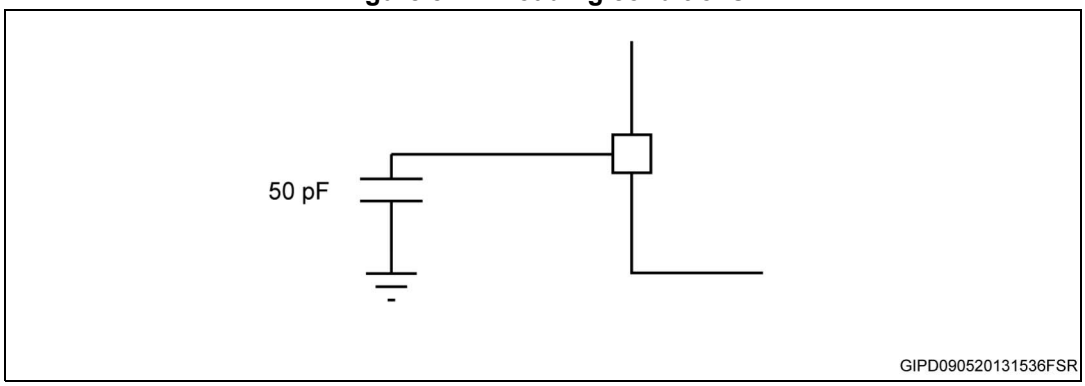
Figure 4. Supply current measurement conditions



5.1.5 Loading capacitors

The loading conditions used for the pin parameter measurement are shown in *Figure 5*:

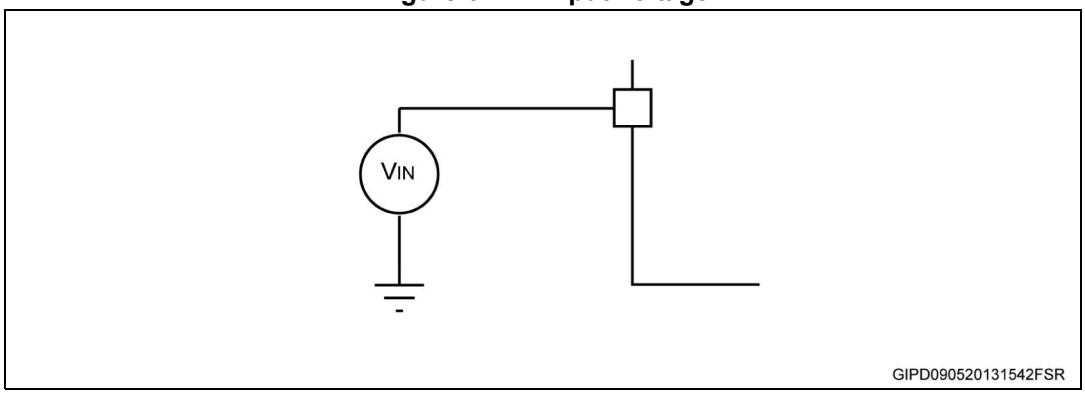
Figure 5. Pin loading conditions



5.1.6 Pin output voltage

The input voltage measurement on a pin is described in *Figure 6*.

Figure 6. Pin input voltage



5.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 2. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on any other pin(2)	VSS -0.3	VDD +0.3	
V_{DD} - V_{DDA}	Variation between different power pins		50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins(3)		50	
V_{ESD}	Electrostatic discharge voltage	Refer to absolute maximum ratings (electrical sensitivity) in *Section 5.4.1 on page 31*.		

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 3. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDDX}	Total current into VDDX power lines(2)	100	mA
I_{VSSX}	Total current out of VSSX power lines(2)	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to *Table 11 on page 21*	
	Output current source by any I/Os and control pin		
$I_{INJ(PIN)}$(3), (4)	Injected current on any pin	±4	
$I_{INJ(TOT)}$(3), (4), (5)	Sum of injected currents	±20	

1. Data based on characterization results, not tested in production
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $\Sigma_{IINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma_{IINJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 4. Thermal characteristics

Symbol	Ratings	Max.	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

5.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 5*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 5. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}, V_{DDA1}	Operating voltages		3(1)		5.5(1)	V
V_{DD}, V_{DDA}	Nominal operating voltages		3.3(1)		5(1)	
V_{OUT}	Core digital power supply			1.8(2)		
	C_{VOUT}: capacitance of external capacitor(3)	at 1 MHz	470		3300	nF
	ESR of external capacitor(2)		0.05		0.2	Ω
	ESL of external capacitor(2)					
Θ_{JA}(4)	FR4 multilayer PCB	VFQFPN32		26		°C/W
T_A	Ambient temperature	Pd = 100 mW	-40		105	°C

1. The external power supply can be within range from 3 V up to 5.5 V.
2. Internal core power supply voltage.
3. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
4. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 6. Operating conditions at power-up/power-down

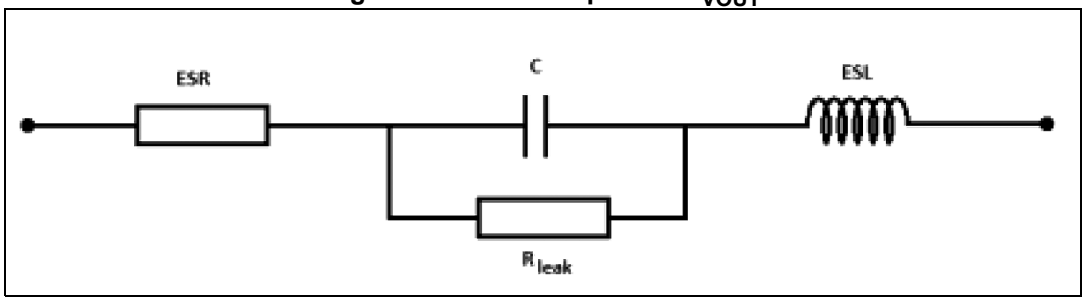
Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(2)	Unit
t_{TEMP}	Reset release delay	V_{DD} rising		3		ms
V_{IT}+	Power-on reset threshold		2.65	2.8	2.98	V
V_{IT}-	Brownout reset threshold		2.58	2.73	2.88	

1. Guaranteed by design, not tested in production.
2. Power supply ramp must be monotone.

5.3.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VOUT}[(b)] to the VOUT pin. The C_{VOUT} is specified in *Section 5.3: Operating conditions*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 7. External capacitor C_{VOUT}



5.3.2 Internal clock sources and timing characteristics

HSI RC oscillator

The HSI RC oscillator parameters are specified under general operating conditions for V_{DD} and T_A.

Table 7. HSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)(1), (2)	V_{DD} = 3.3 V T_A= 25 °C	-1%		+1%	%
		V_{DD} = 3.3 V -40 °C ≤ T_A ≤ 105 °C	-4%		+4%	
		V_{DD} = 5 V -40 °C ≤ T_A ≤ 105 °C	-4%		+4%	
$t_{SU(HSI)}$	HSI oscillator wakeup time including calibration			1		µs

1. Data based on characterization results, not tested in production.
2. Variation referred to f_{HSI} nominal value.

b. ESR is the equivalent series resistance and ESL is the equivalent inductance.

LSI RC oscillator

The LSI RC oscillator parameters are specified under general operating conditions for V_{DD} and T_A.

Table 8. LSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{LSI}	Frequency			153.6		kHz
ACC_{LSI}	Accuracy of LSI oscillator	3.3 V ≤ V_{DD} ≤ 5 V -40 °C ≤ T_A ≤ 105 °C	-10%		10%	%
$t_{SU(LSI)}$	LSI oscillator wakeup time			7		µs

1. Guaranteed by design, not tested in production.

PLL internal source clock

Table 9. PLL internal source clock

Symbol	Parameter	Conditions	Min	Typ.	Max.(1)	Unit
f_{IN}	Input frequency(2)	3.3 V ≤ V_{DD} ≤ 5 V -40 °C ≤ T_A ≤ 105 °C		16		MHz
f_{OUT}	Output frequency			96		
t_{lock}	PLL lock time				200	µs

1. Data based on characterization results, not tested in production.
2. PLL maximum input frequency 16 MHz.

5.3.3 Memory characteristics

Flash program and memory/data E^{2}PROM memory

General conditions: T_A = -40 °C to 105 °C.

Table 10. Flash program memory/data E^{2}PROM memory

Symbol	Parameter	Conditions	Min.(1)	Typ.(1)	Max.(1)	Unit
t_{PROG}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	
t_{ERASE}	Erase time for 1 block (128 bytes)			3	3.3	ms
N_{WE}	Erase/write cycles((2)(program memory)	T_A = 25 °C	10 K			Cycles
	Erase/write cycles(2)(data memory)	T_A = 85 °C	100 K			
		T_A = 105 °C	35 K			
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 85 °C	15			Years
	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 105 °C	11			
	Data retention (data memory) after 100 K erase/write cycles at T_A= 85 °C	T_{RET} = 85 °C	15			
	Data retention (data memory) after 35 K erase/write cycles at T_A= 105 °C	T_{RET} = 105 °C	6			
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC		2		mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

5.3.4 I/O port pin characteristics

The I/O port pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 11. Voltage DC characteristics

Symbol	Description	Min.(1)	Typ.	Max.(1)	Unit
V_{IL}	Input low voltage	-0.3		0.3 * V_{DD}	V
V_{IH}	Input high voltage(2)	0.7 * V_{DD}		V_{DD}	
V_{OL1}	Output low voltage at 3.3 V(3)			0.4(4)	
V_{OL2}	Output low voltage at 5 V(3)			0.5	
V_{OL3}	Output low voltage high sink at 3.3 V / 5 V(2),(5), (6)		0.6(4)		
V_{OH1}	Output high voltage at 3.3 V(3)	V_{DD} - 0.4(4)			
V_{OH2}	Output high voltage at 5 V(3)	V_{DD} - 0.5			
V_{OH3}	Output high voltage high sink at 3.3 V / 5 V(2), (5), (6)	V_{DD} - 0.6(4)			
H_{VS}	Hysteresis input voltage(7)	0.1 * V_{DD}			
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.
2. All signals are not 5 V tolerant (input signals can't be exceeded V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).
3. Parameter applicable to signals: GPIO_[0:2], DRIVEOUT[0:3], PWM_AUX.
4. Electrical threshold voltage not yet characterized at -40 ºC.
5. Parameter applicable to signal: SWIM.
6. Parameter applicable to signal: DIGIN [0].
7. Applicable to any digital inputs.

Table 12. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.(1)	Unit
I_{OL1}	Standard output low level current at 3.3 V and V_{OL1}(2)			1.5	mA
I_{OL2}	Standard output low level current at 5 V and $V_{OL\ 2}$(2)			3	
I_{OLhs1}	High sink output low level current at 3.3 V and V_{OL3} (3),(4)			5	
I_{OLhs2}	High sink output low level current at 5 V and V_{OL}(3),(4)			7.75	
I_{OH1}	Standard output high level current at 3.3 V and V_{OH1}(2)			1.5	
I_{OH2}	Standard output high level current at 5 V and V_{OLH2}(2)			3	
I_{OHhs1}	High sink output low level current at 3.3 V and V_{OH3}(3), (4)			5	
I_{OHhs2}	High sink output low level current at 5 V and V_{OH3}(3), (4)			7.75	
I_{LKg}	Input leakage current digital - analog $V_{SS} \leq V_{IN} \geq V_{DD}$(5)			± 1	µA
I_{Inj}	Injection current(6), (7)			±4	mA
ΣI_{Inj}	Total injection current (sum of all I/O and control pins)(6)			± 20	

1. Data based on characterization result, not tested in production.
2. Parameter applicable to signals: GPIO_[0:2], DRIVEOUT[0:3], PWM_AUX.
3. Parameter applicable to signal: SWIM.
4. Parameter applicable to signal: DIGIN [0].
5. Applicable to any digital inputs.
6. Maximum value must never be exceeded.
7. Negative injection current on the ADCIN [7:0] signals (product depending) => SPARE_ADC signals have to avoid since impact the ADC conversion accuracy.

5.3.5 Typical output level curves

This section shows the typical output voltage level curves measured on a single output pin for the two-pad family present in the STWBC device.

Standard pad

This pad is associated to the following signals: DIGIN [0:1], SWIM and GPIO_[0:2] when available.

Figure 8. V_{OH} standard pad at 3.3 V

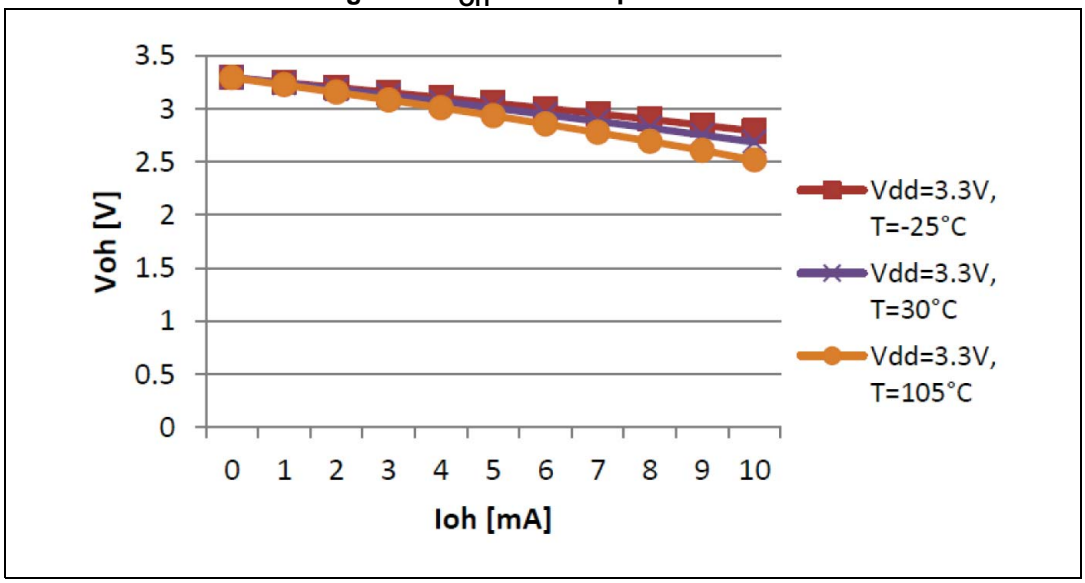


Figure 9. V_{OL} standard pad at 3.3 V

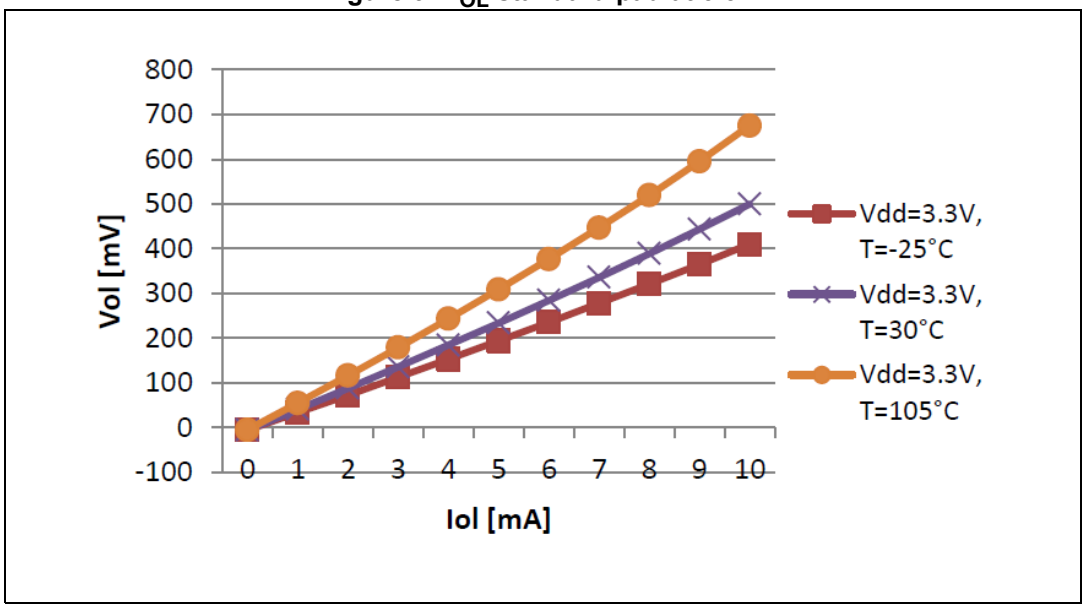


Figure 10. V_{OH} standard pad at 5 V

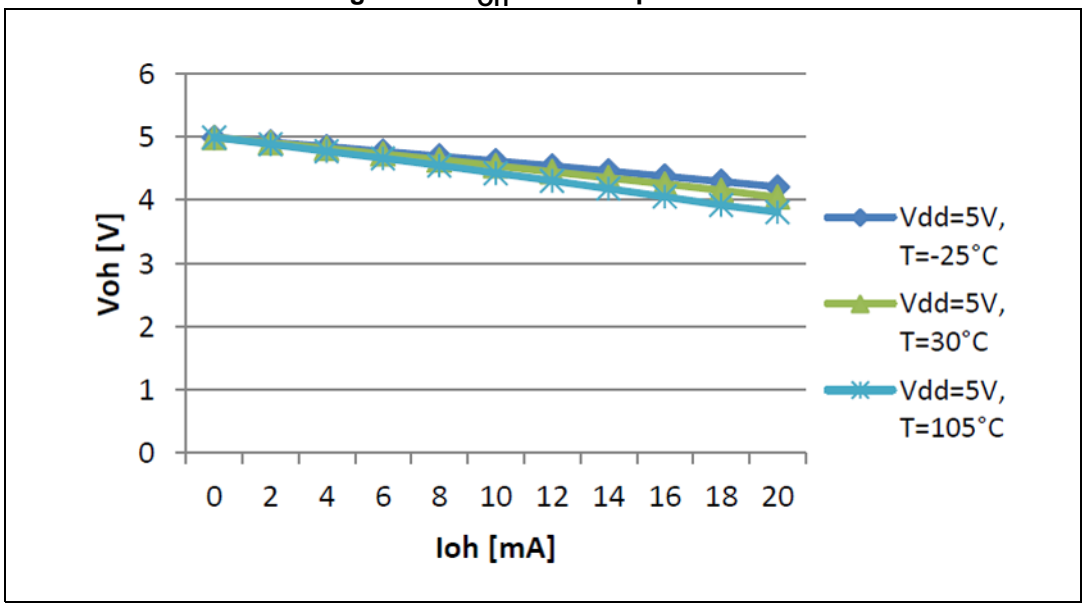
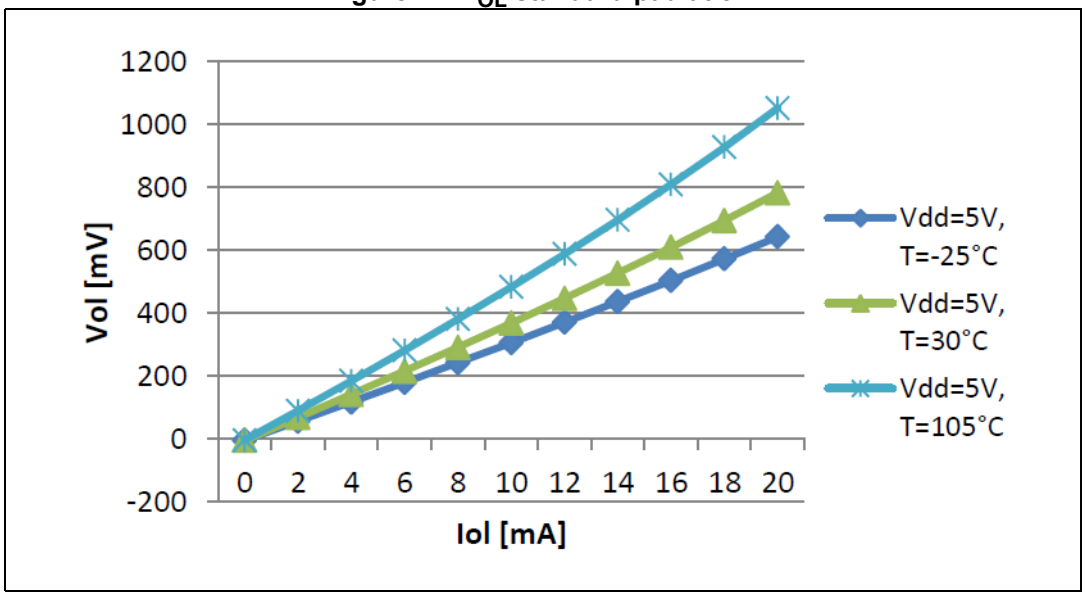


Figure 11. V_{OL} standard pad at 5 V



5.3.6 Fast pad

This pad is associated to the DRIVEOUT[0:3], PWM_AUX signals if the external pin is available.

Figure 12. V_{OH} fast pad at 3.3 V

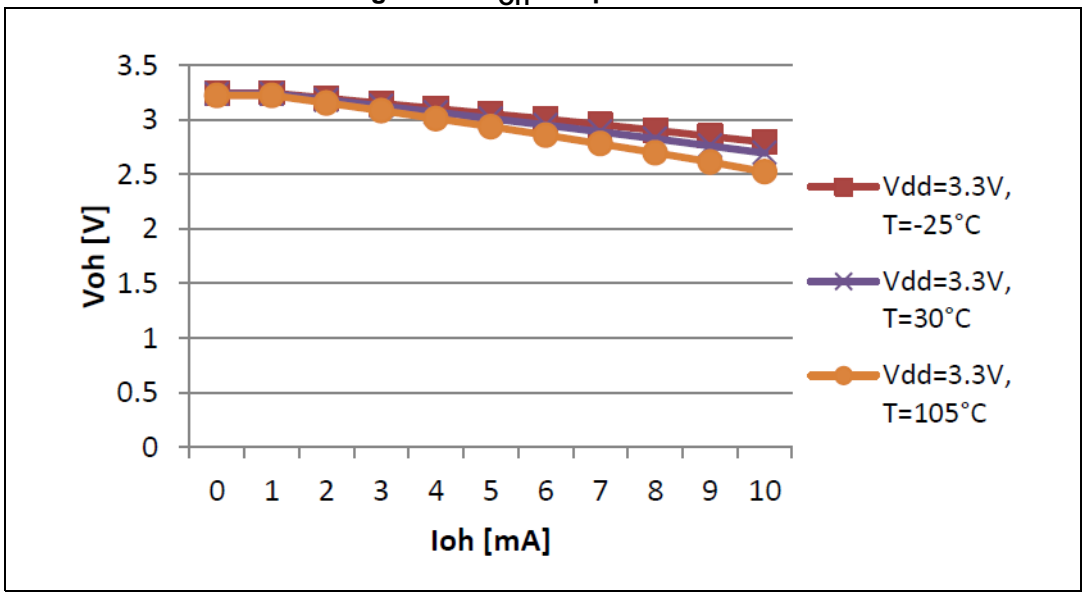


Figure 13. V_{OL} fast pad at 3.3 V

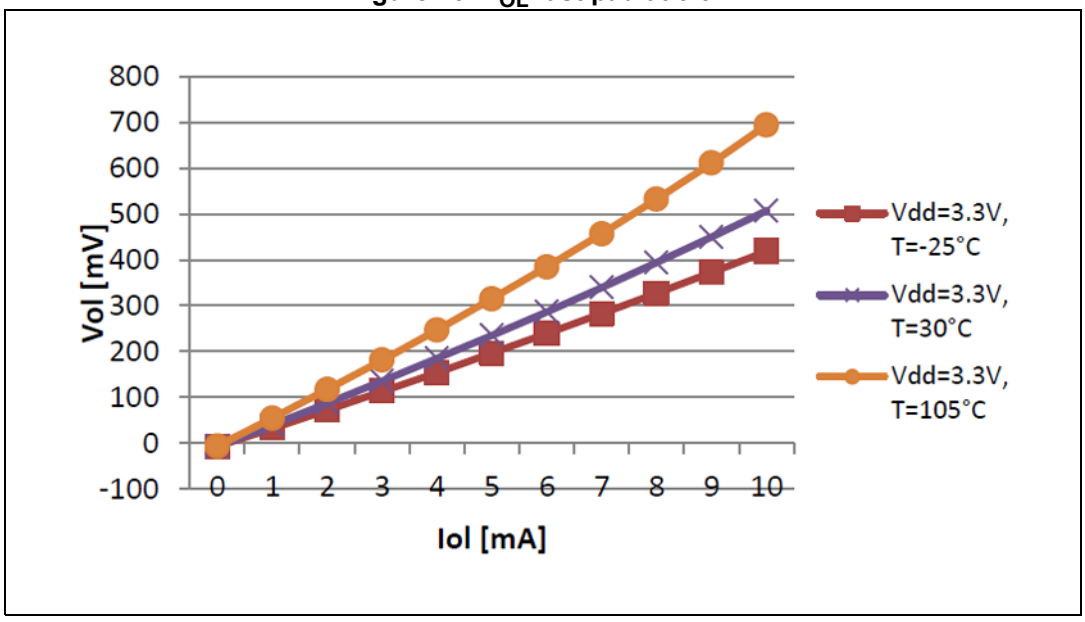


Figure 14. V_{OH} fast pad at 5 V

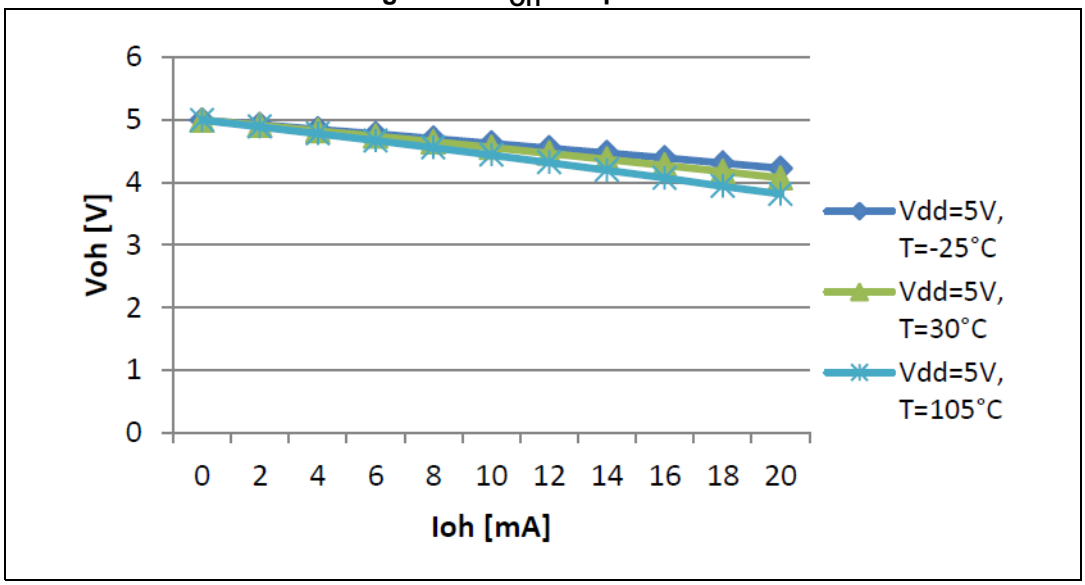
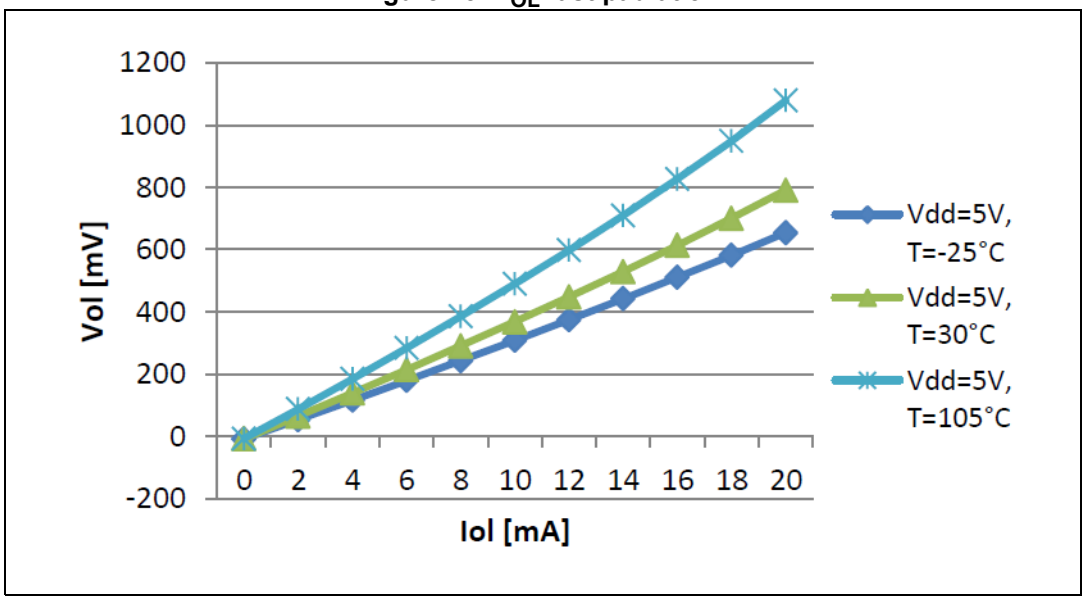


Figure 15. V_{OL} fast pad at 5 V



5.3.7 Reset pin characteristics

The reset pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 13. NRST pin characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)		-0.3		0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)		0.7 x V_{DD}		V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL} = 2 mA			0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)		30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)				75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse(3)		500			
$t_{OP(NRST)}$	NRST output filtered pulse(3)		15			µs

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

5.3.8 I^2C interface characteristics

Table 14. I^2C interface characteristics

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.(1)	Max.(1)	Min.(1)	Max.(1)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(2)		0(2)	900(2)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (VDD = 3.3 to 5 V)(3)		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (VDD = 3.3 to 5 V)(3)		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line(4)		50		50	pF

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
3. I^2C multifunction signals require the high sink pad configuration and the interconnection of 1 K pull-up resistances.
4. 50 pF is the maximum load capacitance value to meet the I^2C std timing specifications.

5.3.9 10-bit SAR ADC characteristics

The 10-bit SAR ADC oscillator parameters are specified under general operating conditions for V_{DDA} and T_A unless otherwise specified.

Table 15. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N	Resolution			10		bit
R_{ADCIN}	ADC input impedance		1			MΩ
V_{IN1}	Conversion voltage range for gain x1		0		1.25(1), (2)	
V_{ref}	ADC main reference voltage(3)			1.250		V

1. Maximum input analog voltage cannot exceed V_{DDA}.
2. Exceeding the maximum voltage on the SPARE_ADC signals for the related conversion scale must be avoided since the ADC conversion accuracy can be impacted.
3. ADC reference voltage at T_A = 25 °C.

ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Table 16. ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Symbol	Parameter	Typ.(1)	Min.(2)	Max.(2)	Unit
$\|E_T\|$	Total unadjusted error(3), (4), (5)	2.8			LSB
$\|E_O\|$	Offset error(3), (4), (5)	0.3			
$\|E_G\|$	Gain error(3), (4), (5), (6)	0.4			
E_{O+G}	Offset + gain error(6), (7)		-8.5	9.3	
E_{O+G}	Offset + gain error(6), (8)		-11	11	
E_{O+G}	Offset + gain error(6), (9)		-14.3	11.3	
$\|E_D\|$	Differential linearity error(1), (2), (3)	0.5			
$\|E_L\|$	Integral linearity error(3), (4), (5)	1.4			

1. Temperature operating: T_A = 25 °C.
2. Data based on characterization results, not tested in production.
3. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject the negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$and $\Sigma_{INJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
4. Results in manufacturing test mode.
5. Data aligned with trimming voltage parameters.
6. Gain error evaluation with the two point method.
7. Temperature operating range: 0 ºC ≤ T_A ≤ 85 ºC.
8. Temperature operating range: -25 ºC ≤ T_A ≤ 105 ºC.
9. Temperature operating range: -40 ºC ≤ TA ≤ 105 ºC.

ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

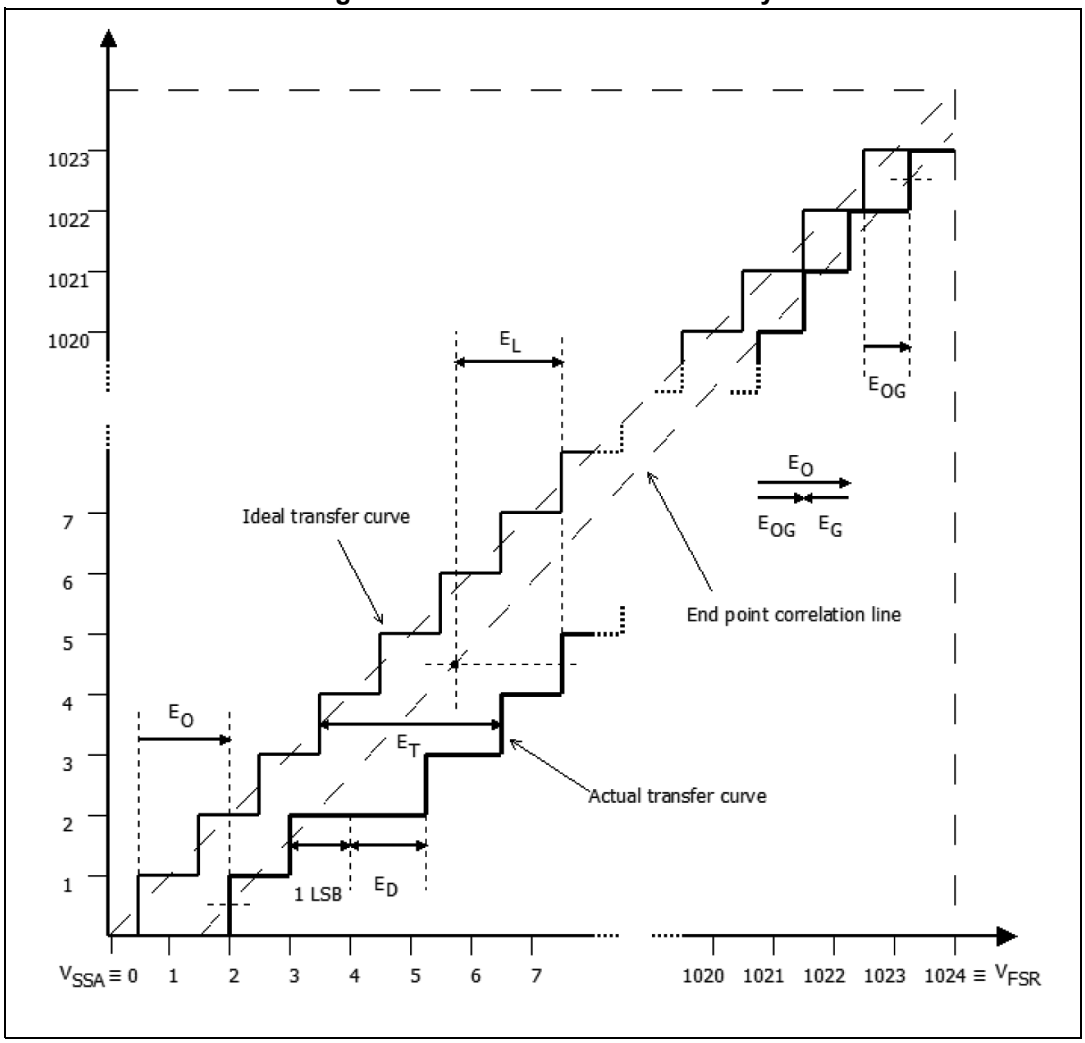
Table 17. ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

Symbol	Parameter	Typ.(1)	Min.(2)	Max.(2)	Unit
$\|E_T\|$	Total unadjusted error(3) (4), (5)	TBD			LSB
$\|E_O\|$	Offset error(3), (4), (5)	0.5			
$\|E_G\|$	Gain error(3), (4), (5), (6)	0.4			
E_{O+G}	Offset + gain error(6), (7)		-8.3	8.9	
E_{O+G}	Offset + gain error(6), (8)		-10.9	10.9	
EO+G	Offset + gain error(6), (9)		-13.8	10.9	
$\|E_D\|$	Differential linearity error(1), **(2)**, (3)	0.8			
$\|E_L\|$	Integral linearity error(3), (4), (5)	2.0			

1. Temperature operating: TA= 25 °C.
2. Data based on characterization results, not tested in production.
3. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be to added to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma_{IINJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
4. Results in manufacturing test mode.
5. Data aligned with trimming voltage parameters.
6. Gain error evaluation with two point method.
7. Temperature operating range: 0 ºC ≤ T_A ≤ 85 ºC.
8. Temperature operating range: -25 ºC ≤ T_A ≤ 105 ºC.
9. Temperature operating range: -40 ºC ≤ TA ≤ 105 ºC. 11.

ADC conversion accuracy

Figure 16. ADC conversion accuracy



ADC accuracy parameter definitions:

- **E_T** = total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
- **E_O** = offset error: deviation between the first actual transition and the first ideal one.
- **E_{OG}** = offset + gain error (1-point gain): deviation between the last ideal transition and the last actual one.
- **E_G** = gain error (2-point gain): defined so that EOG = EO + EG (parameter correlated to the deviation of the characteristic slope).
- **E_D** = differential linearity error: maximum deviation between actual steps and the ideal one.
- **E_L** = integral linearity error: maximum deviation between any actual transition and the end point correlation line.

5.4 EMC characteristics

5.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts * (n + 1) supply pin).

Table 18. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JEDEC/JESD22-A114E	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD STM 5.3.1 ESDA	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JEDEC/JESD-A115-A	200	

Data based on characterization results, not tested in production.

5.4.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to THE each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.

Table 19. Electrical sensitivity

Symbol	Parameter	Conditions	Level
LU	Static latch-up class	T_A = 105 °C	A

6 Thermal characteristics

The STWBC functionality cannot be guaranteed when the device operating exceeds the maximum chip junction temperature (T_{Jmax}).

T_{Jmax}, in °C, may be calculated using equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta J_A)$$

where:

T_{Amax} is the maximum ambient temperature in °C

ΘJ_A is the package junction to ambient thermal resistance in °C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + PI/O_{max}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins where:

$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma [(V_{DD} - V_{OH}) * I_{OH}]$,

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at the low and high level.

Table 20. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	VFQFPN32 - thermal resistance junction to ambient(1)	26	°C/W

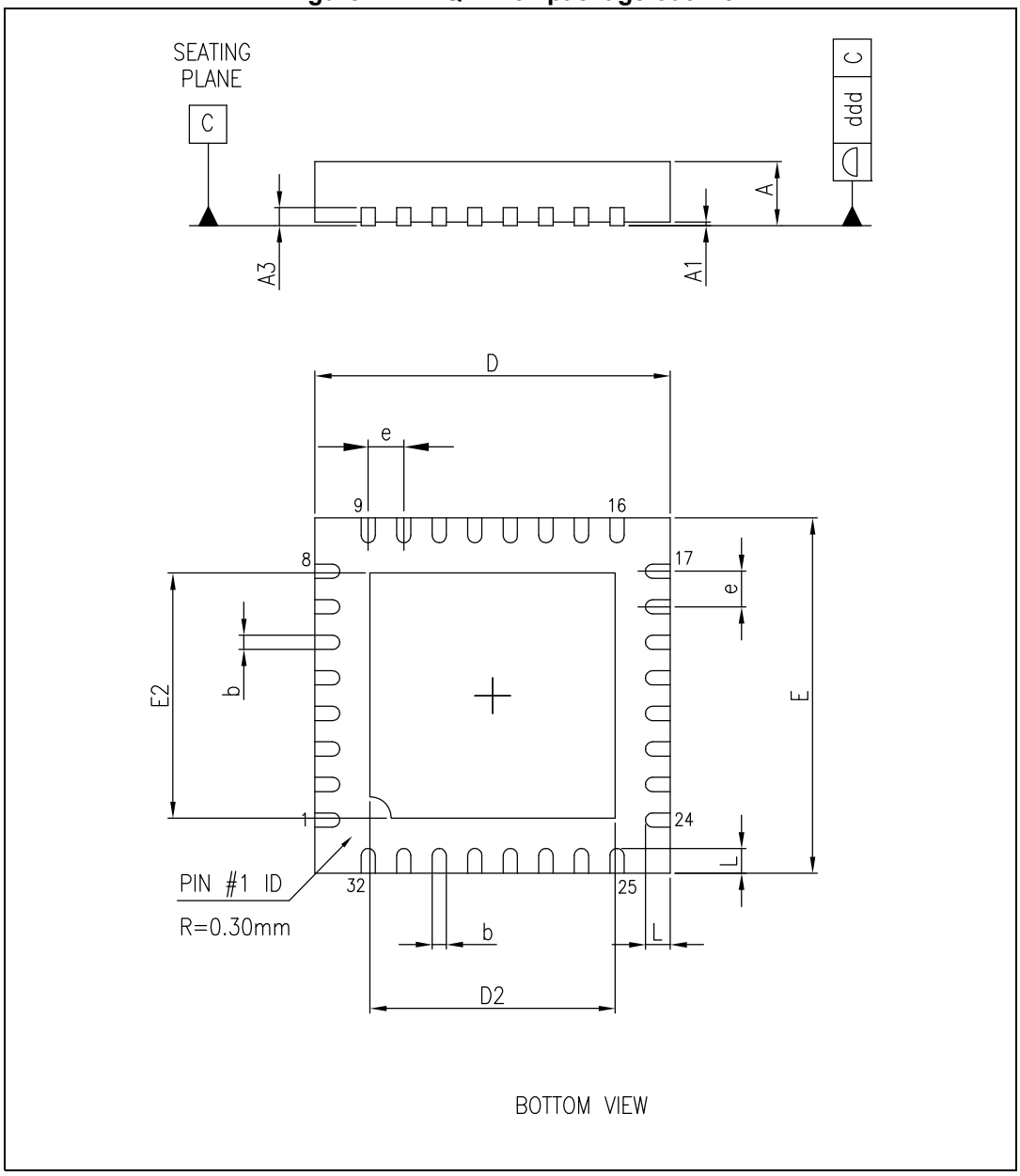
1. Thermal resistance is based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 Package design overview

Figure 17. VFQFPN32 package outline



7.2 Package mechanical data

Table 21. VFQFPN32 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.40	3.45	3.50
E	4.85	5.00	5.15
E2	3.40	3.45	3.50
e		0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

Note: 1. VFQFPN stands for “Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead”.

2. Very thin profile: 0.80 < A ≤ 1.00 mm.

3. Details of the terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.

4. Package outline exclusive of any mold flashes dimensions and metal burrs.

8 Order codes

Table 22. Silicon product order code

Order code	Package	Packaging
STWBC	VFQFPN32	Tube
STWBCTR		Tape and reel

9 Revision history

Table 23. Document revision history

Date	Revision	Changes
18-Dec-2014	1	Initial release.
23-Feb-2015	2	Updated main title *on page 1*. Updated *Section : Applications on page 1* (added “certified” to Qi A11). Added *Section 3: Certified Qi A11 solution on page 9*. Updated *Figure 3: STWBC pinout view on page 10* (updated title, replaced by new figure). Updated *Table 1: Pinout description on page 11* (replaced by new table). Added *Section 5: Electrical characteristics on page 13* and *Section 6: Thermal characteristics on page 32*. Minor modifications throughout document.
26-Feb-2015	3	Updated main title *on page 1*. Updated *Section : Features on page 1* (minor modifications). Updated *Section 1: Description on page 6* (replaced by new Description). Added *Section 2: Introduction to wireless battery charging systems on page 8* (added title and Description from rev. 2, updated title of *Figure 2*). Removed Section “2 STWBC system architecture” from page 7 (*Figure 2 on page 8* moved to *Section 1: Description*). Updated *Section 3: Certified Qi A11 solution on page 9* (renumbered headings). Minor modifications throughout document.