# STW81102

Multi-band RF frequency synthesizer with integrated VCOs

Feature summary

- Integer-N Frequency Synthesizer
- Dual differential integrated VCOs with automatic center frequency calibration:
  - 3000 - 3620 MHz (Direct output)
  - 4000 - 4650 MHz (Direct output)
  - 1500 - 1810 MHz (Internal divider by 2)
  - 2000 - 2325 MHz (Internal divider by 2)
  - 750 - 905 MHz (Internal divider by 4)
  - 1000 - 1162.5 MHz (Internal divider by 4)
- Excellent integrated phase noise
- Fast lock time: 150µs
- Dual modulus programmable prescaler (16/17 or 19/20)
- 2 programmable counters to achieve a feedback division ratio from 256 to 65551 (prescaler 16/17) and from 361 to 77836 (prescaler 19/20).
- Programmable reference frequency divider (10 bits)
- Phase frequency comparator and charge pump
- Programmable charge pump current
- Digital Lock Detector
- Dual Digital Bus Interface: SPI and I^{2}C bus with 3 bit programmable address (1100$A_2A_1A_0$)
- 3.3V Power Supply
- Power down mode (HW and SW)
- Small size exposed pad VFQFPN28 package 5x5x1.0mm
- Process: BICMOS 0.35µm SiGe

VFQFPN28

Applications

- 2.5G and 3G Cellular Infrastructure Equipment
- CATV Equipment
- Instrumentation and Test Equipment
- Other Wireless Communication Systems

Description

The STMicroelectronics STW81102 is an integrated RF synthesizer with voltage controlled oscillators (VCOs). Showing high performance, high integration, low power, and multi-band performances, STW81102 is a low cost one chip alternative to discrete PLL and VCOs solutions.

STW81102 includes an Integer-N frequency synthesizer and two fully integrated VCOs featuring low phase noise performance and a noise floor of -155dBc/Hz. The combination of wide frequency range VCOs (thanks to center-frequency calibration over 32 sub-bands) and multiple output options (direct output, divided by 2 or divided by 4) allows to cover from 750MHz to 905MHz and 1000MHz to 1162.5MHz, from 1500MHz to 1810MHz and 2000MHz to 2325MHz, from 3000MHz to 3620MHz and 4000MHz to 4650MHz bands.

The STW81102 is designed with STMicroelectronics advanced 0.35µm SiGe process.

Order codes

Part number	Temp range, °C	Package	Packing
STW81102AT	-40 to 85	VFQFPN28	Tray
STW81102ATR	-40 to 85	VFQFPN28	Tape & Reel

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1 Block diagram and pin configuration

1.1 Block diagram

Figure 1. Block diagram
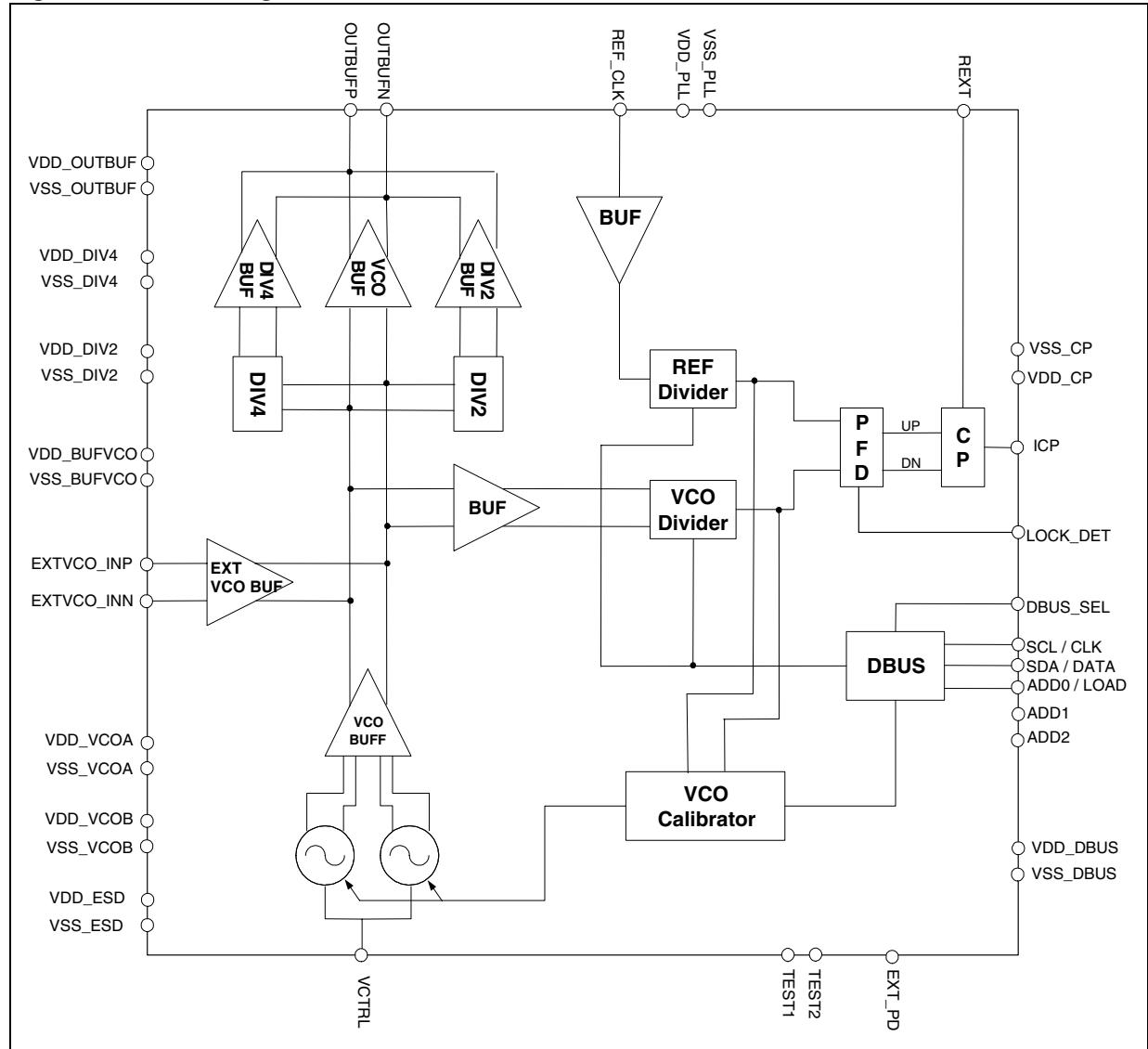
1.2 Pin configuration

Figure 2.   Pin connection (top view)
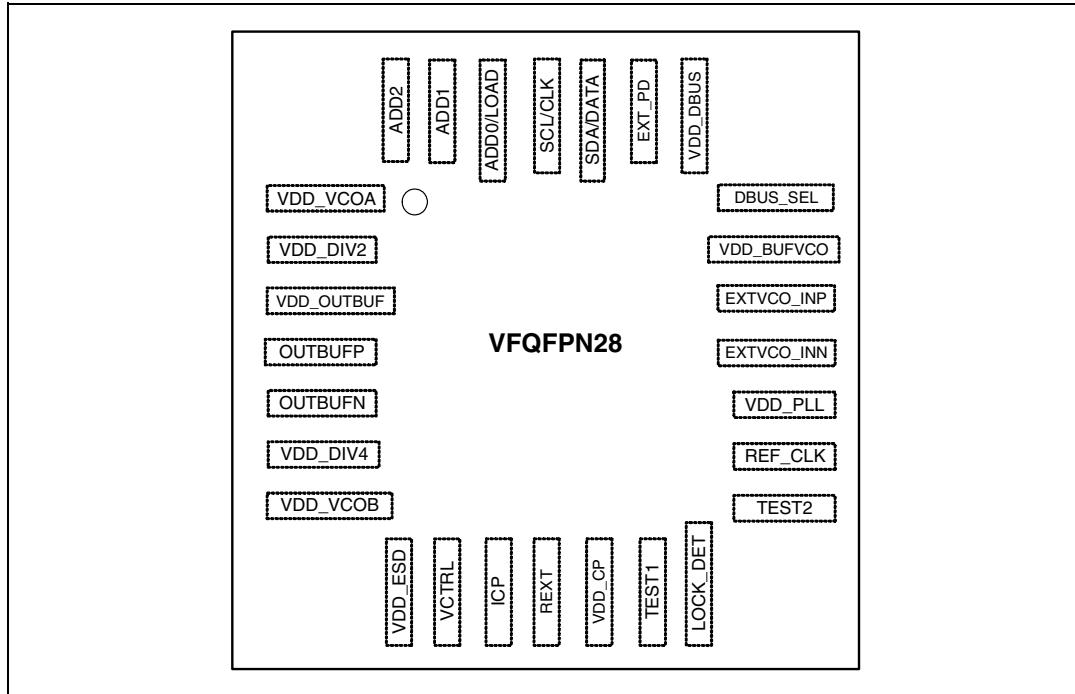
Table 1.   Pin description

Pin No	Name	Description	Observation
1	VDD_VCOA	VCOA power supply	
2	VDD_DIV2	Divider by 2 power supply	
3	VDD_OUTBUF	Output buffer power supply	
4	OUTBUFP	LO buffer positive output	Open collector
5	OUTBUFN	LO buffer negative output	Open collector
6	VDD_DIV4	Divider by 4 power supply	
7	VDD_VCOB	VCOB power supply	
8	VDD_ESD	ESD positive rail power supply	
9	VCTRL	VCO control voltage	
10	ICP	PLL charge pump output	
11	REXT	External resistance connection for PLL charge pump	
12	VDD_CP	Power supply for charge pump	
13	TEST1	Test input 1	Test purpose only; must be connected to GND
14	LOCK_DET	Lock detector	CMOS Output

Table 1.   Pin description (continued)

Pin No	Name	Description	Observation
15	TEST2	Test input 2	Test purpose only; must be connected to GND
16	REF_CLK	Reference clock input	
17	VDD_PLL	PLL digital power supply	
18	EXTVCO_INN	External VCO negative input	Test purpose only; must be connected to GND
19	EXTVCO_INP	External VCO positive input	Test purpose only; must be connected to GND
20	VDD_BUFVCO	VCO buffer power supply	
21	DBUS_SEL	Digital Bus Interface select	CMOS Input
22	VDD_DBUS	SPI and I^2C bus power supply	
23	EXT_PD	Power down hardware	CMOS Input
24	SDA/DATA	I2CBUS/SPI data line	CMOS Bidir Schmitt triggered
25	SCL/CLK	I2CBUS/SPI clock line	CMOS Input
26	ADD0/LOAD	I2CBUS address select pin/ SPI load line	CMOS Input
27	ADD1	I2CBUS address select pin	CMOS Input
28	ADD2	I2CBUS address select pin	CMOS Input

2   Electrical specifications

2.1   Absolute maximum ratings

Table 2.   Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog Supply voltage	0 to 4.6	V
DV_{CC}	Digital Supply voltage	0 to 4.6	V
T_{stg}	Storage temperature	-65 to 150	°C
ESD	Electrical Static Discharge - HBM[1] - CDM-JEDEC Standard - MM	4 1.5 0.2	KV

1.   The maximum rating of the ESD protection circuitry on pin 4 and pin 5 is 800V.

2.2   Operating conditions

Table 3.   Operating conditions (Refer to application diagram)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AV_{DD}	Analog Supply voltage		3.0	3.3	3.6	V
DV_{DD}	Digital Supply voltage		3.0	3.3	3.6	V
I_{VDD1}	V_{DD1} Current Consumption				100	mA
I_{VDD2}	V_{DD2} Current Consumption				15	mA
T_{amb}	Operating ambient temperature		-40		85	°C
T_j	Maximum junction temperature				125	°C
$R_{th\ j\text{-}amb}$	Junction to ambient package thermal resistance	Multilayer JEDEC board		35		°C/W

2.3   Digital logic levels

Table 4.   Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.2*Vdd	V
V_{ih}	High level input voltage		0.8*Vdd			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V
V_{ol}	Low level output voltage				0.4	V
V_{oh}	High level output voltage		0.85*Vdd			V

2.4 Electrical characteristics

Table 5. **Electrical characteristics**

All the Electrical Specifications are intended at 3.3V supply Voltage.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OUTPUT FREQUENCY RANGE						
F_{OUTA}	Output Frequency Range with VCOA	Direct Output	3000		3620	MHz
		Divider by 2	1500		1810	MHz
		Divider by 4	750		905	MHz
F_{OUTB}	Output Frequency Range with VCOB	Direct Output	4000		4650	MHz
		Divider by 2	2000		2325	MHz
		Divider by 4	1000		1162.5	MHz
VCO DIVIDERS						
N	VCO Divider Ratio	Prescaler 16/17	256		65551	
		Prescaler 19/20	361		77836	
REFERENCE CLOCK and PHASE FREQUENCY DETECTOR						
f_{ref}	Reference input frequency		10		200	MHz
	Reference input sensitivity[1]		0.35	1	1.5	Vpeak
R	Reference Divider Ratio		2		1023	
f_{PFD}	PFD input frequency				16	MHz
f_{step}	Frequency step[2]	Prescaler 16/17	$F_{OUT}/65551$		$F_{OUT}/256$	Hz
		Prescaler 19/20	$F_{OUT}/77836$		$F_{OUT}/361$	Hz
CHARGE PUMP						
I_{CP}	ICP sink/source[3]	3bit programmable			5	mA
V_{OCP}	Output voltage compliance range		0.4		V_{dd}-0.3	V
	Spurious[4]	Direct Output (f_{PFD} = 200KHz)		-73		dBc
		Divider by 2 (f_{PFD} = 400KHz)		-83		dBc
		Divider by 4 (f_{PFD} = 800KHz)		-91		dBc
VCOs						
K_{VCOA}	VCOA sensitivity[5]	Lower frequency range	40	55	70	MHz/V
		Intermediate frequency range	60	75	95	MHz/V
		Higher frequency range	80	105	140	MHz/V
K_{VCOB}	VCOB sensitivity[5]	Lower frequency range	30	45	60	MHz/V
		Intermediate frequency range	40	55	70	MHz/V
		Higher frequency range	50	70	90	MHz/V

Table 5.   Electrical characteristics (continued)
All the Electrical Specifications are intended at 3.3V supply Voltage.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	VCO A Pushing[5]			4	7	MHz/V
	VCO B Pushing[5]			14	20	MHz/V
V_{CTRL}	VCO control voltage[5]		0.4		3	V
	LO Harmonic Spurious[5]				-20	dBc
I_{VCOA}	VCOA current consumption	f_{VCO}=3.3GHz ; amplitude [11]		30		mA
		f_{VCO}=3.3GHz ; amplitude [00]		16		mA
I_{VCOB}	VCOB current consumption	f_{VCO}=4.3GHz ; amplitude [11]		22		mA
		f_{VCO}=4.3GHz ; amplitude [00]		11		mA
I_{VCOBUF}	VCO buffer consumption			15		mA
I_{DIV2}	DIVIDER by 2 consumption			17		mA
I_{DIV4}	DIVIDER by 4 consumption			13		mA
LO OUTPUT BUFFER						
P_{LO}	Output level			0		dBm
R_L	Return Loss[5]	Matched to 50ohm		15		dB
I_{OUTBUF}	Current Consumption	DIV4 Buff		27		mA
		DIV2 Buff		23		mA
		Direct Output		39		mA
EXTERNAL VCO (Test purpose only)						
	Frequency range		3.0		4.65	GHz
	Input level		0		+6	dBm
	Current Consumption	VCO Internal Buffer		15		mA
PLL MISCELLANEOUS						
I_{PLL}	Current Consumption	Input Buffer, Prescaler, Digital Dividers, misc.		12		mA
T_{lock}	Lock up time [5], [6]	25KHz PLL bandwidth; within 1 ppm of frequency error		150		µs

1. In order to achieve best phase noise performance 1V peak level is suggested.

2. The frequency step is related to the PFD input frequency as follows:
    - f_{step} = f_{PFD} for Direct Output
    - f_{step} = f_{PFD}/2 for Divided by 2 Output
    - f_{step} = f_{PFD}/4 for Divided by 4 Output

3. see relationship between ICP and REXT in the Circuit Description section (Charge Pump)

4. The level of the spurs may change depending on PFD frequency, Charge Pump current, selected channel and PLL loop BW.

5. Guaranteed by design and characterization.

6. Frequency jump from 2300 to 2150 MHz; it includes the time required by the VCO calibration procedure (7 f_{PFD} cycles with f_{PFD}=400KHz).

2.5 Phase noise specification

Table 6.   **Phase noise specification**

Parameter	Test conditions	Min	Typ	Max	Unit
PHASE NOISE PERFORMANCE[1]					
In Band Phase Noise Floor – Closed Loop[2]					
Normalized In Band Phase Noise Floor	ICP=4mA, PLL BW = 50KHz; including reference clock contribution		-222		dBc/Hz
In Band Phase Noise Floor Direct Output	ICP=4mA, PLL BW = 50KHz; including reference clock contribution		$-222+20\log(N)+10\log(f_{PFD})$		dBc/Hz
In Band Phase Noise Floor Divider by 2			$-228+20\log(N)+10\log(f_{PFD})$		dBc/Hz
In Band Phase Noise Floor Divider by 4			$-234+20\log(N)+10\log(f_{PFD})$		dBc/Hz
PLL Integrated Phase Noise – Direct Output					
Integrated Phase Noise 100Hz to 40MHz	F_{OUT} = 4.3 GHz, f_{PFD} = 200KHz, f_{STEP} =200 KHz, PLL BW = 15KHz, ICP=4mA		-35		dBc
			1.4		° rms
PLL Integrated Phase Noise – Divider by 2					
Integrated Phase Noise 100Hz to 40MHz	F_{OUT} = 2.15 GHz, f_{PFD} = 400KHz, f_{STEP} =200 KHz, PLL BW = 20KHz, ICP=3mA		-44		dBc
			0.52		° rms
PLL Integrated Phase Noise – Divider by 4					
Integrated Phase Noise 100Hz to 40MHz	F_{OUT} = 1.075 GHz, f_{PFD} = 800KHz, f_{STEP} =200 KHz, PLL BW = 30KHz, ICP=2.5mA		-51		dBc
			0.22		° rms
VCO A Direct (3000MHz-3620MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-56		dBc/Hz
Phase Noise @ 10 KHz			-83		dBc/Hz
Phase Noise @ 100 KHz			-107		dBc/Hz
Phase Noise @ 1 MHz			-129		dBc/Hz
Phase Noise @ 10 MHz			-149		dBc/Hz
Phase Noise @ 40 MHz			-159		dBc/Hz
VCO B Direct (4000MHz-4650MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-54		dBc/Hz
Phase Noise @ 10 KHz			-82		dBc/Hz
Phase Noise @ 100 KHz			-106		dBc/Hz
Phase Noise @ 1 MHz			-128		dBc/Hz
Phase Noise @ 10 MHz			-148		dBc/Hz
Phase Noise @ 40 MHz			-158		dBc/Hz

Table 6.   Phase noise specification (continued)

Parameter	Test conditions	Min	Typ	Max	Unit
VCO A with divider by 2 (1500MHz-1810MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-62		dBc/Hz
Phase Noise @ 10 KHz			-89		dBc/Hz
Phase Noise @ 100 KHz			-113		dBc/Hz
Phase Noise @ 1 MHz			-135		dBc/Hz
Phase Noise @ 10 MHz			-151.5		dBc/Hz
Phase Noise Floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 2 (2000MHz-2325MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-60		dBc/Hz
Phase Noise @ 10 KHz			-88		dBc/Hz
Phase Noise @ 100 KHz			-112		dBc/Hz
Phase Noise @ 1 MHz			-134		dBc/Hz
Phase Noise @ 10 MHz			-151.5		dBc/Hz
Phase Noise Floor @ 40 MHz			-155		dBc/Hz
VCO A with divider by 4 (750MHz-905MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-68		dBc/Hz
Phase Noise @ 10 KHz			-95		dBc/Hz
Phase Noise @ 100 KHz			-119		dBc/Hz
Phase Noise @ 1 MHz			-141		dBc/Hz
Phase Noise @ 10 MHz			-154		dBc/Hz
Phase Noise Floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 4 (1000MHz-1162.5MHz) – Open Loop[3]					
Phase Noise @ 1 KHz			-66		dBc/Hz
Phase Noise @ 10 KHz			-94		dBc/Hz
Phase Noise @ 100 KHz			-118		dBc/Hz
Phase Noise @ 1 MHz			-140		dBc/Hz
Phase Noise @ 10 MHz			-154		dBc/Hz
Phase Noise Floor @ 40 MHz			-155		dBc/Hz

1. Phase Noise SSB.
    VCO amplitude setting to value [11].
    All the closed-loop performances are specified using a Reference Clock signal at 76.8 MHz with phase noise of
    -135dBc/Hz @1KHz offset, -145dBc/Hz @10KHz offset and -149.5dBc/Hz of noise floor.

2. Normalized PN = Measured PN – 20log(N) – 10log(f_{PFD}) where N is the VCO divider ratio (N=B*P+A) and f_{PFD} is the
    comparison frequency at the PFD input

3. Typical Phase Noise at centre band frequency

> Upon request an Evaluation Kit is available including a powerful simulation tool
> (STWPLLSim) which allows to estimate very accurately the Phase Noise of the device
> according to the desired project parameters (VCO Frequency, Selected Output Stage,
> Reference Clock, Frequency Step, …); refer to the Application Information (*Section 7*) for
> more details.

3 Typical performance characteristics

The phase noise is measured with the Agilent E5052A Signal Source Analyzer. All the closed-loop measurements are done with f_{STEP}=200 KHz setting properly the f_{PFD} and the Charge Pump current. The loop filter configuration used is depicted in the paragraph 8 (Application Diagram) and the Reference Clock signal is at 76.8 MHz with phase noise of -135dBc/Hz @1KHz offset, -145dBc/Hz @10KHz offset and -149.5dBc/Hz of noise floor.

Figure 3. VCO A (Direct output) open loop phase noise
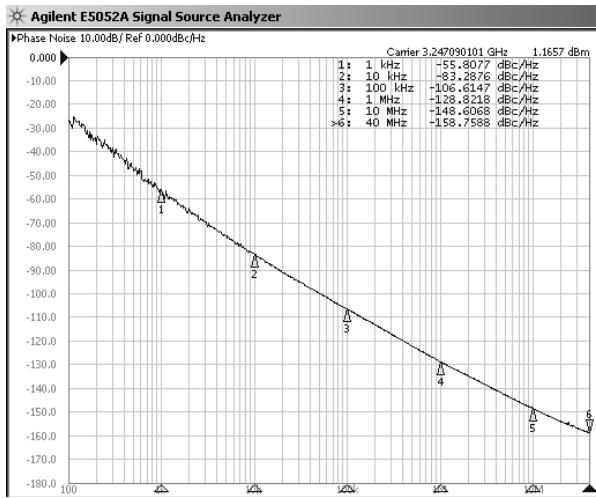
Figure 4. VCO B (Direct output) open loop phase noise
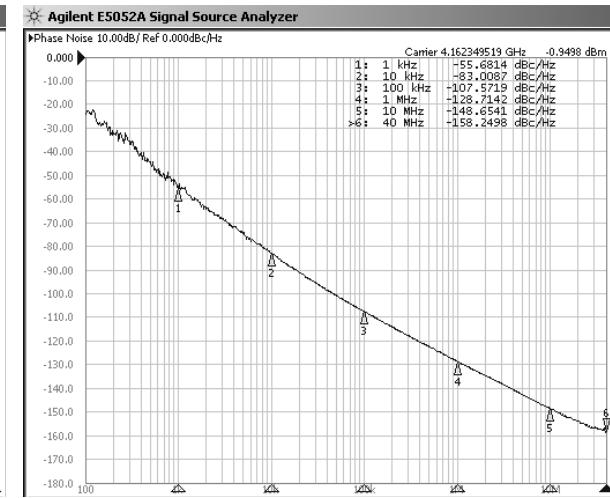
Figure 5. VCO A (Direct output) closed loop phase noise at 3.6GHz (F_{STEP}=200KHz; F_{PFD}=200KHz; I_{CP}=3mA)
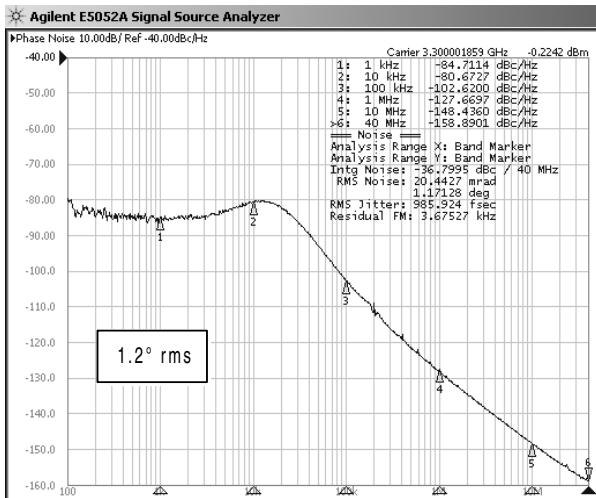
Figure 6. VCO B (Direct output) closed loop phase noise at 4.3GHz (F_{STEP}=200KHz; F_{PFD}=200KHz; I_{CP}=4mA)
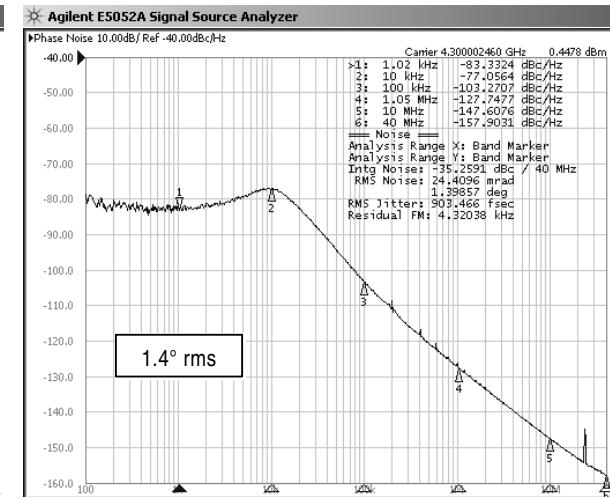
Figure 7. **VCO A (Div. by 2 output) closed loop phase noise at 1.65GHz (F$_{STEP}$=200KHz; F$_{PFD}$=400KHz; I$_{CP}$=2mA)**
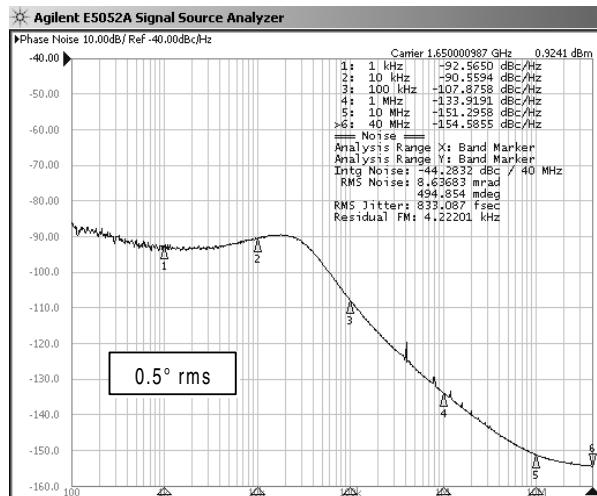
Figure 8. **VCO B (Div. by 2 output) closed loop phase noise at 2.15GHz (F$_{STEP}$=200KHz; F$_{PFD}$=400KHz; I$_{CP}$=3mA)**
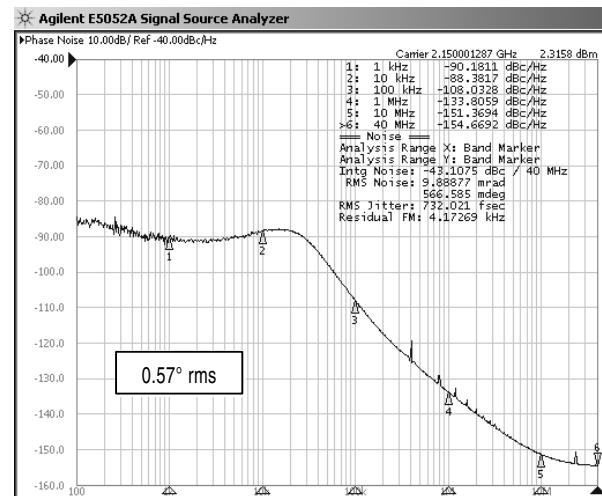
Figure 9. **VCO A (Div. by 4 output) closed loop phase noise at 825MHz (F$_{STEP}$=200KHz; F$_{PFD}$=800KHz; I$_{CP}$=1.5mA)**
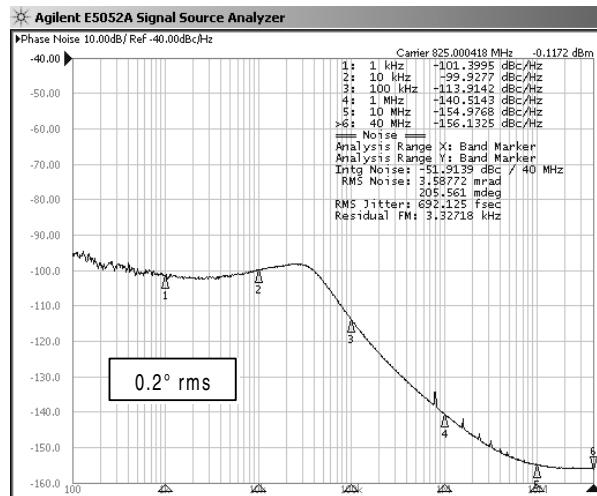
Figure 10. **VCO B (Div. by 4 output) closed loop phase noise at 1.075GHz (F$_{STEP}$=200KHz; F$_{PFD}$=800KHz; I$_{CP}$=2.5mA)**
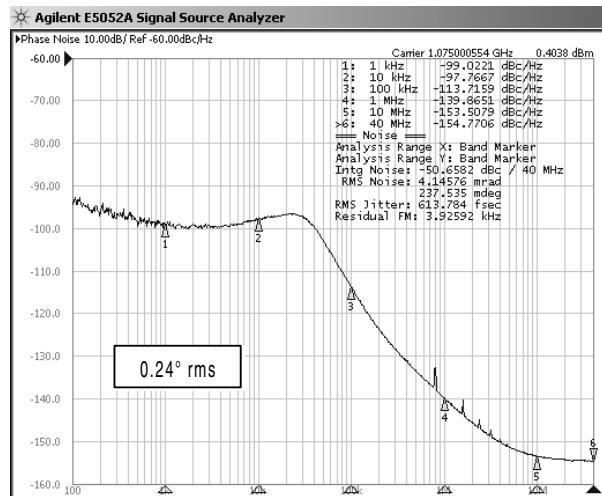
Figure 11.   PFD Frequency Spurs (Direct Output; F_PFD=200KHz)
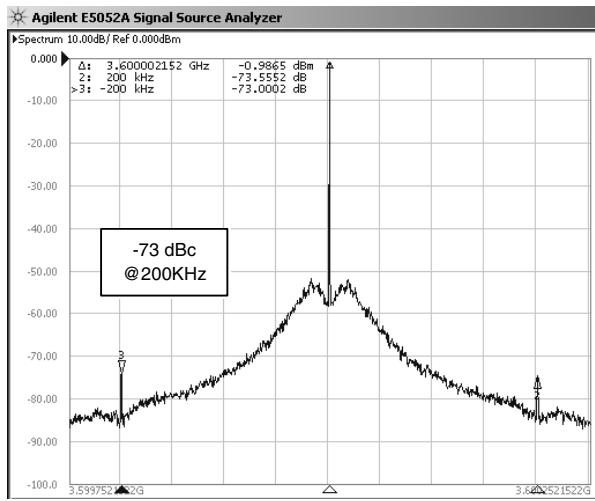
Figure 12.   PFD Frequency Spurs (Div. by 2 Output; F_PFD=400KHz)
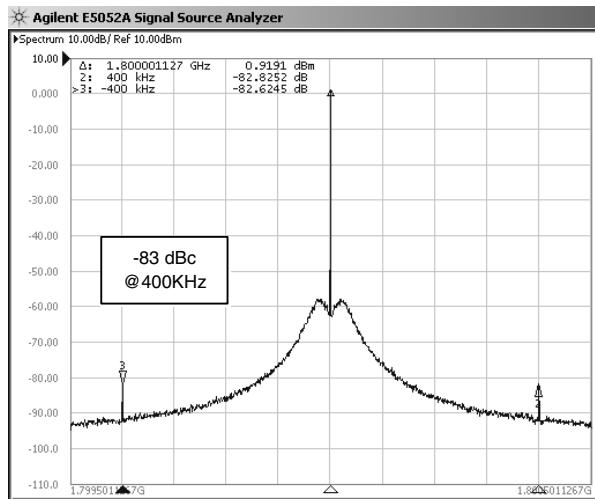
Figure 13.   PFD Frequency Spurs (Div. by 4 Output; F_PFD=800KHz)
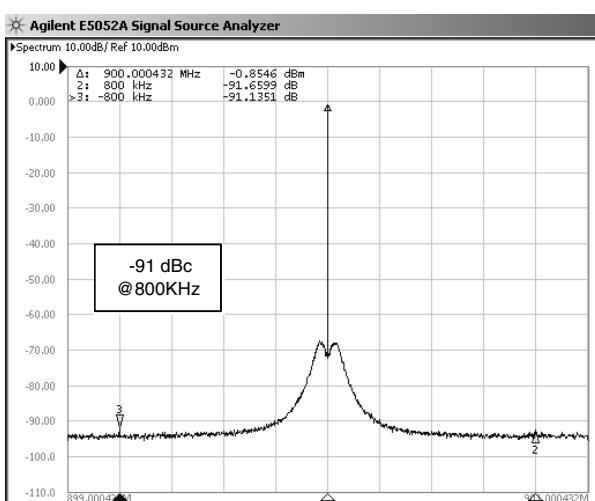
Figure 14.   Settling Time (Final Frequency=2.15 GHz; F_PFD=400KHz; I_CP=3mA)
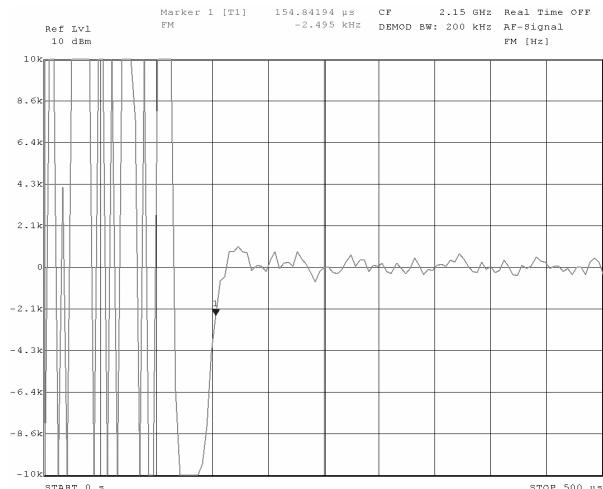
4 General description

The block diagram of *Figure 1* shows the different blocks, which have been integrated to achieve an integer-N PLL frequency synthesizer.

The STW81102 consists of 2 internal low-noise VCOs with buffer blocks, a divider by 2, a divider by 4, a low-noise PFD (Phase Frequency Detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a programmable dual-modulus prescaler. The A-counter (5 bits) and B counter (12 bits) counters, in conjunction with the dual modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where $N = B*P + A$. The division ratio of both reference and VCO dividers is controlled through the selected digital interface (I^2C bus or SPI).

The selection of the digital interface type is done by the proper hardware connection of the pin DBUS_SEL (0 V for I^2C bus, 3.3 V for SPI).

All devices operate with a power supply of 3.3 V and can be powered down when not in use.

4.1 Circuit description

4.1.1 Reference input stage

The reference input stage is shown in *Figure 15*. The resistor network feeds a DC bias at the Fref input while the inverter used as the frequency reference buffer is AC coupled.

Figure 15. Reference Frequency Input Buffer
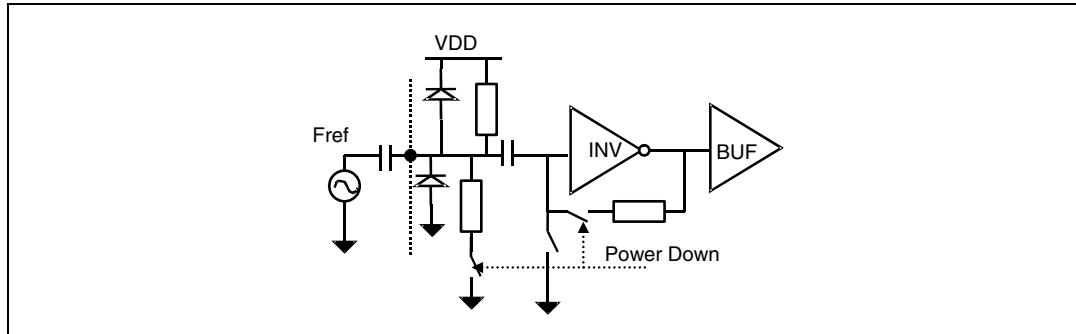
4.1.2 Reference divider

The 10-bit programmable reference counter allows the input reference frequency to be divided to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

4.1.3 Prescaler

The dual-modulus prescaler P/P+1 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus (P) is programmable and can be set to 16 or 19. It is based on a synchronous 4/5 core which division ratio depends on the state of the modulus input.

4.1.4 A and B counters

The A (5 bits) and B (12 bits) counters, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler make it possible to generate output frequencies which are spaced only by the reference frequency divided by the reference division ratio. Thus, the division ratio and the VCO output frequency are given by these formulas:

$N = B \cdot P + A$

$$F_{vco} = \frac{(B \cdot P + A) \cdot F_{ref}}{R}$$

where:

F_{vco}: output frequency of VCO.

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface).

B: division ratio of the main counter.

A: division ratio of the swallow counter.

F_{ref}: input reference frequency.

R: division ratio of reference counter.

N: division ratio of PLL

For a correct work of the VCO divider, B must be strictly higher than A. A can take any value ranging from 0 to 31. The range of the N number can vary from 256 to 65551 (P=16) or from 361 to 77836 (P=19).

Figure 16. VCO Divider Diagram
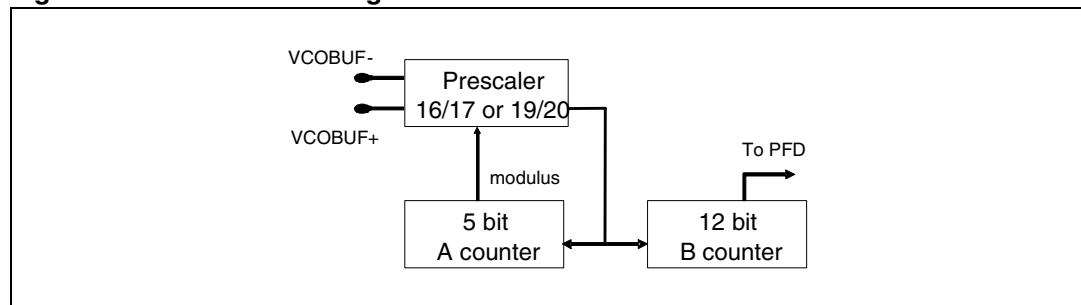
4.1.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 17 is a simplified schematic of the PFD.

Figure 17. PFD diagram
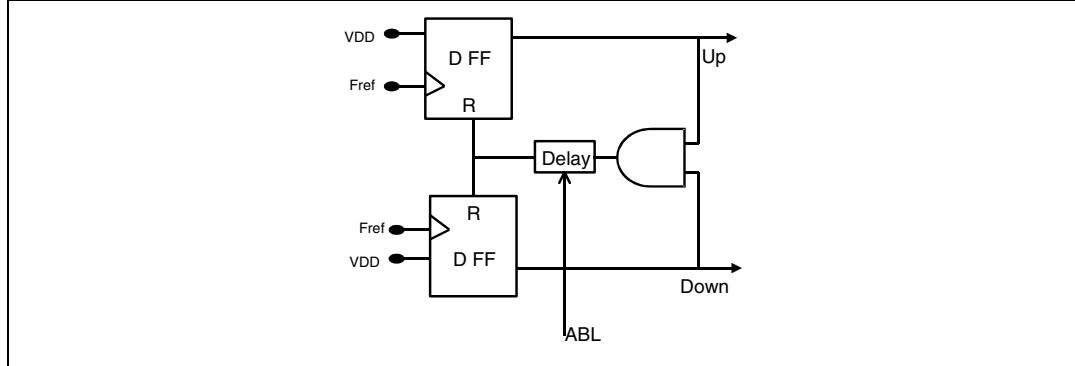
4.1.6 Lock detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). Lock Detect signal is high when the PLL is locked. When Power Down is activated, Lock Detect is let to high level (Lock Detect consumes current only during PLL transients).

4.1.7 Charge pump

This block drives two matched current sources, Iup and Idown, which are controlled respectively by UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (to be connected to the REXT input pin) and a selection among 8 by a 3 bit word.

The minimum value of the output current is: $I_{MIN} = 2*VBG/REXT$ (VBG~1.17 V)

Table 7. Current value vs selection

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=4.7 KΩ
0	0	0	I_{MIN}	0.5 mA
0	0	1	$2*I_{MIN}$	1.0 mA
0	1	0	$3*I_{MIN}$	1.5 mA
0	1	1	$4*I_{MIN}$	2.0 mA
1	0	0	$5*I_{MIN}$	2.5 mA
1	0	1	$6*I_{MIN}$	3.0 mA
1	1	0	$7*I_{MIN}$	3.5 mA
1	1	1	$8*I_{MIN}$	4.0 mA

Note: *The current is output on pin ICP. During the VCO auto calibration, ICP and VCTRL pins are forced to VDD/2*

Figure 18. Loop filter connection
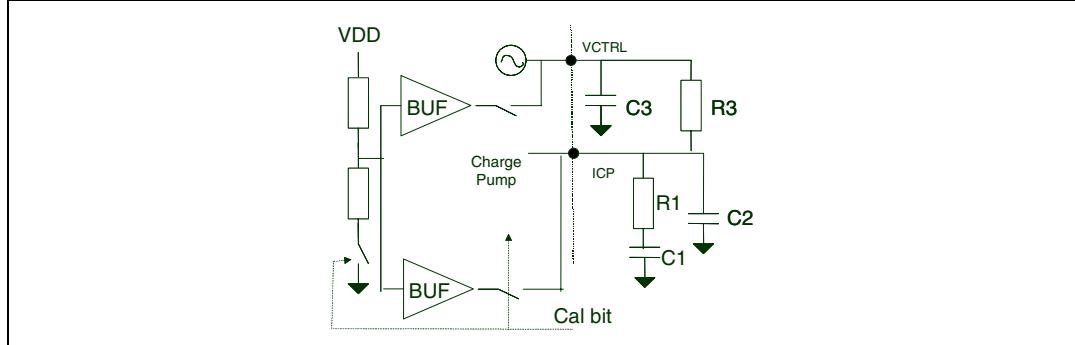
4.1.8 Voltage controlled oscillators

VCO Selection

Within STW81102 two low-noise VCOs are integrated to cover a wide band from 3000MHz to 3620MHz and 4000MHz to 4650MHz (direct output), from 1500MHz to 1810MHz and 2000MHz to 2325MHz (selecting divider by 2), from 750MHz to 905MHz and 1000MHz to 1162.5MHz (selecting divider by 4).

VCO A frequency range 3000MHz-3620MHz
VCO B frequency range 4000MHz-4650MHz

VCO Frequency Calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors to the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variation on the VCO center frequency.

An automatic selection of the range is performed when the bit SERCAL rises from "0" to "1". The charge pump is inhibited and the pins ICP & VCTRL are at VDD/2 volts. Then the ranges are tested to select the one which with this VCO input voltage is the nearest to the desired output frequency (Fout = N*Fref/R). When this selection is achieved the signal ENDCALB (which means End of Calibration) falls to "0", then the charge pump is enabled again and SERCAL should be reset to "0" before the next channel step. The PLL has just to perform fine adjustment around VDD/2 on the loop filter to reach Fout, which enables a fast settle.

Figure 19. VCO Sub-Bands Frequency Characteristics
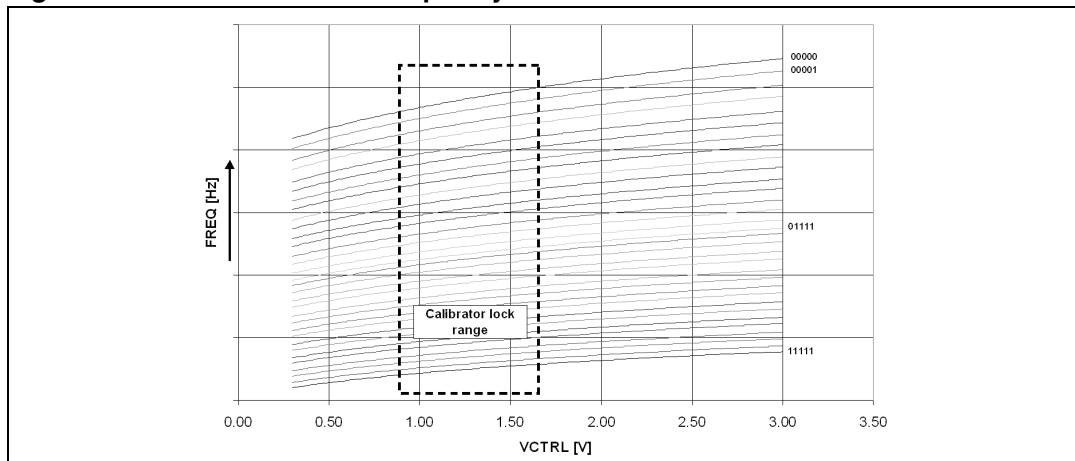
The SERCAL bit should be set to "1" at each division ratio change. It should be noted that in order to reset the autocalibrator State Machine after a power-up, and anyway before the first calibration, the INITCAL bit should be set to "1" and back to "0" (this operation is automatically performed by the Power On Reset circuitry). The calibration takes approximately 7 periods of the PFD Frequency.

The maximum allowed f_{PFD} to perform the calibration process is 1 MHz. Using an higher F_{PFD} the following procedure should be adopted:

1. Calibrate the VCO at the desired frequency with an f_{PFD} less than 1 MHz
2. Set the A, B and R dividers ratio for the desired f_{PFD}

VCO Voltage Amplitude Control

The voltage swing of the VCOs can be adjusted over 4 levels by means of two dedicated programming bits (PLL_A1 and PLL_A0). Higher amplitudes provide best phase noise while lower ones save power.

The following table gives the voltage level expected on the resonator nodes, the current consumption and the phase noise @1MHz.

Table 8.   VCO A performances vs. amplitude setting (Freq=3.3GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current Consumption (mA)	PN @1MHz (dBc/Hz)
00	1.1	16	-125
01	1.3	18	-126
10	1.9	27	-128.5
11	2.1	30	-129

Table 9.   VCO B performances vs. amplitude setting (Freq=4.3GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current Consumption (mA)	PN @1MHz (dBc/Hz)
00	1.1	11	-124
01	1.3	14	-125
10	1.9	20	-127.5
11	2.1	22	-128

5   I²C bus interface

The I²C bus interface is selected by hardware connection of the pin #21 (DBUS_SEL) to 0 V.

Data transmission from microprocessor to the STW81102 takes place through the 2 wires (SDA and SCL) I²C-BUS interface. The STW81102 is always a slave device.

The I²C-bus protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as receiver. The device that controls the data transfer is known as the Master and the others as the slave. The master will always initiate the transfer and will provide the serial clock for synchronization.

5.1   General features

5.1.1   Data validity

Data changes on the SDA line must only occur when the SCL is LOW. SDA transitions while the clock is HIGH are used to identify START or STOP condition.

Figure 20.   Data validity
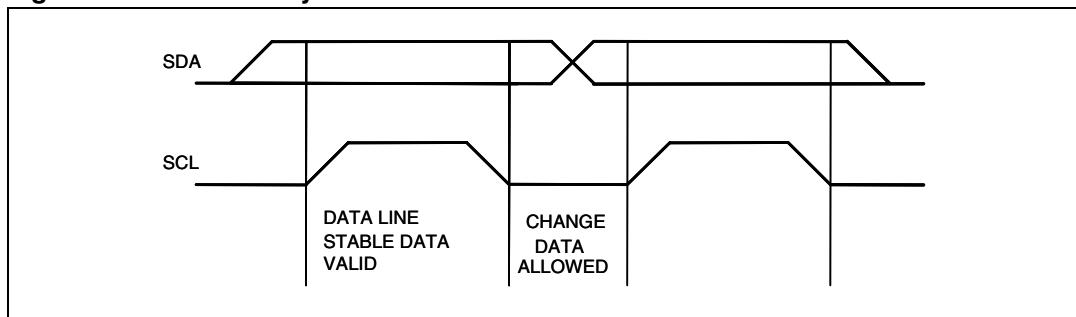
5.1.2   START condition

A Start condition is identified by a HIGH to LOW transition of the data bus SDA while the clock signal SCL is stable in the HIGH state. A Start condition must precede any command for data transfer.

5.1.3   STOP condition

A LOW to HIGH transition of the data bus SDA identifies stop while the clock signal SCL is stable in the HIGH state. A STOP condition terminates communications between the STW81102 and the Bus Master.

Figure 21.   Start and Stop condition
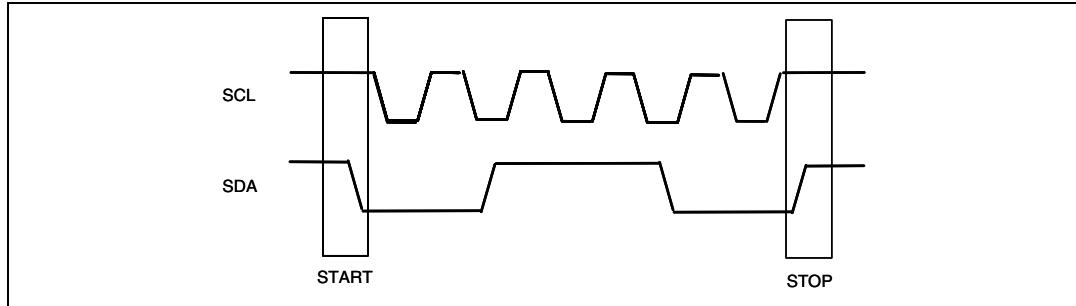
5.1.4   Byte format and acknowledge

Every byte transferred on the SDA line must contain bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA low to acknowledge the receipt of 8 bits data.

Figure 22.   Byte format and acknowledge
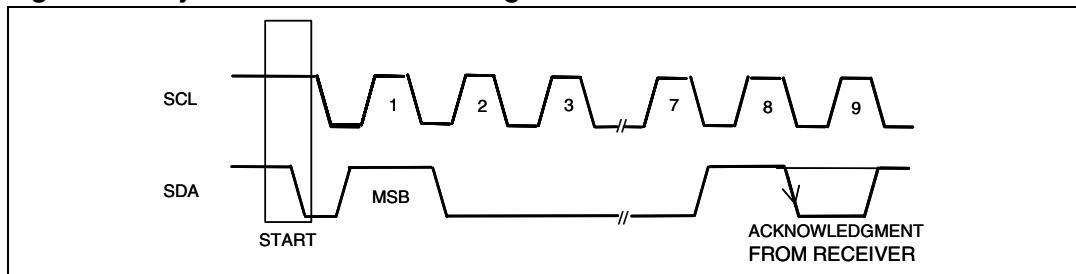
5.1.5   Device addressing

To start the communication between the Master and the STW81102, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The first 7 MSB's are the device address identifier, corresponding to the I²C-Bus definition. For the STW81102 the address is set as "$1100A_2A_1A_0$", 3bits programmable. The 8th bit (LSB) is the read or write operation bit (RW; set to 1 in read mode and to 0 in write mode).

After a START condition the STW81102 identifies on the bus the device address and, if matched, it will acknowledge the identification on SDA bus during the 9th clock pulse.

5.1.6   Single-byte write mode

Following a START condition the master sends a device select code with the RW bit set to 0. The STW81102 gives an acknowledge and waits for the internal sub-address (1 byte). This byte provides access to any of the internal registers.

After the reception of the sub-address internal byte the STW81102 again responds with an acknowledge. A single-byte write to sub-address 00H will change the "FUNCTIONAL_MODE" register, so a single-byte write with sub-address 04H will change the "CONTROL" register and so on.

Table 10.   Single-byte write mode

S	1100A$_2$A$_1$A$_0$	0	ack	sub-address byte	ack	DATA IN	ack	P

5.1.7   Multi-byte write mode

The multi-byte write mode can start from any internal address. The master sends the data bytes and each one is acknowledged. The master terminates the transfer by generating a STOP condition.

The sub-address decides the starting byte. A multi-byte with sub-address 01H and 2 DATA_IN bytes will change the "B_COUNTER" and "A_COUNTER" registers (01H,02H), so a multi-byte with sub-address 00H and and 6 DATA_IN bytes will change all the STW81102 registers.

Table 11.   Multi-byte write mode

S	1100A$_2$A$_1$A$_0$	0	ack	sub-address byte	ack	DATA IN	ack	....	DATA IN	ack	P

5.1.8   Current byte address read

In the current byte address read mode, following a START condition, the master sends the device address with the rw bit set to 1 (No sub-address is needed as there is only 1 byte read register). The STW81102 acknowledges this and outputs the data byte. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

Table 12.   Current Byte Address Read

S	1100 A$_2$ A$_1$ A$_0$	1	ack	DATA OUT	No ack	P

5.2   Timing specification

Figure 23.   Data and clock
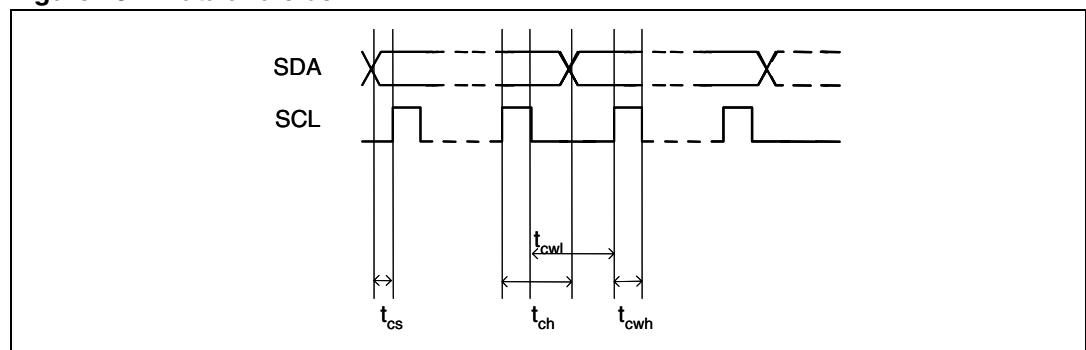
Table 13.   Data and clock

Symbol	Parameter	Minimum time (ns)
T$_{cs}$	Data to clock set up time	2
T$_{ch}$	Data to clock hold time	2
T$_{cwh}$	Clock pulse width high	10
T$_{cwl}$	Clock pulse width low	5

Figure 24.   Start and stop
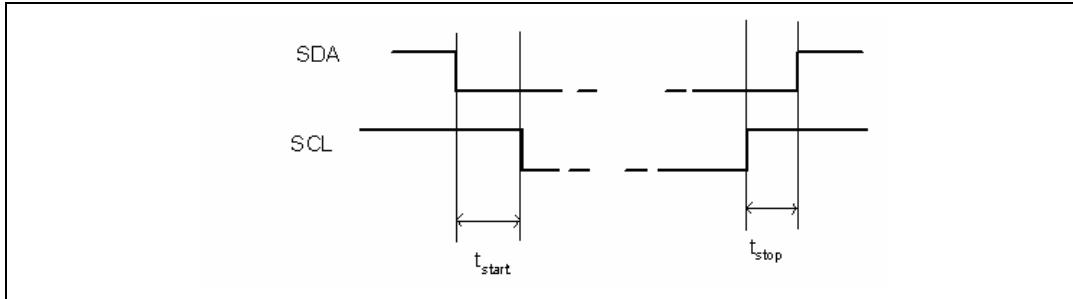
Table 14.   Start and stop

Symbol	Parameter	Minimum time (ns)
T_{start}	Clock to data start time	2
T_{stop}	Data to clock down stop time	2

Figure 25.   Acknowledge
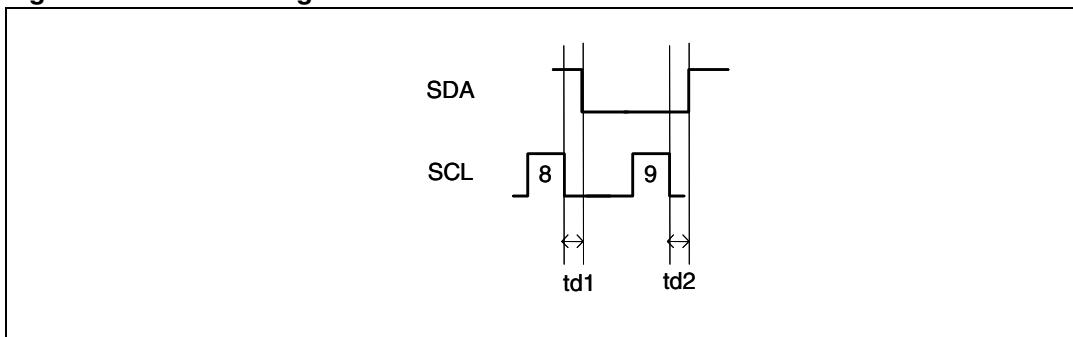
Table 15.   Acknowledge

Symbol	Parameter	Minimum time (ns)
T_{d1}	Ack begin delay	2
T_{d2}	Ack end delay	2

5.3 I²C registers

STW81102 has 6 write-only registers and 1 read-only register.

The following table gives a short description of the write-only registers list.

Table 16. Write-only registers list

HEX CODE	DEC CODE	DESCRIPTION
0x00	0	FUNCTIONAL_MODE
0x01	1	B_COUNTER
0x02	2	A_COUNTER
0x03	3	REF_DIVIDER
0x04	4	CONTROL
0x05	5	CALIBRATION

5.3.1 FUNCTIONAL_MODE

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
PD6	PD5	PD4	PD3	PD2	PD1	PD0	B11

FUNCTIONAL_MODE register is used to select different functional mode for the STW81102 synthesizer according to the following table:

Table 17. Different functional mode of the FUNCTIONAL_MODE register

Decimal value	Description
0	Power down mode
1	Enable VCO A, output frequency divided by 2
2	Enable VCO B, output frequency divided by 2
3	Enable external VCO, output frequency divided by 2
4	Enable VCO A, output frequency divided by 4
5	Enable VCO B, output frequency divided by 4
6	Enable external VCO, output frequency divided by 4
7	Enable VCO A, direct output
8	Enable VCO B, direct output
9	Enable external VCO, direct output

5.3.2 B_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B10	B9	B8	B7	B6	B5	B4	B3

B[10:3]. Counter value (bit B11 in the previous register, bits B[2:0] in the next register)

5.3.3 A_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B2	B1	B0	A4	A3	A2	A1	A0

Bits B[2:0] for B Counter, A Counter value.

5.3.4 REF_DIVIDER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R9	R8	R7	R6	R5	R4	R3	R2

Reference Clock divider ratio R[9:1] (bits R1, R0 in the next register).

5.3.5 CONTROL

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R1	R0	PLL_A1	PLL_A0	CP SEL2	CP SEL1	CP SEL0	PSC_SEL

The CONTROL register is used to set the Charge Pump current, the VCO output voltage amplitude and the Prescaler Modulus.

PLL_A[1:0]: VCO amplitude

CPSEL[2:0]: Charge Pump output current

PSC_SEL: Prescaler Modulus select ('0' for P=16, '1' for P=19)

The LO output frequency is programmed by setting the proper value for A,B and R according to the following formula:

$$F_{OUT} = D_R \cdot (B \cdot P + A) \cdot \frac{F_{REF\_CLK}}{R}$$

$$
\text{where } D_R \text{ equals }
\begin{cases}
1 & \text{for Direct Output} \\
0.5 & \text{for Output Divided by 2} \\
0.25 & \text{for Output Divided by 4}
\end{cases}
$$

and P is the selected Prescaler Modulus

5.3.6   CALIBRATION

MSB							**LSB**
b7	b6	b5	b4	b3	b2	b1	b0
INIT CAL	SER CAL	SEL EXT CAL	CAL4	CAL3	CAL2	CAL1	CAL0

This register controls VCO calibrator.

INITCAL: resets the auto-calibrator State Machine (writing to "1" and back to "0")

SERCAL: at "1" starts the VCO auto-calibration (should be reset to "0" at the end of calibration)

SELEXTCAL: test purpose only; must be set to '0'

CAL[4:0]:   test purpose only; must be set to '0'

5.3.7   READ-ONLY register

MSB							**LSB**
b7	b6	b5	b4	b3	b2	b1	b0
DEV_ID1	DEV_ID0	LOCK_ DET	INT CAL4	INT CAL3	INT CAL2	INT CAL1	INT CAL0

This register is automatically addressed in the 'current byte address read mode'.

DEV_ID[1:0]:   device identifier bits; returns '00'

LOCK_DET: "1" when PLL is locked

INTCAL[4:0]:   internal value of the VCO control word

5.3.8   Default configuration

At Power On Reset the following configuration is automatically loaded:

– FUNCTIONAL MODE = 1 (VCOA with divided by 2 output)
– A COUNTER = 8
– B COUNTER = 562
– R DIVIDER = 192
– PLL_A[1:0] = [10]
– CP_SEL[2:0] = [111]
– PSC_MOD_SEL set to "0" (Modulus = 16)

This is corresponding to an output frequency of 1800MHz and a PFD frequency of 400KHz using a 76.8MHz reference clock (calibration algorithm of the VCO is automatically started).

5.4   VCO calibration procedure

The calibration of the VCO center frequency is activated by a '0' to '1' transition of the SERCAL bit (CALIBRATION Register bit[6]).

In order to program properly the device, ensuring the VCO calibration, the following procedure is required before every channel change:

   a)   Reset the "CALIBRATION" Register using a single-byte write sequence (sub-address 05H) with all the bits set to '0'

   b)   Program all the Registers using a multi-byte write sequence with the desired settings (Functional Mode, B and A counters, R counter, VCO amplitude, Charge Pump, Prescaler Modulus) and the SERCAL bit of the "CALIBRATION" Register (05H) set to '1'

The maximum allowed PFD frequency (f_{PFD}) to perform the calibration process is 1 MHz; if the desired f_{PFD} is higher than 1MHz the following steps are needed:

   –   Perform all the steps of the calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that f_{PFD} is $\leq$ 1MHz.

   –   Program the device with the proper setting for the desired VCO and PFD frequencies according to the above step b) only.

6   SPI digital interface

6.1   General features

The SPI digital interface is selected by hardware connection of the pin #21 (DBUS_SEL) to 3.3V.

The STW81102 IC is programmed by means of a high-speed serial-to-parallel interface with write option only. The 3-wires bus can be clocked at a frequency as high as 100MHz to allow fast programming of the registers containing the data for RF IC configuration.

The programming of the chip is done through serial words with whole length of 26 bits. The first 2 MSB represent the address of the registers. The others 24 LSB represent the value of the registers.

Each Data bit is stored in the internal shift register on the **rising edge** of the CLOCK signal.

On the **rising edge** of the LOAD signal the outputs of the selected register are sent to the device.

Figure 26.   SPI input and output bit order
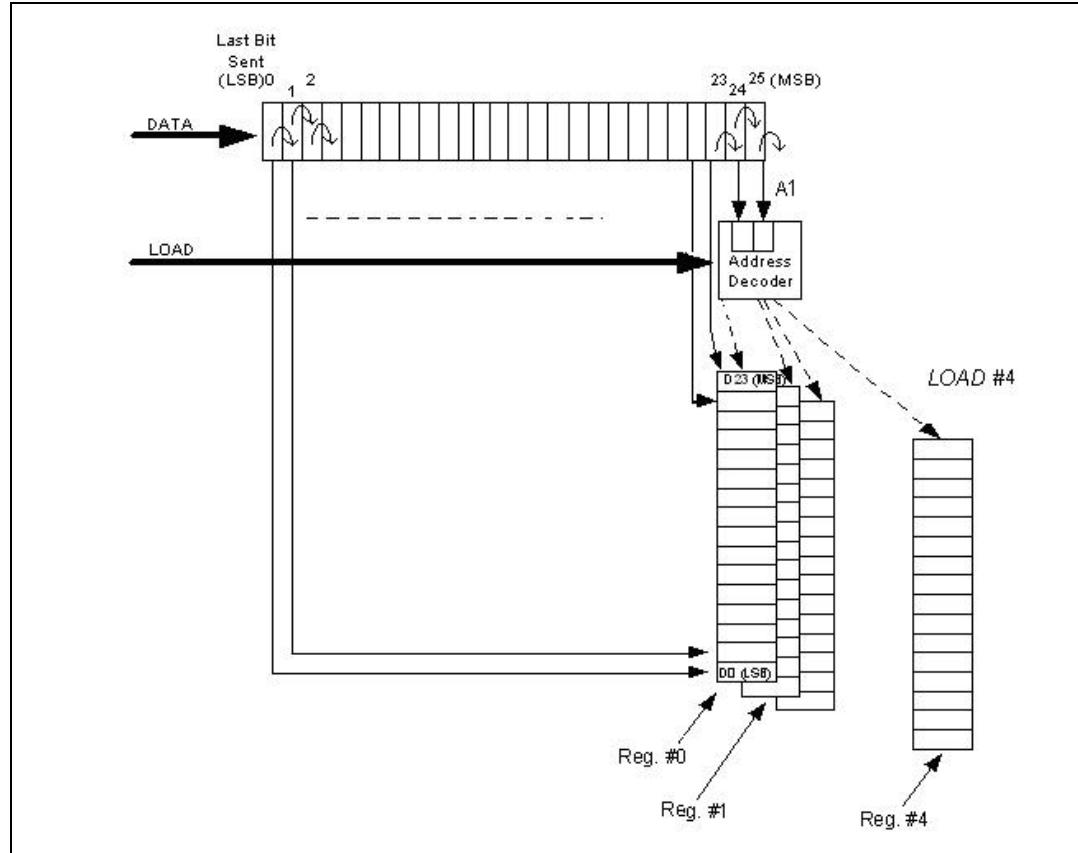
Table 18.   SPI data structure

MSB   **LSB**

Address		Data for Register (24 bits)																							
A1	A0	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 19.   Address decoder and outputs

Address		Outputs			
A1	**A0**	**DATABITS D23-D0**	**No**	**Name**	**Function**
0	0	24	0	ST1	Reference divider, VCO amplitude, VCO Calibration, Charge Pump current, Prescaler Modulus
0	1	24	1	ST2	Functional modes, VCO dividers
1	0	24	2	ST3	Reserved
1	1	24	3	ST4	Reserved

6.2   Timing specification

Figure 27.   SPI Timing specification
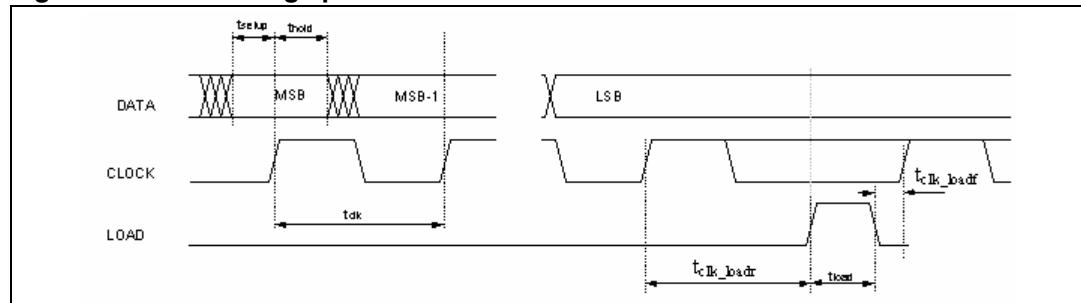
Table 20.   SPI Timing specification

Parameter	Description	Min.	Typ.	Max.	Unit
tsetup	DATA to CLOCK setup time	0.8			ns
thold	DATA to clock hold time	0.2			ns
tclk	CLOCK cycle period	10			ns
tload	LOAD pulse width	3			ns
tclk_loadr	CLOCK to LOAD rising edge	2			ns
tclk_loadf	CLOCK to LOAD falling edge	0.5			ns

6.3 Bits table

Table 21. Bits (Serial Interface Address = 00h; Register name = ST1)

Bit	Name	Description
[23]	R9	REFERENCE CLOCK DIVIDER RATIO
[22]	R8	
[21]	R7	
[20]	R6	
[19]	R5	
[18]	R4	
[17]	R3	
[16]	R2	
[15]	R1	
[14]	R0	
[13]	PLL_A1	VCO Amplitude Control
[12]	PLL_A0	
[11]	CPSEL2	Charge Pump output current Control
[10]	CPSEL1	
[9]	CPSEL0	
[8]	PSC_SEL	Prescaler Modulus select ('0' for P=16, '1' for P=19)
[7]	INITCAL	test purpose only; must be set to '0'
[6]	SERCAL	Enable VCO calibration (see *Section 6.4*)
[5]	SELEXTCAL	test purpose only; must be set to '0'
[4]	CAL4	test purpose only; must be set to '0'
[3]	CAL3	
[2]	CAL2	
[1]	CAL1	
[0]	CAL0	

Table 22.   Bits (Serial Interface Address = 01h; Register name = ST2)

Bit	Name	Description
[23]	PD6	DEVICE FUNCTIONAL MODES
[22]	PD5	0. Power down
[21]	PD4	1. Enable VCO A, output frequency divided by 2 2. Enable VCO B, output frequency divided by 2
[20]	PD3	3. Enable external VCO, output frequency divided by 2
[19]	PD2	4. Enable VCO A, output frequency divided by 4
[18]	PD1	5. Enable VCO B, output frequency divided by 4 6. Enable external VCO, output frequency divided by 4
[17]	PD0	7. Enable VCO A, direct output 8. Enable VCO B, direct output 9. Enable external VCO, direct output
[16]	B11	B Counter Bits
[15]	B10	
[14]	B9	
[13]	B8	
[12]	B7	
[11]	B6	
[10]	B5	
[9]	B4	
[8]	B3	
[7]	B2	
[6]	B1	
[5]	B0	
[4]	A4	A Counter Bits
[3]	A3	
[2]	A2	
[1]	A1	
[0]	A0	

The LO output frequency is programmed by setting the proper value for A,B and R according to the following formula:

$$F_{OUT} = D_R \cdot (B \cdot P + A) \cdot \frac{F_{REF\_CLK}}{R}$$

where D_R equals $\begin{cases} 1 & \text{for Direct Output} \\ 0.5 & \text{for Output Divided by 2} \\ 0.25 & \text{for Output Divided by 4} \end{cases}$

and P is the selected Prescaler Modulus

6.3.1 Default configuration

At Power On Reset the following configuration is automatically loaded:

– FUNCTIONAL MODE = 1 (VCOA with divided by 2 output)
– A COUNTER = 8
– B COUNTER = 562
– R DIVIDER = 192
– PLL_A[1:0] = [10]
– CP_SEL[2:0] = [111]
– PSC_MOD_SEL set to "0" (Modulus = 16)

This is corresponding to an output frequency of 1800MHz and a PFD frequency of 400KHz using a 76.8MHz reference clock (calibration algorithm of the VCO is automatically started).

6.4 VCO calibration procedure

The calibration of the VCO center frequency is activated by a '0' to '1' transition of the SERCAL bit (ST1 Register bit[6]).

In order to program properly the device, ensuring the VCO calibration, the following procedure is required before every channel change:

a) Program the ST1 Register with the desired settings (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) and SERCAL bit set to '0'

b) Program the ST2 Register with the desired settings (Functional mode, B and A counters)

c) Program the ST1 Register with the desired settings (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) and SERCAL bit set to '1'

The maximum allowed PFD frequency (f_{PFD}) to perform the calibration process is 1 MHz; if the desired f_{PFD} is higher than 1MHz the following steps are needed:

– Perform all the steps of the calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that f_{PFD} is $\leq$ 1MHz.

– Program the device with the proper setting for the desired VCO and PFD frequencies according to the above step a) and b) only.

7   Application information

The STW81102 features three different alternatively selectable bands: direct output (3.0 to 3.62GHz and 4.0 to 4.65GHz), divided by 2 (1.5 to 1.81GHz and 2.0 to 2.325GHz) and divided by 4 (750 to 905MHz and 1000 to 1162.5MHz). In order to achieve a suitable power level, a good matching network is needed to adapt the output stage to a 50Ω load. Moreover, since most of commercial RF components have single ended input and output terminations, a differential to single ended conversion could be required.

Below different matching configurations for the three bands are suggested as a guideline for the design of own application board.

The user can find in the Evaluation Kit the ADS Design for each matching configuration suggested in this section. The name of the corresponding ADS Design is reported in each figure.

The ADS designs provide only a first indication of the output stage matching and they should be reworked according to the user choice for layout, board substrate, components and so on.

The ADS designs of the Evaluation Boards are provided with a complete electromagnetic modelling (board, components, ...).

7.1   Direct Output

If a differential to single conversion is not needed it is possible to match the output buffer of the STW81102 in the simple way shown in *Figure 28*.

Figure 28.   Differential/single ended output network in the 3.0 - 4.65GHz range (MATCH_LC_LUMP_4G_DIFF.dsn)
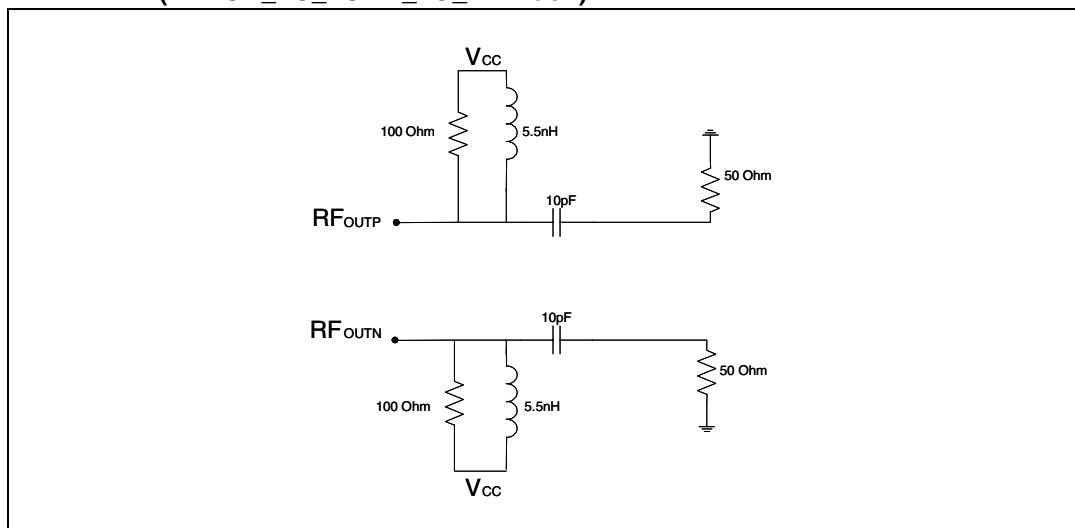
Since most of discrete components for microwave applications are single ended, the user can easily use one of the two outputs and terminate the other one to 50Ω with a 3dB power loss.

Alternatively it is possible to combine the 2 outputs in different ways. A first topology for the direct output (3GHz to 4.65GHz) is suggested in *Figure 29*. It basically consists of a simple LC balun and a matching network to adapt the output to a 50Ω load. The two LC networks shift output signal phase of -90° and +90° thus combining the 2 outputs. This topology, designed for a center frequency of 4GHz, is intrinsically narrow band, since the LC balun is tuned at a single frequency. If the application requires a different sub-band, the LC combiner could be easily adjusted to be tuned at the frequency of interest.

Figure 29.   LC lumped balun and matching network (MATCH_LC_LUMP_4G.dsn)
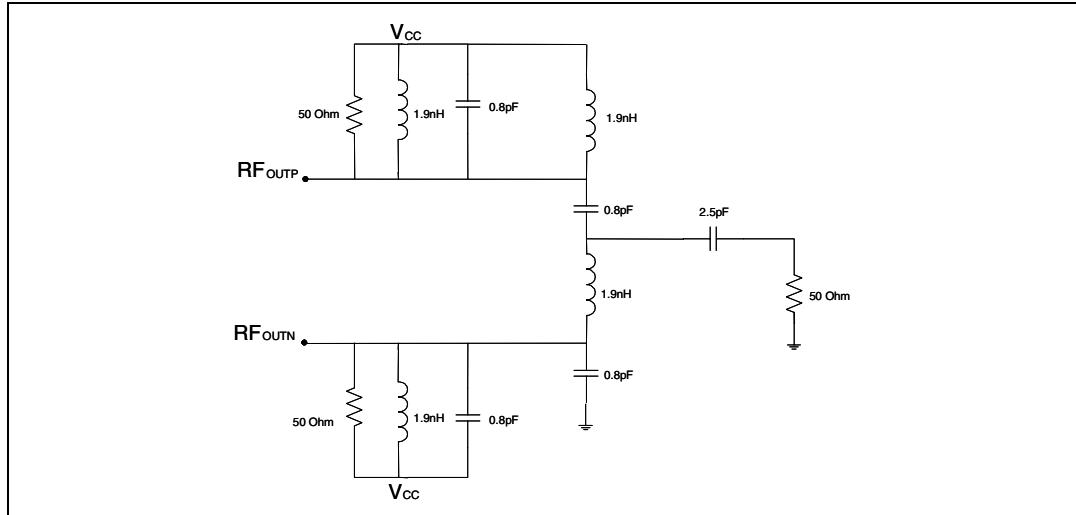
The 1.9nH shunt inductor works as a DC feed for one of the open collector terminal as well as a matching element along with the other components. The 1.9nH series inductors are used to resonate the parasitic capacitance of the chip.

For an optimum output matching it is recommended to use 0402 Murata or AVX capacitors and 0403 or 0604 HQ Coilcraft inductors. It is also advisable to use short interconnection paths to minimize losses and undesired impedance shift.

An alternative topology, which allows for a more broadband matching and balanced to unbalanced conversion, is shown it *Figure 30*.

Figure 30.   Evaluation Board (EVB4G) matching network (MATCH_EVB4G.dsn)
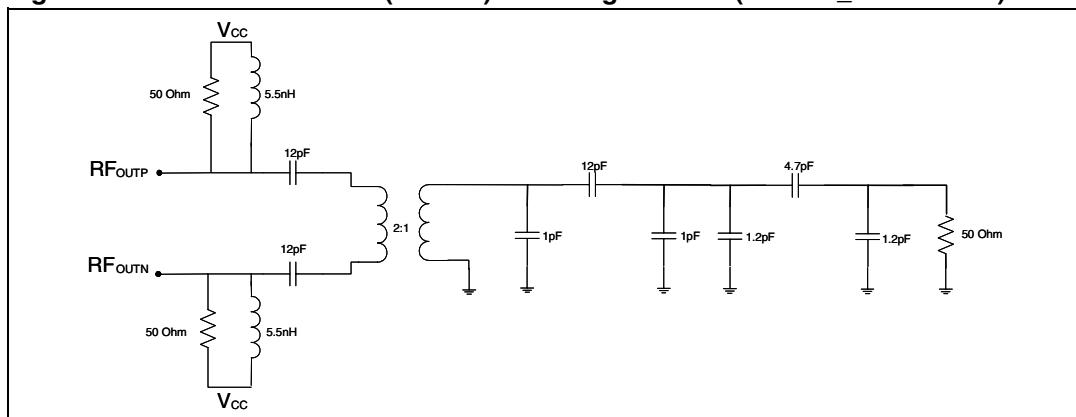
For the differential to single conversion the 50 to 100Ω Johanson balun is recommended (3700BL15B100).

7.2 Divided by 2 Output

If the user's application does not require a balanced to unbalanced conversion, the output matching reduces to the simple circuit shown below (*Figure 31*).

This solution can be easily used to provide one single ended output just terminating the other output at 50Ω with a 3dB power loss.

Figure 31. Differential/single ended output network in the 1.5 - 2.325GHz range (MATCH_LC_LUMP_2G_DIFF.dsn)
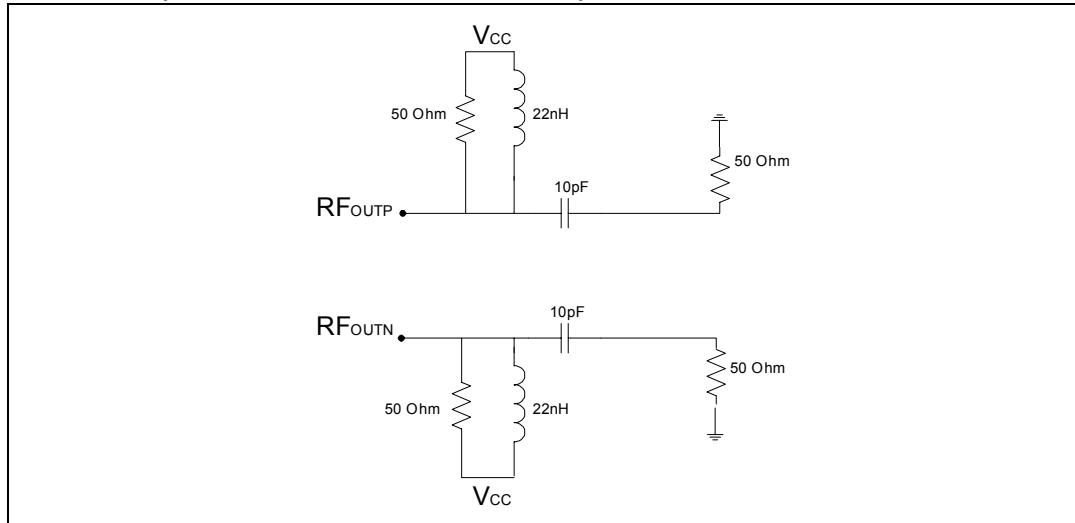
A first solution to combine the differential outputs is the lumped LC type balun tuned in the 2GHz band (*Figure 32*).

Figure 32. LC lumped balun for divided by 2 output (MATCH_LC_LUMP_2G.dsn)
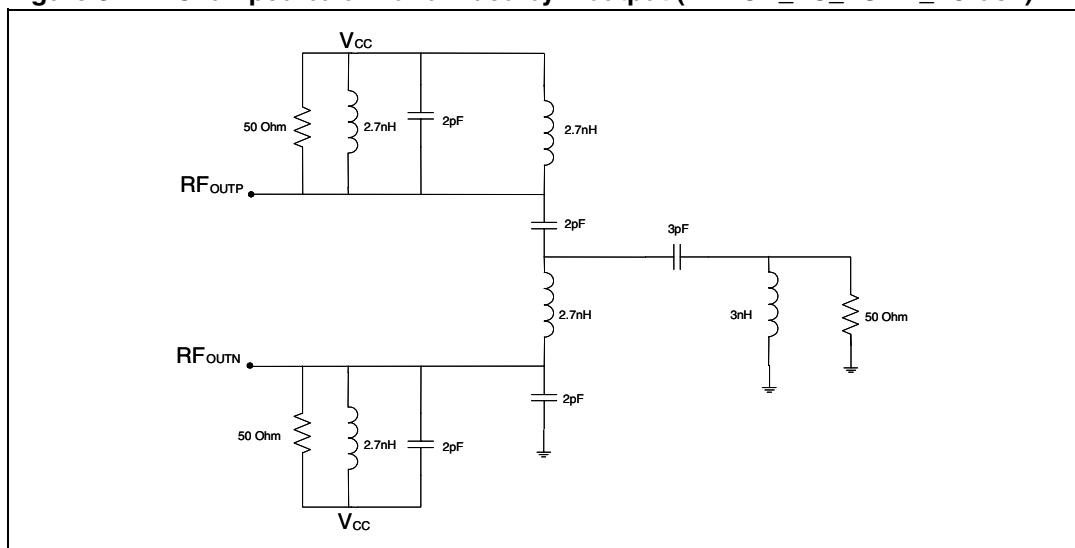
The same recommendation for the SMD components applies also for the divided by 2 output.

Another topology suitable to combine the two outputs for the divided by 2 frequencies is represented in *Figure 33*.

Figure 33.   Evaluation Board (EVB2G) matching network (MATCH_EVB2G.dsn)
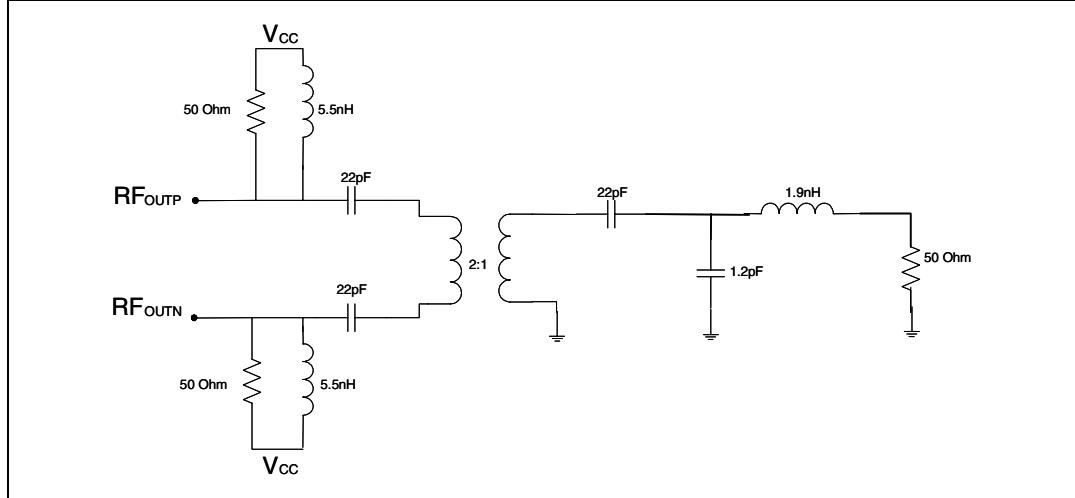
For the differential to single conversion the 50 to 100Ω Johanson balun (1600BL15B100) is recommended.

7.3   Divided by 4 Output

The same topology, components values and considerations of *Figure 31*, applies also for the divided by 4 output (MATCH_LC_LUMP_1G_DIFF.dsn).

As for the previous sections, a solution to combine the differential outputs is the lumped LC type balun tuned in the 1GHz band (*Figure 34*).

Figure 34.   LC lumped balun for the divided by 4 output (MATCH_LC_LUMP_1G.dsn)
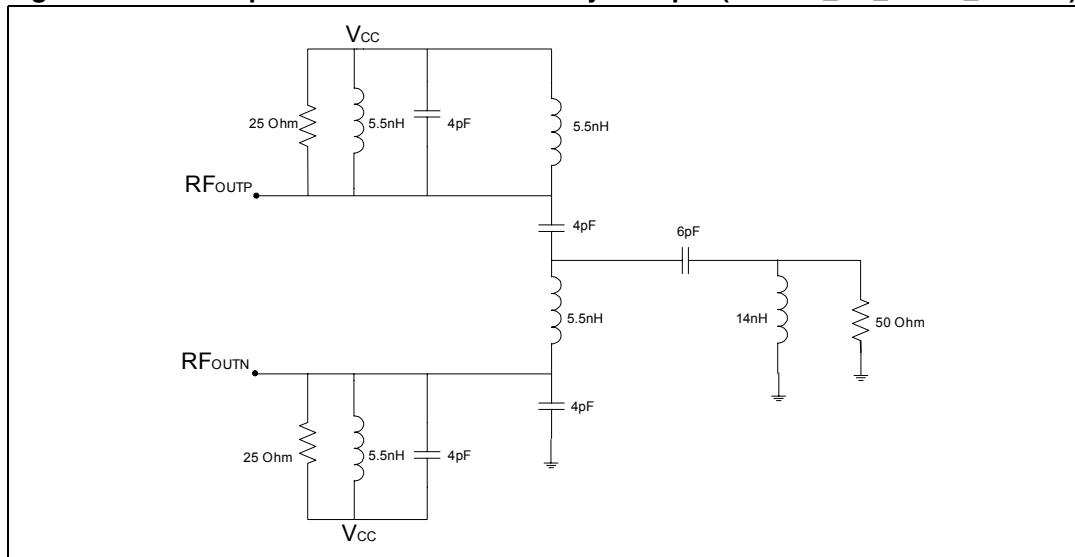
If the user prefers to use an RF balun it is possible to adopt the same topology depicted in *Figure 33*, just changing the balun and the matching components (*Figure 35*). The suggested balun for the 0.75 - 1.17GHz frequency range is the 1:1 Johanson 900BL15C050.

Figure 35.   Evaluation Board (EVB1G) matching network (MATCH_EVB1G.dsn)
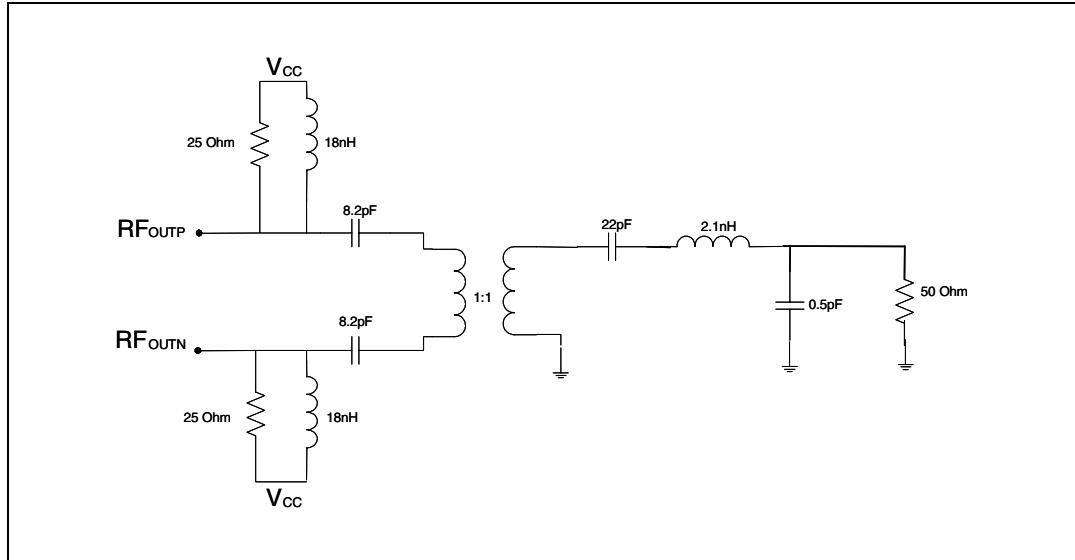
7.4   Evaluation Kit

Upon request an Evaluation Kit can be delivered. It includes:

●   Evaluation Board

●   GUI (Graphical User Interface) to program the device

●   Measured S parameters of the RF output

●   ADS2005 schematics providing guidelines for application board design

●   STWPLLSim software for PLL loop filter design and noise simulation

Three different Evaluation Kits are available, one optimized for 1GHz frequency range, one for 2GHz frequency range and the last one for 4GHz range.

While ordering please specify the following order codes:

Table 23.   Order code of the evaluation kit

Part Number	Description
STW81102-EVB1G	1GHz frequency range - Divider by 4 output optimized
STW81102-EVB2G	2GHz frequency range - Divider by 2 output optimized
STW81102-EVB4G	4GHz frequency range - Direct output optimized

The three Evaluation Kits differ only for the output stage network and can be adapted from one frequency band variant to a different one replacing properly the macthing components and the balun.

8 Application diagram

Figure 36. Application diagram
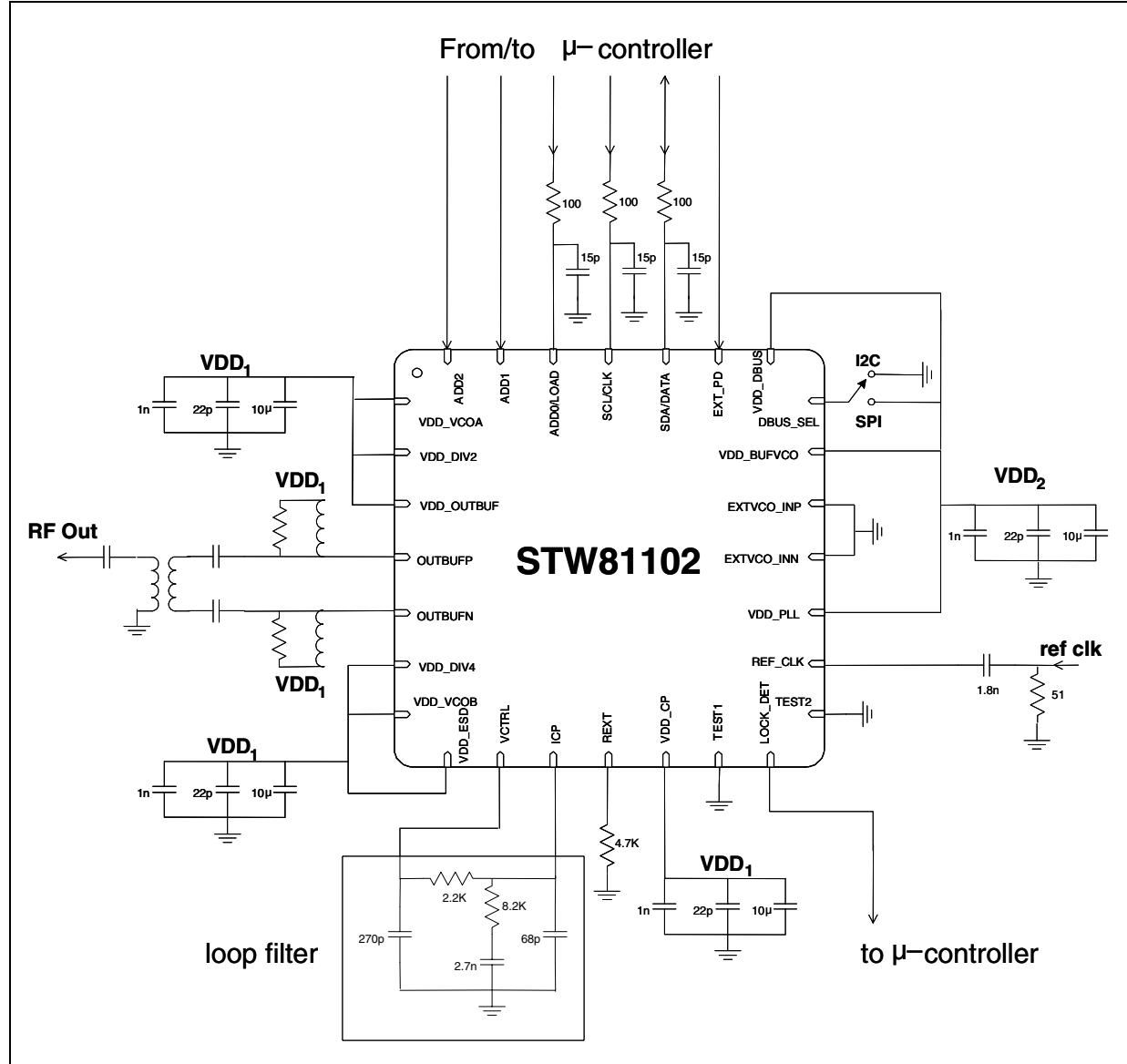
Note: 1 *See Application Information (Section 7) for further information on Output Matching topology.*

2 *EXT_PD, ADD2, ADD1 (and ADD0 when I^2C Bus is selected) can be hard wired directly on the board.*

3 *Loop Filter values are for 200KHz frequency step.*

9   Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: http://www.st.com.

Figure 37.   VFQFPN28 Mechanical Data & Package Dimensions

| REF.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	0.031	0.035	0.039
A1		0.020	0.050		0.0008	0.0019
A2		0.650	1.000		0.025	0.039
A3		0.200			0.0078	
b	0.180	0.250	0.300	0.007	0.0098	0.012
D	4.850	5.000	5.150	0.191	0.197	0.203
D1		4.750			0.187	
D2	2.950	3.100	3.250	0.116	0.122	0.128
E	4.850	5.000	5.150	0.191	0.197	0.203
E1		4.750			0.187	
E2	2.950	3.100	3.250	0.116	0.122	0.128
e		0.500			0.020	
L	0.350	0.550	0.750	0.014	0.022	0.029
P			0.60			0.0236
K			14°			14°
ddd			0.080			0.003

Notes: 1) VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Packages No lead.
Very thin: A = 1.00 Max.
2) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
Exact shape and size of this feature is optional.

OUTLINE AND MECHANICAL DATA
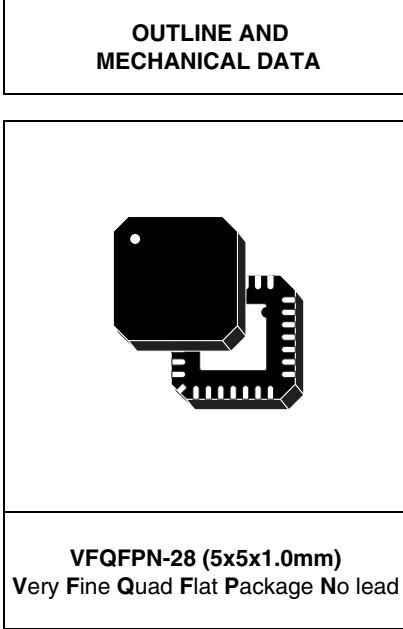
VFQFPN-28 (5x5x1.0mm)
Very **F**ine **Q**uad **F**lat **P**ackage **N**o lead
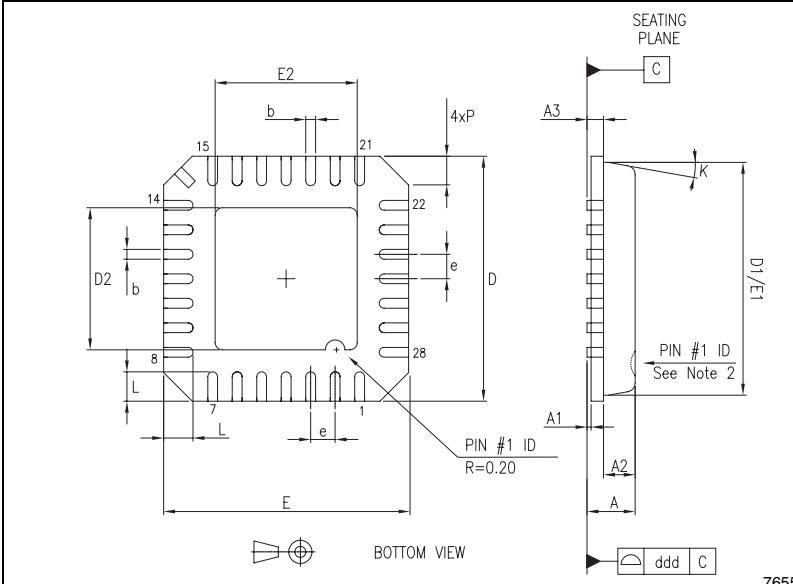
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10 Revision history

Table 24.   Document revision history

Date	Revision	Changes
06-Mar-2006	1	Initial release.
16-Jun-2006	2	Changed from preliminary data to maturity. Updated *Section 2: Electrical specifications*; *Section 7: Application information* and *Section 8: Application diagram*.

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