

N-channel 800 V, 0.07 Ω typ., 46 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

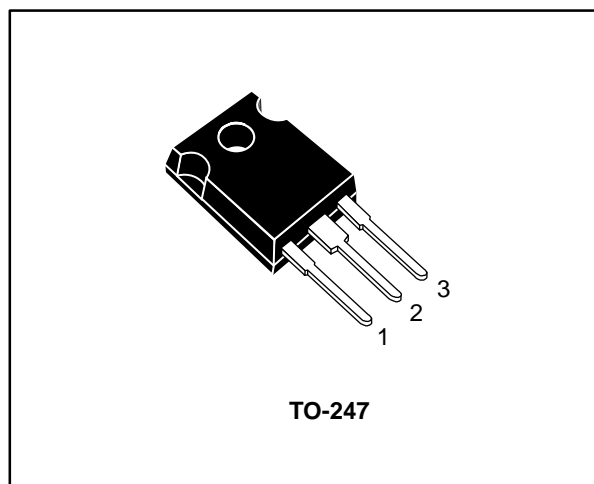
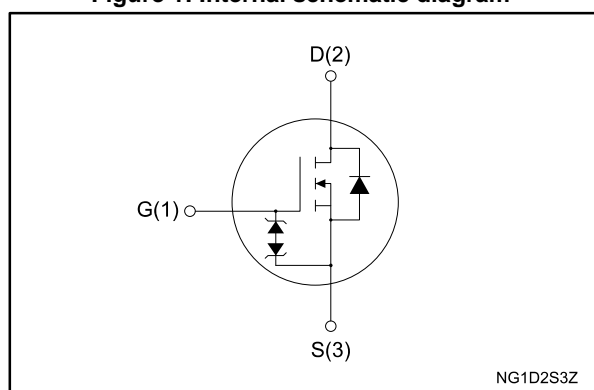


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STW65N80K5	800 V	0.08 Ω	46 A	446 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW65N80K5	65N80K5	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±30	V
I _D	Drain current (continuous) at T _{case} = 25 °C	46	A
	Drain current (continuous) at T _{case} = 100 °C	30	
I _{DM} ⁽¹⁾	Drain current (pulsed)	184	A
P _{TOT}	Total dissipation at T _{case} = 25 °C	446	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Operating junction temperature		

Notes:

- (1) Pulse width is limited by safe operating area.
 (2) I_{SD} ≤ 46 A, di/dt=100 A/μs; V_{DS} peak < V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}.
 (3) V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.28	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR} ⁽¹⁾	Avalanche current, repetitive or not repetitive	16	A
E _{AS} ⁽²⁾	Single pulse avalanche energy	700	mJ

Notes:

- (1) Pulse width limited by T_{jmax}.
 (2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 800\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 800\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			50	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 23\text{ A}$		0.07	0.08	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	3230	-	μF
C_{oss}	Output capacitance		-	310	-	
C_{rss}	Reverse transfer capacitance		-	3	-	
$C_{\text{oss(eq)}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }640\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	734	-	μF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	1.9	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 640\text{ V}$, $I_{\text{D}} = 46\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14 : "Test circuit for gate charge behavior")	-	92	-	nC
Q_{gs}	Gate-source charge		-	18	-	
Q_{gd}	Gate-drain charge		-	65	-	

Notes:

⁽¹⁾ $C_{\text{oss(eq)}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 400\text{ V}$, $I_{\text{D}} = 23\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13 : "Test circuit for resistive load switching times" and Figure 18 : "Switching time waveform")	-	34	-	ns
t_{r}	Rise time		-	30	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	90	-	
t_{f}	Fall time		-	10	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		46	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		184	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 46\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 46\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	650		ns
Q_{rr}	Reverse recovery charge		-	20		μC
I_{RRM}	Reverse recovery current		-	60		A
t_{rr}	Reverse recovery time	$I_{SD} = 46\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	845		ns
Q_{rr}	Reverse recovery charge		-	28		μC
I_{RRM}	Reverse recovery current		-	66		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

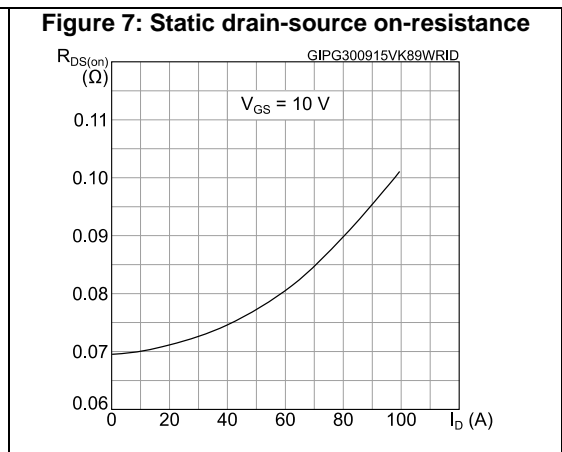
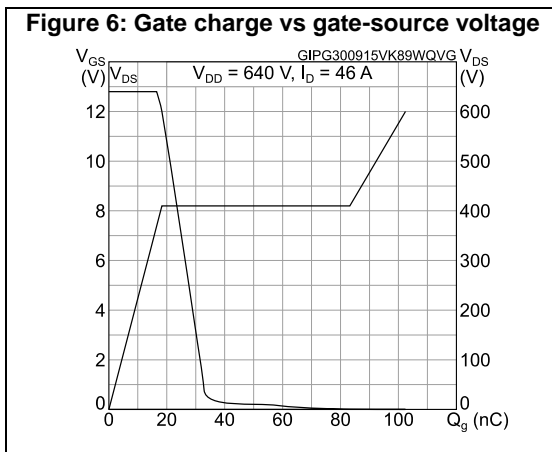
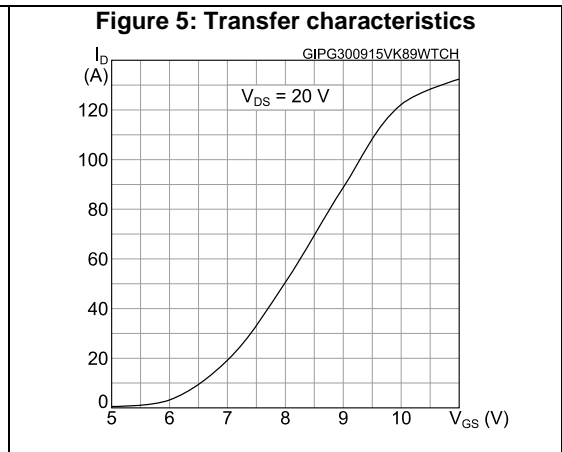
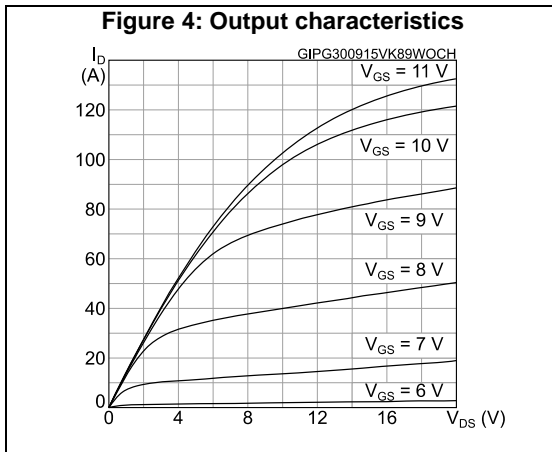
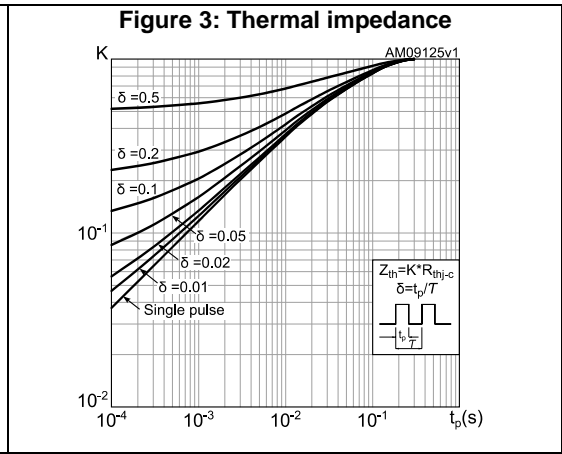
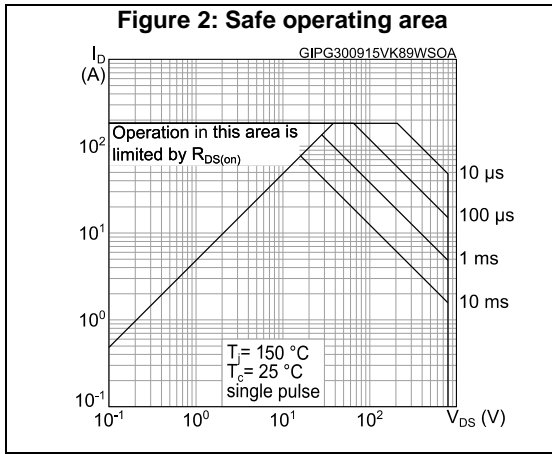


Figure 8: Capacitance variations

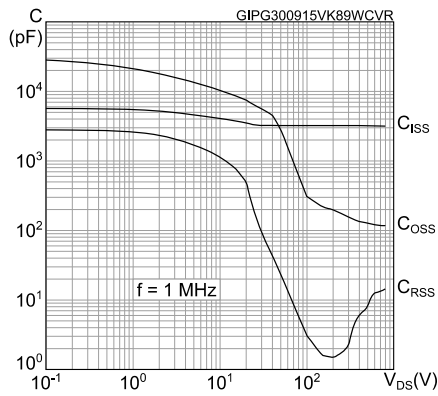


Figure 9: Normalized gate threshold voltage vs temperature

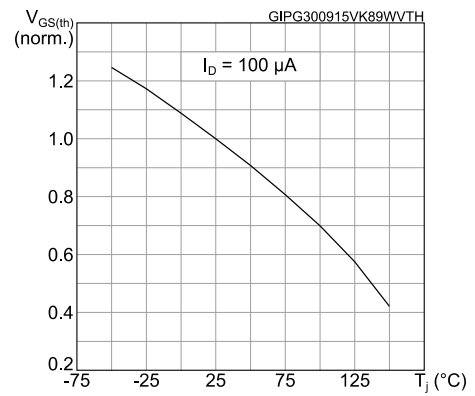


Figure 10: Normalized on-resistance vs temperature

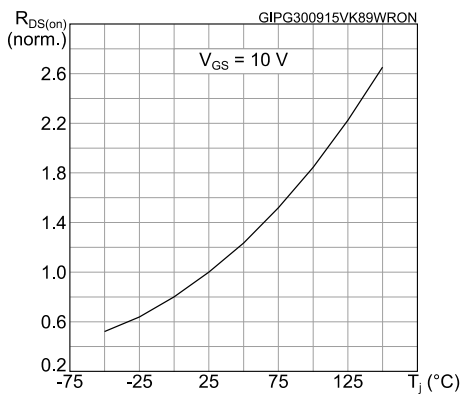


Figure 11: Normalized V(BR)DSS vs temperature

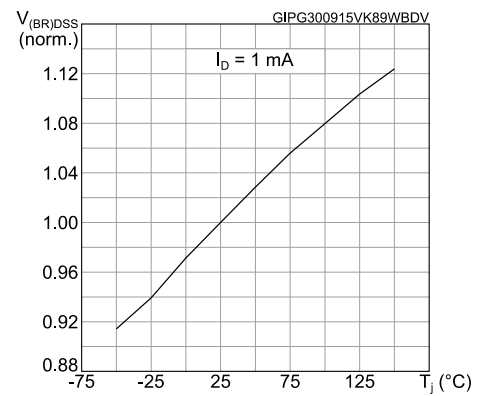
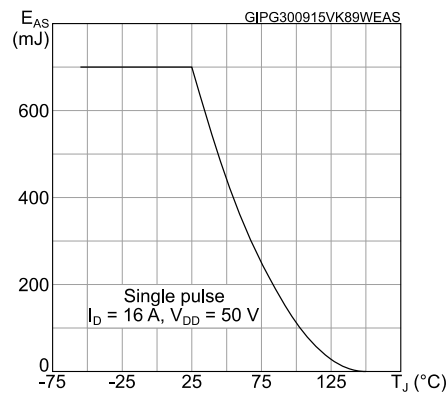
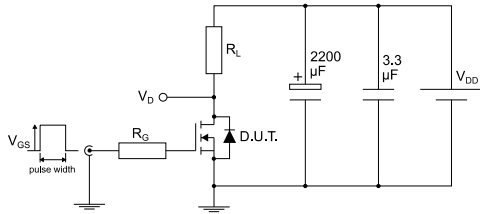


Figure 12: Maximum avalanche energy vs temperature



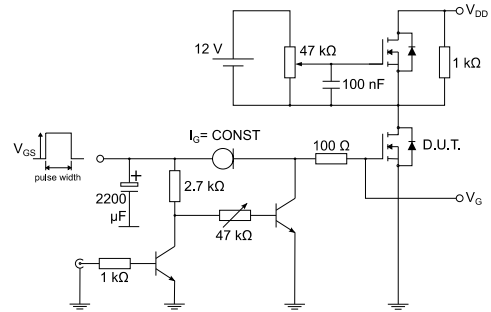
3 Test circuits

Figure 13: Test circuit for resistive load switching times



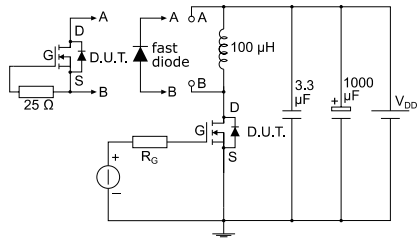
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Figure 14: Test circuit for gate charge behavior



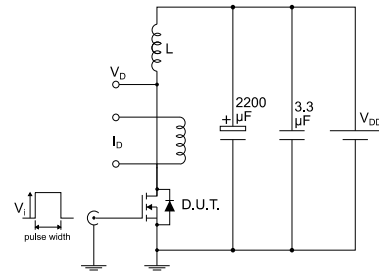
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Figure 15: Test circuit for inductive load switching and diode recovery times



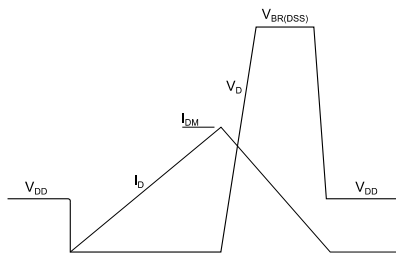
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Figure 16: Unclamped inductive load test circuit



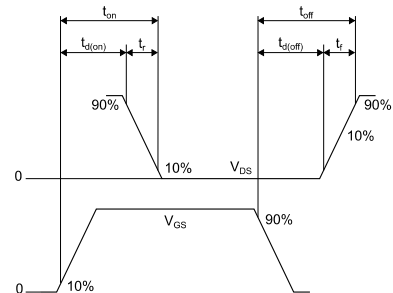
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19: TO-247 package outline

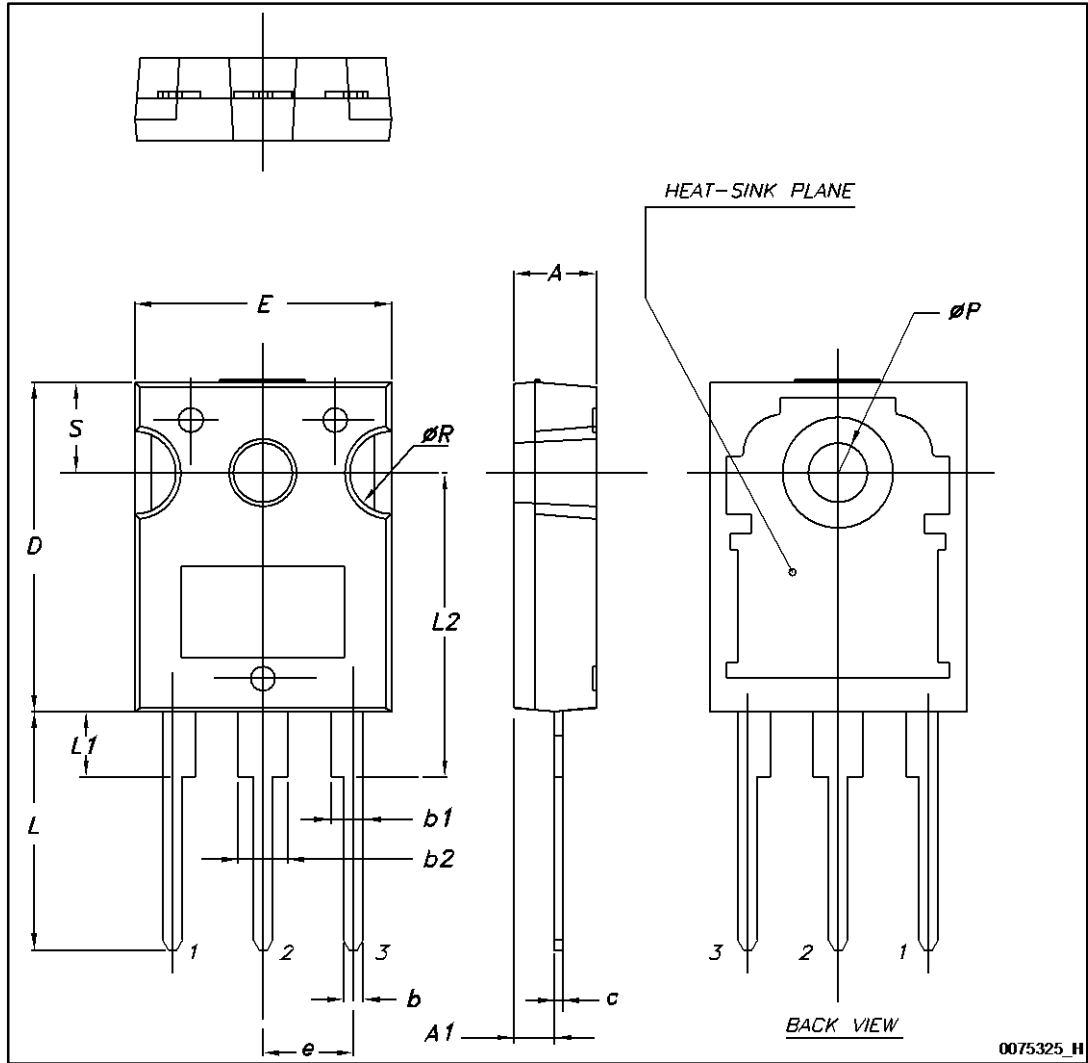


Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-May-2015	1	First release.
02-Oct-2015	2	Text and formatting changes throughout document. Datasheet status promoted from preliminary to production data. On cover page: - updated title description and Features table. Updated sections - Electrical ratings and Electrical characteristics. Added section - Electrical characteristics (curves).

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