

## N-channel 600 V, 0.045 $\Omega$ typ., 52 A MDmesh™ M2 Power MOSFET in a TO-247 package

Datasheet - production data

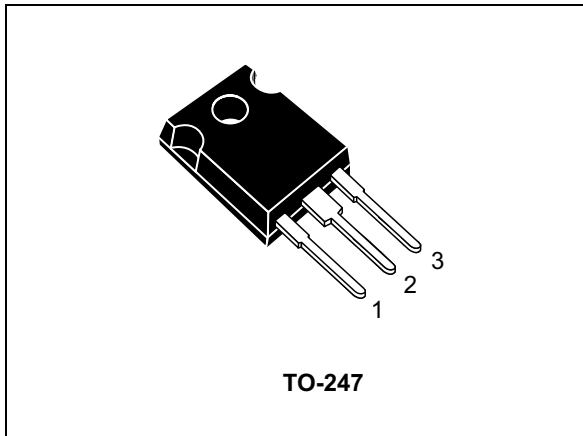
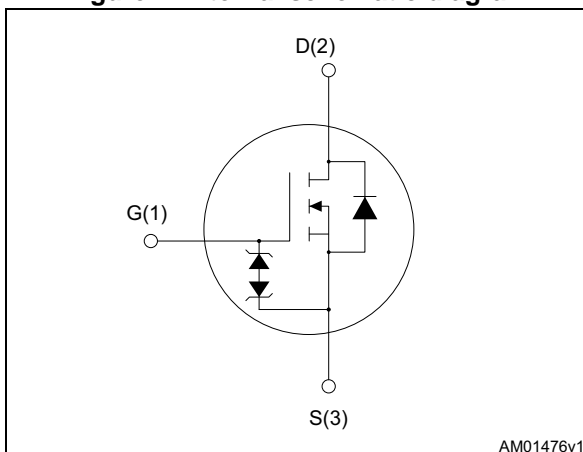


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STW56N60M2	650 V	0.055 $\Omega$	52 A

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STW56N60M2	56N60M2	TO-247	Tube

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	52	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	33	A
$I_{DM}^{(1)}$	Drain current (pulsed)	208	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	350	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 52\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max	0.36	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$ )	7.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	1100	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 10$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 26\text{ A}$		0.045	0.055	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	3750	-	pF
$C_{oss}$	Output capacitance		-	175	-	pF
$C_{rss}$	Reverse transfer capacitance		-	6.6	-	pF
$C_{o(er)}^{(1)}$	Equivalent Output Capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	740	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 52\text{ A}$ , $V_{GS} = 10\text{ V}$ , (see <a href="#">Figure 15</a> )	-	91	-	nC
$Q_{gs}$	Gate-source charge		-	13.5	-	nC
$Q_{gd}$	Gate-drain charge		-	41	-	nC

1.  $C_{oss}$  eq. is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 26\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> and <a href="#">Figure 19</a> )	-	18	-	ns
$t_r$	Rise time		-	26.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	119	-	ns
$t_f$	Fall time		-	14	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		52	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		208	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 52\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 52\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	496		ns
$Q_{rr}$	Reverse recovery charge		-	10		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	41		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 52\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	632		ns
$Q_{rr}$	Reverse recovery charge		-	14		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	45		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

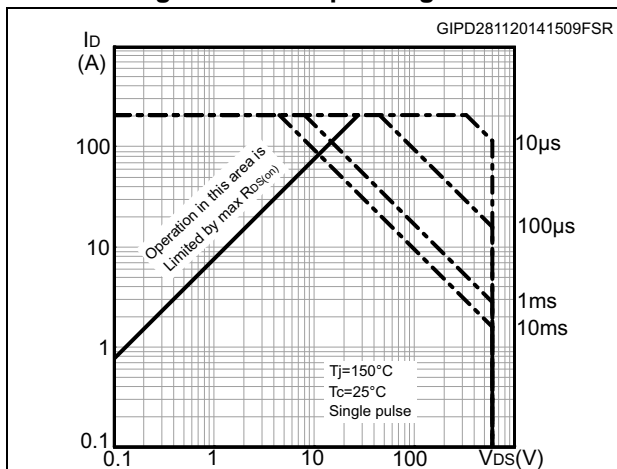


Figure 3. Thermal impedance

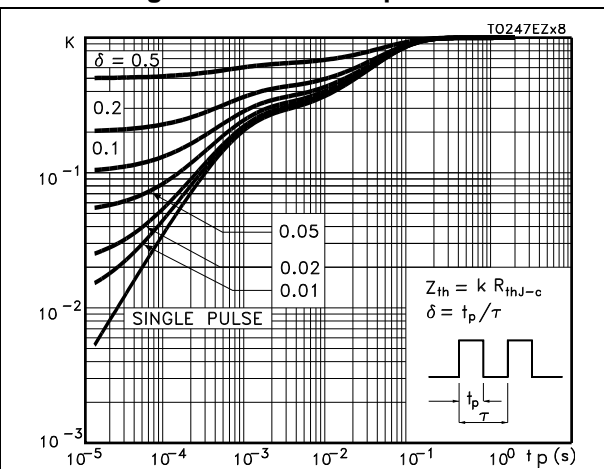


Figure 4. Output characteristics

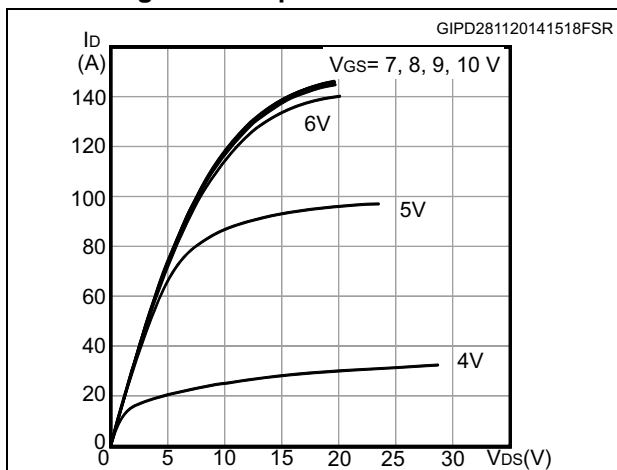


Figure 5. Transfer characteristics

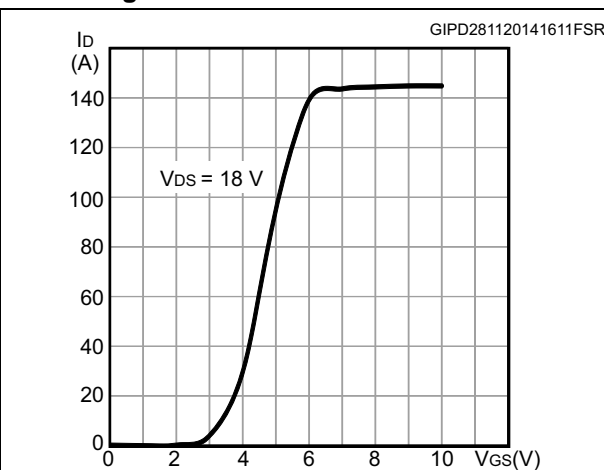


Figure 6. Normalized gate threshold voltage vs. temperature

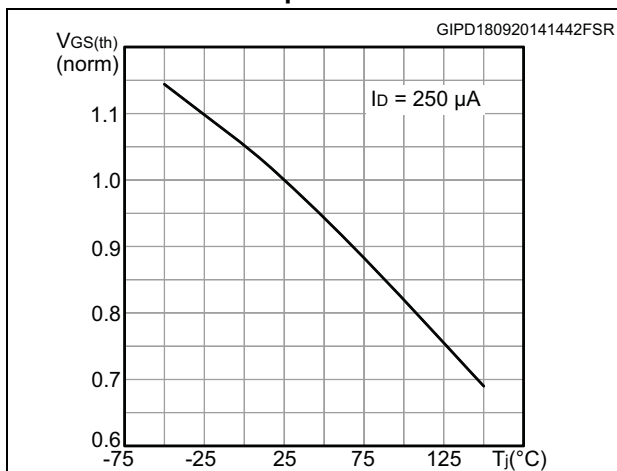


Figure 7. Normalized  $V_{(BR)DSS}$  vs. temperature

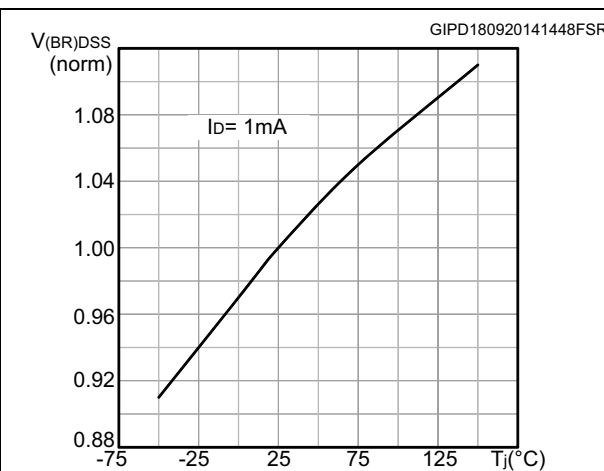


Figure 8. Static drain-source on-resistance

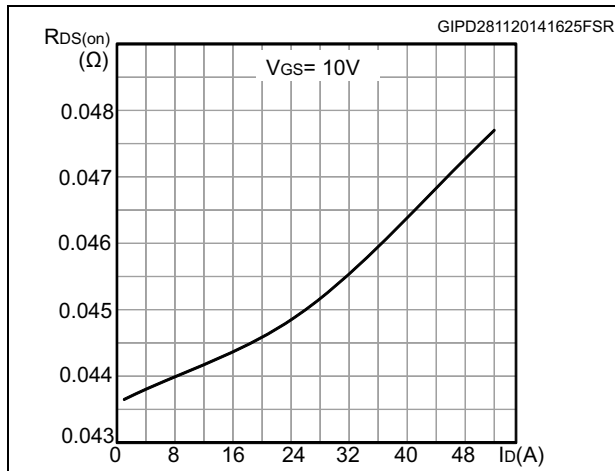


Figure 9. Normalized on-resistance vs. temperature

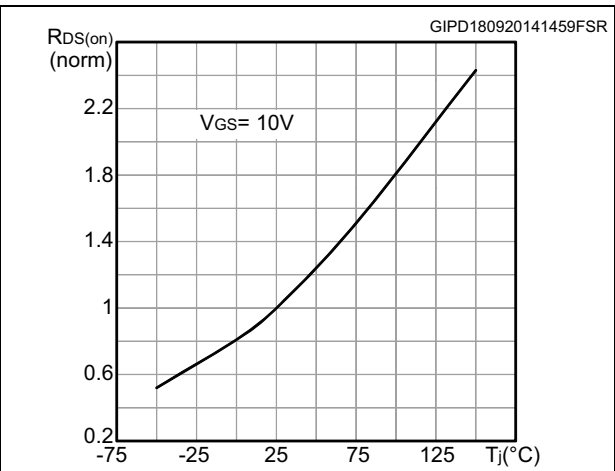


Figure 10. Gate charge vs. gate-source voltage

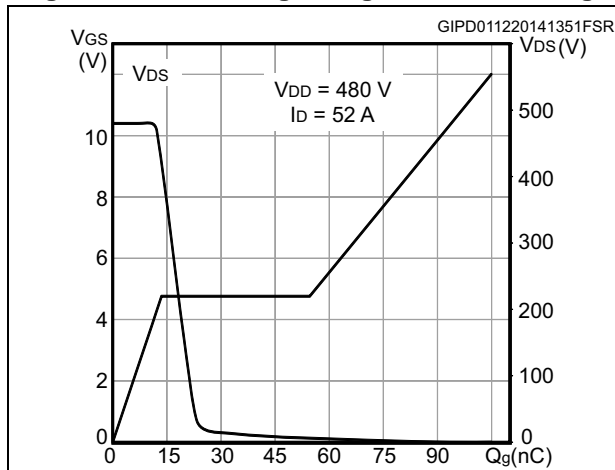


Figure 11. Capacitance variations

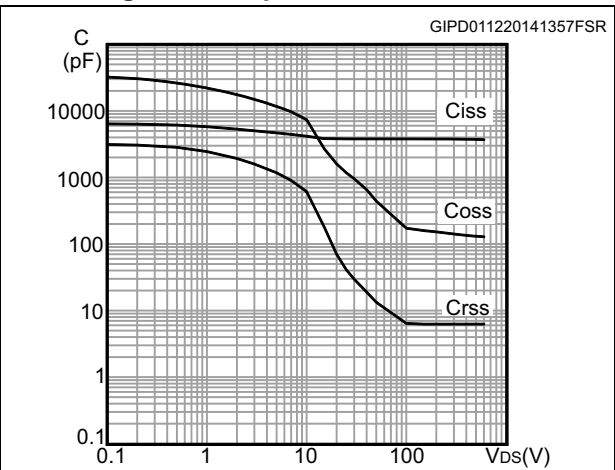


Figure 12. Output capacitance stored energy

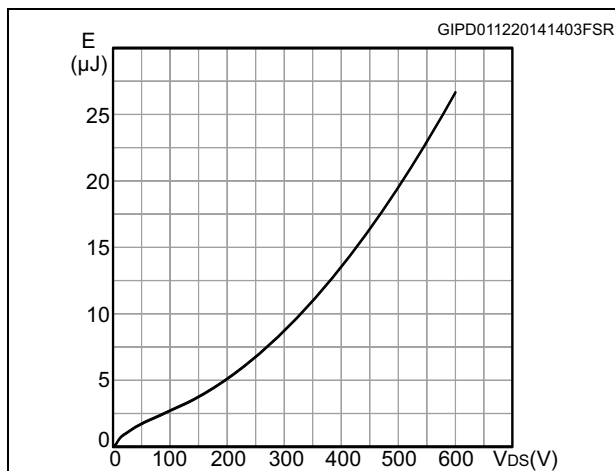
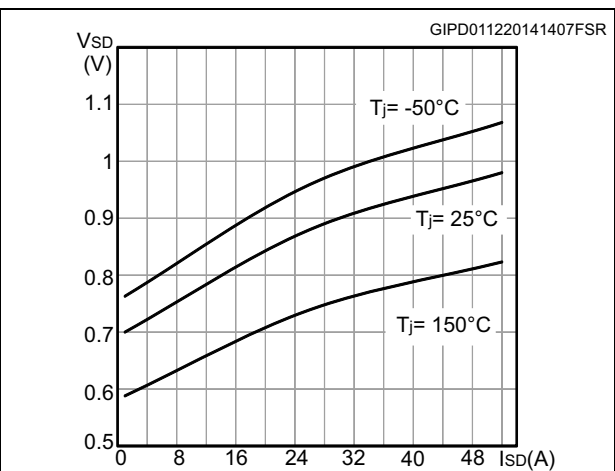


Figure 13. Source-drain diode forward characteristics



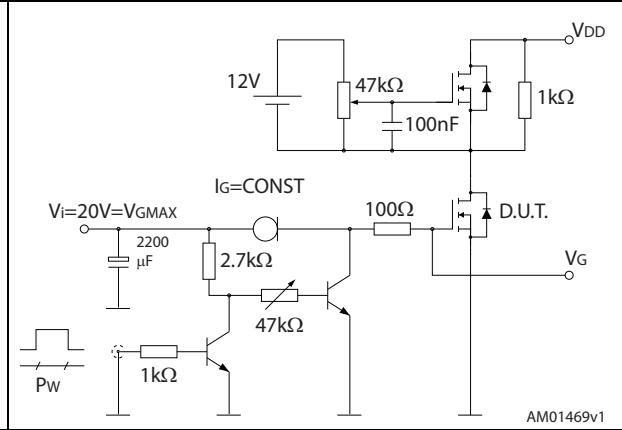
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



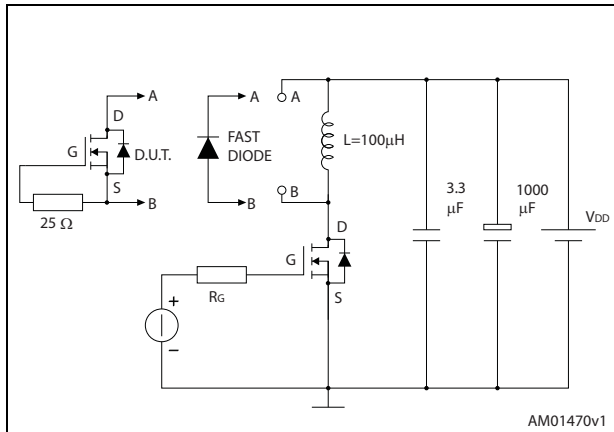
AM01468v1

**Figure 15. Gate charge test circuit**



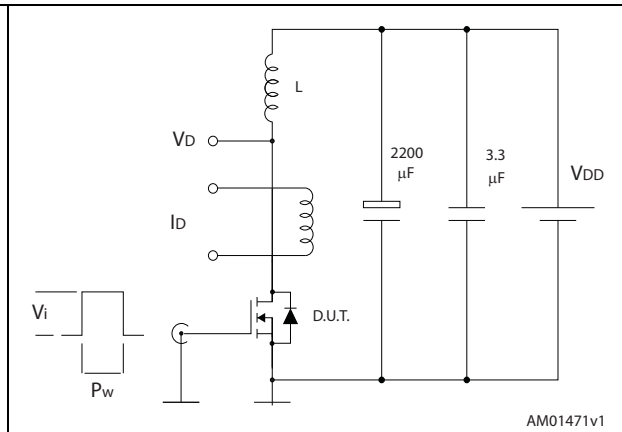
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**



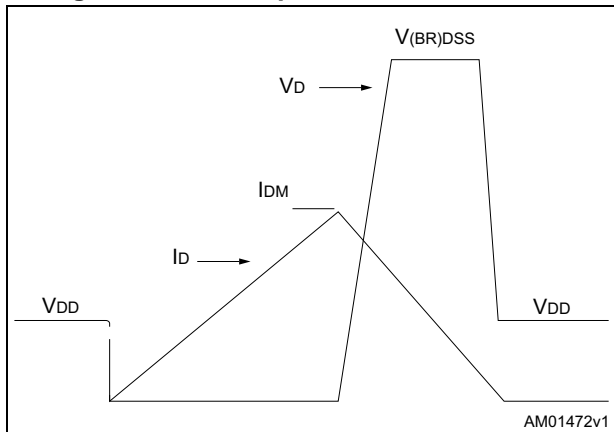
AM01470v1

**Figure 17. Unclamped inductive load test circuit**



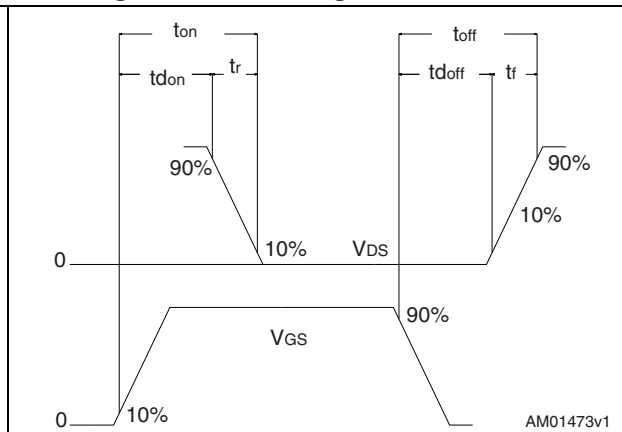
AM01471v1

**Figure 18. Unclamped inductive waveform**



AM01472v1

**Figure 19. Switching time waveform**



AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 20. TO-247 drawing

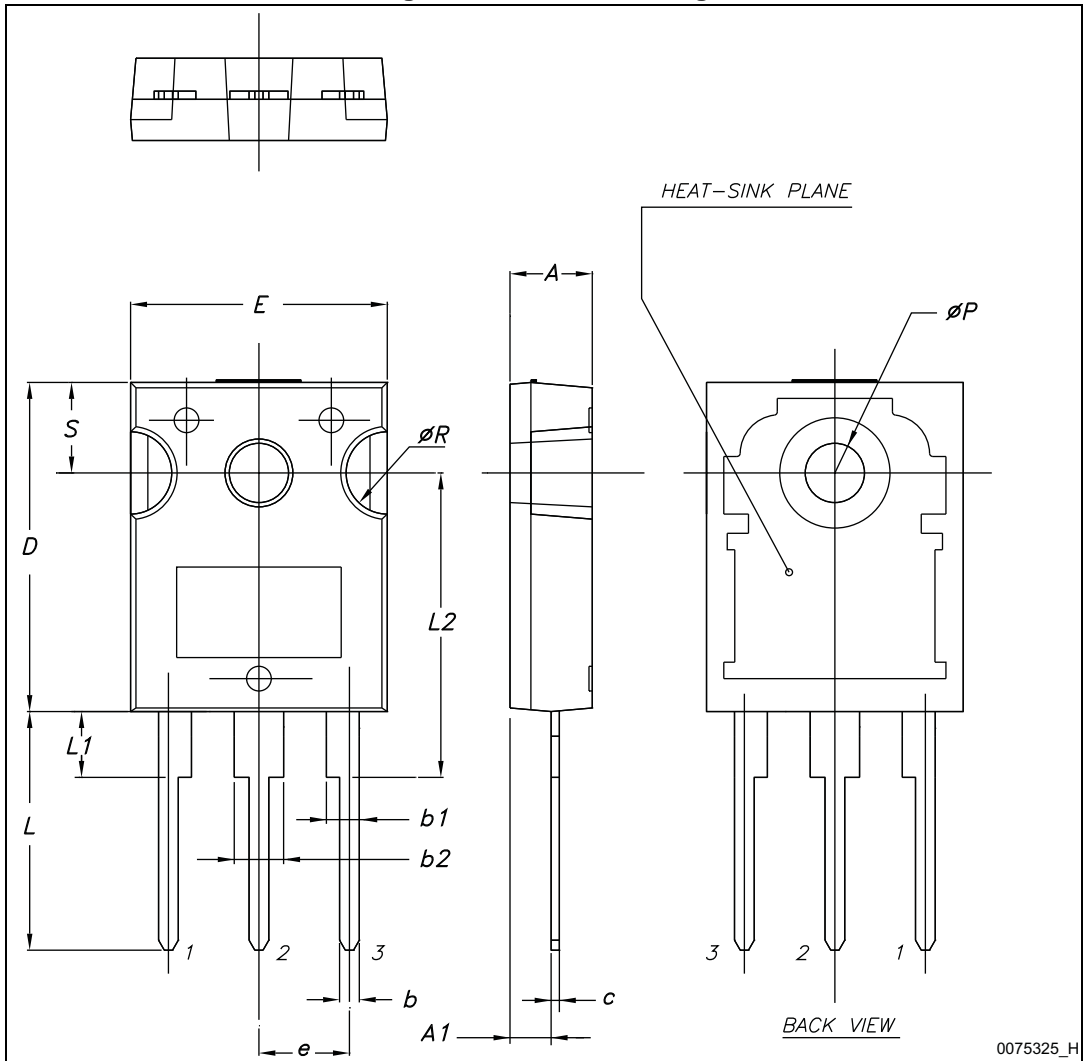


Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Dec-2014	1	Initial release.
10-Dec-2014	2	Updated <a href="#">Section 3: Test circuits</a> .

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved