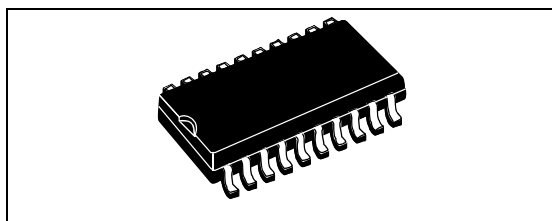


## I<sup>2</sup>C bus-controlled video matrix switch

### Features

- 20 MHz bandwidth
- Cascadable with another STV6415A (internal address can be changed by pin 7 voltage)
- Eight inputs (CVBS, RGB, Chroma, ...)
- Six outputs
- Possibility of chroma signal for each input by switching off the clamp with an external resistor bridge
- I<sup>2</sup>C bus-controlled
- 6.5 dB gain between any input and output
- -55 dB crosstalk at 5 MHz
- Full ESD protection



### Description

The main function of the STV6415A is to switch eight video input sources on the six outputs.

Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs.

All switching possibilities are controlled through the I<sup>2</sup>C bus.

**Table 1. Device summary**

Order code	Packaging
STV6415AB	SO 20 Plastic small outline package

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# 1 General description

Figure 1. STV6415A Pin-out diagram

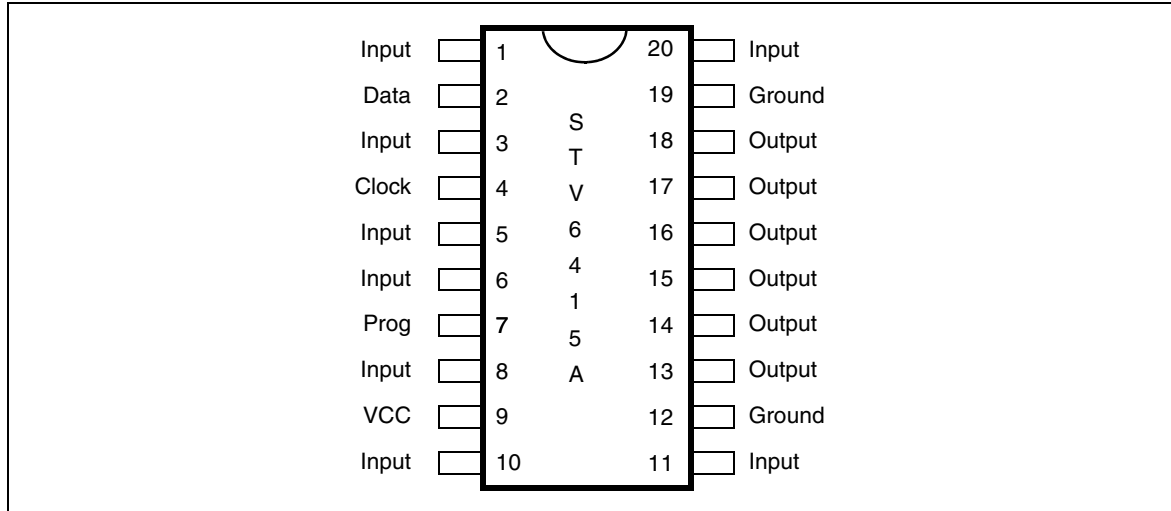
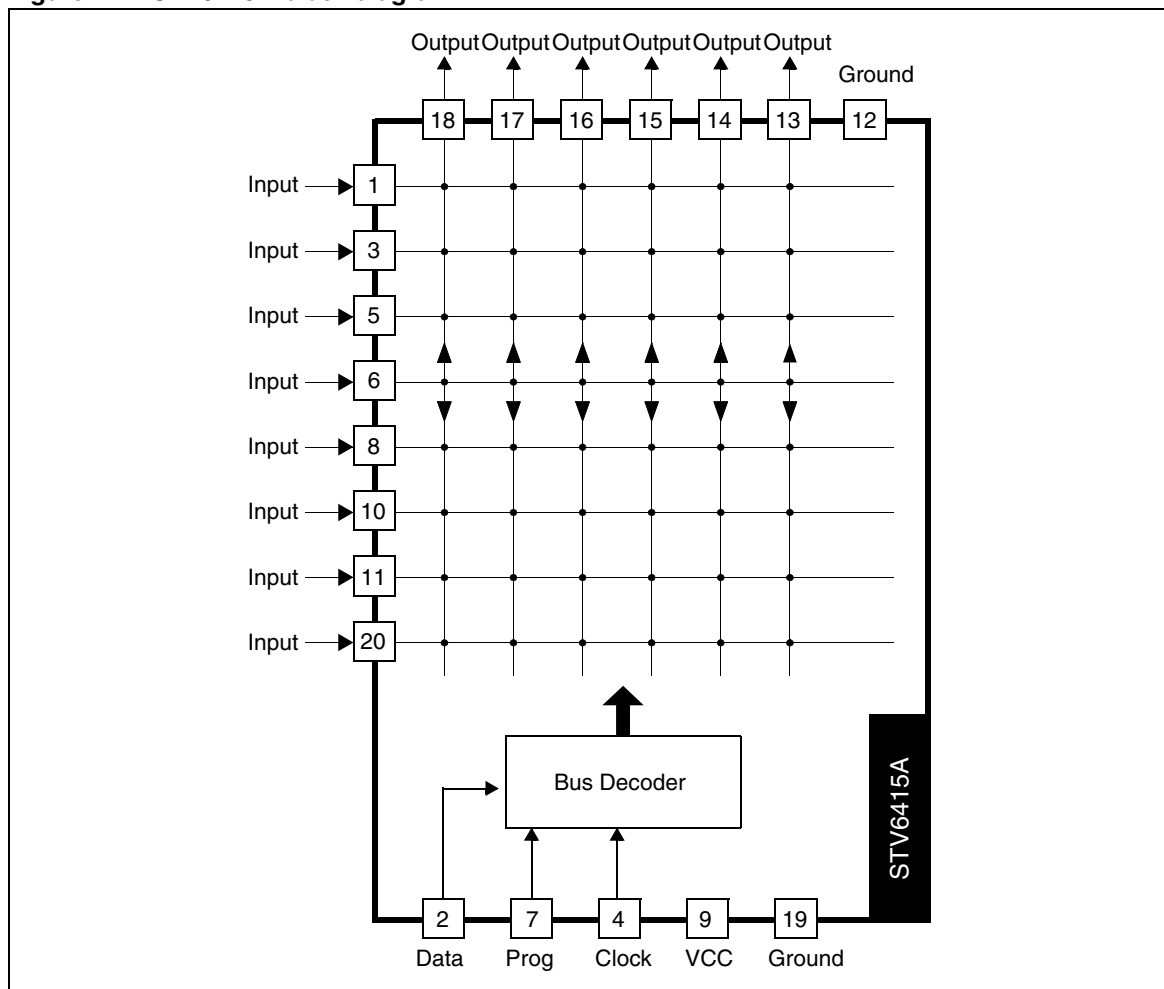


Figure 2. STV6415A block diagram



The main function of the STV6415A is to switch eight video input sources on the six outputs. Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs. The lowest level of each signal is aligned on each input (bottom of sync pulse for CVBS or Black Level for RGB signals).

The nominal gain between any input and output is 6.5 dB. For Chroma signals, the alignment is switched off by forcing, with an external 5 V<sub>DC</sub> resistor bridge on the input. Each input can be used as a normal input or as a Chroma input (with external resistor bridge). All the switching possibilities are changed through the I<sup>2</sup>C bus.

Driving a 75 Ω load requires an external transistor.

The switch configuration is defined by words of 16 bits: the I<sup>2</sup>C address (8 bits) then one output configuration (8 bits). Therefore, six separated words of 16 bits are necessary to determine the starting configuration at power-on (power supply: 0 to 10 V).

A new configuration needs only the words (16 bits) of the changed output channels.

## 2 Electrical characteristics

### 2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage (pin 9)	12	V
$T_A$	Operating ambient temperature range	0 to +70	°C
$T_{STG}$	Storage temperature range	-20 to +150	°C

### 2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}$	Junction-to-ambient thermal resistance SO20	100	°C/W

### 2.3 Electrical characteristics

( $T_A = 25\text{ °C}$ ,  $V_{CC} = 10\text{ V}$ ,  $R_{LOAD} = 10\text{ k}\Omega$ ,  $C_{LOAD} = 3\text{ pF}$  (unless otherwise specified))

Table 3. Electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply voltage (pin 9)	8	10	11	V
$I_{CC}$	Power supply current (without load on outputs; $V_{CC} = 10\text{ V}$ )	14	19	25	mA
<b>Inputs</b>					
	Signal amplitude (CVBS signal)			2	$V_{PP}$
	Input current (input voltage = $5 V_{DC}$ )		1	3	$\mu\text{A}$
	DC level	3.3	3.6	3.9	V
	DC level shift (temperature from 0 to 70°C)		5	100	mV
<b>Outputs</b> ( $V_{IN} = 1 V_{PP}$ for all dynamic tests) Pins 13,14, 15, 16, 17 and 18					
	Dynamic	4.5	5.5		$V_{PP}$
	Output impedance		25	50	$\Omega$
	Gain	6	6.5	7	dB
	Bandwidth	7	15 20		MHz
	Crosstalk		-60 -55	-50 -45	dB
			$f = 3.58\text{ MHz}$ $f = 5\text{ MHz}$		

Table 3. Electrical characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	DC Level	2.40	3.05	3.50	V
	Minimum output load ( $R_{LOAD}$ )	2			k $\Omega$

## 2.4 I<sup>2</sup>C bus characteristics

( $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 10\text{ V}$ )

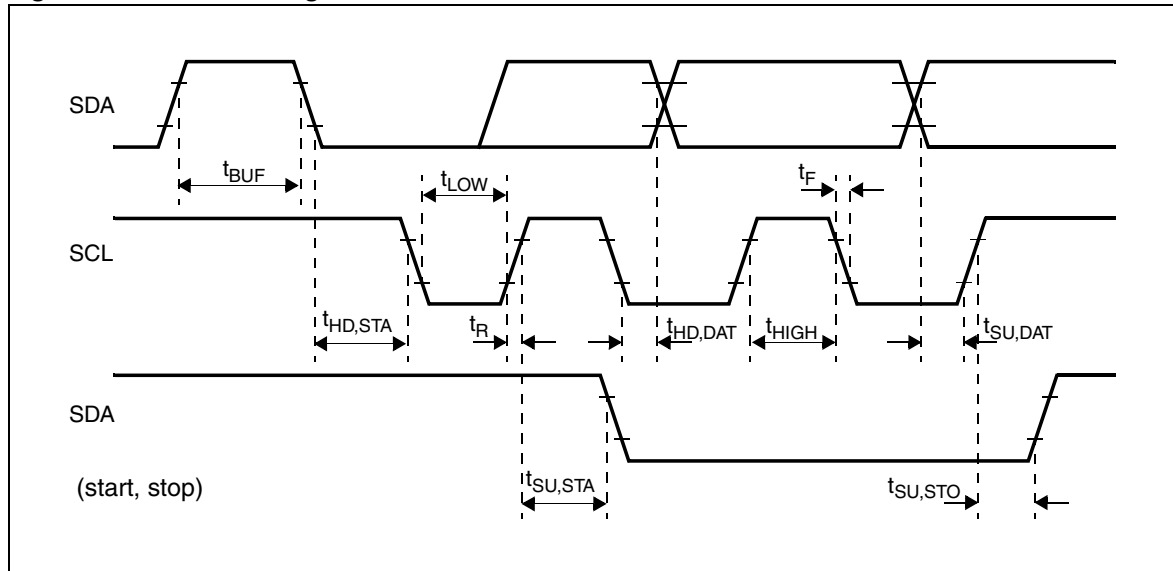
Table 4. I<sup>2</sup>C bus characteristics

Symbol	Parameter	Test conditions	Min.	Max.	Unit
<b>PROG (pin 7)</b>					
	Threshold voltage (typical value is 1.3)		1.00	1.65	V
<b>SCL (pin 4)</b>					
$V_{IL}$	Low level input voltage		-0.3	+1.0	V
$V_{IH}$	High level input voltage		2.3	$V_{CC} + 0.3$	V
$I_{LI}$	Input leakage current	$V_I = 0\text{ to }V_{CC}$	-10	+10	$\mu\text{A}$
$f_{SCL}$	Clock frequency		0	100	kHz
$t_R$	Input rise time	1.5 V to 3 V		1000	ns
$t_F$	Input fall time	3 V to 1.5 V		300	ns
$C_I$	Input capacitance			10	pF
<b>SDA (pin 2)</b>					
$V_{IL}$	Low level input voltage		-0.3	+1.0	V
$V_{IH}$	High level input voltage		2.3	$V_{CC} + 0.3$	V
$I_{LI}$	Input leakage current	$V_I = 0\text{ to }V_{CC}$	-10	+10	$\mu\text{A}$
$C_I$	Input capacitance			10	pF
$t_R$	Input rise time	1.5 V to 3 V		1000	ns
$t_F$	Input fall time	3 V to 1.5 V		300	ns
$V_{OL}$	Low level output voltage	$I_{OL} = 3\text{mA}$		0.4	V
$t_F$	Output fall time	3 V to 1.5 V		250	ns
$C_L$	Load capacitance			400	pF
<b>Timing</b>					
$t_{LOW}$	Clock low period		4.7		$\mu\text{s}$
$t_{HIGH}$	Clock high period		4.0		$\mu\text{s}$
$t_{SU, DAT}$	Data set-up time		250		ns
$t_{HD, DAT}$	Data hold time		0	340	ns
$t_{SU, STO}$	Set-up time from clock high to stop		4.0		$\mu\text{s}$

**Table 4. I<sup>2</sup>C bus characteristics (continued)**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
t <sub>BUF</sub>	Start set-up time following a stop		4.7		μs
t <sub>HD, STA</sub>	Start hold time		4.0		μs
t <sub>SU, STA</sub>	Start set-up time following clock low-to-high transition		4.7		μs

**Figure 3. I<sup>2</sup>C bus timing**



## 2.5 I<sup>2</sup>C bus selections

The I<sup>2</sup>C chip address is defined by the first byte. The second and following bytes define the input/output configurations.

**Table 5. First byte (address)**

0x86	0b1000 0110	When PROG pin is connected to Ground
0x06	0b0000 0110	When PROG pin is connected to V <sub>CC</sub>

## 2.5.1 Second and following bytes (input/output selection)

**Table 6. I<sup>2</sup>C bus output selections**

Output address (MSB)	Input address (LSB)	Selected output	
00000	XXX	Pin 18	Output is selected by the 5 MSBs.
00100	XXX	Pin 14	
00010	XXX	Pin 16	
00110	---	Not used	
00001	XXX	Pin 17	
00101	XXX	Pin 13	
00011	XXX	Pin 15	
00111	---	Not used	

**Table 7. I<sup>2</sup>C bus input selections**

Output address (MSB)	Input address (LSB)	Selected input	
00XXX	000	Pin 5	Input is selected by the 3 LSBs.
00XXX	100	Pin 8	
00XXX	010	Pin 3	
00XXX	110	Pin 20	
00XXX	001	Pin 6	
00XXX	101	Pin 10	
00XXX	011	Pin 1	
00XXX	111	Pin 11	

**Example:** 00100 101 connects pin 10 (input) to pin 14 (output) (equals 25 in hexadecimal)



## 2.6 Input/output pin configurations

Figure 4. Input configuration

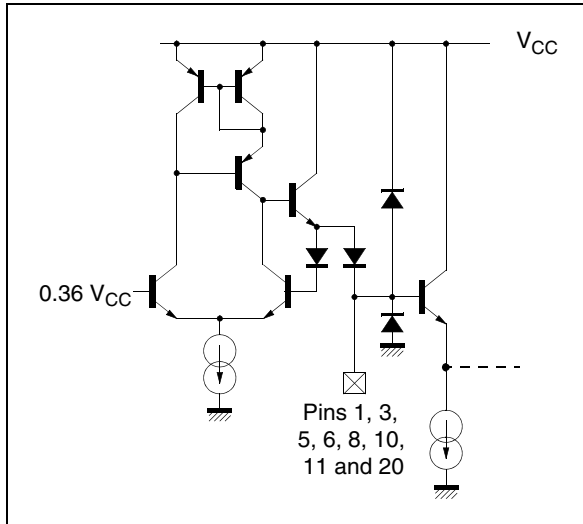


Figure 5. Output configuration

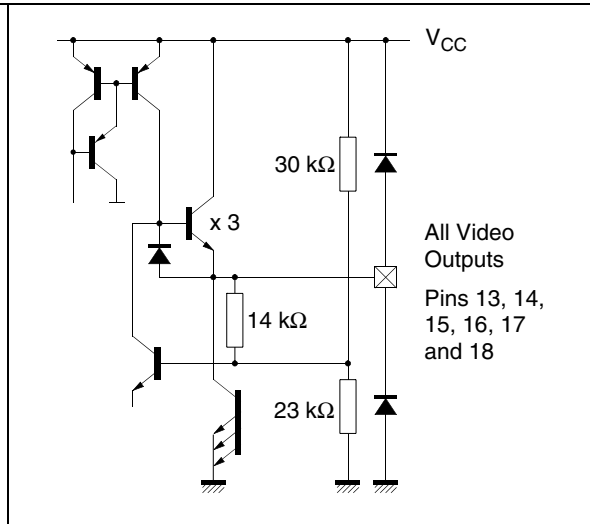


Figure 6. Bus I/O configuration

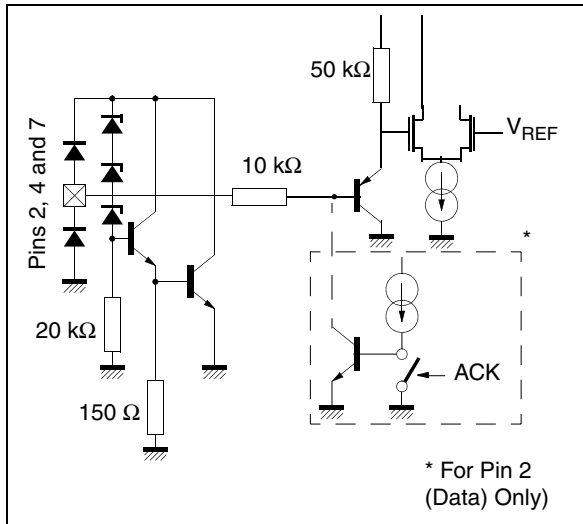
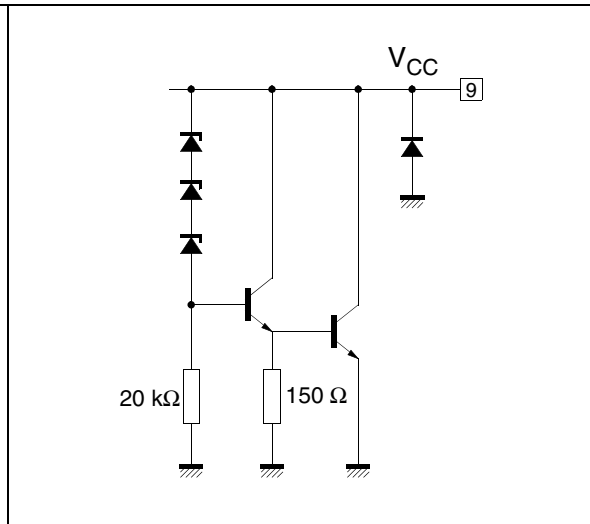


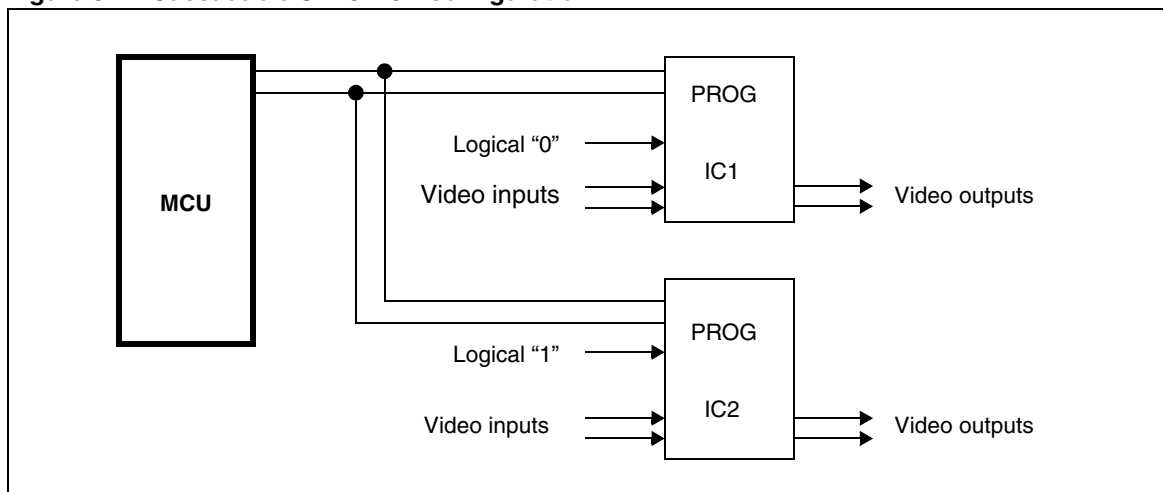
Figure 7. VCC pin configuration



## 2.7 Using a second STV6415A

The programming input pin (PROG) allows two STV6415A circuits to operate in parallel, and to select them independently through the I<sup>2</sup>C bus by modifying the address byte. Consequently, the switching capabilities are doubled, or IC1 and IC2 can be cascaded.

Figure 8. Cascadable STV6415A configuration

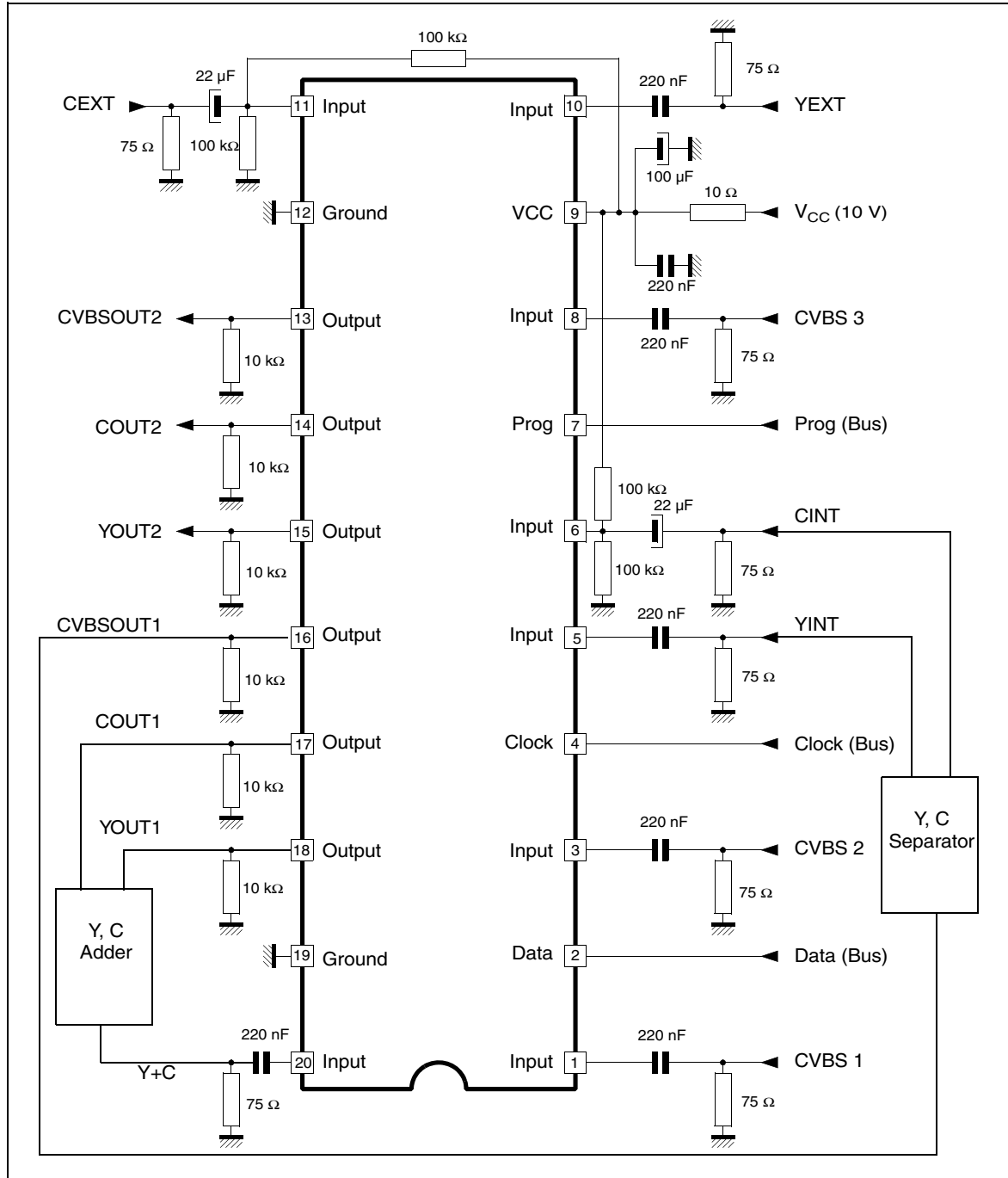


## 2.8 Application diagram

Whenever an input is not used, it must be bypassed to ground through a 220 nF capacitor.

*Note: The application diagram presented here is an example only and is subject to change without notice. The real application diagram will depend on application conditions and constraints.*

**Figure 9. Application diagram**



### 3 Package mechanical data

Figure 10. 20-pin plastic SO (small outline) package, 300-mil width

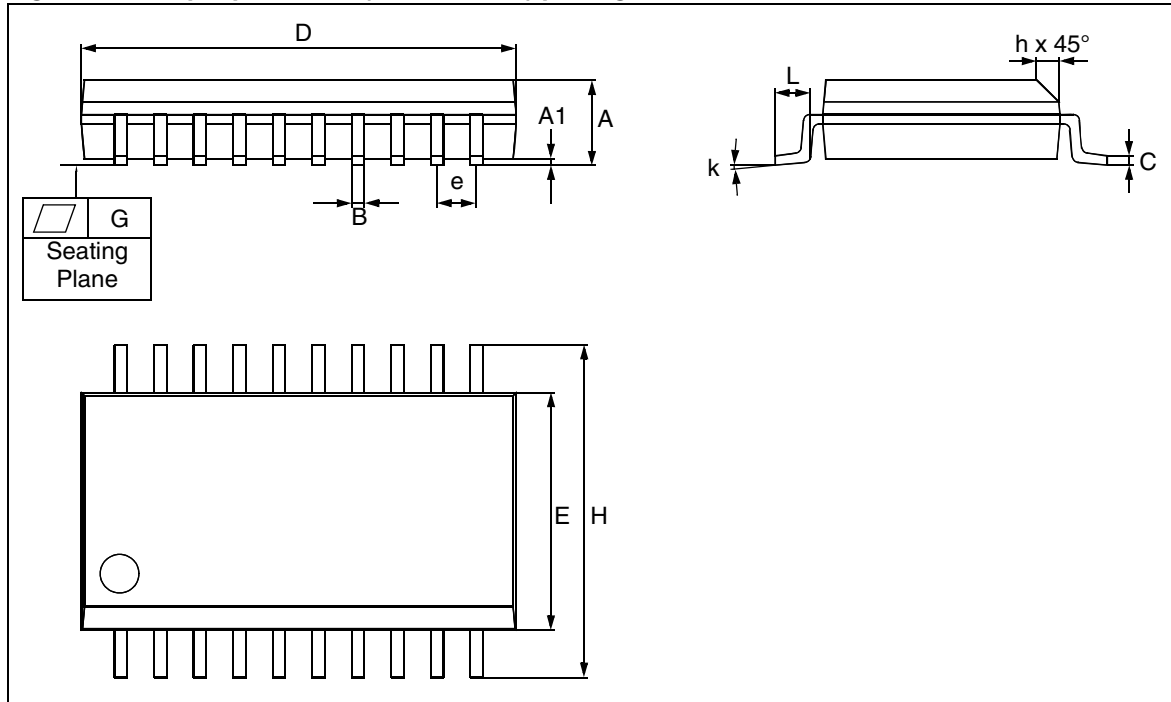


Table 8. SO20 package

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.0926		0.1043
A1	0.10		0.30	0.0040		0.0118
B	0.33		0.51	0.0130		0.0200
C			0.32			0.0125
D	12.60		13.00	0.4961		0.5118
E	7.40		7.60	0.2914		0.2992
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.74	0.010		0.029
k	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
G			0.10			0.004
	Number of pins					
N	20					

### 3.1 Environmental

In order to meet environmental requirements, STMicroelectronics offers the STV6415A in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at [www.st.com](http://www.st.com).

The ECOPACK version can be identified by the letter 'E' beside the ST logo. Both types are compatible with ROHS.

## 4 Document revision history

Table 9. Document revision history

Date	Revision	Changes
28-Aug-2008	1	Initial Release

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